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Integration Platform for Tunable Carbon Nanotube Electromechanical Resonators

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If you are a superman, you don’t need to swing like a spiderman. What you need to do is fly freely in the air. Be your superman.

My life reminder

Abstract

Carbon nanotubes (CNTs) possess several outstanding material properties, such as high stiffness, light weight, and one-dimensional structures. These are key factors for high resonant frequency of a vibration structure. Hence, CNTs are promising nano-materials for high frequency resonators. Moreover, the already high resonant frequency of a suspended CNT can be further increased by applying strain. Micro-actuation by a MEMS actuator can reduce the slack of the suspended CNT and increase strain upon the CNT, which enables a broad tunable frequency range from MHz to GHz. In this study, a scalable CNT-MEMS integration platform was developed, and the first tunable CNT resonator with an embedded MEMS actuation system was demonstrated.

To integrate a low-defect suspended CNT into a pre-defined MEMS actuator, a fabrication process has been developed. Using top-down micro-machining, a temporary supporting structure is fabricated so as to avoid physical rupture of suspended CNTs during wet processing. In addition, an Al_2O_3 layer is deposited by atomic layer deposition (ALD) to protect as-grown CNTs from resist contamination during post-growth processing. The post-growth wet processing enables the metallization on top of as-grown CNTs by lift-off. The patterned metals provide improved electrical contacts and robust doubly-clamped configuration. Based on the developed integration process, the influence of processing conditions on CNT performance and the long-term stability of device resistance were investigated.

To adjust the strain on the integrated CNT, a micro-actuation system was designed. The system was driven by an electro-thermal bent-beam actuator. To avoid electrical and thermal interferences between the actuator and CNT device, an insulation mechanical configuration, called adapter, was designed. This adapter is compact, and it consists of only two discrete silicon structures. More importantly, it can be fabricated using the developed integration process. This adapter can electro-thermally insulate the CNT from the actuator, while the CNT is strained by the actuator. Hence, the investigation the CNT electrical response to strain is possible.

The entire integrated CNT-MEMS device, including. a suspended CNT, an adapter, and a thermal actuator, can be fabricated using the developed integration process. The functionality of the fabricated CNT-MEMS device was first verified by quasi-static

electromechanical loading tests. The electrical current variations of the strained CNTs were measured during the tensile tests. The reproducible and reversible strain-induced current modulation of the tested CNTs confirms the device functionality. In the final dynamic characterization, the resonant frequency of the suspended CNT was tuned by driving the actuator. The frequency modulation mechanism was attributed to the reduction of the slack of the CNT. This demonstrates a tunable CNT resonator and confirms the capability of the integration platform.

Zusammenfassung

Kohlenstoffnanoröhren (CNTs) besitzen viele herausragende Materialeigenschaften, wie z.B. hohe Steifigkeit, geringes Gewicht und eine eindimensionale Struktur. Diese sind Schlüsselfaktoren für hohe Resonanzfreqenzen einer schwingenden Struktur. Daher sind CNTs vielversprechende Nanomaterialien für Hochfrequenzresonatoren. Ausserdem kann die Resonanzfrequenz einer freihängenden CNT durch Dehnung noch weiter erhöht werden. Mikroaktuation durch einen MEMS-Aktuator kann den Durchhang der freihängenden CNT verringern und die mechanische Spannung erhöhen, wodurch ein breit einstellbarer Frequenzbereich von MHz bis GHz ermöglicht wird. In dieser Studie wurde eine skalierbare CNT-MEMS Integrationsplattform entwickelt und der erste einstellbare CNT-Resonator mit integriertem MEMS-Aktuationssystem demonstriert.

Ein Integrationsprozess wurde entwickelt, um eine frei hängende CNT niedriger Defektdichte in einen MEMS-Aktuator zu integrieren. Unter Verwendung von Top-down-Mikrofabrikation wird eine temporär stützende Struktur hergestellt, die ein Reissen der freihängenden Struktur während der Nassprozessierung verhindert. Zusätzlich wird eine Al2O3-Schicht durch Atomlagenabscheidung aufgebracht, um die gewachsenen CNTs während der Prozessierung nach dem Wachstum vor Kontamination mit Photolack zu schützen. Die Nassprozessierung nach dem Wachstum ermöglicht die Metallisierung auf CNTs durch ein Lift-off-Verfahren. Die oben aufgebrachte Metallisierung bietet verbesserte elektrische Kontakte und eine robuste, beidseitig geklemmte Konfiguration. Unter Verwendung des entwickelten Integrationsprozesses wurden der Einfluss von Prozessschritten auf die Betriebseigenschaften der CNTs und die Langzeitstabilität des Bauteilwiderstands untersucht.

Um die Dehnung der integrierten CNT einstzustellen, wurde ein Mikroaktuationssystem entworfen. Das System wird durch einen auf gebogenen Balken basierenden elektrothermischen Aktuator angetrieben. Um elektrische und thermische Störeinflüsse zwischen dem Akutator und dem CNT Bauteil zu vermeiden, wurde ein isolierender mechanischer Aufbau, im Folgenden „Adapter“ genannt, entworfen. Dieser Adapter ist kompakt und besteht aus lediglich zwei separaten Siliziumstrukturen. Insbesondere kann er mit dem entwickelten Integrationsprozess hergestellt werden. Der Adapter kann die CNT elektrothermisch vom Aktuator isolieren, während die CNT durch den Aktuator gedehnt wird. Dies ermöglicht die Untersuchung der elektrischen Antwort der CNT auf Dehnung.

Das gesamte integrierte CNT-MEMS-Bauteil, das eine freistehende CNT, einen Adapter und einen thermischen Aktuator beinhaltet, kann mit dem entwickelten Integrationsprozess hergestellt werden. Die Funktionalität des gesamten CNT-MEMS-Bauteils wurde zuerst durch quasistatische elektromechanische Zugtests überprüft. Die Änderungen des elektrischen Stroms in den gedehnten CNTs wurden während des Zugtests gemessen. Die reproduzierbare und reversible durch Dehnung verursachte Strommodulation der getesteten CNTs bestätigt die Funktionalität der Bauteile. Bei der abschliessenden dynamischen Charakterisierung wurde die Resonanzfrequenz der freihängenden CNT durch den Aktuator eingestellt. Der Frequenzmodulationsmechanismus wurde zurückgeführt auf die Reduktion des Durchhangs der CNT. Somit wurde ein einstellbarer CNT-Resonator demonstriert und die vollständige Entwicklung der Integrationsplattform nachgewiesen.

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This work has been performed ten thousand kilometers away from home. I would like to thank my family, 李林阿花, 李金德, 曾粉妹, 李嘉蕙, 楊明勳, 楊謹謙, for being patient and enduring my absence in the past six year. Last but not the least; I want to say thank you

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List of symbols and SI units

Symbol	SI unit	Description
AF		Amplification factor of a bent beam
A_{ib}	[m^2]	Cross-section area of an inclined beam
A_{cnt}	[m^2]	Cross-section area of a CNT
E_{cnt}	[Pa]	Young's modulus of CNT
E_{Si}	[Pa]	Young's modulus of Si
$F_{Buckle,sb}$	[N]	Buckling force of a suspension beam
$F_{Buckle,ib}$	[N]	Buckling force of an inclined beam
F_{ext}	[N]	External force loading on a bent-bent actuator
F_{axial}	[N]	Axial force in a CNT
$f_{F_{axial}}$	[Hz]	Resonant frequency of a CNT strained by an axial force, F_{axial}
I_d	[A]	Drain current of a CNTFET
I_a	[A]	Electrical current passing through an actuator
I_{cnt}	[A]	Electrical current passing through a CNT
I_{sb}	[m^4]	Area moment of inertia of a suspension beam
k	[m^2·kg/s]	Planck constant (=6.626×10^{-34})
l_{sb}	[m]	Length of a suspension beam
l_{ib}	[m]	Length of an inclined beam
L_{cnt}	[m]	Length of a CNT
$I_{m,cnt}$	[m^4]	Area moment of inertia of a cylindrical CNT
n		Number of bent beam pairs in a thermal actuator
R_m	[Ω]	Measured device resistance of a CNTFET
R_c	[Ω]	Electrical contact resistance of a CNTFET
R_{cnt}	[Ω]	CNTFET channel resistance
R_0	[Ω]	A curve fitting resistance of the maximum resistance versus strain
R_1	[Ω]	A curve fitting resistance of the maximum resistance versus strain
R_x^M	[N]	Reaction force in x-direction at the end of an inclined beam
$R_x^{M,\Delta T}$	[N]	Reaction force of an incline beam caused by thermal expansion
$R_x^{M,\sigma_{res}}$	[N]	Reaction force of an incline beam caused by residual stress
$R_x^{M,F_{ext}}$	[N]	Reaction force of an incline beam caused by an external force loading
S		Slack of CNT

Symbol	SI unit	Description
T	[K]	Temperature
t	[m]	Thickness
$u_{y,f}$	[m]	Free displacement (without force output) of a bent beam
u_y^M	[m]	Displacement at point M in y direction
V_a	[V]	Actuation voltage
V_{gd}^{ac}	[V]	AC gate voltage
V_{gd}^{dc}	[V]	DC gate voltage
V_{sd}^{ac}	[V]	AC source-drain voltage
V_{gd}^{dc}	[V]	DC gate voltage
α_{si}	[1/K]	Thermal expansion coefficient of Si
β		A curve fitting value of the maximum resistance versus strain
ε		Strain
ε_{cnt}		CNT strain
σ_e	[Ω-cm]	Electrical resistivity
σ_{res}	[Pa]	Residual stress
θ	[Degree]	Inclined angle of an inclined beam
ΔT	[K]	Average temperature increase
ρ_{cnt}	[kg/m^3]	Mass density of CNT

List of abbreviations

Abbreviation	Full phrase
AFM	Atomic force microscopy
ALD	Atomic layer deposition
BHF	Buffered hydrofluoric acid
CNT	Carbon nanotube
CNTFET	Carbon nanotube field effect transistor
cCVD	Catalyzed chemical vapor deposition
MEMS	Micro electro-mechanical system
NMP	N-methylpyrrolidone (resist remover)
Poly-Si	Polycrystalline silicon
RIE	Reactive ion etching
SWNT	Single-walled carbon nanotube
SiNW	Silicon nanowire
sc-Si	Single-crystalline silicon
SOI	Silicon on insulator
SEM	Scanning electron microscopy
TEM	Transmission electron microcopy
TSV	Through silicon via
VHF	Vapor hydrofluoric acid

Contents

Chapter 1 Introduction

The advantages of miniaturization of electronics and transducers are smaller dimensions and lower power consumption. Micro-electro-mechanical systems (MEMS) is an example of the miniaturization trend of transducers. Micro-scaled sensors and actuators can be fabricated by top-down surface and bulk micromachining. While the device dimensions are further shrunk down to nano-scale, new synthesis methods of nano-structures provide alternative techniques to fabricate miniaturized devices. Carbon nanotubes (CNTs), explored in 1991 by Ijima [1], is an example of a nano-structure that is integrated into a device via a bottom-up approach. Carbon nanotubes exhibit outstanding material properties, and have drawn tremendous research attention. For example, the high on/off current ratio of CNT field effect transistors (CNTFET) makes it a promising electronic component for logic applications [2]. Additionally, the use of CNTs has been demonstrated in different applications [3], such as transducers and gas sensors.

1.1. Motivation

Among various types of applications, sensitive mass balance based on an electro-mechanical CNT resonator is of great interest [4]. As a vibrating structure, the high mechanical stiffness [5], light weight [6], and one-dimensional structure of a CNT raises the resonant frequency up to the GHz range [7]. In addition, the resonant frequency increases dramatically with a small axial force compared to the already high resonant frequency achieved by a non-strained CNT [8]. This is due to the transition from a beam vibration to a string vibration [9], and the extended elastic range of the CNTs. (<~5%) [10]. For example, the resonance frequency of a non-strained 2 µm long CNT is 10 MHz, and it can reach 1 GHz if a strain of 1.74% is applied. Due to the high gauge factor, the resonance can be measured by monitoring the piezoresistive current, which leads to higher signal to noise ratio drain current peaks at resonance compared to sensing by capacitive current [11]. These material properties have made CNTs a promising candidate for high frequency tunable resonators.

- **Comparison of material properties**

Another competitive nano-structure, silicon nano-wires (SiNW), also shows a great potential in high resonant frequency applications. A brief comparison of selected material

properties of CNT and SiNW is shown in Table 1-1. The Young's modulus of SiNW is size-dependent at nanometer scale. The gauge factor is dependent on the channel state. In the accumulation mode, the gauge factor is similar to that of bulk silicon; while in the depletion mode, the gauge factor is much higher by a factor of tens [12]. This increase in gauge factor is attributed to a strain-induced charge trapping change on the oxide-passivated surface, so-called giant piezoresistance effect [12, 13]. In addition to the material properties compared in Table 1-1, another advantage of CNT is the inert surface. The adsorption of oxygen can temporarily change the electronic properties of CNTs [14]. However, no additional oxide layer forms on the surfaces of CNTs. In the contrast, the surface of Si will acquire a thin native oxide layer (t_{ox}= 1~2 nm) in ambient air. This additional native oxide introduces tensile stress in SiNW [15] and subsequently influences the resonant frequency [16]. In summary, compared with SiNWs, CNTs have better properties for high frequency mechanical resonators.

Table 1-1 Comparison of the material properties of CNT and SiNW

	CNT	**SiNW**
Young's modulus	1 TPa [5, 17]	169 Gpa (t_{si}= 300 nm) [18] 53 GPa (t_{si}= 12 nm) [18]
Mass density	1340 Kg/m^3[6]	2300 Kg/m^3
Fracture strain	5.3% [10] 13% [19]	6% (t_{si}= 100~200 nm) [20] 30% (t_{si}= 5~20 nm) [21]
Gauge factor	1000 [22] 2900 [23]	67 [12] 1806 [12]

- **Integration of on-chip actuation**

A common resonant frequency tuning method of a CNT resonator is to introduce an electrostatic force by a gate electrode [24]. The suspended CNT deforms laterally, resulting in resonant frequency modulation. In this configuration, there is no movable structure on the chip, except for the suspended CNT. Hence, slack is determined once the fabrication process is completed. Slack refers to the length of a CNT which is in excess of the straight line distance between its two clamping sites. If slack is involved in the vibration, it

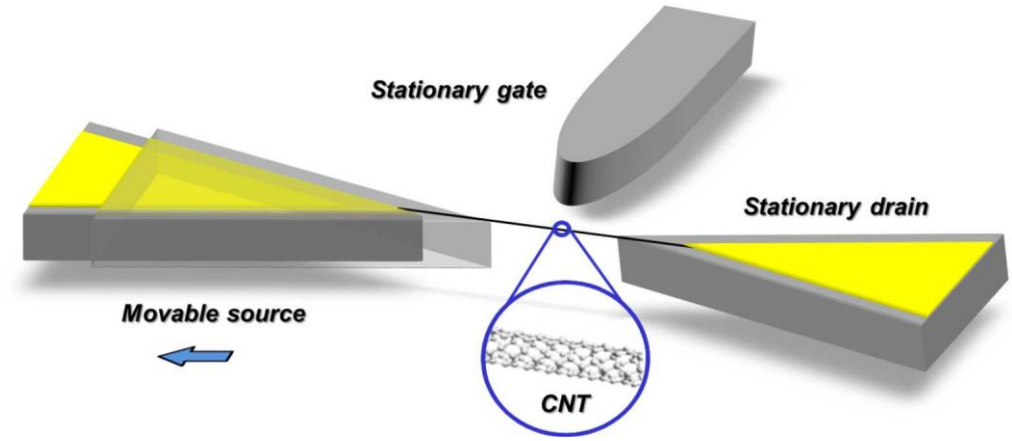


Figure 1-1 Schematic sketch of an integrated CNT-MEMS device.

introduces additional out-of-excitation-plane modes [25], and the analysis becomes more complicated. This situation can be remedied by on-chip actuation. A precision MEMS actuator can reduce the slack of a suspended CNT, and a slack-free CNT resonator can be achieved. Moreover, the embedded actuator can adjust the axial strain of the suspended CNT. The actuation force of a MEMS actuator (~μN) is much larger than the axial strain induced by the electrostatic force (~40 pN if gate distance= 1 μm and gate voltage= 1 V). This can achieve a larger tunable range of the CNT resonant frequency.

1.2. Objectives

The research goal of this thesis was the development of a process flow for the integration of suspended CNTs and MEMS actuators. The final process is expected to fabricate high quality integrated CNT-MEMS devices, which can fulfill the following requirements:

- low-defect, clean suspended CNTs
- reliable electrical contacts of the integrated CNTs
- robust mechanical clamping of the suspended CNTs
- simultaneous and independent operation of the CNT and MEMS components

A conceptual device is shown in Figure 1-1. A CNT is suspended between a stationary drain electrode and a movable source electrode (driven by an actuator). The suspended CNT is clamped by a top metal layer. This metal layer provides improved electrical contacts and mechanical clamping. A side-gate electrode is employed to bias the CNTFET and excite the suspended CNT into vibration at the same time.

1.3. Contents of chapters

The major part of this thesis is the development of the integration process. The contents of each chapter are listed below:

Chapter 2: The state-of-the-art fabrication processes for suspended CNTs are briefly reviewed.

Chapter 3: The development of the CNT-MEMS integration process flow is described in detail. The process flow was developed on silicon-on-insulator (SOI) chips. The integration process of SOI and CNTs is abbreviated to SOIC. The development began with the integration of suspended CNTFETs into predefined stationary Si micro-structures (SOIC2 and SOIC3 shown in Table 1-2). The two key features of SOIC, a supporting oxide bridge and a protective Al_2O_3 layer, were developed to enable post-growth wet processing and to eliminate contamination of resist during lithography. A CNT selection method was explored to improve orientation control of integrated CNTs. It can improve the device yield by 6 times. In this chapter, the development of the selected process steps is discussed. Using the fabricated devices, the influence of liquid HF etching on the metal contacts and the long-term device stability were investigated.

Chapter 4: The design parameters of MEMS electro-thermal actuators are discussed. In addition, a compact and versatile mechanical structure was introduced to make the integrated CNT and MEMS actuator to be simultaneously and independently operational.

Chapter 5: Using the integrated CNT-MEMS devices, electro-mechanical loading tests were performed. The preliminary results verified the functionality of the CNT-MEMS device. Moreover, a tunable CNT resonator was demonstrated with the embedded MEMS actuation system.

Chapter 6: The achievements of this thesis are summarized. The developed integration process is compared with state-of-the-art integration processes.

An overview of the development of the integration process and the structure designs is listed in Table 1-2. Note that the first design layout, SOIC1, was used to evaluate different potential integration approaches, and no working CNT devices were fabricated. Hence, SOIC1 is not included in this table.

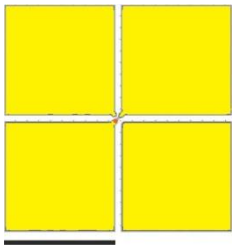
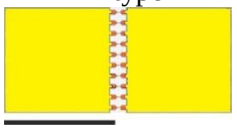
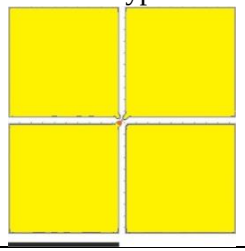
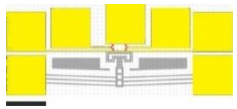
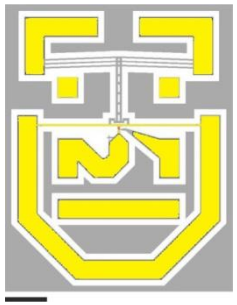
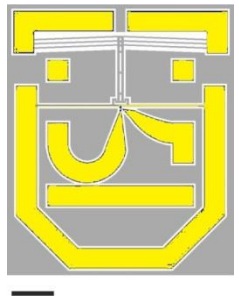
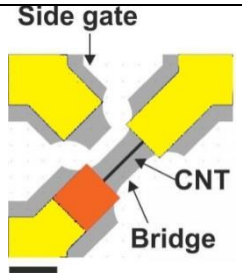
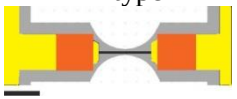
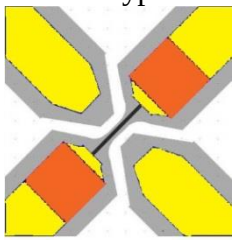
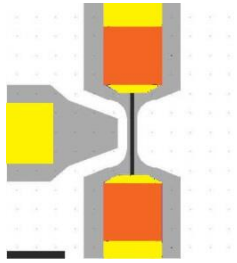
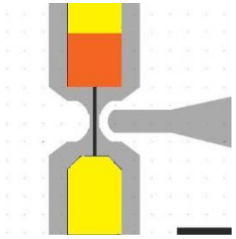
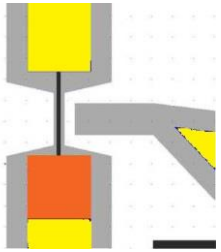
Table 1-2 Development of the integration process and design layout

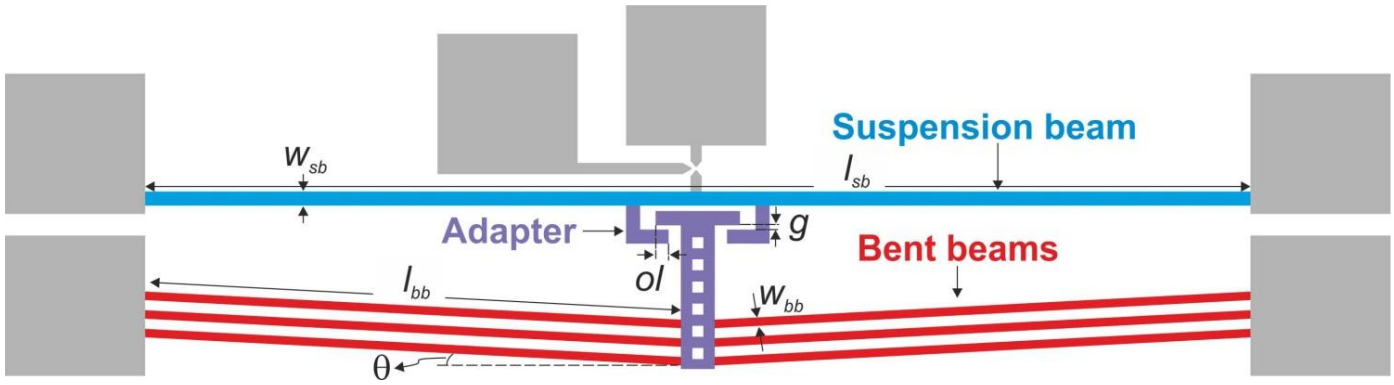
Subject \ Layout		SOIC2	SOIC3	SOIC4	SOIC4s	SOIC5
SOI wafer	Device layer	t_{device}=5 μm ρ=0.005-0.05 Ω-cm	t_{device}=5 μm ρ=0.005-0.05 Ω-cm	t_{device}=5 μm ρ<0.01 Ω-cm	t_{device}=5 μm ρ<0.01 Ω-cm	t_{device}=5 μm ρ<0.01 Ω-cm
	BOX layer	t_{BOX}=2 μm	t_{BOX}=2 μm	t_{BOX}=1 μm	t_{BOX}=1 μm	t_{BOX}=1 μm
	Handle layer	T_{handle}=400 μm ρ=0.005-0.05 Ω-cm	T_{handle}=400 μm ρ=0.005-0.05 Ω-cm	T_{handle}=300 μm ρ>2500 Ω-cm	T_{handle}=300 μm ρ>2500 Ω-cm	T_{handle}=300 μm ρ>2500 Ω-cm
Process	Lithography-1 Si structures	UV	DUV	DUV	DUV	DUV
	DRIE	The Bosch process	The Bosch process	The Bosch process	The Bosch process	The Bosch process
	Oxide by wet thermal oxidation	t_{SiO2}=1.7 μm	t_{SiO2}=645 nm	t_{SiO2}=500 nm	t_{SiO2}=500 nm	t_{SiO2}=500 nm
	Polishing particles	Diamond particles	Silica particles	Silica particles	Silica particles	Silica particles
		[Investigation] Polishing by diamond and silica particles in Sec. 3.6.1with samples C#SOIC2-RTC1 / C#SOIC2-RTC2				
	Lithography-2 catalysts	UV	UV	UV	UV	UV
	Catalyst lift-off	Acetone	Acetone	Acetone & NMP	Acetone & NMP	Acetone & NMP
			[Investigation] Catalyst lift-off with additional NMP cleaning in Sec 3.6.2 with samples C#Ox1-C1 / C#Ox1-C2			
	CNT growth	Heat up in air 15 min growth	Heat up in air 15 min growth	Heat up in air 15 min growth	Heat up in air 30 min growth	Heat up in air 30 min growth
	Protective layer during lithography			ALD Al_2O_3	ALD Al_2O_3	ALD Al_2O_3
		[Investigation] The improved CNT cleanliness with ALD Al_2O_3 in Sec. 3.6.3 with samples C#SiN-C1 C#SiN-C2 D#20-5A_C#SOIC3-R3C2 D#21-7D_C#SOIC3-R5C1				

Subject \ Layout		SOIC2	SOIC3	SOIC4	SOIC4s	SOIC5
Process	Protective layer during lithography	**[Investigation]** The thickness of Al_2O_3 for the protection during oxygen plasma ashing in Sec. 3.6.4 with samples C#Ox2-C1 / C#Ox2-C2 / C#Ox2-C3				
	CNT selection					Oxygen plasma ashing
					[Investigation] Selective removal of CNTs by oxygen plasma ashing. In Sec. 3.6.4 with samples C#SOIC5-O2-C1	
	Lithography-3 metal	UV	DUV	DUV	DUV	DUV
	Cr/Au thickness	5 nm/200 nm	2 nm/200 nm	2 nm/150 nm	2 nm/150 nm	1 nm/150 nm
					[Investigation] Device resistance stability versus the thickness of adhesion Cr layer in Sec.3.8 with samples C#SOIC4s-150Au-1 C#SOIC4s-150Au-2 C#SOIC5-0.5Cr150Au C#SOIC5-1Cr150Au C#SOIC5-2Cr150Au	
	Release	Liquid HF	Liquid HF	Liquid HF/Vapor HF*1	Liquid HF/Vapor HF*2	Liquid HF
		[Investigation] The influence of HF etching on CNT device resistances Sec. 3.7 with samples C#SOIC3-R3C2 / C#SOIC3-R4C1				

*1 C#SOIC4-R5C1 was released by vapor HF.

*2 C#SOIC4s-RVHFC1 was released by vapor HF.

Subject \ Layout		SOIC2	SOIC3	SOIC4	SOIC4s	SOIC5
Design	Device components	• Source, drain, gate	• Source, drain (, gate)	• Source, drain, gate • Actuation system	• Source, drain, gate • Actuation system • RF GSG pads	• Modified shapes of source, drain, gate • Actuation system • RF GSG pads
	Device overview (scale bar 100 µm) Si Catalyst Metal		2T type  4T type 			
	Close-up of the electrode layout for CNTFET (scale bar 3 µm) Si Catalyst Metal	 Bridge width=2 µm Gate distance=1 µm	2T type  4T type  Bridge width= 0.5/ 0.75 µm Gate distance= 0.5/0.75 µm	 Bridge width=0.5 µm Gate distance=0.5 µm	 Bridge width=0.5 µm Gate distance=0.5 µm	 Bridge width=0.5 µm Gate distance=0.5 µm

Subject \ Layout		SOIC2	SOIC3	SOIC4	SOIC4s	SOIC5
Actuation system	Suspension beam			l_{sb}=370 µm w_{sb}=4 µm	l_{sb}=400 µm w_{sb}=4 µm	l_{sb}=400 µm w_{sb}=4 µm
	Adapter			g=1 µm ol=7.5 um	g=0.75 µm ol=2.5 um	g=0.5 µm ol=2.5 um
	Bent beam			l_{bb}=175 µm θ=2° w_{bb}=3 µm	l_{bb}=175 µm θ=2° w_{bb}=3 µm	l_{bb}=200 µm θ=2° w_{bb}=3 µm
						

Chapter 2 Current developments

The fabrication techniques of suspended CNTs are reviewed in this chapter and mirror the historical developments in this field. The initial research focus was the investigation of fundamental CNT material properties, such as Young's modulus and mechanical strength. With sufficient understanding of the CNT properties, the research focus gradually moved to applications, for example high frequency resonators and strain gauges. The following literature review of fabrication techniques will focus on the evolution of fabrication processes for suspended CNTs only.

2.1. Material property investigation

In the beginning of the research on suspended CNTs, the main focus was the extraction of Young's modulus and tensile strength. With the assistance of high resolution transmission electron microscopy (TEM), the diameters of CNTs were measured. Thermal vibration and forced vibration of freestanding CNTs were recorded during in-situ measurements. Treating a CNT as a rod or a cantilever, the Young's modulus of the CNT could be derived [5, 26] from its vibration frequency under classical continuum elasticity assumptions. Additionally, the static deformation of a CNT resulting from an external electrostatic force was measured in TEM, and the Young's modulus of the CNT was extracted [26]. In addition to in-situ measurements with TEM, atomic force microscopy (AFM) was commonly employed in measuring the bending and stretching stiffness of suspended CNTs [10, 17]. The Young's modulus derived from the experiments mentioned above is typically around E_{cnt}= 1 TPa. In the measurements, suspended or freestanding CNTs were prepared globally on chips, rather than in specific locations. The subsequent experiments were performed on selected well-suspended CNTs.

In order to measure the piezoresistive response of CNTs, electrical contacts to the CNTs are required. In [27], CNTs were grown by catalyzed chemical deposition (cCVD) from patterned catalyst islands on a SiO_2/Si substrate. Metal leads were patterned by electron beam lithography to contact these as-grown CNTs [28]. A trench was etched in the SiO_2 layer to make a partially suspended CNT [29]. Using an AFM to bend the suspended segment of a CNT, the electromechanical characteristics of the CNT were revealed. However, AFM indentation is limited to laterally bending a suspended CNT. Polycrystalline silicon (poly-Si) cantilevers were fabricated to apply axial strain on suspended CNTs [30].

With the suspended poly-Si cantilever, the out-of-plane AFM indentation was converted into in-plane axial strain [22, 31]. Suspended CNTs were integrated into suspended Si cantilevers for the first time by Franklin [30].

2.2. On-chip actuation

In addition to AFM indentation, on-chip actuation was also employed in straining CNTs. With the implement of on-chip actuation, applications related to straining CNTs can be achieved on a single chip. One type of the on-chip actuation is attained by the electrostatic force between a suspended CNT and a back-gate electrode. This type of device typically consists of one suspended CNT and three stationary electrodes. The fabrication is similar to the previous fabrication process of a suspended CNT with metal contacts for AFM indentation [29]. This approach is commonly utilized in CNT resonators [24, 32-34].

Another type of on-chip actuation is accomplished by movement of a MEMS actuator, such as an electrostatic comb-drive actuator and an electro-thermal bent-beam actuator [35-39]. Due to the difficulties of fabricating a suspended CNT on a MEMS actuator, assembly of a suspended CNT onto a pre-fabricated MEMS actuator is still the main approach for integration.

2.3. Integration of suspended CNTs on Si micro-structures

An integration process involving a suspended CNT and a MEMS actuator is more challenging compared to the fabrication of suspended CNTs on flat SiO_2/Si substrates. The difficulties mainly result from the fragility of the suspended CNTs, process-induced contaminations, and the ineffective orientation control of as-grown CNTs. Micron-long suspended CNTs can be damaged by viscous forces and capillary forces during wet processing. Additionally, the surfaces of CNTs tend to be contaminated by process chemicals, especially photographic resists. These two issues both occur in post-growth process steps. To avoid rupture and contamination, CNT growth is typically performed at the end of the entire process. However, only refractory metals, such as molybdenum (Mo) [30] and titanium nitride (TiN) [40], can endure the elevated growth temperature (~850 °C) in the cCVD growth process [41]. Additionally, the as-grown suspended CNTs are held in position by the van der Waal's force between CNTs and metals. If a CNT is small in diameter and the clamped length is short, the clamping force might not be sufficient to

clamp the ends of the CNT firmly while it is subjected to a strain, and sliding will occur [42].

All the structures, including micro-electrodes, trenches and metal leads, need to be fabricated prior to CNT growth to avoid the risky rupture and processing contamination in the post-growth processing. To properly integrate as-grown CNTs into these predefined structures, it is important to control the location and orientation of as-grown CNTs. However, the cCVD growth method only allows for location control but not direction control. To actively align growth direction, a controlled gas flow [43, 44] and an electrical field [45, 46] were introduced during the cCVD procedure. Different from these active control methods, another approach, called directed growth, is commonly used in aligning suspended CNTs to predefined structures. It was initially demonstrated on a substrate with a predefined array of Si pillars [47, 48]. Catalysts were patterned on top of the Si pillars, and CNT growth would initiate from these pillars. The as-grown CNTs were likely to bridge to the neighboring Si pillars, and hence, the directions of suspended CNTs could be defined by the patterns of the Si pillar array. This method was later applied on a suspended Si cantilever [30]. Based on this approach, a sharp Si tip was introduced to improve the direction control of suspended CNTs on micro-structures [49]. Taking advantage of this approach, suspended CNTs can be aligned to the pre-fabricated micro-structures or actuators [40, 50]. However, the area on the side wall of the neighboring structure is relatively larger than the top surface, so as-grown CNTs are more likely to bridge to the side wall, rather than the top surface. This makes it difficult to electrically contact CNTs with the metal leads on top of the micro-structures. Tilted metal evaporation together with an on-chip shadow mask is helpful to establish the electrical contact, even if a suspended CNT is attached to the side wall of a micro-structure [50].

In conclusion, it is still challenging to efficiently integrate clean suspended CNTs into pre-defined micro-structures with reliable electrical contacts and mechanical clamping. In the next chapter, an improved process for integrating suspended CNTs into MEMS structures is revealed.

Chapter 3 Process development for integrating suspended CNTs into Si micro-structures

Silicon-on-insulator (SOI) chips are chosen as substrates for the integration process. The melting temperature of single crystal Si is as high as 1415 °C [51]. Hence, Si can endure the CNT growth temperature (~850 °C). Moreover, the reliable mechanical property of Si [52] as well as the advantageous in-plane actuation of SOI chips is beneficial for straining suspended CNTs. Two types of SOI chips were employed in the integration process. The process development began with the SOI chips, consisting of a 5 μm thick device layer, a 2 μm thick buried oxide layer, and a 400 μm thick handle layer. Considering further integration with backside through-silicon-vias (TSVs) and high operational frequency of CNT resonators, the process development was continued with the second type of SOI chips with a reduced buried oxide layer (1 μm) and a thinner handle layer (300 μm). The second type of SOI chips have a heavily-doped Si device layer (ρ_{device}< 0.01 Ω-cm) to lower the driving voltage of an electro-thermal actuator and a resistive handle layer (ρ_{handle}> 2500 Ω-cm) to reduce the high frequency signal coupling through the substrate.

3.1. Approach

The integration process aimed to fabricate high quality suspended CNTs on MEMS actuators. Additionally, the process needed to be compatible with the backside TSV processing. The requirements of the integration process included:

- Clean, low-defect suspended CNTs
- Low electrical contact resistances of CNTs
- Robust mechanical clamping of the suspended CNTs
- Photomask-based lithographic process

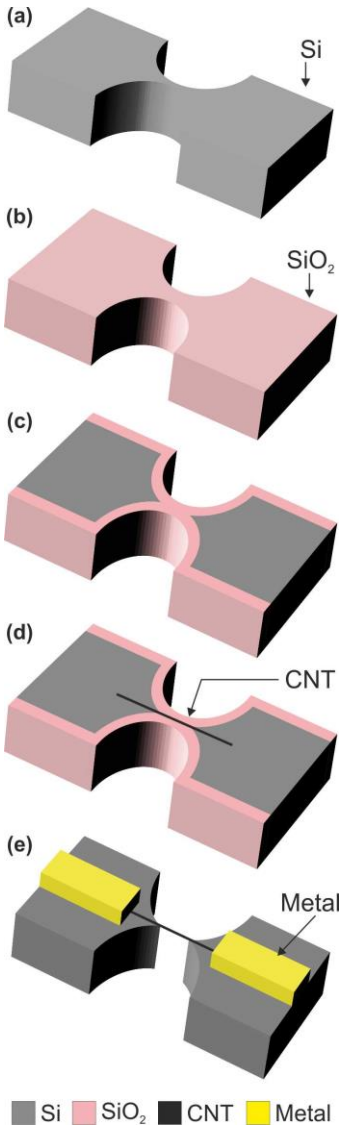


Figure 3-1 Sketch of the conceptual process flow for CNT integration into MEMS with a temporary support. A Si bridge was fabricated (a) and following oxidation converted the narrowest segment of the bridge into SiO_2 (b). After removing the top oxide (c), CNTs were grown on the bridge (d), and metallization was subsequently performed. Finally, the oxide bridge was etched by liquid HF, and the CNT became suspended (e).

The combination of direct CNT growth and top metallization by lift-off can fulfill all the requirements listed above. However, it is nearly impossible to perform wet processing on long and suspended CNTs without damaging them. A temporary supporting structure can resolve this problem by providing a CNT with physical support during post-growth wet processing. The concept of this approach is shown in Figure 3-1. A Si bridge was patterned (Figure 3-1a). The narrowest part of the bridge was fully converted into SiO_2 by thermal oxidation (Figure 3-1b). In order to avoid the successively built-up structures, like CNTs

and metals, being detached in the final release step, the top oxide layer needed to be removed (Figure 3-1c). The plane surface of the oxide bridge was able to provide physical support for the as-grown CNT (Figure 3-1d). Hence, post-growth wet processing was enabled, and metal leads were patterned by resist-based wet lift-off process. After metallization, the oxide bridge was etched by liquid hydrofluoric acid (HF) in the final release step (Figure 3-1e), and the CNT and MEMS structures became suspended.

3.2. Integration process flow

The patterns of all the Si structures were defined onto a 0.5-µm thick PMMA/MMA resist layer by deep UV lithography (DUV, ABM DUV mask aligner with a 220 nm filter). The minimum feature size of the design patterns on the photomask was 0.5 µm. Using the resist layer as an etching mask, the Si device layer was etched using the Bosch process (STS ICP) (Figure 3-2a). After stripping the resist, the chip was globally oxidized by wet thermal oxidation. A 500 nm thick SiO_2 layer was produced on Si surfaces, and therefore, the narrower part of the Si bridge was fully converted into SiO_2. To prevent the successively built-up structures, such as CNTs and metals, from detaching in the last release step, the oxide layer on top of the Si device layer needed to be removed. Mechanical polishing (Logitech PM5 autolap) removed the top oxide and achieved a plane surface on the oxide bridge. The suspension used for polishing was Logitech SF1, which contained silica particles (~65 nm in diameter) (Figure 3-2b).

A barrier layer was required to prevent the formation of silicide from the iron catalysts at the elevated CNT growth temperature [53]. A short wet thermal oxidation step was performed to produce a thin SiO_2 layer (t_{SiO2}= 25 nm) as the required barrier layer. To define a CNT growth site, a catalyst window (3 µm by 3 µm) was patterned onto a photoresist layer (Shipley S1818, t_{S1818}= 1.5 µm) at one end of these two Si electrodes by UV lithography (Karl Süss MA6 mask aligner). The catalysts used in this process were ferritin-wrapped iron particles. These iron particles were adsorbed on the chip surface from an aqueous catalyst solution [41]. After the adsorption, the chip was rinsed by de-ionized water to remove the residual catalyst solution. Following this a lift-off was performed briefly in three consecutive acetone baths. The chip was further cleaned by a resist remover, N-methylpyrrolidone (NMP). Catalysts only remained within the growth site. CNTs were grown from these catalysts by catalyzed chemical vapor deposition at 850 °C [41]. Statistically, some of the CNTs reach the other side of the bridge (Figure 3-2c). To protect

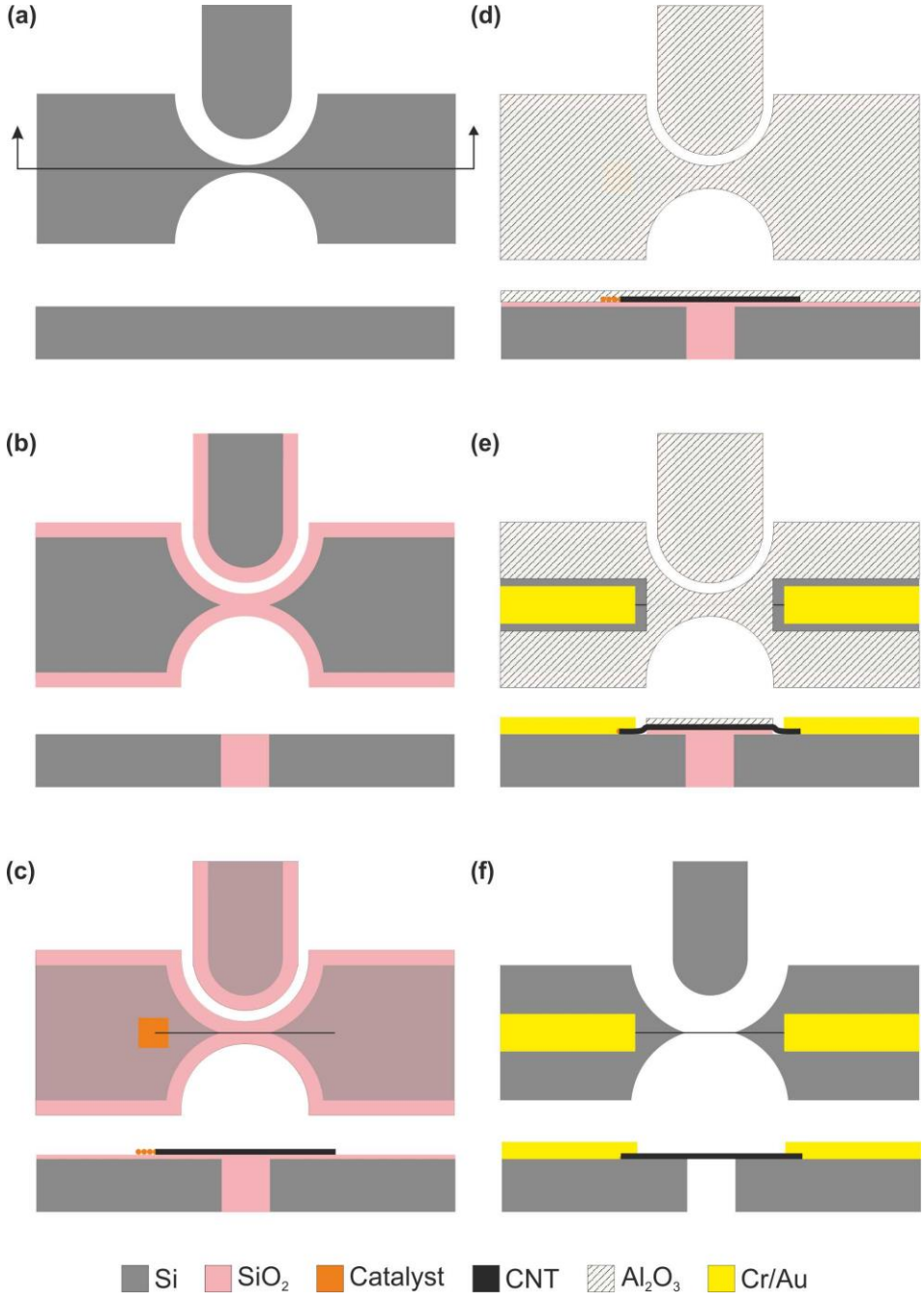


Figure 3-2 Integration process flow (top view and cross section of the device layer on an SOI chip). (a) DUV lithography & silicon etching by the Bosch process; (b) thermal oxidation & removal of top oxide by polishing for the temporary supporting bridge; (c) thermal oxidation, catalyst patterning & CNT growth; (d) global deposition of a thin protective Al_2O_3 layer by ALD; (e) etching of the Al_2O_3 at contact windows by BHF & metallization; (f) removal of SiO_2 and Al_2O_3 by concentrated liquid HF & drying in a critical point dryer.

the as-grown CNTs from being contaminated by the sticky resist in the following lithography for metal patterning, an Al_2O_3 layer (~40 nm) was deposited on the entire chip by low temperature atomic layer deposition (ALD) at 150 °C (Figure 3-2d). To define electrical contact on the aligned CNT, two lithography options were demonstrated. One was DUV lithography with three positive-tone resist layers on top of each other, i.e. two layers of PMMA/MMA and one layer of PMMA (t_{total}~1.8 µm). The other was UV lithography with negative-tone photoresist (~4 µm), AZ nLOF 2070. Since the CNT was still fully covered by the protective Al_2O_3 layer, it was possible to perform an optional cleaning step by oxygen plasma ashing to remove the resist residues on the contact areas. To make the Al_2O_3-covered CNTs accessible to the subsequently-deposited metals, the chip was dipped in a 6% buffered hydrofluoric acid (BHF) for 1.5 min, while the patterned resist layer served as an etching mask. After the BHF etching, the chip was baked on a hot plate at 100 °C for 90 s. A stack of metals, 2 nm chromium (Cr) and 200 nm gold (Au) or 1 nm Cr and 150 nm, was deposited by an electron-beam evaporator (Plassys II MEB550SL) at a deposition rate of 0.1 nm/s. The metal lift-off was carried out in NMP at 80 ˚C for three hours (Figure 3-2e). The sacrificial SiO_2 layer and the protective Al_2O_3 layer were etched by 48% liquid HF for 3 min to leave the CNT suspended. The SOI chip was dried in a super critical point dryer (CPD, Tousimis Automegasamdri 915B) (Figure 3-2f).

3.3. Design

There are three key design parameters of the device layout. These parameters are the side gate distance (*g*), Si bridge width (*w*), and metal pitch (*l*), as indicated in Figure 3-3. In

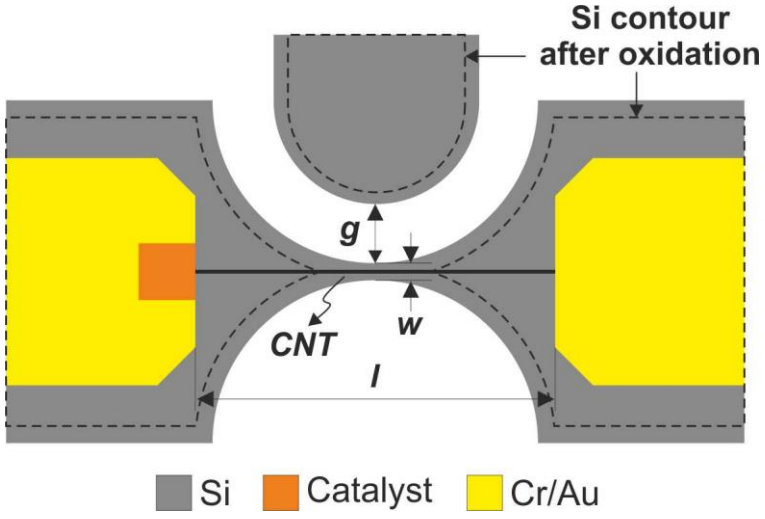


Figure 3-3 Three key parameters of the layout design.

order to improve gate modulation of the integrated CNTFET, the side gate distance should be as small as possible. Here, the gap was designed as g= 0.5 µm. Since the Si bridge needed to be fully oxidized, increasing the bridge width prolongs the oxidation duration. Moreover, a wider bridge tends to support more CNTs, and hence, there would be more CNTs in one device. Consequently, the bridge width of w= 0.5 µm was chosen. The pitch between two metal leads sets the requirement of the minimum CNT length. CNTs which are longer than the pitch can be contacted by metals. Considering the Si structure and process tolerance, the minimum pitch was set as l = 4.5 µm.

3.4. Fabrication results

3.4.1. Polishing

Figure 3-4 shows a scanning electron microscopy (SEM) image of a tilt view of three Si electrodes and the supporting oxide bridge after removing the top oxide by polishing (corresponding to the process step in Figure 3-2b). The mid-segment of the bridge was fully oxidized, and two opposite Si electrodes became visible after the 500 nm thick top oxide was removed. No abrupt step is seen in the topography of the polished bridge. This is important in avoiding kinks in the as-grown CNTs supported by the bridge. The topography of the polished oxide bridge was measured by a white light interferometer to be a shallow concave, where the center was 0.1 µm lower than the two ends. The small particles seen on the side walls of the Si electrodes in Figure 3-4 are likely residual silica particles. They are

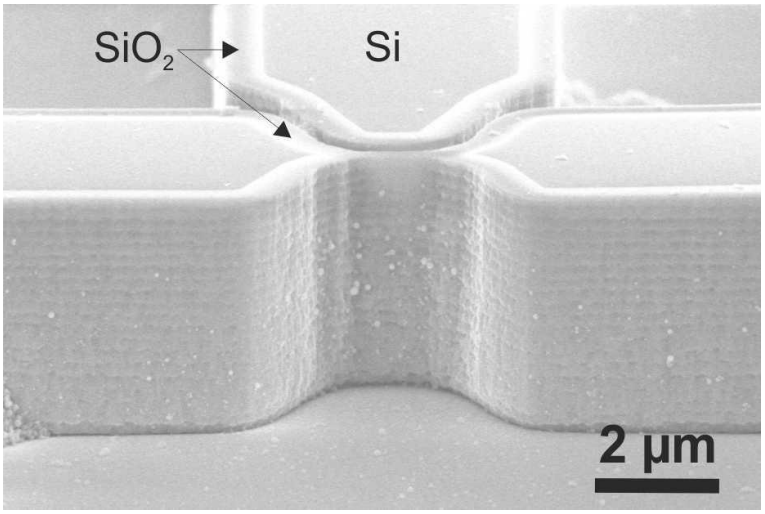


Figure 3-4 SEM image of a tilt view of three polished Si electrodes and an oxide bridge. The middle of the oxide bridge was measured to be slightly lower than the two opposite Si electrodes by 0.1 µm. (C#SOIC4)

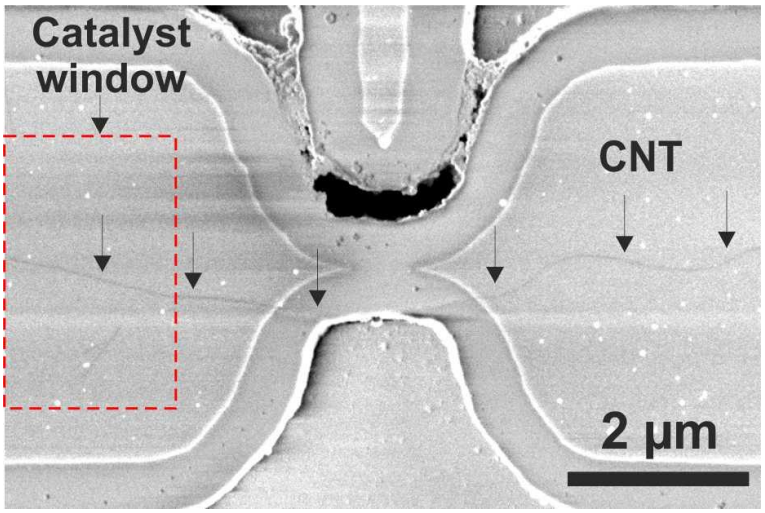


Figure 3-5 SEM image of a CNT grown from the defined catalyst window (dashed line enclosed area) to the opposite Si electrode. (C#SOIC4s)

etched by liquid HF in the final release. The mechanical polishing can produce smooth surface in addition to the topography. The root mean square roughness of the polished Si surface was as smooth as 0.1 nm, measured by atomic force microscopy (AFM).

3.4.2. Catalyst patterning

To define the CNT growth site, typically one growth window is patterned at the front end of one Si electrode for each device, as shown in Figure 3-2c. The synthesis of CNTs is initialized from the catalysts within the growth site. Without any external electrical field or gas flow during growth, CNTs are growing freely in all directions. In an ideal situation, one CNT bridges to the opposite Si electrode, as shown in Figure 3-5. Adsorption in a catalyst solution of higher concentration allows more CNTs to be grown along the oxide bridge to the opposite Si electrode. However, the possibility of gate leakage currents caused by CNTs of undesired orientations is also increased and CNT bundles form more often. As a result, defining the best concentration is challenging. During the process development, a target was set as the concentration which could result in 12 as-grown CNTs within one growth site (3 µm by 3 µm). If the CNT growth is random in all directions, one of these 12 as-grown CNTs could be within the tolerable direction (±15°) per device. The tolerance angle was calculated based on the layout of the catalyst site and the metal leads. This is a useful guideline to tune the catalyst concentration. However, the best yield achieved was 1% and thus an efficient method of cutting incorrectly-orientated CNTs was explored to improve the situation, which is discussed in section 3.6.4.

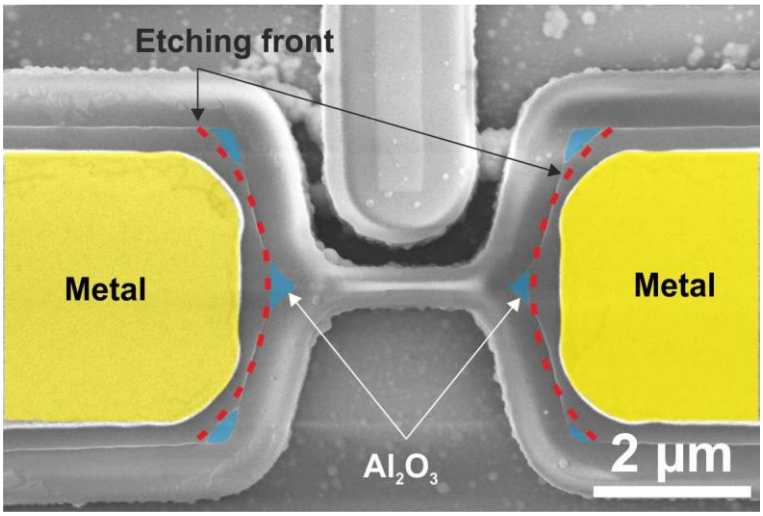


Figure 3-6 Top view of a device after metallization. The dashed line indicates the etch front on the Al_2O_3 layer. The etched Al_2O_3 areas were larger than the metal leads because of the inclined profile of the resist and the over-etching by BHF. Note that no CNT is seen in this figure. Yellow color of metals and blue color of Al_2O_3 are added to enhance the visibility. (C#SOIC5)

3.4.3. Metallization

Before metal evaporation, the protective Al_2O_3 layer on the metal contact areas needed to be removed. No additional lithography was required for this step. The resist layer patterned for metallization served as an etching mask, the contact windows on the Al_2O_3 layer were opened by BHF etching. In this BHF etching step, the Al_2O_3 layer must be completely removed so that the CNTs can be electrically contacted by metals. To ensure the Al_2O_3 layer was completely removed on the contact windows of hundreds of devices on a 1.8 cm by 1.8 cm chip, improved wetting by 20% isopropanol (IPA) [54] and over-etching were performed. Figure 3-6 shows an SEM image after metallization. As indicated by the dashed line, the etched Al_2O_3 layer was broader than the metal leads due to the inclined profile of the resists (for lift-off process) and the over-etching during opening contact windows on the Al_2O_3 layer by BHF.

3.4.4. Liquid HF release

If a CNT is properly clamped at both ends, it can remain in the same position during liquid HF release and will become suspended after release. A released CNT is shown in Figure 3-7a [55]. The two ends of the suspended CNT were clamped by the metal leads on the Si electrodes. A clamped-clamped configuration is indicated by the CNT trace extending into the metal lead (Figure 3-7b [55]). The robust clamping can provide sufficient clamping

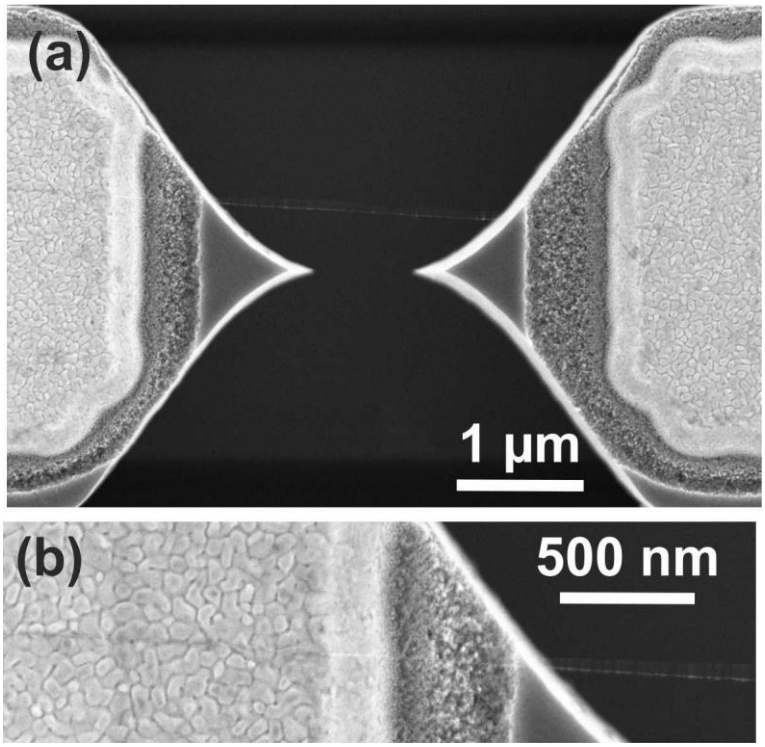


Figure 3-7 (a) A suspended CNT across a gap between two Si electrodes [55]; (b) close-up of the clamping site on the left Si electrode shown in (a) [55]. A doubly-clamped configuration is indicated by the CNT trace extending into the contact region. The porous structures seen around the metal leads are likely to be porous silicon structures, resulting from the galvanic effect during liquid HF etching (D#13_C#SOIC3-R2C1). ©2011 , IEEE

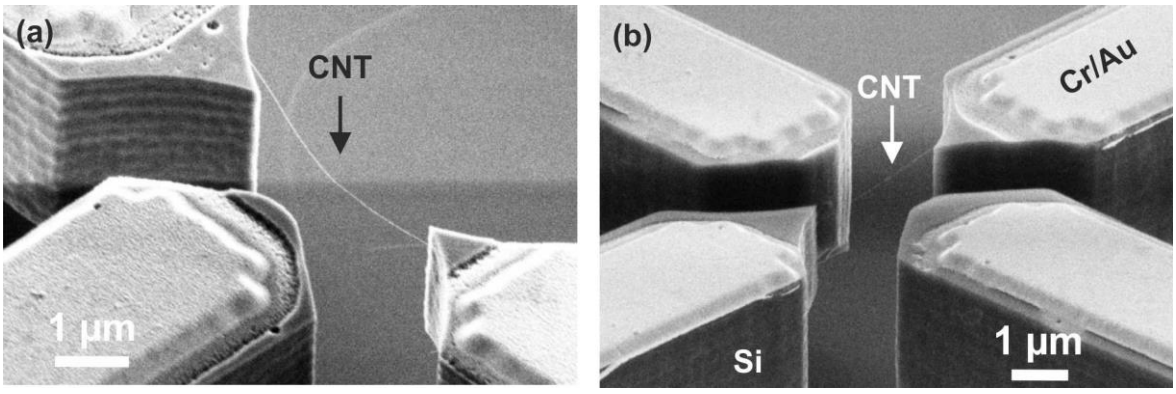


Figure 3-8 Two different gate configuration; (a) a suspended CNT with single Si side-gate; (b) a suspended CNT with double Si side-gates (a: D#20-5A_C#SOIC3-R3C2/ b: D#23-4c_C#SOIC3-R3C5).

force to hold the CNT in position during the release and drying procedures. Moreover, the robust mechanical clamping can prevent the CNT from sliding while it is strained by a MEMS actuator during operation (see section 5.1). The porous structures surrounding the metal leads seen in Figure 3-7 are likely porous Si. The porous Si structures resulted by a so-called galvanic effect [56], occurring in liquid HF etching when both Au and heavily-doped Si are present. Using the integration process, a suspended CNT can be equipped with single or double side-gates, as shown in Figure 3-8.

3.5. Characterization

After the final release, the integrated suspended CNTs were characterized by several measurements. These included electrical transport measurements, Raman spectroscopy inspection, and SEM observation. The sequence of these measurements is important because the induced by-products or defects during the previous measurement can influence the following characterization. The electrical transport measurements of the CNTFETs are typically performed first to avoid laser induced degradation during Raman inspection. Electron-beam induced carbonaceous deposition during SEM observation can be detected by Raman spectroscopy. Thus SEM will influence the analysis of the CNT quality by Raman. In addition to the amorphous carbon, the inspected CNT devices will be electrically charged by the electron-beam in the SEM, and the electrostatic discharge (ESD) during probing in the following electrical measurements usually causes failure of the CNT devices, as was observed in suspended CNTs on SOI chips. As a result, Raman spectroscopy is the second characterization, and SEM is done as the last step.

3.5.1. Raman inspection

Raman spectroscopy is a powerful tool to reveal the properties and quality of CNTs [57]. Here, confocal Raman spectroscopy (excitation with $\lambda = 532$ nm, power= 0.5 mW, integration time= 60 s, averaged over 3 measurements) was used to examine the integrated suspended CNTs. Figure 3-9 shows a typical Raman spectrum of an integrated suspended CNT. The G^+ (1587 rel.cm^{-1}) and G^- (1565 rel.cm^{-1}) peaks are a typical signature of semiconducting single-walled CNTs (SWNTs). According to the RBM peak appearing at 194 cm^{-1}, the diameter of the CNT is determined to be 1.18 nm [58]. A D-band peak is attributed to asymmetric contamination on the surfaces of CNTs or atomic structural defects in CNTs [57]. The measured intensity of the D-band peak is low, and the consequently low ratio of D to G-band intensity ($D/G^+=1/224$) suggests high quality of the SWNT [59, 60].

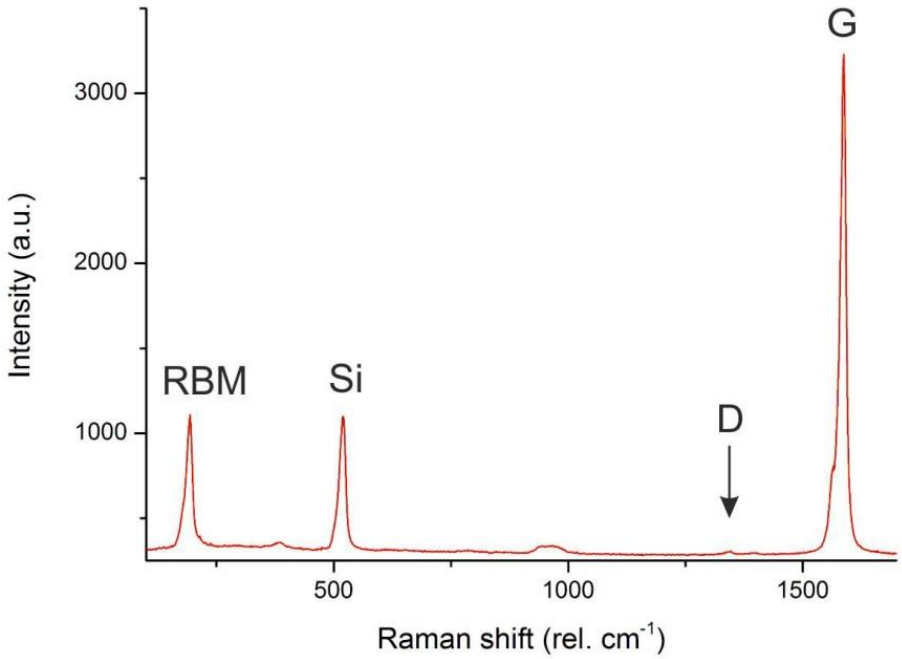


Figure 3-9 A typical Raman spectrum of an integrated suspended CNT after liquid HF release (λ= 532 nm, laser power= 0.5 mW, integration time= 60 s, averaged over 3 measurements). The spectrum indicates that the corresponding CNT is a semiconducting single-walled CNT with a diameter of 1.18 nm, and the high quality of the CNT is suggested by the low ratio of D-band to G-band intensity (1/224) (D#E19_C#SOIC5-STB2C1).

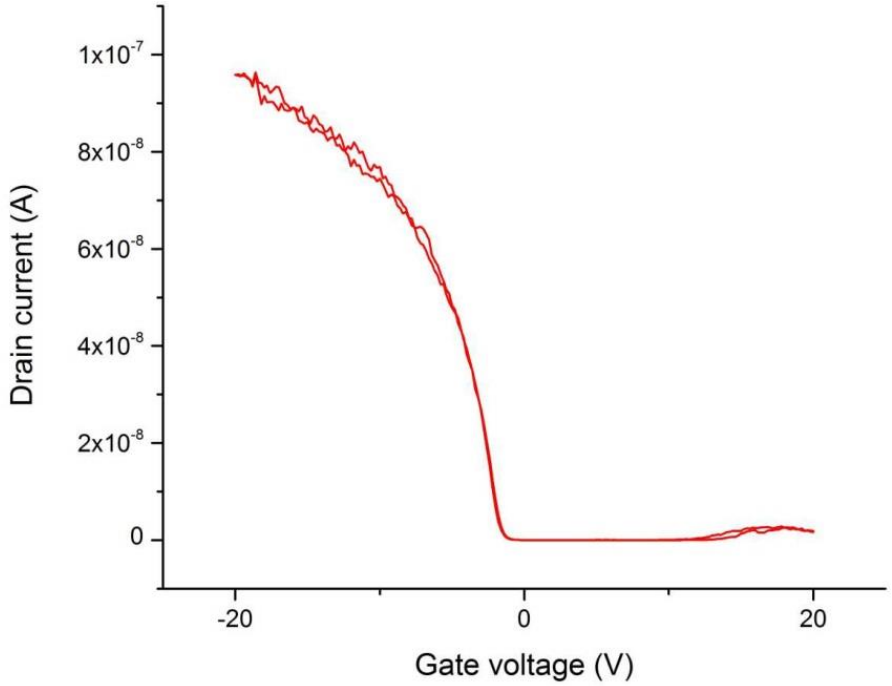


Figure 3-10 Low-hysteresis transport measurement of a suspended CNTFET operated in ambient air by a continuous gate voltage round sweep (V_{gd}=0 V→+20 V→−20 V→0 V). The applied constant source-drain voltage was V_{ds}=50 mV. The extracted hysteresis was 65 mV (D#E06_C#SOIC5-1Cr150Au).

3.5.2. Transport measurements

With the fabricated Si side-gate(s), transport measurements of CNTFETs can be performed to reveal the electronic characteristics of suspended CNTs. Transport measurements were performed with a commercial semiconductor characterization system, Keithley 4200, in ambient conditions (relative humidity= 47% and temperature= 21°C in the ETH FIRST cleanroom). The source-drain voltage was typically set to V_{ds}= 100 mV or V_{ds}= 50 mV. The compliance of the source and drain currents was 1 µA. The increment of the sweeping gate voltage was ΔV_{gd}= 100 mV or ΔV_{gd}= 200 mV, corresponding to a continuous gate sweep rate of 1 V/s and 2 V/s. A transport measurement of a suspended CNTFET is shown in Figure 3-10. The source-drain voltage V_{ds}= 50 mV was applied, and the gate voltage (V_{gd}) applied on the single side-gate, sweeping from V_{gd}=0 V→ +20 V → −20 V → 0 V, by an increment of ΔV_{gd}=200 mV. The gate leakage current was less than 25 pA (not shown). The hysteresis in the I_d-V_{gd} curve is calculated to be 65 mV. The small hysteresis indicates that few charge trapping sites were present around the CNT [61], namely there were little contamination on the suspended CNT and small non-suspended segments overlapping with the native oxide of the Si source/drain electrodes. The minimum device resistance within ±20 V V_{gd} range was 519 kΩ. In addition to this device, the minimum resistances of other 10 suspended CNTFETs fabricated in different process runs were distributed from 91 kΩ to 319 kΩ, revealing the capability of the process in fabrication of suspended CNTFETs on Si micro-structures. The device resistances are comparable to or lower than the device resistances of CNTs integrated into MEMS in literature [30, 40, 50].

3.6. Process development

The integration process flow described in section 3.2 is the combination of individual improved process steps. In this section, the development of selected important steps will be described in detail.

3.6.1. Removing top oxide by mechanical polishing

Instead of using common reactive ion etching (RIE), mechanical polishing was employed to remove the oxide on the top surface (Figure 3-2b) because of the considerations to surface roughness and topography. A smooth surface is preferred for the CNT growth due to the desired small CNT diameter distribution [62]. Typically, RIE-etched surfaces are rougher, compared to the polished surface of 0.1 nm in roughness. In addition to surface roughness, a plane surface is beneficial in avoiding kinks in as-grown CNTs. However, it is very difficult

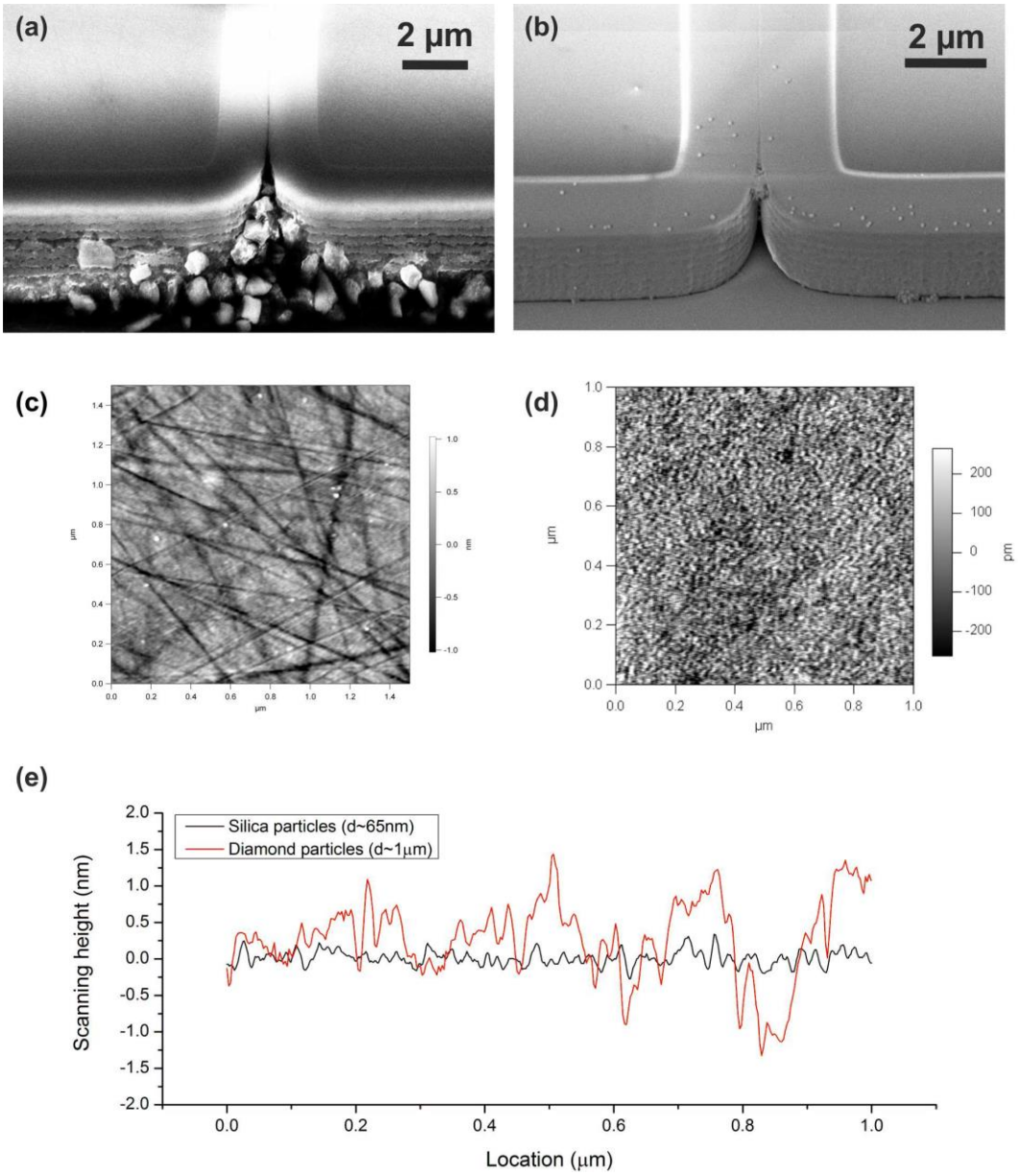


Figure 3-11 Mechanical polishing by diamond particles (~1 μm) or silica particles (~65 nm); (a) SEM tilt view of Si edges with accumulated diamond particles; (b) SEM tilt view of Si edges with less accumulated silica particles; (c) AFM scanning height of diamond polished Si surface; (d) AFM scanning height of silica polished Si surface; (e) roughness of these two polished surfaces measured by AFM. (C#SOIC2-RTC1 by diamond particles; C#SOIC2-RTC2 by silica particles)

to achieve a flat top surface of the oxide bridge by RIE. The etching will stop at the Si surface once the top oxide is completely removed by RIE. However, there is no etching stop in the mid-part of the oxidized bridge (see the cross-section in Figure 3-2b), which can cause a small over-etching resulting in undesired abrupt steps at the boundary of the oxide bridge and the Si electrodes. These steps will consequently cause kinks in as-grown CNTs.

Mechanical polishing can result in a smooth and flat surface. However, after the polishing procedure, it was difficult to completely remove the small polishing particles. A sample polished by diamond particles (d~1 μm) is shown in Figure 3-11a. Many diamond particles accumulated at the structure corners. These particles became smaller during polishing, making the cleaning task even more challenging. To address this issue, diamond particles were replaced by silica particles (d~65 nm) because silica is the same material as the sacrificial layer in the process. Thus, if there are residual silica particles on the polished surfaces, they are completely removed during the release step and will not cause any problems to CNT-devices. With a proper cleaning procedure, most of the silica particles can be rinsed away and only some particles remain, as shown in Figure 3-11b. The key to the effective removal of the particles is to keep polished sample surfaces wet throughout the entire cleaning procedure. Both diamond and silica particles can result in smooth surfaces as shown in Figure 3-11c and Figure 3-11d respectively. Figure 3-11e compares the surface roughness of the two polished surfaces. The smaller size of the silica particles resulted in a relatively smoother polished surface.

3.6.2. Patterning catalysts

Catalyst patterning plays an important role in the integration process because it determines the location and the number of catalysts and as-grown CNTs. The following section describes the catalyst adsorption, lift-off, and an efficient method of monitoring the catalyst concentration.

- **Catalyst adsorption**

Before the adsorption, two treatments were performed. The first was to dip the chip into a 1% NaOH bath for 1 s to remove the resist residues in the catalyst windows. The second was to wet the chip surface by dipping into a 20% IPA bath [54] for 5 s. Immediately after the wetting, the chip was immersed in to a catalyst solution. A sufficient volume of the catalyst solution was required (>3 ml) to lower the impact of the small amount of IPA brought into the catalyst solution by the chip. Usually, four SOI chips were sequentially

immersed into the same catalyst solution for 5 min each, and these chips had similar number of as-grown CNTs at each of the growth sites.

- **Catalyst lift-off**

The lift-off of the discrete catalysts is different from that of a continuous thin metal film. Right after dipping into acetone, the resist layer on the chip was mostly dissolved and the catalysts became suspended in acetone. To prevent the suspended catalysts from attaching to the substrate again, the lift-off was performed briefly in three different acetone baths, and the chip was cleaned in NMP at 80 °C for 15 min. This procedure is shown in Figure 3-12. Since most of the catalysts became suspended and remained in the first acetone bath, the first acetone bath was renewed for each chip, while the following baths were able to be used for four chips (typically four SOI chips were processed in the same run). The cleaning of NMP was a required step because it removed the S1818 resist residues together with the catalysts. This cleaning step influenced the resolution of the patterned growth sites. To demonstrate the effectiveness, a high concentration catalyst solution was applied on two oxidized Si chips (t_{SiO2}= 2 µm), where growth sites were already defined with resist. The lift-off procedure was performed according to the first three steps in Figure 3-12, but the NMP cleaning step was skipped on the second chip. These two chips were processed in the same growth run, and the growth results are shown in Figure 3-13. The patterns of as-grown CNTs (high density) were better defined on the first chip with NMP cleaning, while on the second chip, CNTs even grew outside the defined areas. Moreover, by comparing the density of the as-grown CNTs within patterned areas, there is no noticeable difference in the

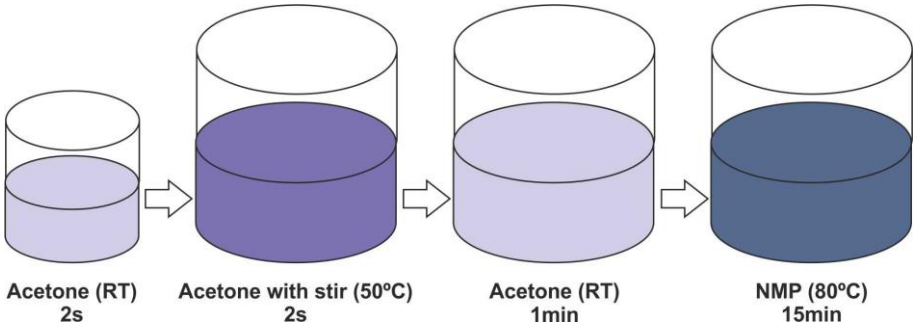


Figure 3-12 Catalyst lift-off procedure. The chip was dipped briefly into different acetone baths and transferred quickly to avoid the catalysts from re-attaching the substrate. “RT” stands for room temperature.

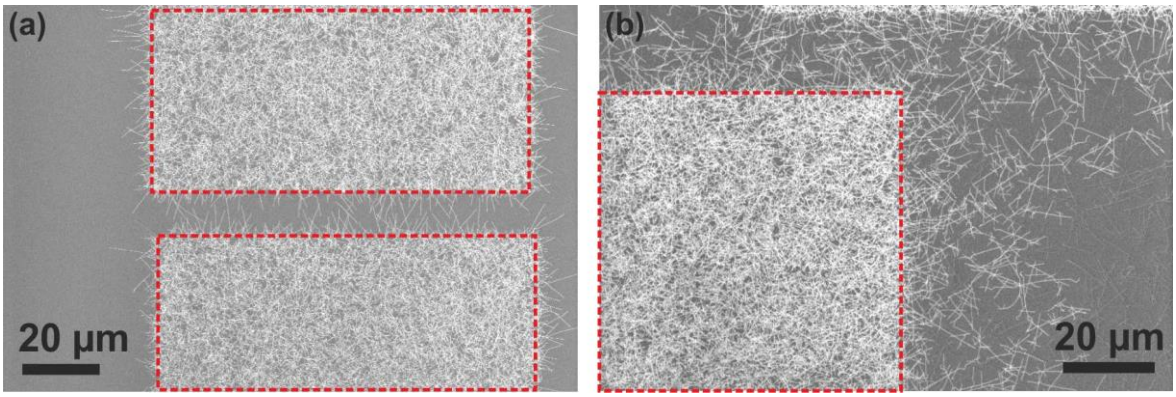


Figure 3-13 Comparison of as-grown CNTs on two SiO_2 chips (t_{SiO2}=2 µm); (a) lift-off of catalysts with NMP cleaning; (b) lift-off of catalysts without NMP cleaning. Defined catalyst areas are highlighted with dashed line enclosed blocks. (C#Ox1-C1 and C#Ox1-C2).

CNT density on these two chips, which suggests that NMP does not suppress the subsequent CNT growth. As a result, the cleaning of NMP is helpful to in well patterning the location of CNT growth sites without sacrificing CNT growth yield.

- **Monitoring the catalyst concentration**

The number of CNTs grown from a patterned growth site is related to the concentration of the catalyst solution. It is important to correlate the catalyst concentration with the number of as-grown CNTs on SOI chips. The concentration needed to be adjusted regularly due to the drift of growth conditions of the LPCVD machine and the aging of the catalyst solution. However, it was time consuming and impractical to prepare integrated SOI chips exclusively for the concentration tests. Oxidized Si dummy chips were employed to monitor the concentration in an efficient way. The correlation between the dummy chip and the SOI chip was obtained by comparing the as-grown CNT densities, as shown in Figure 3-14. As long as the conditions of the dummy chips and SOI chips were maintained, the growth results on the dummy chips could predict the growth conditions on SOI chips. In addition to the correlation in the CNT density, the as-grown CNTs on these two types of chips were found to be similar in length distribution. This was very useful in monitoring the drift of the growth conditions of the LPCVD machine. Using these dummy chips, the drift of the growth conditions and the aging of the catalyst solution could be efficiently monitored, and the concentration could be tuned properly.

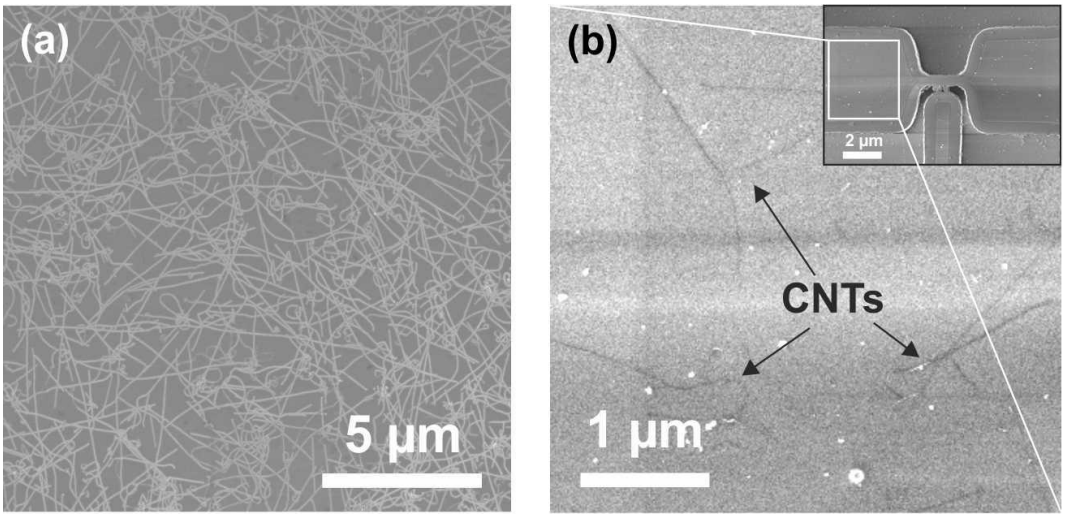


Figure 3-14 As-grown CNT density correlation between an oxidized Si dummy chip and an SOI chip; (a) SEM image of as-grown CNTs on a dummy chip with a thick SiO_2 layer (t_{SiO2}~2 µm); (b) SEM image of as-grown CNTs on an SOI chip with a thin SiO_2 layer (t_{SiO2}~25 nm) (a:C#Ox2-CD; b:C#SOIC5).

3.6.3. ALD Al_2O_3 assisted lithography

To prevent CNTs from being in direct contact with sticky resists, a protective layer is introduced to separate CNTs from resists during lithography [55, 63]. After processing the resist on top of the protective layer, harsh cleaning can be performed as the CNTs are protected. This protective layer can be removed without damaging the CNTs. This step also lifts off any remaining resist residues. Consequently, cleanliness is ensured, even without high temperature annealing for cleaning.

- **Material of the protective layer**

The material of the protective layer determines the effectiveness of this approach. Here, low temperature ALD Al_2O_3 is chosen as the protective layer material for three reasons. Firstly, the Al_2O_3 layer can be etched by liquid hydrofluoric acid (HF) or phosphoric acid (H_3PO_4). Liquid HF is often used to release CNTs [64, 65], and H_3PO_4 has not been reported to be harmful for CNTs in literature. Secondly, if SiO_2 is used as substrate material, the Al_2O_3 layer can be selectively removed by H_3PO_4 because of the good selectivity over SiO_2 etching [66]. Thirdly, ALD is assumed not to cause defects in CNTs because ALD Al_2O_3 has been demonstrated for CNT-device passivation [67-70]. As a result, ALD Al_2O_3 is considered as a suitable material of the protective layer.

Table 3-1 Comparison of process conditions of the four chips used in the two investigations of ALD protective layer assisted lithography.

Chip	Substrate	Process steps
A	As grown CNTs on SiN/Si	ALD/ resist coating/ acetone/ BHF
B	As grown CNTs on SiN/Si	resist coating/ acetone
C	As grown CNTs on SOI	ALD/ lithography/ O_2 plasma/ BHF/ metallization/ liquid HF/ critical point drying
B	As grown CNTs on SOI	lithography/ metallization/ vapor HF

- **Concept verification on non-suspended CNTs**

To verify the effectiveness of the protective layer in maintaining clean surfaces of CNTs, a resist removal test with acetone was performed on as-grown CNTs. Two identical Si chips with a silicon nitride thin film were used as substrates for the growth of CNTs. After the CNT growth, an ALD Al_2O_3 layer of 40 nm was deposited at 150 ˚C onto the as-grown CNTs on one chip, chip A. The other chip, chip B, without an Al_2O_3 layer, was used as a control sample. A resist, AZ nLOF 2070, was spun on both chips, followed by a baking step at 110 °C for 60 s. These two chips were subsequently dipped into acetone at 50 ˚C for 10 min to strip the resist layer. Chip A was further etched by 6% BHF for 30 s to remove the Al_2O_3 layer. The process steps of these two chips are summarized in Table 3-1. AFM scans were utilized to compare the surface conditions of these two chips. Figure 3-15 shows the AFM scanning height images of these two chips [63, 71]. The surface of chip A, which was covered by Al_2O_3, appeared smoother compared to chip B. The dots on the CNT and the

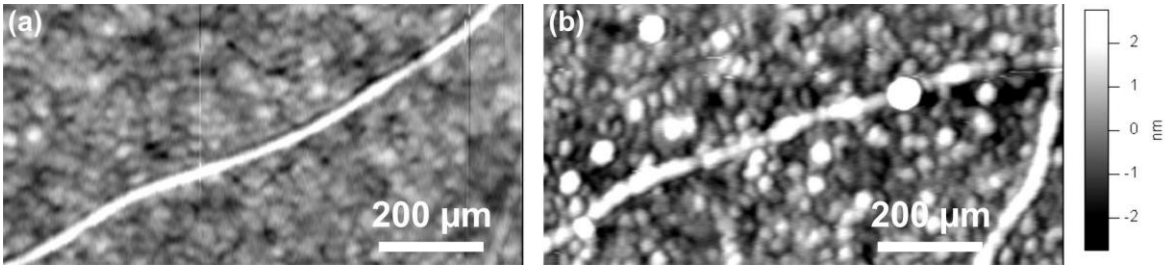


Figure 3-15 AFM scanning height images of two chips with CNTs after removing photoresists in acetone and etching Al_2O_3 in BHF (a) chip A, where the CNT was covered with an Al_2O_3 protective layer and (b) chip B, where the CNT was not covered with an Al_2O_3 layer during spin coating [63,71] (a: C#SiN-C1;b:C#SiN-C2). © 2014, Elsevier

surroundings shown in Figure 3-15b were few nanometers in height, and they were likely to be residual resists. The particle size was comparable with findings in literature [61, 72-74]. Here, no visible residues were found on the Al_2O_3-covered CNT after removing the resist and the Al_2O_3 layer.

- **ALD Al_2O_3 assisted metallization**

After confirming the effectiveness of the protective layer in the previous test, the ALD Al_2O_3 layer was introduced to the integration process. To compare the surface conditions of CNTs with and without an Al_2O_3 layer during metallization, two SOI chips, chip C and D, were prepared. Using the integration process (Figure 3-2a to Figure 3-2c), CNTs were grown on these two SOI chips. In the following metallization and release steps, these two SOI chips were processed differently. Chip C was covered with an ALD Al_2O_3 layer (Figure 3-2d) before lithography with AZ nLOF 2070 (Figure 3-2e). Oxygen plasma ashing (100 W for 30 s, Technics Plasma 100-E) was performed to remove resist residues on the metal contact areas. This chip was released by liquid HF for 3 min (Figure 3-2f). Chip D, used as a control sample, was processed by the same metallization process without an Al_2O_3 layer and without oxygen plasma ashing afterwards. Chip D was released by vapor HF at 40 ˚C for 2 hours. In terms of the defects in CNTs, vapor HF is similar with liquid HF, and neither cause defects to CNTs. More details about vapor HF are described in Appendix I. The process conditions of these two chips are summarized in Table 3-1. Electrical transport measurements, Raman spectroscopy and SEM inspection were carried out to characterize the suspended CNTs on these two chips. The SEM images of the suspended CNTs on chips

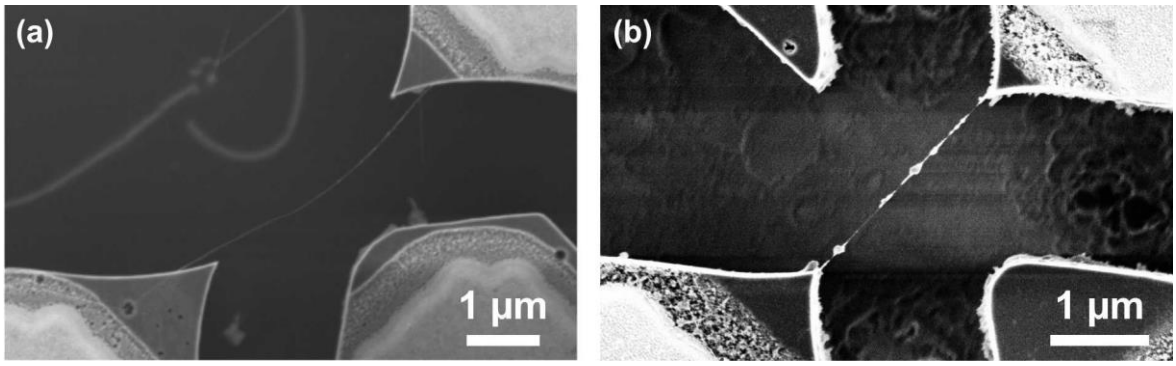


Figure 3-16 SEM images of suspended CNTs; (a) chip C, where the CNT was covered by an ALD Al_2O_3 layer during lithography; (b) chip D, where the CNT was in direct contact with resist during lithography [63] (a: D#20-5A_C#SOIC3-R3C2; b: D#21-7D_C#SOIC3-R5C1). © 2014, Elsevier

C and D are shown in Figure 3-16a and b respectively [63]. There were no residues found on the suspended CNT on chip C (Figure 3-16a), which was covered with the Al_2O_3 layer during lithography. However, residues were seen on the CNT on chip D (Figure 3-16b), where the CNT was in contact with resists during lithography.

To obtain a quantitative comparison of these two suspended CNTs, they were inspected by a confocal Raman spectroscope (λ= 532 nm, integration= 60 s). From the spectra shown in Figure 3-17a [63], the D-band peak of the CNT on chip C (spectrum 3) was nearly undetectable. The intensity ratio of D peak to G peak was close to 0, indicating little process-induced contamination on the surface of the CNT or few defect in it [75]. The two spectra measured on chip D had D/G ratios of 0.23 (spectrum 1) and 0.35 (spectrum 2). Spectrum 1and 2 were measured on segment 1 and 2 of the CNT on chip D, as indicated in Figure 3-17b [63]. In addition to the higher D/G ratios compared to spectrum 3, increased background signal intensities were also observed in both spectrum 1 and 2. Higher background signal intensity and more resist residues were both observed on segment 1. The profile of the background signal is similar with the spectrum profile measured on an AZ nLOF 2070-coated SOI chip (Figure 3-18 [63]). As a result, the residues of AZ nLOF 2070 are highly relevant to the increased background signal intensities in spectrum 1 and 2.

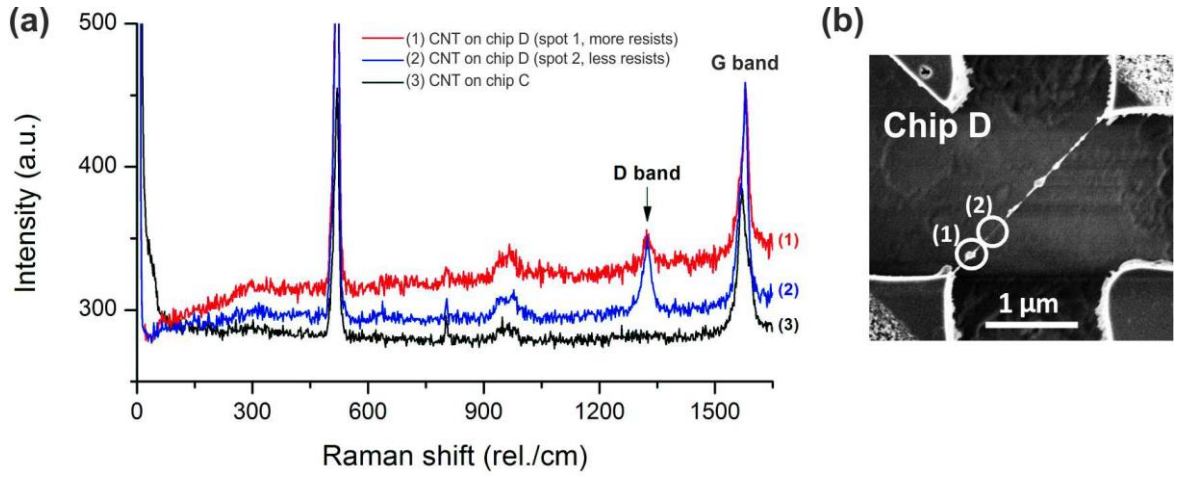


Figure 3-17 (a) Raman spectra of suspended CNTs on chip C (spectrum 3) and on the control chip D (spectrum 1 and 2). Spectrum 1 and 2 were measured at two segments on the same CNT, and the locations are indicated in the SEM image in (b). The D/G ratio is 0.23 for spectrum 1, 0.35 for spectrum 2, and 0 for spectrum 3. (λ= 532 nm, integration time= 60 s) [63] (CNT on chip C: D#20-5A_C#SOIC3-R3C2; CNT on Chip D: D#21-7D_C#SOIC3-R5C1). © 2014, Elsevier

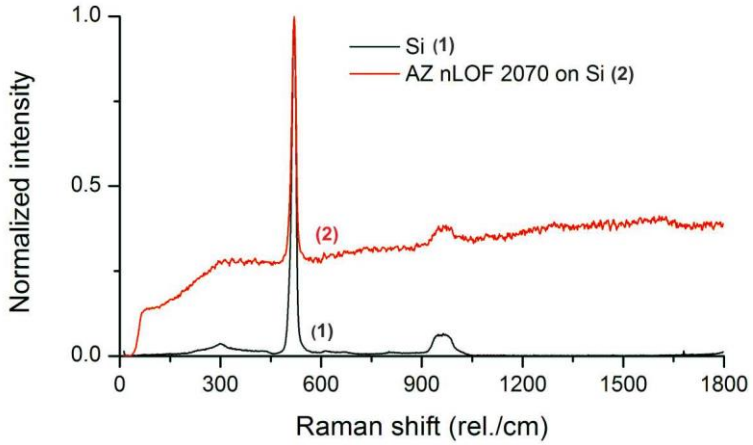


Figure 3-18 Raman spectra of a blank Si surface and AZ nLOF 2070 on Si (λ= 532 nm, integration time= 60 s) [63]. © 2014, Elsevier

Electrical transport characteristics of the CNTs on chips C and D were measured to evaluate their respective performance. The applied source-drain bias (V_{ds}) was 50 mV, and the gate voltage continuously swept from −15 V to 15 V and back to −15 V at a sweep rate of 1 V/s. The transport measurements were performed in ambient air. The measured I_d-V_{gs} curve of the CNTFET on chip C is shown in Figure 3-19 [63]. The minimum resistance was as low as 91 kΩ. Moreover, the gate hysteresis was determined to be 0.5 V in ambient conditions. The hysteresis is relatively small for photolithography-processed CNTs [61, 76] but still

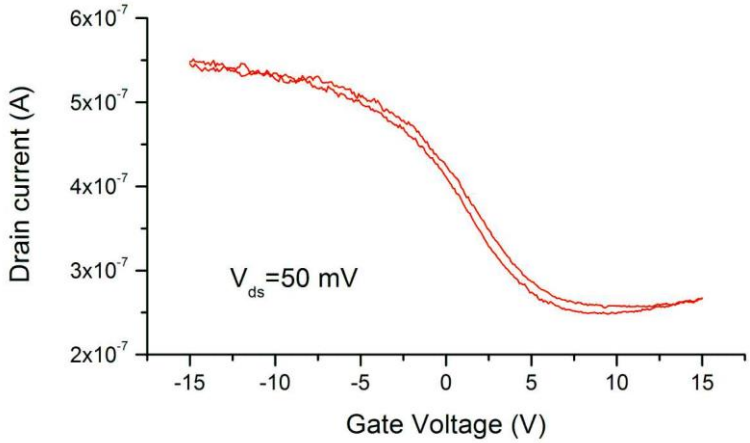


Figure 3-19 Transport measurement of the suspended CNTFET protected from intimate contact with resist during lithography. The minimum resistance was 91 kΩ, and the hysteresis of the dual sweeps was 0.5 V at the gate voltage sweep rate of 1 V/s in ambient air (D#20-5A_C#SOIC3-R3C2). © 2014, Elsevier

larger than the hysteresis of CNTFETs made of as-grown CNTs [50]. The same setting was applied in the measurement of the device on the control chip D, but this device had a resistance higher than 1 GΩ.

The clean surface of the as-grown CNT on chip C was preserved by the protective Al_2O_3 layer. The effectiveness is confirmed by the low intensity D-band peak and low background signal in Raman inspection. Moreover, the clean contact interface between the CNT and metals contributed to the low device resistance of 91 kΩ. The low hysteresis of the I_d-V_{gs} curves is attributed to the suppression of residual resists on CNTFET channel because fewer charge trapping sites were present around the suspended CNTFET [61]. In conclusion, the ALD Al_2O_3 layer can maintain clean surfaces of CNTs during lithography, and the issue of residual resist contamination can be addressed and consequently high device performance can be ensured.

3.6.4. CNT selection

The concentration of the catalyst solution is highly relevant to the number of as-grown CNTs. As discussed previously, the target concentration was set as 12 CNTs grown from each growth site. However, some of the as-grown CNTs could bridge to the gate and result in gate leakage currents. To improve the situation, oxygen plasma ashing can be performed after the deposition of the Al_2O_3 layer to selectively remove the unwanted CNTs, which are partially suspended. This method was demonstrated by the following experiment. The top

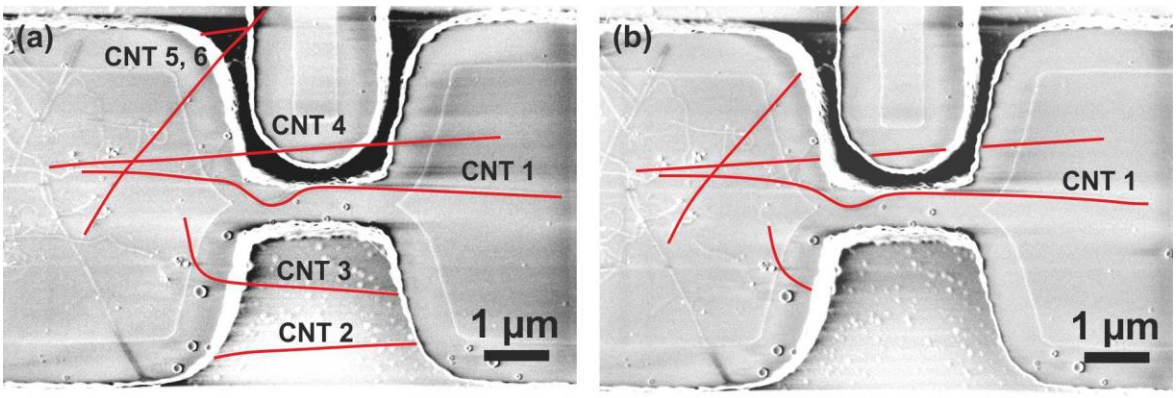


Figure 3-20 Selective removal of CNTs; (a) after ALD deposition, a non-suspended CNT (CNT 1) was fully covered by Al_2O_3, but partially suspended CNTs (CNT2-6) were not fully covered due to the inert surface for ALD nucleation; (b) after oxygen plasma ashing (100 W for 30 s), all the non-protected suspended segments of CNT 2-6 were burned, and the integrity of CNT 1 was preserved due to the protection of ALD Al_2O_3 CNT1~6 are highlighted by red lines.(C#SOIC5-O2-C1).

view of one device after the deposition of the Al_2O_3 layer is shown in Figure 3-20a. Six CNTs were grown over the border of the left Si electrode seen in Figure 3-20a, and only one of them lay on the oxide bridge (CNT 1). Because of the inert surfaces of low-defect CNTs for ALD nucleation [69, 77], the suspended segments of CNT 2-6 were not covered with the Al_2O_3. However, the Al_2O_3 was able to be deposited gradually on the oxide bridge. If the thickness of Al_2O_3 was larger than the diameter of the CNT, the non-suspended CNT on the bridge, CNT 1 in Figure 3-20a, would be fully covered by the Al_2O_3 layer. After a short oxygen plasma ashing (100 W for 30 s), all the non-protected suspended segments of CNTs were burned and only the completely-protected CNT 1 remained, as shown in Figure 3-20b. The selection can remove CNTs of undesired orientation and enlarge the tolerance of the catalyst concentration.

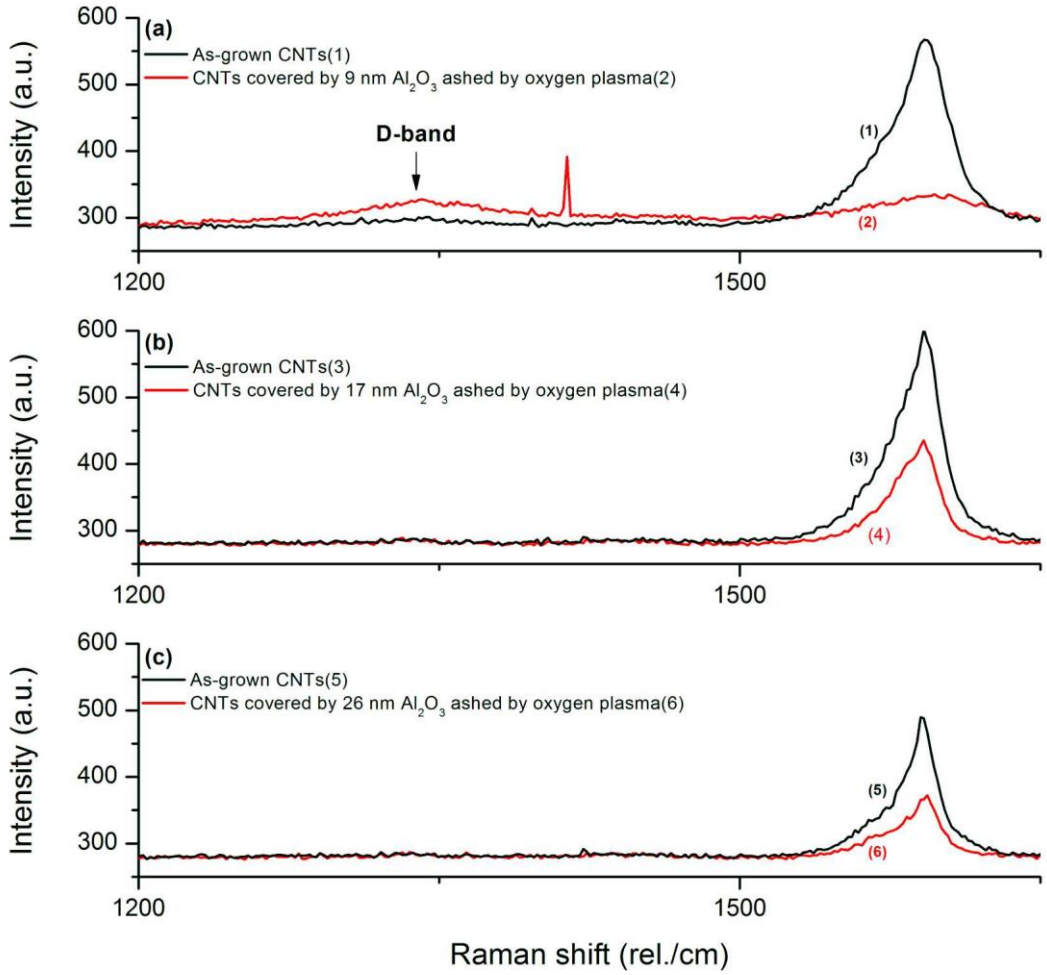


Figure 3-21 Raman spectra of as-grown CNTs (black) and Al_2O_3-covered CNTs after oxygen plasma ashing (100 W for 30 s) (red) for different Al_2O_3 thicknesses of (a) 9 nm; (b) 17 nm; (c) 26 nm [63] (a: C#Ox2-C1, b: C#Ox2-C2, c: C#Ox2-C3). © 2014, Elsevier

The Al_2O_3 layer needs to be thick enough so as to shield the CNT from harsh plasma ashing. An experiment was designed to determine the minimum required thickness of the protective Al_2O_3 layer for oxygen plasma ashing. In this experiment, as-grown CNTs on three oxidized Si chips were covered with three different thicknesses of the ALD Al_2O_3 layer, i.e. 9 nm, 17 nm and 26 nm respectively. Raman inspection was performed on these three chips before the ALD deposition and after the oxygen plasma ashing (100 W for 30 s). The measured Raman spectra of these three samples are plotted in Figure 3-21 [63]. For the CNTs covered with 9 nm Al_2O_3, the D-band intensity increased after the plasma treatment, which was not seen in the other two spectra of the CNTs covered with 17 nm and 26 nm Al_2O_3. As a result, the minimum thickness of ALD Al_2O_3 is in the range of 9 nm to 17 nm. Note that the attenuation of the G-peak intensity on each sample is a consequence of the deposited ALD Al_2O_3 layer [78].

3.6.5. Alignment of photomasks

The requirement for high alignment precision in the integration process arose from the desire for a higher yield of CNTs grown across the bridge. As a result, the growth site was patterned closer to one end of a Si electrode so that the tolerance of the growth angle was

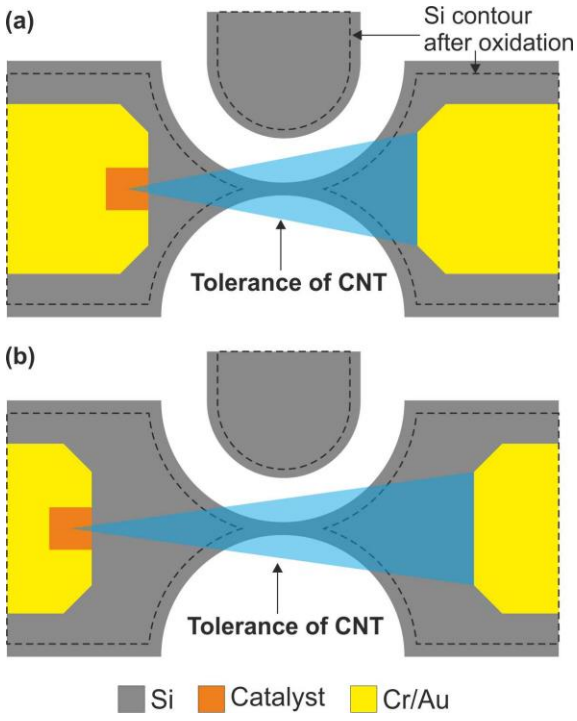


Figure 3-22 A catalyst window and metal leads were designed close to the bridge to increase the tolerance of the length and orientation of as-grown CNTs.

larger and the required CNT length was shorter, as illustrated in Figure 3-22. To achieve this, a catalyst window needed to be aligned to the end of the narrow and short oxide bridge, and hence, the alignment tolerance became smaller. Furthermore, to electrically contact the CNTs, the metal leads should be well aligned to the as-grown CNTs, whose ends were located at the small front ends of the Si electrodes.

A suitable alignment marker is essential for good alignment. In the integration process, after mechanical polishing, the edges of Si structures were rounded, which made it difficult to align to the round-edged structures in an alignment marker. To resolve this problem, the alignment marker was modified. As shown in Figure 3-23, arrow-shaped alignment markers patterned in the Si layer were surrounded by narrow trenches (0.8 µm wide), which reduced the stress concentration on the edges during polishing. Moreover, the 0.8-µm trenches were filled up with oxide after thermal oxidation, and the resist thickness on top of the marker became more uniform. Both of these factors contributed to better visibility of the patterned alignment markers under a mask aligner. In addition, owing to the "arrow shape", two markers were aligned along a "visually guided line", which enhanced the visibility of small misalignments between the two alignment markers. With the refined alignment markers, the misalignment was typically within 0.5 µm.

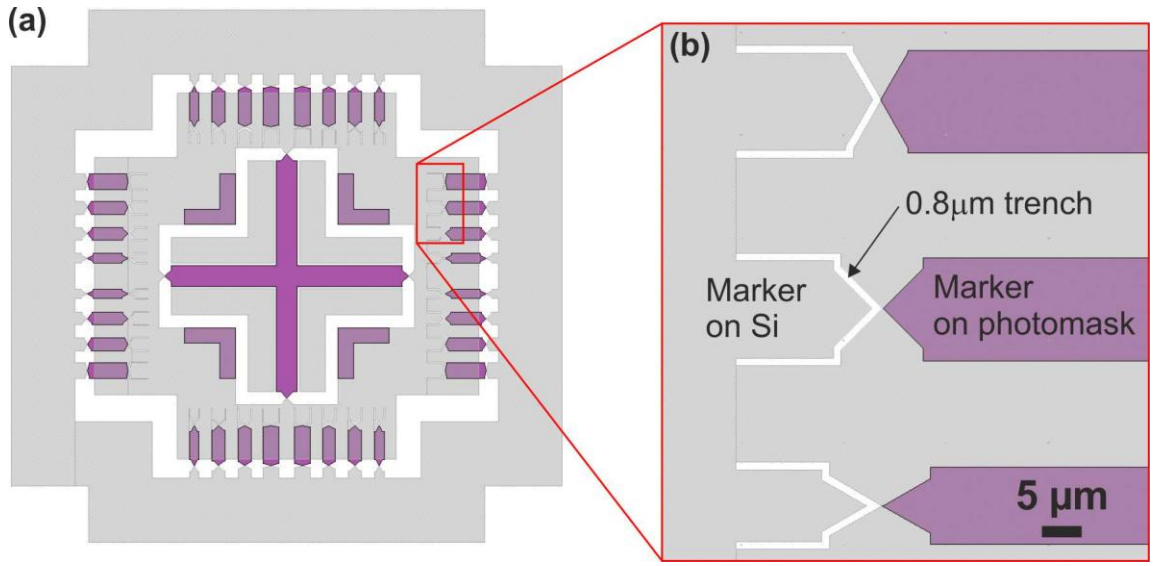


Figure 3-23 (a) Overview of the alignment markers; (b) close-up of the alignment markers. The arrow-shaped alignment markers could guide sight and enhance precision during alignment. With the alignment makers, the misalignment was typically within 0.5 µm.

In the early phase of the process development, all the lithography steps were based on UV lithography. During the development, two lithography steps, one for Si structures and one for metals, were replaced by DUV lithography. The UV lithography for patterning catalysts and the following lift-off procedure were well-developed, and hence, the catalyst patterning remained based on UV lithography. Two mask aligners were used in the process. However, a mismatch between alignment markers (less than 1 µm across a 18 mm by 18 mm chip) was often observed. This phenomenon was more obvious when the previous alignment marker was patterned by a different mask aligner. The Carl Süss MA6, for UV lithography, is an automatic mask aligner, while the ABM mask aligner, for DUV lithography, is a manual aligner. The mismatch was possibly caused by different mask contact pressures in the two different aligners, which influenced the flatness of the chip and consequently the alignment. As a result, using more than one mask aligner in the same process might influence the alignment precision. To improve this situation, the most critical alignment, the metal layer, was performed by the ABM DUV aligner, which was the same with Si structure patterning. Hence, the misalignment could be reduced.

3.7. Influence of liquid HF etching on metal contacts

After metallization, liquid HF etching is performed to leave CNTs suspended. The change of the contact resistance after liquid HF release can be used as an indicator in the investigation of the influence of liquid HF etching on metal contacts. A measured resistance of a CNTFET (R_m) is the summation of two contact resistances (R_c) and the resistance of the CNTFET channel (R_{cnt}). With the device layout, contact resistance cannot be extracted by a two-terminal resistance measurement. Alternatively, the change in the measured resistance (ΔR_m) can be representative of the change in the contact resistances (ΔR_c) if the resistance of the CNTEFT channel remains the same in the two measurements. The absence of the SiO_2 after release can lead to reduced gate capacitance (dielectric constant of SiO_2=3.9 > air). Hence, the apparent R_{cnt} will change after release even if the same gate voltage is applied. In order to reveal the change in contact resistances, the variations of the CNTFET channel resistance should be reduced. The on-state resistance of a CNTFET channel ($R_{cnt\text{-}on}$) mainly depends on the intrinsic properties of the CNT and the contact metals. Hence, $R_{cnt\text{-}on}$ was assumed to not be influenced by liquid HF release, and it was treated as a constant value in the following analysis. Figure 3-24 shows two I_d-V_{gd} curves measured on the same CNTFET (contact metals: 2 nm Cr/ 200 nm Au) before and after the

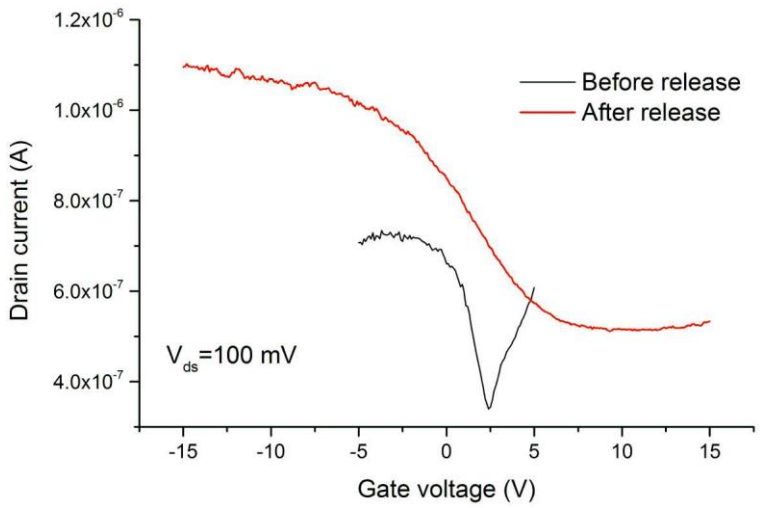


Figure 3-24 Transport measurements of a CNTFET before and after liquid HF release (D#20-5A_C#SOIC3-R3C2).

liquid HF release. As expected, the curve was stretched with regard to the gate voltage, which was attributed to weaker gate modulation. The on-state resistance changed from 136 kΩ (before release) to 105 kΩ (after release).

To confirm the reproducibility, seven CNTFETs (contact metals: 2 nm Cr/ 200 nm Au) were fabricated in another process run and measured by the same settings. Some of the CNTFETs could not reach a saturated on-state regime, namely the I_d was still increasing slightly with more negative V_{gd}. As a result, the following comparison was made based on the minimum measured device resistance (R_{min}) in the applied V_{gd} range (±30 V). The measurement results of the seven CNTFETs are listed in Table 3-2. Three of these CNTFETs showed decreased device resistances, three showed increased resistances, and one remained nearly the same. The device resistances of the 7 CNTFETs were distributed in

Table 3-2 Minimum measured resistance (R_{min}) of 7 CNTFETs before and after liquid HF release (devices from chip C#SOIC3-R4C1).

Device#	#20-3E	#20-6B	#22-2H	#23-8g	#23-10H	#23-10G	#23-7g
R_{min} before release (kΩ)	193	191	296	214	130	181	317
R_{min} after release (kΩ)	139	224	196	160	215	298	319

the range of 130 kΩ to 317 kΩ, and the resistance difference after release was within ±117 kΩ. From the eight measured CNTFETs in these two experiments, the resistance change resulting from liquid HF release was more like variations, rather than a consistent degradation of the contacts between CNTs and metals. The fluctuation could be partially attributed to the resistance variation of CNTFET channel due to the limited V_{gd} range. In conclusion, the influence of liquid HF acid on the doubly-clamped metal contacts is considered to be minor.

3.8. Investigation of metal contact for long-term stability

It was reported that the adhesion Cr layer could influence the long-term stability of CNT device in ambient conditions if the metal contacts (2 nm Cr/ 60 nm Au) were not encapsulated [70]. The Cr layer was required to improve the adhesion between Au and SiO_2. In the integration process, SiO_2 on the Si device layer is removed together with the Al_2O_3 layer on the metal contact areas before metallization. Hence, metals are directly deposited on top of CNT and Si surfaces (Figure 3-2e). The adhesion between Si and Au enables Au as a one-component metal on Si surfaces [79, 80]. As a result, CNT devices contacted with Au alone or with Cr/Au are achievable using the integration process. To reveal the influence of Cr layer on CNT device stability, CNT devices contacted with 150-nm thick Au alone and with different thickness of Cr (0.5, 1, 2 nm) and 150-nm thick Au were fabricated.

3.8.1. 150 nm Au alone

In the lift-off process of a 150 nm thick Au layer, delamination was not observed. The 150-nm thick Au layer could be patterned on Si surfaces, as shown in Figure 3-25a. Without any

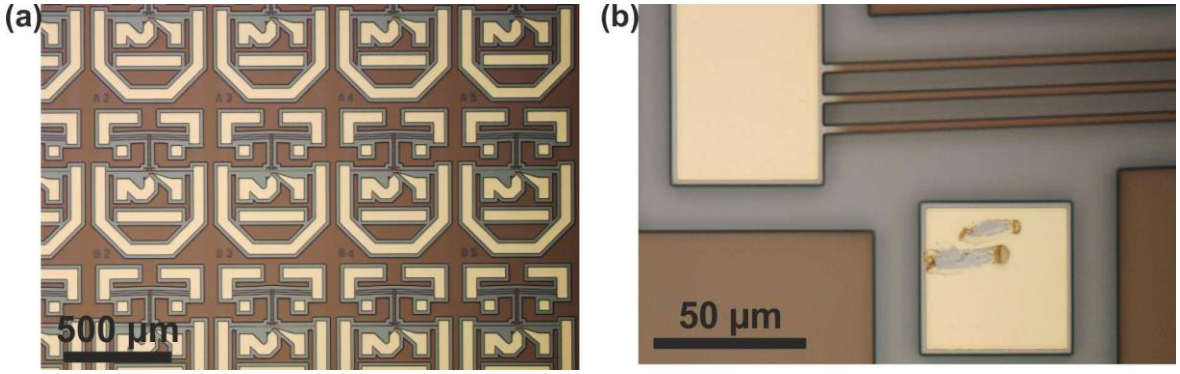


Figure 3-25 (a) A 150 nm thick Au layer was patterned by lift-off on Si surfaces; (b) the ruptures of the Au layer after probing (C#SOIC4s-150Au-1).

Table 3-3 Resistances distribution of the 20 monitored Au-contacted CNTFETs before and after liquid HF release.

	Before release	**After release**
R_m < 1 MΩ	5 devices	0
1 MΩ < R_m < 5 MΩ	14 devices	0
R_m > 5 MΩ	1 devices	18 devices (R_m=5~10 MΩ : 3 devices; R_m=10~50 MΩ :5 devices; R_m>50 MΩ : 10 devices)
Gate leakage	0	2 devices

adhesion layer, the smallest metal features patterned by lift-off were squares of 1.26 μm by 1.26 μm, which were the smallest patterns on the photomask for metallization. In the subsequent electrical measurements, it was observed that a probe needle could easily rupture the Au layer, as shown in Figure 3-25b. However, the electrical measurement could still be performed, but the resistances of the devices increased dramatically after liquid HF release. As Table 3-3 shows, before release, only one device (out of 20) showed a resistance higher than 5 MΩ, but after liquid HF release, the resistances of 18 devices (out of 18) were higher than 5 MΩ, and two devices were excluded due to gate leakage currents. A hint to the cause of the loss of contacts was found in an SEM observation of the monitored devices.

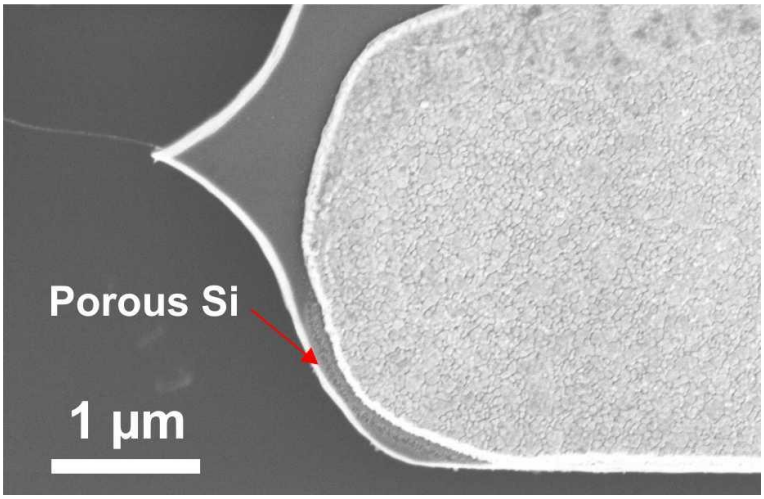


Figure 3-26 A Si electrode of an Au-contact CNTFET after liquid HF release. The porous Si formed only on the lower border of the Au lead, instead of all around the Au lead. This indicates that not all the Au layer was in intimate contact with the Si electrode. The poor physical contact between the CNT and the Au lead was assumed to be the root cause of the loss of electrical contact after liquid HF release (D#C1-C3_C#SOIC4s-150Au-1).

Figure 3-26 is an SEM image taken from one released device. The porous Si was found only around the lower border of the Au lead. Typically, if Si and Au are in good physical contact, porous Si will form around the entire metal lead border during liquid HF etching, as Figure 3-7 shows. Hence, it was assumed that the adhesion between Au and Si on the upper border of the Au lead was not sufficient and partial delamination occurred. Before release, a CNT was still attached to Au by van der Waal's forces, which were weak due to the weak interaction between Au and CNT [81]. During the release procedure, the forces were not sufficient to hold CNTs in position. This might explain the increase in contact resistance of the Au-contacted devices after liquid HF release. To enhance the adhesion, another SOI chip (C#SOIC4s-150Au-2) with 4 non-suspended Au-contacted CNTFETs was annealed at 270 °C for 15 min in vacuum (a recipe from [82]). Two of these CNTFETs with higher resistances ($R_{A4\text{-}D2}$=4694 kΩ and $R_{AE\text{-}C3}$=5192 kΩ) lost electrical contacts after annealing, while increased resistances were measured in the other two CNTFETs, $R_{BN1\text{-}D1}$=419 kΩ (before)/ 1321 kΩ (after); $R_{BN1\text{-}A3}$=375 kΩ (before)/ 2737 kΩ (after)).

3.8.2. 0.5 nm/ 1 nm/ 2 nm Cr and 150 nm Au

Suspended CNTFETs with different thicknesses of adhesion Cr layer and 150-nm thick Au were fabricated respectively on three SOI chips. The conditions of these three SOI chips are listed in Table 3-4. The CNTFETs contacted by a Cr adhesion layer and Au layer did not lose electrical contacts after liquid HF release, unlike the CNTFETs contacted with Au alone. These 47 CNTFETs were stored in ambient air (relative humidity= 47%, temperature= 21°C, in the ETH FIRST cleanroom) for two months. During this period of time, they were measured periodically. As mentioned previously in section 3.7, the changes in the measured device resistance (ΔR_m) can be representative of the variation in the contact

Table 3-4 The conditions and abbreviations of the three SOI chips for the long-term stability investigation.

Metals	**0.5 nm Cr/ 150 nm Au**	**1 nm Cr/ 150 nm Au**	**2 nm Cr/ 150 nm Au**
Chip	C#SOIC5-0.5Cr150Au	C#SOIC5-1Cr150Au	C#SOIC5-2Cr150Au
Number of devices	19 devices	15 devices	13 devices
Monitoring duration	2 months	2 months	2 months

Table 3-5 Stability of the suspended CNTFETs with good electrical contacts ($R_{m,initial}$<1 MΩ).

Metal	# of devices ($R_{m,initial}$ < 1 MΩ)	# of devices (R_m<1 MΩ after 2 months)
0.5Cr150Au	12	11 (92%)
1Cr150Au	10	7 (70%)
2Cr150Au	7	5 (71%)

resistances (ΔR_c) if the channel resistance remains the same, i.e. ΔR_{cnt}= 0. To reveal the variation of the contact resistances, the devices were measured at the same gate voltage, V_{gd}= 0 V, to keep a CNTFET channel as a resistor with a constant resistance. The measured device resistances (V_{gd}= 0 V) of the suspended CNTFETs with different thicknesses of Cr and 150 nm Au are shown in Figure 3-27. The device stability is represented by the metal contact properties. To evaluate the device stability of these measured CNTFETs, a criterion for a device with good contacts was set as R_{min}<1 MΩ. Initially, 26 suspended CNTFETs (out of 47) fit the resistance criterion. After 2 months, more than 70% of these devices remained qualified. The details are listed in Table 3-5. It is promising that such high ratio of the monitored CNTFETs could remain in a relatively low resistance range in ambient air for 2 months. Moreover, there is no noticeable correlation between the yield and the Cr thickness if Cr is not thicker than 2 nm.

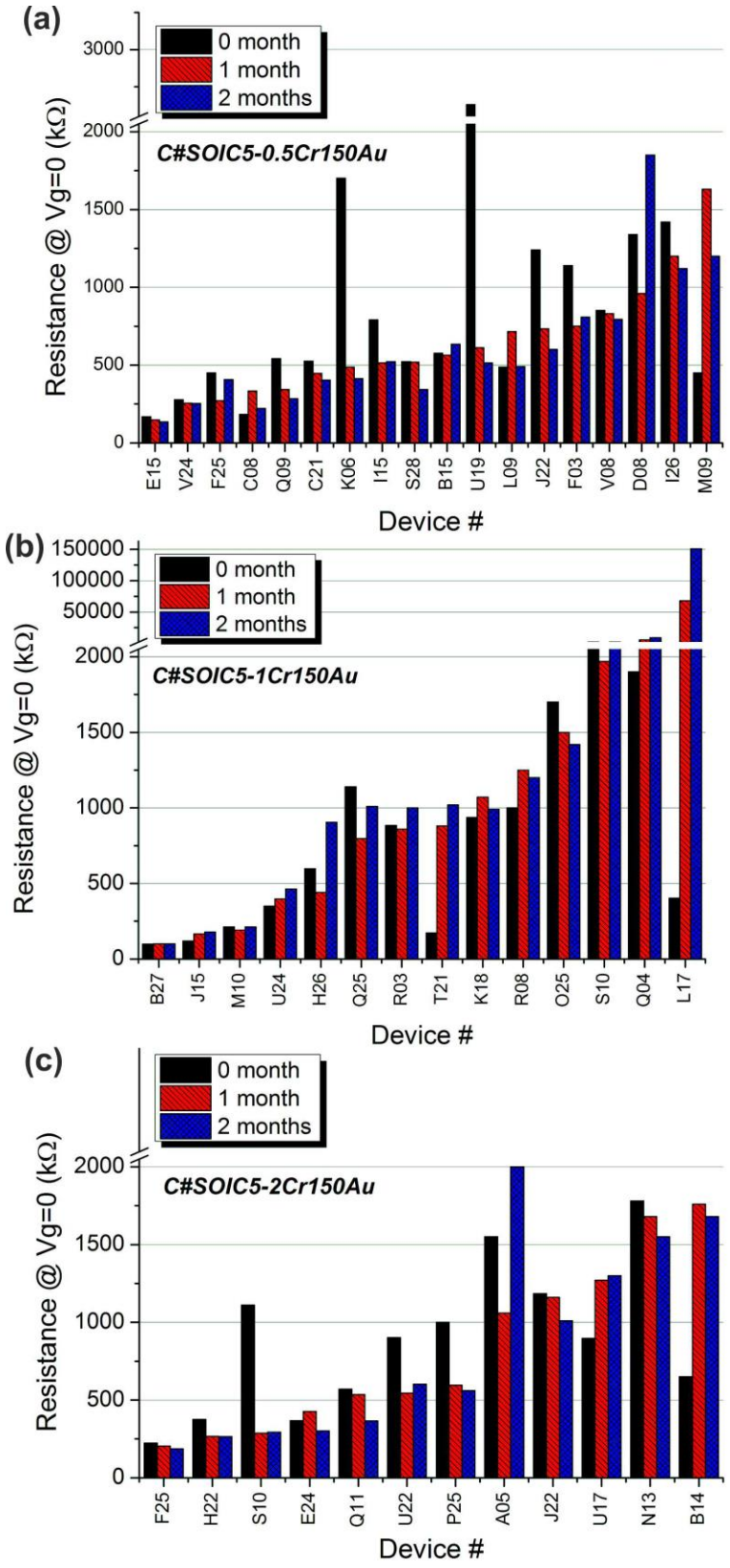


Figure 3-27 Device resistances of suspended CNTFETs with (a) 0.5 nm Cr, (b) 1 nm Cr, (c) 2 nm Cr and 150 nm Au stored in ambient air within 2 months.

3.9. Discussions

3.9.1. Features of the integration process

- **Key features**

The key features of the integration process are the supporting oxide bridge and the protective ALD Al_2O_3 layer. With the assistance of the supporting oxide bridge, CNTs are not suspended until the final liquid HF release. As a result, there is no concern for the rupture of CNTs due to the capillary forces or viscous forces during post-growth wet processing. In addition, the thin ALD Al_2O_3 layer deposited right after CNT growth can prevent as-grown CNTs from intimate contact with resists during lithography. Hence, the contamination issue caused by sticky resists can be avoided. The effectiveness of these two features in preventing rupture and contamination was confirmed by the clean surfaces of the fabricated suspended CNTs (Figure 3-8) and the low D/G ratio of the measured Raman spectrum (Figure 3-9).

- **Post-growth top metallization**

The post-growth metallization avoids the degradation of metals at the elevated growth temperature. As the electrical measurement results showed in section 3.5.2, the resistances of the fabricated CNTFETs were distributed in the range of few hundred kΩ. The resistances of the Cr/Au contacted CNTFET could be as low as 91 kΩ. The device resistances are comparable with or even lower than those reported by the CNT-MEMS integration processes in literature [30, 40, 50]. In addition to improved electrical contacts, top metallization also enables the doubly-clamped mechanical clamping configuration. The robust clamping is helpful to hold the suspended CNTs during liquid HF release.

- **Selective removal of undesired CNTs**

The combination of the oxide bridge and the ALD Al_2O_3 layer also grants the selective protection of correctly-directed CNTs during oxygen plasma ashing. The selection method employed here removes undesired CNTs and preserves the well-aligned CNTs, unlike the active growth control by external forces [45, 83] or on a crystalline substrate [43]. This method does not require sophisticated electrical field or gas flow control, and it is not limited to only dedicated substrates, like sapphire or quartz substrates. The selectivity depends on the topography of the substrate, and hence it is not possible to selectively

remove CNTs on a flat surface by this method. However, this selection method matches perfectly with CNT-MEMS integration, because a supporting structure can easily be patterned in MEMS structures. Consequently, the orientation of the remaining CNTs can be defined by lithography, and the control of any desired directions is possible on one individual chip or in one growth run.

- **Formation of micro-trenches after CNT growth**

In most of the CNT-MEMS integration processes [30, 40, 49, 50], micro-trenches for suspended CNTs are patterned prior to CNT growth so as to prevent damage and contamination due to post-growth processing. However, while CNTs grow across the micro-trench, they are more likely to attach to the side walls of neighboring MEMS structures, instead of the predefined metal contacts on the top surfaces. Hence, the metals could not contact the CNTs properly. In contrast, in the present integration process, CNTs grow on the top of the oxide bridge, which is beneficial for effectively contacting CNTs by top metals.

3.9.2. Gate modulation

Considering the single device layer of an SOI chip and the compatibility with the integration process, a Si side-gate electrode, located laterally close to a suspended CNT, is the simplest gate configuration for a CNT field effect transistor.

- **Reduction of the gate distance by DUV**

The distance between the CNT and the side gate electrode, so-called gate distance, was defined by lithography. To improve the gate modulation of a CNTFET channel, DUV lithography was employed to shrink the gate distance. The gap between the Si bridge and the side-gate was 0.5 µm on the photomask. If a CNT was grown along the center of the bridge, the final gate distance was 1.1 µm. This gate distance was half of the minimum achievable gate distance by UV lithography (assuming the resolution of UV lithography was 1 µm). Note that the widening of gate distance (from 0.5 µm to 1.1 µm) was mainly due to the thermal oxidation.

- **Simulation of gate potential**

An electrical potential distribution simulated using the commercial simulation software COMSOL is shown in Figure 3-28a. If V_{gd}= 10 V is applied on the side-gate, the potential at the middle of the gap between the source and drain electrodes is 2.7 V (which is 1.1 µm

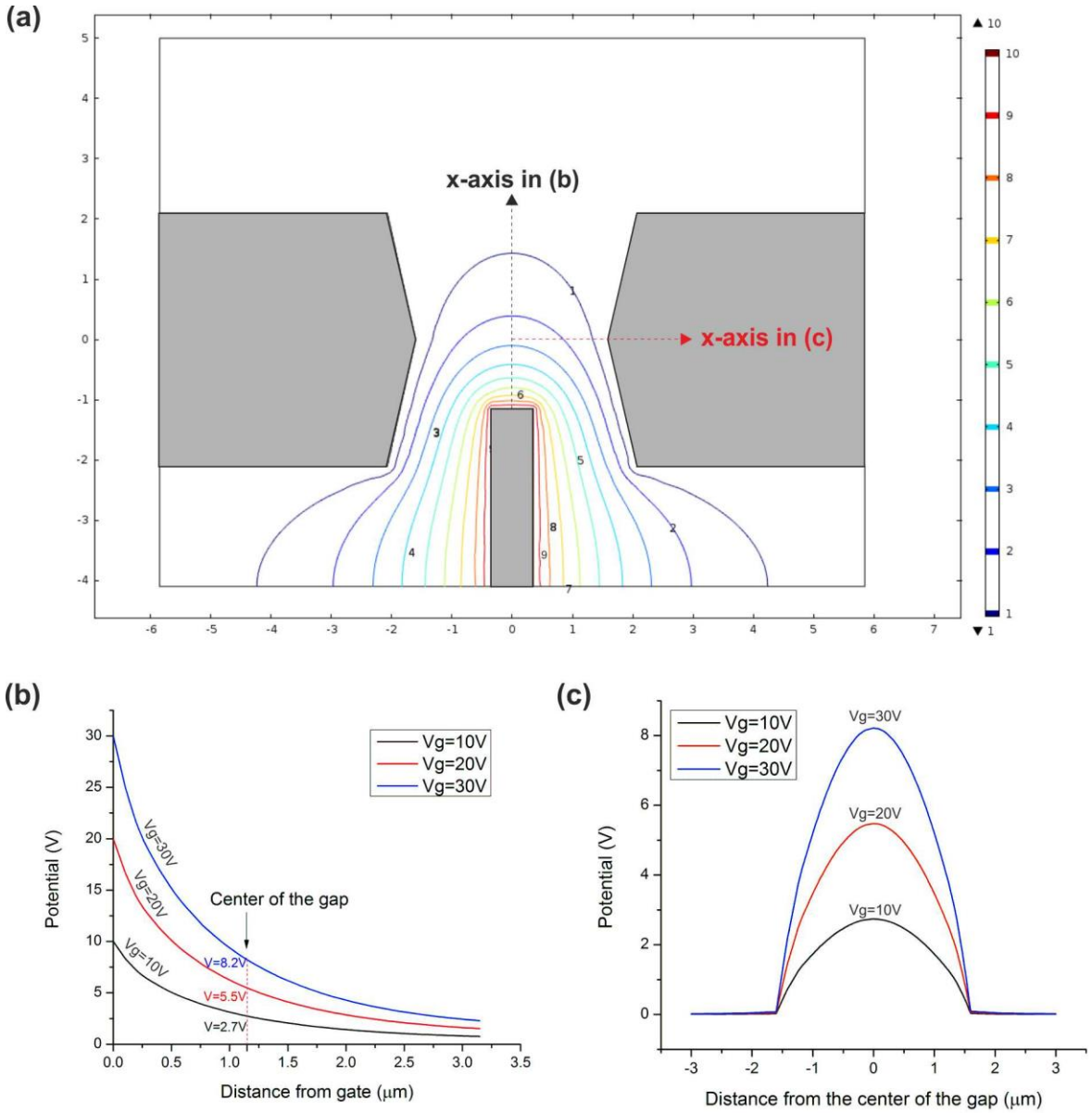


Figure 3-28 (a) Simulation of the electrical potential in a three electrode configuration (V_{gd}= 10 V is applied on the side-gate and 0 V on the other two electrodes); (b) the potential distribution along the axis of the side-gate with different gate voltages; (c) the potential distribution along the direction of a CNT, i.e. along the axis of the Si electrodes.

away from the gate). Due to the screening effect by the source and drain electrodes, the electrical potential drops with the gate distance quickly (Figure 3-28b). Consequently, a higher side-gate voltage would be required to provide a sufficient electric potential to modulate the CNTFET channel. In addition to the potential at the center of the CNT, the electrical potential along the CNT is plotted in Figure 3-28c. Assuming that the CNT is aligned to the center of the Si electrodes, only the small segment at the center of the CNTFET channel can be efficiently modulated by the gate field. Considering the potential screening, the gate voltage was typically set between V_{gd}= 10 V to V_{gd}= 30 V in the transport measurement.

- **Double side-gates**

The root cause of the severe attenuation of the gate field could be attributed to geometrical constraints imposed by CNTs. The distance between two opposite Si electrode was squeezed such as to shorten the required CNT length and to increase tolerance of growth direction. The reduction of the gap between the source and drain enhances the screening effect. A double side-gate configuration can compensate for the screened gate potential from the one gate. An example is shown in Figure 3-29. Equipped with double side-gates, the small band gap semiconducting CNTFET could transit from on-state at V_{gd}= −10 V to off-state at V_{gd}= 22 V. Double side-gates ensure that a CNT which is not perfectly aligned

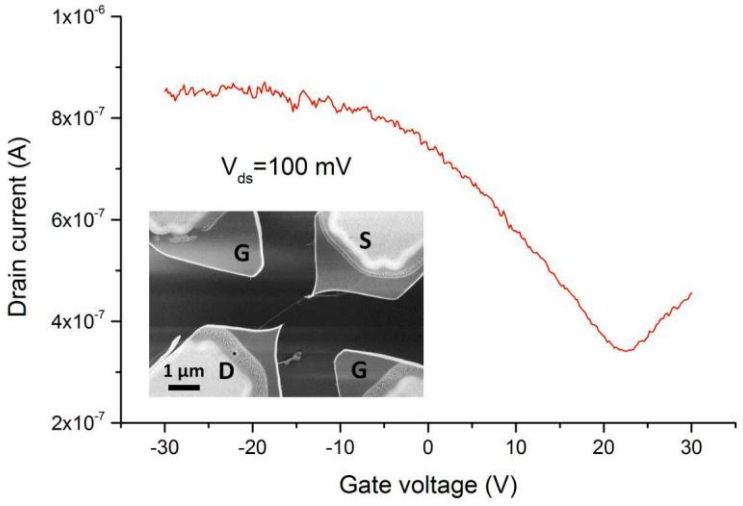


Figure 3-29 Transport measurement of a suspended CNTFET equipped with double side-gates. The inset is the SEM image taken from the CNT after the measurement (D#11H_C#SOIC3-R3C5). © 2011, IEEE

to the center of the electrodes is not on the far side of the (single) gate electrode.

- **Modulation of Schottky barrier**

The gate voltage modulates the resistance of the CNTFET channel as well as the widths of the Schottky barriers at the metal-CNT contact interfaces. According to the investigation in [84], the modulation of Schottky barriers could be more important than the channel modulation for a CNTFET. Considering the configuration of a suspended CNTFET with side gates, like the device shown in the inset of Figure 3-29, the Schottky barriers at the metal-CNT contact interfaces could hardly be modulated by the gate voltage since the gate potential was mostly screened by the thick Si electrodes. A simulation shown in Figure 3-30 illustrates the decay of the gate potential on the top surface of a Si electrode. The potential was extracted from a plane above the Si surface by 10 nm. Even if the gate voltage is as high as 30 V, the potential at the Si border is still lower than 0.1 V. The inefficient modulation of the Schottky barriers might be the reason why CNTFETs with double side-gates still require relatively high gate voltages for transistor operation. The weak coupling between the side-gate and Schottky barriers can be improved without adding another structural layer for top-gates or introducing complex process steps to change the height of

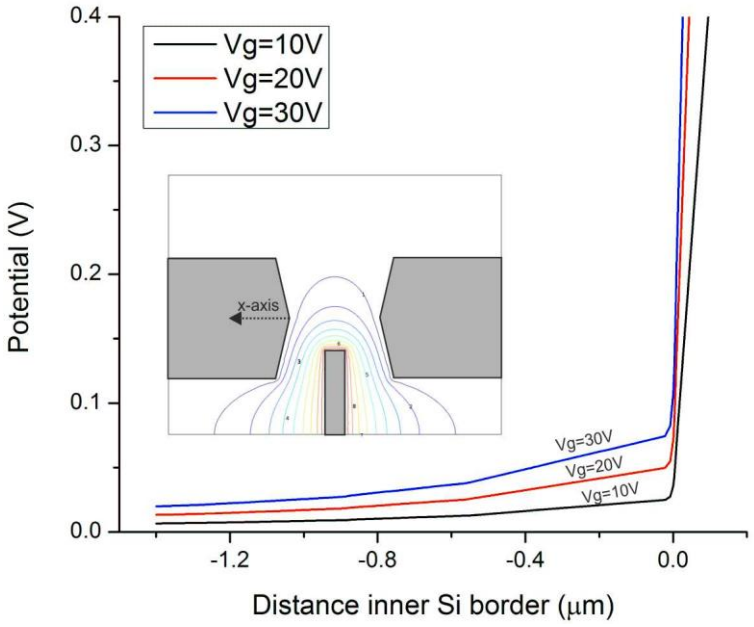


Figure 3-30 Electrical field decay along the Si electrode with different side-gate voltages (the potential was extracted from a plane above the Si surface by 10 nm).

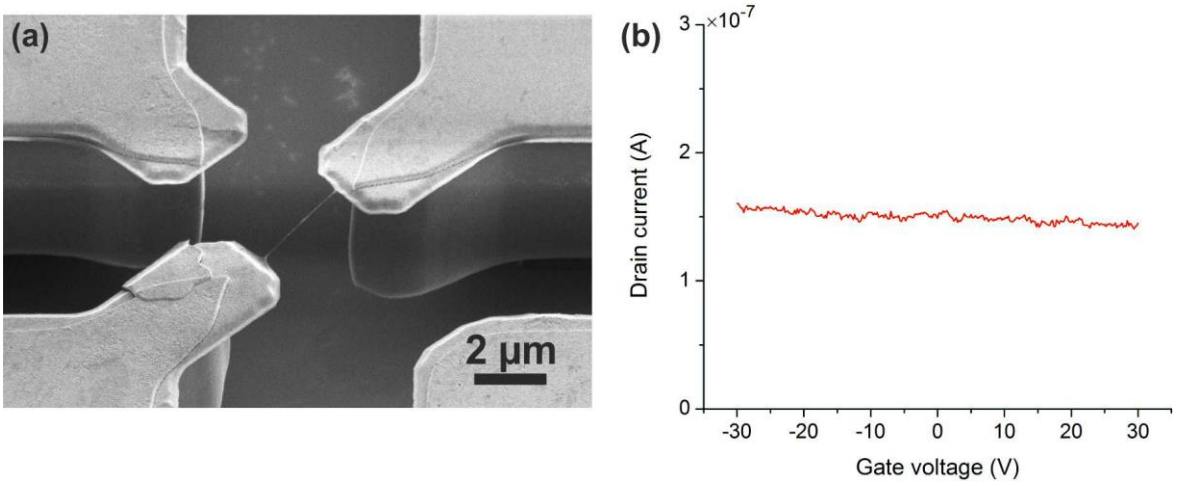


Figure 3-31 (a) SEM image of a suspended CNTFET with protruding contact metals; (b) Transport measurement of the CNTFET shown in (a)(V_{ds}= 0.2V) (D#LF3FET4L_C#SOIC2-R6S3).

the side-gate. The idea is simply to move the CNT-metal contact toward the border of the Si electrodes by enlarging the metal leads. The transport measurement shown previously in Figure 3-10 reveals the characteristics of a suspended CNTFET with enlarged metal leads. The improved gate-coupling shown in the transport measurement demonstrates the importance of the modulation of the Schottky barriers. If the metal lead is larger than the Si electrode, the protruding metal lead will screen the gate potential and worsen the modulation of the Schottky barrier. A CNTFET with protruding contact metals is shown in Figure 3-31a. The metal leads were larger than the Si electrodes underneath. The electrical contacts between the CNT and the metals were not located at the border of the protruding metal leads, but at the Si border. This is because the adhesion Cr layer in the protruding part tended to be oxidized quickly. As a result, the gate potential was mostly screened by the protruding metals, which might have led to the weak gate coupling in the transport measurement in Figure 3-31b.

In conclusion, side gate is the simplest gate configuration for the integration process, but the gate potential tends to be attenuated by the screening effect of the thick Si electrodes. Double side-gates can improve the modulation of the CNTFET channel, and enlarged metal leads (as large as the Si electrodes) can improve the modulation of Schottky barriers.

3.9.3. Liquid HF influence on CNTs

The suspended CNTs fabricated by the integration process typically show a low D-band peak in Raman inspection, as shown in Figure 3-9. The low intensity ratio of D-band peak

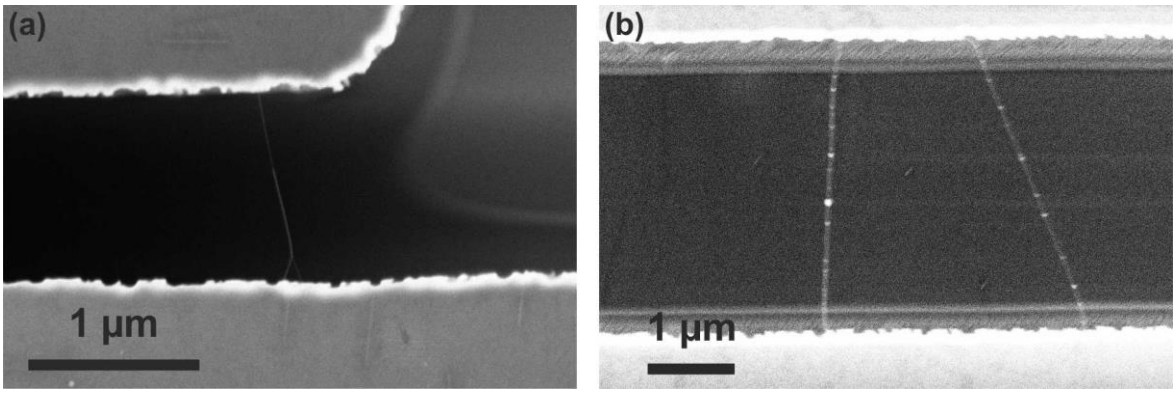


Figure 3-32 (a) As-grown suspended CNTs before the drying test; (b) suspended CNTs after the drying test in critical point dryer. These CNTs were from the same test SOI chip.

to G-band peak suggests that the high CNT quality was preserved throughout the process, including the final liquid HF release. However, different findings were reported in literature. A reversible D-band peak was measured on the same CNT after different runs of liquid HF release and drying process [85]. The other dipped the same CNT sample into liquid HF to remove the oxide gradually and compared the D-band peak intensity after each dip [86]. In these two investigations, it was mentioned that liquid HF acid as well as the residues of HF etching had a negative influence on CNTs, concluded from increased D-band peak intensity. The different conclusions about the influence of liquid HF release might result from the quality of the as-grown CNTs and the liquid HF release procedures. In the present process, CNTs are grown at an elevated temperature of 850 °C, and the as-grown CNTs typically show very low D/G ratios. In general, CNTs with fewer intrinsic defects are chemically more inert. Secondly, the aqueous by-products of the SiO_2 etching in liquid HF acid, H_2SiF_6 and H_2O, can be rinsed away by sufficient de-ionized water. In our experiments, there were typically no visible residues found by SEM observation or detectable contamination by Raman inspection. One potential contamination could originate from the drying procedure in a critical point dryer. From previous experiences, residues were sometimes found on the suspended CNTs after drying in a critical point dryer. One example is shown in Figure 3-32. As-grown suspended CNTs appeared clean before any processing (Figure 3-32a), but after a drying test in a supercritical point dryer, some contamination decorated the suspended CNTs (Figure 3-32b).

The oxidation of carbon atoms by nitric acids is employed to functionalize the inert surfaces of CNTs [87, 88], but oxidation is not involved with liquid HF acid. Additionally, the

fluorination of CNTs does not occur at room temperature [89]. Summarizing the findings from the literature and our experiment results, it is concluded that liquid HF acid does not degrade low-defect CNTs.

3.9.4. Adhesion of Au-Si

The adhesion between Au and Si enables the patterning of micro-size Au leads on Si surfaces without delamination during wet lift-off procedure. The non-suspended CNTFETs with Au contacts were able to be electrically characterized by transport measurements. However, the adhesion seemed insufficient to maintain CNTs in good contact with Au for further processing. The resistances of these Au-contacted CNT devices were increased dramatically after liquid HF release or annealing. From the observation of a liquid HF released device (Figure 3-26), partial delamination was found in the Au lead border. This might result in the increased resistances or loss of electrical contacts. Hence, a thin adhesion Cr layer is required (as thin as 1 nm) for further processing and reliable probing.

3.9.5. Long-term stability of CNTFETs in ambient air

From the investigation of device stability in section 3.8.2, the thickness of the adhesion Cr layer (0.5 µm to 2 nm) was found to be irrelevant to the resistance stability for two months. Moreover, more than 70% of the selected CNT devices did not degrade within the two months. This is promising, because the thin adhesion Cr layer enables the liquid HF release step, and at the same time, it does not cause severe issues in device stability. Moreover, an investigation of non-suspended CNTFETs with different thicknesses of Cr (0.5, 1, 2 nm) and 150-nm thick Au showed similar resistance stability within two months (more details in

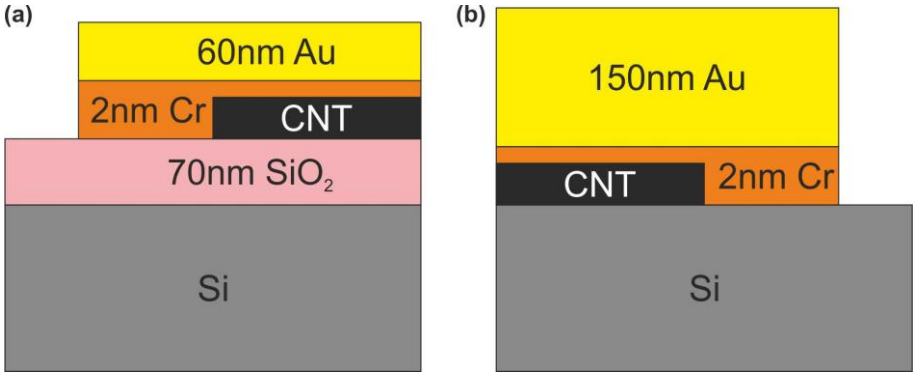


Figure 3-33 Comparison of the contact configuration; (a) contact profile redrawn from [70]; (b) contact profile in the integration process. The major differences are the SiO_2 layer and the thickness of the Au layer.

described in Appendix II). The consistent results of suspended and non-suspended CNT devices indicate liquid HF release does not retard the device stability. In addition, the hypothesized metal oxidization did not cause severe degradation within 2 months, which is different from Helbling's finding [70]. The discrepancy may arise from different conditions of metal contacts. A comparison of the contact configuration in [70] and in the present integration process is shown in Figure 3-33. Two major differences are the oxide layer and the thickness of the Au layer. In the integration process here, metals are directly deposited on CNTs and Si surfaces. The absence of the SiO_2 on top of Si enables inter-diffusion of Au, Cr and Si [80, 82, 90]. In addition, the thick Au may also delay the oxygen diffusion from surrounding along the grain boundaries to the Cr/Au interface, and hence the oxidation is postponed. Another difference is the cleanliness of the contact interfaces. In the integration process, the contact interface of Si/CNT/Cr/Au remains resist-free due to the ALD Al_2O_3 protective layer. The clean contact interface may be beneficial for long-term stable electrical contacts. However, it is difficult to clarify which factor is mainly responsible for the discrepancy. Further studies are required to clarify the hypothesis of oxygen-blocking thick Au, the inter-diffusion due to the absence of SiO_2, and the clean contact interfaces.

3.10. Summary

With the physical support of the oxide bridge and the protective ALD Al_2O_3 layer, post-growth wet processing can be performed without the concerns of the rupture of CNTs and contamination of resist during the lithographic processing. Taking advantage of the oxide bridge together with the Al_2O_3 layer, undesired suspended CNTs can be removed by oxygen plasma ashing, and the correctly-aligned CNTs can be preserved. The selection enlarges the process tolerance concerning the adsorption density of the catalyst solution, and it can also improve the yield of working devices by eliminating gate leakage currents. The following top metallization with the clean contact interfaces with CNTs resulted in reproducible and reasonably low resistances, as low as 91 kΩ. In addition to the improved electrical contacts, top metallization also contributes to the robust doubly-clamped boundary condition. All the lithography steps in the integration process are based on photomasks, and hence it is feasible to scale up the integration process to a wafer-level process.

The fully-developed integration process enables the investigation of essential CNT device properties, such as the influences of processing on CNTs, long-term device stability in

ambient air, and optimized structural configuration for better gate coupling. These studies are helpful in understanding the behavior of CNT-MEMS devices.

Chapter 4 Embedded micro-actuation system

Bent-beam electro-thermal actuators are capable of generating large forces (2.5 mN) as well as large displacements (20 μm) at low actuation voltages (5~12 V) [91]. Moreover, high precision control of the displacement has been demonstrated [92]. Hence, thermal actuators have been commonly employed in straining nano-structures [36, 38, 92-95]. Considering these advantages, electro-thermal bent-beam actuators were selected for straining suspended CNTs.

4.1. Design of an embedded micro-actuation system

To design the thermal actuator, the material properties, such as the electrical conductivity and residual stress of the Si device layer, were first measured. In addition to the actuator, a compact mechanical structure was designed to electrically and thermally insulate CNTs from the thermal actuator. This structure can also transfer actuation force so as to strain CNTs.

4.1.1. Characterization of the Si device layer

The electrical conductivity is an important design factor because it determines the amount of heat generated in a Si bent-beam at a given actuation voltage. The heat subsequently influences the displacement and force of the actuator. In addition, the residual stress of the Si device layer is partially relaxed after liquid HF release. The stress relaxation causes a deformation of the actuator, resulting in an uncontrolled strain in the CNTs. The remaining stress becomes the internal stress of the actuator. If the internal stress overwhelms the structural rigidity, the beams of the actuator would buckle. Thus, the electrical conductivity and the residual stress are important design parameters.

- **Electrical conductivity**

The electrical conductivity of the device layer of the SOI wafer was measured by a four-point probe at different temperatures on a thermal chuck. The temperature range of the measurement was between T= 20°C and T= 55°C and was limited by the thermal chuck. In the small temperature range, the relationship between the conductivity and the temperature was simplified as a linear dependency. The temperature dependency of the conductivity of the device layer is expressed as $\sigma_e = \sigma_0 - C_0 \cdot T$, where σ_0= 32152 S/m, C_0= 25 S/(m·K), and T is the temperature in Kelvin.

Table 4-1 Measured residual stresses on the three SOI chips.

	Process	Extracted stress
Chip#1	ICP Liquid HF release	−3~−6 MPa
Chip#2	ICP Thermal oxidation (*T*=995 °C for 5.5 hours) Liquid HF release	−22~−24 MPa
Chip#3	ICP CNT growth (*T*=850 °C for 15 min) Liquid HF release	−3~−6 MPa

- **Thermal stress**

The stress of the Si device layer of a SOI wafer originates from the thermal expansion coefficient mismatch between Si and SiO_2 during the wafer fabrication procedure. The stress is affected by high temperature process steps due to an annealing effect [96]. During the integration process, three high temperature steps are involved, i.e. twice thermal oxidation and the CNT growth. The first thermal oxidation (*T*= 995°C for 5.5 hours to convert the Si supporting bridge into SiO_2) is taken into account. The second thermal oxidation (*T*= 995°C for 15 min to produce a barrier layer for CNT growth) is much shorter and considered as a minor effect. Thus, it is not investigated here.

Silicon bent beams were fabricated on three SOI chips to extract the residual stresses after different process steps, as listed in Table 4-1. After release procedures, the bent beams became suspended, and the stresses were partially relaxed by deforming the bent beams. By measuring the relative displacement of a bent beam after release, the thermal stress was calculated. As listed in Table 4-1, chip#1 was used to measure the initial stress of an as-delivered SOI wafer, chip#2 for thermal oxidation (*T*= 995 °C for 5.5 hours), and chip#3 for CNT growth process (*T*= 850 °C for 15 min). The initial stress was compressive with a magnitude of 3~6 MPa. On chip#2, increased compressive stresses, in range of 22~24 MPa, were measured. The relatively short duration and lower temperature of the CNT growth process did not cause noticeable change in the residual stresses, and the extracted residual stress was similar to the initial value. These results can be explained by the thermal annealing effect reported in literature [96]. The glass transition temperature is between *T* = 900 °C and 950 °C. A process performed at a temperature which is higher than this transition temperature can alter the interface force between the Si device layer and buried

oxide layer. This explains the noticeable change only observed after the thermal oxidation (T= 995 °C), but not after the CNT growth (T= 850 °C).

These measured electrical conductivity and residual stresses were taken into account in the following design of the actuation system.

4.1.2. Insulation between a suspended CNT and a thermal actuator

Bent-beam actuators are suitable for straining CNTs since they enable large output forces, large displacements, and high displacement precision. This actuation mechanism also has drawbacks. The heat generated in the thermal actuator during the operation can influence the CNT under test. To reduce the heat flux to the CNT, additional heat dissipation routes were added between the CNT and the actuator [38, 93]. In addition to the heat transfer, the actuation voltage can result in a voltage difference across the CNT, which would consequently cause an electrical current to flow through the CNT. This current would complicate the analysis of the electrical response of the CNT to strain. If a high electrical current (> 1μA) is induced, the CNT might be damaged. As a result, the CNT needs to be electrically insulated from the actuator. An approach of adding an insulation material to make two components electrically insulated and mechanically connected was demonstrated by Tsai et al. [97]. Another approach of using a symmetrical structure and symmetrical

Table 4-2 Summary of the approaches in literature for thermal and electrical insulation.

Type of insulation	**Method**	**Remarks & implementation in the integration process**
Thermal [38,93]	Enhanced heat dissipation to the substrate	It causes more heat loss and thus higher driving power is required.
Electrical [97]	Adding an insulation layer	It is challenging to maintain a dielectric material in liquid HF etching of the developed integration process.
Electrical [92]	Symmetrical structure and biasing to virtually set the central structure to be 0 V	The fabrication of a non-perfectly symmetrical structure would make voltage of the central structure deviate from the ideal 0 V. A high actuation voltage would enlarge the deviation. Hence, the actuation voltage is dependent on the fabrication tolerance.
Thermal & electrical [98]	Producing a thick oxide layer as an insulation layer for heat and electrical current	It is not feasible to perform thermal oxidation when CNTs are integrated.

electrical biasing without any additional insulation material was introduced by Shaoning et al. [92]. Using this approach, the voltage of the central structure is ideally 0 V. The influence of the actuation voltage on the specimen, which is located at the center, can be reduced. Another solution to decouple the electrical current and heat flux at the same time is to embed a thick oxide layer in the thermal actuator structure [98]. Some of these methods are not efficient in thermal and electrical insulation between the CNT and the thermal actuator, while others are difficult to implement in the integration process. These mentioned approaches in literature are summarized in Table 4-2. A versatile de-coupling "adapter" structure was designed to efficiently insulate heat and electrical current at the same time. The adapter is compact in structure, and it can be fabricated using the integration process. No additional deposition processing is required. In addition to efficiently blocking the heat flux and electrical current from a thermal actuator, the adapter can buffer the residual stress induced deformation of a thermal actuator, which is essential for the as-grown CNTs integrated into thermal actuators. The following sub-sections describe the working mechanism of electrical insulation, heat reduction, and mechanical buffer respectively.

- **Electrical insulation**

The configuration of the adapter is compact. It consists of two discrete Si structures, one hook and one T-shaped structure, as shown in Figure 4-1b. Taking advantage of the native oxide (~1 nm), formed on the Si side walls after liquid HF release, a small voltage difference between the hook and T-shaped structure can be insulated. To reduce the voltage difference across the adapter, two actuation voltages (V_a) with identical amplitudes but opposite polarities are applied, as shown in Figure 4-1a. Thus, the voltage of the actuator center is 0 V. Moreover, because the hook serves as the drain electrode for the integrated CNTFET, it is electrically grounded via a long Si suspension beam. As a result, the voltage difference between the hook and T-shaped structure is ideally 0 V. However, device geometries are always subject to fabrication tolerances, and consequently the voltage difference will slightly deviate from the ideal value of 0 V. The deviation is expected to be small, and it is increased with the actuation voltage. Considering the maximum sustainable electrical field of a thin oxide, ~10 MV/cm [99], the maximum sustainable voltage will be approximately 2 V, provided that the thickness of the native oxide is 1 nm on Si side walls. As a result, the thin native oxide is capable of insulating the small voltage difference across the adapter for certain actuation voltage range.

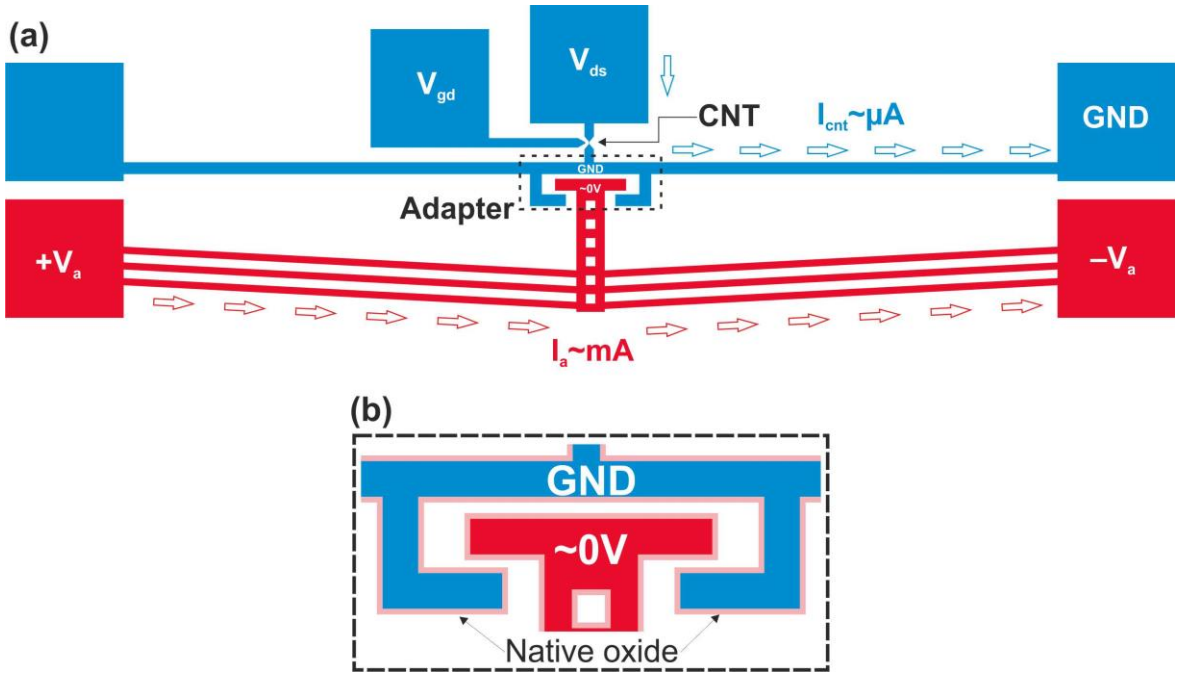


Figure 4-1 (a) Schematic diagram of the voltage assignment of a CNT-MEMS device with symmetrical biasing of the actuator. The two electrical currents, one passing through CNTs (I_{cnt}) and the other passing through the actuator (I_a), are separated by the native oxide on the side walls of the adapter; (b) close-up of the hook and T-shaped structure in the adapter.

- **Reduction of heat flux**

The native oxide not only serves as an insulation layer but also contributes to the high thermal resistance at the interface. According to [100], the presence of a thin native oxide layer at the interface can increase the thermal resistance by at least 50%. Moreover, the rough contact surfaces on the side walls, which result from the Bosch process, can significantly reduce the physical contact areas, and subsequently, the heat conduction through the interface is suppressed. As a result, the adapter is expected to be helpful in reducing the heat flux from the actuator to the CNT. Because of the difficulty with precision measurement of the thermal conductivity of the contact interface, the effectiveness in reducing the heat flux will be evaluated in section 4.4.2 on the basis of measurement and simulation results.

- **Mechanical buffer**

As discussed previously, the relaxation of the residual stress in the Si device layer after liquid HF release can cause certain deformation of a bent beam. The small deformation is

amplified by the mechanical configuration of the bent-beam thermal actuator and results in a large displacement. The displacement could exceed the linear stretchable range of a short suspended CNT, and inelastic elongation or rupture may occur. To avoid this, the gap within the adapter is a buffering space for the pre-deformation of the thermal actuator during liquid HF release. With the space in the adapter, the integrity of CNTs can remain. This is especially important for the as-grown CNTs on a thermal actuator because the CNTs are integrated on the actuator prior to liquid HF release and they are inevitably involved in the stress relaxation procedure.

4.1.3. Actuation system

The entire actuation system includes a suspension beam, bent beams, and the adapter. The three main components are illustrated in Figure 4-2. The design for each component is described in this section.

- **Suspension beam**

The force of the actuator is transferred to the suspended CNT via the adapter. During operation, the long suspension beam is deformed, and subsequently the CNT is strained. To reduce the required actuation force, the lateral bending stiffness of the suspension beam is preferably low. However, the compressive residual stress of the Si device layer may make the soft beam buckle after liquid HF release. Hence, the lowest bending stiffness of the suspension beam is limited by the residual stress.

The stiffness of the suspension beam depends on its geometry. The thickness is determined by the device layer and processing. The minimum beam width is limited by the minimum line width of the metal leads, which are patterned on the suspension beam for the electrical connection of the CNT. The only design parameter is the length of the suspension beam.

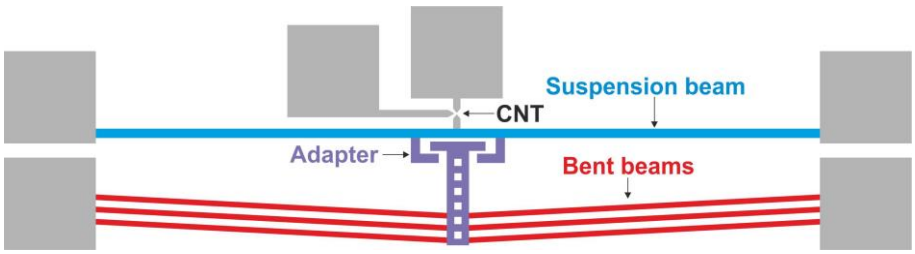


Figure 4-2 Three main components in the actuation system.

The buckling force of a fixed-fixed beam is correlated to the beam dimension as [101]

$$F_{Buckle,\mathrm{sb}} = \frac{4 \cdot \pi^2 E_{Si} I_{sb}}{\left(l_{sb}\right)^2} \tag{4.1}$$

where E_{Si} is the Young's modulus of Si, I_{sb} is the area moment of inertia of the beam, and l_{sb} is the beam length. To avoid buckling, the designed suspension beam is 400 μm in length, 3 μm in width, and 4.5 μm in thickness. The corresponding buckling stress is 31 MPa, which is larger than the maximum measured residual stress in the Si device layer (−24 MPa). Comparing the lateral bending stiffness of the suspension beam (5.13 N/m) to the axial elongation stiffness of a 4 μm long CNT (0.18 N/m), most of the output force of the actuator contributes to the deformation of the suspension beam.

- **Bent beams**

A bent beam is made of two inclined beams, as shown in Figure 4-3. It is simple in structure, but the working mechanism involves multi-physics, such as electrical joule heating, heat transfer, and thermal expansion induced mechanical deformation. The design parameters include the dimensions of the inclined beams, the inclined angle, and the number of bent beams.

The thickness of an inclined beam is defined by the Si device layer and the process steps of thermal oxidation and polishing. As mentioned previously, the final thickness of the Si layer after the entire process is expected to be 4.5 μm. In order to reduce out-of-plane deformation during operation, the ratio of beam thickness to beam width should be as high as possible. With the fixed Si thickness, the ratio is determined by the beam width. The

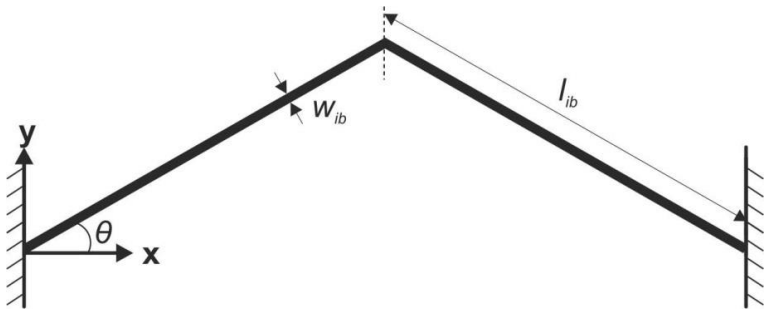


Figure 4-3 Sketch of a bent beam, consisting of two inclined beams.

lower limit of the beam width depends on the internal forces. The internal stress mainly results from thermal expansion, the residual stress of the Si device layer, and external force loading. If the total internal force is larger than the buckling force of the inclined beam, the input energy of the actuator will be inefficiently converted to output displacement and force [91]. Considering the out-of-plane stiffness and the efficiency of the actuator, a beam width of 2 μm is designed, providing four times higher out-of-plane stiffness than the in-plane stiffness.

In addition, the length (l_{ib}) and inclined angle (θ) of the inclined beam are two dominant parameters for the mechanical amplification factor (AF) of the actuator. The free displacement (without force output) and beam geometry is described by the following equation [102]

$$u_{y,f} = A_{ib}\alpha_{Si}\Delta T {l_{ib}}^3 \cdot \frac{\sin\theta}{12 I_{ib}\cos^2\theta + A_{ib}{l_{ib}}^2\sin^2\theta} \tag{4.2}$$

where A_{ib} is the cross section area of the inclined beam, α_{Si} is thermal expansion coefficient of Si, ΔT is the average temperature increase, and l_{ib} is the length of the inclined beam. Eq. (4.2) can be re-arranged as

$$u_{y,f} = \left(\alpha_{Si}\Delta T l_{ib}\right)\cdot\left(\frac{A_{ib}{l_{ib}}^2\sin\theta}{12 I_{ib}\cos^2\theta + A_{ib}{l_{ib}}^2\sin^2\theta}\right) = (\Delta l_{ib})\cdot(AF) \tag{4.3}$$

Eg. (4.3) describes that the free displacement is the multiplication of the thermal expansion in the inclined beam, Δl_{ib}, and the structural amplification factor, AF. A larger AF value means a larger displacement at a given temperature increase. The amplification factor decreases with the inclined angle in a non-linear way. For an inclined beam of 2 μm in width, 4.5 μm in thickness, and 175 μm in length, the amplification factor decreases from AF= 40 at θ= 1°, AF= 26 at θ=2°, and to AF= 14 at θ= 4°. However, decreasing the inclined angle increases the internal stress while the thermal expansion (Δl_{ib}) is fixed. A higher internal stress tends to trigger the formation of micro-cracks in Si and consequently reduces the durability of a bent-beam actuator [103]. Considering these factors, the inclined angle was set to be θ= 2 °. The other dominant parameter of the amplification factor is the beam length. The beam length is a trade-off between the amplification factor and the beam buckling force. The length of the bent-beam was determined to be l_{ib} = 175 μm, which

Table 4-3 Dimensions of the suspension beam and the inclined beams.

	Thickness (μm)	Width (μm)	Length (μm)	Angle (°)
Suspension beam	4.5	3	400	0
Inclined beam	4.5	2	175	2

correspond to an amplification factor AF= 26 and a buckling force of $F_{Buckle,ib}$= 40.80 μN. The dimensions of the suspension beam and the inclined bent beam are listed in Table 4-3.

A series of bent beams can improve the linear actuation of a bent-beam actuator. Additionally, an external force loading can be distributed by these bent beams and thus the internal stress of each inclined beam is reduced. The thermal actuator is designed to be equipped with a series of three bent beams. Considering the maximum required force output (~1 μN), each bent beam contributes 0.33 μN. The corresponding reaction force in each inclined beam is 4.33 μN, which is around one tenth of the buckling force of the inclined beam ($F_{Buckle,ib}$ =40.80 μN).

- **Estimation of buckling in bent beams**

To predict the occurrence of buckling in bent beams, all the structural dimensions of the suspension beam and bent beams need to be taken into account. Due to the symmetry of the actuator, only half of the set of the bent beams are considered. Assuming that the boundary conditions of each bent beam are identical, the following analysis is based on one inclined beam only, as shown in Figure 4-4. The governing equation of the inclined beam subjected

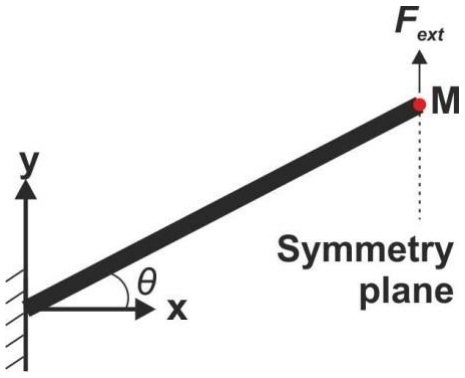


Figure 4-4 An inclined beam subjected to an external force and internal stresses.

to an external force, internal thermal expansion, and residual stress, is as follows [104]

$$\begin{bmatrix} \left(\cos^2\theta\cdot\frac{A_{ib}E_{Si}}{l_{ib}}+\sin^2\theta\cdot\frac{12E_{Si}I_{ib}}{l_{ib}^{\,3}}\right) & \cos\theta\cdot\sin\theta\cdot\left(\frac{A_{ib}E_{Si}}{l_{ib}}-\frac{12E_{Si}I_{ib}}{l_{ib}^{\,3}}\right) \\ \cos\theta\cdot\sin\theta\cdot\left(\frac{A_{ib}E_{Si}}{l_{ib}}-\frac{12E_{Si}I_{ib}}{l_{ib}^{\,3}}\right) & \left(\sin^2\theta\cdot\frac{A_{ib}E_{Si}}{l_{ib}}+\cos^2\theta\cdot\frac{12E_{Si}I_{ib}}{l_{ib}^{\,3}}\right) \end{bmatrix}\begin{bmatrix} 0 \\ u_y^M \end{bmatrix} \\ =\begin{bmatrix} \alpha_{Si}\Delta T E_{Si}A_{ib}\cos\theta \\ \alpha_{Si}\Delta T E_{Si}A_{ib}\sin\theta \end{bmatrix}+\begin{bmatrix} \sigma_{res}A_{ib}\cos\theta \\ \sigma_{res}A_{ib}\sin\theta \end{bmatrix}+\begin{bmatrix} R_x^M \\ \frac{F_{ext}}{2\cdot n} \end{bmatrix} \tag{4.4}$$

where σ_{res} is the residual stress in Si, R_x^M is the reaction force in x-direction at point M (as indicated in Figure 4-4), F_{ext} is the external force, and n is the number of bent beams. Assuming a small deformation of the inclined beam, the total reaction force can be described as the superposition of the reaction forces resulting from the thermal expansion ($R_x^{M,\Delta T}$), the residual stress ($R_x^{M,\sigma_{res}}$), and the external force loading ($R_x^{M,F_{ext}}$) at point M. The total reaction force (R_x^M) can be expressed as

$$\begin{aligned} R_x^M &= R_x^{\mathrm{M},\Delta T}+R_x^{M,\sigma_{res}}+R_x^{M,F_{ext}} \\ &= \alpha_{Si}\Delta T E_{Si}A_{ib}\left(\frac{B}{D}\cdot\sin\theta-\cos\theta\right)+\sigma_{res}A_{ib}\left(\frac{B}{D}\cdot\sin\theta-\cos\theta\right)+\frac{B}{D}\cdot\frac{F_{ext}}{2n} \end{aligned} \tag{4.5}$$

with

$$B=\cos\theta\cdot\sin\theta\cdot\left(\frac{A_{ib}E_{Si}}{l_{ib}}-\frac{12E_{Si}I_{ib}}{l_{ib}^{\,3}}\right)$$

$$D=\sin^2\theta\cdot\frac{A_{ib}E_{Si}}{l_{ib}}+\cos^2\theta\cdot\frac{12E_{Si}I_{ib}}{l_{ib}^{\,3}}$$

The thermal expansion induced stress and the residual stress are independent of the number of bent-beams because both of them originate from each inclined beam. Inserting the maximum measured residual stress (σ_{res}= −24 MPa) and the maximum required force ($F_{ext,max}$= 1/6 µN) into Eq. (4.5), the maximum normal reaction force along the inclined beam can be calculated as

$$R_{norm}^M=(R_x^{\mathrm{M},\Delta T}+R_x^{A,\sigma_{res}}+R_x^{A,F_{ext}})\cdot\cos\theta=-10^{-9}\cdot(381\cdot\Delta T+20812+4312)\cdot\cos 2 \tag{4.6}$$

In Eq. (4.6), the only undetermined parameter is the average temperature increase (ΔT), which is relevant to the displacement of the actuator. If the maximum displacement is

identical to the maximum elongation (5%) of the 4 µm long CNT, the normal force is R_{norm}^{M}= 32.04 µN. The bent beams will not buckle because R_{norm}^{M}< $F_{Buckle,ib}$= 40.80 µN. If the gap in the adapter after release is larger than 270 nm, buckling will occur while straining the CNTs.

From Eq. (4.6), a quantitative comparison of every component of the internal stress can be seen. The residual stress after liquid HF release results in a reaction force along the bent beam, which is approximately equal to a half of the buckling force. While the actuator is driven, the internal force rapidly approaches the buckling force because of the thermal expansion. Compared with these two stresses, the stress resulting from the external force load is lower (10% of the beam buckling force). This is because the stiffness of the suspension beam is low and the external loading is distributed by the three bent beams.

- **Adapter**

In addition to serving as an electrical and thermal insulator, the adapter also transmits actuation force to the suspended CNT. A thin native oxide has been shown to be intact under a static mechanical load of 1 MPa [105]. The maximum required force for CNT straining here is 1 µN. To make the mechanical contact pressure lower than 1 MPa, the overlap between the hook and the T-shaped structure needs to be larger than 0.4 µm (Si layer thickness =4.5 µm).

Considering the maximum measured residual stress ($\sigma_{res,max}$ = −24 MPa) as well as the mechanical amplification factor (*AF*= 26), the deformation of the actuator after release is approximately 0.65 µm. Hence, the gap should be larger than 0.65 µm before liquid HF release. However, the minimum gap size fabricated by the integration process is 1.2 µm (0.5 µm on photomask→0.7 µm after DUV and ICP→1.2 µm after thermal oxidation). As a result, the practical gap size is always larger than the minimum required 0.65 µm for buffering the structural deformation after liquid HF release.

4.2. Fabrication results

Figure 4-5a shows an overview of the entire system after liquid HF release. The system includes the adapter, the thermal actuator, and two sets of 3-terminal Si electrodes for the integrated as-grown CNTs. In addition, two Si mesas are seen in this figure. They filled up the empty space to make the Si etching rate of the Bosch process and the polishing force

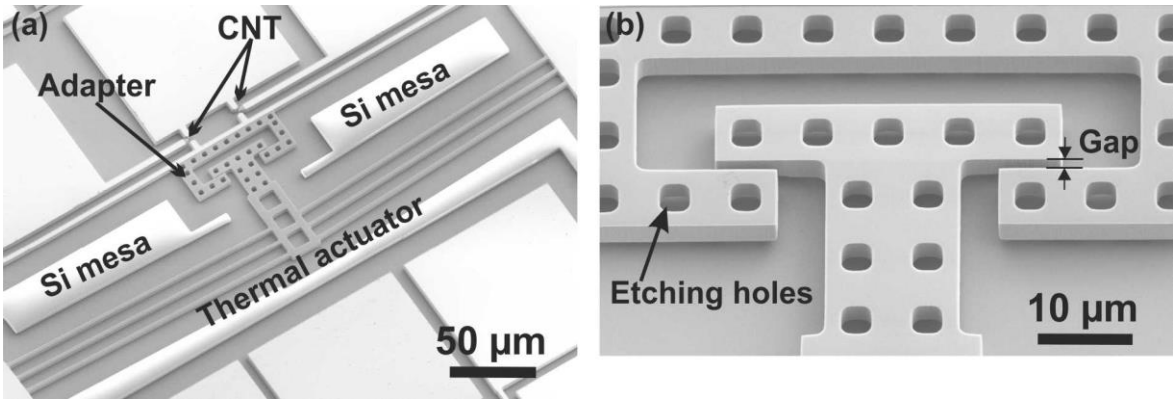


Figure 4-5 (a) Overview of the entire actuation system, consisting of the adapter, the actuator, and the Si electrodes for the integrated suspended CNTs. Two anchored Si mesas were included for more uniform Si etching and uniform mechanical polishing pressure; (b) close-up of the released adapter and the etching holes. The gap within the adapter is around 1.4 µm (D#BW1_C#SOIC4-RE1C1).

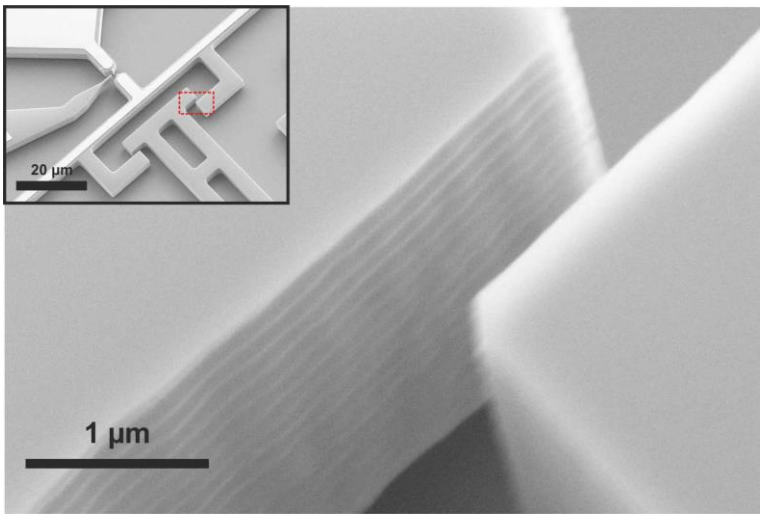


Figure 4-6 SEM image of the scallops on the side wall within the adapter after liquid HF release (C#SOIC4s-150Au-1).

more uniform on the chip. To reduce the liquid HF etching time, etching holes were patterned on the adapter as shown in Figure 4-5b. The required undercut was around 3 µm for the entire actuation system. The gap in the adapter seen in Figure 4-5b is 1.4 µm wide. The gap is larger than the critical gap size of 0.27 µm, which was calculated based on the buckling force of the inclined beam in the previous section. During the development of the integration process, the gap size on the photomask was designed between 0.5 µm and 1 µm

to make sure that a gap in the adapter was properly patterned and etched through. The gap after liquid HF release was between 0.9 µm and 1.4 µm. Hence, the output efficiency of the actuator may be attenuated due to the occurrence of the beams buckling at high actuation voltages.

As shown in Figure 4-6, scallops on the side walls of the adapter, which were initially etched by the Bosch process, still remained after thermal oxidation and liquid HF release steps. Reduced physical contact areas in the interface of T-shaped structure and the hook can suppress the heat flux from the thermal actuator to the CNT. Further analysis of the thermal resistance at the interface will be discussed in section 4.4.2.

The Si mesas seen in Figure 4-5a are helpful in improving the uniformity of the polishing pressure. At the center segments of the three inclined beams of an actuator, the beam thickness difference is as small as 0.02 µm. The difference could be as large as 1.7 µm without these mesas. The same profile of these inclined beams in the actuator is beneficial for linear actuation. However, polishing still changes the topography of inclined beams. A typical profile of the polished inclined beam is shown in Figure 4-7. The mid-segment of the beam remains relatively flat, and the thickness is 4 µm. The pad and the central shuttle are thicker than the mid-segment by 0.46 µm and 0.25 µm respectively. This is because the

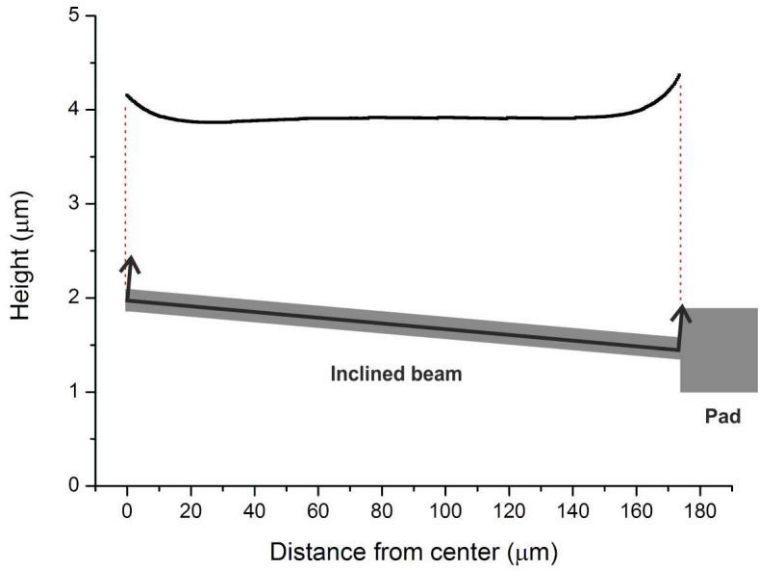


Figure 4-7 Profile of a polished inclined beam, measured by white light interferometer. The mid-flat segment is 4 µm thick, which is lower than the pad and the central shuttle by 0.46 µm and 0.25 µm respectively.

polishing pressure is locally higher in the structures of smaller areas. Hence, slightly over-polishing occurred in the narrow inclined beams.

4.3. Characterization of the fabricated actuation system

The operational voltage range for CNT straining can be defined, based on the relationship of the actuation voltage and the corresponding displacement. Hence, the displacements of the actuator and the adapter were measured at different actuation voltages. Moreover, to verify the effectiveness of the adapter in electrically insulating the CNT from the actuator, the leakage currents through the adapter were monitored at various actuation voltages.

4.3.1. Displacement of the actuation system

The actuation systems were characterized in ambient conditions (relative humidity = 28% and temperature = 23 °C) and in SEM vacuum chamber to reveal the performance in different environments.

- **Measurement in air**

The measurement setup is shown in Figure 4-8. The actuator is driven by two Keithley 2400 sourcemeters, which are controlled by LabVIEW program. Polytec MAS-400 Micro System Analyzer (PMA) takes images during the measurement. By comparing the position change relative to the initial image, the displacement of a moving object is calculated. Two monitoring areas are typically selected, one on a moving part and the other on a stationary part as shown in Figure 4-9. The displacement measurements in these two selected areas are independent. The measured displacement of the stationary part is representative of external disturbance. By subtracting the displacement of the moving part by that of the stationary part, the influence of external disturbance can be eliminated and accurate displacement of the moving part can be extracted. With a proper selection of monitoring areas, spatial resolution of 5 nm is achievable. Using this setup, the displacements of the actuator and the hook structure were measured and plotted in Figure 4-10. The actuation voltage at which the actuator starts contact with hook is defined as the contact voltage (V_c) of the adapter. If the actuation voltage exceeds the contact voltage, the CNT under test will be strained. The contact voltage is the lower bound of the operational range for CNT tensile test. The contact voltage of the adapter operated in ambient air was around V_c= 2.8 V. The displacement rate was 0.8 μm/V. The hook moved backward slightly before moving forward with the actuator, which might be attributed to surface forces.

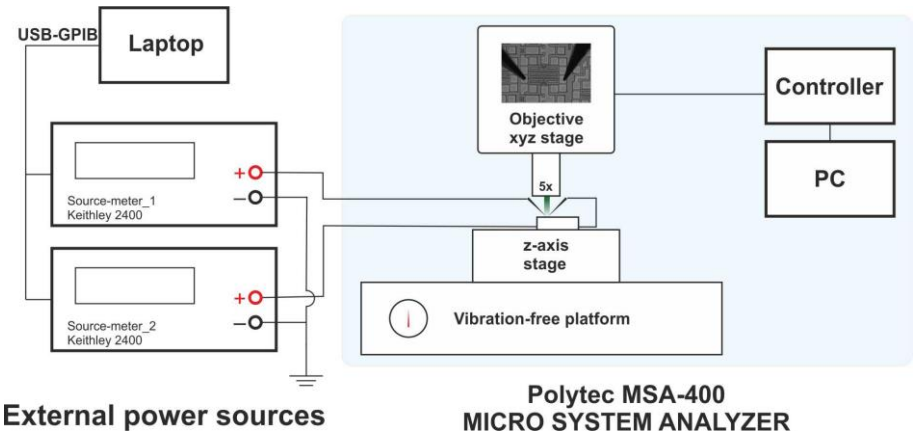


Figure 4-8 The measurement setup in ambient air. The displacement is measured using a Polytec MSA-400 MICRO SYSTEM ANALYZER. The actuator is driven by two external sourcemeters, Keithley 2400.

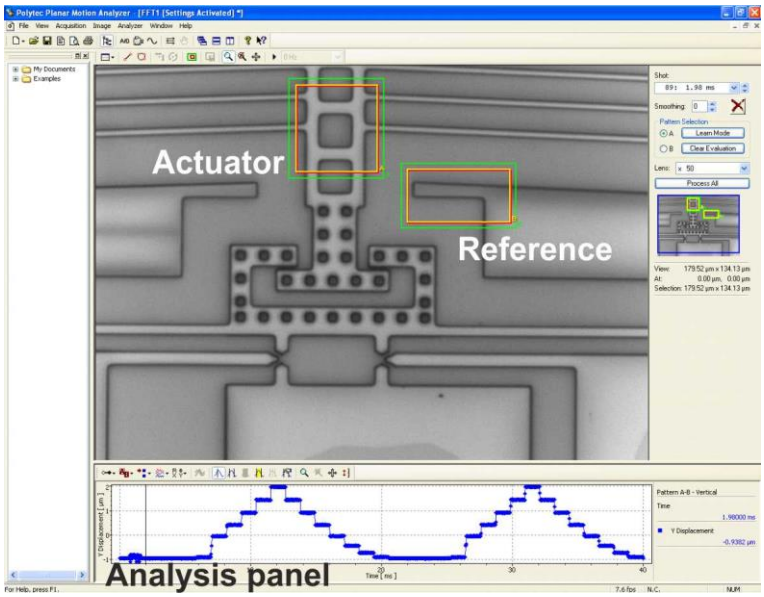


Figure 4-9 Snap shoot of the user interface of the Polytec MAS-400. Images are recorded while operating the actuator. Two monitoring areas are typically selected, and the displacements are simultaneously shown in the analysis panel.

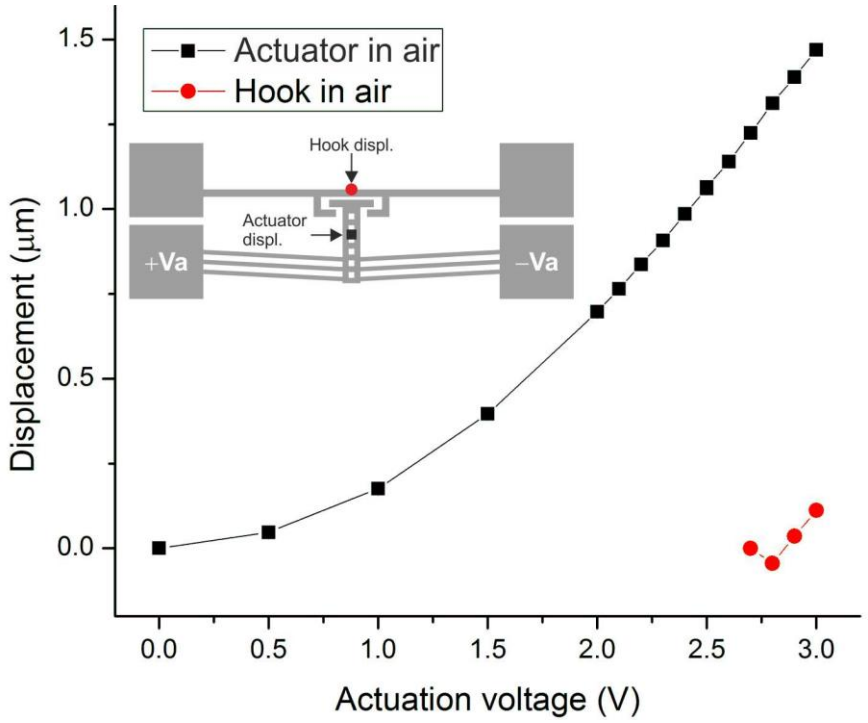


Figure 4-10 Displacements of the actuator and the hook versus different actuation voltage. The measurements were performed in ambient air (relative humidity = 28% and temperature = 23 °C). Error bars (<10 nm) are not visible in the plot scale (D#BW1-B4D_C#SOIC4-RE2C1).

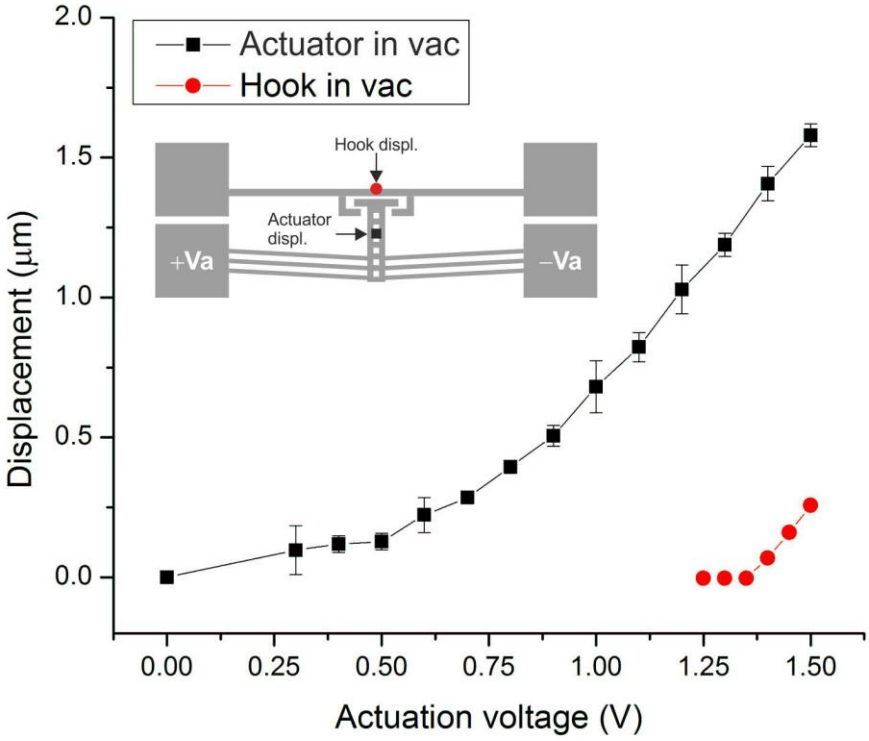


Figure 4-11 Characterization of the actuator and the hook in an SEM vacuum chamber. Error bars of the hook displacement (<10 nm) are not visible in the plot scale (D#BW1-C4D_C#SOIC4-R5C1).

- **Measurement in vacuum**

The control of the actuator in an SEM chamber was similar to the previous measurement in ambient air. The only difference in measurement is that the displacements were manually measured. The displacement range of the actuator was larger than that of the hook. Due to lower SEM magnification, the measurement errors of the actuator were larger. The measured displacement versus the actuation voltage is plotted in Figure 4-11. The contact voltage in vacuum was V_c = 1.4 V. The displacement rate was approximately 1.9 μm/V.

4.3.2. Monitoring the leakage current through the adapter

To verify if the CNT was electrically insulated from the actuator, the leakage current through the adapter was monitored. The adapters were characterized in ambient air using a semiconductor characterization system, Keithley 4200. During the tests, the actuation voltage swept from V_a= 0 V to V_a= 7 V and back, and the voltage of the hook was set at 0 V, as shown in the inset of Figure 4-12. The contact voltage of the adapter is V_c= 2.8 V in ambient air. The leakage currents of three consecutive sweeps of one device (measured two

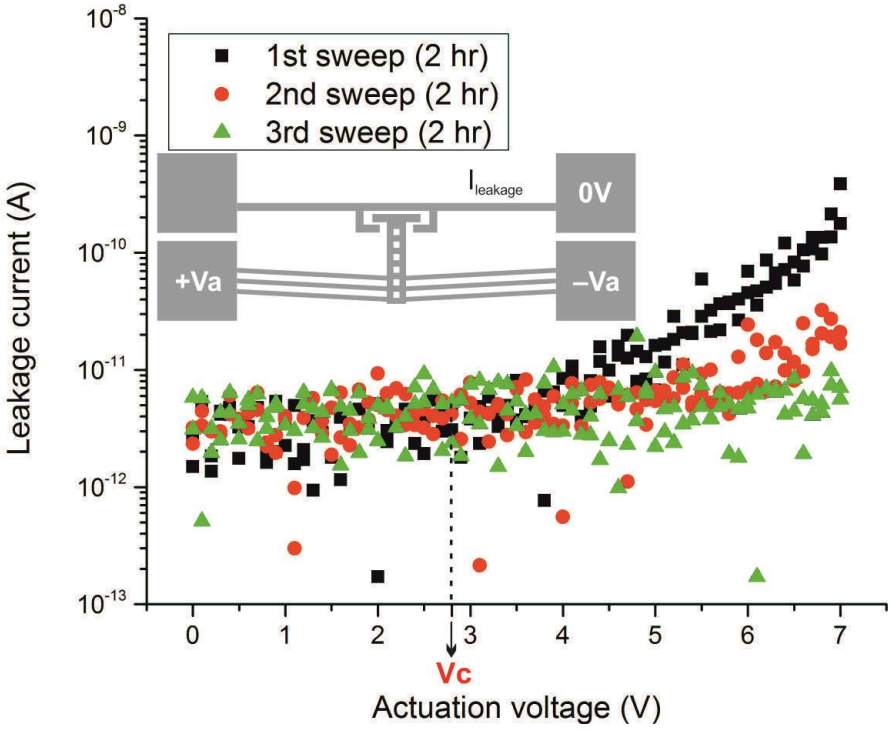


Figure 4-12 Three consecutive measurements of the leakage currents through the adapter. The device was measured 2 hours after liquid HF release (D#AN-C0U_C#SOIC4-RE2C1).

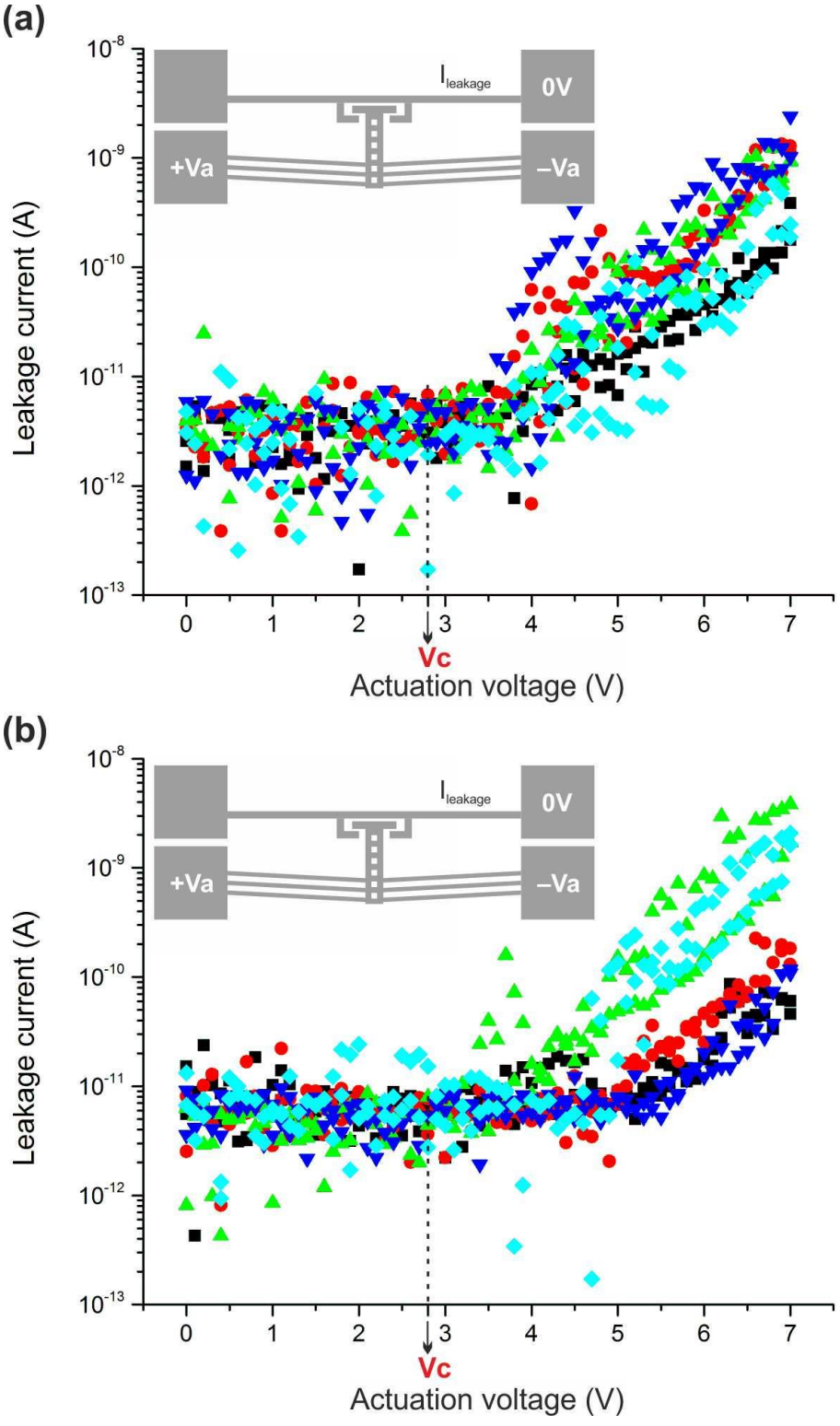


Figure 4-13 Leakage currents versus actuation voltages; (a) five devices measured 2 hours after liquid HF release (D#AN-C0U~D#AN-C4U on chip C#SOIC4-R13C1); (b) five devices measured 1 day after liquid HF release (D#AN-A0U~D#AN-A4U on chip C#SOIC4-RE2C1). One type of symbol represents the measured leakage currents from one device.

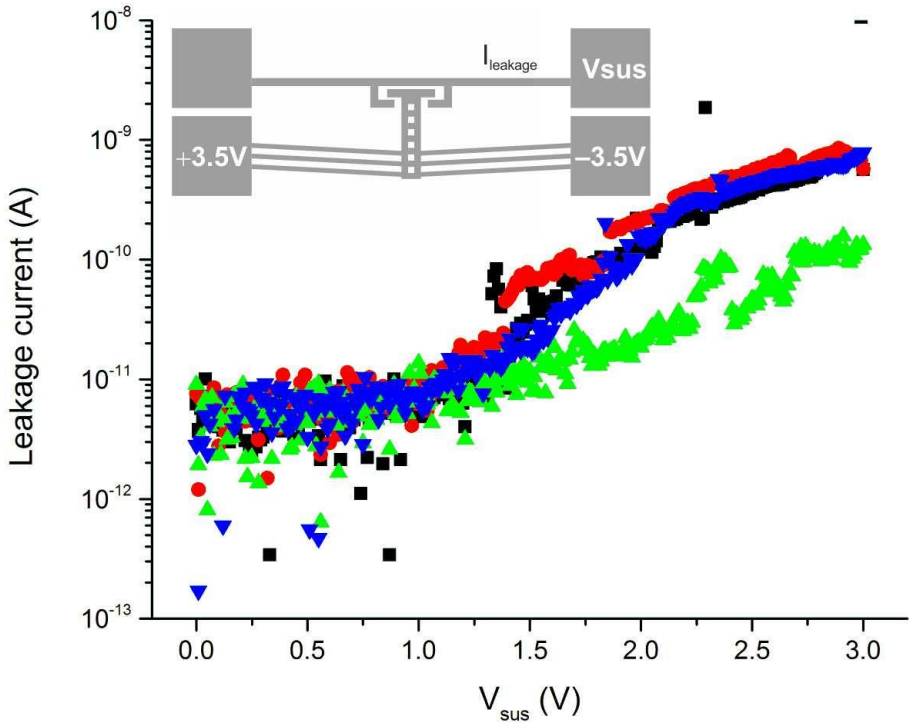


Figure 4-14 Leakage currents versus different applied voltages at the suspension beams (V_{sus}). The sustainable voltage of the native oxides within the adapter was around 1 V. One type of symbol represents the measured leakage currents from one device (D#BW1-D1U~D#BW1-D4U on chip C#SOIC4-RE2C1).

hours after liquid HF release) are shown in Figure 4-12. In the three V_a sweeps, the leakage current remained in the same range (~10 pA) after the T-shaped structure and the hook were in contact ($V_a > V_c$). The leakage current started to increase while the actuation voltage exceeded V_a= 4 V in the first sweep. Comparing these three sweeps, the leakage current was found to decrease after each sweep. In the third measurement, the leakage current remained in the range of 10 pA up to V_a= 7 V. This phenomenon was reproducible for other five devices. Considering this effect, the following leakage currents were measured from the first V_a sweep of each device. Five devices were characterized 2 hours after liquid HF release. The measurement results are shown in Figure 4-13a. The leakage current started to increase at V_a= 4 V. Five other devices were measured one day after liquid HF release, and the measurement results are shown in Figure 4-13b. The leakage currents of three devices started to increase at around V_a= 5 V, while for the other two devices, the leakage currents started to increase at V_a= 4 V. To quantify the sustainable voltage difference across the native oxides in the adapter, the actuation voltage was fixed at V_a= 3.5 V (>V_c= 2.8 V), and the voltage of the suspension beam (V_{sus}) swept from V_{sus}= 0 V to V_{sus}= 3 V and back. The

measured leakage currents of four devices (1 day after liquid HF release) are shown in Figure 4-14. The sustainable voltage of the native oxides was around 1 V.

4.4. Discussion

4.4.1. Electrical insulation of native oxides

The measurements of leakage currents reveal the operational ranges of the adapters. For a freshly released device, the operational voltage is up to V_a= 4 V. This operational voltage is higher than the adapter contact voltages of V_c= 1.4 V in vacuum and V_c= 2.8 V in air. Hence, the native oxides within adapter can provide sufficient electrical insulation for CNTs under straining tests. Further air exposure can increase the operational range. In Figure 4-13, the operational voltage was increased from V_a= 4V (2 hours) to around V_a= 5V (1 day). This also indicates that thicker native oxide formed within the first 2 hours after release, compared to the oxide grown in one day. According to the investigations in [106, 107], native oxide can form faster if Au and heavily-doped Si are both involved in liquid HF etching. Due to the galvanic effect, the Si surface is etched and becomes porous. The larger surface to volume ratio of the porous Si surfaces results in fast growth of native oxides. This could explain why the operation voltage is up to V_a= 4V after exposed to the air for 2 hours, but it did not increase much after one day. However, it is difficult to measure the thickness of native oxide by an ellipsometer because the measured signals were much noisier than that of the original SOI surface. This might be attributed to the rough Si surfaces after liquid HF etching (402 pm to 531 pm in root-mean-square roughness).

As shown in Figure 4-12, consecutive measurements lowered the leakage currents. This might result from the further oxidation induced by the high temperature while driving the actuator up to V_a= 7 V in air (the actuator broke down at V_a= 9V in air).

4.4.2. Low thermal conductance of point contacts

To estimate the increased temperature of the suspended CNT during a tensile test in vacuum, a commercial simulation software, COMSOL (ver.4.3a), was used to create a 3-dimensional finite element model. In the simulation, three physics modules were employed, *Electric currents (ec)*, *Heat transfer in solids (ht)*, and *Solid mechanics (solid)*. In the heat transfer module, convection and radiation were negligible [108], and hence, only heat conduction was taken into account. The model was created on the basis of the parameters measured or extracted from the characterization of the actuation system in section 4.3. Details of the

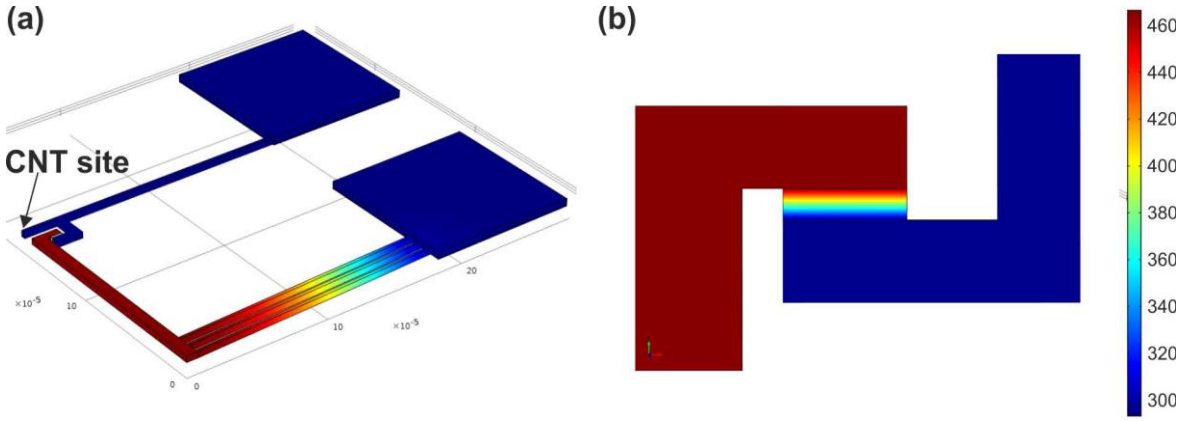


Figure 4-15 (a) Simulated temperature distribution of the actuator and adapter, operated at V_a = 1.5 V in vacuum. The label "CNT site" refers to the clamping site of the suspended CNT. The suspended CNT was not included in the simulation model; (b) close-up of the temperature difference in the physical contact interface (temperature unit: Kelvin).

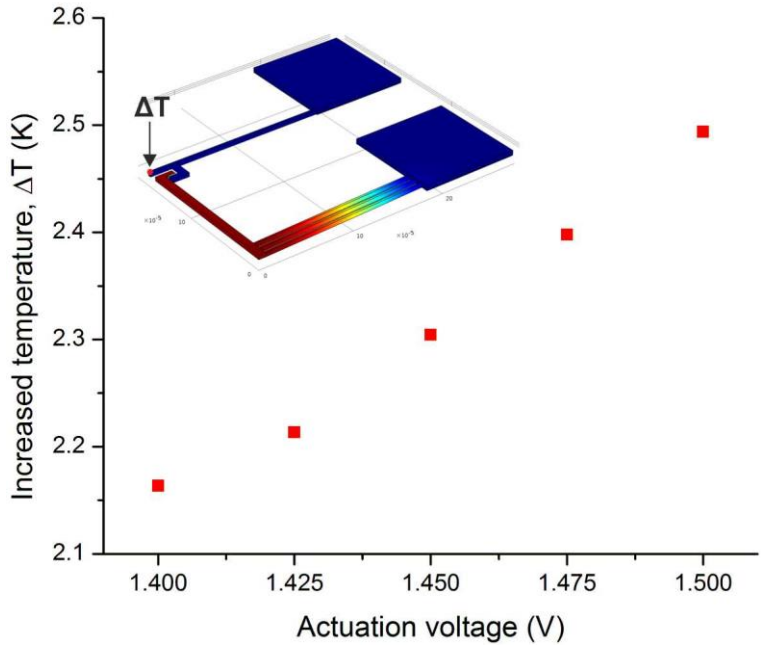


Figure 4-16 Simulated actuation voltage dependency of the increased temperature at the CNT site after the T-shaped structure and hook are in contact.

simulation parameters and the simulation method are listed and described in Appendix IV. The simulated temperature distribution of the adapter and actuator at V_a= 1.5 V is shown in Figure 4-15a, where the virtual location of a suspended CNT was indicated as "CNT site," but a CNT was not included in the simulation model. As the close-up in Figure 4-15b shows, the hook side remains at a low temperature, while the T-shaped structure, which is connected to the thermal actuator, is heated up. The temperature difference across the interface is 191 K, and the corresponding thermal conductance of the contact interface is 105 nW/K. The actuation voltage dependency of the temperature at the CNT site is plotted in Figure 4-16. When a suspended CNT is strained by 5% at V_a= 1.475V, the temperature increase will be less than 2.5 K.

The simulation results indicate that the adapter can efficiently reduce the heat flux flowing from the actuator to the CNT site. Thus, during tensile tests, the influence of the increased temperature induced by the actuator is minimized, and the piezoresistive response of the tested CNT can be revealed. The low thermal conductivity in the adapter can be attributed to the native oxide layer on the side walls as well as the small contact areas (Figure 4-6). The presence of a native oxide can reduce the heat transfer across solid interfaces [100]. Moreover, the reduced physical contact areas, resulting from the rough side wall surfaces, can lower the thermal conduction. An investigation of the heat transfer [109] of a metal-metal point contact shows that the thermal conductance is around 30 nW/K, which is comparable to the thermal conductance of 105 nW/K, extracted from the simulation. As a result, the low thermal conductance can be explained by point contacts at the interface.

4.4.3. Operation in ambient conditions

Comparing the performance of the two actuators operated in air (Figure 4-10) and in vacuum (Figure 4-11), a noticeable difference can be observed in the output displacement at an identical actuation voltage. The difference is mainly attributed to the presence of the air. While operating a thermal actuator in ambient air, heat can be dissipated to the substrate via air. Using the simulation model developed in Appendix IV, a simulation based on the measurement in ambient air was performed to estimate the heat dissipation. Among different heat dissipation routes, heat conduction via the air underneath the actuator to the substrate is much higher than the heat dissipation via Si to the pads, as shown in Figure 4-17. The heat dissipation through the air accounts for approximately 70% of the total power. The high heat dissipation could be attributed to the large overlapping areas of the bent beams with the substrate and the small gap between the actuator to the substrate. This explains why

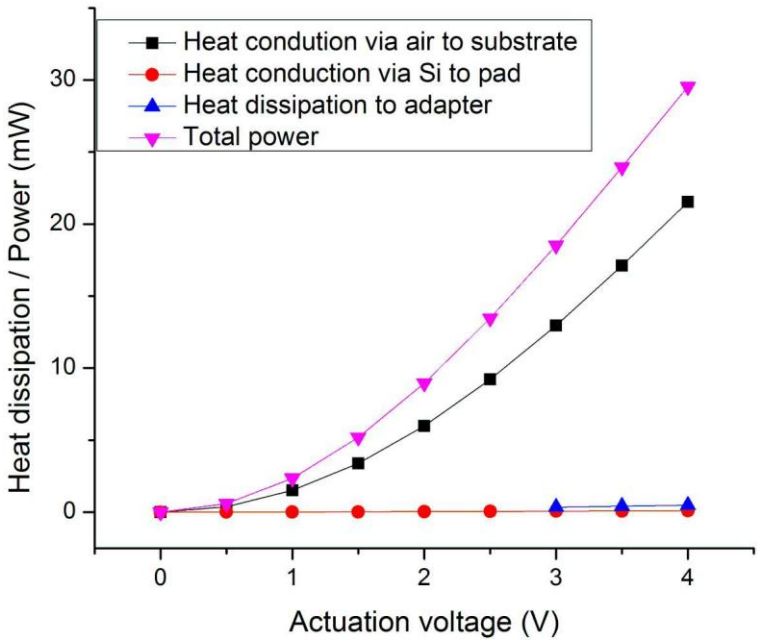


Figure 4-17 Heat dissipations and total power supply versus the actuation voltage. The heat conduction via air to the substrate accounts for the heat dissipated through the bottom side of the actuator.

the operation of the thermal actuator in ambient air required higher actuation voltages to reach the same displacement output as in vacuum.

In addition to the difference in actuation performance, another difference of the operation in air and in vacuum is the behavior of the suspension beam. As shown in Figure 4-10, the hook snapped to the T-shaped structure when the gap was as close as 44 nm. This could be explained by the surface forces existing within the adapter, such as capillary, van der Waals, electrostatic, and chemical forces [110]. The snap-in effect was consistently observed in most of the devices operated in ambient air, but not in vacuum. Moreover, the simulated temperature of the T-shaped structure operated in vacuum (430 K) was much higher than that in air (298 K) when the T-shaped structure was close to the hook (gap~150 nm). As a result, this effect could be mainly attributed to the capillary forces resulted from the condensed moisture on the surfaces of the adapter in ambient air.

4.5. Summary

An electro-thermal bent-beam actuator was selected for the actuation system due to its large force output, large displacement, and low driving voltage. A mechanical configuration, the

adapter, was designed to electrically and thermally decouple the thermal actuator and the integrated CNT. Taking advantage of the native oxide on the side walls of the adapter, the CNT can be electrically insulated from the actuator. Moreover, the reduced contact areas in the adapter suppress the heat flux from the actuator to the CNT. The actuation system, including a suspension beam, three bent beams, and the adapter, was designed according to the measured electrical conductivity and residual stresses of the SOI device layer. A slack-free 4 μm long suspended CNT can be strained by 5% at V_a= 1.5 V (in vacuum). Moreover, according to the simulation result of the actuation system at this output displacement, the increased temperature of the CNT will be only 2.5 K, which could be attributed to the effective heat suppression by the adapter. The electrical measurements of leakage currents indicate that, the adapter can electrically insulate the CNT from the actuator up to V_a= 4 V, providing sufficient operational range for straining the CNT in ambient air and in vacuum. In conclusion, the designed actuation system can strain the integrated CNT, and it also minimizes the electrical and thermal interferences from the thermal actuator.

Chapter 5 Demonstrations of CNT strain tuning by the embedded actuation system

A suspended CNT can be fabricated together with an embedded MEMS actuator by using the developed integration process. The CNT and the thermal actuator can function simultaneously and independently with the assistance of the adapter. This chapter outlines how fabricated CNT-MEMS devices were used for the demonstrations of strain tuning. The static electrical responses and dynamic mechanical responses were investigated respectively in section 5.1, and section 5.2.

5.1. *In situ* electro-mechanical loading tests

5.1.1. Sample preparation

Packaging is required to interface the device with the external instruments to perform electrical measurements inside an SEM chamber. In the packaging procedure, wire-bonding is considered as a risky step due to electrostatic discharge (ESD). The suspended CNTs could hardly survive the harsh conditions which occurred when the wire-bonding was performed. To resolve this problem, wire bonding was performed prior to the final release, and the release was performed in vapor HF. Thus, some devices still worked when the modified procedure was completed. Figure 5-1 shows a tilt view of a wire-bonded CNT-MEMS device after release. The connection wires are aluminum wires of 30 μm in diameter.

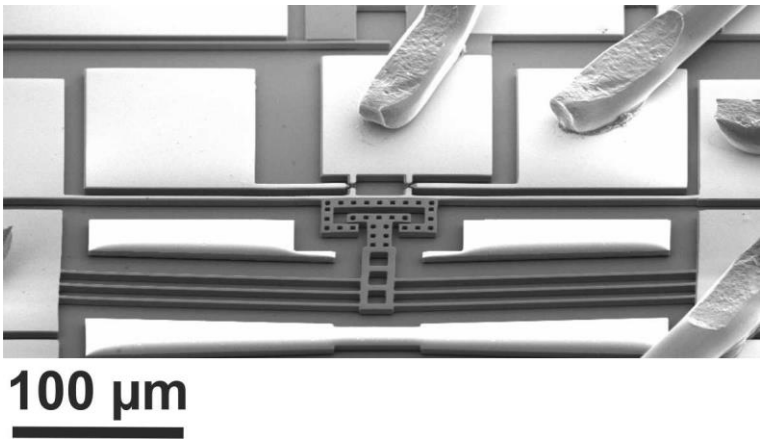


Figure 5-1 SEM tilt view of a wire-bonded CNT-MEMS device in an SEM chamber. The bonding wires used here are aluminum wires of 30 μm in diameter (D#BW1-C4D_C#SOIC4-R5C1).

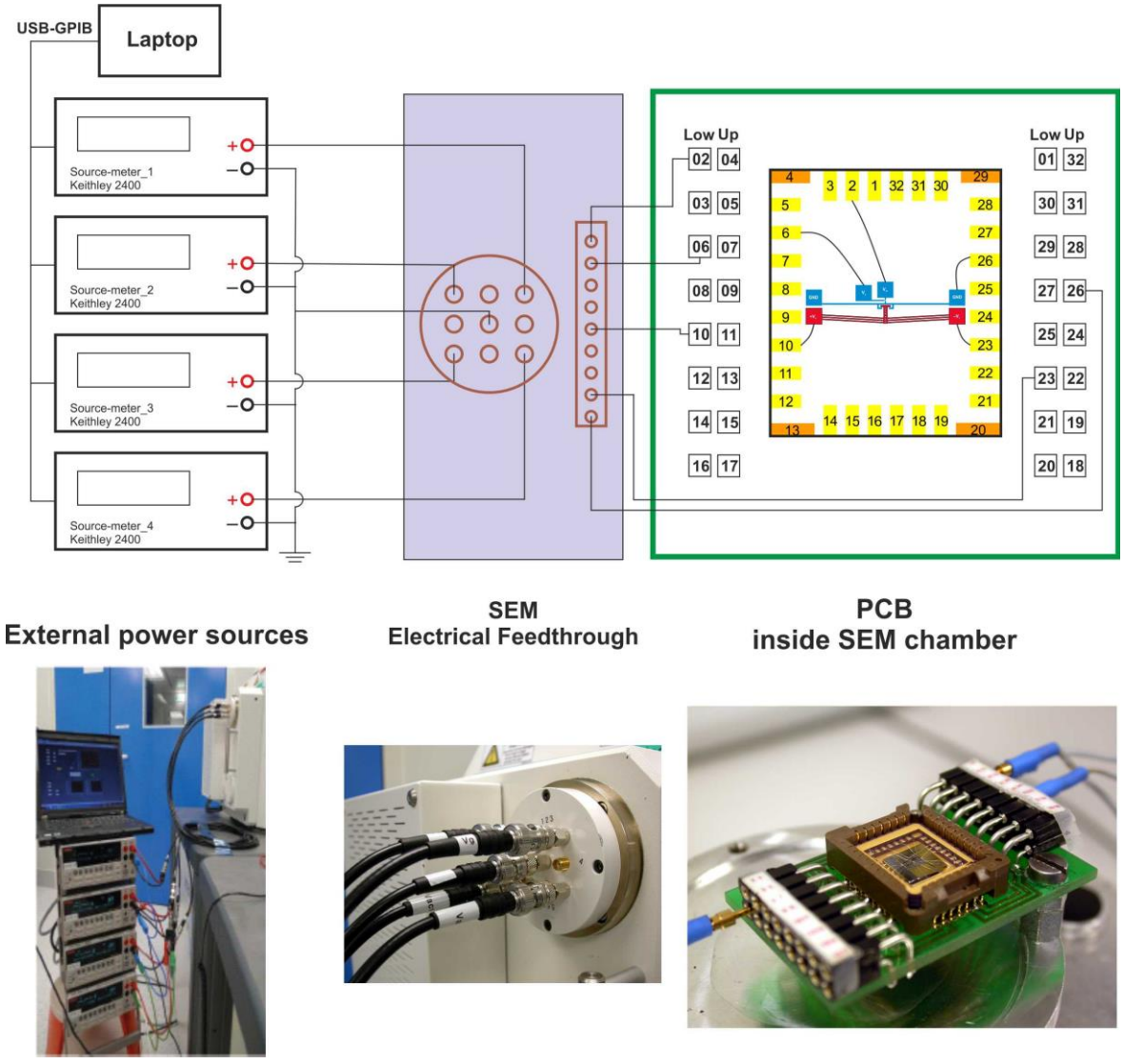


Figure 5-2 Experimental setup of the *in-situ* electro-mechanical loading test. The images shown in the lower row are the major parts corresponding to the schematic setup shown above.

One important measure to protect wire-bonded CNT devices from an ESD hazard is to connect the source and drain electrodes (or corresponding leads on package) by an additional wire. After the device is properly installed in the measurement setup, the wire can be manually removed. This electrical bypass can effectively eliminate the issue of the high current pulses induced by ESD.

5.1.2. Experimental setup

The experimental setup is shown in Figure 5-2. Four high precision Keithely 2400 sourcemeters were employed respectively to provide a gate voltage (V_{gd}), a source-drain voltage (V_{sd}), and two actuation voltages ($+V_a$ and $-V_a$). These sourcemeters were connected to the wire-bonded device inside the SEM chamber via an electrical feedthrough. The voltage assignment of a CNT-MEMS device is shown in Figure 5-3. LabVIEW virtual instruments (VIs) were programmed to control all the sourcemeters for various voltage sweeps and record electrical data produced during measurements. A Keithley GPIB-USB adapter was used for the communication between the sourcemeters and the laptop.

5.1.3. Tensile test

To monitor the electrical characteristics of the CNTFET in different environments, transport measurements were performed during the sample loading procedure. Before evacuating the SEM chamber, the device was measured in N_2-rich air (due to the N_2 purging from SEM chamber). After evacuating the chamber, the transport measurement was conducted again. As the measured I_d-V_{gd} curves in Figure 5-4 show, the transistor characteristics of the device did not change much until the suspended CNTs was scanned by the electron beam (E-beam) of the SEM. After the short E-beam scanning, the drain current in the N-branch suddenly increased.

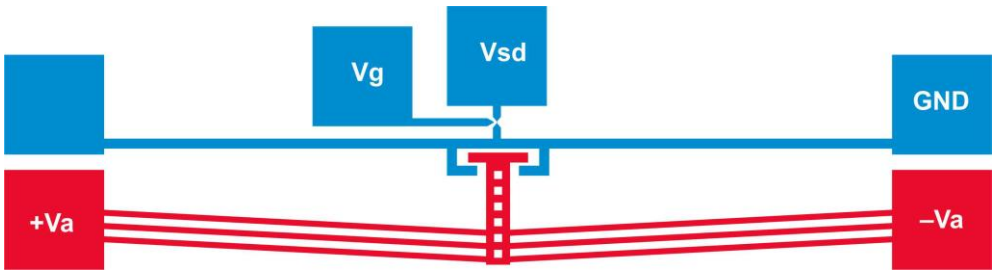


Figure 5-3 Schematic sketch of the voltage assignment of the CNT-MEMS device.

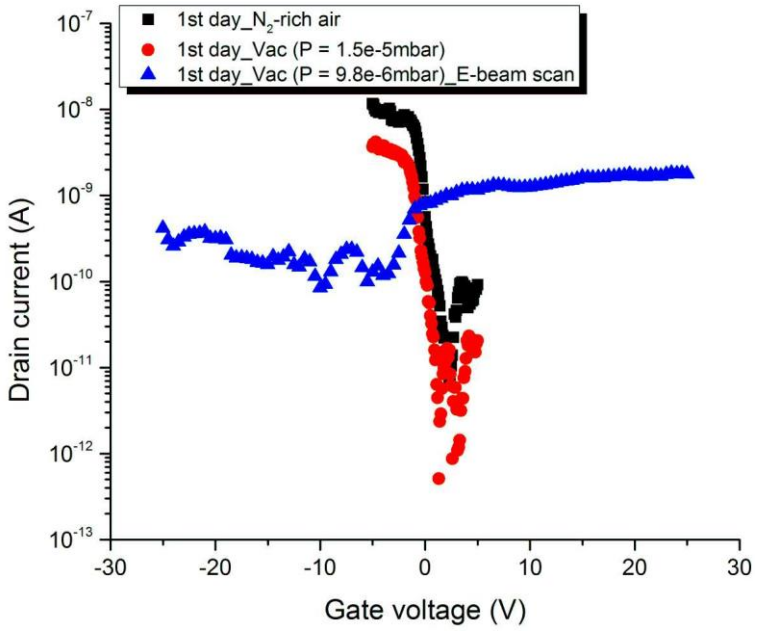


Figure 5-4 Transition of transistor characteristics of the CNTFET in N_2-rich air (before evacuation), in vacuum (after evacuation), and after E-beam scanning (D#BW1-C4D_C#SOIC4-R5C1).

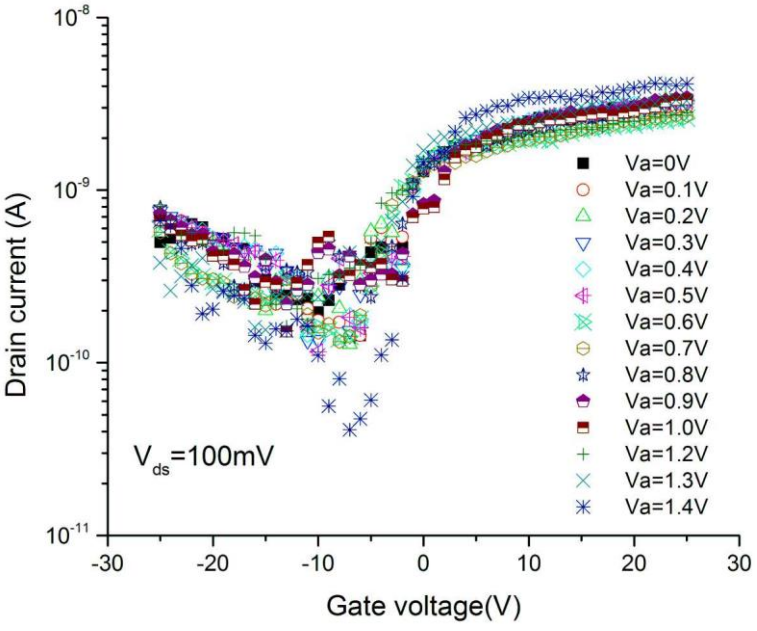


Figure 5-5 Transport measurements at different actuation voltages (D#BW1-C4D_C#SOIC4-R5C1).

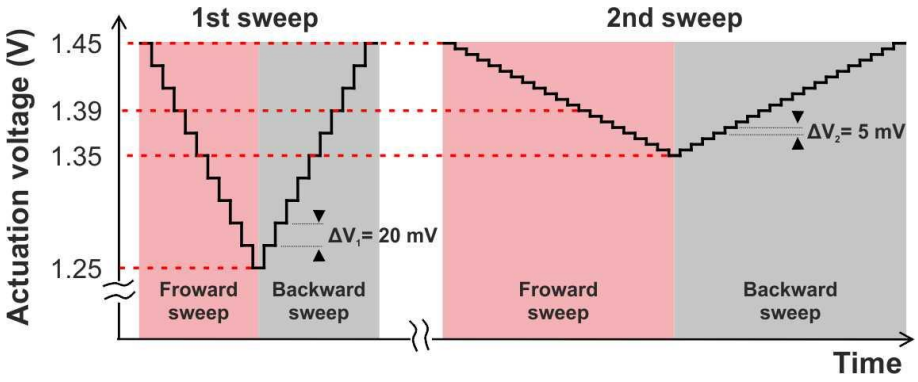


Figure 5-6 Measurement protocol of actuation voltage sweeps.

In the beginning of the tensile test, the actuation voltage was increased slowly and the transport measurement was performed at each actuation voltage. During the tensile tests, the E-beam was turned off to avoid disturbing the transport measurements. The corresponding displacements of the actuator and the elongation of the CNT were measured afterwards. Noticeable changes were observed when the actuation voltage exceeded V_a= 1.3 V. The selected transport measurements from V_a= 0 V to V_a= 1.4 V are shown in Figure 5-5. The upper limit of the actuation voltage was set at V_a= 1.45 V. Two round V_a sweep with smaller increments were performed according to the measurement protocol shown in Figure 5-6. In the first sweep, the actuation voltage swept from V_a= 1.45 V to V_a= 1.25 V and back with a step voltage of ΔV_a= 20 mV. At each actuation voltage, a transport measurement with a sweeping gate voltage from V_g= −25 V to V_g= +25 V was performed. To measure finer current variations with strain, the second sweep was conducted from V_a= 1.45 V to V_a= 1.35 V and back with a step voltage of ΔV_a= 5 mV.

A few selected transport measurements at different actuation voltages are shown in Figure 5-7. The inset shows an SEM image of the suspended CNTs under test. During the tensile test, there was no obvious change observed until the actuation voltage was higher than V_a= 1.39 V. With the increased actuation voltage, the drain current in the N-branch of the I_d-V_{gd} curve increased, but the drain current decreased in the P-branch and at the off-state (V_{gd}= −7 V). During the second round V_a sweep (defined in Figure 5-6), the I_d-V_{gd} curves at the same V_a overlap rather well. Figure 5-8 demonstrates the reproducibility/reversibility under strain cycling. The high reproducibility indicates that there was no irreversible change at the clamping sites, such as sliding, and the CNTs were strained within the elastic range.

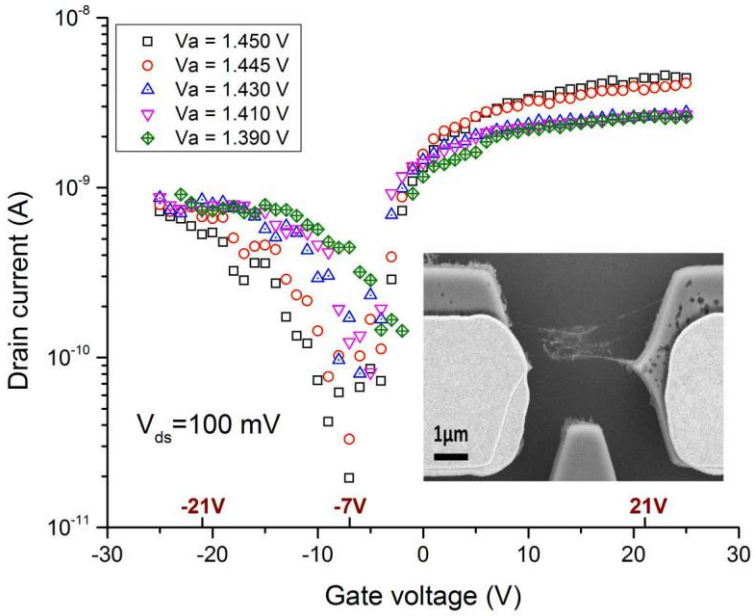


Figure 5-7 The selected I_d-V_{gd} curves at different actuation voltages. The inset is an SEM image of the CNT-device under test (D#BW1-C4D_C#SOIC4-R5C1).

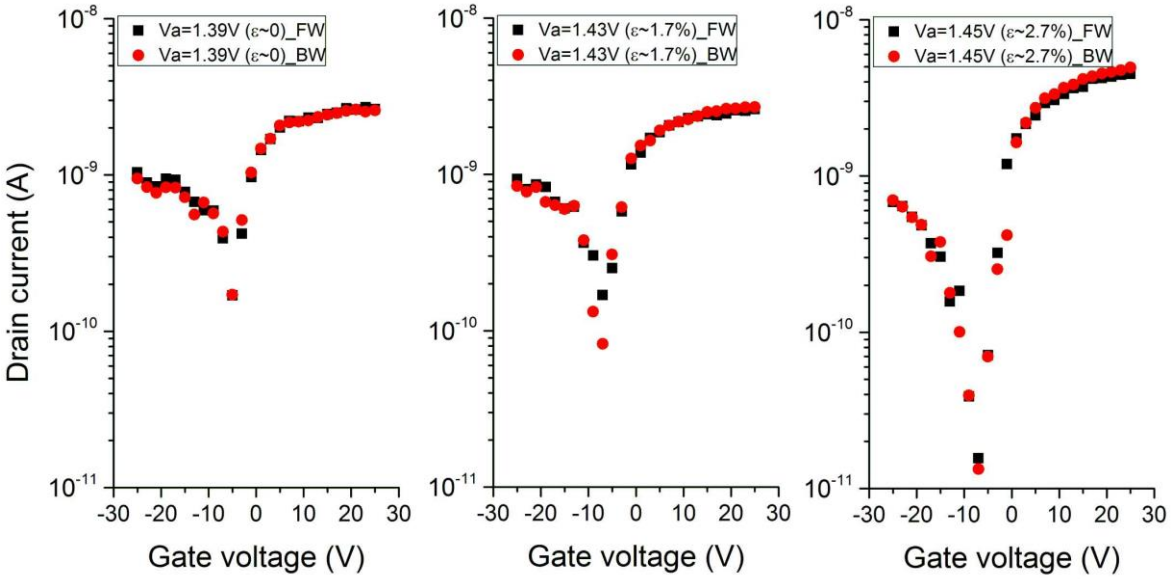


Figure 5-8 Reproducibility/reversibility of CNTFET transport measurements at different actuation voltages. The high reproducibility indicates there were no irreversible changes at the clamping, such as sliding, and the CNTs were strained within the elastic range. (FW: forward V_a sweep/ BW: backward V_a sweep in the measurement protocol) (D#BW1-C4D_C#SOIC4-R5C1).

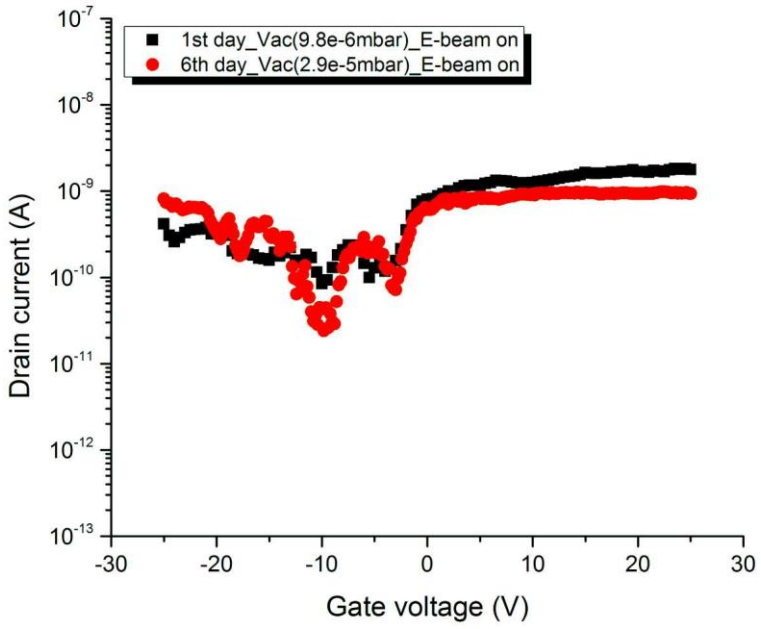


Figure 5-9 Two I_d-V_{gd} curves measured after a short E-beam scan in the first and sixth day. The similarity of these two curves indicates the integrity of the measured device (D#BW1-C4D_C#SOIC4-R5C1).

After 5 days, the same CNT device was measured again to confirm the integrity of the device. Similar transition of transistor characteristics was observed when the device was measured in N_2-rich air, in vacuum, and after E-beam scan in vacuum. After the short E-beam scanning, the drain current in the N-branch increased. As shown in Figure 5-9, the measured I_d-V_{gd} curve was similar to that measured in the first day, suggesting that the device was not damaged by the previous tensile tests.

5.1.4. Analysis

From the transport measurements during the tensile tests, the drain currents at three gate voltages were selected and plotted with V_a in Figure 5-10. These three selected gate voltages, V_{gd}= −21 V, −7 V, and +21 V, correspond to P-branch, off-state, and N-branch of the CNTFET respectively. In Figure 5-10, two types of current modulation are clearly seen. At the off-state, the drain current started to decrease at V_a= 1.39 V, while the current in N-branch started to increase at V_a= 1.43 V. However, two different modulation trends are not expected from one CNT. A uniaxial strain can change the band gap in a semiconducting CNT, and the chiral angle of the strained CNT determines the band gap change tendency [111]. The drain current will be modulated accordingly due to the band gap modification by strain [112]. Hence, the properties of the CNT determine increased or decreased current modulation upon strain. The existence of two different current change characteristics indicates that more than one CNT was involved during the tensile test. Additionally, these two current modulations were initiated at different V_a. This might result from different slack in different CNTs. The slack means the excessive CNT length compared to the distance

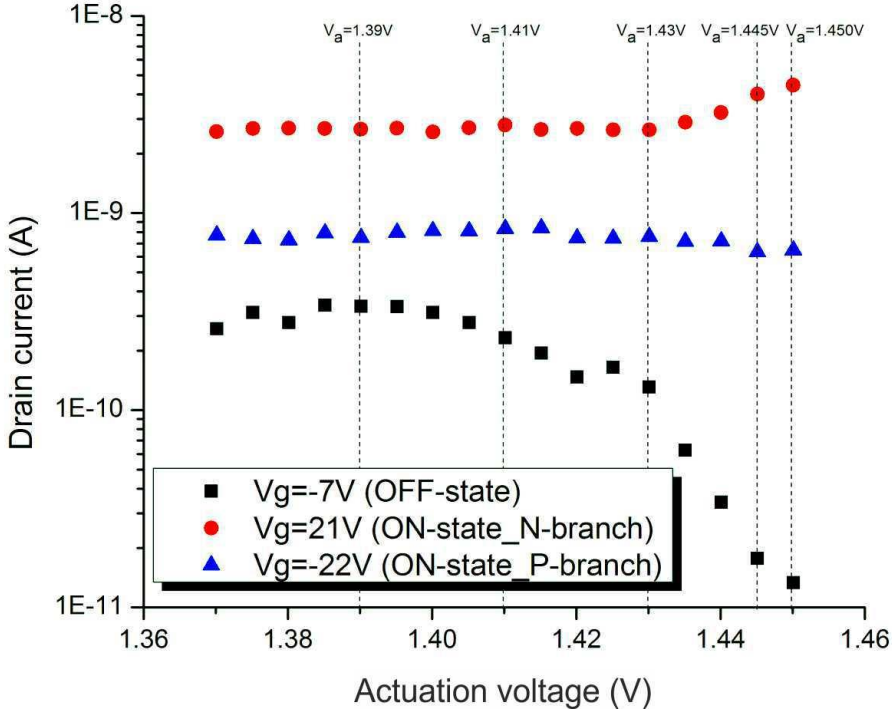


Figure 5-10 Drain current modulation at different gate biases, corresponding to different channel states of the CNTFET. The existence of two different current change characteristics indicates more than one CNT was involved in the tensile testes. The drain currents which were shown in Figure 5-7 are indicated by dashed lines.

between its two clamping sites.

It is assumed that only two CNTs were involved and responding during the tensile tests. One CNT contributed for the increased drain current (in N-branch), and the other was responsible for the decreased current (in P-branch and at off-state). The following analysis is focused on the measured decreased current at the off-state, i.e. V_{gd}= −7 V. To analyze the strain, the length of the responding CNT needs to be determined. From the SEM picture of the CNT device, the minimum possible CNT length was 3.7 µm and the maximum possible length was 4.3 µm. Hence, the length was assigned as 4 µm, and a 7.5% uncertainty was propagated in the following analysis. The elongation of the CNTs under test was calculated from the increased gap distance between the source and drain Si electrodes. By dividing the elongation by the assumed length of the CNTs, the strain was obtained The maximum resistance of a strained CNT can be correlated to the calculated strain (ε_{cnt}) by the following equation [65]

$$R_{\max}(\varepsilon_{cnt}) = R_0 + R_1 \cdot \exp(\beta \cdot \varepsilon_{cnt}) \tag{5.1}$$

The values of R_0, R_1 and β can be obtained by fitting the measured off-state resistances (at V_{gd}= −7 V) and the corresponding strain in a curve, as shown in Figure 5-11. Among these three parameters, β is the most important one because β is correlated to the band gap change

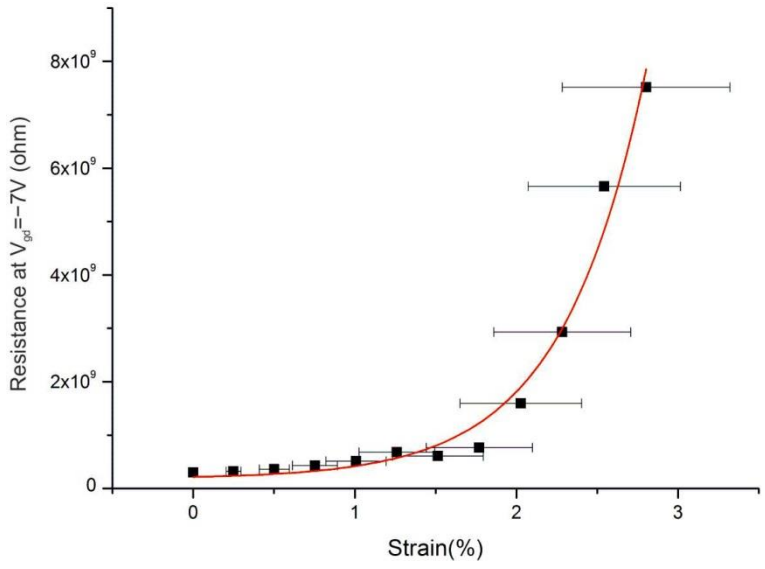


Figure 5-11 Curve fitting of the expression of the device resistances at V_{gd}= −7 V to the corresponding CNT strain levels.

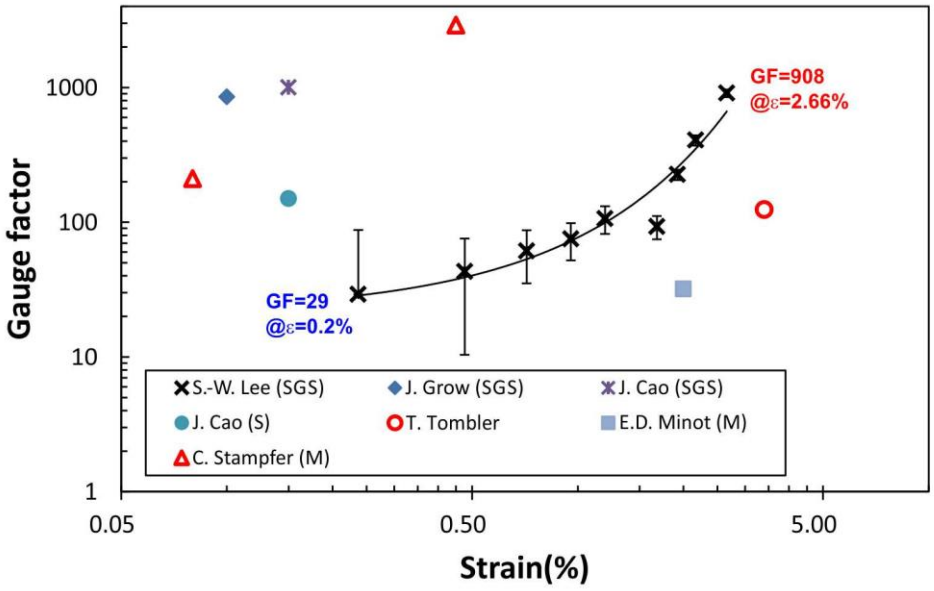


Figure 5-12 Comparison of the gauge factors with regard to strain extracted from this work and literature. The abbreviations, *S*, *SGS*, and *M* in the legend, stand for the electrical properties of the strained CNTs (*S*: semiconducting; *SGS:* small band gap semiconducting; *M*: metallic).

rate with strain by the following equation [65]

$$\frac{dE_{gap}}{d\varepsilon_{cnt}} = \beta kT \tag{5.2}$$

where k and T are Boltzmann constant and temperature. Taking the fitted β= 193 into Eq. (5.2), the strain-dependency of the band gap can be calculated as $\frac{dE_{gap}}{d\varepsilon_{cnt}} = +50\ meV/\%$ (T= 300 K). The theoretical strain change rate induced by axial strain is in the range of ±100 meV/% [113]. In addition, the gauge factors (*GF*) of the strained CNT can be calculated. By referencing to the zero strain at V_a= 1.39V, the gauge factor was increased from *GF*= 29 at ε_{cnt}= 0.2% to *GF*= 908 at ε_{cnt}= 2.6%. A comparison of the extracted gauge factors here and the gauge factors reported in literature [22, 23, 29, 65, 114, 115] is plotted in Figure 5-12. The calculation of the uncertainty of the extracted *GF* values was detailed in Appendix V. From the comparison, the extracted gauge factors at different strains are comparable with the results in literature. The analysis above is made on the basis of a fixed off-state gate voltage, i.e. V_{gd}= −7 V. During the tensile test, the gate voltage corresponding to the maximum device resistance was found to change gradually from V_{gd}= −4 V to

V_{gd}= −7 V, instead of being at a particular off-state gate voltage. This might be attributed to the fact that more than one CNT was involved in the tensile test. Hence, the gauge factor could be alternatively calculated based on the maximum measured device resistances. The maximum extracted gauge factors was GF= 175 (ε= 2.6%), assuming that the CNTs were strain-free at V_a= 1.395 V.

The high reproducibility of the tensile tests seen in Figure 5-8 can be attributed to the robust clamping and precision actuation. With the clamped-clamped configuration, the CNTs did not slide while they were strained. As a result, reproducible current modulation upon strain could be measured. In addition, the actuation system also plays an important role in the reversible tensile test. With the stable output displacement, the CNTs were held steadily while transport measurements were performed. The fine displacement resolution (~10 nm/5mV at V_a~ 1.4 V) made it possible to measure the static electrical response of the CNT to a small change in strain ($\Delta\varepsilon$= 0.25%).

A higher actuation voltage results in larger output displacement and higher actuator temperature. According to the modeling in [116], the drain current of a CNTFET at off-state increases with the increased temperature because the carriers in the CNTFET have higher energy at a higher temperature. During the tensile tests, the drain current at off-state (V_g= −7 V) decreased with the actuation voltage, as shown in Figure 5-10. As a result, the drain current modulation was mainly attributed to the piezoresistive response of the CNTs, rather than the increased temperature. Based on this, it is concluded that the heat flux is suppressed by the adapter. This confirms the effectiveness of the adapter in thermal insulation.

A transition of the transistor characteristics was observed after scanning the CNTFET briefly with the E-beam. The transition did not occur whilst the CNTFET was stored in the SEM vacuum chamber for one hour. Without additional energy, the gas molecules on the CNT surfaces were desorbed slowly, and they influenced the device transistor characteristics over a long time (at least for one hour). With additional energy, such as that provided by E-beam, the gas molecules could be released from the surfaces, and the device characteristics subsequently changed. This phenomenon is similar to the recovery mechanism of CNT gas sensors assisted by heat energy or UV light [117, 118]. In the experiment, the device characteristics only changed after the first E-beam scanning, and further E-beam exposure did not cause noticeable change.

5.2. Tunable CNT resonator

A mechanical strain influences not only the electrical band gap of a CNTFET but also the mechanical resonant frequency of the CNT when vibrating. If a CNT acts as a vibrating structure, the resonant frequency is increased with the applied axial strain [8]. If the applied uniaxial force is much higher than the CNT beam rigidity, the mechanical behavior of the CNT changes from that of a beam to that of a string [9, 119, 120].

5.2.1. Measurement technique

While a CNT is resonating at its resonant frequency, the amplitude of the mechanical vibration will be enhanced by the quality factor. The enhanced vibration amplitude leads to larger CNT-gate capacitance modulation as well as greater axial strain in the CNT. Both of these effects cause a change in the drain current of the CNT. As a result, by measuring the drain current variation, the resonant frequency of a CNT can be determined. Two measurement techniques have been developed respectively based on sensing *1-omega* current [24] and *2-omega* current [11, 121], where the *omega* is the mechanical vibration frequency of the CNT. The drain current measured by the *1-omega* technique includes two capacitive currents, which are respectively caused by the alternating gate voltage and the mechanical vibration of the CNT. In the *2-omega* technique, the drain current results from the piezoresistive effect of the CNT and a nonlinear mixing effect. However, the additional parasitic capacitances (metal leads to substrate) combined with the high CNT resistance (due to the electrical contacts of the CNT) form an electrical low pass filter around the CNT, which severely attenuates high frequency signals from the device. To resolve this problem, a mixing circuit technique is employed in these two measurement techniques [24]. The mixing technique applies two AC signals with a small frequency difference (Δf~*tens of kHz*) as the source-drain voltage (V_{sd}) and the gate voltage (V_{gd}). Using the CNT as a mixer, these two signals can be mixed, and a component with a low frequency of Δf in the drain current can propagate outside the device and be measured.

The advantage of the *2-omega* measurement technique is better signal to noise ratio compared with the capacitive measurement [11]. Here, *2-omega* measurement technique was employed to measure the tunable resonance frequency of the suspended CNTs integrated on MEMS actuators. The implementation of the measurement technique and the resonance measurements were contributed by Dr. Stuart Truax.

5.2.2. Refined design for high frequency measurements

- **Resistive handle layer**

To reduce the signal coupling through the substrate, the integration process was transferred to the second type of SOI chips, where the handle layer was highly resistive (ρ >2500 Ωcm). With the resistive handle layer, the signal coupling can be suppressed, even if the potential of the substrate is floating [122].

- **Refined layout**

To interface the CNT-MEMS device with five probes, the layout of the device had to be refined accordingly. The modified micro-structures are shown in Figure 5-13. To drive the actuator, two pads were fabricated for two DC probes ($+V_a$ and $-V_a$). Ground-signal-ground high frequency probes (GSG) were utilized with consideration to the transmission of high frequency signals in V_{gd} and V_{sd}. A GSG probe consists of three needles with a fixed pitch of 150 µm. Only the middle needle carries signals and the other two are grounded to reduce the electrical interferences. To land these two GSG probes (six needles) on one device, five

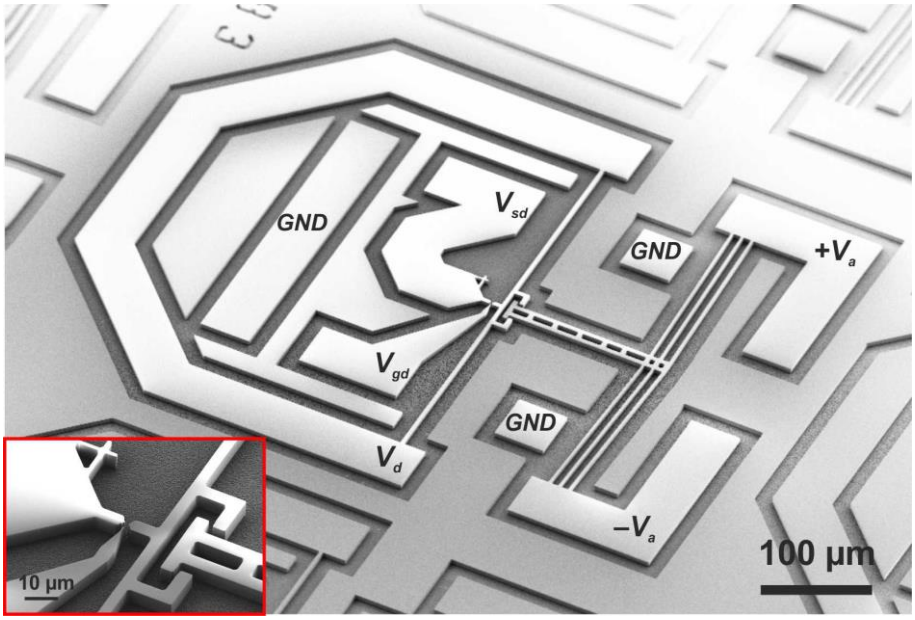


Figure 5-13 The refined micro-structures according to the probing requirements. To drive the actuator, two pads were fabricated for two DC probes ($+V_a$ & $-V_a$). To feed high frequency signals to CNT and measure the low frequency output, two RF GSG probes and one DC probe were used to connect the gate electrode (V_{gd}), source electrode (V_{sd}) and drain electrode (V_d) respectively. The inset shows the close-up of the site for integrated CNTs (C#SOIC4s_RVHFC1).

pads were fabricated, and one of them was shared by the two ground needles of the GSG probes. In addition to the four probes, the drain electrode was connected by a DC probe. The reason for the U-shaped drain electrode was for a symmetrical routing for the drain current.

Before resonance measurement, all the devices on a SOI chip (500 devices) were characterized by performing transport measurements, and working devices were identified and selected. The preliminary characterization was performed with DC probes, which inevitably scratch the Au layer (150 nm) during probing. To avoid the GSG probe landing on the scratched Au layer, the probing area of source and gate electrodes were elongated. Hence, there was sufficient space for two landing sites for both DC and GSG probes. As a result, reliable physical and electrical contacts between the GSG probes and the electrode can be ensured.

- **Undercut of the gate electrode**

In order to reduce the capacitive coupling among the source, drain and gate electrodes from the neighboring Si side walls, the lateral distances between two electrodes were enlarged. Consequently, the gate electrode was shrunk to a slim shape in the front end, as shown in the inset of Figure 5-13. The drawback of a slim gate electrode is the large suspended part of the electrode after liquid HF release. While applying the gate voltage on the gate electrode, the electrostatic force between the gate and substrate might cause the vibration of the suspended part of the gate electrode. Consequently, the electrical coupling with CNT would be influenced due to the mechanical vibration of the gate electrode. The resonance of the gate electrode would introduce a “fake” resonance peak in CNT resonance frequency measurement. The signal resulting from the vibration of the gate electrode could be identified by measuring a dummy device. However, if this resonant frequency is close to the resonant frequency of the suspended CNT under test, it would be difficult to decouple these two neighboring resonant peaks. By controlling the undercut of the gate electrode, the gate resonant frequency can be shifted away from the CNT resonance frequency range. The typical suspension length of the integrated CNTs is between 2 and 4 μm, corresponding to an initial fundamental resonant frequency range of 1 to 4 MHz (without pre-strain). A simulation of the first resonant frequency of the gate electrode with different undercuts could help to determine a suitable undercut. If the undercut was set 3 μm, the first resonant frequency of the gate electrode was 19.4 MHz. With an increase in undercut, the resonant

frequency was reduced and approaching the CNT resonant frequency range. When the undercut was 10 µm, the resonant frequency occurred at 3.9 MHz, which is in the same frequency range with the CNT resonant frequency. To reduce the minimum required undercut, the suspension structures were designed to be 5 µm wide, and etching holes were patterned for a larger suspended structure, as shown in Figure 4-5b. Hence, to completely release the actuator, the required undercut is around 3 µm. In this way, the resonant frequency of suspended CNTs can be distinguished from the resonance of the gate electrode.

5.2.3. Measurement setup and measurement results

A schematic diagram of the *2-omega* measurement system is shown in Figure 5-14. The actuator is not shown in the setup because it is electrically insulated from the CNT under test by the adapter (refer to section 4.3 for the adapter characterization). To implement the mixing circuit, two high frequency function generators were employed to output a gate voltage (V_{gd}^{ac}) and source-drain voltage (V_{sd}^{ac}) with frequency of f and $2f+\Delta f$ respectively. The current component with a specific frequency of Δf in the drain current was measured by a lock-in amplifier. To provide the lock-in amplifier with a reference signal with the frequency of Δf, a frequency mixer was used to mix the doubled frequency of V_{gd}^{ac} and the frequency of V_{sd}^{ac}.

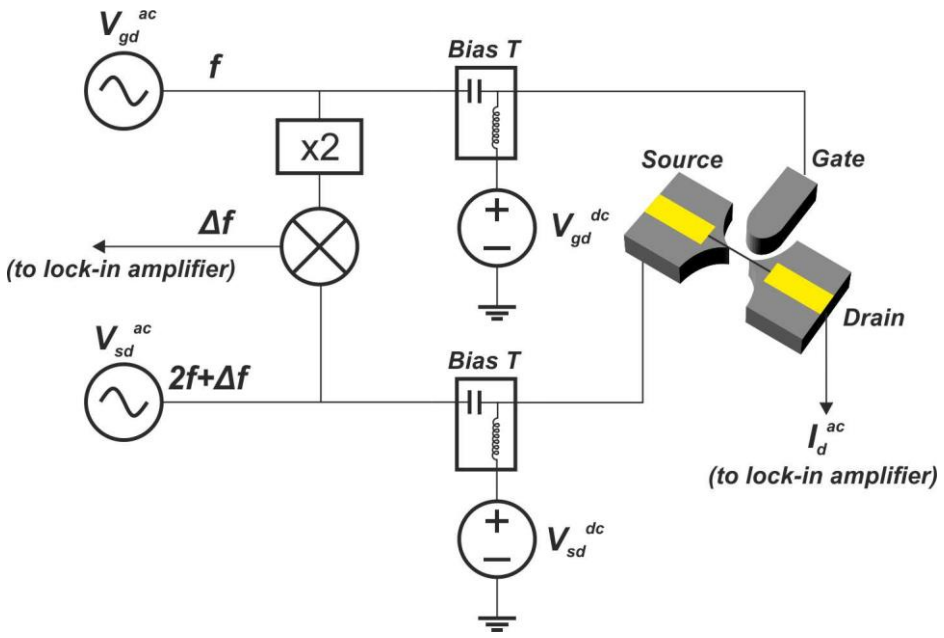


Figure 5-14 Schematic diagram of *2-omega* measurement (courtesy of Dr. S. Truax).

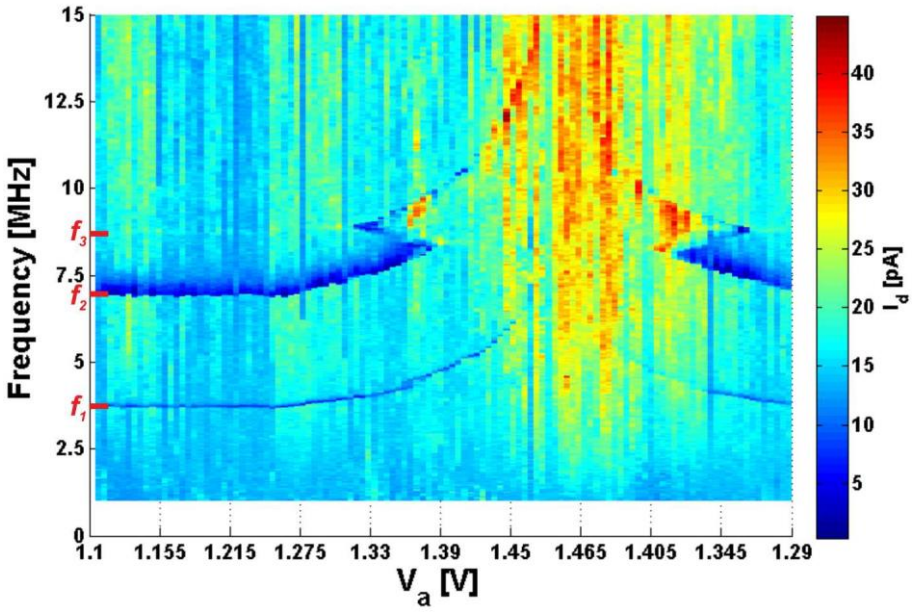


Figure 5-15 CNT resonant frequency tuned by the embedded actuation system. The resonant frequency increased with the actuation voltage of the actuator (V_a), starting from V_a= 1.27V. The color of the plot is representative of the measured *2-omega* current [124] (D#BE3-A1_C#SOIC4s-R4C1).

A similar measurement protocol to the tensile test was utilized for the strain-dependent frequency response measurements. The actuation voltage was increased to adjust the strain of the suspended CNT. At each individual actuation voltage, the frequencies of the gate voltage (V_{gd}^{ac}) and source-drain voltage (V_{sd}^{ac}) were swept in a defined range so as to measure the CNT resonance peak. A measurement of a strain-tunable CNT resonator is demonstrated in Figure 5-15 [123]. The measurement parameters are $V_{gd}^{ac} = 400\,mV\ (rms)$, $V_{sd}^{ac} = 7\,mV\ (rms)$, $V_{gd}^{dc} = 1V$, $V_{sd}^{dc} = 10mV$. The substrate was biased with 1 V, which was the same as the DC bias of the gate electrode. In Figure 5-15, there are three measured resonance peaks shown, and the initial frequencies (without strain) are f_1= 3.75 MHz, f_2= 6.96 MHz, and f_3= 8.71 MHz, respectively. The contrast of the third resonant peak was not high until it was increased with the actuation voltage. These resonance frequencies did not change when the actuation voltage was still lower than V_a= 1.27 V. But they were increased with the actuation voltage when the actuation voltage was higher than V_a= 1.27 V, as seen from Figure 5-15. Hence, this actuation voltage, V_a= 1.27 V, was determined as the contact voltage of the adapter (V_c). The increase in resonant frequency could be attributed to the reduction of the slack and the subsequent strain in the CNT. Comparing the trace of the

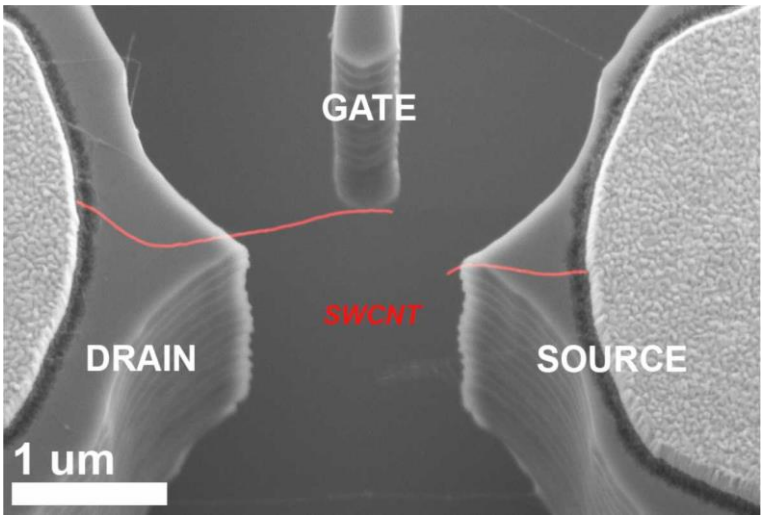


Figure 5-16 SEM image of the measured CNT device. The broken CNT is highlighted with red color for better visibility. The initial gap is g_0= 1.47 µm. The suspended CNT broke during the unloading procedure, and the image was taken after the measurement [124] (D#BE3-A1_C#SOIC4s-R4C1).

resonance frequency in the loading and unloading of axial strain procedure, the responses are found to be reproducible and consistent. However, the drain current dropped at V_a= 1.29 V during the backward sweep. After the measurement, the device was inspected by SEM. As shown in Figure 5-16, the suspended CNT was broken. This accounts for the loss of the drain current during the unloading procedure.

5.2.4. Analysis

The measured resonant frequencies increased with the applied actuation voltage, as shown in Figure 5-15. According to the characterization of the actuation system (shown in Figure 4-11), the displacement rate is around 1.9 nm/mV, which corresponds to a 300 nm displacement from V_a= 1.3 V to V_a= 1.45 V. The fundamental resonant frequency of a strained clamped-clamped CNT can be obtained by the following equation [8]

$$f_{F_{axial}} = \frac{4.73^2}{2\pi L_{cnt}^{\ 2}} \sqrt{\frac{E_{cnt} I_{cnt}}{\rho_{cnt} A_{cnt}}} \sqrt{1 + \frac{F_{axial} L_{cnt}^{\ 2}}{4\pi^2 E I_{\mathrm{m},cnt}}} \tag{5.3}$$

where L_{cnt} is the length of the CNT, E_{cnt} is the Young's modulus of the CNT, $I_{m,cnt}$ is the area moment of inertial, ρ_{cnt} is the mass density of the CNT, A_{cnt} is the cross-sectional area of the CNT, and F_{axial} is the axial force load. Using the calculated axial strain corresponding to the applied actuation voltage, the frequency change of the CNT resonances can be

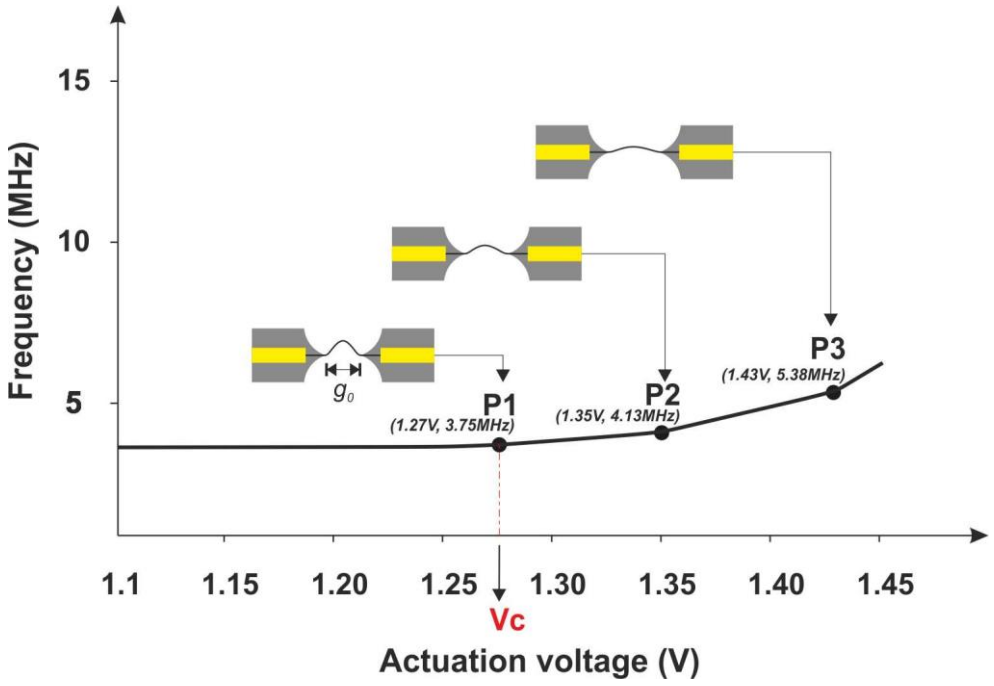


Figure 5-17 Re-plotted 1st frequency response versus actuation voltage and schematic sketches of the hypothesized slack at three different operation points.

calculated using the above theory. However, the calculated frequency change is higher than the corresponding measured frequency change by two orders of magnitude. This suggests that the increased resonant frequency is not induced by the strain-tuning effect described by the theory above.

An explanation for the slow frequency increase is the reduction of the CNT slack by the displacement of the actuation system. According to the modeling in [25], the presence of slack can influence the vibration modes of a suspended CNT. If a suspended CNT behaves like a hanging chain, the resonant frequency is dependent on the slack by the following relationship

$$f \propto S^{-\frac{1}{4}} \tag{5.4}$$

,where slack is denoted by *S*. Assuming slack was involved in the resonance measurement in Figure 5-15, a finite slack was taken into account in the following analysis. The hypothesized slack conditions are shown on three selected operation points in Figure 5-17. The initial distance between the two clamping sites of the CNT (g_0= 1.47 μm) was measured from the SEM image of the device (Figure 5-16). The displacement of the

Table 5-1 Simulation displacement based on measured actuation voltages and currents (simulation by COMSOL).

Point in Figure 5-17	Actuation voltage (V)	Increased displacement (nm)
Point 1	1.27 (V_c)	0 (reference)
Point 2	1.35	149
Point 3	1.43	325

actuation system was simulated by using the previously constructed finite element simulation model (refer to the COMSOL simulation in Appendix IV). The displacement at V_c= 1.27 V (point 1) is set at the initial state. By referring to point 1, the relative displacements at the other two selected points are listed in Table 5-1. According to Eq. (5.4), the resonant frequencies at point 3 and point 2 can be correlated as:

$$\frac{f_{P3}}{f_{P2}} = \left(\frac{S_{P3}}{S_{P2}}\right)^{-\frac{1}{4}} \tag{5.5}$$

The slack is defined by the following equation:

$$S = \frac{L_{cnt} - \left(g_0 + \Delta d\right)}{L_{cnt}} \tag{5.6}$$

,where Δd is the increased displacement of the adapter. Inserting the simulated increased displacements and measured resonant frequencies into Eq. (5.5) and Eq. (5.6), the length of the CNT is calculated as L_{cnt}= 1.89 μm. The initial slack is around 22%.

Slack can result in several vibration modes in directions perpendicular to the plane of the excitation force. When slack is reduced, these modes are expected to diminish [25]. This phenomenon can be observed in the second resonance peak in Figure 5-15. The signal of the second resonance peak was intense before the actuation system pulled the CNT, and it diminished at V_a= 1.4V, at which the slack was assumed to be mostly reduced.

Based on these two pieces of evidence discussed above, the increased resonant frequency can be attributed to the reduction of the slack in the range of V_a= 1.27V to V_a= 1.45V. Beyond this voltage range, the CNT resonator became slack-free, and further displacement of the actuation system could induce strain in the CNT, which would increase the CNT

resonant frequency rapidly. The vibration mode of the CNT will be quickly transited from beam vibration to string vibration if the uniaxial force is much larger than the critical force,$F_{critical} = 24 \cdot E_{cnt} I_{cnt} / {L_{cnt}}^2$ [120]. However, this transition force (~2.4 pN) is too small to be observed in the designed system, even if the actuator is driven by a voltage increment of ΔV_a= 1mV (corresponding to uniaxial force of ~1.6 nN), which is much larger than $F_{critical}$). As a result, after the gradual increases in frequency due to the reduction of the slack, the resonant frequency is expected to jump to several hundreds of MHz range due to entering the regime of string vibration.

5.3. Summary

In this chapter, the static electrical response and dynamic mechanical response to strain were demonstrated with the fabricated CNT-MEMS devices. The extracted gauge factors in the tensile test are comparable with findings in literature. Moreover, the measured increased fundamental resonance frequency can be theoretically explained by the reduction of slack.

Chapter 6 Conclusions and outlook

6.1. Conclusions

In this thesis, an integration process has been developed to fabricate low-defect suspended CNTs on MEMS actuators. With the supporting oxide bridge as well as the protective ALD Al_2O_3 layer, post-growth wet processing can be performed without the concerns for rupture and process-induced contamination. Taking advantage of the inert surface of CNTs for ALD nucleation and the oxide bridge, undesired CNTs can be selectively removed using oxygen plasma ashing, and correctly-aligned CNTs are preserved. With the protective ALD Al_2O_3 layer, the cleanliness of the contact interface between CNTs and metals can be preserved. The resist-free contact interfaces contribute to the improved device resistances of the fabricated CNTFETs. The device resistances are typically distributed in the range of 91 kΩ to few hundred kΩ. More than 70% of the investigated suspended CNTFETs showed stable device resistances (lower than 1 MΩ) in the period of 2 months in ambient storage conditions (humidity= 47%, temperature= 21 °C).

The top metallization enables the doubly-clamped configuration. With the robust clamping, CNTs can be anchored securely at the ends during the release process. Hence, the device resistances of the monitored CNTFETs changed less than ±171 kΩ after liquid HF release, and no consistent degradation was observed among these devices due to liquid HF release. In addition, robust clamping can prevent CNTs from sliding while they are subjected to strain. Reproducible and reversible strain tuning shown in the preliminary tensile tests prove the robustness of the doubly-clamped configuration.

In addition to the process integration, an adapter has been designed to make the CNT and the thermal actuator function independently and simultaneously. With this adapter, a suspended CNT can be mechanically strained by the embedded actuator while at the same time, the CNT under test is electrically insulated from the thermal actuator by native oxides. Moreover, the heat flux from the actuator is suppressed by the reduced contact areas within the adapter. The multi-functionalities of the adapter were proven by the preliminary tensile tests. With the integrated CNT-MEMS device, a tunable CNT resonator was demonstrated. The fundamental resonant frequency of the suspended CNT was modulated from 3.75 MHz to 6.30 MHz by the actuation system. The gentle increase in the resonant frequency is attributed to the reduction of the slack of the CNT.

A brief comparison between the present integration process and literature [30, 35, 39, 40, 47, 49, 50, 124-126] is made in Table 6-1. The main features of the developed integration process are listed below:

- Compatible with post-growth wet processing
- Post-growth top metallization
- Resist-free electrical contact interfaces
- Low device resistances
- Low-defect suspended CNTs
- Doubly-clamped configuration
- Selection of correctly-aligned CNTs
- Scalable integration process
- Low hysteresis of suspended CNTFETs operated in ambient conditions

In the integration, top-down surface micromachining assists the bottom-up CNT synthesis technique of cCVD by providing physical supports and enabling the CNT direction selection. Finally, the merger of the advantages in microtechnology and nanotechnlogy enables a broader operational range of the high frequency tunable CNT resonator.

6.2. Outlook

All the lithographic process steps in the integration process are based on photomasks. The fabrication of the CNT-MEMS devices are parallel processing. Five hundred MEMS devices can be fabricated on a single SOI chip of the dimensions of 1.8 cm by 1.8 cm. With the capability of selecting correctly-aligned CNTs, a reasonable yield of working CNT-MEMS devices out of the 500 MEMS devices can be expected. With sufficient number of CNT-MEMS devices, the device long-term stability can be further investigated. In this thesis, the device resistances were monitored for up to 2 months. However, it is still not clear what contributes most to the small device resistance variation over this period of time. Further studies are required to clarify the root cause for the possible device degradation. The long-term stability is a key criterion for practical applications.

After achieving reliable fabrication yield and long-term device stability, the process can be scaled up to wafer level processing, and can be further integrated with TSVs and CMOS-ICs. This will be a leap toward commercialization of CNT-devices.

Table 6-1 Comparison of state-of-the-art integration processes of suspended CNTs and MEMS

Author	Year	CNT synthesis	Si	Photo mask	Metal(s)	Device resistance	Actuation	Applications
Cassell [47]	1999	Directed growth with cCVD	Si (pillar)	V				
Franklin [30]	2002	Directed growth with cCVD	Poly	V	Mo (bottom)	S:100 kΩ-1MΩ M: tens of kΩ	Optional : AFM	• Electro-mechanical characteristics study
Williams [35]	2002	Assembly	Poly				Comb-drive (Electrostatic)	• Mechanical loading test
Englander [124]	2003	Local synthesis	Poly					• Low thermal budget
Jungen [49]	2007	Directed growth with cCVD	Poly (tip)	V			Bent-beam (Thermal)	
Karp [40]	2009	Directed growth with cCVD	SC	V	TiN (bottom)	12 MΩ	Comb-drive (Electrostatic)	
Muoth [50]	2010	Directed growth with cCVD	Poly (tip)		Pd (top)	330 kΩ 89 kΩ		• Hysteresis free CNTFETs
Zhou [125]	2010	Directed growth with laser-assisted CVD	SC		Ru (bottom)	0.8 GΩ~20 GΩ		
Muoth [126]	2012	Transfer	Poly		Pd (bottom)	2.5 MΩ 1.7 MΩ		• Hysteresis free CNTFETs
Muoth [39]	2013	Transfer	Poly		Pd (top & bottom)		Bent-beam (Thermal)	• Hysteresis free CNTFETs • Electro-mechanical characteristics study
This work	2013	cCVD with direction selection	SC	V	Cr/Au (top)	91 kΩ	Bent-beam (Thermal)	• Low hysteresis CNTFETs • Electro-mechanical characteristics study • Tunable resonators

Appendix

Appendix-I : Liquid HF and vapor HF

The release process in the integration process was mainly performed by liquid HF. To ensure the long term device stability, an additional ALD Al_2O_3 layer was employed to encapsulate the metal contacts of CNT devices. Liquid HF was once replaced by vapor HF in the integration process (SOIC4 and SOIC4s in Table 1-2) due to the better etching selectivity of Al_2O_3 over SiO_2. However, the encapsulation layer is not included in the standard integration process since the CNT devices with thin Cr (as thin as 2 nm or thinner) and 150-nm thick Au did not show severe degradation of device resistances in ambient conditions (investigated in Sect.3.8) within two months. Hence, the release process recipes of liquid and vapor HF were both developed. The following table briefly compares these two release methods.

Table A-1 Comparison of release processes of vapor HF and liquid HF.

Subjects	Vapor HF	Liquid HF
Accompanied process step	H_3PO_4 etching prior to vapor HF etching to remove Al_2O_3 layer	Drying in a super critical point dryer
Introduction of defects to CNTs	No	No
Etching uniformity	Etching rate is dependent on the location, and loading effect is observed	Relatively more uniform
Requirement for adhesion	At least 2 nm Cr (3 hour etching time at 60°C)	At least 0.5 nm Cr (3 min etching time)
Handling	Easy	Medium (chip surface might dry while bring transferred from the HF acid to DI water beaker)

In the integration process, a protective ALD Al_2O_3 layer is used to separate CNTs from resists during lithography steps. Note this Al_2O_3 layer is different from the encapsulation

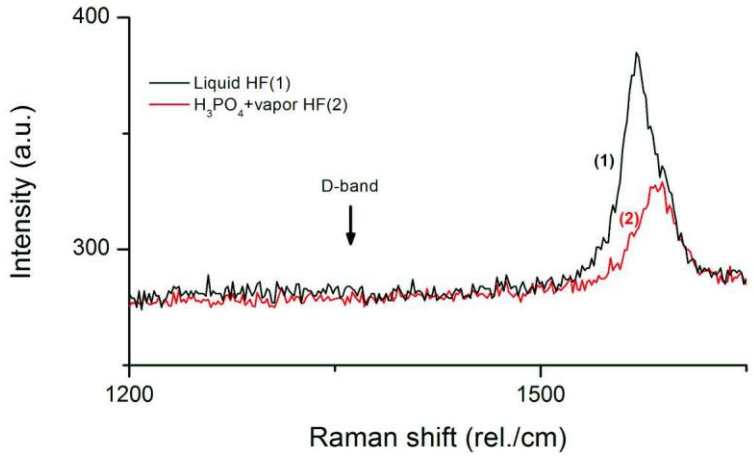


Figure A-1 Raman spectra of two suspended CNTs released respectively by HF (48% for 3 min) and H_3PO_4 (68% at 55 °C for 15 min) and vapor HF (at 40 °C for 2 hours) (integration time= 60 s). No noticeable D-band peak is observed in these spectra [63] (D#20-5A_C#SOIC3-R3C2 by liquid HF / D#23-6F_C#SOIC3-R3C8 by H_3PO_4 and vapor HF). © 2014, Elsevier

layer for long-term device stability. In order to etch SiO_2 by vapor HF, the protective Al_2O_3 layer needs to be removed in H_3PO_4 (56% at 55°C) for 15 min prior to vapor HF etching. Figure A-1 [63] shows two Raman spectra of two suspended CNTs released by liquid and vapor HF respectively. The absence of D band peak in these spectra indicates both of these two release approaches did not cause defects in CNTs.

Appendix-II : Device stability of non-suspended CNT devices

In addition to the suspended CNT devices (Sec. 3.8), the device stability of non-suspended CNTs was also investigated. The following investigation was performed on two types of CNT devices, namely devices contacted with Au alone and Cr/Au.

- **150 nm Au alone**

Twenty non-suspended Au-contacted CNTFETs were stored in ambient air (relative humidity= 47%, temperature= 21°C, in the ETH FIRST cleanroom) for one month, and these devices were measured periodically. To reveal the variation of the contact resistances, these 20 devices were divided into two groups according to the gate modulation characteristics. For CNTFETs which could be well modulated by the gate voltages, the on-state device resistance or minimum resistance was used for long-term resistance monitoring. Figure A-2a shows a typical I_d-V_{gd} curve of this type of device, and the resistance at V_{gd}= 10 V was recorded. For the rest of the CNTFETs with weak gate modulation, the monitored resistance was selected as the resistance at V_{gd}= 0 V. A typical transport characteristic of this type CNTFET is shown in Figure A-2b. The electrical measurements were performed by the semiconductor characterization system, Keithley 4200. The measured resistances of these two types of CNTFETs are shown in Figure A-3. There was no consistent degradation tendency shown by these devices.

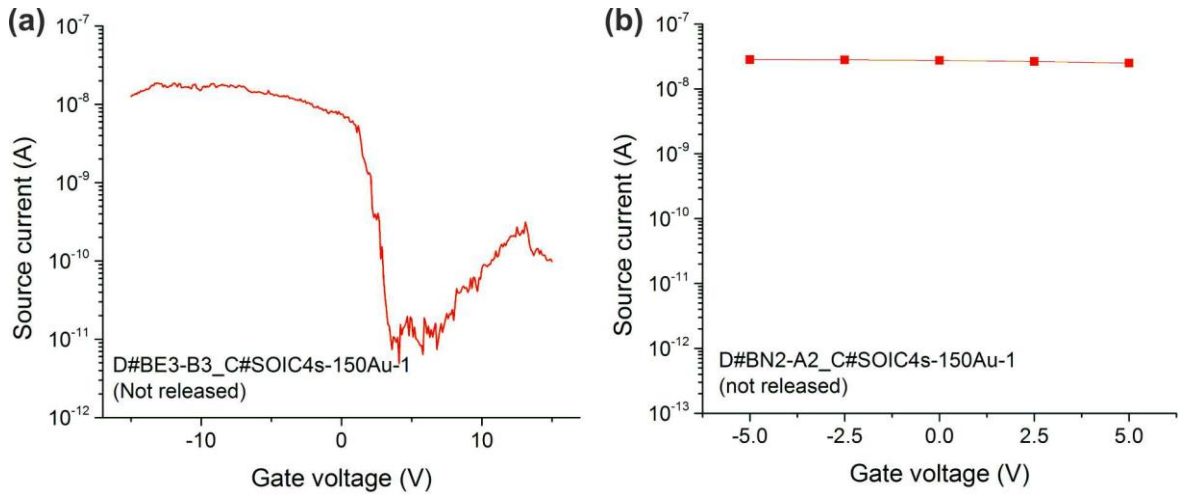


Figure A-2 (a) Transport measurement of a non-suspended CNTFET with good gate modulation; (b) transport measurement of a non-suspended CNTFET with weak gate modulation.

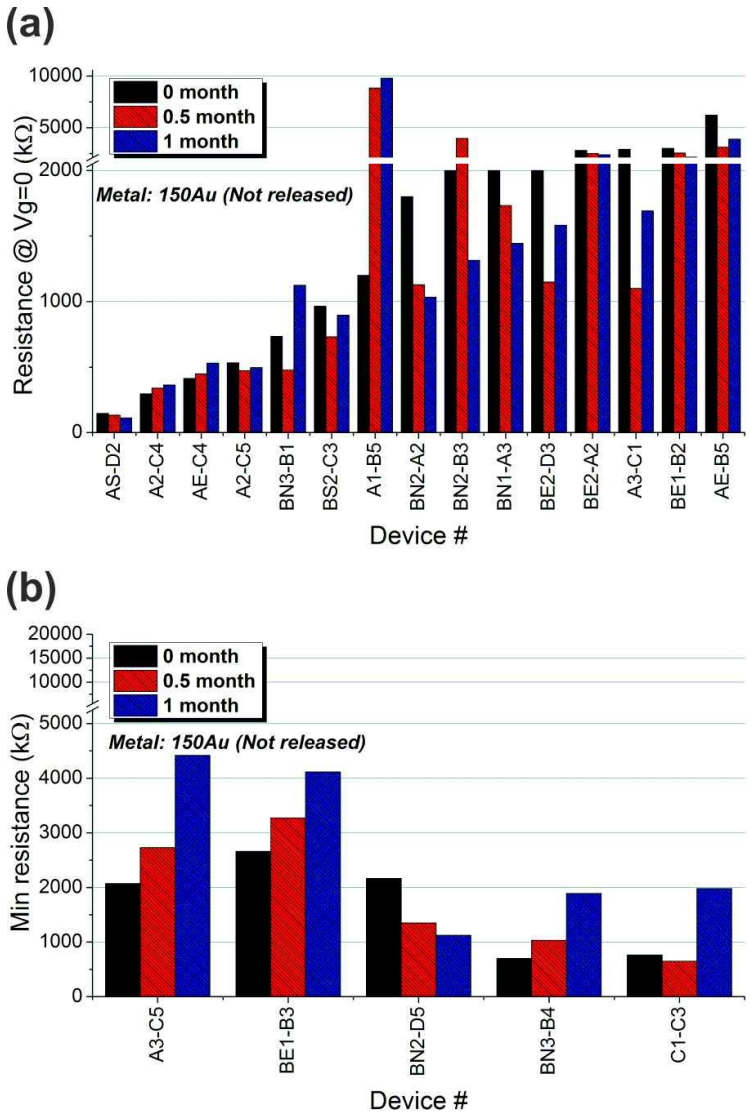


Figure A-3 (a) Resistances at V_{gd}= 0 V of 15 CNTFETs (weak gate coupling) measured within one month; (b) minimum (so-called on-state) resistances of 5 CNTFETs (good gate coupling) measured within one month (C#SOIC4s-150Au-1).

- **0.5/1/2 nm Cr and 150 nm Au**

The second type CNTFETs were electrically contacted with an adhesion layer and a metal layer, i.e. 0.5/1/2 nm Cr and 150 nm Au. The conditions of the four investigated SOI chips are listed in Table A-2. There were 97 devices in total measured for at least for 2 months. One of these chips, C#SOIC5(NR)-1Cr150Au-1, was fabricated 2 months earlier, and the devices on this chip were monitored for 4 months. The measurement setup and parameters and the storage conditions are the same with previous Au-contacted CNTFETs. The same

Table A-2 Conditions of the four SOI chips with non-suspended CNTFETs for the long-term stability investigation.

Metals	**0.5 nm Cr/150 nm Au**	**1 nm Cr/150 nm Au**	**2 nm Cr/150 nm Au**
Chips	C#SOIC5(NR)-0.5Cr150Au	C#SOIC5(NR)-1Cr150Au-1&2	C#SOIC5(NR)-2Cr150Au
Number of devices	47	19	31
Monitoring duration	2 months	4 months for 1Cr150Au-1 2 months for 1Cr150Au-2	2 months

device classification rule was applied to divide the devices into two groups, namely gate-modulated CNTFETs and weak gate-modulated CNTFETs.

The transport measurements of three non-suspended CNTFETs with different Cr thicknesses are shown in Figure A-4a, b, and c respectively. Within the monitoring period of 8 weeks, none of the three types of the CNTFETs showed a consistent or noticeable degradation. Similar resistance variations with regard to time can be found in the measurements of the monitored devices, as shown in Figure A-4d to Figure A-4f and Figure A-5. On the other hand, it is also found that few of the monitored devices, for example G10 on C#SOIC5(NR)-0.5Cr150Au and F22 on C#SOIC5(NR)-2Cr150Au, did show gradually increased resistances in ambient air.

To evaluate the device stability of these measured CNTFETs, a criterion for a device with good contacts was set as R_{min}<1 MΩ. At the end of the monitoring time, 4 months for C#SOIC5(NR)-1Cr150Au-1, and 2 months for the rest chips, more than 72% of the non-suspended devices remained qualified. The details are listed in Table A-3. The results are comparable with those of suspended CNTFETs investigated in Sec. 3.8.2. In addition, the yield did not show a correlation with the thickness of the Cr layer.

Table A-3 Stability of the **non-suspended** CNTFETs with good electrical contacts ($R_{m,initial}$<1 MΩ)

Metal	**# of devices ($R_{m,initial}$ < 1 MΩ)**	**# of devices (R_m<1 MΩ after 2 or 4 months)**
0.5Cr150Au	29	21 (72%)
1Cr150Au	11	11 (100%)
2Cr150Au	22	19 (86%)

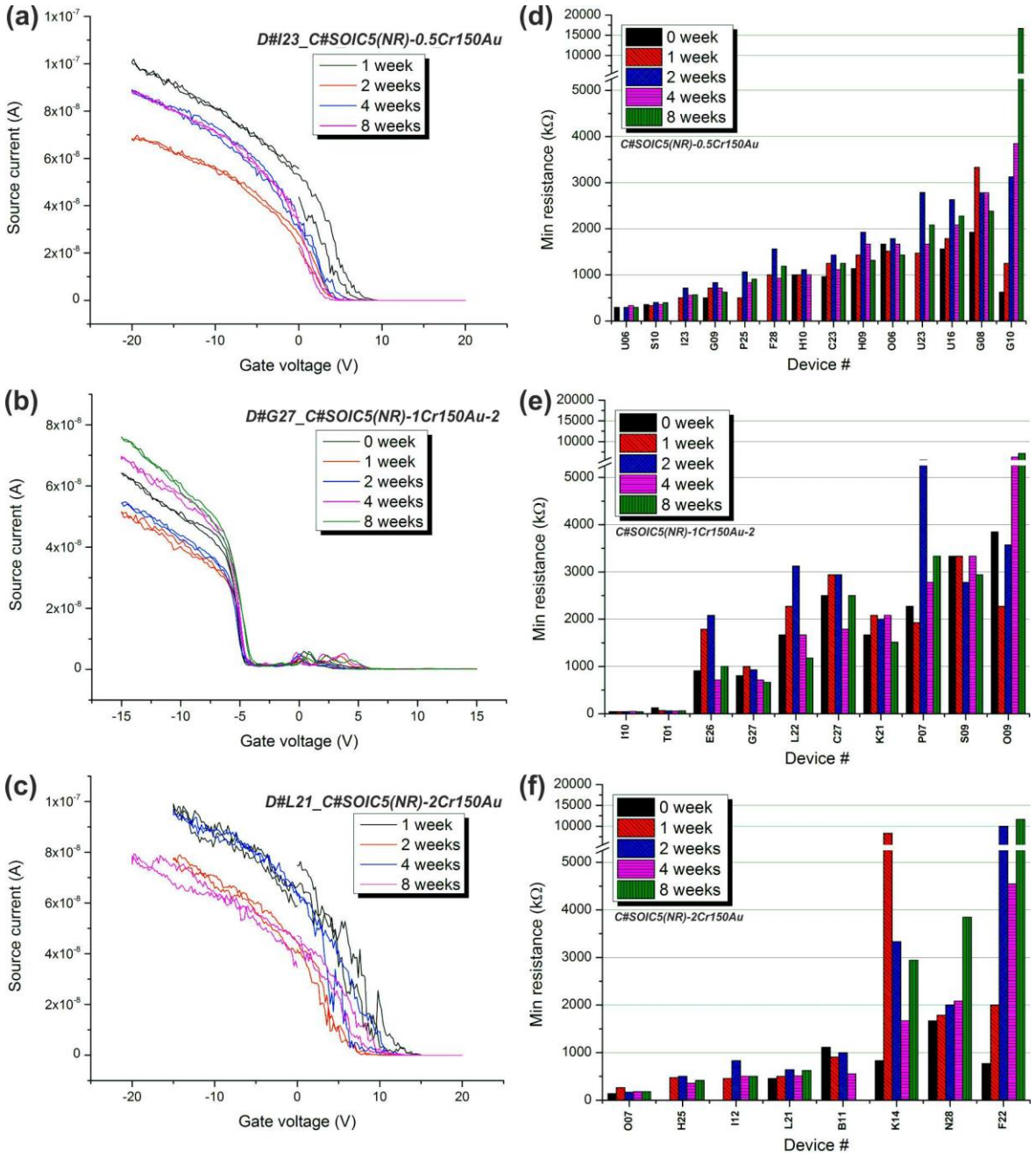


Figure A-4 Device stability monitoring of **non-suspended well gate-modulated** CNTFETs within 8 weeks. The transport measurements of 3 example CNTFETs with different Cr thicknesses and 150 nm Au are shown in (a) 0.5 nm Cr; (b) 1 nm Cr; (c) 2 nm Cr. The minimum measured resistances of all the gate-modulated CNTFETs within 8 weeks with (d) 0.5 nm Cr; (e) 1 nm Cr; (f) 2 nm Cr and 150 nm Au.

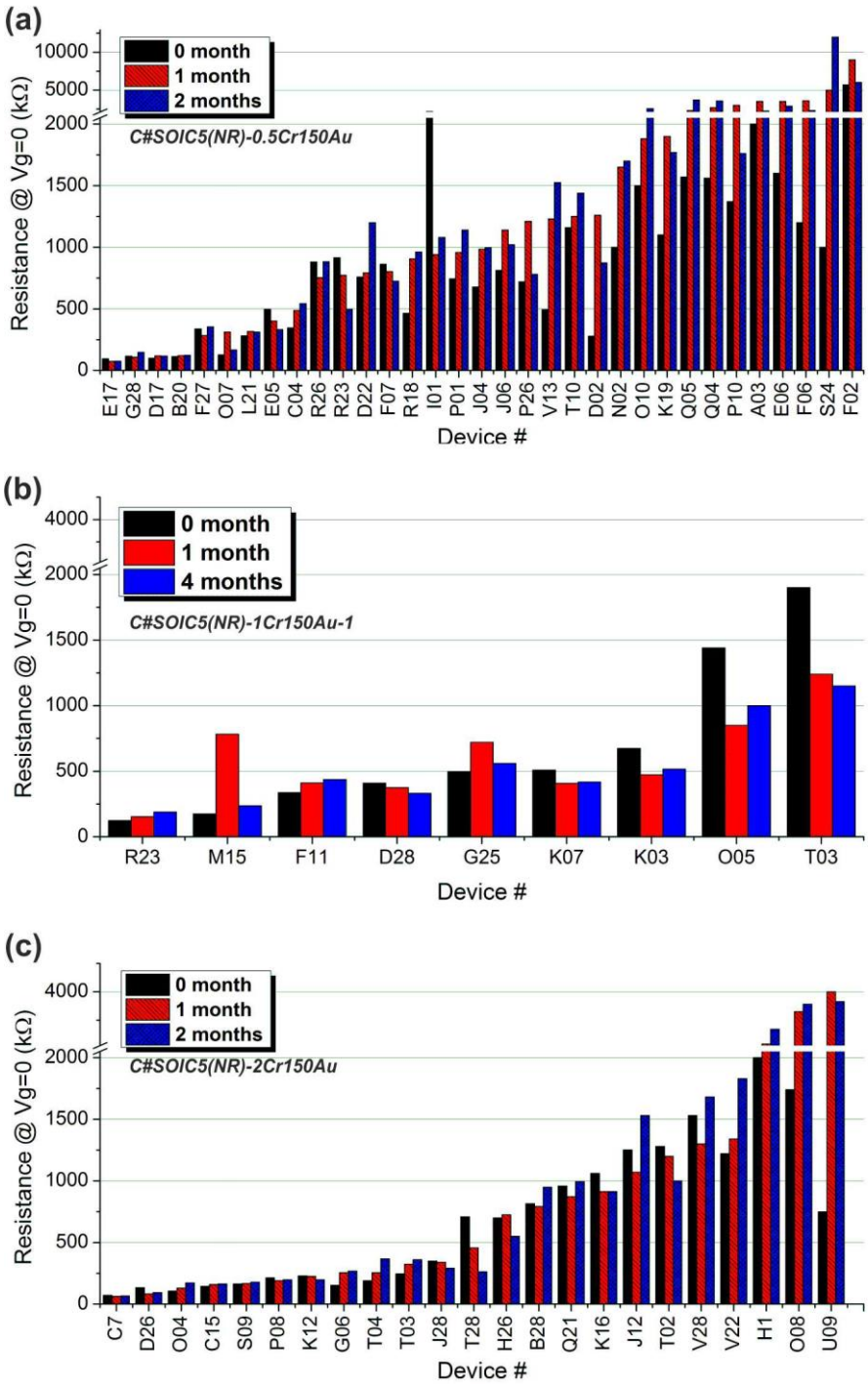


Figure A-5 Stability measurement of **non-suspended** **weak gate-modulated** CNTFETs for 8 (or16) weeks. The measured resistances with gate bias V_{gd}= 0 V of all the weak gate-modulated CNTFETs with (a) 0.5 nm Cr, (b) 1 nm Cr, (c) 2 nm Cr and 150 nm Au.

Appendix-III : Index of CNTFETs

Table A-4 Index of CNTFETs.

Device #	Transport measurement	Raman spectrum	SEM	Section
D#13_C#SOIC3-R2C1			Figure 3-7	Sec.3.4.4.
D#20-5A_C#SOIC3-R3C2	Figure 3-19 Figure 3-24	Figure 3-17a Figure A-1	Figure 3-8a Figure 3-16a	Sec.3.4.4. Sec. 3.6.3 Sec. 3.7 Appendix I
D#23-4c_C#SOIC3-R3C5			Figure 3-8b	Sec.3.4.4.
D#E19_C#SOIC5-STB2C1		Figure 3-9		Sec.3.5.1
D#E06_C#SOIC5-1Cr150Au	Figure 3-10			Sec.3.5.2.
D#21-7D_C#SOIC3-R5C1		Figure 3-17a	Figure 3-16b	Sec.3.6.3.
D#11H_C#SOIC3-R3C5	Figure 3-29		Figure 3-29	Sec.3.9.2.
D#LF3FET4L_C#SOIC2-R6S3	Figure 3-31b		Figure 3-31a	Sec.3.9.2.
D#23-6F_C#SOIC3-R3C8		Figure A-1		Appendix I
C#SOIC3-R4C1				Sec.3.7
C#SOIC4s-150Au-1 & -2				Sec. 3.8.1 Appendix II

Appendix-IV : Simulation of temperature distribution

A commercial simulation tool, COMSOL (ver.4.3a), was used to simulate the joule heating in the bent-beams, and the resulting temperature distribution as well as the mechanical deformation. In the multi-physics model, three modules were employed, i.e. *Electric currents (ec)*, *Heat transfer in solids (ht)*, and *Solid mechanics (solid)*. In the heat transfer module, only the heat conduction was taken into account. Some of the parameters for the 3D model were measured from the fabricated devices or extracted from the measurements. The other parameters for material properties were taken or derived from literature. The major parameters used in the simulation are listed in Table A-5.

Table A-5 Major parameters for the multi-physics simulation by COMSOL.

Parameters		Value	Source
Bent-beam dimensions	Width	2 μm	Measured (SEM)
	Length	175 μm	Mask layout
	Thickness	4.2 μm	Measured (Interferometer)
	Inclined angle	2°	Mask layout
Suspended beam dimensions	Width	3 μm	Measured (SEM)
	Length	370 μm	Mask layout
	Thickness	4.2 μm	Measured (Interferometer)
The gap of the spacer in the adapter		1.4 μm	Measured (SEM)
Temperature-dependent electrical conductivity (Silicon)		32152-25·T [S/m*K] (T=293~328 K)	Measured (4-point probe and a thermal chock)
Young's Modulus (Silicon)		169 GPa (110)	Reference [127]
Temperature-dependent thermal conductivity (Silicon)		$(-1.12 \times 10^{-6}) \times T^3 + (2.31 \times 10^{-3}) \times T^2 - 1.66 \times T + 463$ [W/(m*K)] (valid for T=300~800 K)	Reference [128]
Temperature-dependent thermal expansion coefficient (Silicon)		$10^{-6} \times [(1.53 \times 10^{-8}) \times T^3 - (3.13 \times 10^{-5}) \times T^2 + (2.24 \times 10^{-2}) \times T - 1.69]$ [1/K] (Valid for Temp=300~800 K)	Reference [129]

The electrical conductivity of a bare SOI wafer was measured by a four-point probe. However, the distribution of Boron dopants changed due to the thermal oxidation. In addition, the device layer was trimmed by thermal oxidation and mechanical polishing. So, the electrical conductivity of the device layer at the end of the process would be different

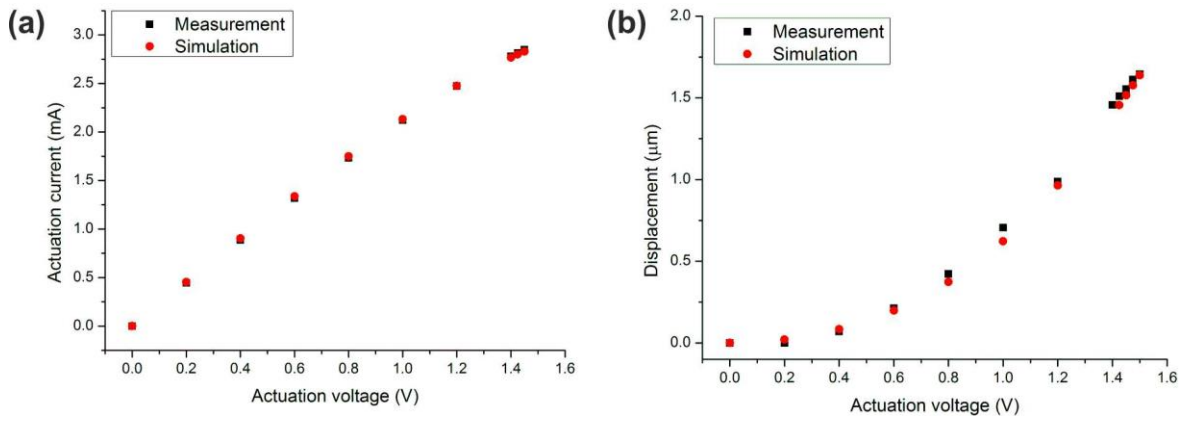


Figure A-6 Comparison of measurement and simulation of the actuator operated in vacuum (a) actuation currents and (b) actuator displacement with the actuation voltages.

from that measured on the SOI wafer. In the simulation, the electrical conductivity of an SOI wafer was refined according to the measured actuation voltages and currents recorded in the characterization of the actuator. Iteration was carried out with two modules, i.e. *Electric current* and *Heat transfer in solids*. The conductivity was refined as $\sigma_e = \sigma_0 - C_0 \cdot T$, where $\sigma_0 = 25500$ S/m, $C_0 = 25$ S/(m·K), and T is the temperature in Kelvin. Figure A-6a shows the measured and simulated actuation currents and voltages.

The following simulation was performed in two parts. The first was the simulation of the displacement and the voltages of the actuator before the T-shaped structure started to pull the hook. The second part was the simulation of the displacements, the voltages, and the temperature distribution while the T-shaped structure was in contact with the hook. The reason why the simulation was performed in two parts is to avoid the complex simulation of the contact voltage of the adapter, at which the two components were about to be in contact. Hence, a small transition during contact beginning was not included in the simulation, but this did not influence the simulation of the temperature distribution after contact.

In the first part, only the actuator part (including the T-shaped structure) was simulated. Iteration among the three physics modules was performed, and actuator displacements at various actuation voltages were obtained.

In the second part, the simulation started from the status that the T-shaped structure and the hook were in contact. In the *Electric current* module, only the actuator was included since the hook was electrically isolated from the actuator by the native oxides at least up to

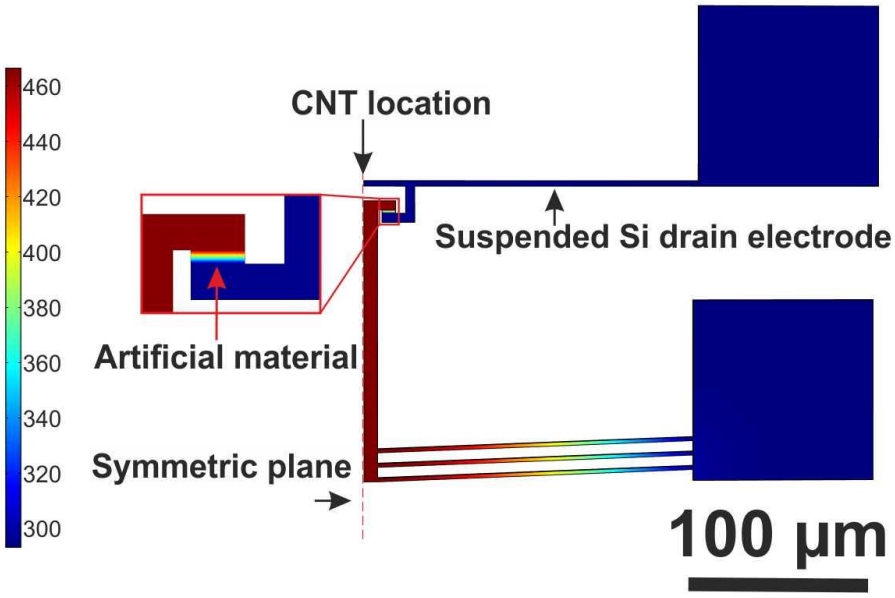


Figure A-7 Simulated temperature distribution at actuation voltage V_a= 1.5 V. The artificial material was created to simulate the heat conduction through the interface. The simulated temperature difference between the hook and the T-shaped structure is 191 K.

V_a= 4 V (see section 4.1.2) The actuation voltage swept from 1.4 V to 1.5 V by increments of 0.025V. In the *Heat transfer in solids* module, both the actuator and the suspended Si drain were taken into account. Additionally, to simulate the heat transfer through the interface, an artificial material was created and inserted between the T-shaped structure and the hook. Once the temperature distribution was obtained, the displacement of the actuator was subsequently simulated in *Solid mechanics* with a force loading, which was representative of the restoring force of the suspended Si drain electrode. The thermal conductivity of the artificial material determines the heat flux from the actuator to the suspended Si drain electrode, which influences the temperature distribution and the resulting displacement. The thermal conductivity of the artificial material was iterated until the simulated displacement fitted the measured displacement for all the simulated voltages. The simulated actuator displacements for the entire actuation voltage range were plotted together with the measurement results in Figure A-6b. The simulated temperature distribution at V_a= 1.5 V is shown in Figure A-7. The temperature difference between the T-shaped structure and the hook is 191 K. The heat flux through the articifical material, namely through the interface, is 20.2 µW. Hence, the thermal conductance is 105 nW/K.

Appendix-V : Propagation of uncertainties

- **Uncertainty of strain**

During the tensile tests, the smallest increment of the actuation voltage was 5 mV. Due to the limited resolution of the manual measurement by SEM inspection, the displacements of the adapter were measured with a larger incremental voltage of 25 mV so that noticeable displacements could be properly measured. The measured adapter displacements were fitted by a curve. The obtained curve was use for the displacement interpolation between V_a= 1.35 V to V_a= 1.50V. This resulted in a displacement uncertainty of 3.57%.

As shown in the inset in Figure 5-7, there were several CNTs in the measured device. The maximum possible CNT length was 4.3 µm, and the minimum possible length was 3.7 µm. As a result, the CNT length was determined as l_{cnt}= 4 um with 7.5% uncertainty.

The strain of the CNT is defined as

$$\varepsilon_{cnt} = \frac{d}{l_{cnt}} \tag{A-1}$$

,where d is the adapter displacement. According to the formula of error propagation [130], the error in the strain can be expressed as

$$\Delta\varepsilon_{cnt} = \sqrt{(\frac{1}{l_{cnt}})^2 \cdot \Delta d^2 + (\frac{d}{l_{cnt}^2})^2 \cdot \Delta l_{cnt}^2} \tag{A-2}$$

The strain uncertainty is $\Delta\varepsilon_{cnt}/\varepsilon_{cnt} = 8.3\%$.

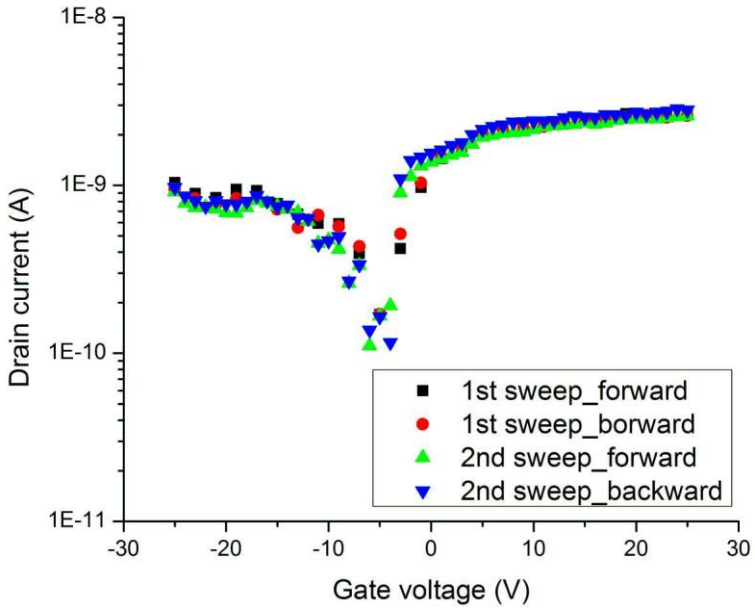


Figure A-8 Four I_d-V_{gd} curves measured at V_a=1.39 V.

- **Uncertainty of gauge factor**

The uncertainty of the drain current was derived from four measured I_d-V_{gd} curves at V_a= 1.39 V, as shown in Figure A-8. The uncertainty of the measured drain current at OFF-state (V_{gd}= 7 V) is 12.9%.

The gauge factor is expressed as

$$GF = \frac{\Delta R_{cnt}}{R_{cnt}} \cdot \varepsilon_{cnt} \tag{A-3}$$

The absolute error of the gauge factor is

$$\Delta GF = \sqrt{\left(\frac{I_0}{I_{\varepsilon_{cnt}}} - 1\right)^2 \cdot \frac{\Delta \varepsilon_{cnt}{}^2}{\varepsilon_{cnt}{}^4} + \frac{I_0{}^2}{\varepsilon_{cnt}{}^2 \cdot I_{\varepsilon_{cnt}}{}^4} \cdot \Delta I_{\varepsilon_{cnt}}{}^2} \tag{A-4}$$

,where the I_0 is the drain current at ε= 0, and $I_{\varepsilon_{cnt}}$ is the drain current at ε_{cnt}. Inserting the uncertainties of the strain and drain current into Eq.A4, the error of the gauge factor was calculated at each strain level. The result is plotted in Figure 5-12.

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Publications

Reviewed journal articles

a1. S.-W. Lee, M. Muoth, T. Helbling, M. Mattmann, and C. Hierold, "Suppression of resist contamination during photolithography on carbon nanomaterials by a sacrificial layer," *Carbon*, vol. 66, pp. 295-301, 2014.

a2. S.-W. Lee, S. Truax, Y. Liu, C. Roman, and C. Hierold, "Carbon nanotube resonators with capacitive and piezoresistive current modulation readout," *Applied Physics Letters*, vol. 103, 2013.

a3. M. Muoth, S. -W. Lee, K. Chikkadi, M. Mattmann, T. Helbling, A. Intlekofer, and C. Hierold, "Encapsulation of electrical contacts for suspended single-walled carbon nanotubes by atomic layer deposition," *physica status solidi (b)*, vol. 247, pp. 2997-3001, 2010.

a4. M. Muoth, T. Helbling, L. Durrer, S.-W. Lee, C. Roman, and C. Hierold, "Hysteresis-free operation of suspended carbon nanotube transistors," *Nature Nanotechnology*, vol. 5, pp. 589-592, 2010.

a5. M. Muoth, F. Gramm, K. Asaka, L. Durrer, T. Helbling, C. Roman, S. -W. Lee, and C. Hierold, "Chirality assignment to carbon nanotubes integrated in MEMS by tilted-view transmission electron microscopy," *Sensors and Actuators B: Chemical*, vol. 154, pp. 155-159, 2011.

Conference proceedings (reviewed)

c1. S.-W. Lee, M. Muoth, L. Durrer, C. Roman, and C. Hierold, "Integration of clamped-clamped suspended single-walled carbon nanotubes into SOI MEMS," 6th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS 2011), Feb. 20-23, Kaohsiung, Taiwan, pp. 37-40, 2011.

c2. M. Muoth, F. Gramm, K. Asaka, L. Durrer, T. Helbling, C. Roman, S. -W. Lee, and C. Hierold, "Tilted-view transmission electron microscopy-access for chirality assignment to carbon nanotubes integrated in MEMS," Eurosensors XXIII Conference, September 6-9, Lausanne, Switzerland, pp. 601-604, 2009.

c3. M. Muoth, S.-W. Lee, and C. Hierold, "Platform for strainable, TEM-compatible, MEMS-embedded carbon nanotube transistors," 24th International Conference on Micro Electro Mechanical Systems (MEMS 2011), January 23-27, Cancun, Mexico, pp. 83-86, 2011.

c4. R. Gueye, S.-W. Lee, W. A. Vitale, S. Truax, T. Akiyama1, C. Roman, A. Ionescu, C. Hierold, D. Briand, and N.F. de Rooij, "RF-TSVs compatible with harsh-environment post-processing for VIA-FIRST 3D integration," The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 2013), Jun. 16-20, Barcelona, Spain, 2013.

c5. W. Liu, K. Chikkadi, S.-W. Lee, C. Hierold, and M. Haluska, "Fabrication of CNTFETs with low-resistance electrical contacts," The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers 2013), Jun. 16-20, Barcelona, Spain, 2013.

Poster presentation

p1. S.-W. Lee, M. Muoth, T. Helbling, M. Mattmann, and C. Hierold, "ALD-assisted metal lift-off for contamination-free contact areas to carbon nanotubes," presented at the 36th Int. Conf. on Micro and Nano Engineering (MNE 2010), Genoa, Italy, Sept 19-22, 2010.

p2. M. Muoth, S.-W. Lee, L. Durrer, T. Helbling, F. Gramm, and C. Hierold, "Electrical contact formation for suspended single-walled carbon nanotubes," in 3rd *MRC Graduate Symposium, ETH Zurich*, Zurich, Switzerland, May 14, 2008.

p3. M. Muoth, S.-W. Lee, L. Durrer, T. Helbling, R. Grundbacher, and C. Hierold, "Suspended single-walled carbon nanotubes integrated in electromechanical systems," in 4th *MRC Graduate Symposium, ETH Zurich*, Zurich, Switzerland, June 10, 2009.

p4. S.-W. Lee, M. Muoth, C. Roman, H. Chandrahalim, C. Hierold, "Integration of suspended single-walled carbon nanotubes in SOI MEMS," in *Annual Meeting of nano-tera.ch*, Bern, Switzerland, April 29, 2010.

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Curriculum vitae

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