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Bufler, F.M.; Smith, L.

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3D Monte Carlo simulation of FinFET and FDSOI devices with accurate quantum correction

F.M. Bufler · L. Smith

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Abstract The performance of FinFET and FDSOI devices is compared by 3D Monte Carlo simulation using an enhanced quantum correction scheme. This scheme has two new features: (i) the quantum correction is extracted from a 2D cross-section of the 3D device and (ii) in addition to using a modified oxide permittivity and a modified work function in subthreshold, the work function is ramped above threshold to a different value in the on-state. This approach improves the accuracy of the quantum-correction for multi-gate devices and is shown to accurately reproduce 3D density-gradient simulation also at short channel lengths. 15 nm FDSOI device performance with thin box and back-gate bias is found to be competitive: compared to a FinFET with (110)/(110) sidewall/channel orientation, the on-current for *N*-type devices is 25 % higher and the off-current is only increased by a factor of 2.5.

Keywords 3D Monte Carlo · Quantum effects · Fully-depleted SOI devices · FinFET

1 Introduction

In order to keep the short-channel effect under control, for continued gate-length scaling bulk MOSFETs have to be replaced by thin-film or multi-gate devices [1]. Fully-depleted

SOI (FDSOI) devices with a thin buried-oxide (BOX) and back-gate bias [2] and FinFETs [3] are the most promising candidates. One crucial question is how far FDSOI technology can still compete with FinFETs upon further scaling. It is the purpose of this work to investigate this issue by advanced TCAD simulation where all relevant effects are taken into account on a physical basis.

Relevant effects comprise the crystallographic orientation dependence of the surface mobility as well as of the nonlinear longitudinal drift velocity, quasi-ballistic velocity overshoot, three-dimensional (3D) arbitrarily shaped device geometry and size quantization. 3D Monte Carlo simulation on unstructured meshes is an adequate tool for this situation. Thanks to the self-consistent single-particle approach and parallelization it has become fast enough for TCAD applications [4].

An aspect of special concern is the incorporation of quantum effects into Monte Carlo simulation. Three approaches are being used in literature: subband models based on solutions of the Schrödinger equation on (d-1)-dimensional slices of d-dimensional device structures [5–9], effective potential methods [10–13] and approaches which extract modified effective oxide thickness and workfunction from a previous quantum simulation [14, 15]. From a TCAD perspective, a quantum approach must in particular meet three requirements: (i) the orientation dependence of the surface mobility must be captured, (ii) the mobility degradation due to surface roughness must be included and (iii) it must be possible to treat arbitrary device geometries. Although the subband models feature the orientation- and roughness-dependence of surface mobility [16], the whole device cannot be completely quantized for general and realistic geometries, which is especially true for 3D devices with source/drain contacts from above. In general, this necessitates the introduction of a quantum box in real- and energy-

F.M. Bufler
Synopsys Schweiz GmbH, 8050 Zürich, Switzerland

F.M. Bufler (✉)
Institut für Integrierte Systeme, ETH Zürich, 8092 Zürich,
Switzerland
e-mail: bufler@iis.ee.ethz.ch

L. Smith
Synopsys Inc., Mountain View, CA 94043, USA

space. At the boundary of this box energy conservation during the mapping from a bulk- into a subband-electron is only approximately satisfied [5]. This raises the question how results depend on the choice of the quantum box. Therefore these elaborate schemes are only reliable on ideal structures such as a rectangular double-gate device [7–9]. Effective potential approaches can be applied to general geometries, but due to the vanishing carrier density at the gate-oxide interface it is difficult to consider the mobility reduction with a combination of diffusive and specular surface scattering and it is therefore often neglected [12, 13]; an effective-field dependent surface scattering rate can consider surface roughness, but has no automatic orientation dependence [10, 11]. Modifying the effective oxide thickness and the workfunction is a pragmatic choice, but it combines the orientation-dependence of surface mobility due to energy- and parallel-momentum conservation of specular surface scattering [4] with the ability to accurately capture the electrostatic quantum effect.

We therefore adopt this pragmatic approach and generalize it in order to retain the accuracy of the quantum-correction also for non-planar devices such as FinFETs. Moreover, we show that the quantum-correction can be extracted from a 2D cross-section of the 3D device and remains accurate also for short-channel devices, thus using in a multi-scale approach long-channel results in short-channel device simulation.

This quantum-corrected 3D Monte Carlo approach is then applied to compare the performance of FDSOI devices and FinFETs at a gate length of 15 nm. Stress is not considered in this work in order to allow for a meaningful comparison between single-gate and multi-gate devices upon scaling.

2 Monte Carlo model

In this work, analytical band structure descriptions are used. For electrons, a two-band model with anisotropic non-parabolicity is used which compares favorably to corresponding pseudopotential device simulations [17]. For holes, we use a six-band $\mathbf{k} \cdot \mathbf{p}$ band structure [18]. Phonon, ionized impurity and surface roughness scattering are considered. For electron-phonon scattering, intervalley scattering and elastic acoustic intravalley scattering with coupling constants according to Jacoboni and Reggiani [19] are adopted. Only the acoustic deformation potential $\mathcal{E} = 8.52$ eV is modified in order to match the experimental velocity-field characteristics with a band structure which deviates from the standard nonparabolic ellipsoidal model as described above. Hole-phonon scattering includes elastic acoustic and optical phonons with parameter values reported in Ref. [20]. Ionized impurity scattering is modeled

according to Brooks and Herring (see Ref. [19]), but the screening length is computed with degenerate statistics and carrier temperatures and the rate is calibrated with a doping-dependent prefactor to compensate the mobility overestimation. Surface roughness scattering consists of a combination of 15 % diffusive and 85 % specular scattering. Specular scattering is governed by conservation of energy and parallel-momentum, and for anisotropic band structures this leads to the orientation dependence of surface mobility, see Fig. 1 of Ref. [4] and the corresponding discussion. Note that the diffusive percentage of 15 % is *not* changed as a function of crystallographic surface orientation; the orientation dependence comes automatically from energy and parallel-momentum conservation in anisotropic band structures and this model reproduces without any adjustment (Fig. 2 of Ref. [4]) the measured 20 % decrease and 100 % mobility increase in *N*-type and *P*-type FinFETs [3, 21], respectively, when the (100)/(100) sidewall/channel configuration is rotated by 45° around the wafer normal.

3 Quantum correction

Quantization increases the threshold voltage and pushes the charge centroid away from the gate-oxide interface [14]. It is possible to reproduce density-gradient transfer characteristics in planar bulk MOSFETs by classical drift-diffusion simulation where the threshold voltage shift is accommodated by changing the workfunction and the increased effective oxide thickness is translated into a reduced effective oxide permittivity [15]. The situation changes in 3D since the cross-section of the FinFET in Fig. 1 has a different shape compared to the mostly planar FDSOI in Fig. 2

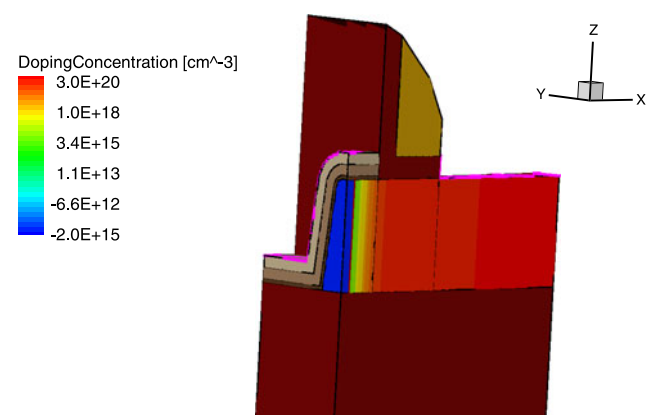


Fig. 1 Geometry and doping profile of the FinFET device. The gate length is $L_G = 15$ nm, the fin height $H = 20$ nm and the fin width at the top $W = 5$ nm before corner rounding. The thickness of the buried oxide is $t_{\text{box}} = 145$ nm and the sidewall angle is 7°. The gate oxide with 0.7 nm interfacial oxide and 2 nm HfO_2 has an EOT of about 1.05 nm

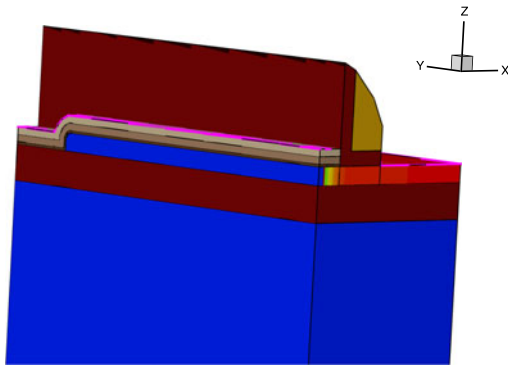


Fig. 2 Geometry and doping profile of the FDSOI device. The gate length is $L_G = 15$ nm, the silicon film thickness $t_{Si} = 5$ nm and the width $W = 200$ nm. The thickness of the buried oxide is $t_{BOX} = 10$ nm. The gate oxide is the same as for the FinFET in Fig. 1 with an EOT of about 1.05 nm. The doping of silicon below the BOX is as in the channel $1 \times 10^{15} \text{ cm}^{-3}$

and can involve different crystallographic surface orientations. Furthermore, the computational burden of extracting the quantum correction from simulations of the complete device structure becomes significantly larger in 3D.

We therefore propose an enhanced quantum-correction scheme. It is based on a 2D cross-section which strongly improves the computational efficiency. In addition, the effective workfunction of the gate contact is allowed to vary above the threshold voltage as a function of the gate voltage; this increases the accuracy of the results especially for non-planar devices such as FinFETs. As a third advantage, our new approach will permit to replace the density-gradient method as quantum reference by Schrödinger-Poisson solutions on the 2D cross-section; this will improve the physical accuracy without introducing additional computational issues that might arise in a full 3D device structure.

In Fig. 3, the different steps of the new quantum-correction scheme are shown by plotting the electron sheet density (normalized by the perimeter of the gate contact which is approximated by $(2H + W)$) in the 2D cross-section (compare Fig. 7 in Appendix) as a function of the gate voltage. First, the effective permittivity ϵ_{ox} is computed in the on-state from the difference in charge centroid between density-gradient and classical simulation. This is done separately for the directions perpendicular to the top side and the sidewall of the fin, using different quantization masses for the density-gradient simulation arising from different crystallographic surface orientations. In the second step, the threshold voltage shift is extracted in the subthreshold regime and translated into a new value Wf_1 for the workfunction which additionally compensates for small threshold voltage shifts that may arise from the new value of ϵ_{ox} . So far, this corresponds to the approach of Ref. [15], and it can be seen that the density-gradient results are already well reproduced in the case of the FDSOI device. However, the

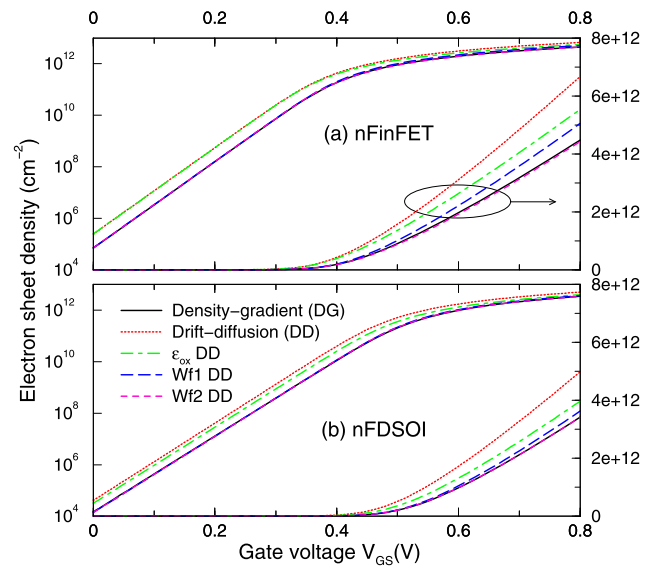


Fig. 3 Electron sheet density in logarithmic (left axis) and linear (right axis) scale of a 2D slice in the yz -plane of Figs. 1 and 2, obtained from a vertical cut in the middle of the channel of (a) the FinFET and (b) the FDSOI device. Compared are density-gradient simulations with classical results without correction, corrected permittivity ϵ_{ox} , additionally corrected workfunction Wf_1 in subthreshold and additional linear ramp of the workfunction above threshold to the value Wf_2 in the on-state. The y -axis and the z -axis in Figs. 1 and 2 point in (110) and (001) direction, respectively

electron charge in the FinFET is still overestimated above threshold. Therefore, a second value Wf_2 is extracted in the on-state and the workfunction is linearly ramped from Wf_1 at the threshold voltage to Wf_2 in the on-state. This scheme perfectly reproduces the density-gradient curve.

The decisive question is, of course, if this scheme remains also accurate upon scaling, i.e. if the values for ϵ_{ox} , Wf_1 and Wf_2 extracted from the 2D cross-section are sufficient to reproduce density-gradient transfer-characteristics at short gate lengths. This is investigated in Fig. 4 for FinFETs with gate lengths of 100 nm and 15 nm. The agreement between quantum-corrected drift-diffusion and density-gradient simulations turns out to be quite good. Since we are dealing with quantization normal to the transport direction, a corresponding correction should be expected not to depend on gate length which is confirmed by this comparison.

4 Monte Carlo simulation of short-channel FinFET and FDSOI devices

In this section, the short-channel performance of FinFET and FDSOI devices is compared by Monte Carlo simulation using the quantum-correction scheme of the previous section. Figure 5 shows the transfer characteristics of P -type and N -type FinFET and FDSOI devices for both

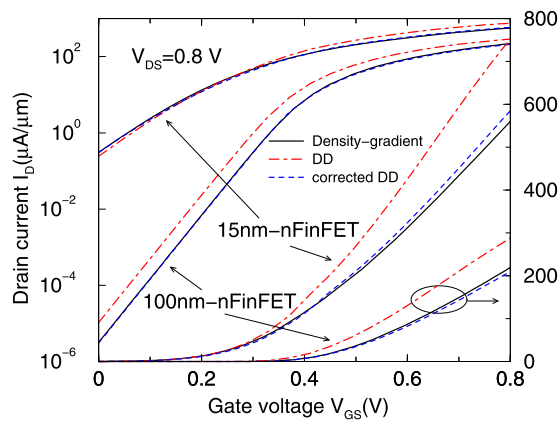


Fig. 4 3D density-gradient, drift-diffusion and quantum-corrected drift-diffusion simulation of the transfer characteristics in a 15 nm and a 100 nm FinFET in logarithmic (*left axis*) and linear (*right axis*) scale. (110)/⟨110⟩ sidewall/channel orientation is used

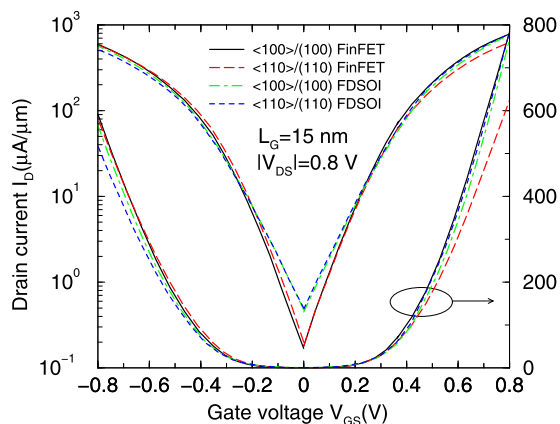


Fig. 5 3D quantum-corrected Monte Carlo simulation of the transfer characteristics in *P*-type and *N*-type 15 nm FinFET and FDSOI devices with (110)/⟨110⟩ and (100)/⟨100⟩ sidewall/channel orientations, respectively, in logarithmic (*left axis*) and linear (*right axis*) scale

(110)/⟨110⟩ and (100)/⟨100⟩ sidewall/channel orientations at a gate length of 15 nm, i.e. the two device orientations differ by a rotation by 45 degrees around the (001) wafer normal (also for FDSOI devices, we refer to the sidewall surface in analogy to FinFETs although this surface has negligible influence in this case). This means that in the case of the FDSOI devices essentially only the channel direction is affected by the 45° rotation the relevant surface always being the (001) top-side surface. In contrast, for FinFETs also the relevant sidewall direction is different in the two configurations. The original physical workfunction W_f has been roughly adjusted for *N*-type and *P*-type devices such that the threshold voltage is around 0.15 V at a gate length of 15 nm. Note that the drift-diffusion simulation in Fig. 4 and the Monte Carlo simulation in Fig. 5 show—for the same quantum-correction—a different off-current for the *N*-type 15 nm-FinFET. The reason is that drift-diffusion simula-

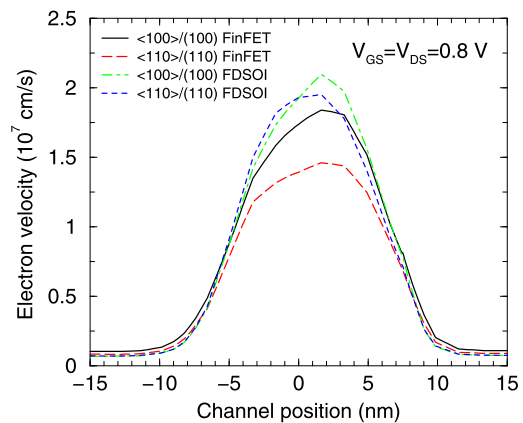


Fig. 6 Electron drift velocity along the channel obtained via averaging with the electron density over the device cross-section in the on-state

tion increasingly underestimates the threshold voltage for decreasing gate length as already observed previously (see Fig. 6 of Ref. [22]) which consequently leads to a too high drift-diffusion off-current.

It can be seen in Fig. 5 that the off-current for FinFETs is indeed smaller than for FDSOI devices. This is expected since more gates increase the electrostatic channel control, but due to a thin BOX and the applied back-gate bias this difference is not very large. The on-currents have in general a similar level, but for the (110)/⟨110⟩ sidewall/channel orientation the *N*-type FDSOI device has a 25 % higher performance than FinFET (as noted above the FDSOI devices have always the (001) top-side surface). The crystallographic orientation-dependence can be related to the velocity profiles in the channel which for *N*-type devices are displayed in Fig. 6. For FinFETs, the electron velocity in the source-side of the 15 nm-channel is larger for the (100)/⟨100⟩ sidewall/channel orientation and the situation is opposite for FDSOI devices. In both cases, this corresponds to the order of the on-currents (the absolute values are also determined by the electron sheet density which is larger for FinFETs, compare Fig. 3). Quasi-ballistic transport is prominent since in a large part of the channel the electrons have an average velocity higher than the saturation velocity, but not in the important region after the beginning of the channel.

For a more detailed physical interpretation of the crystallographic orientation dependence, we specify in Table 1 the on-currents both for the gate length of 15 nm and for the larger gate length of 100 nm. The situation is easier to understand in the case of FDSOI devices where essentially only the (001) surface is relevant. In the long-channel FDSOI devices, the on-current is almost the same for both channel directions because the surface mobility is isotropic for the (001) surface. In the short-channel devices, nonlinear transport leads to a higher on-current for ⟨110⟩ channel direction in *N*-type FDSOI devices and a higher on-current for ⟨100⟩

Table 1 3D Monte Carlo on-currents in 15 nm and 100 nm *N*-type and *P*-type devices with (100)/⟨100⟩ and (110)/⟨110⟩ sidewall/channel orientations (in units of $\mu\text{A}/\mu\text{m}$). The third direction, i.e. the wafer normal, points in both configurations in (001) direction, which in particular means that for FDSOI devices always only the (001) surface orientation is relevant. The differences between the two configurations arise for FDSOI devices therefore only from the different channel orientations

Device type	15 nm- <i>N</i>	100 nm- <i>N</i>	15 nm- <i>P</i>	100 nm- <i>P</i>
100 FinFET	783	273	592	143
110 FinFET	625	221	581	188
100 FDSOI	767	182	566	67
110 FDSOI	785	182	518	65

channel direction in *P*-type FDSOI devices because holes have in contrast to electrons a higher bulk drift velocity for ⟨100⟩ transport direction in the nonlinear regime (see Fig. 1 of Ref. [23]). The 100 nm-FinFETs are also governed by the surface mobility. Here, the dominant sidewall surface leads to a higher hole current for (110) sidewall orientation and a higher electron current for (100) sidewall orientation in agreement with corresponding effective mobilities [4]. For 15 nm-FinFETs, the combined influence of different surface orientations on nonlinear and quasi-ballistic transport in different channel directions is difficult to quantify. In the case of *P*-type FinFETs, the situation is reversed relative to the 100 nm devices and the advantageous nonlinear and quasi-ballistic transport in ⟨100⟩ direction overcompensates the negative influence of the (100) sidewall surface orientation as already reported previously [23]. For *N*-type 15 nm-FinFETs, the situation remains the same as for 100 nm devices, possibly due to a larger contribution of quasi-ballistic transport, which in contrast to nonlinear electron transport is advantageous for ⟨100⟩ transport direction [24], or the still present influence of the favorable (100) sidewall surface orientation.

Finally, it should be noted that the present study refers to a specific choice of geometry and doping. The quantitative conclusions will change upon modifications; e.g. a wider fin will degrade the subthreshold slope of the FinFET and heavy doping below the thin BOX can improve FDSOI performance.

5 Conclusions

Short-channel performance of FinFET and FDSOI devices has been compared by 3D Monte Carlo simulation with a new accurate quantum-correction scheme. In the future, this scheme will also permit efficient quantum-correction based on 2D Schrödinger-Poisson solutions and therefore to enhance the accuracy especially for new channel materials.

Thanks to thin BOX and back-gate bias, FDSOI devices show comparable performance as FinFETs at a gate length of 15 nm. A definitive comparison will also need to consider the different possibilities for introducing stressors in FinFETs and FDSOI devices which was beyond the scope of this work.

Acknowledgements We would like to thank A. Erlebach and F.O. Heinz for useful discussions.

Appendix: On the quantum correction method

In this appendix, we present more details on our quantum correction method. The quantum-mechanical reference in this work is the density-gradient approach. In the context of the quantum correction, the advantage of density-gradient simulation is that it is also possible to simulate the complete 3D device structure which allows to verify the accuracy of the quantum-corrected DD simulations by comparing the corresponding transfer characteristics at different gate lengths as is done in Fig. 4. The parameter of density-gradient simulation is the quantization mass. This mass changes with the crystallographic orientation of the gate interface. In the present work, values for (100), (110) and (111) surface orientations are considered and during device simulation always the value of the nearest surface is used. For example, the electron (hole) quantization masses for (110) and (100) surface orientations are 0.32 (0.91) and 0.92 (0.26) in units of the free electron mass, respectively (for electrons, always the quantization mass of the valley with the largest mass in surface direction is taken since it dominates the electron density).

The new values for effective oxide thickness and work-function used as a quantum correction are extracted from 2D device simulations on a cross-section of the 3D device which is shown for the FinFET in Fig. 7. The interfacial oxide is divided into different regions for the top side and the two sidewalls and two different values for ϵ_{ox} are used as resulting from the different crystallographic orientations. In the case of the *N*-type (*P*-type) FinFETs with (110) sidewall and (001) top side, the effective permittivity values are 2.83 (3.01) and 2.94 (2.68) in units of the vacuum permittivity instead of the original value of 3.9. In case of discrepancies in the sheet densities between density-gradient and quantum correction, a division into more regions could be considered, but the present results as in Fig. 3 suggest that this will probably not be necessary.

When replacing density-gradient simulation by 2D Schrödinger-Poisson solutions on the cross-section in Fig. 7 as the quantum-mechanical reference, 3D MC simulation will still not explicitly use subbands, of course. However, the corresponding correction for threshold voltage and channel

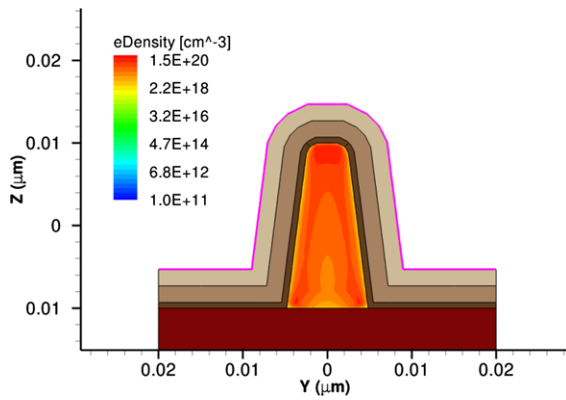


Fig. 7 Electron density at a gate voltage of $V_{GS}=0.8$ V according to 2D density-gradient simulation. The simulated structure was obtained by a vertical cut through the middle of the FinFET in Fig. 1. The gate stack consists of interfacial oxide, HfO_2 , titanium nitride and the gate contact line

charge will accurately be taken into account and the comparison between density-gradient and quantum-corrected DD in Fig. 4 shows that the density profile itself is not important. The crystallographic orientation dependence of the surface mobility is not due to quantization, but originates from the boundary condition in the presence of a gate interface and is therefore captured both in semiclassical transport (via conservation of energy and parallel-momentum) and in quantum transport (via e.g. vanishing wave functions at the gate interface) [4].

Strain changes subband structure and population resulting from Schrödinger-Poisson solutions, but the corresponding change in threshold voltage and channel charge is captured in our quantum correction approach analogously to the unstrained case. Concerning surface mobility, the strain-induced change in the bulk band structure changes the effect of energy and parallel-momentum conservation leading to a similar stress response as subband models (see Fig. 3 of Ref. [4]).

References

- Colinge, J.P.: Multi-gate SOI MOSFETs. *Microelectron. Eng.* **84**, 2071–2076 (2007)
- Planes, N., Weber, O., Barral, V., Haendler, S., Noblet, D., Croain, D., Bocat, M., Sassoulas, P.-O., Federspiel, X., Cros, A., Bajolet, A., Richard, E., Dumont, B., Perreau, P., Petit, D., Golanski, D., Fenouillet-Béranger, C., Guillot, N., Rafik, M., Huard, V., Puget, S., Montagner, X., Jaud, M.-A., Rozeau, O., Saxod, O., Wacquant, F., Monsieur, F., Barge, D., Pinzelli, L., Mellier, M., Boeuf, F., Arnaud, F., Haond, M.: 28nm FDSOI technology platform for high-speed low-voltage digital applications. In: *Symp. on VLSI Tech.*, Honolulu, Hawaii, June 2012, pp. 133–134 (2012)
- Basker, V.S., Standaert, T., Kawasaki, H., Yeh, C.-C., Maitra, K., Yamashita, T., Faltermeyer, J., Adhikari, H., Jagannathan, H., Wang, J., Sunamura, H., Kanakasabapathy, S., Schmitz, S., Cummings, J., Inada, A., Lin, C.-H., Kulkarni, P., Zhu, Y., Kuss, J., Yamamoto, T., Kumar, A., Wahl, J., Yagishita, A., Edge, L.F., Kim, R.H., McLellan, E., Holmes, S.J., Johnson, R.C., Levin, T., Demarest, J., Hane, M., Takayanagi, M., Colburn, M., Paruchuri, V.K., Miller, R.J., Bu, H., Doris, B., McHerron, D., Leobandung, E., O’Neill, J.: A $0.063 \mu\text{m}^2$ FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch. In: *Symp. on VLSI Tech.*, Honolulu, Hawaii, June 2010, pp. 19–20 (2010)
- Bufler, F.M., Heinz, F.O., Smith, L.: Efficient 3D Monte Carlo simulation of orientation and stress effects in FinFETs. In: *Proc. SISPAD*, Glasgow, UK, September 2013, pp. 172–175 (2013)
- Fischetti, M.V., Laux, S.E.: Monte Carlo study of electron transport in silicon inversion layers. *Phys. Rev. B* **48**(4), 2244–2274 (1993)
- Jungemann, C., Emunds, A., Engl, W.L.: Simulation of linear and nonlinear electron transport in homogeneous silicon inversion layers. *Solid-State Electron.* **36**, 1529–1540 (1993)
- Saint-Martin, J., Bournel, A., Monsef, F., Chassat, C., Dollfus, P.: Multi sub-band Monte Carlo simulation of an ultra-thin double gate MOSFET with 2D electron gas. *Semicond. Sci. Technol.* **21**, L29–L31 (2006)
- Lucci, L., Palestri, P., Esseni, D., Bergagnini, L., Selmi, L.: Monte Carlo study of transport, quantization, and electron-gas degeneration in ultrathin SOI n-MOSFETs. *IEEE Trans. Electron Devices* **54**, 1156–1164 (2007)
- Sampedro, C., Gámiz, F., Godoy, A., Valin, R., Garcia-Loureiro, A., Ruiz, F.G.: Multi-subband Monte Carlo study of device orientation effects in ultra-short channel DGSOI. *Solid-State Electron.* **54**, 131–136 (2010)
- Winstead, B., Ravaioli, U.: A quantum correction based on Schrödinger equation applied to Monte Carlo device simulation. *IEEE Trans. Electron Devices* **50**, 440–446 (2003)
- Palestri, P., Eminent, S., Esseni, D., Fiegna, C., Sangiorgi, E., Selmi, L.: An improved semi-classical Monte-Carlo approach for nano-scale MOSFET simulation. *Solid-State Electron.* **49**, 727–732 (2005)
- Ghetti, A., Carnevale, G., Rideau, D.: Coupled mechanical and 3-D Monte Carlo simulation of silicon nanowire MOSFETs. *IEEE Trans. Nanotechnol.* **6**, 659–666 (2007)
- Mori, T., Azuma, Y., Tsuchiya, H., Miyoshi, T.: Comparative study on drive current of III–V semiconductor, Ge, and Si channel n-MOSFETs based on quantum-corrected Monte Carlo simulation. *IEEE Trans. Nanotechnol.* **7**, 237–241 (2008)
- Hudé, R., Villanueva, D., Clerc, R., Ghibaudo, G., Robillart, E.: A simple approach to account for the impact of quantum confinement on the charge in semiclassical Monte Carlo simulations of bulk nMOSFETs. In: *Proc. ULIS*, Bologna, Italy, April 2005, pp. 159–162 (2005)
- Bufler, F.M., Hudé, R., Erlebach, A.: On a simple and accurate quantum correction for Monte Carlo simulation. *J. Comput. Electron.* **5**, 467–469 (2006)
- Pham, A.T., Jungemann, C., Meinerzhagen, B.: Microscopic modeling of hole inversion layer mobility in unstrained and uniaxially stressed Si on arbitrarily oriented substrates. *Solid-State Electron.* **52**, 1437–1442 (2008)
- Bufler, F.M., Heinz, F.O., Tsibizov, A., Oulmane, M.: Simulation of (110) nMOSFETs with a tensile strained cap layer. *ECS Trans.* **16**(10), 91–100 (2008)
- Bufler, F.M., Erlebach, A., Oulmane, M.: Hole mobility model with silicon inversion layer symmetry and stress-dependent piezococonductance coefficients. *IEEE Electron Device Lett.* **30**, 996–998 (2009)
- Jacoboni, C., Reggiani, L.: The Monte Carlo method for the solution of charge transport in semiconductors with application to covalent materials. *Rev. Mod. Phys.* **55**, 645–705 (1983)
- Bufler, F.M., Meinerzhagen, B.: Hole transport in strained $\text{Si}_{1-x}\text{Ge}_x$ alloys on $\text{Si}_{1-y}\text{Ge}_y$ substrates. *J. Appl. Phys.* **84**, 5597–5602 (1998)

21. Akarvardar, K., Young, C.D., Baykan, M.O., Ok, I., Ngai, T., Ang, K.-W., Rodgers, M.P., Gausepohl, S., Majhi, P., Hobbs, C., Kirsch, P.D., Jammy, R.: Impact of fin doping and gate stack on FinFET (110) and (100) electron and hole mobilities. *IEEE Electron Device Lett.* **33**, 351–353 (2012)
22. Granzner, R., Polyakov, V.M., Schwierz, F., Kittler, M., Doll, T.: On the suitability of DD and HD models for the simulation of nanometer double-gate MOSFETs. *Physica E* **19**, 33–38 (2003)
23. Bufler, F.M., Erlebach, A.: Monte Carlo simulation of the performance dependence on surface and channel orientation in scaled pFinFETs. In: *Proc. ESSDERC*, Montreux, Switzerland, September 2006, pp. 174–177 (2006)
24. Bufler, F.M., Keith, S., Meinerzhagen, B.: Anisotropic ballistic in-plane transport of electrons in strained Si. In: *Proc. SISPAD*, Leuven, Belgium, September 1998, pp. 239–242 (1998)