Modelling and ZVS control of an isolated three-phase bidirectional AC-DC converter

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Modelling and ZVS Control of an Isolated Three-Phase Bidirectional AC-DC Converter

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Keywords

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Abstract

This paper presents an isolated three-phase bidirectional AC-DC converter with a novel modulation strategy that enables Zero-Voltage-Switching (ZVS) for all switches over the whole AC line period. The AC-DC converter allows the direct coupling of a three-phase AC system with a DC port applying a single high-frequency transformer. A novel modelling approach for the power flows and the derivation of the control variables under ZVS conditions are provided. The design of components including loss models and simulation results of a $11\,\text{kW}$ electric vehicle battery charger to connect to the $230\,\text{V}_{\text{rms}}$, $50\,\text{Hz}$ mains considering a battery voltage range of $380\,\text{V}$ to $540\,\text{V}$ validate the theoretical analysis.

Introduction

Three-phase isolated AC-DC converters are widely used for applications like charging (hybrid-)electric vehicles, interfacing storage batteries (e.g. for uninterruptible power supplies) or supplying energy from large photovoltaic systems to the medium-voltage grid. Some applications require bidirectional power flow capability, e.g. for implementing Vehicle-2-Grid (V2G) concepts or grid battery storage systems.
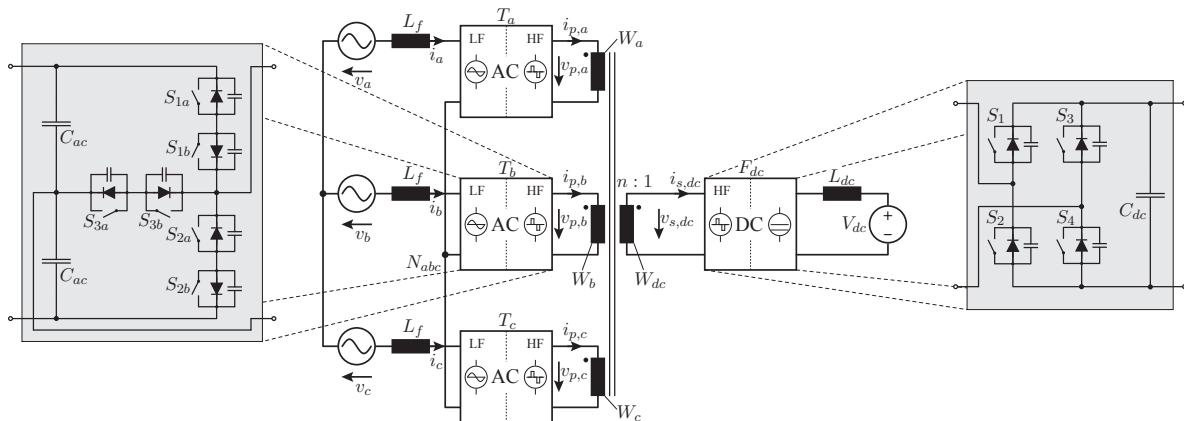

Figure 1: Isolated three-phase bidirectional AC-DC converter based on a multi-port approach with T-type circuits T_a, T_b, T_c on the AC side applying bidirectional switches and a full-bridge F_{dc} with unidirectional switches on the DC side. The three AC ports and the DC port are magnetically coupled via a four-winding transformer.

Conventional bidirectional two-stage solutions consist often of a three-phase 2-level or 3-level PWM boost rectifier (e.g. NPC, T-Type) and a subsequent high-frequency isolated DC-DC converter such as Dual Half-Bridge (DHB), Dual Active (Full-)Bridge (DAB) or resonant DC-DC converters. Single-stage isolated three-phase AC-DC converters comprise for instance the Cuk-derived unidirectional buck-boost converter [1, 2], the three-phase AC-DC DAB [3] and the three-phase soft-switched AC-DC converter consisting of a cycloconverter and a voltage-source converter [4].

Another approach for isolated three-phase bidirectional AC-DC power conversion based on a multi-port converter has been presented in [5]. Compared to state-of-the-art three-phase systems, a multi-port converter is stackable and hence, single converter modules can be connected in series or parallel at the input/output ports for medium- or high-voltage applications. Moreover, a multi-port system exhibits the capability to couple several AC and DC systems (e.g. AC grids and DC energy sources/storages) directly via a single transformer structure.

In this paper, for the isolated three-phase bidirectional AC-DC converter based on a multi-port approach proposed in [5] and shown in Fig. 1, a novel Zero-Voltage-Switching (ZVS) modulation strategy and a novel modelling approach for the power flows are presented. The proposed modulation strategy ensures ZVS conditions for all switches over the whole AC line period.

In the following, first the converter topology, the operating principle with the modulation and control strategy under ZVS conditions and the calculation of the control variables are shown. Then, the mathematical analysis of the power flows in the converter is given. Afterwards, the design of a prototype system including loss models is presented. Finally, simulation results verify the theoretical analysis.

Converter Topology

First, the converter topology including the applied high-frequency transformer is presented. Thereafter, an equivalent circuit of the converter is derived.

Fig. 1 shows the considered isolated three-phase bidirectional AC-DC converter based on a multi-port approach with three AC ports and one DC port. The T-type circuits T_a, T_b, T_c connect to the three-phase AC system with phases a, b, c and the star point N_{abc}. Furthermore, a full-bridge F_{dc} is connected to the DC port. The T-type circuits and the full-bridge are magnetically coupled via a four-winding transformer. The T-type circuits consist of half-bridges with a clamping switch using bidirectional switches whereas the full-bridge applies unidirectional switches. The switching devices are MOSFETs which are suitable when ZVS conditions are met for every switching action. Bidirectional switches are realized by an anti-serial connection of two MOSFETs with common source potential.

The T-type circuits and the full-bridge apply high-frequency (HF) square-wave voltages with or without clamping interval to the corresponding windings with a given phase angle in relation to a chosen reference. The switching frequency is chosen to be well above the frequency of the three-phase AC system and the capacitors assumed to be large enough, so that the amplitudes of the generated square-wave voltages can be considered as constant during one switching cycle.

The three AC side windings W_a, W_b, W_c of the transformer are wound on separate legs as shown in Fig. 2, such that the winding fluxes, respectively the applied voltages, are added. The DC side winding W_{dc} is wound around the AC winding legs where the space in between defines the size of the leakage inductance. The magnetizing inductance is neglected, so that all of the windings conduct the same current referred to a specific winding. Electrically, all windings are connected in series. An equivalent circuit is given in Fig. 3 where the AC side referred leakage inductance L_σ is drawn.

As discussed in [5], by applying a four-winding transformer with separated AC winding legs, the AC side applied voltages are added, which enables the use of the nearly constant sum of the absolute values of the phase voltages for controlling the converter. The combination of the three AC ports with its voltage sum $v_{p,s}$ can be represented approximately as a DC port to describe the AC-DC converter in terms of the well-known DAB [6]. Analogously to the DAB, the power transfer between the three AC ports and the DC port is controlled by phase-shifts.
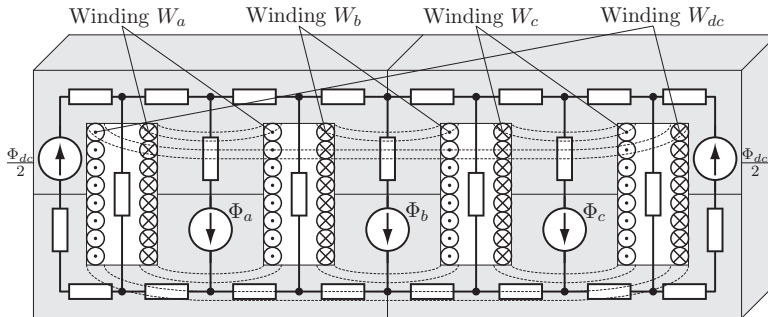

Figure 2: Four-winding transformer consisting of two sets of E-cores and its reluctance model with winding flux sources $\Phi_a, \Phi_b, \Phi_c, \Phi_{dc}/2$. The AC side windings W_a, W_b, W_c are wound on the inner legs with the DC side winding W_{dc} wound around them. The space between AC windings and DC winding defines the size of the leakage inductance L_σ.
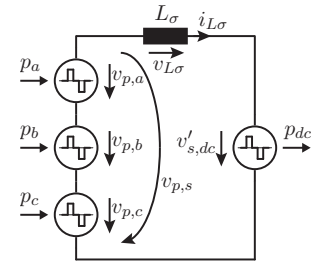
Figure 3: AC side referred equivalent circuit of the converter in Fig. 1 for representing phase-shift control with leakage inductance L_σ.

Operating Principle

Like the three-port DC-DC converters discussed in [7–9], the considered three-phase AC-DC converter is operated by phase-shift control. The clamping intervals and the phase-shifts are the control variables. The leakage inductance L_σ of the transformer acts as decoupling and energy transfer element between the square-wave voltages (see Fig. 3). During one half-cycle of the AC phase voltage, two of the switches in the T-type circuit are constantly turned on. These are for example S_{1b} and S_{2b} for the positive and S_{1a} and S_{2a} for the negative half-wave in circuit T_b. In the following, the modulation strategy to achieve ZVS for all switches over the whole AC line period is presented. Thereafter, the control variables are determined by minimizing the transformer leakage inductance RMS current. Finally, a sequential calculation scheme is presented to find the control variables analytically.

Modulation and Control under ZVS Conditions

In the following, the modulation is derived for positive instantaneous power flows from the AC ports. To allow power flowing back into the AC grid also for reactive power compensation at the AC ports, the modulation scheme has to be slightly adapted.

For simplification, the phase voltages are sorted by their absolute values in descending order and accordingly named by $v_{ph1}, v_{ph2}, v_{ph3}$, such that the control variables $\delta_{ph1}, \delta_{ph2}, \delta_{ph3}, \delta_{dc}, \phi_{ph1}, \phi_{ph2}, \phi_{ph3}, \phi_{dc}$ only have to be obtained in a $30°$ sector of the AC line voltage (see Fig. 4). The solutions are then assigned to the corresponding phase in each sector.

By applying a positive or negative voltage $v_{L\sigma}$ across the leakage inductance L_σ (see Fig. 3), the current waveform $i_{L\sigma}$ can be controlled during the switching cycle T_s as shown in Fig. 4. For positive $v_{L\sigma}$, in case of interval $[\tau_2, \tau_5]$ where positive voltages across the AC side windings are applied, $i_{L\sigma}$ increases. In interval $[\tau_5, \tau_6]$, $v_{L\sigma}$ is zero, so that $i_{L\sigma}$ stays constant. For negative voltage $v_{L\sigma}$ in interval $[\tau_6, \tau_7]$ where positive voltage across the DC side winding is applied, $i_{L\sigma}$ decreases.

To ensure ZVS conditions, the turn-off current in the MOSFET has to be large enough to charge/discharge the drain-source capacitances. Therefore, in interval $[\tau_2, \tau_7]$, the current $i_{L\sigma}$ has to be positive, whereas negative in interval $[\tau_8, \tau_{13}]$ as shown by the dots in Fig. 4 for ZVS on AC and DC side. This is achieved by defining a current reversal interval where the maximum available voltage is applied across the transformer leakage inductance L_σ as depicted in Fig. 4 by the grey colored areas. During time interval $[\tau_1, \tau_2]$ the port voltages $v_{p,ph1}, v_{p,ph2}, v_{p,ph3}$ are positive whereas $v'_{s,dc}$ is negative and vice versa during $[\tau_7, \tau_8]$. The current reversal interval should be large enough to increase/decrease the current to the minimum
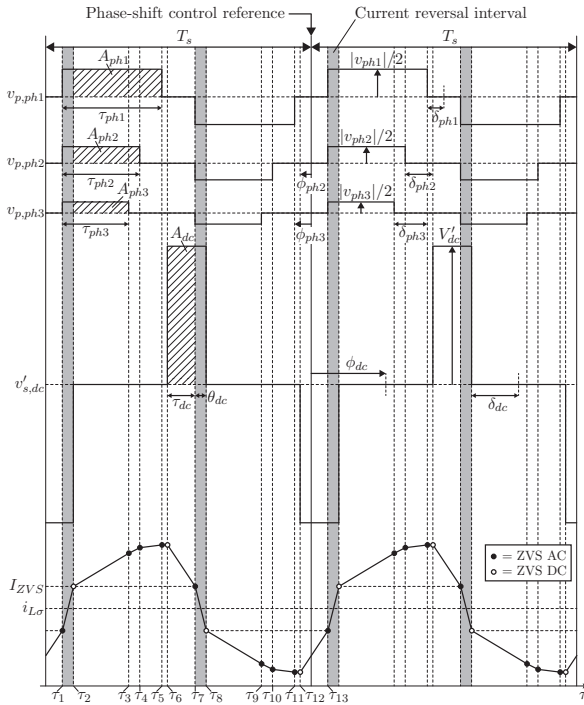

Figure 4: Square-wave voltages $v_{p,ph1}, v_{p,ph2}, v_{p,ph3}$ applied to the AC windings, the AC side referred square-wave voltage $v'_{s,dc}$ applied to the DC winding and the resulting transformer leakage inductance current $i_{L\sigma}$ in case of $|v_{ph1}| > |v_{ph2}| > |v_{ph3}|$ in AC-to-DC operation over two switching cycles T_s.
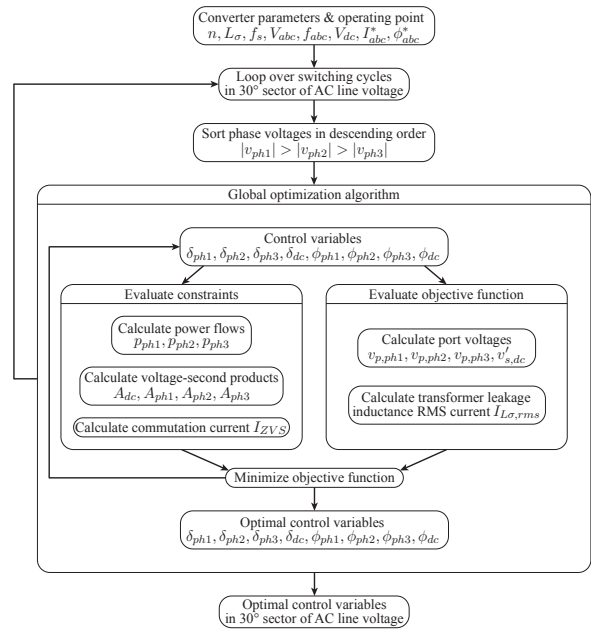
Figure 5: Visualization of the optimization procedure to find optimal control variables by minimizing the transformer leakage inductance RMS current $I_{L\sigma,rms}$ subject to power flow and ZVS constraints. I^*_{abc}, ϕ^*_{abc} represent the reference values (RMS current and phase angle) for the AC currents. For PFC operation $\phi^*_{abc} = 0$.

commutation current needed for ZVS. Simultaneously, this interval should not be too large, because it does not contribute to active power transfer.

To guarantee ZVS for every switching transition, the current points $i_{L\sigma}(\tau_1)$ and $I_{ZVS} = i_{L\sigma}(\tau_2)$ are symmetrically aligned across zero. This is done by setting the voltage-second product of the DC port equal to the sum of the voltage-second products of the AC ports during the power transfer interval $[\tau_2, \tau_7]$ according to

$$A_{dc} = A_{ph1} + A_{ph2} + A_{ph3} \tag{1}$$

as shown by the shaded areas in Fig. 4. Since the sum of the absolute phase voltages varies with a six-pulse waveform, the primary referred DC voltage V'_{dc} should be always greater than its peak value (always boost operation).

Optimal Control Variables

The solutions of the clamping intervals $\delta_{ph1}, \delta_{ph2}, \delta_{ph3}, \delta_{dc}$ and the phase-shifts $\phi_{ph1}, \phi_{ph2}, \phi_{ph3}, \phi_{dc}$ (see Fig. 4) are numerically determined by minimizing the transformer leakage inductance RMS current $I_{L\sigma,rms}$ subject to power flow and ZVS constraints in order to minimize conduction losses. The optimization procedure is shown in Fig. 5. For every switching cycle $T_s = 2\pi/\omega_s$, the optimization routine calculates the optimal control variables. The optimization problem is stated as

$$\min_x \left[\frac{1}{T_s} \int_0^{T_s} i_{L\sigma}^2(x, \tau)\, d\tau \right] \text{ with respect to } x = \begin{bmatrix} \delta_{ph1} \\ \delta_{ph2} \\ \delta_{ph3} \\ \delta_{dc} \\ \phi_{ph1} \\ \phi_{ph2} \\ \phi_{ph3} \\ \phi_{dc} \end{bmatrix} \text{ with } x_{lb} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ -\pi \\ -\pi \\ -\pi \\ -\pi \end{bmatrix},\ x_{ub} = \begin{bmatrix} \pi/2 \\ \pi/2 \\ \pi/2 \\ \pi/2 \\ \pi \\ \pi \\ \pi \\ \pi \end{bmatrix} \tag{2}$$

where x denotes the vector of control variables which is restricted to lower and upper bounds x_{lb}, x_{ub} respectively. The first equality constraints are given by the AC side reference power flows $p_{ph1}^*, p_{ph2}^*, p_{ph3}^*$ according to

$$p_{ph1} = p_{ph1}^*,\quad p_{ph2} = p_{ph2}^*,\quad p_{ph3} = p_{ph3}^* \tag{3}$$

where the instantaneous powers $p_{ph1}, p_{ph2}, p_{ph3}$ are calculated as shown later (e.g. for phase a by (20) inserting (21), (22), (23)). The DC side power flow is then inherently given. Further constraints are

$$\phi_{ph1} = 0,\quad \phi_{ph2} = \delta_{ph2} - \delta_{ph1},\quad \phi_{ph3} = \delta_{ph3} - \delta_{ph1} \tag{4}$$

where phase 1 is defined as phase-shift control reference and ϕ_{ph2}, ϕ_{ph3} are written as functions of the AC side clamping intervals (see Fig. 4). The last equality constraint is given by the voltage-second product equalization using (1). The inequality constraints arise from the position of the square-wave voltage applied by the DC port in relation to the AC side applied HF voltages and the minimum commutation current for ZVS. The rising edge of the HF DC port voltage from 0 to V_{dc} is constrained to interval $[\tau_1, \tau_7]$ by means of

$$-\phi_{dc} + \delta_{dc} \geq \delta_{ph1}\ (= \tau_1),\quad -\phi_{dc} + \delta_{dc} \leq \delta_{ph1} + \pi\ (= \tau_7) \tag{5}$$

whereas the constraints for the rising edge from $-V_{dc}$ to 0 in interval $[\tau_1, \tau_7]$ are given as

$$-\phi_{dc} - \delta_{dc} \geq \delta_{ph1}\ (= \tau_1),\quad -\phi_{dc} - \delta_{dc} \leq \delta_{ph1} + \pi\ (= \tau_7). \tag{6}$$

The minimum commutation current $I_{min} > 0$ needed for ZVS leads to the constraint

$$I_{ZVS} \geq I_{min}, \tag{7}$$

where the ZVS current point $I_{ZVS} = i_{L\sigma}(\tau_2) = i_{L\sigma}(\tau_7)$ is calculated according to Fig. 4 and given by

$$I_{ZVS} = -\frac{|v_{ph1}| + |v_{ph2}| + |v_{ph3}| + 2nV_{dc}}{4\omega_s L_\sigma} (\phi_{dc} + \delta_{dc} + \delta_{ph1}). \tag{8}$$

Analytic Control Variables

With the control variables numerically obtained by the above described optimization procedure (see Fig. 5), the rising edge of the HF DC port voltage from 0 to V_{dc} is always lagging the falling edge of the HF AC port voltage of phase 1 from $|v_{ph1}|/2$ to 0. This circumstance is used in the following for determining the control variables $\tau_{ph1}, \tau_{ph2}, \tau_{ph3}, \tau_{dc}, \theta_{dc}$ shown in Fig. 4 analytically in a sequential calculation scheme.

First, from the minimum commutation current I_{ZVS} needed for ZVS, the length of the current reversal interval is determined as

$$\theta_{dc} = \frac{4\omega_s L_\sigma I_{ZVS}}{|v_{ph1}| + |v_{ph2}| + |v_{ph3}| + 2nV_{dc}} \tag{9}$$

where $\omega_s = 2\pi/T_s$. With the reference phase currents $i^*_{ph3}, i^*_{ph2}, i^*_{ph1}$, the control variables $\tau_{ph3}, \tau_{ph2}, \tau_{ph1}$ are then calculated by sequentially solving the equations

$$i^*_{ph3} = \frac{\text{sign}(v_{ph3})}{2\pi} \int_0^{\tau_{ph3}-\theta_{dc}} \frac{|v_{ph1}| + |v_{ph2}| + |v_{ph3}|}{2\omega_s L_\sigma} \tau + I_{ZVS} \, d\tau, \tag{10}$$

$$i^*_{ph2} = i^*_{ph3} \frac{\text{sign}(v_{ph2})}{\text{sign}(v_{ph3})} + \frac{\text{sign}(v_{ph2})}{2\pi} \int_0^{\tau_{ph2}-\tau_{ph3}} \frac{|v_{ph1}| + |v_{ph2}|}{2\omega_s L_\sigma} \tau + i_{L\sigma}(\tau_3) \, d\tau, \tag{11}$$

$$i^*_{ph1} = i^*_{ph2} \frac{\text{sign}(v_{ph1})}{\text{sign}(v_{ph2})} + \frac{\text{sign}(v_{ph1})}{2\pi} \int_0^{\tau_{ph1}-\tau_{ph2}} \frac{|v_{ph1}|}{2\omega_s L_\sigma} \tau + i_{L\sigma}(\tau_4) \, d\tau, \tag{12}$$

where the integral terms represent the average current over a switching cycle from the AC ports to the DC port (see Fig. 4). Finally, the voltage-second product equalization (1) shown by the shaded areas in Fig. 4 leads to

$$\tau_{dc} = \frac{1}{2nV_{dc}} \left[|v_{ph1}|(\tau_{ph1} - \theta_{dc}) + |v_{ph2}|(\tau_{ph2} - \theta_{dc}) + |v_{ph3}|(\tau_{ph3} - \theta_{dc}) \right]. \tag{13}$$

The obtained control variables can then be transformed to clamping intervals $\delta_{ph1}, \delta_{ph2}, \delta_{ph3}, \delta_{dc}$ and phase-shifts $\phi_{ph1}, \phi_{ph2}, \phi_{ph3}, \phi_{dc}$ according to

$$\delta_{ph1} = \frac{1}{2}(\pi - \tau_{ph1}), \ \ \delta_{ph2} = \frac{1}{2}(\pi - \tau_{ph2}), \ \ \delta_{ph3} = \frac{1}{2}(\pi - \tau_{ph3}), \ \ \delta_{dc} = \frac{1}{2}(\pi - \theta_{dc} - \tau_{dc}), \tag{14}$$

$$\phi_{ph1} = 0, \ \ \phi_{ph2} = \delta_{ph2} - \delta_{ph1}, \ \ \phi_{ph3} = \delta_{ph3} - \delta_{ph1}, \ \ \phi_{dc} = -(\delta_{ph1} + \theta_{dc} + \delta_{dc}). \tag{15}$$

Fig. 6 shows the control variables assigned to the phases for a mains period calculated with parameters from Table I at an input power of 11 kW and a DC voltage of 460 V.

Modelling of Power Flows

For designing and controlling a multi-port converter system, the mathematical description of the power flows depending on the control variables is essential. The optimization procedure shown in Fig. 5 requires the calculation of the power flows $p_{ph1}, p_{ph2}, p_{ph3}$ for evaluating the power equality constraints (3).

The well-known approach uses piecewise linear equations for the transformer leakage inductance current where several mathematical cases depending on the phase-shifts and the clamping intervals have to be distinguished. Due to the mathematical complexity, especially for high port numbers, the following analysis uses basic superposition principles to find general analytical formulas for the power flows. With this approach, there is no need for mathematical distinction of cases.

The mathematical analysis of the power flows at the AC ports and the DC port is based on the AC side referred equivalent circuit of the converter topology shown in Fig. 3. The T-type circuits and the full-bridge are modelled by HF square-wave voltage sources $v_{p,a}, v_{p,b}, v_{p,c}, v'_{s,dc}$ with clamping intervals.

For the analytical description of the power flow at an AC port, first the power flow between two ports applying square-wave voltages with clamping intervals is modelled (see Fig. 8a).
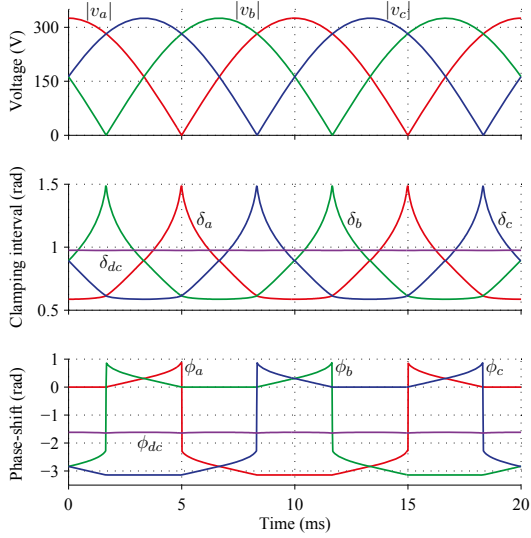
Figure 6: Control variables in terms of clamping intervals $\delta_a, \delta_b, \delta_c, \delta_{dc}$ and phase-shifts $\phi_a, \phi_b, \phi_c, \phi_{dc}$ over a mains period. For example, at 5 ms the clamping interval δ_a reaches its maximum value of $\pi/2$ where the reference power $p_a^* = 0$ (PFC operation).
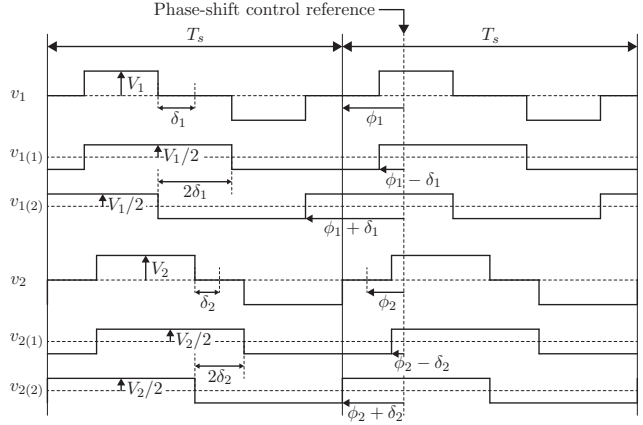
Figure 7: Square-wave voltages v_1, v_2 with clamping intervals $2\delta_1, 2\delta_2$ and the underlying square-wave voltages $v_{1(1)}, v_{1(2)}, v_{2(1)}, v_{2(2)}$ without clamping intervals and duty cycles 50 % which add up to v_1 and v_2 respectively.

Power Flow between two Ports

The power flow over one switching cycle $T_s = 2\pi/\omega_s$ between two ports (from a first port 1 to a second port 2) applying square-wave voltages with clamping intervals as shown in Fig. 8a is based on the well-known power flow equation [10] (power from primary port p to secondary port s)

$$P_{ps} = \frac{V_p n V_s}{\omega_s L_\sigma} (\phi_p - \phi_s) \left(1 - \frac{|\phi_p - \phi_s|}{\pi}\right). \tag{16}$$

There, two square-wave voltages with 50 % duty cycles, amplitudes V_p, V_s and phases $\phi_p, \phi_s \in \{-\pi, \pi\}$ are applied across the windings of a two-winding transformer with primary referred leakage inductance L_σ, negligible large magnetizing inductance and turns ratio $n = N_p/N_s$. The phase angles are measured against a given reference, a positive angle defines a leading signal and a negative angle a lagging signal with respect to the reference.

The two-port circuit with clamping intervals drawn in Fig. 8a can be modelled by the equivalent four-port circuit drawn in Fig. 8b where only square-wave voltages without clamping intervals and duty cycles of 50 % occur. This is done by splitting up voltage v_1 with clamping interval into a sum $v_{1(1)} + v_{1(2)}$ of two voltages with 50 % duty cycle, no clamping interval and a phase-shift of $2\delta_1$ against each other as depicted in Fig. 7. Analogously, this is done for the voltage v_2. The power transferred from port 1 to port 2 is then given by

$$P_{12} = \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{1(1)} i_{L\sigma} \, d\tau}_{P_{12(1)}} + \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{1(2)} i_{L\sigma} \, d\tau}_{P_{12(2)}} \tag{17}$$

with the two power shares of voltage sources $v_{1(1)}, v_{1(2)}$ (see Fig. 8b). The leakage inductance current $i_{L\sigma}$ is split up into three parts $i_{L\sigma(I)}, i_{L\sigma(II)}, i_{L\sigma(III)}$ which are obtained by applying the superposition principle as shown in Fig. 9 by selectively short-circuiting voltage sources. In this way, the power exchange of source $v_{1(1)}$ with sources $v_{1(2)}, v'_{2(1)}, v'_{2(2)}$ is described. The power share $P_{12(1)}$ in (17) can then be written as

$$P_{12(1)} = \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{1(1)} i_{L\sigma(I)} \, d\tau}_{P_{12(1)(I)}} + \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{1(1)} i_{L\sigma(II)} \, d\tau}_{P_{12(1)(II)}} + \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{1(1)} i_{L\sigma(III)} \, d\tau}_{P_{12(1)(III)}}. \tag{18}$$
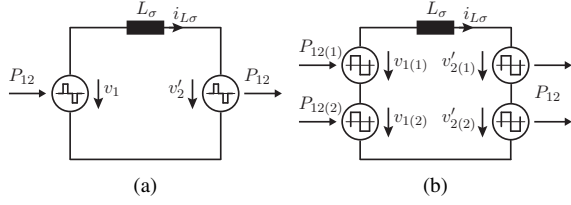
Figure 8: Simplified circuit of a two-port converter applying square-wave voltages with clamping intervals (a) and the equivalent four-port circuit applying square-wave voltages without clamping intervals at the ports (b).
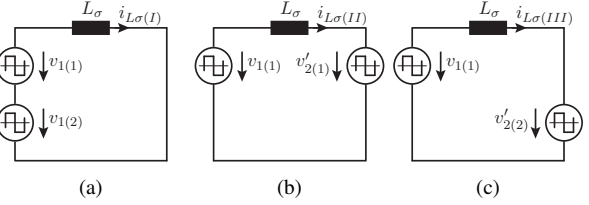
Figure 9: Leakage inductance current $i_{L\sigma} = i_{L\sigma(I)} + i_{L\sigma(II)} + i_{L\sigma(III)}$ obtained by applying the superposition principle with three parts (a), (b), (c) by selectively short-circuiting voltage sources.

Analogously, the second power share $P_{12(2)}$ is described. From Fig. 9 and (18) it is concluded, that the power shares $P_{12(1)(I)}, P_{12(1)(II)}, P_{12(1)(III)}$ are given by (16). This is also the case for the power shares $P_{12(2)(I)}, P_{12(2)(II)}, P_{12(2)(III)}$. By summing up all the power shares, the resulting power transferred per switching cycle from port 1 to port 2 applying square-wave voltages v_1, v_2 with clamping intervals $2\delta_1, 2\delta_2$ and phases ϕ_1, ϕ_2 as shown in Fig. 7 is thus given as

$$
\begin{aligned}
P_{12} = \frac{V_1 n V_2}{4\omega_s L_\sigma} \Bigg[& ((\phi_1 - \delta_1) - (\phi_2 - \delta_2)) \left(1 - \frac{|(\phi_1 - \delta_1) - (\phi_2 - \delta_2)|}{\pi} \right) \\
& + ((\phi_1 - \delta_1) - (\phi_2 + \delta_2)) \left(1 - \frac{|(\phi_1 - \delta_1) - (\phi_2 + \delta_2)|}{\pi} \right) \\
& + ((\phi_1 + \delta_1) - (\phi_2 - \delta_2)) \left(1 - \frac{|(\phi_1 + \delta_1) - (\phi_2 - \delta_2)|}{\pi} \right) \\
& + ((\phi_1 + \delta_1) - (\phi_2 + \delta_2)) \left(1 - \frac{|(\phi_1 + \delta_1) - (\phi_2 + \delta_2)|}{\pi} \right) \Bigg].
\end{aligned}
\tag{19}
$$

This analytical power equation represents the basis for modelling the power flows at the AC ports as functions of the control variables in the three-phase AC-DC converter.

Power Flow at AC Ports

With the general power flow equation (19), in a next step, the analytical formulas for the power flows at the AC ports are derived. This is exemplarily done for phase a. The same derivation applies to phases b, c. Looking at Fig. 3, the previous mentioned superposition principle is also applicable. For phase a, the voltage source $v_{p,a}$ exchanges power with all other sources $v_{p,b}, v_{p,c}, v'_{s,dc}$ which leads to the power flow

$$
p_a = \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{p,a} i_{L\sigma(1)} \, d\tau}_{p_{a(1)}} + \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{p,a} i_{L\sigma(2)} \, d\tau}_{p_{a(2)}} + \underbrace{\frac{1}{T_s} \int_0^{T_s} v_{p,a} i_{L\sigma(3)} \, d\tau}_{p_{a(3)}}
\tag{20}
$$

from the AC port a to all other ports. The leakage inductance current is split up into three parts $i_{L\sigma(1)}, i_{L\sigma(2)}, i_{L\sigma(3)}$. The power shares are then formulated by means of (19) and given by

$$
p_{a(1)} = P_{12}(V_1 = v_a/2, nV_2 = -v_b/2, \delta_1 = \delta_a, \phi_1 = \phi_a, \delta_2 = \delta_b, \phi_2 = \phi_b),
\tag{21}
$$

$$
p_{a(2)} = P_{12}(V_1 = v_a/2, nV_2 = -v_c/2, \delta_1 = \delta_a, \phi_1 = \phi_a, \delta_2 = \delta_c, \phi_2 = \phi_c),
\tag{22}
$$

$$
p_{a(3)} = P_{12}(V_1 = v_a/2, V_2 = V_{dc}, \delta_1 = \delta_a, \phi_1 = \phi_a, \delta_2 = \delta_{dc}, \phi_2 = \phi_{dc}).
\tag{23}
$$

(20) together with (21), (22), (23) is then used in the optimization procedure shown in Fig. 5 for numerically calculating the power flows $p_{ph1}, p_{ph2}, p_{ph3}$.
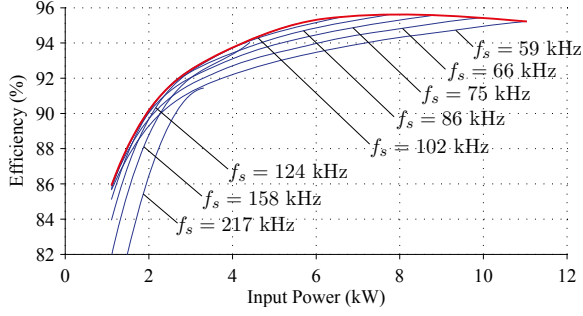
Figure 10: Calculated efficiencies over the input power range for a battery voltage of 460 V and different switching frequencies. By increasing the switching frequency with decreasing input power, the converter efficiency can be boosted, up to a frequency of around 124 kHz at 3 kW input power. The red line shows the maximum efficiency when the frequency is varied.
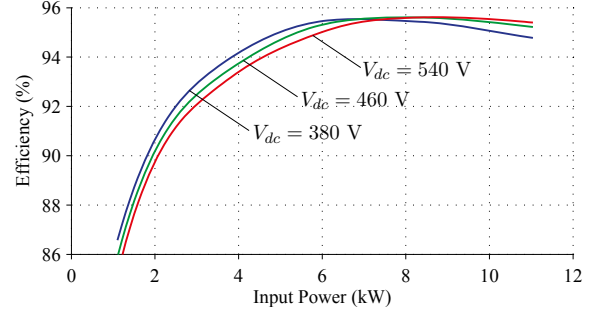

Figure 11: Calculated efficiencies over the input power range for battery voltages 380 V, 460 V and 540 V. Due to relatively high auxiliary losses caused by the four fans in the prototype system and conduction losses caused by the circulating current through all ports, the efficiency decreases relatively fast at low input power.

Prototype System

As a prototype system, a 11 kW electric vehicle battery charger to connect to the three-phase $230\,V_{rms}$, 50 Hz mains with an output voltage range of 380 V to 540 V of a Lithium-ion battery is considered. The AC and DC port switching devices are chosen to be 650 V MOSFETs of type STY145N65M5 with a typical on-resistance of 12 mΩ at a junction temperature of 25 °C [11]. The system parameters are listed in detail in Table I. A 3D drawing of the prototype system is shown in Fig. 13.

Converter Components and Loss Model

In the following, the converter components are described with their loss models to calculate the efficiency of the converter applying the proposed ZVS control scheme with analytically determined control variables. Table II summarizes the components of the prototype system whereas Fig. 10 shows the calculated efficiencies over an input power range from 10 % to 100 % for a battery voltage of 460 V and different switching frequencies. By increasing the switching frequency with decreasing input power, the converter efficiency can be boosted, up to a frequency of around 124 kHz at 3 kW input power. The maximum efficiencies which can be achieved by varying the switching frequency are drawn in Fig. 11 for battery voltages 380 V, 460 V and 540 V. A peak efficiency of 95.6 % is reached at an input power of 8.7 kW and a battery voltage of 540 V. The estimated power density is around 2.5 kW/L. Fig. 12 shows the calculated distribution of the power losses among the converter components at the maximum input power and a battery voltage of 460 V.

Power MOSFETs

The losses of the power MOSFETs are mainly determined by conduction losses. Switching losses P_{sw} per MOSFET are approximated by measurement data. To reduce conduction losses, N_s number of MOSFETs are paralleled, so that the power loss per switch i is then approximated by

$$P_{Si} = \frac{R_{ds,on}}{N_s} I_{Si,rms}^2 + N_s P_{sw}\left(\frac{I_{Si}}{N_s}\right) \quad i = \{1a, 1b, 2a, 2b, 3a, 3b, 1, 2, 3, 4\}. \tag{24}$$

Table I: Parameters of the prototype system.

Mains voltage	V_{abc}	$230\,V_{rms} \pm 10\,\%$
Mains frequency	f_{abc}	50 Hz
Battery voltage	V_{dc}	380 V … 540 V
Output power	P_{dc}	11 kW
Switching frequency	f_s	50 kHz … 140 kHz
Transformer turns ratio	n	1
Transformer leakage inductance	L_σ	11.5 µH
Transformer magnetizing inductance	-	neglected
Inductors	L_f	100 µH
Capacitors	C_{ac}	20 µF
Inductor	L_{dc}	100 µH
Capacitor	C_{dc}	60 µF

Table II: Components of the prototype system.

| MOSFETs $S_{1a}, S_{1b}, S_{2a}, S_{2b}$	2x STY145N65M5, 650 V
MOSFETs S_{3a}, S_{3b}	3x STY145N65M5, 650 V
MOSFETs S_1, S_2, S_3, S_4	3x STY145N65M5, 650 V
Transformer	2x 2x E 80/38/20 N87
	9 AC side turns, 9 DC side turns
	Litz wire, 2205 strands, 0.071 mm
Inductors L_f	2x Kool Mu 4317 26u, 27 turns
	Litz wire, 20 strands, 0.355 mm
Inductor L_{dc}	2x Kool Mu 4022 26u, 24 turns
	Litz wire, 45 strands, 0.355 mm
Capacitors C_{ac}	36x Syfer 1825J500564KX, 560 nF
Capacitor C_{dc}	108x Syfer 1825J500564KX, 560 nF
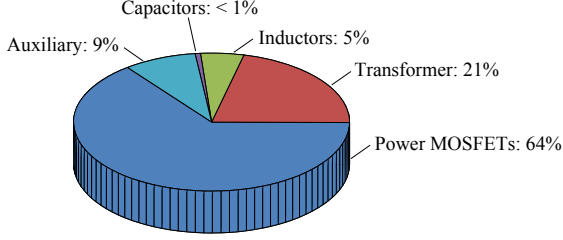
Figure 12: Calculated distribution of the power losses among the converter components at an input power of 11 kW and a battery voltage of 460 V.
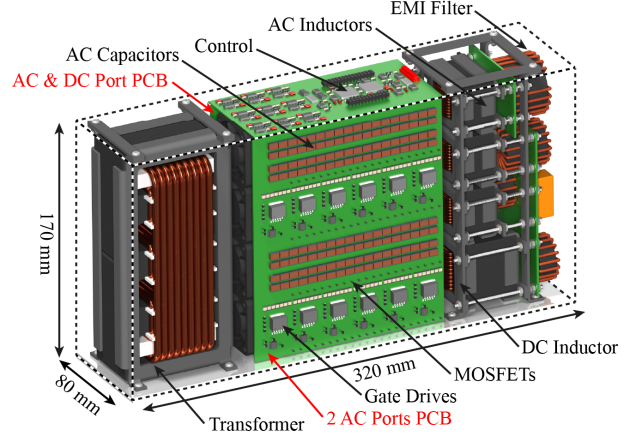

Figure 13: 3D drawing of the 11 kW prototype system with a peak efficiency of 95.6 % at an input power of 8.7 kW, a battery voltage of 540 V and a power density of 2.5 kW/L.

For conduction loss calculations, a junction temperature of 60 °C is assumed, as the thermal heat sink to ambient resistance is small in order to keep conduction losses low.

Transformer

The turns ratio n of the transformer is chosen such that $V'_{dc} > \hat{V}_{abc}/2$ (with V'_{dc} referred to the AC side) is always satisfied, also at the lowest battery voltage of 380 V (operation always in boost mode). The transformer leakage inductance L_σ is determined in such a way, that the maximum input power of 11 kW can be transferred at the lowest switching frequency of 50 kHz and the lowest battery voltage of 380 V. For the transformer, two stacked E-core sets E 80/38/20 with N87 material [12] next to each other are used with the AC side windings wound on separate legs and the DC winding around them as drawn in Fig. 2. The air space between AC windings and DC winding defines the size of the leakage inductance. In the loss model, the core losses per volume are calculated by applying the improved Generalized Steinmetz Equation (iGSE) [13]. The skin and proximity effect losses per unit length in litz wires for each current harmonic are determined according to [14]. The external magnetic field strength for evaluating proximity effect losses is derived by a 1D approximation using the Dowell method [15].
For the given core arrangement, total losses including core losses as well as skin and proximity effect losses using litz wire are minimized subject to turns ratio and leakage inductance constraints. The optimal turns number are found to be 9 for all windings. 2114 strands for the AC windings and 2538 for the DC winding with a diameter of 0.08 mm lead to lowest transformer losses. The prototype system applies the available litz wire with 2205 strands with a diameter of 0.071 mm.

Inductors

The AC side filter inductors L_f are built with two stacked E-cores of type Kool Mu 4317, the DC side filter inductor L_{dc} with two stacked E-cores of type Kool Mu 4022. The chosen material for both core types is 26u from Magnetics [16]. Powder cores are ideally suited for the prototype system because they offer a distributed air gap and a high saturation flux density of around 1 T and are therefore advantageous over a ferrite core with a large air gap exhibiting considerable fringing magnetic field. Both inductors are wound with litz wire of 0.355 mm strand diameter, 20 strands in case of the AC inductors L_f and 45 strands for the DC inductor L_{dc}. The number of turns for AC inductors are 27, for DC inductor 24, so that a minimum inductance value of 100 µH is guaranteed at the highest peak current.
The core losses per volume are calculated by using the iGSE, the Steinmetz parameters are obtained from [16]. The skin and proximity effect losses per unit length in litz wires for each current harmonic are calculated according to [14]. Also for the inductors, the external magnetic field strength is derived by a 1D approximation using the Dowell method [15].

Capacitors

For AC and DC port capacitors C_{ac}, C_{dc}, paralleled 560 nF ceramic capacitors with dielectric X7R from Syfer [17] are used. Multilayer ceramic capacitors exhibit high energy density and are therefore ideally suited to achieve high power densities. Determining the HF capacitor RMS current $I_{Ci,rms}$, dissipation power losses are calculated according to

$$P_{Ci} = \frac{R_{esr}}{N_c} I^2_{Ci,rms} \quad i = \{ac, dc\} \tag{25}$$
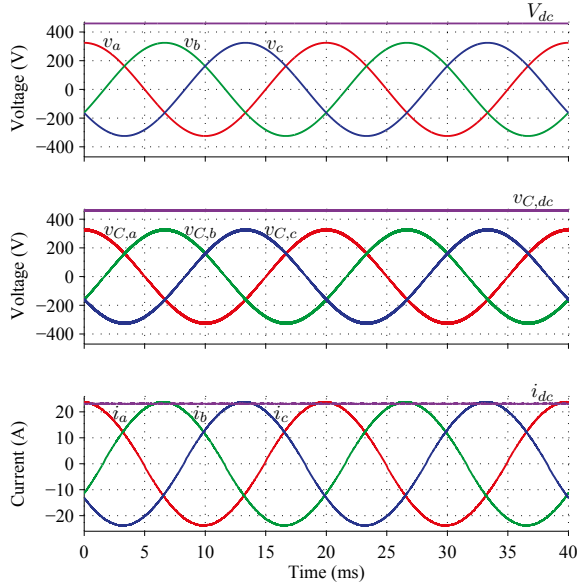
Figure 14: Simulated AC phase currents i_a, i_b, i_c and DC current i_{dc} of the AC-DC converter with parameters given in Table I for reference values $I^*_{abc} = 16\,\mathrm{A_{rms}}, \phi^*_{abc} = 0$ in AC-to-DC operation. The capacitor voltages $v_{C,a}, v_{C,b}, v_{C,c}$ represent the voltages across the series connection of the two capacitors C_{ac} in each phase. $v_{C,dc}$ is the voltage across the DC capacitor C_{dc}.
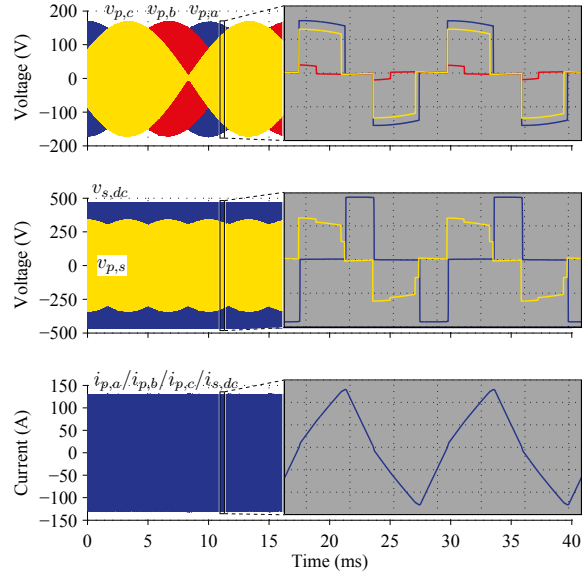
Figure 15: Simulated voltages $v_{p,a}, v_{p,b}, v_{p,c}, v_{s,dc}$ across the transformer windings, resulting voltage sum $v_{p,s}$ and transformer winding currents $i_{p,a}, i_{p,b}, i_{p,c}, i_{s,dc}$ of the AC-DC converter with parameters given in Table I for reference values $I^*_{abc} = 16\,\mathrm{A_{rms}}, \phi^*_{abc} = 0$ in AC-to-DC operation.

where R_{esr} denotes the equivalent series resistance obtained from datasheet and N_c the number of capacitors paralleled.

Auxiliary Losses

Besides the load dependent loss shares shown in the previous sections, a constant loss share for precharging relays, gate drives, control, sensing and four fans of 40 W is considered. Additional losses caused by a two-stage EMI filter are approximated by an equivalent resistance of 4 mΩ.

Cooling System

The number of semiconductors basically defines the base plate size of the heat sink as 160 mm × 113 mm for AC and DC side switching devices, so that a double-sided heat sink can be used. Four 40 mm × 40 mm fans of type San Ace 40 are applied for forced convection cooling. After optimizing the cooling system as described in [18], a thermal heat sink to ambient resistance of $R_{th,s-a} = 0.12\,\mathrm{K/W}$ results which in turn leads to a Cooling System Performance Index (CSPI) of 20.8.

Simulation Results

The proposed converter is simulated in GeckoCIRCUITS [19] with a simulation model according to Fig. 1 and the parameters given in Table I for an input current reference $I^*_{abc} = 16\,\mathrm{A_{rms}}$ and an output voltage $V_{dc} = 460\,\mathrm{V}$ in AC-to-DC operation for a mains voltage of $230\,\mathrm{V_{rms}}$ as can be seen in Fig. 14 and Fig. 15.

Conclusion

An isolated three-phase bidirectional AC-DC converter based on a multi-port approach with a novel modulation strategy to ensure ZVS for all switches over the whole AC line period is presented. The derivation of the control variables under ZVS conditions is based on a novel modelling approach of the power flows applying basic superposition principles to avoid mathematical distinction of cases. For validating the theoretical analysis, the design of components including loss models as well as simulation results of a 11 kW electric vehicle battery charger are provided. Compared to state-of-the-art three-phase systems, single converter modules can be connected in series or parallel at the input/output ports for medium- or high-voltage applications. Due to the circulating current through all ports, a relatively large chip area is required on the AC side. A peak efficiency of 95.6 % is reached at an input power of 8.7 kW, a battery voltage of 540 V and a power density of 2.5 kW/L.

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