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Motor-Integrated Three-Phase Multi-Level Si/GaN Inverter Systems for Future Servo Drives

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Abstract

Ongoing industrial automatization and modernization relies on accurate, fast, compact, easy-to-install, and easy-to-maintain Variable Speed Drive (VSD) systems. Moreover, they must align with global energy-saving targets. The latter drives a concurrent trend towards local DC supply grids installed on manufacturing sites (e.g., up to 800 V), which enables a direct energy exchange between multiple VSD systems without loading the AC grid interface.
In this context, Integrated Motor Drives (IMDs) are gaining popularity. Compared to standard drive systems with the power electronics accommodated in a dedicated cabinet, IMDs offer a more compact realization by arranging the drive and motor in a single housing. This eliminates the need for expensive shielded cables between the inverter stage and the motor, allowing for a more straightforward on-site installation. Advantageously, the IMD design is facilitated considerably when operated on a DC supply grid, as only the inverter stage has to be integrated into the motor (i.e., without active/passive rectifier front-end). However, the close proximity of motor and inverter leads to potentially higher operating temperatures of the power electronic components. This is particularly challenging for, e.g., servo applications, which have mission profiles with overload torques of two to three times the nominal torque during several seconds.
Accordingly, motor integration does not only rely on a compact inverter design, but also on high efficiency, and on a good (transient) cooling capability of the power electronics, in particular of the semiconductors. These challenges can be tackled with Wide Bandgap (WBG) semiconductor devices, featuring improved conduction and switching performance compared to the established Si-IGBTs. Yet, the high switching speeds of these devices may lead to issues such as resonances in the motor windings, which necessitate the use of an output filter to protect the motor from the inverter stage.
Multi-Level (ML) inverter topologies lend themselves to minimizing the volume of such output filters. Moreover, they allow the utilization of lower voltage semiconductors featuring superior switching and on-state performance.

The primary objective of this thesis is to explore ML inverter solutions for Permanent Magnet Synchronous Motor (PMSM) IMDs with high short-term overload capability. Thereby, the comparison is extended beyond pure power density and efficiency considerations and also includes aspects such as mechanical realization effort, reliability, and complexity.
The initial step involves investigating the optimal level number of a ML Flying

Capacitor inverter (FCi) with a full sine-wave *LC* output filter. The analysis is based on a straightforward device Figure-of-Merit (FOM) for Si and GaN semiconductor technology and highlights the potential benefits of ML topologies, especially for Si with comparatively poor performing semiconductors for higher voltage ratings. When accounting for the performance of the semiconductor devices available on the market, the analysis leads to a feasible realization of a 7L-FCi for Si and a 3L-FCi for GaN semiconductor technology. Subsequently, both possible IMD candidates are designed in the most compact way for a 99% inverter efficiency at 7.5 kW nominal output power, providing a high short-term overload capability (i.e., three times nominal current during three seconds). Based on similar anticipated total volumes (incl. *LC* output filters), the less complex 3L-FCi is realized as a phase-modular hardware demonstrator. Its overload capability is characterized by a transient dynamic thermal model, and the expected properties (i.e., nominal efficiency as well as the short-term overload capability) are experimentally confirmed
In the next step, the analysis is expanded to consider alternative topologies, such as the 7L-Hybrid Active Neutral-Point Clamped Converter (7L-HANPC), which achieves with reduced complexity the same compact filter inductor volume as the 7L-FCi. Hence, for a comprehensive evaluation, both the 7L-HANPC as well as the 7L-FCi are built and their nominal and overload performance is experimentally verified and compared with the 3L-FCi. Ultimately, the 3L-FCi stands out as the preferred option, featuring the best overall trade-offs for motor integration with minimal realization effort.
Last but not least, by reconfiguring the PMSM to a dual three-phase winding machine, a Stacked Polyphase Bridge Inverter (SPBI) topology, specifically a converter system formed by two Series-Stacked Two-Level three-phase Converters (2L-SSCs), can be employed with similar semiconductor effort as the 3L-FCi. The 2L-SSC benefits from a standard six-pack semiconductor arrangement, has no additional capacitors besides the DC link (i.e., no flying capacitors), and features a straightforward Common Mode (CM) cancellation capability. This leads to a further reduction in complexity and to a considerable reduction in volume and losses if only a CM choke instead of a full sine-wave *LC* output filter is required in the design; however, the volume and losses are increased compared to a 3L-FCi if a full sine-wave *LC* output filter is targeted for maximum motor-friendliness.

Kurzfassung

Die kontinuierlich fortschreitende industrielle Automatisierung und Modernisierung ist auf präzise, hochdynamische und kompakte Motorantriebsysteme angewiesen, die einfach zu installieren und zu warten sind. Darüber hinaus müssen sie mit den Erwartungen der globalen Energiesparmassnahmen übereinstimmen. Letzteres führt zu zunehmender Einführung von Gleichspannungsverteilsystemen in Industrieanlagen (mit bis zu 800 V), welche den direkten Energieaustausch zwischen mehreren Antrieben ohne Belastung der Wechselstromnetzschnittstelle ermöglicht.
In diesem Kontext gewinnen integrierte Motorantriebe, sogenannte Integrated-Motor Drives (IMDs), zunehmend an Popularität. Verglichen zu Standardsystemen, bei denen die Leistungselektronik in einem eigenen Schaltschrank untergebracht ist, bietet ein integrierter Motorantrieb eine kompaktere Realisierung, bei welcher die Elektronik und der Motor in einem einzigen Gehäuse platziert werden. Dadurch entfällt die teure geschirmte Verkabelung zwischen Umrichter und Motor, was eine einfachere Installation des Systems ermöglicht. Des Weiteren ist die Motorintegration begünstigt durch den Betrieb am Gleichspannungsnetz, da nur der Wechselrichter (ohne aktiven/passiven Gleichrichter) im Motor untergebracht werden muss.
Allerdings führt die räumliche Nähe von Motor und Umrichter zu erhöhten Betriebstemperaturen der elektronischen Komponenten. Dies ist vor allem eine Herausforderung für Systeme, welche hohe kurzzeitige Überlastdrehmomente bereitstellen müssen, wie es z.B. bei einem Umrichter für Servomotoren der Fall ist mit zwei- bis dreifachem nominalem Drehmoment während mehrerer Sekunden.
Dementsprechend sind integrierte Motorumrichter nicht nur auf eine kompakte Realisierung der Leistungsstufe angewiesen, sondern auch auf einen hohen elektrischen Wirklungsgrad, sowie auf eine gute (transiente) Kühlbarkeit der Leistungselektronik, und hier vor allem der Leistungshalbleiter. Diese Herausforderungen können mit modernen Leistungshalbleitertechnologien mit weitem Bandabstand (Wide-Bandgap (WBG) Leistungshalbleiter) bewältigt werden, die im Vergleich zu etablierten Si-IGBT ein verbessertes Leit- und Schaltverhalten aufweisen. Andererseits kann die hohe Schaltgeschwindigkeit dieser Bauteile zu Problemen führen, wie z.B. zu Resonanzen in der Motorwicklung, was den Einsatz eines Ausgangsfilters zum Schutz des Motors vor der Wechselrichterstufe erforderlich macht.
Multi-Level (ML) Umrichter bieten sich an, um das Volumen solcher Ausgangsfilter zu minimieren. Zudem gestatten sie die Verwendung von Halbleitern

mit tieferen Sperrspannungen, welche ein besseres Leit- und Schaltverhalten aufweisen als solche mit höheren Sperrspannungen.

Das Hauptziel dieser Arbeit ist die Untersuchung von integrierten ML Motor-Wechselrichter-Lösungen für einen Permanentmagnet-Synchronmotor (PMSM) mit hohem Kurzzeit-Überlastdrehmoment. Der Vergleich fokussiert dabei nicht nur auf die Betrachtung der Leistungsdichte und der Effizienz der verschiedenen Topologien, sondern schliesst auch Aspekte wie den mechanischen Realisierungsaufwand, Zuverlässigkeit und Komplexität mit ein.
In einem ersten Schritt wird die optimale Anzahl von Ausgangsspannungslevels eines ML Flying-Capacitor (FC) Umrichters mit Sinus-*LC*-Ausgangsfilter untersucht. Die Analyse basiert auf einer einfachen Halbleiterleistungskennzahl (einer sogenannten Figure-of-Merit (FOM)) für Si und GaN Halbleitertechnologien. Die Resultate verdeutlichen, dass ML-Wechselrichter besondere Vorteile beim Einsatz von Si Leistungshalbleitern haben, da diese Transistoren für höheren Sperrspannungen nicht konkurrenzfähig sind. Unter Berücksichtigung der auf dem Markt erhältlichen Leistungsschalter, führt die Analyse zu möglichen Realisierungen eines 7L FC-Umrichters für Si und eines 3L FC-Umrichters für GaN Technologie.
Im Anschluss werden beide IMD-Kandidaten auf eine möglichst kompakte Art für 99% Umrichtereffizienz bei 7.5 kW nominaler Ausgangsleistung ausgelegt, inklusive einer hohen Kurzzeit-Überlastfähigkeit (d.h., dreifachen Nennstrom während drei Sekunden). Da die zu erwartenden Volumina (inkl. *LC*-Ausgangsfilter) für beide Implementierungen ähnlich sind, wird der wesentlich einfachere 3L GaN FC Umrichter als phasenmodularer Hardware Demonstrator gebaut. Seine Überlastfähigkeit wird mittels eines transienten thermischen Modells charakterisiert und die erwarteten Eigenschaften (d.h., seine Effizienz im nominalen Betrieb sowie sein Verhalten im Überlastfall) experimentell bestätigt.
Im nächsten Schritt wird die Untersuchung auf alternative Topologien erweitert. Dabei erreicht ein siebenstufiger Hybrid-Wandler (7L Hybrid Active Neutral Point Clamped (HANPC) Konverter) das gleiche kompakte Filtervolumen wie ein 7L Si FC Umrichter, jedoch mit einem geringeren Realisierungsaufwand. Für einen umfassenden Vergleich werden sowohl der 7L HANPC als auch der 7L FC Umrichter gebaut, ihre Nenn- und Überlastfähigkeit experimentell verifiziert und ihre Eigenschaften anschliessend mit der 3L FC Wechselstufe verglichen. Letztere erweist sich als die bevorzugte Option, da sie bei minimaler Komplexität die besten Gesamteigenschaften für eine Motorintegration ausweist.
Durch Umkonfigurieren des PMSM zu einem Doppel-Dreiphasen-Wicklungs-

system kann eine Stacked-Polyphase-Bridge-Umrichter Topologie (SPBI), genauer gesagt eine two Series-Stacked Two-Level three-phase Converter (2L SSC) Topologie, mit dem einem 3L FC Umrichter gleichen Halbleiteraufwand eingesetzt werden. Dabei profitiert der 2L SSC von einer Standard-Six-Pack-Halbleiteranordnung, benötigt neben dem Zwischenkreis keine zusätzlichen Kondensatoren (d.h. keine Flying Capacitors) und erlaubt eine einfache Gleichtaktspannungsunterdrückung. Verglichen mit dem 3L FC Umrichter führt dies zu einer Vereinfachung des Systems und, wenn nur eine CM Drossel anstelle eines Sinus-*LC*-Ausgangsfilters erforderlich ist, zu einer beträchtlichen Verringerung des Volumens und der Verluste; allerdings erhöhen sich das Volumen und die Verluste im Vergleich zu einem 3L FC Umrichter, wenn ein Sinus-*LC*-Ausgangsfilter für maximale Motorfreundlichkeit vorgesehen wird.

Abbreviations

2L-SSC	Series-Stacked Two-Level three-phase Converter
3L-FCC	3L-Flying Capacitor Converter
4L-FCC	4L-Flying Capacitor Converter
7L-FCC	7L-Flying Capacitor Converter
7L-HANPC	7L-Hybrid Active Neutral-Point Clamped Converter
ADC	Analog-to-Digital Converter
ANPC	Active Neutral-Point Clamped
CHB	Cascaded H-Bridge
CM	Common Mode
CSPI	Cooling System Performance Index
DC	Direct Current
DM	Differential Mode
DS	Drain-Source
DSP	Digital Signal Processor
EDM	Electric Discharge Machining
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
EV	Electric Vehicle
FC	Flying Capacitor
FCi	Flying Capacitor inverter
FCC	Flying Capacitor Converter
FEM	Finite Element Method
FOC	Field-Oriented Control
FOM	Figure-of-Merit
FPGA	Field-Programmable Gate Array
GaN	Gallium-Nitride
GD	Gate Driver
GS	Gate-Source

HANPC	Hybrid Active Neutral-Point Clamped
HB	Half-Bridge
HEMT	High-Electron-Mobility Transistor
HF	High-Frequency
HS	High-Side
HSW	Hard Switching
HV	High-Voltage
IC	Integrated Circuit
IGBT	Insulated-Gate Bipolar Transistor
IMD	Integrated Motor Drive
LCA	Life-Cycle Assessment
LF	Low-Frequency
LS	Low-Side
LV	Low-Voltage
MF	Medium-Frequency
ML-FCi	Multi-Level Flying Capacitor inverter
ML	Multi-Level
MMC	Modular Multi-Level Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	Medium-Voltage
NPC	Neutral-Point Clamped
PCB	Printed Circuit Board
PE	Protective Earth
PES	Power Electronic Systems Laboratory
PFC	Power Factor Correction
PHSW	Partial-Hard Switching
PMSM	Permanent Magnet Synchronous Motor
PSPWM	Phase-Shifted PWM
PV	Photovoltaic
PWM	Pulse Width Modulation

R_{dson}	on-state resistance
RMS	Root Mean Square
Si	Silicon
SiC	Silicon-Carbide
SPBI	Stacked Polyphase Bridge Inverter
SSW	Soft Switching
SMD	Surface-Mount Device
SVPWM	Space Vector PWM
THD	Total Harmonic Distortion
TIM	Thermal Interface Material
VSD	Variable Speed Drive
VSI	Voltage Source Inverter
WBG	Wide Bandgap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

Contents

1 Introduction

The constant need to boost productivity in industry, fueled by competitive pressures and emphasized by a shortage of workers leads to an increasing degree of automation in modern industrial manufacturing and warehouse processes [1, 2]. Thereby, Variable Speed Drives (VSDs) supplying, e.g., high-performance servo motors are ubiquitous, as they enable accurate control of position, speed and torque while achieving high total system efficiencies, which comply with the current interest in sustainable production and energy savings [3].

Typically, such a VSD system is realized as a standalone three-phase inverter combined with an active/passive front-end rectifier stage and is accommodated in a dedicated cabinet. The motor itself is connected to the VSD over a shielded power cable (length of up to several meters) to confine conducted and radiated Electromagnetic Interference (EMI) emissions that originate from the Pulse Width Modulation (PWM) voltages of the inverter. This system arrangement provides high flexibility in the selection and combination of individual components and allows the placement of the power electronics in a convenient environment at some distance from the motor. However, shielded motor cables are expensive [4], considerably heavier [5], and are at risk of being incorrectly connected during commissioning [6]. Moreover, they lead to additional voltage stresses on the insulation of the motor windings due to overvoltages caused by voltage reflections at the motor terminals (i.e., transmission line effects) [7].

Said voltage reflections in motor cables are accentuated even further with the adoption of Wide Bandgap (WBG) semiconductor devices, i.e., Silicon-Carbide (SiC) and Gallium-Nitride (GaN) power transistors. While they are a promising alternative to the state-of-the-art Si-IGBTs thanks to their reduced switching losses and improved on-state performance, they also introduce

significantly increased switching speeds of 20 … >50 V/ns, which lead to detrimental voltage reflections even for short motor cables [8].

Accordingly, there has been a growing trend towards drive systems with motor-integrated inverters, so-called *Integrated Motor Drives (IMDs)*, which largely eliminate the requirement of complex shielded wiring. Thanks to the arrangement of the machine and drive electronics in the same enclosure a simple and compact installation of the system is possible [9, 10]. While IMD concepts are not a novel invention [11], in recent years various IMDs have been commercialized, showcasing potential reductions in the total volume of 10%–20%, and overall cost reductions in installation and manufacturing of up to 30%–40% compared to equivalent separately arranged drive systems [12].

Expedient for motor integration, an increasing interest from industry in distributed *DC-Link supply grids* has emerged (e.g., with DC-Link voltages of up to 800 V to lower the DC-cabling cross-section) [13]. In this configuration, several independent drives operate on a common DC bus, allowing a direct energy exchange of accelerating and braking motors over local DC energy storage elements and thus improving the total system efficiency. The active/passive rectifier front-end, which was previously required for each drive separately, is replaced with a central bidirectional Power Factor Correction (PFC) rectifier unit for connection to the AC mains. The resulting lower number of components of the drive itself (i.e., only the inverter) strongly facilitates the direct integration into the motor [14].

1.1 Challenges

Motor-integration of the inverter stage poses several challenges to the power electronics field [9, 15–18], three out of which are a major focus of this work:

- **Limited Space for the Power Electronics**
  Inevitably, the arrangement of the power electronics in the same housing as the motor imposes significant limitations on the available mounting area and volume for the inverter stage. For instance, in order to facilitate compatibility with existing industrial system installations, the specific motor frame size (and thus indirectly also the diameter) of a given motor should be retained despite drive integration (e.g., adhering to the NEMA frame size [19]). As a result, a compact design for the IMD necessitates a high power density (ρ) of the inverter stage.

- **Elevated Motor Temperatures**
  Placing the power electronics in close proximity to the motor comes at

the cost of potentially higher operating temperatures of the semiconductors and the other electronic components. Given that the motor is the primary heat source (e.g., typical electric motor efficiencies range from 90-95%), the ambient temperature of the inverter stage is increased, especially when opting for a more compact integration without a thermal barrier between the power electronics and the motor. Consequently, in order to limit further self-heating (and/or additional cooling effort) of various power electronic components in the motor-loss-dominated environment, high inverter efficiencies η (e.g., >99%) are required.

- **Short-Term Overload Capability**
  VSDs are exposed to application-specific mission profiles. For instance, servo drives include the requirement for providing transient *overload* torques, e.g., during acceleration or braking operation, which exceed the nominal operation torque typically by a factor of two to three for several seconds [20].
  Compared to the electronic components of the inverter stage, the motor itself is not significantly affected by the high transient current stresses thanks to its large iron/copper mass, which results in a large thermal time constant (i.e., several tens of minutes for servo motors in the single-digit kilowatt power range [21]). On the other hand, the electronic components are orders of magnitudes smaller and consequently have considerably smaller thermal time constants in the range of several milliseconds. For the power transistors in particular, the short-term increase of conduction and switching losses in combination with the already high ambient operating temperature in the vicinity of the motor can lead to critical semiconductor junction temperatures close to their respective maximum ratings.
  As a consequence, not only nominal inverter efficiency must be high, but also the expected short-term overload losses must be limited and an adequate (transient) cooling capability must be provided in the IMD design.

The above-addressed challenges can advantageously be tackled utilizing *WBG* devices: With their improved switching and conduction losses, they achieve higher efficiencies and enable higher power densities, e.g., the cooling effort is reduced and higher possible switching frequencies minimize the DC-Link capacitor volume [15]. Furthermore, if not impaired by their packaging, they can operate with high junction temperatures (>300 °C in theory), which

makes them especially well-suited for high-temperature environments such as in an IMD [22].

However, as mentioned, these benefits of WBG devices come at the cost of increased switching speeds (i.e., high $\mathrm{d}v/\mathrm{d}t$), which imposes various challenges despite the omitted cable in an IMD. For example, now, the overvoltages due to voltage reflections in the motor cable can also occur inside the stator winding itself [23, 24]. As a result, the uneven voltage distribution over the windings potentially leads to premature insulation aging and partial discharge, impairing the overall lifetime of the motor [25].

Improving Motor-Friendliness

Besides the high switching speeds, in general, the PWM voltages generated from the inverter are not ideal for the motor [26–28]. Hence, there is a strong incentive to *protect the motor* from the power electronic stage:

- *dv/dt-Filter:* Current standards allow a $\mathrm{d}v/\mathrm{d}t$ at the motor terminals in the range of 3...6 V/ns to restrain the uneven voltage distributions in the windings caused by high switching speeds [19, 29]. Consequently, dedicated small (active or passive) filter structures can be employed limiting the switching speed of WBG inverters according to the standards [30]. However, these filter structures have their cutoff frequency above the inverter switching frequency, and hence, they do not suppress switching frequency Common Mode (CM) and/or Differential Mode (DM) components of the inverter PWM voltages.

- *DM-Filter:* This type of filter provides sinusoidal line-to-line voltages to the motor terminals, leading to sinusoidal phase currents for an open star-point winding configuration, and hence, mitigates HF motor losses [31, 32]. However, the CM voltage components (inclusive CM $\mathrm{d}v/\mathrm{d}t$) are not mitigated by this filter, which, e.g., leads to ground leakage currents, CM EMI emissions and CM voltages over the motor bearings. The latter can cause Electric Discharge Machining (EDM) bearing currents that damage the motor bearings [33].

- *CM-Filter:* By reducing the CM voltage at the motor terminals the above mentioned CM problems can be mitigated. For this purpose, there are active CM filters, which inject a CM compensation voltage [34, 35], and passive CM filters (i.e., a CM choke with DC-side referenced filter capacitors), which, however, are only used as combined CM and DM filter [32, 36]. Alternatively, when a CM choke is introduced between

inverter and motor without additional capacitive filter elements, the main focus is generally to attenuate the parasitic CM currents in the system, i.e., reducing conducted CM EMI emissions [37, 38].

- *Full Sine-Wave LC Output Filter (DM/CM-Filter):* The installation of a DC-side referenced *LC* output filter fully shields the motor from the PWM voltages of the inverter stage [32]. This not only eliminates harmful $\mathrm{d}v/\mathrm{d}t$-effects but also suppresses the build-up of CM voltage over the motor bearings, and thus prevents it from EDM damages [31]. Moreover, Low-Frequency (LF) CM resonances, which can be excited in the motor independently of the switching speeds [23], are eliminated, as are any High-Frequency (HF) losses in the motor. The latter helps to increase the overall system efficiency (i.e., of motor and WBG drive with output filter combined) compared to a standard IGBT drive system without an output filter [28, 39].

Targeting high power densities, the filter volume must be minimized. Considering the sine-wave *LC* output filter for maximum motor-friendliness, the filter cutoff frequency can be selected relatively high for WBG devices—thanks to the high possible switching frequencies—which accordingly enables compact filter designs [28]. Nevertheless, for conventional two-level inverter systems, the filter size still dominates the overall inverter volume and thus limits the achievable power density [40].

Multi-Level (ML) Inverters

This motivates the use of *Multi-Level (ML)* inverter concepts, as they offer advantages such as:

- multiple voltage levels at the switch node of ML bridge-legs, which helps to more closely approximate the desired sinusoidal output voltage waveform, and hence, reduces the required output filter volume,
- an increased effective switching frequency (f_{eff}, for certain ML topologies)—relevant to output filtering—for a given device switching frequency (e.g., in Flying Capacitor (FC) inverters),
- a lower switched voltage of each power semiconductor, resulting in lower switching losses per device, and thus facilitating passive cooling over natural convection,

- the possibility to employ lower voltage power semiconductors, offering an improved device level Figure-of-Merit (FOM) and thus leading to a further increase in system efficiency [41].

Nonetheless, there is a clear trade-off between the reduced filter volume and increased efficiency in ML inverters on the one side, and the resulting higher number/volume of semiconductors, gate drives, and the overall increased complexity compared to standard 2L inverters on the other side.

1.2 Aims and Contributions

This thesis evaluates different ML inverter concepts in order to achieve a high power density ρ, a high efficiency η, and a high short-term overload capability required for IMD systems in, e.g., servo applications. Acknowledging the high variety of application scenarios of IMDs, spanning various power, torque, and supply voltage ranges, the present thesis considers an exemplary 7.5 kW ML inverter design for driving a Permanent Magnet Synchronous Motor (PMSM) with a nominal speed of 4500 rpm and $p = 4$ pole pairs. Thereby, the specifications of **Table 1.1** apply. However, note that many aspects discussed in this thesis are also applicable to IMDs operating within other power, torque, and voltage ranges.

Tab. 1.1: Specifications for the analyzed Integrated Motor Drive (IMD).

Parameter		Value
DC-Link Voltage	V_{DC}	800 V
Nominal Output Power	P_{nom}	7.5 kW
Nominal Peak Output Voltage Amp.	$v_{\mathrm{out,nom}}$	330 V
Nominal Peak Phase Current Amp.	$i_{\mathrm{out,nom}}$	15 A
Overload Peak Phase Current Amp.	$i_{\mathrm{out,OL}}$	45 A
Overload Duration	t_{OL}	3 s
Inverter Output Frequency Range	f_{out}	$0 - 300$ Hz
Min. Nominal Inverter Efficiency	$\eta_{\mathrm{nom,min}}$	99 %
Motor Case (Ambient) Temperature	T_{case}	90 °C
Cooling System		Natural Conduction

- In a first step, a preliminary study on the optimal level number N in an IMD with sine-wave LC output filter is conducted. The focus of this study presented in **Chapter 2** lies on the Flying Capacitor inverter (FCi) topology, where either GaN power transistors or Si MOSFETs can be

utilized for the given 800 V DC-Link voltage. Based on a simple semiconductor FOM, a higher number of levels N is identified as especially beneficial for semiconductor technologies with poor performance at higher voltages (i.e., Si MOSFETs), while for implementation with GaN devices a lower N yields a promising $\eta\rho$-performance. In the end, when considering the available semiconductors on the market, a 7L-FCi for Si and a 3L-FCi for GaN can be identified as the most promising IMD candidates.

- With the most promising level numbers determined, in **Chapter 3**, possible IMD realizations for the 7L Si and 3L GaN FCi are evaluated, which provide the required short-term overload capability. Anticipating similar power densities for a 99% nominal target efficiency, the significantly less complex 3L-FCi design is realized. A dynamic transient thermal model is employed to analyze the overload capability, and the expected performance is experimentally confirmed for nominal and overload operation.

- Expanding the analysis beyond purely FCi topologies to include other alternatives in combination with an LC output filter, the previously dismissed 7L inverter can be advantageously realized as 7L-Hybrid Active Neutral-Point Clamped Converter (7L-HANPC) with reduced complexity. Accordingly, **Chapter 4** undertakes a comprehensive hardware-based comparison involving the 7L Si FCi, the 7L-HANPC (Si and GaN), and the 3L GaN FCi. This evaluation encompasses crucial aspects related to mechanical realization, control effort, and overload capability, all based on realized hardware and measurements. Ultimately, the findings reveal that the 3L GaN FCi offers the best overall trade-off for the IMD under consideration.

- In **Chapter 5**, the investigation is extended to an alternative topology with identical semiconductor effort as the 3L GaN FCi. By reconfiguring the considered PMSM from a single three-phase winding machine to a dual three-phase winding machine, the same semiconductors can be used for a realization of a Stacked Polyphase Bridge Inverter (SPBI), specifically a converter system formed by two Series-Stacked Two-Level three-phase Converter (2L-SSC) systems. Advantageously, this topology does not require any Flying Capacitors and, moreover, provides a straightforward CM cancellation capability. Hence, a thorough comparison of the 2L-SSC and the 3L-FCi is presented in this chap-

ter, considering a design with CM choke only and a design with full sine-wave *LC* output filter.

1.3 List of Publications

Key insights presented in this thesis have already been published in international scientific journals, conference proceedings, or presented at workshops. The publications created as part of this thesis, or also in the scope of other related projects, are listed below.

1.3.1 Journal Papers

- **G. Rohner**, T. Gfrörer, P. S. Niklaus, D. Bortis, M. Schweizer, and J. W. Kolar, "Comparative Evaluation of Three-Phase Three-Level GaN and Seven-Level Si Flying Capacitor Inverters for Integrated Motor Drives Considering Overload Operation," in *IEEE Access*, vol. 4, no. 1, pp. 7356-7371, 2024. DOI: 10.1109/ACCESS.2024.3350728.
- **G. Rohner**, T. Gfrörer, P. S. Niklaus, J. Huber, D. Bortis, M. Schweizer, and J. W. Kolar, "Hardware-Based Comparative Analysis of Multilevel Inverter Topologies for Integrated Motor Drives Considering Overload Operation," in *IEEE Open Journal of Power Electronics*, vol. 4, no. 1, pp. 2644-1314, 2023. DOI: 10.1109/OJPEL.2023.3327423.
- **G. Rohner**, J. Huber, S. Mirić, and J. W. Kolar, "Comparative Evaluation of Three-Phase Three-Level Flying Capacitor and Stacked-Bridge Polyphase GaN Inverter Systems for Integrated Motor Drives," in *Electronics*, vol. 13, no. 7: 1259, 2024. DOI: 10.3390/electronics13071259.

1.3.2 Conference Papers

- **G. Rohner**, S. Mirić, D. Bortis, M. Schweizer, and J. W. Kolar, "Comparative Evaluation of Overload Capability and Rated Power Efficiency of 200V Si/GaN 7-Level FC 3-Φ Variable Speed Drive Inverter Systems," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Phoenix (online), USA, June 2021. DOI: 10.1109/APEC42165.2021.9487125.
- **G. Rohner**, D. Bortis, M. Schweizer, and J. W. Kolar, "Optimal Level Number and Performance Evaluation of Si/GaN Multi-Level

Flying Capacitor Inverter for Variable Speed Drive Systems," in *Proc. of the IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Chiang Mai, Thailand, December 2022. DOI: 10.1109/ICEMS56177.2022.9982999.

1.3.3 Further Contributions

- J. W. Kolar, J. Azurza Anderson, S. Mirić, M. Haider, M. Guacci, M. Antivachis, G. Zulauf, D. Menzi, P. S. Niklaus, J. Miniböck, P. Papamanolis, **G. Rohner**, N. Nain, D. Cittanti, and D. Bortis, "Application of WBG Power Devices in Future 3-Φ Variable Speed Drive Inverter Systems "How to Handle a Double-Edged Sword"," in *Proc. of the IEEE International Electron Devices Meeting (IEDM)*, San Francisco, USA, December 2020. DOI: 10.1109/IEDM13553.2020.9372022.

- S. Mirić, R. Giuffrida, **G. Rohner**, D. Bortis, and J. W. Kolar, "Design and Experimental Analysis of a Selfbearing Double-Stator Linear-Rotary Actuator," in *Proc. of the IEEE International Electric Machines & Drives Conference (IEMDC)*, Hartford, USA, Mai 2021. DOI: 10.1109/IEMDC47953.2021.9449501.

- D. Bortis, **G. Rohner**, and J. W. Kolar, "Wide-Band-Gap-Antriebsumrichter: Aktuelle Trends und Technische Lösungen," presented at the *VDE DACH-Fachtagung "Elektromechanische Antriebssysteme 2021"*, online, November 2021. DOI: not available.

- M. Haider, P. S. Niklaus, M. Madlener, **G. Rohner**, and J. W. Kolar, "Comparative Evaluation of Gate Driver and *LC*-Filter Based dv/dt-Limitation for SiC-Based Motor-Integrated Variable Speed Drive Inverters," in *IEEE Open Journal of Power Electronics*, vol. 4, no. 1, pp. 450-462, 2023. DOI: 10.1109/OJPEL.2023.3283052.

2

Optimal Level Number and Performance Evaluation of Si/GaN Multi-Level Flying Capacitor Inverter for Variable Speed Drive Systems

This chapter summarizes the most relevant findings of a preliminary study evaluating the optimal level number in a Multi-Level IMD also published in:

- **G. Rohner**, D. Bortis, M. Schweizer, and J. W. Kolar, "Optimal Level Number and Performance Evaluation of Si/GaN Multi-Level Flying Capacitor Inverter for Variable Speed Drive Systems," in *Proc. of the IEEE International Conference on Electrical Machines and Systems (ICEMS)*, Chiang Mai, Thailand, 2022.

Motivation

ML topologies such as the Flying Capacitor inverter (FCi) offer a known benefit in semiconductor loss and output filter size reduction. However, for higher level numbers also Gate Drivers, PCB overhead, and FC volume increase. Consequently, the optimal level number concerning overall efficiency and power density for a possible IMD implementation with Si and GaN semiconductor technology must be evaluated.

Executive Summary

This chapter analyzes the optimal number of voltage levels concerning power density for a motor-integrated Multi-Level Flying Capacitor inverter (ML-FCi) with 800 V DC-Link driving a 7.5 kW PMSM. The analysis is performed for an ML-FCi, as it enables high efficiency and power density required for motor integration on the one hand and decreases the output filter volume with increasing output voltage level numbers N on the other hand. General scaling laws of the ML-FCi are derived analytically and a Pareto optimization based on real hardware dimensions is performed to determine which number of levels is optimal in terms of power density and efficiency and which system performance is achieved for employing Si or GaN power transistors.

2.1 Introduction

Targeting a three-phase inverter with full sine-wave *LC* output filter suitable for motor integration, high power density ρ and high-efficiency η are of paramount importance. Thereby, utilizing ML topologies offers several advantages: On the device level, lower voltage power semiconductors with an improved FOM can be used, thus leading to increased system efficiencies. Moreover, on the topology level, multiple output voltage levels allow a closer approximation of the ideally sinusoidal output voltage waveform, reducing the required *LC* filter volume.

The main classes of ML inverter topologies are identified as Cascaded H-Bridge (CHB), Neutral-Point Clamped (NPC) and FC inverters [42], which have been studied and compared in literature for various applications [43, 44]. Thereby, targeting a motor drive application with *LC* output filter, the FC offers an increased effective switching frequency (i.e., the switching frequency measured at the switch node is a multiple of the device switching frequency), which reduces the *LC* output filter volume even further compared to the mentioned alternatives. Furthermore, it provides DC operation capability to generate a motor standstill torque.

However, there are realizations of the same topology with different numbers of levels N for a similar DC-Link voltage specification, e.g., the FCi operated with an input voltage of 800-1000 V can be found as 3L [45], 5L [46], 7L [47], 9L [48], 10L [49] or even 13L [50] implementation. Naturally, this raises the question about the optimal number of levels of such an ML-FCi in terms of efficiency η and power density ρ. Differently to the aforementioned volume

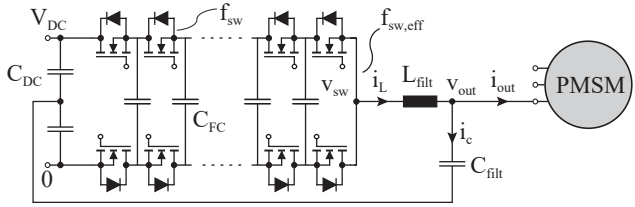


Fig. 2.1: Single bridge-leg of a three-phase Multi-Level Flying Capacitor inverter (ML-FCi) (i.e., with N output voltage levels) with full sine wave LC output filter driving a three-phase PMSM.

reduction of the output filter, a higher number of levels results in higher complexity, i.e., a higher number of switches, gate drivers, FCs, measurement and control circuits, and accordingly in a potentially larger converter volume as also shown in [51].

In this preliminary study, the optimal number of levels is determined for a motor integrated ML-FCi (cf. **Fig. 2.1**), first in a general form based on scaling laws and then using the example of an 800 V DC-Link 7.5 kW VSD system with *nominal* specifications as given in **Table 1.1**.
In **Section 2.2** the general scaling of the power transistors, the FCs and the LC output filter stage is derived for an ML-FCi as a function of the number of levels N. In a first step, N-independent constant total semiconductor losses $P_{\text{semi,tot}}$ are assumed, which are equally divided into conduction losses $P_{\text{cond,tot}}$ and switching losses $P_{\text{sw,tot}}$. The analysis could also be performed for an arbitrary loss distribution, i.e. $P_{\text{cond,tot}} = s \cdot P_{\text{semi,tot}}$ where $s = [0...1]$. In **Section 2.3**, these assumptions are withdrawn and, based on the *nominal* specifications of **Table 1.1**, a Pareto optimization is performed for an ML-FCi with respect to achievable efficiency η and (volumetric) power density ρ for different numbers of levels N. It is also investigated which N is optimal for the realization of the ML-FCi based on Si MOSFETs and GaN power transistors, whereby an implementation with discrete components and a fully integrated, chip-based realization are considered. Finally, **Section 2.4** concludes the chapter.

2.2 Multi-Level Component Scaling

2.2.1 Power Semiconductors

Compared to a 2L inverter, the DC-Link voltage in an N-level inverter is divided equally among $(N-1)$ power semiconductors connected in series. Thus, as the number of levels N increases, the voltage V_B to be blocked by each semiconductor decreases with $1/(N-1)$, i.e. $V_B(N) = V_{DC}/(N-1)$. Depending on the application, V_B is typically set to about $50-70\,\%$ of the specified device blocking voltage V_{rated}. In the following analysis, for V_B a safety factor of $k_s = 3/2$ is assumed, which results in a required N-dependent maximum voltage blocking capability V_{rated} (cf. **Fig. 2.3 (a)**) as

$$V_{rated}(N) = k_s \cdot V_B(N) = k_s \cdot \frac{V_{DC}}{N-1}. \tag{2.1}$$

However, due to the series connection of the $(N-1)$ semiconductors, the total on-state resistance of one bridge-leg and/or phase $R_{dson,tot}$ increases proportionally with the on-state resistance of a single switch R_{dson} and with the increasing level number N as $R_{dson,tot}(N) = (N-1) \cdot R_{dson}$. Under the above mentioned assumption of constant and N-independent semiconductor losses $P_{semi,tot}$ (and equal partitioning into conduction and switching losses), this means that for constant conduction losses per bridge leg ($P_{cond,tot} = R_{dson,tot} \cdot I^2_{out,eff}$), the same total on-state resistance $R_{dson,tot}$ must be achieved in an N-level inverter as in a 2L inverter. Thus in an N-level inverter the on-state resistance per switch R_{dson} to be achieved (cf. **Fig. 2.3 (a)**) must decrease with increasing number of levels N by factor of $1/(N-1)$,

$$R_{dson}(N) = \frac{R_{dson,tot}}{(N-1)}. \tag{2.2}$$

This on-state resistance R_{dson} must be achieved at nominal junction temperature T_j, which according to **Table 1.1** for the underlying application at least equals the ambient temperature $T_j = T_{amb} = 90\,^\circ\mathrm{C}$. Consequently, the R_{dson} typically specified in datasheets at $T_j = 25\,^\circ\mathrm{C}$ must be selected even smaller. For the considered case of $90\,^\circ\mathrm{C}$, the on-state resistance of Si and GaN increases according to $R_{dson}(90\,^\circ\mathrm{C}) = k_T \cdot R_{dson}(25\,^\circ\mathrm{C})$ approximately by a factor of $k_T = 1.5$.
Furthermore, assuming that semiconductor technology and blocking voltage capability of the used devices remain unchanged, a reduction in on-state resistance $R_{dson}(N)$ according to (2.2) would require the die area A_{die} of each switch to increase linearly with N. However, the required blocking voltage

Tab. 2.1: Power semiconductor technology fitting parameters given such that all quantities concerned (e.g. R_{dson}, A_{die}, V_{rated}, $C_{\text{oss,Q}}$, FOM) result in SI units.

Parameter	Si	GaN
k_{R}	$4.8 \cdot 10^{-13}$	$0.26 \cdot 10^{-9}$
α_{R}	2.5	1.1
k_{C}	$2.4 \cdot 10^{-1}$	$2.7 \cdot 10^{-3}$
α_{C}	-1.6	-0.7
k_{FOM}	$8.68 \cdot 10^{12}$	$1.42 \cdot 10^{12}$
α_{FOM}	-0.9	-0.4

V_{rated} decreases according to (2.1) with $1/(N-1)$, which results in a lower on-state resistance R_{dson} for the same die area A_{die} as derived in [41]. The on-state resistance R_{dson} at 25 °C of a single switch scales with rated voltage as

$$R_{\text{dson}} = \frac{k_{\text{R}} \cdot V_{\text{rated}}^{\alpha_{\text{R}}}}{A_{\text{die}}}, \tag{2.3}$$

where the technology-specific constant k_{R} and the voltage-scaling factor α_{R} represent material parameters and are listed in **Table 2.1** for Si and GaN power transistors.
As a result, $\alpha_{\text{R}} >> 1$ implies that for a constant A_{die} the on-state resistance R_{dson} decreases even more than with $1/(N-1)$ as required in (2.2), which is e.g. the case for Si devices. Conversely, by substituting (2.2) into (2.3), the required chip area per switch A_{die} or the total chip area of a bridge-leg and/or phase of the inverter $A_{\text{die,tot}}$ can be calculated as

$$A_{\text{die}}(N) = \frac{k_{\text{R}} \cdot V_{\text{rated}}(N)^{\alpha_{\text{R}}}}{R_{\text{dson}}(N)} \propto (N-1)^{1-\alpha_{\text{R}}} \tag{2.4}$$

and

$$A_{\text{die,tot}}(N) = 2(N-1) \cdot A_{\text{die}}(N) \propto (N-1)^{2-\alpha_{\text{R}}}. \tag{2.5}$$

It can be seen that for a Si inverter and constant total on-state resistance $R_{\text{dson,tot}}$, the chip area per switch A_{die} as well as the total chip area of the Si inverter $A_{\text{die,tot}}$ decrease with increasing level number N (cf. **Fig. 2.3 (b)** and **(c)**). For GaN with $\alpha_{\text{R}} = 1.1 \approx 1$, however, although A_{die} decreases slightly with increasing N, $A_{\text{die,tot}}$ of the GaN inverter increases quasi linearly with N. When assuming constant costs per chip area [\$/cm^2], a proportional scaling of the semiconductor costs with $A_{\text{die,tot}}$ results. Thus for a Si inverter the costs decrease with increasing N, but are increasing for a GaN-based realization. If

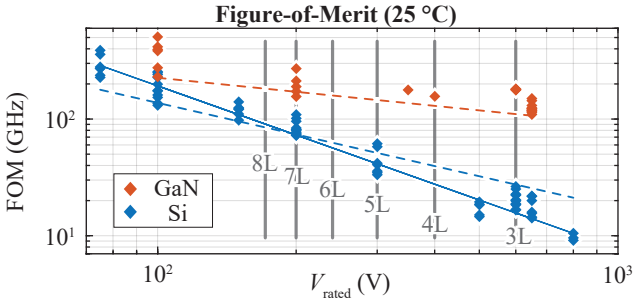


Fig. 2.2: FOM for latest commercially available Si and GaN power transistors for the R_{dson} at 25 °C and $C_{\text{oss,Q}}$ at $1/k_{\text{s}} = 2/3$ of the rated voltage V_{rated}. Dashed trend lines are derived with (2.8) using the parameters given in **Table 2.1**. For Si an alternative solid trend line is proposed for later use in the Pareto optimization. This helps not to overestimate devices with higher voltage ratings, as these additionally suffer from high Q_{rr} losses compared to the lower voltage semiconductors, an effect not captured by the FOM. The thick gray lines indicate the minimum semiconductor blocking voltage $V_{\text{rated}}(N)$ required for the different numbers of levels N considering $k_{\text{s}} = 3/2$ as safety factor.

it is additionally considered that the costs per chip area decrease with lower blocking voltages V_{rated}, then the costs again scale proportionally with A_{die}, i.e. for Si a strong cost reduction with increasing N can be expected, while the costs for GaN remain almost constant or only slightly decrease with N.

One would also expect the charge-equivalent output capacitance of a switch $C_{\text{oss,Q}}$ to decrease with a smaller A_{die}. However, since the semiconductor can be designed for a lower rated voltage V_{rated}, the expected $C_{\text{oss,Q}}$ increases with lower V_{rated} or with increasing level number N (cf. **Fig. 2.3 (d)**) as

$$C_{\text{oss,Q}}(N) = k_{\text{C}} \cdot V_{\text{rated}}(N)^{\alpha_{\text{C}}} \cdot A_{\text{die}}(N) \propto (N-1)^{1-\alpha_{\text{R}}-\alpha_{\text{C}}} = (N-1)^{1+\alpha_{\text{FOM}}}. \quad (2.6)$$

The technology-specific constant k_{C} and the voltage-scaling factor α_{C} listed in **Table 2.1** were determined empirically in [41] considering $C_{\text{oss,Q}}$ at 2/3 V_{rated}.

The voltage-dependent $C_{\text{oss,Q}}$ is an important parameter for the choice of semiconductors, because while the on-state resistance R_{dson} determines the conduction losses P_{cond}, $C_{\text{oss,Q}}$ together with the switching frequency f_{sw} defines the minimum hard-switching losses for Zero Current Switching (ZCS)

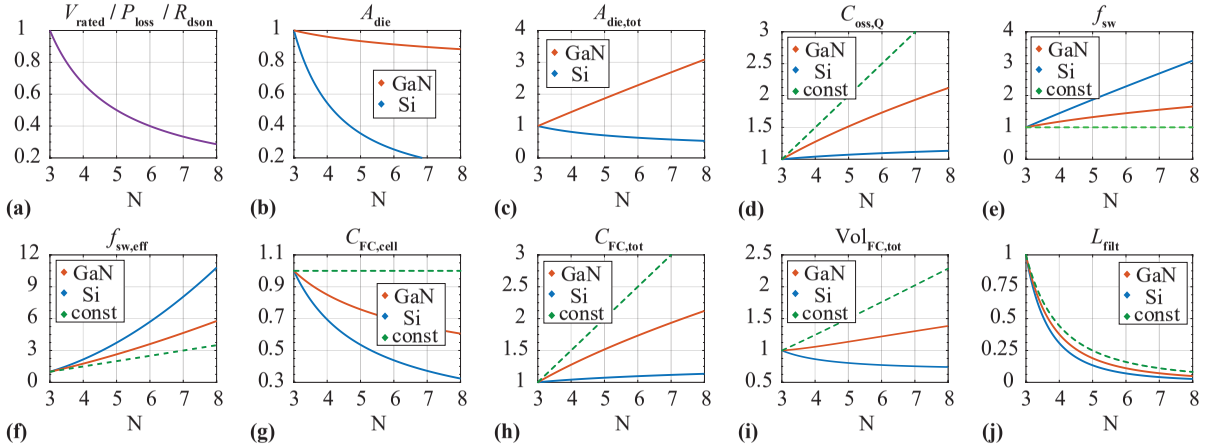


Fig. 2.3: Scaling of the different characteristic quantities in an ML FCi as a function of the number of levels N according to (2.1) to (2.15) for Si and GaN. The green dashed lines labeled with "const", emulate a semiconductor technology with a constant FOM ($\alpha_{FOM} = 0$), where all semiconductors feature the same and blocking voltage independent FOM as a 600 V power transistor. This illustrates how much the FOM-dependent quantities of an FCi are affected by the topology itself and how much they are influenced by the choice of semiconductor technology. All plots are normalized with the corresponding values of an $N = 3$ design.
For a 99 % semiconductor efficiency at the nominal power and current specified in **Table 1.1** and with equal partitioning in conduction and switching losses for $N = 3$, this results in an R_{dson} of 55.6 mΩ for both semiconductor technologies. The required die area for the same R_{dson} is larger for Si than for GaN with $A_{die,Si} = 114\,mm^2$ and $A_{die,GaN} = 7.98\,mm^2$. The respective charge equivalent output capacitance $C_{oss,Q,Si} = 984$ pF is also larger than $C_{oss,Q,GaN} = 245$ pF, which results in a lower possible switching frequency for Si than for GaN with the same switching losses, i.e., $f_{sw,Si} = 40$ kHz and $f_{sw,GaN} = 159$ kHz.

according to

$$P_{\text{semi,tot}}(N) = P_{\text{cond,tot}} + P_{\text{sw,tot}} = (N-1) \cdot (R_{\text{dson}} \cdot I_{\text{out,rms}}^2 + f_{\text{sw}} \cdot C_{\text{oss,Q}} \cdot V_{\text{B}}^2), \quad (2.7)$$

which along with the smaller current-dependent loss components (V-I overlap losses) - especially for fast current/voltage transitions - account for the largest part of the total switching losses. Therefore, to achieve high efficiencies and/or high switching frequencies, semiconductors with low R_{dson} and $C_{\text{oss,Q}}$ are advantageously used.
In order to compare semiconductors with different on-state resistances R_{dson}, output capacitances $C_{\text{oss,Q}}$, rated voltages V_{rated} and technologies (Si, GaN, SiC), various FOMs have been derived [41, 52, 53], where the simplest FOM is only defined by two mentioned quantities R_{dson} (cf. (2.3)) and $C_{\text{oss,Q}}$ (cf. (2.6)) as

$$\text{FOM} = \frac{1}{R_{\text{dson}} \cdot C_{\text{oss,Q}}} = k_{\text{FOM}} \cdot V_{\text{rated}}^{\alpha_{\text{FOM}}}, \quad (2.8)$$

with $k_{\text{FOM}} = 1/(k_{\text{R}} \cdot k_{\text{C}})$ and $\alpha_{\text{FOM}} = -(\alpha_{\text{R}} + \alpha_{\text{C}})$ defined in [41].
Thus, a high FOM value corresponds to a low $R_{\text{dson}}C_{\text{oss,Q}}$-product or lower semiconductor losses. FOM values of commercially available Si and GaN semiconductor devices are shown in **Fig. 2.2** as a function of rated blocking voltage V_{rated}. In addition, the trend line given by (2.8) is indicated. As already shown in e.g. [41], for Si and GaN power semiconductors, the FOM increases with smaller blocking voltage V_{rated}, i.e., the semiconductor performance increases at lower blocking voltages, especially for Si due to a steeper slope (i.e. more negative α_{FOM}), motivating the choice of a high level number N. Furthermore, the minimum semiconductor blocking voltages $V_{\text{rated}}(N)$ required for the different numbers of levels N are shown with thick gray lines in **Fig. 2.2**. It can be noted that the distances between the indicated lines of V_{rated} become narrower with increasing N, and thus the benefit in terms of improved semiconductor properties also decreases with increasing N. Especially for GaN featuring a relatively flat FOM over V_{rated}, a higher level number reduces the semiconductor losses less effectively.
Nevertheless, neglecting the current-dependent switching losses as in (2.7) for given total switching losses $P_{\text{sw,tot}}$, the maximum possible switching frequency f_{sw} of one switching cell can be determined directly from $C_{\text{oss,Q}}$ according to

$$f_{\text{sw}}(N) = \frac{P_{\text{sw,tot}}}{(N-1) \cdot C_{\text{oss,Q}}(N) \cdot V_{\text{B}}(N)^2} \propto (N-1)^{-\alpha_{\text{FOM}}}. \quad (2.9)$$

As shown in **Fig. 2.3 (e)**, the switching frequency of each switching cell f_{sw} can be increased as the number of levels N increases, but the increase of f_{sw} becomes less and less for higher N, similar to the FOM. However, the effective switching frequency (cf. **Fig. 2.3 (f)**)

$$f_{sw,eff}(N) = (N-1) \cdot f_{sw}(N) \propto (N-1)^{1-\alpha_{FOM}} \tag{2.10}$$

measurable at the switch node still increases with more than $(N-1)$, which is advantageous especially with regard to the *LC* output filter volume, as will be discussed in *Section 2.2.3*.

2.2.2 Flying Capacitors

As thoroughly described in [50] for phase-shifted PWM, the FC of each FC cell, which here also include the DC-Link capacitors for high frequency currents, are sequentially charged and discharged with the load current i_{out}, whereas the duration of the charge and discharge interval actually depends on the converter operating condition. For phase-shifted PWM the worst case charge/discharge duration is found as $\delta T(N) = 1/f_{sw,eff}(N) = 1/((N-1) \cdot f_{sw}(N))$, leading to a worst case change in charge of $\delta Q_{FC}(N) = i_{out,max}/f_{sw,eff}(N)$. The resulting peak-to-peak FC voltage ripple $\Delta V_{FC,pp}(N) = \delta Q_{FC}(N)/C_{FC,cell}$ is either limited by the semiconductor blocking voltage V_{rated} and typically fixed at a certain percentage of $V_B(N)$, i.e., $\Delta V_{FC,pp}(N) = V_B(N) \cdot k_{FC}$ with k_{FC} in the range of k_{FC} =[0...0.2], or is limited thermally by the maximum allowed Root Mean Square (RMS) current in the FCs. Neglecting the latter, the required capacitance per FC cell $C_{FC,cell}$ is given with

$$C_{FC,cell}(N) = \frac{i_{out,max}}{\Delta V_{FC,pp}(N) \cdot f_{eff}(N)} \propto (N-1)^{\alpha_{FOM}}. \tag{2.11}$$

Neglecting the advantage of increasing the switching frequency $f_{sw}(N)$ due to better semiconductor FOM with increasing N, i.e. considering $\alpha_{FOM} = 0$ and thus $f_{sw}(N) = \text{const.}$, the required capacitance per cell $C_{FC,cell}$ remains constant regardless of the chosen N, as derived in [50] and also indicated in **Fig. 2.3 (g)** with the green dashed line. However, considering the actual FOMs of Si and GaN, it can be noted that the required capacitance per cell even decreases with N. Accordingly, since for each cell the same capacitance $C_{FC,cell}(N)$ is required, the total capacitance of a single phase $C_{FC,tot}(N)$ is found as

$$C_{FC,tot}(N) = (N-1) \cdot C_{FC,cell} \propto (N-1)^{1+\alpha_{FOM}}. \tag{2.12}$$

As shown in **Fig. 2.3 (h)**, $C_{\mathrm{FC,tot}}(N)$ increases linearly when $\alpha_{\mathrm{FOM}} = 0$, i.e., $f_{\mathrm{sw}}(N) = \text{const.}$ (green dashed line), however, when the actual FOMs are taken into account, the increase in total capacitance is much smaller, especially for Si.

For the calculation of the corresponding capacitor volume $\mathrm{Vol}_{\mathrm{FC,tot}}(N)$, it must be considered that the FCs of the different cells are operated with different bias voltages, i.e. $V_{\mathrm{FC,n}}(N) = V_{\mathrm{DC}}/(N-1) \cdot n$ with $n = [1...(N-1)]$ (cf. **Fig. 2.1**). As the capacitor voltage rating increases, the dielectric layer thickness increases linearly [54], causing the volumetric capacitance density ρ_{cap} [F/m^3] to decrease. The corresponding scaling can be found under the simple assumption that for a given type of capacitor and a bias voltage doubling, two capacitors are connected in series in order to double the dielectric strength and two in parallel because of the required capacitance, and thus the capacitance density ρ_{cap} decreases quadratically with the rated capacitor voltage $V_{\mathrm{cap,rated}}$, i.e. with the stored energy, as

$$\rho_{\mathrm{cap}} = \frac{k_{\mathrm{cap}}}{V_{\mathrm{cap,rated}}^2}, \tag{2.13}$$

where a certain capacitor technology performance factor k_{cap} is considered. This scaling is verified by analyzing the capacitor density of commercially available ceramic and film capacitor series. The analysis also reveals that the X6S series from TDK shows one of the highest capacitance densities at zero voltage bias, with the empirically fitted value of $k_{\mathrm{cap}} = 6.24 \cdot 10^6$ FV^2/m^3. However, it has to be taken into account that the capacitance of Class II type ferroelectric ceramics strongly decays with increasing bias voltage. For example, the capacitance of the 450 V X6S capacitor (C5750X6S2W225K250KA) drops at rated voltage below $d = 20\,\%$ compared to the rated capacitance measured at zero voltage, thus, in this case, a five times larger capacitance must be installed compared to (2.12) if all capacitors were biased at the rated voltage (i.e. $V_{\mathrm{FC,n}}(N) = V_{\mathrm{cap,rated}}$). Nevertheless, even with derating, X6S capacitors still feature a higher capacitance density than bias-independent CoG ceramics or film capacitors and are thus considered for further analysis. Consequently, in addition to the voltage-dependent nominal capacitance density according to (2.13), a bias-dependent capacitance derating d must also be

taken into account when calculating the total FC volume of a single bridge-leg

$$\mathrm{Vol}_{\mathrm{FC,tot}}(N) = \sum_{n=1}^{N-1} \frac{C_{\mathrm{FC,cell}}(N) \cdot V_{\mathrm{FC,n}}(N)^2}{k_{\mathrm{cap}}} \cdot 1/d \propto (N-1)^{\alpha_{\mathrm{FOM}}-1} \cdot N \cdot (2N-1). \quad (2.14)$$

Assuming again a constant and N-independent switching frequency $f_{\mathrm{sw}}(N)$, the FC volume would increase sharply with N, as shown in **Fig. 2.3 (i)** (green dashed line). However, thanks to the improving FOM with increasing N, the increase in FC volume is weakened for GaN or the FC volume can even be reduced for Si.

2.2.3 Output Filter

The dimensioning of the output filter depends directly on $f_{\mathrm{sw,eff}}(N)$ and the voltage step amplitude $V_{\mathrm{DC}}/(N-1)$ measurable at the switch node of the ML-FCi, since these directly define the necessary filter inductance for a desired maximum peak-to-peak current ripple $\Delta i_{\mathrm{L,pp}}$ as

$$L_{\mathrm{filt}}(N) = \frac{V_{\mathrm{DC}}/(N-1)}{4 \cdot f_{\mathrm{sw,eff}}(N) \cdot \Delta i_{\mathrm{L,pp}}} \propto (N-1)^{\alpha_{\mathrm{FOM}}-2}. \quad (2.15)$$

The corresponding scaling of the output filter inductor $L_{\mathrm{filt}}(N)$ assuming a constant current ripple is shown in **Fig. 2.3 (j)** for Si, GaN, and $f_{\mathrm{sw}}(N) = \mathrm{const.}$. Consequently, selecting a certain current ripple, the output filter inductance $L_{\mathrm{filt}}(N)$ is directly defined. Subsequently, the output filter capacitance $C_{\mathrm{filt}}(N)$ is determined based on the required LC filter attenuation, e.g., to ensure a minimum output voltage quality. However, the choice of L and C is restricted to the following limits:

1. L_{min}: Maximum allowed current ripple $\Delta i_{\mathrm{L,pp}}$.
2. L_{max}: Maximum allowed voltage drop v_{L} across L_{filt} at maximum electrical output frequency $f_{\mathrm{out,max}}$.
3. $C_{\mathrm{min,1}}$: Maximum allowed voltage ripple at the output Δv_{out}.
4. $C_{\mathrm{min,2}}$: Minimum required filter attenuation at $f_{\mathrm{sw,eff}}$, such that $f_{\mathrm{sw,eff}}$ and the filter resonance frequency f_{LC} are well separated.
5. $C_{\mathrm{max,1}}$: Minimal allowed f_{LC} such that $f_{\mathrm{out,max}}$ is not attenuated.
6. $C_{\mathrm{max,2}}$: Maximum reactive current i_{C} for $f_{\mathrm{out,max}}$.

From this, the design with the smallest filter volume can be chosen, which generally coincides with the lowest possible inductance L_{filt}, since the volume of the filter capacitors is negligible in comparison.

2.3 Pareto Analysis and Performance Evaluation

From the simplified analysis conducted up to this point, Si will benefit from a higher number of levels N in terms of power density since the total chip area $A_{\text{die,tot}}$ as well as the filter inductance L_{filt} decrease and the required total flying capacitance $C_{\text{FC,tot}}$ remains almost constant. However, for GaN the trend is not so obvious, since $A_{\text{die,tot}}$ and $C_{\text{FC,tot}}$ increase strongly and only L_{filt} becomes smaller. In order to evaluate the optimal N and achievable system performance over all efficiencies based on physical components and layouts, a $\eta\rho$-Pareto optimization is performed, considering a Si and a GaN based realization of the bridge-legs of the motor-integrated ML FCi with the nominal specifications given in **Table 1.1**. For this purpose, following assumptions were made:

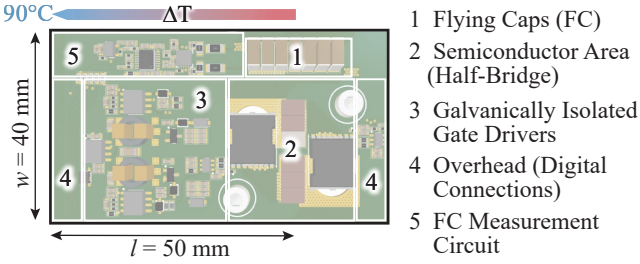


Fig. 2.4: Rendered 3D CAD image of the layout of a FC cell of the motor-integrated 7L FCi prototype power stage with labeling of the main components whose volume is considered in the Pareto optimization. It is assumed that the FC cell is mounted on a copper plate which is laterally attached to the 90 °C motor housing. Thus, the heat is extracted from the semiconductor area (main loss source) to the housing with a maximum allowed $\Delta T = 8\,^{\circ}\text{C}$ along the copper plate.

- The optimization considers a peak-to-peak inductor current ripple $\Delta i_{\text{L,pp}}$ of 80 % from the nominal peak output current $i_{\text{out,nom}}$. The peak-to-peak FC voltage ripple $\Delta V_{\text{FC,pp}}$ is limited to 15 % of $V_{\text{B}}(N)$.
- Additional volumes for, e.g., gate drivers, measurement circuits and electrical signal connections are taken into account according to the layout of a 7L FCi cell shown in **Fig. 2.4** for a motor-integrated prototype with 200 V Si switches. The required heatsink volume is calculated based on the assumption that a single FCi cell is mounted on a copper

plate, which is laterally attached to the 90 °C motor housing. As the width w and length l of the copper plate are given by the FCi cell layout, the thickness of the copper plate with a thermal conductivity of $\lambda = 394\,\mathrm{W/mK}$ is adjusted to achieve a maximum temperature difference of $\Delta T = 8\,°\mathrm{C}$ along the plate up to the semiconductor area, where the majority of the losses originate (cf. **Fig. 2.4**).Any additional mechanical structures for mounting are not considered in the optimization.

- The FCs (including the high-frequency DC-Link capacitors) are realized with the already mentioned 450 V X6S capacitors. Additionally, the losses of the FCs are calculated from the RMS current as proposed in [55], and in case the maximum rated capacitor operating temperature is exceeded, the capacitance value is increased accordingly.
- The volume and losses of the output filter inductor L_{filt} are calculated with a design script that uses toroidal powder cores with soft saturation characteristics and low losses at high frequencies (KoolMu HF from Magnetics [56]).

The resulting Pareto fronts for a 3L to 8L FCi employing either Si or GaN semiconductors and featuring the FOMs discussed in *Section 2.2.1* are shown in **Fig. 2.5 (a)**. It is noted that for both semiconductor technologies, the efficiency increases with higher numbers of levels because low-voltage semiconductors with an improved FOM can be used, resulting in lower switching and conduction losses. Furthermore, regardless of the selected number of levels, the power density can be increased by selecting a higher switching frequency f_{sw}, since the volumes of passive components (FCs and output filter) are reduced. However, due to higher switching losses, this comes at the cost of lower efficiency, even though the Pareto optimization tries to counteract this increase by selecting semiconductors with smaller die areas, i.e., smaller $C_{\mathrm{oss,Q}}$, because at the same time, this leads to larger conduction losses due to a larger R_{dson}.
Higher switching frequency also results in a larger heatsink volume (thicker copper plate), which compensates for the volume reduction of the passive components at the maximum achievable power density. In addition, the volume reduction of the inductor stagnates at this point, since it is limited either thermally by a higher core loss density or mechanically by, e.g., a minimum wall thickness of 3 mm.
The Pareto-optimal designs with the highest power density at a minimum efficiency of 99 % (dots in **Fig. 2.5 (a)**) are compared in terms of volume **Fig. 2.5 (b)** for different numbers of levels N. The semitransparent volume bars for Si

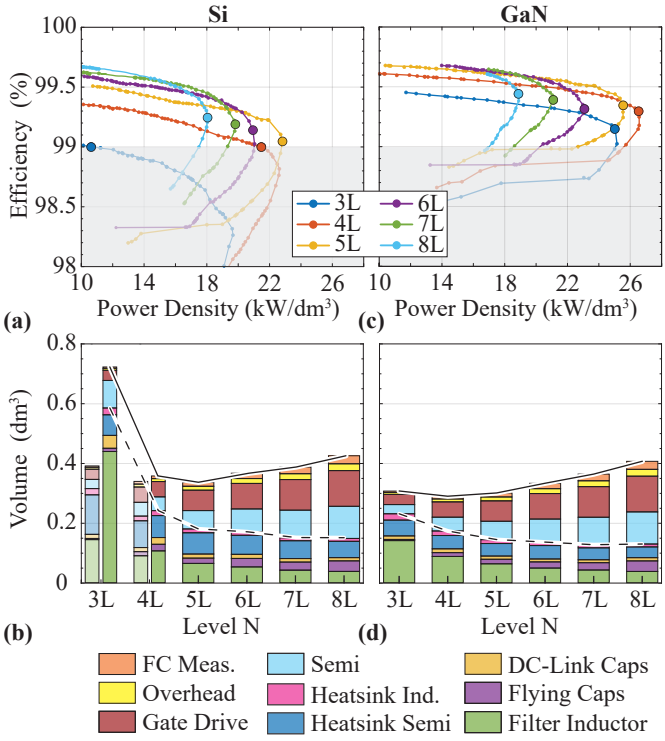


Fig. 2.5: (a) Pareto fronts of 7.5 kW 3L-8L FCIs employing virtual FOM-based semiconductors with appropriate voltage rating $V_{\text{rated}} = 3/2 \cdot V_{\text{B}}$ in either Si or GaN technology. **(b)** Overall volume distribution of Pareto-optimal designs with maximum power densities and efficiencies higher than 99 % (dots) considering a hardware realization with discrete components. The semitransparent volume bars for Si show the volume distribution for the Pareto-optimal designs with maximum power densities which do not reach the 99 % efficiency target. In addition, the dashed line indicates the overall volume obtained for the adoption of a fully integrated design, where the semiconductors, gate drives and measurement circuits are housed in a single package with negligible volume and/or integrated directly in the Printed Circuit Board (PCB).

show the volume distribution of the Pareto-optimal designs with maximum power density, which however do not reach the 99 % efficiency level.
For both semiconductor technologies, it can be seen that the efficiency achieved for the Pareto-optimal design with maximum power density increases with the number of levels N. However, apart from a Si 3L design, this efficiency improvement leads to an almost constantly increasing total FCi volume, i.e., with a Si 5L FCi and a GaN 4L FCi the highest power density is achieved if a realization with discrete devices and components is considered. For GaN, it can be further observed that already for the GaN 3L FCi a high power density and a similar overall volume as for the 4L FCi is obtained. This can be explained by the fact that for GaN already at $N = 3$ a high switching frequency can be selected, resulting in an inductor volume that is already smaller than the volume occupied by the half-bridges, gate drives and measurement circuits. Thus, as N is further increased, these volumes increase more than what can be saved with a smaller inductor volume, resulting in an overall optimal 4L FCi design for GaN.

In contrast, for Si and considering the 99 % efficiency target, the inductor volume strongly dominates the overall FCi volume for $N = 3$. Therefore, with a higher number of levels N, this dominant volume fraction is greatly reduced and the total volume reaches its minimum at $N = 5$. For higher N, the volume shares of the half-bridges, gate drivers and measuring circuits start to dominate and the total volume increases accordingly.
Nevertheless, considering now a suitable realization of the optimal 4L GaN FCi, it is found that there are no commercially available 400 V GaN switches which would be required for an $N = 4$ design. Therefore, the same semiconductors as for an $N = 3$ would have to be used (e.g., blocking voltages around 600 V/650 V), which would shift the Pareto front to lower efficiencies and power densities. For the same reason, a strong shift of the Pareto fronts for $N = 5$ and 6 can be observed for GaN, where currently only 200 V and 600 V/650 V switches are available on the market which also offer a greater variety of R_{dson} values. With these considerations, the optimal feasible design for GaN results in a 3L FCi.
If semiconductor availability is also considered for Si, 300 V Si switches are available for the optimal Si design with N = 5, but the current 300 V Si switches suffer from large reverse recovery losses (Q_{rr} losses), which are not included in the selected FOM[1]. The same is true for $N = 6$, so a 7L Si FCi with compet-

[1]The reverse recovery losses could be considered as shown in [52], if manufacturers would specify the required information in the datasheet.

itive 200 V semiconductors emerges as a feasible design for Si when discrete devices and components are used.

In general, however, it can be seen in **Fig. 2.5 (b)** that for ML FCis with a higher number of levels, a large part of the total FCi volume consists of gate drivers, semiconductors, measurement circuits and additional volume, e.g., for signal tracks on the PCB (cf. layout in **Fig. 2.4**), if discrete components are used. These volumes are highly dependent on the available Integrated Circuit (IC) packages and the designer's circuit choice, as one can, for example, choose between bootstrap circuitry or galvanic isolation [57] to power the gate drives, or choose a more integrated gate driver option [58], which is becoming more popular due to reduced complexity and improved switching performance. Theoretically, a customized solution is also possible where these functions are fully integrated into a single chip or even into the PCB. To account for this degree of freedom of realization, the dashed line in **Fig. 2.5 (b)** shows the trend of a "fully integrated" ML-FCi realization, where only the volumes of the filter inductor, the capacitors, the heatsink and the semiconductors are considered. This solution now shows the other extreme and the truth for the fully integrated system lies somewhere between the solid and dashed lines of **Fig. 2.5 (b)**. Basically, however, it can be stated that for the given specifications of the motor-integrated converter, even a fully integrated design with more than $N = 6 - 8$ cannot significantly increase the power density anymore.

2.4 Summary

In this chapter, the optimal number of voltage levels for a motor-integrated 7.5 kW ML-FCi with *LC* full sine wave output filter is investigated with respect to the selected semiconductor technology (Si/GaN). Based on derived scaling laws and subsequently performed comprehensive $\eta\rho$-Pareto optimizations it is shown that higher numbers of levels N are especially useful for semiconductor technologies whose FOM strongly depends on the power semiconductor voltage blocking capability, i.e. show a large negative α_{FOM}, as given for Si power transistors. WBG power semiconductors show a significantly better, but rather flat FOM characteristic, which means that already with a low number of voltage levels a high efficiency and a high power density are achieved, but with an increasing number of levels this performance cannot be enhanced significantly anymore.
Taking into account the discrete blocking voltage levels of commercially

available semiconductors and, especially for Si, the additional reverse recovery losses occurring for hard switching, the *7L Si FCi*, as well as the *3L GaN FCi*, achieve the highest (volumetric) power densities in the Pareto optimizations for a design with discrete components (power transistors, gate drives, isolated gate drive power supplies, etc.) and a minimum required efficiency of 99 %. The comparison between the two implementations shows that compared to the 7L Si FCi, with the 3L GaN FCi the inverter volume can be reduced by another 20 % with considerably less complexity.
Moreover, the study reveals that with the trend towards fully integrated implementations, in which the required volume for gate drivers, measurement and control circuits is largely eliminated, the optimal number of levels shifts to higher values, but the benefit in power density decreases significantly for level numbers beyond $N = 6 - 8$.

3

Comparative Evaluation of Three-Phase Three-Level GaN and Seven-Level Si Flying Capacitor Inverters for Integrated Motor Drives Considering Overload Operation

This chapter summarizes the most relevant findings in the context of designing, building and experimentally analyzing an ML-FCi IMD also published in:

- **G. Rohner**, T. Gfrörer, P. S. Niklaus, D. Bortis, M. Schweizer, and J. W. Kolar, "Comparative Evaluation of Three-Phase Three-Level GaN and Seven-Level Si Flying Capacitor Inverters for Integrated Motor Drives Considering Overload Operation," in *IEEE Access*, vol. 4, pp. 7356-7371, 2024.

Motivation

Having identified the optimal FCi level number as 3L for GaN and 7L for Si considering semiconductors available on the market, this chapter presents potential implementations of these two IMDs that provide the required short-term overload capability. Given that both solutions exhibit similar $\eta\rho$ characteristics, the experimental verification focuses on the considerably less complex 3L-FCi hardware demonstrator's performance.

Executive Summary

IMDs are gaining popularity in industrial VSD applications, thanks to their more compact realization and simpler installation. However, mission profiles of, e.g., servo applications, demand overload torques of two to three times the nominal value during several seconds, which is thermally challenging for the power electronics. Accordingly, high efficiency and power density of the inverter are of paramount importance for motor integration. ML-FCis benefit from a reduced output filter volume and improved switching and on-state performance of low-voltage devices for increasing number of levels N, whereas the PCB overhead and gate drive volume increases. In this chapter, the most power-dense solution between a seven-level (7L) FCi with Si semiconductors and a three-level (3L) FCi with GaN semiconductors is evaluated. Thereby, a straightforward design procedure allows to dimension both FCis for 99% efficiency at nominal operation, while providing a high short-term overload torque (three times the nominal torque) also for low inverter output frequencies. Due to its slightly higher power density and greatly reduced complexity, a phase module of the 3L GaN FCi is realized as an IMD hardware demonstrator. A transient thermal model is employed to specify the feasible overload operating range, considering the limited heat spreading in the baseplate and parameter variations, e.g., from manufacturing tolerances. The experimental analysis of the demonstrator verifies an efficiency of 98.94% and the practically required overload capability.

3.1 Introduction

In the previous chapter, a preliminary study on the optimal level number for a motor-integrated 7.5 kW FCi has been conducted. Thereby, a $\eta\rho$ Pareto optimization based on the *nominal* operating conditions provided in **Table 1.1** has identified the lower level counts of $N = 5$ for Si and $N = 4$ for GaN semiconductor technology as optimal for a simple and idealized FOM-based semiconductor model. For an actual implementation, however, only a limited number of semiconductors with certain discrete blocking voltages, and especially for Si devices, with low reverse-recovery (Q_{rr}) losses, are available on the market. As a consequence, $N = 7$ for Si and $N = 3$ for GaN are considered for the motor-integrated ML-FCi at hand.

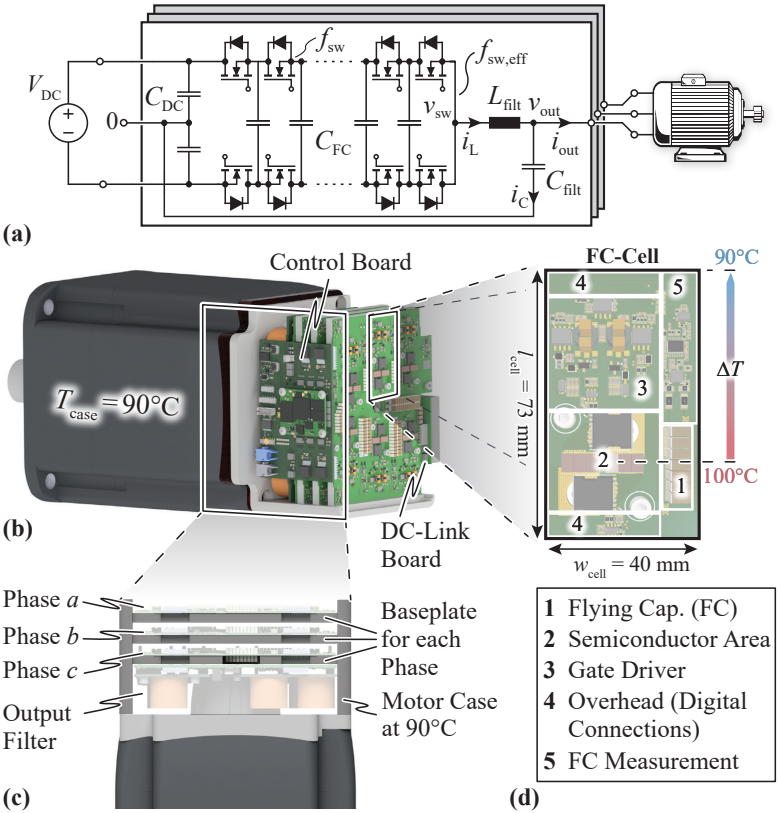


Fig. 3.1: (a) Schematics of a ML FCi phase module. **(b)** Phase-modular IMD setup. **(c)** Side view without DC-Link and control board. **(d)** Rendered 3D layout of a FC-cell of a 7L-FCi prototype with labeled main components whose volumes are considered in the design optimization (Section 3.2). The temperature gradient over the baseplates of the phases to the motor case at T_{case} = 90 °C is assumed as maximum ΔT = 10 °C.

Several inverter motor integration concepts have been discussed in the literature and were classified into four main arrangements: Radial housing mount, radial stator mount, axial endplate mount and axial stator mount [16]. If the specific frame size (and thus indirectly also the diameter) of a given motor should be maintained despite drive integration (e.g., NEMA frame size [19]) an axially mounted drive is often the only option. In this case, however, the frame size restricts the available mounting area for the inverter. In order to overcome this limitation, one possible approach is to utilize a

phase modular assembly such as shown in **Fig. 3.1 (b)**, where each phase module is mounted on an individual baseplate, which is fixed on two sides to the elongated motor case (cf. **Fig. 3.1 (c)**). At the remaining two sides, the control board as well as an interconnecting DC-Link board are attached, providing similar connection distances for all phases.

The thermal management of an IMD varies with the type of integration and the target requirements. The power electronics can be thermally insulated from the motor, thus allowing a more independent design of motor and/or power electronics, especially with two separate cooling systems (i.e., water cooling, forced or natural convection cooling over the housing/additional cooling fins or heat conduction over the flange), but resulting in a larger total volume. Alternatively, the power electronics can be thermally connected to the motor leading to a more compact integration into a single housing without thermal barriers, but at the cost of potentially higher operating temperatures of the semiconductors in the vicinity of the motor. For example in the case at hand, the inverter stage has to be able to operate at the peak temperature of the naturally cooled motor housing (i.e., $T_{\text{case}} = 90\,^{\circ}\text{C}$ as specified in **Table 1.1**). This is especially challenging in applications such as servo drives, where high transient overload torques are required. Thereby, the nominal operation torque is typically exceeded by a factor of two to three for several seconds [20], e.g., during acceleration and braking operations. This leads to a high transient current stress in the inverter and thus results in high conduction and switching losses respectively, which is especially critical considering the maximum allowed semiconductor junction temperature in combination with the already elevated ambient operating temperature in the vicinity of the motor. Generally, power semiconductors are rated for junction temperatures of 150 °C to 175 °C, Digital Signal Processors (DSPs) and current sensors up to 125 °C, and capacitors in the range of 105 °C to 200 °C.

In this chapter these challenging operating conditions are taken into account for the design of a 7.5 kW ML-FCi for a motor-integrated inverter, driving a PMSM with a nominal speed of 4500 rpm and $p = 4$ pole pairs. **Section 3.2** proposes a straightforward and efficient design procedure for a realization with commercially available Si and GaN semiconductors, i.e., as 7L Si FCi and 3L GaN FCi, identifying the most power-dense solution for given boundary conditions like a high short-term overload torque capability (i.e., $i_{\text{out,OL}} = 45\,\text{A}$ phase current amplitude during 3 s) over a broad range of inverter output frequencies f_{out}, i.e., motor rotational speeds, and a 99 % inverter efficiency during nominal operation (cf. **Table 1.1**). In **Section 3.3**, the overload capability of the most promising design, i.e., of the 3L GaN FCi,

is analyzed in more detail with a transient thermal model. Subsequently, the 3L GaN FCi is realized as a hardware demonstrator and the nominal as well as the thermally critical overload operation are experimentally verified comprehensively. **Section 3.4** concludes the chapter.

3.2 Design Optimization

In order to find the most power-dense realization of the targeted 7.5 kW IMD, both possible design approaches with a 7L-FCi based on Si and a 3L-FCi based on GaN semiconductor technology must be optimized and compared. Thereby, the two ML-FCi systems should be dimensioned for the specifications provided in **Table 1.1** and, in particular, feature a nominal efficiency of 99% and a high short-term overload capability of three times the nominal phase current, i.e., 45 A peak amplitude, during 3 s.

3.2.1 Power Semiconductor Selection

In the first step, specific power transistors have to be chosen for the 7L Si FCi and 3L GaN FCi. Thereby, the overload operation capability of the IMD strongly influences the set of feasible devices as the maximum allowed junction temperatures (175 °C for Si and 150 °C for GaN) must not be exceeded. A straightforward and pragmatic design approach initially considers only the inevitable (temperature-dependent) conduction losses occurring during the short-term overload operation, since they can be quantified easily and allow a quick estimation of the junction temperature.

During the short-term overload operation with an AC output voltage (e.g., at 300 Hz inverter output frequency, the current in each switch has an RMS value of $\frac{1}{\sqrt{2}} \cdot \frac{45\,\mathrm{A}}{\sqrt{2}}$, since the total conduction time is, in average, evenly distributed between the High-Side (HS) and the Low-Side (LS) switches in each FCi-Cell [59]. However, e.g., in servo drive applications, it is desired to achieve the overload capability over a large range of inverter output frequencies: the worst-case stress for the semiconductors then occurs during a short-term motor standstill overload (i.e., DC operation with 0 Hz inverter output frequency), where the conduction losses remain evenly distributed between HS and LS of each FC-cell due to an output voltage close to the mid-point voltage (lack of back EMF), but with a significantly higher RMS current per switch of up to $\frac{1}{\sqrt{2}} \cdot 45\,\mathrm{A}$ in the phase carrying the full (DC) overload output current; this corresponds to doubled conduction losses assuming the same on-state resistance (R_{dson}).

Tab. 3.1: Preliminary semiconductor selection based on the maximum junction temperatures reached during the short-term overload operation ($T_{j,OL,AC}$ for high output frequencies and $T_{j,OL,DC}$ for standstill), considering only (temperature dependent) conduction losses and a simple thermal resistance model $R_{th,jhs}$, assuming a constant baseplate temperature of 100 °C (i.e., excluding semiconductor switching losses and heat spreading in the baseplate).

	Si (200 V, $T_{j,max}$ = 175 °C)	
Device	BSC220N20SFD, 22 mΩ	IPT111N20NFD, 11 mΩ
N_{par}	1	1
$R_{th,jhs} = R_{th,jc} + R_{th,chs}$	0.7 K/W + 0.75 K/W	0.4 K/W + 0.5 K/W
$T_{j,OL,aC}$	127.2 °C	108 °C
$T_{j,OL,DC}$	179 °C	117.1 °C
	GaN (650 V, $T_{j,max}$ = 150 °C)	
Device	GS66516-T, 25 mΩ	GS66516-T, 25 mΩ
N_{par}	1	2
$R_{th,jhs} = R_{th,jc} + R_{th,chs}$	0.3 K/W + 0.4 K/W	0.3 K/W + 0.4 K/W
$T_{j,OL,AC}$	118.5 °C	104.2 °C
$T_{j,OL,DC}$	144.6 °C	108.7 °C

In order to estimate the junction temperature, a straightforward thermal model with a single thermal resistance $R_{th,jhs}$ from the semiconductor junction to the baseplate is used[1]. The baseplate itself is presumed to have a hotspot temperature of 100 °C directly underneath the semiconductor[2] (cf. **Fig. 3.1**). The adopted temperature difference of ΔT = 10 °C between the 90 °C of the motor housing and the hotspot on the baseplate where the semiconductors are mounted accounts for the baseplate's thermal resistance resulting from a practically feasible thickness in the range of several millimeters (cf. **Section 3.2.2**).

The high currents during overload operation and the resulting high conduction losses in combination with the elevated baseplate temperature motivate the selection of semiconductors with large die areas, i.e., low R_{dson}, and a device package with good cooling capabilities. **Table 3.1** shows avail-

[1] This model implies that the periodic loss oscillations from AC output current generation above several tens of Hz are averaged through the thermal capacitances of the semiconductor package [59]. However, the package has a relatively low thermal time constant of several milliseconds to several tens of milliseconds and therefore, during the 3 s overload interval, it reaches its thermal steady state.

[2] This assumption considers ideal heat spreading in the baseplate, which can only be achieved with a very low thermal resistance and/or a very large thermal capacitance allowing to absorb a considerable amount of energy with negligible temperature increase.

able Si and GaN candidate devices with low R_{dson}. For Si, only devices with low reverse recovery (Q_{rr}) losses in hard-switched applications are considered, resulting in the two bottom-side cooled devices with an R_{dson} of 11 mΩ (IPT111N20NFD [60]) and 22 mΩ (BSC220N20SFD [61]) at 25 °C (both from Infineon). Their respective thermal resistance $R_{\mathrm{th,jhs}}$ is composed of two parts: the junction-to-case thermal resistance $R_{\mathrm{th,jc}}$ provided in the datasheet, and the case-to-heatsink thermal resistance $R_{\mathrm{th,chs}}$, which includes the cooling of the semiconductor package through the PCB (with thermal vias and a copper inlay) and a high-performance Thermal Interface Material (TIM) (cf. **Table 3.3**). $R_{\mathrm{th,chs}}$ was measured for an IPT111N20NFD device in [59] and is scaled up by a factor of 1.5 for the BSC220N20SFD to account for the reduced cooling pad size of the package.
For GaN, the top-side cooled device GS66516-T [62] from GaN Systems turns out to be the best-suited device readily available on the market, offering the lowest R_{dson} (25 mΩ at 25 °C) in a package with very good cooling capability. There, $R_{\mathrm{th,jhs}}$ is solely composed of junction-to-case thermal resistance $R_{\mathrm{th,jc}}$ given in the datasheet and the thermal resistance of the TIM (cf. **Table 3.3**), since no cooling through the PCB is required.

Together with the temperature-dependent R_{dson} provided in the respective datasheets, the minimum losses for each device during AC overload operation (i.e., only conduction losses) can be computed and the "best-case" AC junction temperature ($T_{\mathrm{j,OL,AC}}$) obtained. As shown in **Table 3.1**, all considered semiconductor options remain well below the critical maximum junction temperatures.
In contrast, when looking at the standstill overload operation with DC output voltage, the resulting junction temperatures ($T_{\mathrm{j,OL,DC}}$) for the Si 22 mΩ transistor (BSC220N20SFD) and for the GaN option with only one GS66516-T ($N_{\mathrm{par}} = 1$) exceed or are very close to their respective maximum ratings, which leaves no margin for switching losses and/or expected non-ideal heat spreading in the baseplate. This motivates to implement the Si FCi with 11 mΩ semiconductors (IPT111N20NFD) and the GaN FCi with two paralleled GS66516-T devices, which both offer >40 °C junction temperature headroom.

With the power transistors selected, the choice of the switching frequency constitutes the main degree of freedom for the further optimization of the ML-FCi topologies, aiming for maximum power density. Therefore, in the following, first accurate switching loss models for the selected Si and GaN transistors are provided before then discussing the design of the passive components.

Switching Losses of Si 200 V MOSFET ($N = 7$)

The total switching loss energy (i.e., one turn-on and one turn-off transition) of the IPT111N20NFD are calorimetrically measured in a halfbridge configuration with 130 V DC-Link voltage, which corresponds to the expected blocking voltage of each cell in the 7L-FCi, and with external turn-on/off gate resistors of $R_{g,on} = 10\ \Omega$ and $R_{g,off} = 0\ \Omega$, respectively (cf. **Fig. 3.2 (a.i)**). According to measurements of the same device in [53], the Soft Switching (SSW) losses are negligible.

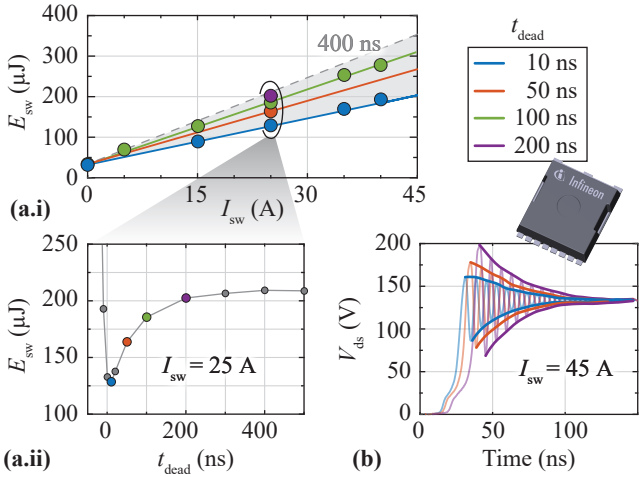


Fig. 3.2: (a.i) Calorimetrically measured combined (one turn-on and one turn-off transition) switching losses of the IPT111N20FD at 130 V with $R_{g,on} = 10\ \Omega$ and $R_{g,off} = 0\ \Omega$) and a Gate Driver (GD) supply voltage of +6 V and −3 V. Q_{rr} losses are included in these measurements and depend on the respective dead time. **(a.ii)** Influence of the dead time on the switching losses at 25 A. A steep loss increase is visible for very small dead times because for a brief time interval, an effective short-circuiting of the halfbridge occurs. **(b)** Influence of the dead time on the voltage overshoot during the hard turn-on transition due to the different reverse recovery currents.

The reverse recovery (Q_{rr}) losses are included in the measured switching losses and can be influenced with the dead time as shown in **Fig. 3.2 (a.ii)** [63]. For a large deadtime, the resulting switching losses as well as the overshoot of the switch-node voltage increase[3] as shown in **Fig. 3.2 (b)**. However, for

[3]For a large dead time, the reverse recovery charge fully accumulates in the pn junction of the MOSFET's body diode and during the hard turn-on of the complementary switch, this

very short dead times, i.e., < 10 ns for 25 A switched current, the half bridge is effectively shorted for a few nanoseconds, which results in a steep increase in the measured losses. In order to ensure sufficient margin regarding this shorting while minimizing the Q_{rr} losses with limited implementation effort, a fixed dead time of 50 ns is chosen.
The Partial-Hard Switching (PHSW) losses can be considered according to [64] and finally, the total Hard Switching (HSW) losses (including Q_{rr}) are calculated as

$$P_{sw} = f_{sw} \cdot (k_0 + k_1 \cdot I_{sw} + k_2 \cdot I_{sw}^2) \tag{3.1}$$

with $k_0 = 31.7\,\mu J$ and the VI-overlap/Q_{rr} loss coefficients $k_1 = 5.3\,\mu J/A$ and $k_2 = 0\,\mu J/A^2$ extracted from the measurement results[4] shown in **Fig. 3.2 (a.i)**; these coefficients are valid for 50 ns dead time and $V_{sw} = 130\,V$.

Switching Losses of GaN 650 V HEMT ($N = 3$)

For a 3L-FCi implementation with GS66516-T devices, the HSW and SSW loss data provided by the manufacturer and shown in **Fig. 3.3** is used, which includes a temperature dependency as discussed in [65]. The corresponding loss coefficients of (3.1) for a HSW transition are fitted as $k_0 = 55.2\,\mu J$, $k_1 = 4.8\,\mu J/A$ and $k_2 = 0.037\,\mu J/A^2$ at a junction temperature of 125 °C, and for a SSW transition as $k_0 = 15.3\,\mu J$, $k_1 = -0.64\,\mu J/A$ and $k_2 = 0.026\,\mu J/A^2$. A fixed dead time of 100 ns is chosen for the realization, which leads to negligible PHSW losses according to [64], however, at the cost of slightly increased reverse conduction losses above approximately 3 A switched current due to the higher source-drain voltage compared to Si, which results from the absence of a physical body diode.

charge is extracted via a reverse-recovery current, which results in additional Q_{rr} losses [63] and the correspondingly large reverse-recovery current I_{rr} leads to an increased overshoot of the switch-node voltage. When reducing the dead time, the reverse-recovery charge is not fully accumulated and thus I_{rr} and Q_{rr} losses are reduced, as is the voltage overshoot.

[4] Note that the loss energy k_0 of the IPT111N20NFD, which in theory represents the capacitive switching loss energy occurring for zero switched current I_{sw}, does not strictly coincide with the theoretically expected value $Q_{oss} \cdot V_{sw}$, but instead varies with the utilized $R_{g,on}$. This behavior has already been observed and discussed in [53] and thus, the measured $k_0 = 31.7\,\mu J$ is considered in the subsequent design analysis.

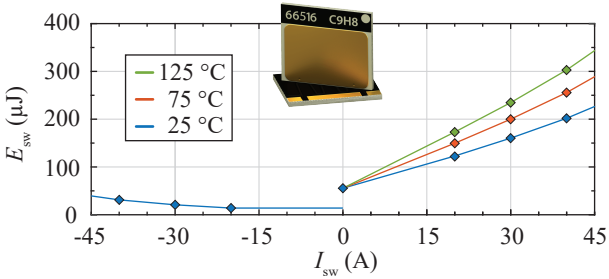


Fig. 3.3: HSW and SSW loss energy of the GS66516-T for 400 V provided by the manufacturer. The temperature dependency results from a temperature-dependent transconductance g_m [65].

3.2.2 Passive Components

With the transistors defined and characterized, the passive components of the ML-FCi remain to be designed/modeled such that the 3L-FCi and 7L-FCi can both be optimized for minimal volume at 99 % nominal target efficiency; the requirement for short-term overload capability must be considered here, too.

LC Output Filter Design

The choice of the filter inductance L_{filt} and capacitor value C_{filt} is restricted by the following limits with the specific design values given in **Table 3.2**:

1. L_{min}: Max. allowed current ripple $\Delta i_{L,pp}$.
2. L_{max}: Max. allowed output voltage drop amplitude v_L across L_{filt} at maximum electrical output frequency $f_{out,max}$.
3. $C_{min,1}$: Max. allowed voltage ripple $\Delta v_{out,pp}$ during nominal operation at the output, ultimately defining the output voltage quality.
4. $C_{min,2}$: Separation by a factor of 5 between the filter resonance frequency f_{LC} and effective switching frequency f_{eff}. Note that this separation also needs to be fulfilled during overload where f_{LC} increases due to the drop in inductance.
5. $C_{max,1}$: Min. allowed f_{LC} such that the output voltage at $f_{out,max}$ is not attenuated (separation by factor 5).
6. $C_{max,2}$: Max. reactive current amplitude i_C for $f_{out,max}$.

The corresponding boundary curves, which define the feasible filter design space [66] (highlighted in red), are visualized in **Fig. 3.4 (a)**.

Tab. 3.2: Main maximum design parameters for the IMD inverter.

Parameter	Description	Value
$\Delta v_{\mathrm{FC,pp}}$	FC Voltage Ripple (Peak-to-Peak)	13 % of Semiconductor Blocking Voltage
$\Delta i_{\mathrm{L,pp}}$	Inductor Current Ripple	80 % of $i_{\mathrm{out,nom}}$ & $i_{\mathrm{out,OL}}$
$\Delta i_{\mathrm{L,pk,OL}}$	Peak Inductor Current (including Ripple)	64 A
$\Delta v_{\mathrm{out,pp}}$	Output Voltage Ripple	8 V (1 % of V_{DC})
Δv_{L}	Voltage Drop over Inductor at $f_{\mathrm{out,max}}$	83 V (25 % of $v_{\mathrm{out,nom}}$)
Δi_{C}	Reactive Current Amplitude at $f_{\mathrm{out,max}}$	7.5 A (50 % of $i_{\mathrm{out,nom}}$)

Note that in terms of volume, the realization of the filter capacitance is much smaller than the inductor and can thus be neglected. Additionally, for an implementation of C_{filt} with CoG dielectric class I capacitors connected to the DC-Link voltage mid-point, negligible losses occur. This motivates the choice of a filter design with minimum inductance L_{filt}.

The frequency of the output current ripple in an ML-FCi can reach several 100 kHz, as the effective switching frequency f_{eff} at the output filter equals $(N-1)$ times the device switching frequency f_{sw} [50]. Therefore, a suitable inductor core material with low HF losses is required, where in addition complete saturation during overload must be avoided. A possible choice of core material is KoolMu HF from Magnetics [56], an iron-based (FeSiAl) powder optimized for low losses at high frequencies. The material features a soft saturation characteristic, i.e., shows a smooth decrease in permeability (inductance) for higher magnetic fields (currents) rather than immediate saturation, i.e., an almost complete loss of the inductance above a certain saturation current, as it is the case with ferrites. This property can be advantageously utilized to design the filter inductor in terms of flux excitation for nominal operation, while during overload a certain drop in inductance is accepted as long as the inductor current peak value $i_{\mathrm{L,pk,OL}}$ does not exceed a certain limit (cf. **Fig. 3.4 (b)** and **Table 3.2**).

Additionally, due to the large thermal capacitance of the copper windings and the magnetic core of the filter inductor, only a minor increase in temperature during the short-term overload operation is expected. Thus, the inductor can also thermally be dimensioned for nominal operation, where surface cooling over natural convection is assumed. The maximum allowed inductor temperature is limited to 155 °C by the considered HF litz wires, whereas

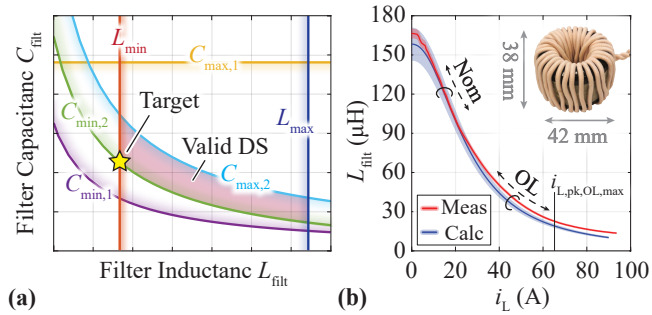


Fig. 3.4: (a) Exemplary visualization of the feasible filter Design Space (DS) defined by the boundary curves deduced from the limitations listed in 1)-6). The filter design with minimal inductance is selected (★) since the volume of the inductor dominates the total filter volume. **(b)** Output filter inductance vs. current for a 3L GaN FCi design using an iron powder magnetic core with soft saturation characteristic. Indicated are the maximum overload inductor peak current as well as the nominal and overload operating areas.

the KoolMu cores would allow higher temperatures [56]. A TIM thermally couples the core and the winding to improve the cooling of the former during nominal operation and to utilize the thermal capacitance of the core during overload, where mainly the conduction losses are substantially increased and thus cooling of the winding is important. Accordingly, a homogeneous temperature of the core and winding can be expected.

For the selected L_{filt} from the presented Design Space (DS), the filter inductor can be dimensioned based on the inductor core material data[5] provided by Magnetics [56] and calculated inductor current waveforms. Thereby, only commercially available toroidal core shapes are considered, which inherently minimize the external magnetic stray field and are thus advantageous for the compact placement in motor-integrated designs (i.e., less critical regarding eddy current losses in close-by metal components and regarding EMI).

Flying Capacitor Design

The FCs need to be designed such that a maximum peak-to-peak voltage ripple $\Delta v_{FC,pp}$ specified in **Table 3.2** is not exceeded [50, 70] even during overload

[5]This type of alloy powder core is not strongly subject to DC-bias dependent losses as it is the case for ferrite [67, 68] and the losses further show only minor temperature dependency [69]. Therefore, the manufacturer data is directly used for the calculation.

with three times the nominal current. The optimization considers 450 V X6S capacitors in all FC stages. They feature a superior volumetric capacitance density [70] despite strong decay in capacitance with increasing bias voltage[6]. However, they are only rated up to 105 °C operating temperature. With an estimated thermal resistance of about 80 K/W per capacitor[7], the expected worst case RMS current in each FC stage of $I_{\mathrm{FC,rms}} = \sqrt{2/(N-1)} \cdot i_{\mathrm{out}}$ [50] and the bias-voltage-dependent Equivalent Series Resistance (ESR) [55], a minimum number of paralleled capacitors for every stage of an N-level ML-FCi is required. This essentially results in two criteria for the FC design, namely a voltage ripple and a thermal limit.

High-Frequency DC-Link Capacitor Design

Similarly to the FC design in **Section 3.2.2** the HF DC-Link capacitors are designed for a maximum allowed voltage variation $\Delta v_{\mathrm{DC,pp}}$, which is typically kept in the range of 1% to 2% of the input voltage. For a simple worst-case approximation (i.e., considering a single phase only with no HF-ripple cancellation among the three phases; peak output current during motor standstill, i.e., duty cycles around 0.5) the required minimum capacitance can be approximated with $C_{\mathrm{DC}} = 1/4 \cdot i_{\mathrm{out,OL}}/(f_{\mathrm{sw}} \cdot \Delta v_{\mathrm{DC,pp}})$ [72]. The same 450 V X6S capacitors are used for the realization as in the FC stages. Thereby, several paralleled capacitors are connected in series to achieve the required blocking voltage of the DC-Link.

Heatsink/Baseplate Volume

As already mentioned in **Section 3.1**, the baseplates on which the individual PCBs implementing the phase bridge-legs are placed, are used as heatsink/heat spreader to thermally connect the ML-FCi to the motor housing. The required

[6] Consequently, for a certain target capacitance the required number of parallel capacitors increases for higher-voltage FC stages. This also means that further optimizing the lower-voltage FC stages with capacitors rated for lower voltages results in a negligible impact on the total volume.

[7] According to [71], a thermal resistance of approximately 27 K/W can be expected per similar sized ceramic capacitor (EIA size 2520) if it is placed individually on a PCB without close-by components. Assuming that the capacitors are cooled via their surface area, the total surface area of n capacitors densely placed side by side is about a factor of two lower compared to the same n capacitors placed with sufficient distance to each other. Considering the small thermal margin of 5 °C between the peak baseplate temperature of 100 °C and the rated temperature of the capacitors as well as possible other heat sources nearby, e.g., semiconductors, an additional 50 % margin is taken into account for the capacitor's thermal resistance R_{th}, which results in about 80 K/W, i.e., allowing losses of 60 mW per capacitor.

baseplate volume is calculated assuming that a single FC-cell is mounted on a copper plate, which is laterally attached to the 90 °C motor housing. The width and length of the copper plate are given by the FCi cell dimensions (cf. w_{cell} and l_{cell} in **Fig. 3.1 (c)**) and the thickness is adjusted to achieve a specified maximum nominal-load temperature rise, with respect to the motor housing, of $\Delta T = 10\,^{\circ}\text{C}$ in the center of the semiconductor mounting area, where the majority of the losses originates (assuming a thermal conductivity of $\lambda_{\text{Cu}} = 394\,\text{W}/(\text{m}\cdot\text{K})$). No additional mechanical support structures are considered.

3.2.3 Optimal ML-FCi Designs

Considering the 7L Si FCi and the 3L GaN FCi topologies and the respective pre-selected power semiconductors, the loss and volume models of the main components introduced above enable the identification of the switching frequencies that result in the most power-dense realizations under the constraint of an efficiency above 99 % during nominal operation.

Volume Optimization with Constant f_{sw} during Nominal and Overload Operation

In a first approach, the switching frequency is not changed during overload operation, and the resulting designs are hereinafter referred to as "OLF1" design (cf. **Fig. 3.5**). The respective volume distribution (of all three phases) as well as the most important *effective* design parameters, i.e., considering possible parallelization of multiple semiconductor devices, are shown in **Fig. 3.5 (a.i)** for a Si-based 7L realization and in **Fig. 3.5 (b.i)** for a GaN-based 3L realization. Thereby, the PCB layout shown in **Fig. 3.1** is used to estimate the required PCB area of, e.g., GD circuits and signal connections. The FCs (purple in **Fig. 3.5 (a.i)**) and HF DC-Link capacitors (yellow) contribute around 30 %[8] to the total phase volume in the "OLF1" design of the 7L Si FCi because they are dimensioned such that the maximum allowed voltage ripple is not exceeded during the short-term overload operation with three times the nominal load current. Consequently, this leads to a low utilization of the

[8] For the physical realization of a DC-supplied drive an additional DC-Link energy storage might be required in close connection to the IMD DC input to cover the high power demands during short-term overload operation. Then, in combination with the DC-bus cable inductance (typically in the range of 0.6 µH/m [73]), a resonance can be excited, which needs to be limited by over-voltage protection circuitry and/or a local damping network. A more detailed analysis of this arrangement exceeds the scope of this chapter.

capacitors during nominal operation (i.e., results in a lower-than-required voltage ripple).

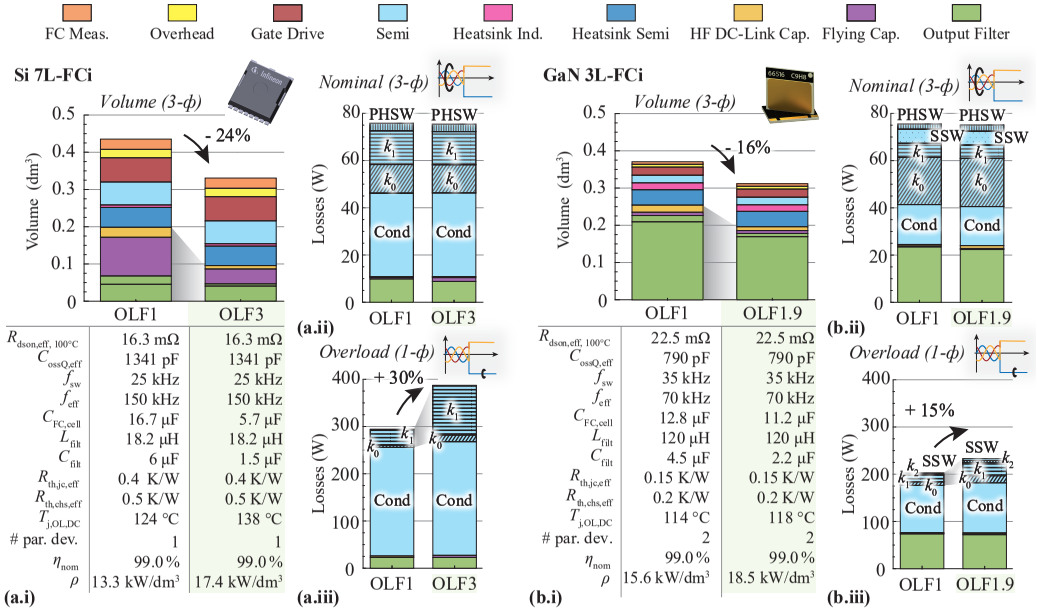
In **Fig. 3.5 (a.ii)** and **Fig. 3.5 (b.ii)** the respective total loss shares of the three-phase inverters during nominal operation is shown, which are dominated by the semiconductor losses with an approximately equal distribution between conduction and switching losses, followed by the total inductor losses. During overload operation the semiconductor conduction losses dominate as expected (cf. **Fig. 3.5 (a.iii)** and **Fig. 3.5 (b.iii)** depicting the loss breakdown of one single phase during the worst-case standstill overload).

Volume Optimization with Increased f_{sw} during Overload Operation

In order to address the mentioned low utilization of the flying capacitors during nominal operation, the capacitors could instead be designed for the nominal load current. Then, however, a linear increase of the switching frequency with the output current during overload is needed to keep the voltage ripple within specifications [59]: With an increase in switching frequency ($3 \cdot f_{sw,nom}$) during a simultaneous increase in current ($3 \cdot i_{out,nom}$), a constant maximum FC voltage ripple can be approximately maintained also during overload. In this way, an overall volume reduction of 24 % can be achieved for the 7L Si FCi design (cf. "OLF3" in **Fig. 3.5 (a.i)**). This reduction comes at the cost of increased switching losses during overload operation, which is visible in **Fig. 3.5 (a.iii)**. The increase in switching losses results in a higher junction temperature[9] $T_{j,OL,DC}$, which, however, is still below the maximum allowed operating temperature (calculated based on the simple thermal model $R_{th,jhs}$ of **Table 3.1** ignoring finite heat spreading in the baseplate).

Similarly, for the 3L GaN FCi the increase in f_{sw} during overload results in a reduction of the FC and HF DC-Link capacitor volume but the reduction is limited by the minimum required number of parallel capacitors discussed in **Section 3.2.2** (thermal limitation rather than voltage ripple limitation). However, the inductor filter volume is reduced as the increase of f_{sw} during overload helps to ensure that despite the drop in inductance during overload operation (soft permeable core material), the inductor current never exceeds the peak value of 64 A defined in **Section 3.2.2**. Consequently, a core with less core material and a stronger drop in inductance over current is allowed (while maintaining the same inductance value during nominal operation as

[9] Note that contrary to the conduction losses (and also contrary to the switching losses during AC operation) the majority of the switching losses in DC overload occur, e.g., in the LS switches of the FCi. Consequently, their $T_{j,OL,DC}$ exceeds the one of the HS switches and is referenced here.



	(a.i)		(b.i)	
$R_{dson,eff,100°C}$	16.3 mΩ	16.3 mΩ	22.5 mΩ	22.5 mΩ
$C_{ossQ,eff}$	1341 pF	1341 pF	790 pF	790 pF
f_{sw}	25 kHz	25 kHz	35 kHz	35 kHz
f_{eff}	150 kHz	150 kHz	70 kHz	70 kHz
$C_{FC,cell}$	16.7 µF	5.7 µF	12.8 µF	11.2 µF
L_{filt}	18.2 µH	18.2 µH	120 µH	120 µH
C_{filt}	6 µF	1.5 µF	4.5 µF	2.2 µF
$R_{th,jc,eff}$	0.4 K/W	0.4 K/W	0.15 K/W	0.15 K/W
$R_{th,chs,eff}$	0.5 K/W	0.5 K/W	0.2 K/W	0.2 K/W
$T_{j,OL,DC}$	124 °C	138 °C	114 °C	118 °C
# par. dev.	1	1	2	2
η_{nom}	99.0 %	99.0 %	99.0 %	99.0 %
ρ	13.3 kW/dm³	17.4 kW/dm³	15.6 kW/dm³	18.5 kW/dm³

Fig. 3.5: (a.i) & **(b.i)** Volume distribution of the resulting designs for the 7L-FCi implemented with Si (IPT111N20NFD) and for the 3L-FCi implemented with GaN power semiconductors (two paralleled GS66516-T), including the most important design parameters given below for comparison. Thereby, the designs labeled with "OLF1", assume the same switching frequency in nominal as in overload operation, while in "OLF3", the switching frequency is increased during overload by a factor of 3 for Si and in "OLF1.9" by a factor of 1.9 for GaN in order to ensure a low converter volume. **(a.ii)** & **(b.ii)** Loss breakup of the nominal operation of all three phases. **(a.iii)** & **(b.iii)** Distribution of the losses during the worst-case standstill overload operation (0 Hz inverter output frequency) of the single phase with full 45 A current is shown.

in "OLF1"). Note that in contrast to the 3L-FCi, the inductor design of the 7L did not change noticeably when the switching frequency increase was introduced, as the core size is thermally limited. Additionally, an increase of f_{sw} helps to maintain a certain ratio f_{eff}/f_{LC} in order to not excite the filter resonance, which could be possible due to the increase in f_{LC} resulting from the decrease of the effective filter inductance. All in all, increasing the switching frequency up to $1.9 \cdot f_{sw,nom}$ during overload reduces the total volume of the 3L GaN FCi by 16 % at the cost of increased overload losses (cf. "OLF1.9" in **Fig. 3.5 (b.i)** and **Fig. 3.5 (b.iii)**) and increased worst-case junction temperature $T_{j,OL,DC}$ (again below the maximum allowed value). Note that the f_{sw} only has to be increased by a factor of 1.9 instead of factor 3 found for the 7L Si FCi realization, since in the 3L GaN design the minimum number of FCs is thermally limited, i.e., regarding the allowed voltage ripple, they are over-dimensioned for normal operation. The situation is similar with the inductor design: An increase by factor 1.9 already keeps the inductor from exceeding the peak value of 64 A and prevents a potential resonance excitation of the filter.

Design Selection for Demonstrator Realization

The final expected power densities[10] and efficiencies of the 7L Si and 3L GaN FCi realizations are comparable according to **Fig. 3.5 (a.i)** and **(b.i)** (column "OLF3" and "OLF1.9" highlighted in green), but for Si a much higher complexity in terms of number of switches, GDs, control signals and FC voltage measurement circuits results. This clearly motivates pursuing the 3L GaN FCi (with an increase in switching frequency of 1.9 during overload) for the further analysis and ultimately the realization of a demonstrator system.

3.3 Hardware Demonstrator - 3L GaN FCi

So far, the overload junction temperature has only been estimated with a simple thermal model facilitating a straightforward design process, which, however, does not include, e.g., finite heat spreading in the baseplate resulting in a hotspot temperature potentially exceeding the previously assumed 100 °C. Aiming for a hardware realization, it is therefore necessary to first analyze the chosen 3L GaN FCi design with an extended thermal model to evaluate which overload torque (i.e., which output current) can be delivered for various inverter output frequencies (i.e., motor rotational speeds). Subsequently, in

[10] Includes 30% additional air volume expected from the realization.

order to show that the chosen design process and the resulting 3L GaN FCi meets the specifications of 99 % efficiency during nominal load operation as well as the thermally challenging short-time overload operation, a hardware demonstrator of the 3L GaN FCi is built and its performance is experimentally verified.

3.3.1 Achievable Overload Torque Prediction with an Accurate Transient Thermal Model

The achievable short-term overload torque (maximum overload current) is limited by the allowed semiconductor junction temperature $T_{j,OL}$. By using an accurate dynamic/transient thermal model of the semiconductor arrangement in the 3L GaN FCi, the junction temperature (and therefore the maximum overload torque) can be accurately estimated for different output frequencies (DC up to $f_{out,max}$) of the inverter. Said thermal model can be obtained by combining a thermal model of the heat spreading in the baseplate extracted from Finite Element Method (FEM) thermal simulations with a thermal model of the semiconductor package provided by the manufacturer.

Thermal FEM Simulation of Heat Spreading

In the FEM simulations, the physical transistor arrangement of the 3L GaN FCi shown in **Fig. 3.6 (a.i)** is simplified by merging all HS and all LS semiconductors into two loss input areas, respectively ($T_{HS,m}$ and $T_{LS,m}$; the areas correspond to the total area of the four HS and the four LS semiconductors). For mechanical stability reasons, the baseplate is realized with 7 mm thick aluminum (AlMgSi, with thermal conductivity $\lambda_{Al} \approx 200\,\mathrm{W/(m \cdot K)}$ instead of copper, where the thickness compared to an equivalent copper baseplate is doubled in order to account for the lower thermal conductivity.

The simulation clearly visualizes the limited transient heat spreading during an exemplary standstill overload, where a total power of about $P_{LS,m} = 115\,\mathrm{W}$ must be dissipated from the hard-switched semiconductors (the low-side transistors $T_{LS,m}$ for negative i_{out}). It was verified that the power dissipated from the soft-switched semiconductor area ($P_{HS,m} = 52\,\mathrm{W}$ in $T_{HS,m}$) can be neglected due to the weak thermal coupling of the two heat sources during the 3 s overload. As visible in **Fig. 3.6 (a.iii)** the local hot spot temperature just below the semiconductor area is expected to be 127 °C, whereas already at a small distance x away from the center, the temperature decays relatively quickly down to $T_{B(z=0)}(x) = 100\,^{\circ}\mathrm{C}$.

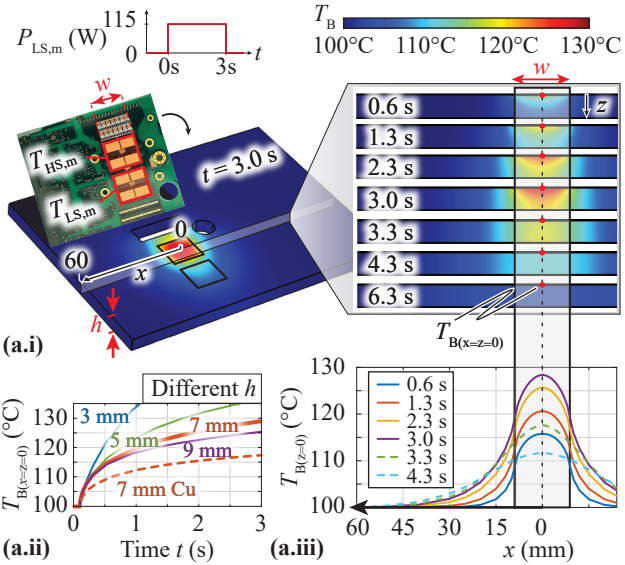


Fig. 3.6: (a.i) FEM simulation of the heat spreading in the 7 mm thick aluminum baseplate during 3 s standstill overload operation. Considering the similar losses of all HS switches and all LS switches, respectively, the four HS and four LS switches are simplified into one chip area each ($T_{HS,m}$ and $T_{LS,m}$). The thermal coupling between the HS and LS area has only a minor influence on the peak temperature during the 3 s period. With the chosen output current direction, hard-switching occurs in the LS switches, which leads to peak losses of $P_{LS,m}$ = 115 W dissipated from $T_{LS,m}$. **(a.ii)** Influence of the baseplate thickness h on the peak temperature in the center of the chip area $T_{B(x=z=0)}$. In the current realization, a baseplate thickness of h = 7 mm is implemented and is also considered in the further thermal analysis. **(a.iii)** Heat spreading in the aluminum baseplate over time and position during the 3 s overload.

Tab. 3.3: Thermal Interface Material.

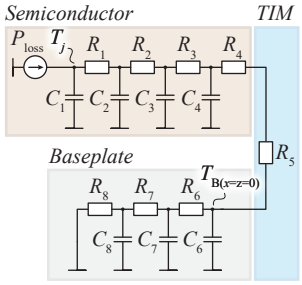
TIM Name	Thermal Conductivity	Pressed Thickness
TG-A1780 [75]	17.8 W/(m · K)	0.3 mm

A further increase in thickness of the baseplate above the current 7 mm would not lead to a significant reduction of the peak temperature after 3 s according to **Fig. 3.6 (a.ii)**, where the local hot-spot temperature $T_{\mathrm{B}(x=z=0)}$ (indicated with red dots in **Fig. 3.6 (a.i)**) over time for different baseplate thicknesses h is analyzed. In case the 7 mm thick aluminum baseplate is replaced with a 7 mm thick copper baseplate (red dashed line in **Fig. 3.6 (a.ii)**), which features about 1.5 times the thermal capacitance (for the same volume) and roughly twice the thermal conductivity compared to aluminum, the increase in $T_{\mathrm{B}(x=z=0)}$ after the 3 s overload could be reduced by 40 % to 117 °C. An even lower hotspot temperature could be achieved with the use of two-phase heat exchangers such as vapor chambers, which show substantially better heat spreading capabilities compared to copper [74].

In any case, as expected, the assumption of a homogeneous baseplate temperature during the whole overload duration, i.e., near-perfect heat spreading, can only be used as a first approximation to eliminate clearly physically impossible designs, but cannot predict the junction temperature accurately. Note that the losses during nominal operation are small due to the 99 % efficiency target, and thus no critical local hot-spot temperature occurs; Consequently, in contrast to the overload operation, the assumption of a 100 °C baseplate temperature below the semiconductors remains valid for nominal load.

Transient Thermal Model

The required dynamic/transient thermal model of the semiconductor arrangement in the 3L GaN FCi can be represented by a Cauer model with several thermal *RC* stages (cf. **Fig. 3.7**). Thereby, the Cauer model of the GaN transistor itself (GS66516-T, highlighted in brown) is provided by the manufacturer. The thermal resistance of the TIM (R_5, highlighted in blue) is determined based on the material's thermal conductivity (cf. **Table 3.3**) and on the physical dimensions of the transistor (cooling pad area of 17.8 mm × 5.7 mm). Finally, the Cauer coefficients for the three thermal RC stages describing the local hot-spot temperature $T_{\mathrm{B}(x=z=0)}$ of the 7 mm thick aluminum baseplate during overload ($R_6C_6 \ldots R_8C_8$, highlighted in grey) are derived from the FEM-simulated step response in **Fig. 3.6 (a.ii)**.



R_{th}	K/W	C_{th}	J/K
R_1	0.008	C_1	$1.48 \cdot 10^{-4}$
R_2	0.124	C_2	$1.37 \cdot 10^{-3}$
R_3	0.13	C_3	$12 \cdot 10^{-3}$
R_4	0.008	C_4	$3.7 \cdot 10^{-3}$
R_5	0.37		
R_6	0.16	C_6	0.24
R_7	0.4	C_7	0.93
R_8	1.024	C_8	5.05

Fig. 3.7: Dynamic thermal model describing the junction temperature T_j increase of a single semiconductor device during the 3 s overload operation. It includes the thermal model of the GS66516-T provided by the manufacturer, an electrically insulating TIM (cf. Table 3.3) and a thermal model describing the hot-spot temperature $T_{B(x=z=0)}$ in the aluminum baseplate extracted from Fig. 3.6 (a.ii).

Achievable Overload Torque

Fig. 3.8 (a) shows the resulting maximum allowed short-term overload output current amplitude for different maximum junction temperatures $T_{j,OL}$ over varying inverter output frequency f_{out} between DC and $f_{out,max}$. For each $T_{j,OL}$ a lower and upper current limit is shown, where the upper output current limits are derived from the loss calculations of **Section 3.2.1** and the accurate transient thermal model of **Fig. 3.7**. In order to account for possible nonidealities expected in the thermal setup and/or inaccuracies in the model, lower output current limits are calculated based on the following assumptions:

- 20 % lower thermal conductivity of the TIM compared to the datasheet specification, combined with a 30 % increased final pressed thickness, resulting in $R_5 = 0.6\,\mathrm{K/W}$.
- 20 % increased capacitive switching losses to account for additional parasitic switch-node capacitances, i.e., $k_0' = 1.2 \cdot k_0$, cf. (3.1).
- 20 % lower switching speed increasing the VI-overlap losses, i.e, $k_1' = 1.2 \cdot k_1$ and $k_2' = 1.2 \cdot k_2$, cf. (3.1).
- 30 % increase of the on-state resistance R_{dson} due to charge trapping effects (dynamic R_{dson}) known to occur in GaN HEMTs [65] in addition to the pronounced temperature dependency, i.e., $R'_{dson,eff,T_j} = R_{dson,T_j} + 0.3 \cdot R_{dson,25°C}$.

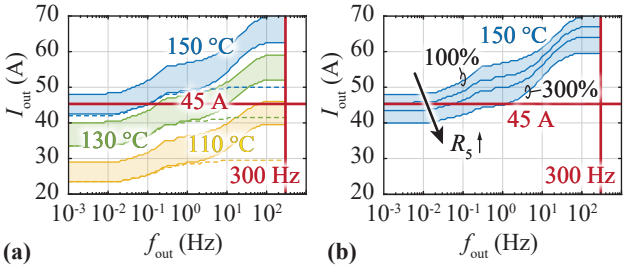


Fig. 3.8: (a) Achievable short-term overload current versus output frequency for different $T_{j,OL}$ limits (110 °C, 130 °C and 150 °C). For each $T_{j,OL}$ a higher and lower limit of output current is given, where the lower limit includes several non-idealities such as increased switching losses due to slower switching transients and parasitic capacitances, increased conduction losses due to dynamic R_{dson}, and a worse performance of the TIM. The dashed lines indicate the lower current limit if instead of the transient thermal model of the semiconductor package simply the steady-state thermal resistance ($R_1 + \ldots + R_4$ of Fig. 3.7) would be considered. **(b)** Achievable output currents over output frequency for $T_{j,OL} = 150$ °C when only the performance of the TIM is reduced (i.e., R_5 is increased from its best-case value in Fig. 3.7 to up to +200%).

From the resulting lower current limits one can conclude that the full overload current (i.e., 45 A) is nearly reached at standstill at a maximum junction temperature of $T_{j,OL} = 150$ °C (lower line of the blue area in **Fig. 3.8 (a)**). An increase of the output frequency to 0.1 Hz (i.e., 1.5 rpm for a PMSM with 4 pole pairs) allows the operation of the system with full overload current amplitude thanks to reduced average losses and the overall thermal capacitance of the setup (in particular the thermal capacitances $C_6 \ldots C_8$ of the baseplate). At higher output frequencies, the thermal capacitances of the semiconductor package become more influential. This can be clearly seen when they are omitted, i.e., the semiconductor package is only modeled with a total thermal resistance $R_{th,jc,tot} = R_1 + \ldots R_4$ without thermal capacitances. This leads to a significantly lower overload output current capability at high output frequencies (dashed lines in **Fig. 3.8 (a)**, only drawn for the lower current limits). Therefore, a certain thermal capacitance close to the heat source is clearly advantageous.

The influence of, e.g., assembly tolerances on the IMD overload performance, can be seen in **Fig. 3.8 (b)**, where the thermal resistance of the TIM (R_5) is increased by +50%, +100% and +200% compared to the initial best-case scenario given in **Fig. 3.7** (corresponding to 100 %). For example, an increase of +50% is approximately reached if the TIM is only pressed to a thickness

of 0.35 mm instead of 0.3 mm during the assembly of the inverter on the baseplate, while its thermal conductivity is simultaneously about 20% lower than specified in ideal datasheet values. Such tolerances are typically present in practice and have a significant impact on the achievable overload torque.

All in all, especially in industrial applications, it is preferred not to design the system close to the maximum temperature ratings, such that during operation the maximum junction temperatures of, e.g., the semiconductors are well below their temperature limits despite various tolerances[11], which increases their lifetime considerably [76]. In the case at hand, if a maximum junction temperature of 130 °C is selected, the full overload torque can still be safely provided for output frequencies above 10 Hz (i.e., 150 rpm) with this setup, while for DC operation still about twice the nominal torque is possible.

3.3.2 Hardware Prototype

Following a phase-modular system approach as described in **Section 3.1**, the power hardware including GDs and measurement circuits of each phase is implemented on a single PCB with a shape defined by the motor housing. This phase module PCB is then placed on an aluminum baseplate, which is thermally connected to the motor housing and, therefore, acts as heatsink. Due to the low complexity of the 3L GaN design, only a part of the total available PCB area is required. As previously shown in **Fig. 3.1** the control hardware as well as (additional) DC-Link capacitors are placed on two separate boards, which laterally connect the PCBs implementing the bridge-legs / phase modules together.

Fig. 3.9 (a.i) and **(a.ii)** show the top view of a single phase module of the 3L GaN FCi with the most relevant components labeled. Furthermore, the employed components are summarized in **Table 3.4**. The top-side cooled power semiconductors are placed on the bottom side (cf. **Fig. 3.9 (a.iii)**) of the PCB and are electrically isolated with the high-performance TIM given in **Table 3.3**. Multiple screw holes placed close to the individual semiconductors together with the soft TIM facilitate a uniformly distributed mounting pressure despite the thin (1 mm) PCB. Since the dimensions of the PCB as well as of the baseplate are defined by the motor housing, for a fair comparison of the power density with the calculated results shown in **Fig. 3.5**, only the dimensions of the populated area of the PCB (80 mm × 82 mm) according to

[11] For example, the motor case temperature could slightly increase above 90 °C and/or the distribution of switching losses between the two parallel devices could be unbalanced due to variations in gate threshold voltage and gate loop inductance, leading to a higher junction temperature than expected from the scenarios considered above.

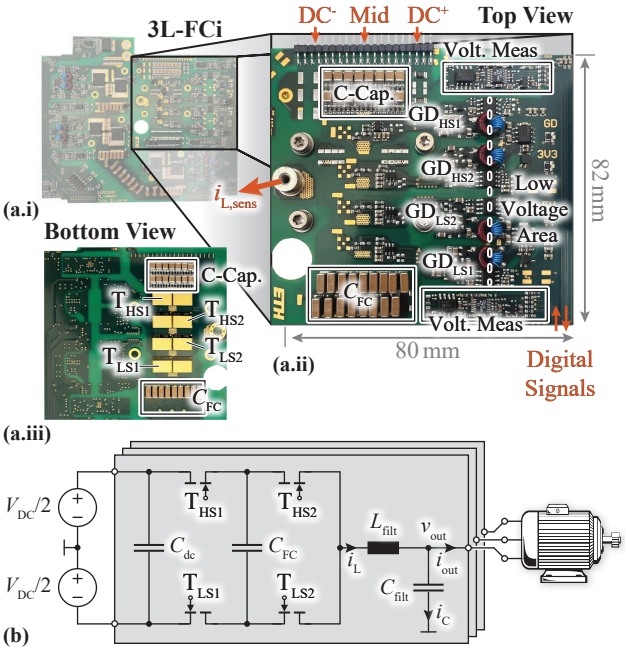


Fig. 3.9: (a.i) Implemented phase module of the 3L GaN FCi hardware prototype. The most important components are labeled in the top **(a.ii)** and bottom view **(a.iii)**. **(b)** Circuit of the phase module.

Fig. 3.9 (a.ii) and the realized toroidal filter inductor volume (120 µH nominal, cf. **Fig. 3.4 (b)**) are considered. The same holds for the baseplate, whose thickness is chosen based on the assumptions detailed in **Section 3.2.2**. With these considerations, the power density of the hardware demonstrator is about 19.5 kW/dm^3, which closely matches the calculated value of 18.5 kW/dm^3 (cf. **Fig. 3.5 (a.ii)**).

In order to minimize the VI-overlap losses, fast switching transients (i.e., high $\mathrm{d}v/\mathrm{d}t$, as seen in (3.1)) are necessary, which requires low-inductive power and gate loop designs. Additionally, as each switch of the 3L GaN FCi is implemented with two parallel devices, a good symmetry in the power and gate loop path is essential such that simultaneous switching is achieved to evenly distribute the current and the resulting losses among the paralleled semiconductors. To this end, a symmetric co-planar power loop layout is arranged on the six-layer power PCB. Note that due to the low-inductive

Tab. 3.4: Main power components and operation parameters of the realized 3L GaN hardware demonstrator shown in **Fig. 3.9** and its filter inductor shown in **Fig. 3.4 (b)**. Quantities are given for a single phase module.

Component	Value	Details
Transistors	12.5 mΩ	GaN Systems GS66516T (650 V, 25 mΩ; 2 x parallel per position)
	35 kHz	$f_{sw,nom}$
	67 kHz	$f_{sw,OL}$ (= $1.9 \cdot f_{sw,nom}$)
Gate Driver (GD)		Infineon 1EDN7511B
GD Insulator		Analog Devices ADuM121N
C_{fc}	11.2 µF	26 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V)
L_{filt}	120 µH	Magnetics Powder Core 0076076A7, 3x stacked per inductor, 32 turns of litz wire with 630 strands
C_{filt}	2.2 µF	22 x CGA9Q4NP02W104J280KA (NP0, 100 nF, 450 V)
Current Sensor		Allegro ACS733KLATR-65AB-T
OpAmp Volt. Meas.		Analog Devices LTC6362
ADC		Analog Devices LTC2311-12

power loop design, no additional commutation capacitors are required for the inner commutation loop formed by T_{HS2}, T_{LS2} and the FCs (cf. **Fig. 3.9 (b)**). The outer power commutation loop consisting of T_{HS1}, T_{LS1}, the FCs and the DC-Link capacitors, which are placed on a separate DC-Link board connected via pin headers, has a larger loop inductance and thus requires the placement of additional commutation capacitors on the power board directly next to the semiconductors (cf. "C-Cap." in **Fig. 3.9 (a.ii)** and **(a.iii)**). The symmetric gate loop is realized with a non-isolated GD integrated circuit (1EDN7511B from Infineon [77]) placed directly over the power transistors on the top layer of the PCB, while mandatory signal isolation as well as the galvanically isolated bipolar supply for the GD (+6 V and −3 V) are placed outside of the power-loop area. This prevents any overlap of fast fluctuating voltage potentials, i.e., voltage steps with logic nets connected to the control board, which would cause undesired CM currents over parasitic capacitances that could lead to errors in the gate and/or measurement signals.

3.3.3 Experimental Performance Verification

For the experimental verification, a phase module of the 3L GaN FCi is operated in open-loop, i.e., without active (closed-loop) output current control, however, the FC voltages are actively balanced with a simple closed-loop proportional controller by means of slight adjustments to the individual switching cells' duty cycles [78]. The aluminum baseplate on which the 3L-FCi is mounted for the measurements is heated to the target operation temperature of 100 °C. Similarly, the inductor is heated by a hot plate to reach the nominal surface temperature of 135 °C as determined from its thermal model.

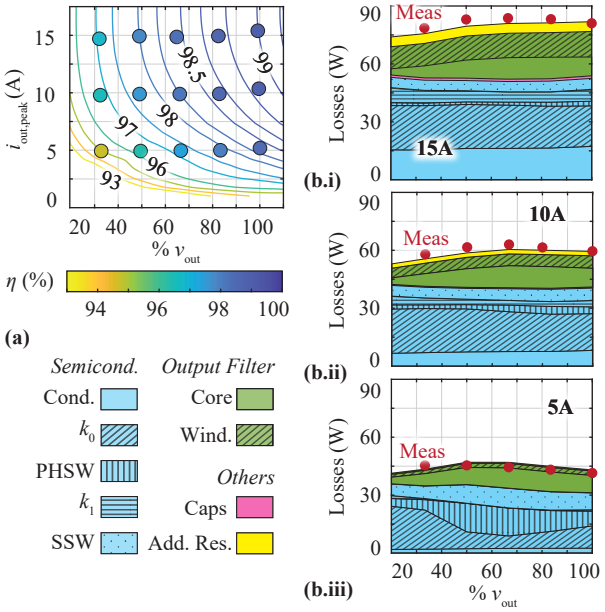


Fig. 3.10: (a) Measured (dots) and calculated (lines) efficiencies for different output powers (nominal and partial load operation) with varying output current amplitudes and a baseplate temperature of 100 °C. Partial load operation is achieved by linearly reducing the output voltage amplitude as well as the fundamental frequency, corresponding to an operation with a constant ratio V/f (V/f-control based operation). **(b.i)-(b.iii)** Measured total losses and calculated loss breakdown for the considered output current amplitudes for nominal and partial load operation, clearly highlighting the dominant contribution of the semiconductor switching losses.

Efficiency and Loss Distribution in Nominal Operation at 100°C Baseplate Temperature

Electrical efficiency measurements for a resistive load are performed with a Yokogawa WT3000 precision power analyzer [79], which according to a comparison with calorimetric efficiency measurements published in [80] achieves very accurate measurement results for systems in the 2 kW – 10 kW power range with efficiencies > 99 %.

The measured and calculated efficiencies for nominal operation and several part load scenarios are given in **Fig. 3.10 (a)**. The nominal operating point is defined according to **Table 1.1** as 7.5 kW for a three-phase system, with a peak output current amplitude of 15 A at 300 Hz output frequency resulting in a peak output voltage amplitude of $v_{\text{out,nom}} = 330$ V (100 % v_{out} in **Fig. 3.10**). Partial load operation is tested with a fixed output current amplitude and a gradually decreasing output voltage to decrease output power. At the same time, the output frequency is decreased such that a constant ratio of voltage to frequency remains (resembling a V/f-controlled drive system [81]). This corresponds to the practically relevant application scenario where a certain constant torque at reduced rotational speed has to be provided. In the nominal operating point an efficiency of 98.94 % is measured, which compared to the anticipated 99 % corresponds to only 1.5 W of additional losses per phase module. As can be observed in the calculated loss breakdown of **Fig. 3.10 (b.i)-(b.iii)**, which are obtained with the loss models of **Section 3.2**, the loss discrepancy could be explained with additional ohmic losses (yellow section) originating from a 15 mΩ resistance, which could be attributed to, e.g., the contribution of connectors, PCB tracks and the current sensor. At nominal output current (cf. **Fig. 3.10 (b.i)**) the losses are dominated by the semiconductor conduction (Cond.) and capacitive switching losses (k_0) losses. The slight change in losses with output voltage is explained with the varying average current ripple depending on the modulation depth (i.e., output voltage amplitude), which in turn impacts the switching losses as well as the HF inductor core losses. A higher inductor current ripple reduces the VI-overlap losses (k_1) but increases the SSW losses. For lower output currents (cf. **Fig. 3.10 (b.ii)** and **(b.iii)**), the higher relative current ripple increases the number of SSW (or PHSW) transitions and thus increases the SSW (or PHSW) loss contribution and reduces the HSW losses (k_0, k_1). In contrast to the semiconductor losses, the contribution of the output filter core losses increases for a higher current ripple (and thus for higher flux density ripple ΔB) following the loss modeling data provided by the manufacturer based on Steinmetz parameters. At the same time, the conduction losses of the

output filter windings (Wind.) and also of the semiconductors increase due to a higher RMS current but compared to the overall losses the influence is negligible.

Fig. 3.11 (a) shows measured waveforms during nominal operation with the characteristic 3L switch node voltage v_{sw} in blue and the inductor current i_L in green. The latter has its maximum ripple at ±200 V output voltage (i.e., 0.25 or 0.75 duty cycle). Due to the output filter, the filtered output voltage (v_{out}, yellow) and output current (i_{out}, magenta) only show negligible distortions.

A thermal image of the PCB's top side, taken with a high-resolution infrared camera (FLIR A655sc [82]), shows equal temperature distribution over the entire board during nominal operation with 100 °C baseplate temperature, which is expected due to the high system efficiency. The semiconductors cannot be directly monitored with the thermal camera, as they are placed on the bottom side of the PCB and are pressed to the aluminum baseplate for cooling. Thus, only the transferred heat through the PCB and vias is visible. Nonetheless, based on the thermal models, T_j is expected to be only 2 °C – 3 °C above the baseplate temperature.

Overload Operation at 100°C Baseplate Temperature

The waveforms for short-term overload output currents with and without spinning rotor are given in **Fig. 3.11 (b)** and **Fig. 3.11 (c)**, respectively. As soon as the output current exceeds the nominal value of 15 A, the switching frequency is linearly increased with the output current up to a factor of 1.9 at 45 A as discussed in **Section 3.2.3**. Contrary to nominal operation, a local increase in temperature around the semiconductor area can be observed during the short-term overload with spinning rotor and even more pronounced for overload at standstill with almost full overload torque, which qualitatively shows the thermal stress caused by the overload losses. Electrical loss measurements show good matching of the losses during standstill overload operation with the respective calculations for 43 A phase current (measured: 255 W, calculated: 233 W, i.e., < 10 % error) when the additional 15 mΩ for connectors and traces are considered.

3.4 Summary

In this chapter, a phase modular IMD fed by an 800 V DC-Link for a 7.5 kW industrial servo drive application is designed and implemented based on

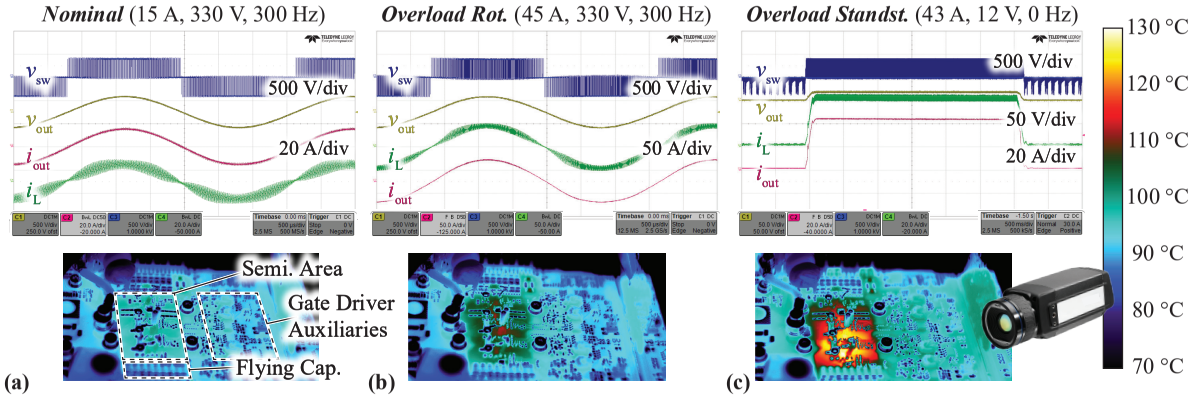


Fig. 3.11: Measured waveforms of the switch-node voltage v_{sw}, filtered output voltage v_{out}, inductor current i_{L} and the filtered output current i_{out} during **(a)** nominal load operation, **(b)** overload operation with maximum output frequency (AC overload) and **(c)** standstill overload operation (DC overload), all for 100 °C baseplate temperature. Additionally, the respective thermal images taken with a high-resolution infrared camera (FLIR A655sc) are displayed to qualitatively show the thermal stress during the different operating modes.

typical specifications. Thereby, the high temperatures close to the motor of around 90 °C are challenging regarding the thermal design, especially when considering the required short-term overload capability of three times the nominal current (i.e., 45 A phase current amplitude during 3 s).

Aiming for the most compact realization, first, two topology candidates with LC output filters, a 3L-FCi based on GaN and a 7L-FCi based on Si power semiconductor technology, are evaluated and compared. The inverter volumes are minimized by allowing an increase in switching frequency during overload operation as it allows to dimension the flying capacitors and the output filter, which is implemented with a soft-permeable inductor core material, mainly for nominal operation as long as thermal limitations during overload operation are respected. Since both, the 3L GaN FCi and 7L Si FCi, promise similar power densities the significantly less complex 3L GaN topology is selected for the realization of a hardware demonstrator. First, a transient thermal model that includes also the heat spreading below the semiconductors in the baseplate is proposed for estimating the achievable overload torque (i.e., max overload current) for given maximum semiconductor junction temperatures, various inverter output frequencies (i.e., various motor speeds) and mechanical/electrical tolerances. Finally, the design approach is validated with the realization of a 3L GaN FCi hardware demonstrator, which achieves the expected efficiency of 99% at nominal load and provides rated overload capacity, i.e., up to three times the nominal current for three seconds.

4

Hardware-Based Comparative Analysis of Multilevel Inverter Topologies for Integrated Motor Drives Considering Overload Operation

This chapter summarizes the most relevant findings concerning the comparative evaluation of three different ML IMDs based on realized hardware demonstrators also published in:

- **G. Rohner**, T. Gfrörer, P. S. Niklaus, J. Huber, D. Bortis, M. Schweizer, and J. W. Kolar, "Hardware-Based Comparative Analysis of Multilevel Inverter Topologies for Integrated Motor Drives Considering Overload Operation," in *IEEE Open Journal of Power Electronics*, vol. 4, pp. 934-944, 2023.

Motivation

Expanding beyond pure FCi designs, the previously dismissed 7L inverter can be realized as 7L-HANPC with reduced complexity. Hence, this chapter presents a thorough hardware-based comparison among the 7L-FCi, 7L-HANPC, and 3L-FCi concerning motor integration with short-term overload capability. Ultimately, it is shown that a realization with a 3L GaN FCi features the best overall trade-offs for the specified IMD.

Executive Summary

With today's demand for increased industrial process automation a trend towards IMDs has evolved allowing a low complexity and compact installation of the drive system. Especially servo applications with high short-term overload requirements (e.g., three times the nominal current for several seconds) are a thermal challenge for the power electronics. Consequently, high efficiencies and power densities are key requirements of these motor-integrated VSDs. ML inverter topologies allow small *LC* output filter designs and benefit from utilizing low-voltage semiconductors with superior conduction and switching performance, and thus represent an interesting approach for future IMDs. In this work an experimental comparison between three different 800 V DC-Link supplied drive systems is presented, namely between a 3L-Flying Capacitor Converter (3L-FCC) (employing 650 V GaN HEMTs), a 7L-Flying Capacitor Converter (7L-FCC) (using 200 V Si MOSFETs) and its promising alternative, a 7L-HANPC (using both, 650 V GaN HEMTs and 200 V Si MOSFETs). All three systems are realized as hardware demonstrators for the same specifications, i.e., for integration into a PMSM with a case temperature of 90 °C, 7.5 kW nominal output power at >99 % efficiency and a short-term overload capability of three times the nominal current for 3 s. Thereby, the efficiencies and the thermally critical overload capability are experimentally verified. Overall, the 3L-FCC shows the best performance trade-off with lowest complexity and/or highest reliability and minimal control effort.

4.1 Introduction

In the previous chapters, the evaluation and optimization of ML IMD was limited to FCi topologies. Thereby, Chapter 3 showed that a 3L-FCC with GaN semiconductors (cf. **Fig. 4.1 (c)**) achieves the nominal target efficiency specification of 99 % (cf. **Table 1.1**) at a maximum power density and minimal complexity, which was experimentally verified with a hardware demonstrator employing 650 V GaN HEMTs. However, in the course of the analysis a 7L-FCC design with 200 V Si MOSFETs was also considered, cf. **Fig. 4.1 (a)**, and promised a similar power density with a remarkably smaller filter volume but dominating PCB volume (more semiconductors, gate drives and flying capacitors) compared to the 3L-FCC. The same small filter volume can be achieved with a 7L-HANPC [80], i.e., a combination of a four transistor Active Neutral-Point Clamped (ANPC) switching stage and only three additional

flying capacitor cells (cf. **Fig. 4.1 (b)**). All in all, the 7L-HANPC requires a significantly lower number of semiconductors and passive energy storage elements (i.e., flying capacitors) and thus qualifies as an attractive 7L alternative with reduced complexity.

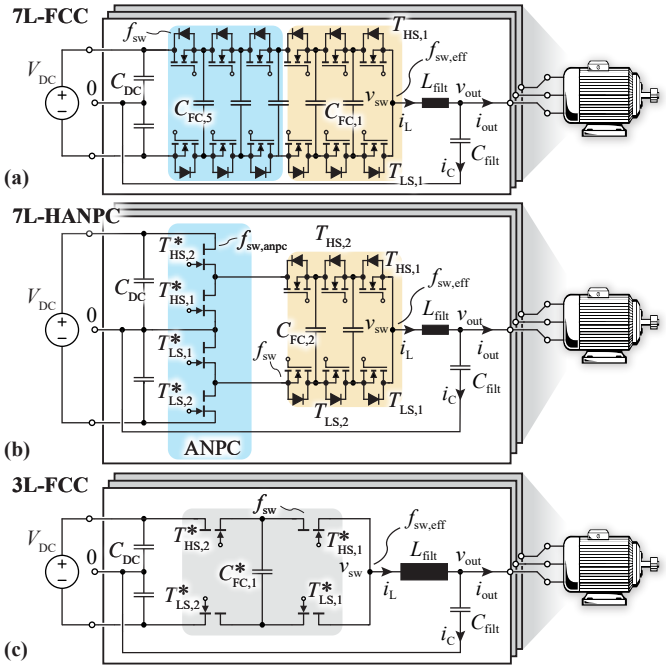


Fig. 4.1: Circuit schematics of the phase modules of a motor-integrated three-phase inverter stage considered in the comparative evaluation in this chapter: **(a)** 7L-FCC, **(b)** 7L-HANPC and **(c)** 3L-FCC. Assuming a DC-Link voltage of 800 V, the 7L-FCC and the FC-cells of the 7L-HANPC are built with 200 V SI MOSFETs, while the 3L-FCC and the ANPC stage of the 7L-HANPC are realized with 650 V GaN HEMTs. The DC-Link referenced full-sinewave output filter largely attenuates DM and CM switching frequency voltage components.

These findings finally motivate a full hardware-based comparison of the three possible IMD implementations (7L-FCC, 7L-HANPC, and 3L-FCC), which is performed in this chapter for the target specifications of **Table 1.1** and **Table 4.1**, including the challenging short-term overload capability.
In the following, the different phase module hardware demonstrators are pre-

sented in **Section 4.2**, briefly summarizing the main hardware design aspects. Subsequently, their performance is experimentally verified in **Section 4.3**, followed by an overall comparison of the three IMD solutions in **Section 4.4**. A compact IMD design is proposed in **Section 4.5** for the topology with the best overall trade-offs. Finally, **Section 4.6** concludes the chapter.

Tab. 4.1: Specifications for the analyzed Integrated Motor Drive (IMD) extending **Table 1.1**.

Parameter		Value
Filter Output Voltage Ripple	$\Delta v_{\mathrm{out,pp}}$	1 % of V_{DC}
Filter Inductor Current Ripple	$\Delta i_{\mathrm{L,pp}}$	80 % of $i_{\mathrm{out,nom}}$

4.2 Design and Realization

All three inverter hardware demonstrators are designed to meet the target specifications of **Table 1.1** and **Table 4.1**, including identical DC-Link voltage, nominal output power, minimum nominal efficiency, short-term overload capability and nominal output waveform quality (i.e., peak-to-peak output voltage ripple $\Delta v_{\mathrm{out,pp}}$). For the sake of brevity, only main aspects of the design are described here. However, the employed design procedure including component modeling has been comprehensively discussed in [83], especially for the 3L-FCC and 7L-FCC. The most important operating parameters are listed in **Table 4.2**, whereas the main components utilized in the presented phase module demonstrators are given in **Table 4.3**.

4.2.1 Design of the 7L-FCC and 3L-FCC

Both, the 7L-FCC and 3L-FCC designs aim at a nominal efficiency of minimum 99 % with minimal volume. During overload operation the semiconductor conduction losses increase quadratically with current (ohmic on-state characteristic of the power transistors) and dominate the mostly linear switching loss increase. Thus, high overload capability calls for power transistors with low R_{dson} and good cooling performance (i.e., low thermal resistance from junction to case and a large cooling pad). Considering the devices available on the market, the 7L-FCC can be implemented using single bottom-cooled 200 V Si MOSFETs (IPT111N20NFD, 11 mΩ, [60]), which are optimized for hard-switched applications. The 99 % efficiency target can be achieved with a device switching frequency of $f_{\mathrm{sw}} = 25\,\mathrm{kHz}$ and for the overload operation

the semiconductor cooling capability is improved with copper inlays and thermal vias in the PCB as shown in **Fig. 4.2 (a.ii)**. In contrast, for the realization of the 3L-FCC two parallel top-cooled 650 V GaN HEMTs (GS66516-T, 25 mΩ, [62]) per switch are required (cf. **Fig. 4.2 (b.ii)**), which operate at a switching frequency of $f_{sw} = 35$ kHz.

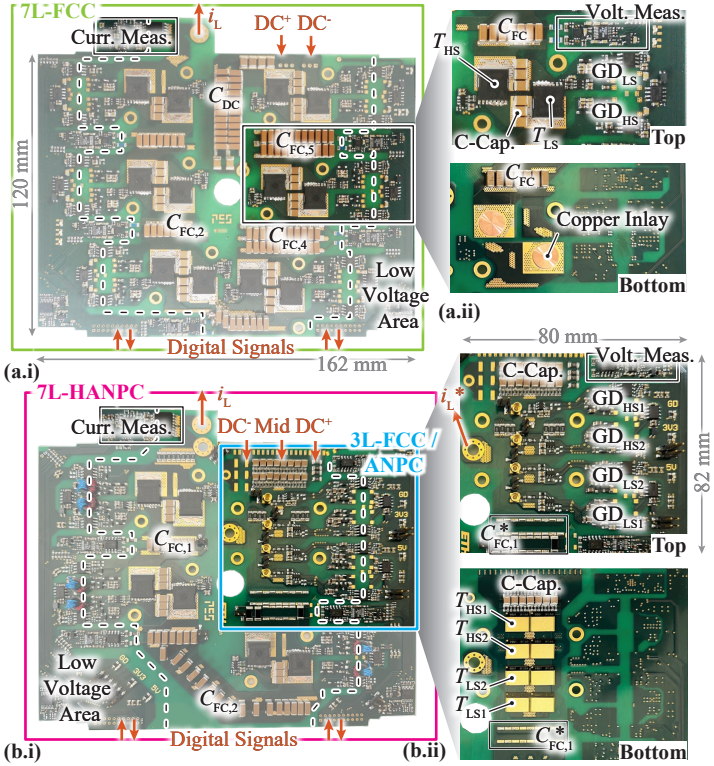


Fig. 4.2: (a.i) Implemented phase module of the 7L-FCC hardware prototype (green box). A single FC-cell is shown in more detail in **(a.ii)** with top and bottom view. **(b.i)** Implemented phase module of the 7L-HANPC (magenta box). The ANPC stage (blue box) can be configured and used as 3L-FCC directly (cf. schematics of Fig. 4.1). **(b.ii)** Enlarged view on the top and bottom of the 3L-FCC / ANPC area with labels of the most important components.

In order to keep the impact of the overload capability on the resulting system volume as small as possible, the switching frequency is increased

linearly with the output current as soon as the nominal current amplitude of 15 A is exceeded [83]. This (seemingly counterintuitive) measure allows to design the flying capacitors according to

$$C_{\mathrm{FC,cell}} = \frac{i_{\mathrm{out}}}{f_{\mathrm{sw}} \cdot \Delta v_{\mathrm{FC,pp}} \cdot N_{\mathrm{FC,cell}}} \tag{4.1}$$

(with $N_{\mathrm{FC,cell}}$ as number of FC-cells) [70] and the HF DC-Link capacitors according to

$$C_{\mathrm{DC}} = \frac{i_{\mathrm{out}}}{4 \cdot f_{\mathrm{sw}} \cdot \Delta v_{\mathrm{DC,pp}}}, \tag{4.2}$$

mainly for nominal operation [83]. Hence, the capacitance can be chosen such that certain maximum allowed voltage ripple (i.e., $\Delta v_{\mathrm{FC,pp}}$ and $\Delta v_{\mathrm{DC,pp}}$) is maintained for nominal output current, while the overload current only has to be taken into account for thermal considerations (i.e., a minimum number of parallel capacitors is required to limit the temperature increase per capacitor due to ESR losses). Furthermore, the output filter inductor is advantageously designed with a soft magnetic alloy powder core (in the present case with Kool Mμ Hf by Magnetics for low HF core losses), which is characterized by a smooth reduction in inductance with increasing current. The filter inductor can then be designed according to [70] as

$$L_{\mathrm{filt}} = \frac{V_{\mathrm{DC}}}{4 \cdot N_{\mathrm{FC,cell}}^2 \cdot f_{\mathrm{sw}} \cdot \Delta i_{\mathrm{L,pp}}} \tag{4.3}$$

for a maximum peak-to-peak filter inductor current ripple of $\Delta i_{\mathrm{L,pp}}$ during nominal operation, while during overload a drop in inductance is accepted (cf. **Fig. 4.3 (a)**). Thereby, the simultaneous increase in switching frequency guarantees that a certain peak current including current ripple is not exceeded (e.g., in the case at hand 64 A). Consequently, these limitations lead to a design-specific required increase in switching frequencies during overload, i.e., an overload factor of 3 for the 7L-FCC and 1.9 for the 3L-FCC, respectively.

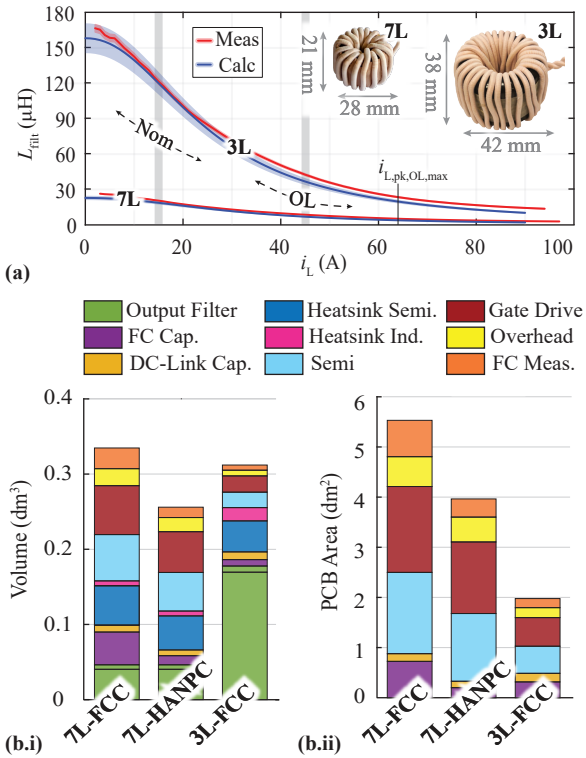


Fig. 4.3: (a) Output filter inductance vs. current of the 7L (7L-FCC and 7L-HANPC) design and 3L-FCC design realized with soft magnetic powder cores. Indicated are the operating range during nominal and overload current, the maximum accepted inductor peak current and the mechanical dimensions of the respective phase module inductor realizations. **(b.i)** Volume breakdown and **(b.ii)** PCB area breakdown expected from the three IMD solutions in comparison. For the 7L-FCC and 3L-FCC they match well with their realizations shown in **Figure 4.2 (a)** and **(b)** (considering a non-ideal packaging overhead factor 1.3 for the volume), while the realization of the 7L-HANPC is larger than necessary due to the multipurpose PCB layout.

4.2.2 Design of the 7L-HANPC

The realization of the 7L-HANPC as an alternative solution to the 7L-FCC should use the same small output filter as labeled in **Fig. 4.3 (a)** with "7L".

Tab. 4.2: Maximum switching frequencies of the hardware demonstrators during nominal ($f_{sw,nom}$) and overload operation ($f_{sw,OL}$) and their respective effective switching frequencies at the switch node ($f_{eff,nom}$ and $f_{eff,OL}$)

	$f_{sw,nom}$	$f_{sw,OL}$	$f_{eff,nom}$	$f_{eff,OL}$
3L-FCC	35 kHz	67 kHz	70 kHz	134 kHz
7L-FCC	25 kHz	75 kHz	150 kHz	450 kHz
7L-HANPC	50 kHz	85 kHz	150 kHz	255 kHz

Consequently, the generated output waveforms must be identical, which means that besides the number of output voltage levels also the effective switching frequency measured at the switch node must match. As visualized and described in more detailed in [80], the 7L-HANPC consists of two stages, namely the ANPC stage (highlighted blue in **Fig. 4.1 (b)**) and a FC stage with three FC-cells (highlighted orange in **Fig. 4.1 (b)**). The ANPC acts as a selector switch and/or unfolder, and connects the FC stage to DC+/0 or 0/DC- respectively, depending on the sign of the desired output voltage. Accordingly, the number of output voltage levels provided by the HANPC is given as

$$N_{lev,HANPC} = 2 \cdot N_{FC,cell} + 1 \tag{4.4}$$

with $N_{FC,cell}$ as the number of FC-cells. In order to match the seven output voltage levels of the 7L-FCC three FC-cells are required. As highlighted in orange in **Fig. 4.1 (a)** and **(b)**, they FC-cells are exactly identical to the lower voltage FC-cells of the 7L-FCC, i.e., they experience the same blocking voltages and can be realized with the same 200 V Si MOSFETs. Meanwhile, the ANPC stage in the 7L-HANPC replaces the higher voltage FC-cells of the 7L-FCC and must withstand $V_{DC}/2$, which requires 650 V semiconductors.
The effective switching frequency f_{eff} at the switch node is given only by the FC-cells and is a multiple of the FC-cell device switching frequency f_{sw}, i.e.,

$$f_{eff} = N_{FC,cell} \cdot f_{sw}. \tag{4.5}$$

Consequently, due to the lower number of FC-cells in the 7L-HANPC, the device switching frequency has to be doubled compared to the 7L-FCC leading to $f_{sw} = 50\,\text{kHz}$. Note, however, that this does not necessarily reduce the total efficiency. The ANPC stage has negligible switching losses due to the infrequent switching operations (determined by the motor speed and/or inverter stage fundamental output voltage frequency which is limited to values below 300 Hz in the case at hand), and thus only contributes to the

conduction losses, which can be kept low by small R_{dson} values. As mentioned previously, a low R_{dson} value is anyways required for the overload operation.

Taking into account the somewhat similar structure of the ANPC stage and the 3L-FCC (cf. **Fig. 4.1**), combined with the chosen low R_{dson} GaN semiconductors, a multi-purpose PCB layout can be realized, i.e., the same PCB can be reconfigured and used as 3L-FCC or as 7L-HANPC as shown in **Fig. 4.2 (b)**. Nonetheless, the rarely switching ANPC stage of the 7L-HANPC could also be realized with 650 V Si devices instead of GaN semiconductors, provided that both feature similar low R_{dson} values.
Considering the overload restrictions of the capacitors and the filter inductor, a switching frequency increase of up to 1.7 is required during overload in the 7L-HANPC. This is considerably lower than the factor 3 required for the 7L-FCC as the flying capacitors at lower levels are mainly thermally limited (i.e., more capacitors are required than absolutely necessary for the maximum voltage ripple at nominal operation) and thus do not need a full switching frequency increase during overload.

Finally, these considerations result in the volume breakdown and required PCB area as shown in **Fig. 4.3 (b.i)** and **(b.ii)** respectively. Clearly visible is the overall lower capacitor volume of the 7L-HANPC compared to the 7L-FCC as three higher voltage flying capacitors are eliminated (which previously required two 450 V X6S ceramic capacitors in series) and in total less switches are needed and consequently also less gate drives. Combined with the small inductor volume, the 7L-HANPC can achieve the overall smallest volume, while the 3L-FCC requires the overall smallest PCB area.

Tab. 4.3: Main power components of the different hardware demonstrators shown in **Fig. 4.2 (a)** and **(b)** with total quantities used for a single phase module.

Component	Value	Details
Transistors 650 V (3L-FCC/ANPC)	12.5 mΩ	GaN Systems GS66516T (25 mΩ, 2 x parallel per position; 27.2 mm^2 meas. device chip area)
Transistors 200 V (7L-FCC/7L-HANPC)	11 mΩ	Infineon IPT111N20NFD (11 mΩ; 29 mm^2 meas. device chip area [53])
Gate Driver (GD)		Infineon 1EDN7511B
GD Insulator		Analog Devices ADuM121N
L_{filt} (3L-FCC)	120 µH	Magnetics Powder Core 0076076A7, 3x stacked per inductor, 32 turns of litz wire with 630 strands
C_{filt} (3L-FCC)	2.2 µF	22 x CGA9Q4NP02W104J280KA (NP0, 100 nF, 450 V)
L_{filt} (7L-FCC/7L-HANPC)	18 µH	Magnetics Powder Core 0076059A7, 2x stacked per inductor, 17 turns of litz wire with 630 strands
C_{filt} (7L-FCC/7L-HANPC)	1.5 µF	15 x CGA9Q4NP02W104J280KA (NP0, 100 nF, 450 V)
C_{fc} (3L-FCC)	11.2 µF	26 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V)
C_{fc} (7L-FCC)	min. 6.9 µF per FC-cell	132 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V)
C_{fc} (7L-HANPC)	min. 14 µF per FC-cell	37 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V)
Current Sensor		Allegro ACS733KLATR-65AB-T
OpAmp Volt. Meas.		Analog Devices LTC6362
ADC		Analog Devices LTC2311-12

4.3 Experimental Performance Verification

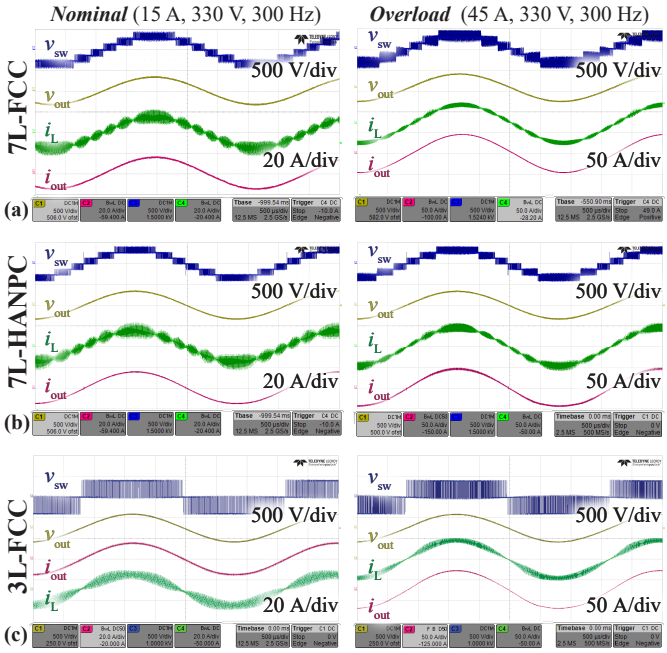


Fig. 4.4: (a) Measured phase module waveforms of the 7L-FCC, **(b)** 7L-HANPC and **(c)** 3L-FCC hardware prototype featuring the switch node voltage v_{sw}, the inductor current i_L, the filtered output voltage v_{out} and the filtered output current i_{out} during nominal operation (left) and overload operation (right), all with 300 Hz output frequency. The waveforms of the 7L-FCC and 7L-HANPC are nearly identical, except for the ripple amplitude in the inductor current waveform during overload, which originates from the different switching frequency increase during overload operation (i.e., up to factor 3 for the 7L-FCC and factor 1.7 for the 7L-HANPC).

The measured key waveforms of all three phase module hardware demonstrators are shown in **Fig. 4.4** for nominal and overload operation at 300 Hz electrical output frequency with a mainly resistive load; including switching frequency increase for output currents above 15 A. Thereby, all measurements were performed in open-loop with phase-shifted PWM modulation, however, a closed-loop controller for the FC voltage balancing was implemented [78]. The baseplate where the respective PCBs are mounted is externally heated

to a temperature of 100 °C to thermally emulate the motor of the IMD system in a simple but effective manner. Under the same conditions electrical efficiency measurements are conducted with a Yokogawa WT3000 precision power analyzer, which according to measurements performed in [79] achieves highly accurate results exceeding its official specifications. The results for nominal and partial load operation are shown in **Fig. 4.5 (a)** achieving a final measured nominal efficiency of 98.90 % for the 7L-FCC, of 99.11 % for the 7L-HANPC and of 98.94 % for the 3L-FCC. The 7L-FCC and 3L-FCC closely match their target efficiency of 99 % and the additional losses (highlighted in yellow in the calculated loss breakdown of **Figs. 4.6 (a-c)** can be explained by ohmic resistances of, e.g, tracks, connectors and current measurement sensors, which have not been accounted for during the design process (corresponds to about 22 mΩ total resistance in the 7L-FCC and 15 mΩ in the 3L-FCC). The 7L-HANPC was designed to generate the same output voltage waveform as the 7L-FCC and thereby manages to exceed the 99 % efficiency mark. Mainly the chosen semiconductors of the ANPC stage have a lower R_{dson} than strictly necessary for the target efficiency at nominal load, since they were chosen for the thermally challenging overload operation.

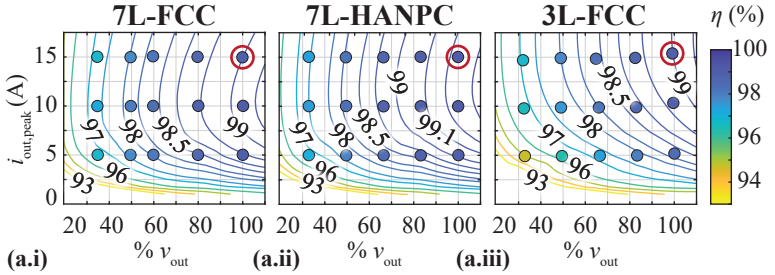


Fig. 4.5: (a.i)-(a.iii) Measured (dots) and calculated (lines) efficiencies for nominal and partial load operation at a baseplate temperature of 100 °C featuring the 7L-FCC, the 7L-HANPC and the 3L-FCC respectively. Thereby, the output voltage v_{out} of 100 % corresponds to 330 V peak amplitude for nominal output power. Hence, note that the nominal operating point, where the design target of minimum 99 % efficiency is defined, corresponds to the measurement at $i_{\mathrm{out,peak}}$ = 15 A and 100 % v_{out} (highlighted with a red circle). Note that partial load is measured for a fixed current with gradually reducing v_{out}. Simultaneously, the output frequency is linearly reduced with v_{out} (i.e., starting from 300 Hz at 100 % v_{out}), which corresponds to a practically relevant scenario, where a constant torque at reduced rotational speed is provided.

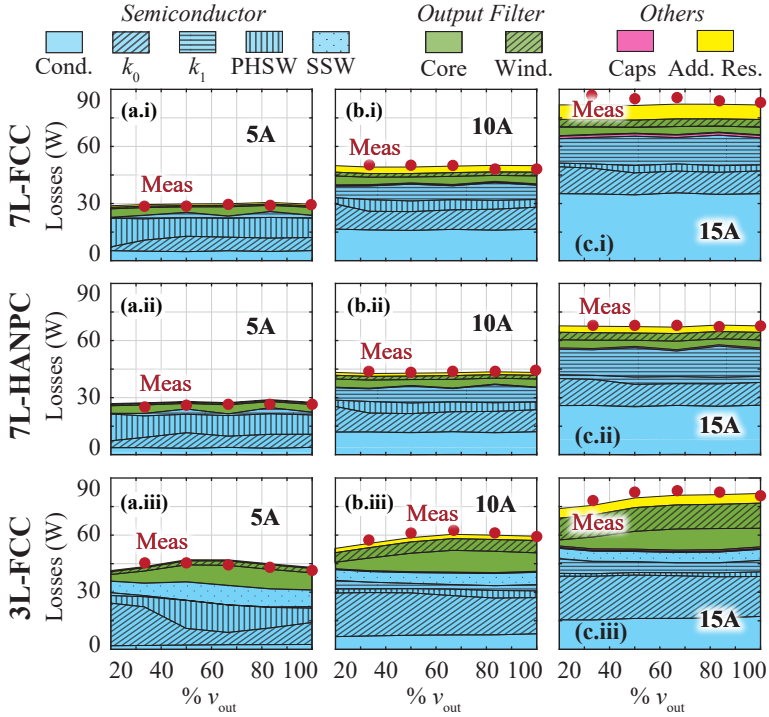


Fig. 4.6: Measured total losses and the calculated loss breakdowns for $i_{\text{out,peak}}$ = [5 A, 10 A and 15 A] are given in **(a.i)**, **(b.i)** and **(c.i)** for the 7L-FCC, in **(a.ii)**, **(b.ii)** and **(c.ii)** for the 7L-HANPC and in **(a.iii)**, **(b.iii)** and **(c.iii)** for the 3L-FCC. The semiconductor losses are colored in light blue with the pattern indicating the distinction between conduction losses ("Cond."), the HSW ("k_0", "k_1") according to $P_{\text{sw}} = k_0 + k_1 \cdot i_{\text{sw}} + k_2 \cdot i_{\text{sw}}^2$ [83], the Partial-Hard Switching ("PHSW") losses, and the Soft Switching ("SSW") losses. Note that these measurements correspond to the presented efficiencies in Figure 4.5.

Compared to the 3L-FCC, both 7L implementations (i.e., 7L-FCC and 7L-HANPC) show a flat loss characteristic over varying output voltage for the same current (cf. **Figs. 4.6 (a.i-c.i)** and **(a.ii-c.ii)**). Given the seven output voltage levels, the mean current ripple remains similar for most generated output voltages, and hence also the semiconductor switching losses and inductor core losses. As already discussed in [83] and clearly visible in **Figs. 4.6 (a.iii-c.iii)**, this is not the case for the 3L-FCC. Note also that the distribution between semiconductor switching and conduction losses in the

3L-FCC (cf. **Fig. 4.6 (c.iii)** in light blue) is dominated by the switching losses. According to [41] the optimum would be a more even distribution, which, however, could not be achieved with off-the-shelf power semiconductors and the overload operation constraints. Thus, a lower R_{dson} (i.e., larger die area) than optimal for nominal operation had to be chosen.

In **Figs. 4.7 (a-c)** thermal camera measurements taken during nominal and overload operation are shown. The Si MOSFET packages of the 7L-FCC and 7L-HANPC are directly visible, e.g., $T_{\mathrm{HS,3}}$ and $T_{\mathrm{LS,3}}$, while for the top cooled GaN HEMTs only the area where they are located on the bottom side of the PCB is discernible (highlighted box labeled with "Semi. ANPC" in **Figs. 4.7 (a.ii-c.ii)** or with "Semi." in **Figs. 4.7 (a.iii-c.iii)** respectively). The high efficiency and thus small losses during nominal operation (cf. **Fig. 4.7 (d.i)**) do not lead to visible hot spots in the thermal images of **Fig. 4.7 (a)**. However, a local temperature increase around the semiconductors can be seen after the 3 s short-term overload operation with 300 Hz electrical output frequency (cf. **Fig. 4.7 (b)**) due to the strongly increased losses shown in **Fig. 4.7 (d.ii)**. Note that due to the generated 300 Hz AC output voltage, the losses and thus also the resulting temperatures are expected to even out over all semiconductor devices, i.e., among others also over the visible packages of $T_{\mathrm{HS,3}}$ and $T_{\mathrm{LS,3}}$. However, mechanical tolerances during the assembly affect the cooling performance in particular and thus can lead to noticeable temperature differences causing uneven stress among the semiconductor devices. Finally, the motor standstill overload (i.e., DC output voltage) highlights the most critical operating point, as one single phase with a peak overload current of 45 A experiences similar losses as the sum of all three phases together in overload operation with rotation (cf. **Fig. 4.7 (d.iii)**). Consequently, thermal hot spots are clearly noticeable for all three prototypes, and as already discussed in detail in [83], the limited heat spreading of the baseplate has an additional impact, especially for the 3L-FCC. Note, however, that the multi-purpose PCB layout of the 3L-FCC leads to further heating in PCB tracks/vias and an even higher concentration of the thermal hot spots, which could be further optimized.

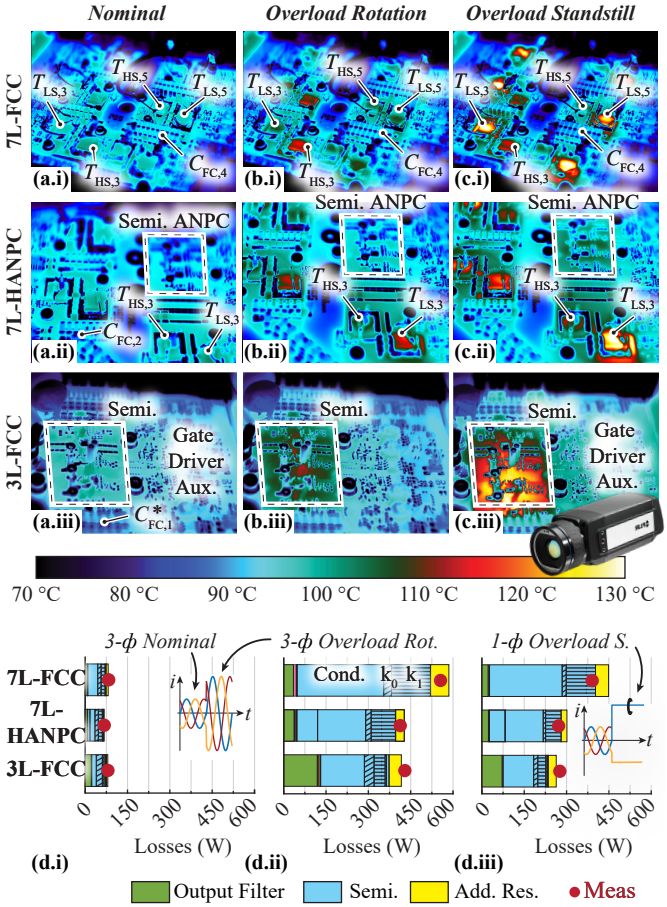


Fig. 4.7: Thermal Camera recordings at 100 °C baseplate temperature of **(a.i)-(a.iii)** nominal operation, **(b.i)-(b.iii)** overload operation with 300 Hz output frequency and **(c.i)-(c.iii)** overload motor standstill operation with 0 Hz output frequency. Note that besides the limited heat spreading in the mounting baseplates combined with high concentration of losses during standstill overload, the PCB tracks and vias of the 3L-FCC are additionally heated due to the multi-purpose PCB layout. **(d.i)-(d.iii)** features the measured losses (red dots) during the different operations together with the calculated loss breakdowns, where "Semi." (colored in light blue) represents the semiconductor losses, which are further divided in conduction and switching losses using the patterns as specified in **Fig. 4.6**.

4.4 Comparative Evaluation

All three hardware prototypes have been built for the same specifications, operate at similar nominal efficiencies and have been tested in nominal and overload operation under the same conditions with a baseplate temperature of 100 °C. This allows an overall comparison visualized in the the radar chart of **Fig. 4.8**. In the following, the main aspects are briefly discussed.

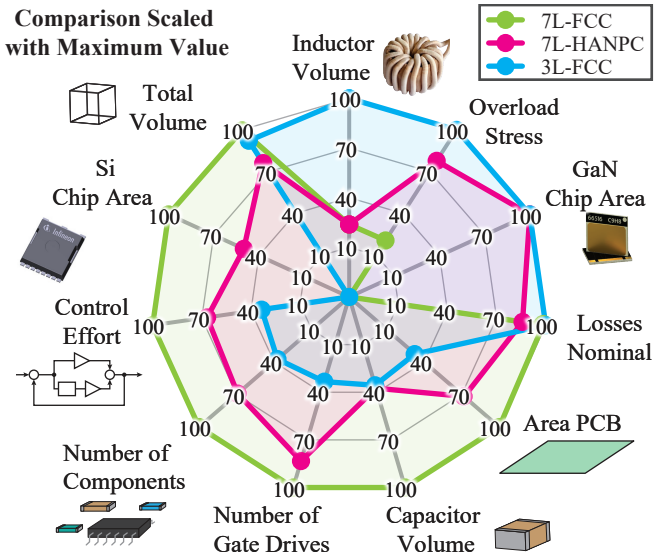


Fig. 4.8: Radar chart indicating key characteristics of the 7L-FCC (green), 7L-HANPC (magenta) and 3L-FCC (blue) built hardware demonstrators of **Fig. 4.2**. 100% corresponds to the maximum value of each category. For a three-phase realization these maximum values are given in the following: Total Volume = 0.33 dm^3 (7L-FCC), Inductor Volume = 0.17 dm^3 (3L-FCC), Capacitor Volume = 0.052 dm^3 (7L-FCC), Area PCB = 5.5 dm^2 (7L-FCC), GaN Chip Area = 652.8 mm^2 (7L-HANPC/3L-FCC), Si Chip Area = 1044 mm^2 (7L-FCC), Number of Gate Drives = 36 (7L-FCC), Number of Components = 2616 (7L-FCC) and Losses Nominal = 75.5 W (7L-FCC). The Control Effort is quantified as number of passive components to be controlled, resulting in 18 units (7L-FCC) for 100 %. The overload stress is defined as inverse of the remaining temperature budget to the maximal allowed junction temperature when peak current is provided during standstill overload. In this case the 100 % value corresponds to 1/7 °C (3L-FCC).

4.4.1 Mechanical Dimensions and Realization Efforts

The obvious benefit of higher number of levels (e.g., 7L) over lower levels (e.g., 3L) is the reduced output filter volume, which is dominated by the filter inductor. While the required inductance value for the same current ripple at nominal load drops by a factor 6 from 120 µH (3L-FCC) to about 20 µH (7L-FCC/7L-HANPC), the inductor volume only reduces by a factor of 4, mainly due to the available core dimensions and the chosen surface cooling, which limit the possible reduction in size. As clearly visible in the schematics of **Fig. 4.1**, the small inductor volume comes at the cost of an increased number of switches and capacitive energy storage units. While both can be recognized in the radar chart of **Fig. 4.8** for the 7L-FCC in form of a high number of gate drives and a large total capacitor volume, the latter nearly coincides for the 7L-HANPC with the 3L-FCC capacitor volume. Even tough the 7L-HANPC has an additional flying capacitor unit, its higher f_{sw} allows a reduced HF DC-Link volume, while the volume of the flying capacitors itself is relatively small (and rather thermally limited), due to the large capacitance/volume density of the Class II ceramic capacitors at lower voltages (i.e., for 133 V and 266 V). Nevertheless, the 3L-FCC shows a clear advantage in terms of a small total number of components (includes besides semiconductors and capacitors also all Surface-Mount Devices (SMDs) of the measurement circuits, gate drives, etc.), which strongly correlates with the required PCB area. All in all, the total achievable volumes are fairly similar with a slight advantage for the 7L-HANPC.

4.4.2 Chip Area

Due to the challenging temperatures close to the motor (T_{case} = 90 °C) and the required short-term overload torque semiconductors with low R_{dson} values are required for all three prototypes. The corresponding measured device die areas (i.e., packaging removed) of the chosen power transistors are given in **Table 4.3**. In order to achieve the low R_{dson} values for the 650 V GaN semiconductors (employed in the 3L-FCC and also in the ANPC stage of the 7L-HANPC), paralleling is required, effectively doubling the total semiconductor chip area of the three-phase inverter to 652.8 mm^2 compared to a design where only efficient nominal operation would be required. Similarly, with a total die area of 1044 mm^2 for 200 V Si MOSFETs in the 7L-FCC and 522 mm^2 in the 7L-HANPC, devices with a larger R_{dson} could have been considered (as can be seen in [83]), and thus reducing the total chip area.

4.4.3 Control Effort

With today's digital control approaches, e.g., utilizing Field-Programmable Gate Arrays (FPGAs), the modulation of a large number of switches is a relatively simple task and hence does not heavily contribute to the overall control effort. However, the flying capacitors must be actively balanced as natural balancing might be insufficient [84–86] and passive balancing concepts [87] result in additional losses and volume. Thus, the number of energy storage elements that need to be controlled increases with the number of flying capacitors to be balanced. Realization-wise, separate voltage sensors (as here) or "advanced" methods based on output current or output voltage measurements [88, 89] are needed to detect imbalances in the voltages. While the selected measurement approach affects the required total number of components, it does not change the number of energy storage elements that need to be managed, which is therefore a good measure for the encountered control effort. Obviously, the filter inductors are a common additional energy storage element in all three prototypes, as their currents need to be actively regulated according to the required motor supply voltage and finally motor torque. The voltage of the (HF) DC-Link capacitors is directly enforced by the DC grid/source for the 7L-FCC and 3L-FCC. In contrast, the 7L-HANPC involves the (floating) DC-Link midpoint (also called Neutral Point) in the output voltage generation, which consequently represents an additional energy storage element to account for [90, 91]. All in all, the resulting measure of control effort highlights the comparatively small complexity of the 3L-FCC (i.e., 6 units for three phases), which increases with the 7L-HANPC and is highest for the 7L-FCC (with 18 units for three phases).

4.4.4 Overload Stress

In [83] a detailed thermal Cauer model for the 3L-FCC has been elaborated, including the heat spreading in the baseplate extracted from FEM thermal simulation. With this dynamic thermal model and the (temperature dependent) semiconductor losses the expected transient peak junction temperature could be approximated. This method is used to introduce a measure of overload stress, which considers the reciprocal of the difference between maximum allowed and the calculated semiconductor junction temperature for the worst case overload operation at standstill. Overall, the 3L-FCC encounters a higher overload stress with the 650 V GaN semiconductors, which are only rated up to 150 °C, compared to the 200 V Si MOSFETs rated up to 175 °C. Combined with non-ideal heat spreading and the high loss density in the 3L arrangement

this results in a calculated margin of only 7 °C. However, the overload stress could be further reduced by more elaborated cooling approaches such as, e.g., heat pipes and heat spreaders, but additional effort compared to the 7L implementations would be required and/or the peak current for standstill overload could be reduced as suggested in [83].

4.4.5 Summary of the Comparative Evaluation

Everything considered, similar nominal efficiencies of around 99 % are achieved for all three solutions. The 7L-FCC offers a small inductor volume at the price of a large capacitor volume, numerous gate drives, semiconductors and overall components, which require a spacious PCB to accommodate. Furthermore, for a three-phase system in total 18 passive energy storage elements need to be regulated, resulting in a comparatively high control effort. With the introduction of the 7L-HANPC, not only the efficiency can be slightly improved, but also most other metrics as for example the number of components, the capacitor volume and the control effort. However, the complexity is still not comparable to the 3L-FCC implementation. Since the overall volumes are similar for all proposed solutions, the main drawback of the 3L-FCC lies in a constrained form factor (defined by the relatively large filter inductor volume), which determines in some cases the minimal achievable height of the power electronics of the IMD.
Of course, future trends develop towards more device integration (e.g., Integrated Power Modules (IPM) and Bipolar-CMOS-DMOS (BCD) technologies), where the gate drive and the power semiconductor are integrated on a single chip and/or in a single package. This will strongly lower the number of discrete components in a 7L implementation while simultaneously lowering the required PCB area. However, even tough the 7L implementations will benefit more from this trend, the number of discrete components will inevitably exceed those of the 3L-FCC drive, and thus result in a lower reliability. Moreover, the control effort, which correlates with the number of energy storage elements such as flying capacitors, will be unaffected by future device integration.

4.5 Proposed 3L-FCC IMD Realization

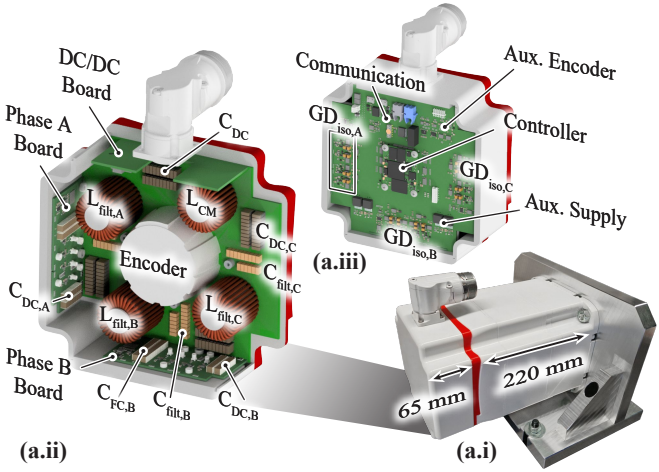


Fig. 4.9: Motor-integrated 3L-FCC design. **(a.i)** Axial extension of the motor housing by 65 mm for inverter placement. **(a.ii)** Proposed arrangement of the IMD, where the modular power stages (i.e., Phase A Board, Phase B Board and Phase C Board) are directly mounted onto the elongated motor case for improved semiconductor cooling. The output filter as well as additional distributed DC-Link capacitance are placed around the encoder, while the DC/DC board provides a 800 V to 24 V voltage conversion for supplying measurement, control, and gate drive circuits of the IMD. **(a.iii)** View on the Top-PCB, which accommodates the isolated gate drive circuits (i.e, $GD_{iso,A}$, $GD_{iso,B}$ and $GD_{iso,C}$), controller, and communication as well as auxiliary circuits.

Highlighting the very interesting overall trade-offs of the 3L-FCC, a possible IMD realization is shown in **Fig. 4.9**. The dimensions of motor and 3L-FCC allow mounting of the power boards (i.e., PCBs that include semiconductors, non-insulated gate drives, flying capacitors, local HF DC-Link capacitors and the inductor current measurement) directly on the walls of the elongated motor case (cf. **Fig. 4.9 (a.ii)**). This results in a superior (dynamic) cooling performance for the temperature critical semiconductors. The gate drive insulation (labeled as GD_{iso} in **Fig. 4.9 (a.iii)**), voltage measurements, controller and auxiliaries (low voltage supplies, encoder, communication interface, etc.) can be placed on an additional PCB on top as no or limited cooling is required. As a side remark, the controller is usually a thermal hot-spot which

in this case can be cooled directly through a TIM over the case of the IMD. The *LC* output filters, additional distributed DC-Link capacitors as well as a possible CM filter inductor (L_{CM}) to limit the CM EMI emissions into the supplying DC grid [32, 73] are placed around the encoder. Last but not least, a DC/DC board visible in **Fig. 4.9 (a.ii)** is mounted to the remaining wall and accommodates a 800 V to 24 V power conversion circuit to supply the low voltage electronics directly from the DC-Link. This proposed IMD solution results in a motor case elongation of only 30 %, which is typically acceptable in industrial installations.

4.6 Summary

In this chapter, three three-phase AC/DC converter hardware prototypes, namely a 7L-FCC, a 7L-HANPC and a 3L-FCC, have been build for the same specifications of an 800 V supplied, 7.5 kW IMD. Thereby, high operating temperatures of the naturally cooled motor (T_{case} = 90 °C) require high nominal efficiencies of the converter stage (around 99 %) and a low transient thermal impedance of the semiconductor cooling for the short-term overload operation (i.e., 3 times nominal current for 3 s). In order to minimize the volume of the demonstrators, an additional increase in switching frequency during overload operation is implemented, which allows to dimension the passives (e.g., flying capacitors and filter inductors) mainly for nominal operation. All three demonstrators have been tested with 100 °C baseplate temperature (incorporates an expected 10 °C temperature difference to the 90 °C motor case) for nominal and overload operation, including the challenging 3 s motor standstill overload with three times the nominal peak current flowing continuously in one phase, i.e., with a DC output voltage and peak losses in one single phase.

All in all, the 3L-FCC meets the nominal and overload design targets with a similar total volume as the alternatively considered 7L topologies, although with a different form-factor. Advantageously, it has the lowest complexity in terms of control effort and, due to the small number of discrete components, the highest reliability can be expected, i.e., the 3L-FCC features the most interesting overall trade-offs.

5

Comparative Evaluation of Three-Phase Three-Level Flying Capacitor and Stacked-Bridge Polyphase GaN Inverter Systems for Integrated Motor Drives

This chapter summarizes the most relevant findings of a comprehensive comparison between an SPBI, more specifically a 2L-SSC, and a 3L-FCC for a motor integrated design also published in:

- **G. Rohner**, J. Huber, S. Mirić and J. W. Kolar, "Comparative Evaluation of Three-Phase Three-Level Flying Capacitor and Stacked-Bridge Polyphase GaN Inverter Systems for Integrated Motor Drives," in *Electronics*, vol. 13, no. 7: 1259, 2024.

Motivation

Investigating alternative topologies with identical semiconductor effort as the best-performing 3L-FCC, the implementation of a 2L-SSC is an interesting option. It requires a modification of the motor from a single three-phase winding-set to a dual three-phase winding-set machine with two separate open star points. However, this approach has the distinct advantage of eliminating the critical FCs from the design. Furthermore, the 2L-SSC offers a straightforward CM cancellation capability, which is especially advantageous when foregoing a full sine-wave *LC* filter and concentrating on a CM choke design. These aspects serve as compelling motivation for a detailed comparison between the 2L-SSC and 3L-FCC.

Executive Summary

This chapter presents a comprehensive comparative evaluation of a three-phase Three-Level (3L) Flying Capacitor Converter (FCC) and a SPBI, specifically a converter system formed by two Series-Stacked Two-Level three-phase Converters (2L-SSC), for the realization of a 7.5 kW IMD with high short-term overload capability. The 2L-SSC requires a motor with two three-phase windings and a symmetrically split DC-Link, but then, advantageously, uses standard six-switch, two-level transistor configurations. In contrast, the bridge-legs of the 3L-FCC feature flying capacitors whose voltages must be actively balanced. Despite the 800 V DC-Link voltage, both topologies employ the same set of state-of-the-art 650 V GaN power transistors, i.e., the same total chip area, and if operated at the same switching frequency, show identical semiconductor losses. In IMDs, EDM damage of the motor bearings is amongst the most relevant issues caused by the common-mode (CM) voltages of the inverter stage. The high effective switching frequency of the 3L-FCC and the possibility of CM voltage canceling in the 2L-SSC facilitate a mitigation of EDM by means of CM chokes, whereby a substantially smaller CM choke with lower losses suffices for the 2L-SSC even when non-ideal CM cancellation is considered; based on exemplary designs with identical specifications and constraints, the 2L-SSC features only about 75% of the volume and 85% of the nominal losses of the 3L-FCC. If, alternatively, motor-friendliness is maximized by including DC-referenced sine-wave output filters, the 3L-FCC's higher effective switching frequency and the 2L-SSC's need for two sets of filters due to the dual-winding-set motor change the outcome. In this case, based on exemplary designs, the 3L-FCC features only about 60% of the volume and only about 55% of the 2L-SSC's nominal losses.

5.1 Introduction

In the previous chapters, the motor is shielded from the power electronics stage by a full sine-wave *LC* output filter. However, for the best-performing 3L-FCC the required filter inductors clearly dominate the volume distribution and lead to additional costs. Alternatively, foregoing such comprehensive motor protection, one can also selectively employ, e.g., dv/dt -filters [92, 93] to limit the rise and fall times of the voltage transitions of WBG inverters at the motor terminals, and DM or CM-filters separately to reduce the respective

Tab. 5.1: Specifications of the analyzed Integrated Motor Drive (IMD) extending the specifications presented in **Table 1.1**.

Parameter		Value
Device Switching Frequency	f_{sw}	35 kHz
Max. Peak CM Volt. at the Motor	$v_{x,max}$	1 % of V_{DC}
Max. Peak-Peak DC-Link Volt. Ripple	$\Delta V_{DC,max}$	1 % of V_{DC}
Max. Peak-Peak FC Volt. Ripple	$\Delta V_{FC,max}$	10 % of $V_{DC}/2$

voltage components from the PWM inverter output that otherwise are applied to the motor directly.

Advantageously, compared to standard two-level inverters, implementing the motor drive as a multi-level inverter, even without full sine-wave *LC* output filter, the lower voltage steps at the switch-node output benefit the motor with lower output voltage harmonics (and thus lower HF motor losses), as well as lower winding voltage stresses [40, 94, 95].
Yet, as demonstrated in preceding chapters, increasing the number of levels leads to significantly higher complexity, and hence, mainly three-level topologies are established also in industrial applications. Prominent three-level topologies are, first, T-type concepts that, however, employ two different types of transistors (i.e., with different voltage blocking capabilities) [96, 97]. Second, diode-clamped structures like the neutral-point-clamped (NPC) converter [98, 99], or, replacing the diodes with transistors, active NPC (ANPC) bridge-legs are widely used in high-power applications. However, there, six instead of only four power semiconductors per bridge-leg are needed. These are clear disadvantages compared to an implementation with a 3L-Flying Capacitor Converter (3L-FCC) shown in **Fig. 5.1(a)**, which uses capacitors for defining additional voltage levels. It features bridge-legs with only four transistors of a single type that are equally stressed in steady-state operation. As highlighted in previous chapters, an 800 V DC-Link system can be realized with the latest 650 V GaN power semiconductor technology, featuring low chip area, low R_{dson}, and low switching losses. This facilitates a small inverter stage footprint and a high power conversion efficiency, both fundamentally important for the motor integration of the inverter.

Yet, as discussed, overload operation requirements such as three times the rated torque for 3 s as expected from motor drives in, e.g., servo applications [20], can only be handled with relatively large FCs to keep the maximum FC voltage ripple amplitude and/or the losses per capacitor below the design limits. The latter can be avoided by increasing the switching frequency

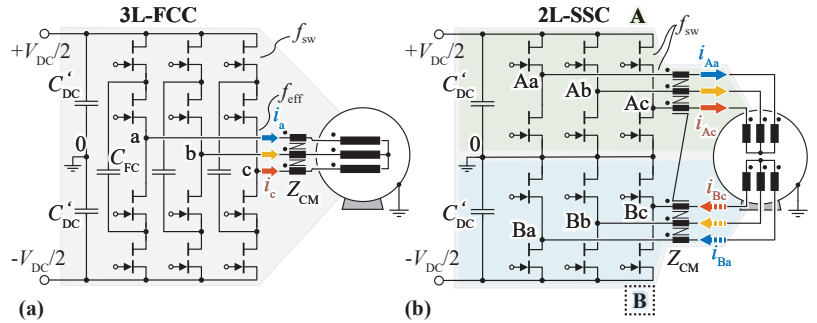


Fig. 5.1: (a) Schematic of 3L-Flying Capacitor Converter (3L-FCC) supplying a three-phase single-winding-set PMSM via a three-phase CM choke. **(b)** Schematic of the Stacked Polyphase Bridge Inverter (SPBI) IMD, realized in the form of a two Series-Stacked Two-Level three-phase Converter (2L-SSC), supplying a dual-winding-set PMSM via a six-phase CM choke. In order to achieve CM voltage cancellation, the switching pattern of inverter B is inverse to inverter A, which results in an opposite phase current flow. Identical torque direction in the PMSM is then achieved by reversing the winding direction of the second winding set (note the dots indicating the winding directions).

in overload periods, which, however, increases implementation complexity. Moreover, the FC voltages might require active control due to shortcomings in the natural balancing behavior when operated with, e.g., non-ideal source impedances, gate drive delays, and input voltage startup/fluctuations [84–86], which adds to the previously mentioned complexity.

Accordingly, alternative inverter concepts are of interest, such as the Stacked Polyphase Bridge Inverter (SPBI): In the case at hand, two three-phase Two-Level inverter stages are stacked, i.e., connected in Series on the DC input side 2L-SSC and each inverter stage supplies an individual three-phase winding set of the motor (cf. **Fig. 5.1(b)**) [100–106]. Advantageously, a 2L-SSC with an 800 V DC input can also employ latest 650 V GaN semiconductors configured in standard two-level half-bridge arrangement, and requires the same number of transistors as a 3L-FCC, but no FCs. Instead, it uses a split DC-Link which is common to all three phases. Note that the 2L-SSC requires a non-standard motor with two three-phase winding systems. For IMDs, this is a limited drawback as there are no long motor cables and no additional external machine terminals, and because a co-design of drive and motor can (and should) be employed for optimum performance [15].

Besides the promising elimination of the FCs, the 2L-SSC's two three-phase inverter stages offer the possibility of mutual CM voltage cancellation similar to [107, 108]. In general, PWM operation of any three-phase inverter stage results in a switched CM voltage at the output terminals. If no output filter is used, the CM voltage is applied to the motor windings and can cause undesired ground leakage currents, conducted and radiated EMI issues, and bearing currents [27, 109]. Whereas the first two aspects are more straightforward to solve in IMDs, where the arrangement of motor and inverter in a single housing without long motor cables facilitates local grounding schemes [110], the issue of bearing currents must still be addressed: Among the different types of bearing currents, the most critical are EDM bearing current pulses, which can damage the motor bearings over time [109]. While mitigation methods such as grounding brushes or insulated bearings can prevent EDM, they suffer from mechanical wear and tear and/or reduced mechanical stability.

Alternatively, the limitation of the CM voltage at the motor to small voltage levels can prevent EDM current pulses with destructive energies from occurring (a more detailed discussion is available in [109]). As investigated in [111], the critical voltage over the bearing for EDM typically is between 1.5 V and 30 V; [109] reports a similar range. Thereby, the voltage over the bearing itself is typically only about 10% of the total applied CM voltage at the motor [111] due to the capacitive voltage divider ratio of the involved parasitic motor capacitances. This leads to a maximum allowed CM voltage of 15 V at the motor terminals. Considering a 50% design safety margin, a maximum CM voltage at the motor of approximately $v_{\mathrm{x,max}} = 8\,\mathrm{V}$ (i.e., 1% of the DC-Link voltage) is considered here **Table 5.1**[1].

With a 3L-FCC such low CM voltage levels at the motor can only be achieved by either using a full sine-wave DC-bus-referenced DM/CM *LC* output filter [111] or (as a main focus of this chapter) by employing a large CM impedance Z_{CMC} (i.e., forming a voltage divider between a CM choke, which is designed for this purpose, and the (capacitive) motor CM impedance), as indicated in **Fig. 5.1(a)** and **Fig. 5.2(a)**.

On the other hand, assuming a symmetric motor design, i.e., the two three-phase winding sets feature identical capacitive coupling to the rotor and the motor frame, the two inverter stages of the 2L-SSC can be controlled in a straightforward way to almost completely eliminate the generation of a

[1]Note that specific values for safe CM voltage levels at the motor may depend on the specific motor and operating conditions [109]; the values considered here is deemed a conservative example.

mutual CM voltage in the first place, as mentioned above. Consequently, only a comparably small additional series CM impedance Z_{CMC} might be needed to account for possible non-idealities in the CM voltage cancellation.
Note that utilizing CM chokes to mitigate EDM in motor drives as targeted in this section is not a standard solution. In fact, many publications show that inserting a CM choke between the inverter and the motor can only reduce earth leakage current peaks, but has no influence on the voltage across the bearings and, therefore, no influence on the occurrence of EDM [33,111]. However, looking at such typical CM choke designs with a low number of turns combined with low device switching frequencies, the resulting impedances are orders of magnitude too small to achieve the required voltage division ratio between CM choke impedance and motor CM capacitance proposed in this chapter. In other words, targeting a high-impedance CM choke design for a standard 2L drive system would result in very large component volumes as (1) the CM voltage quality of a 2L inverter is considerably worse compared to a 3L converter (as shown later in **Fig. 5.4 (a)**), and (2), especially when implemented with IGBTs, a low switching frequency (e.g., in the range of several kHz) will render a specifically for this purpose designed CM choke completely impractical/impossible.

All in all, both topologies, the 3L-FCC and the 2L-SSC are interesting candidates, e.g., featuring identical semiconductor effort and losses, for a 7.5 kW PMSM servo drive system with specifications as given in **Table 1.1** and **Table 5.1**. However, a detailed comparison of the advantages and weaknesses when aiming for motor integration under the side condition of high transient overload capability required by servo drives, high operating temperatures as a consequence of the close proximity to the motor, and the limitation of the CM voltage at the motor to prevent EDM damage to the bearings is still missing.

Therefore, this chapter first explains the operating principles of the 3L-FCC and the 2L-SSC in **Section 5.2**, focusing on the resulting CM voltage generation. Subsequently, in **Section 5.3** both topologies are designed for the specifications given in **Table 1.1** and **Table 5.1**, again with a focus on the CM choke. This enables the comparison of the 3L-FCC and the 2L-SSC IMD with CM choke presented in **Section 5.4**. Targeting a comprehensive analysis, this section also contains an evaluation of the two topologies when realized in combination with a full sine-wave *LC* filter. Finally, **Section 5.5** concludes the chapter.

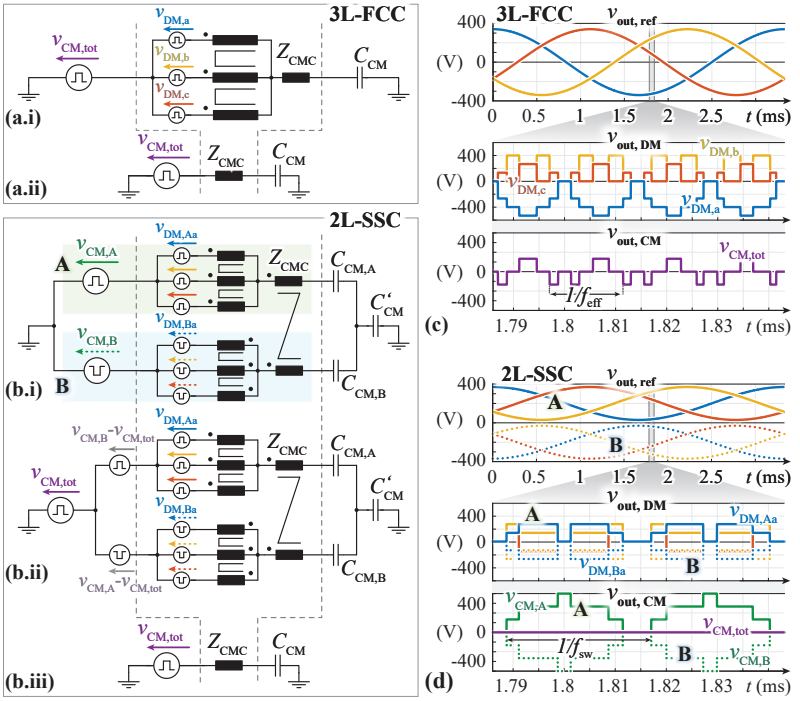


Fig. 5.2: (a.i) Equivalent circuit of the 3L-FCC with separation of the relevant CM and DM components, and **(a.ii)** CM equivalent part only. The PMSM is modeled as a CM capacitance C_{CM} to ground, which represents the motor CM impedance in the frequency range of interest, i.e., around the (effective) switching frequency, see *Section 5.3.4*. **(b.i)** Equivalent circuit of the 2L-SSC with two separate CM and DM sources representing inverters A and B, respectively. The CM voltages are further summarized in **(b.ii)**, which results in the overall CM equivalent circuit in **(b.iii)**. **(c)** Characteristic CM and DM waveforms of the 3L-FCC. **(d)** Characteristic CM and DM waveforms of the 2L-SSC: note how the inverse switching patterns of inverters A and B ideally result in a complete cancellation of the CM voltage ($v_{CM,tot} = 0$).

5.2 Operating Principles

This section provides a brief overview of the operating principles of the 3L-FCC and the 2L-SSC, including the possibility of achieving mutual CM cancellation with the latter for a symmetric motor design. Subsequently, the resulting CM output voltages generated from both topologies are discussed and analytically compared over a full output voltage/current fundamental period.

5.2.1 3L-FCC

The 3L-FCC depicted in **Fig. 5.1(a)** utilizes two half-bridge cells per phase (i.e., four switches in total, each required to block only half the total DC-Link voltage V_{DC}) and a Flying Capacitor C_{FC} to provide three output voltage levels. The effective frequency f_{eff}, which is measured at the switch node advantageously is twice the device switching frequency, i.e., $f_{\mathrm{eff}} = 2 \cdot f_{\mathrm{sw}}$.

The third output voltage level is generated by including the FC in the output current path. Consequently, within a (device) switching period, the FC is charged and subsequently discharged again with the output current for a maximum duration of one effective switching period [50]. This leads to a certain (peak-to-peak) voltage ripple amplitude of ΔV_{FC} around the nominal DC value of the FC voltage, which is $V_{\mathrm{DC}}/2$. During operation, said DC voltage value is ideally maintained by the natural balancing capability when employing Phase-Shifted PWM (PSPWM). However, in reality, natural balancing might not suffice [84–86], and consequently, active balancing concepts of the FCs [78, 88] must be implemented to guarantee reliable performance of the motor drive.

As shown in the equivalent circuit of **Fig. 5.2(a)**, the switched three-level output voltages provided to the motor can be separated in a CM ($v_{\mathrm{CM,tot}}$) and in three DM components ($v_{\mathrm{DM,a}}$, $v_{\mathrm{DM,b}}$ and $v_{\mathrm{DM,c}}$). With a focus of this section on the CM voltage limitation at the motor terminals, the final CM equivalent circuit is depicted in **Fig. 5.2(a.ii)**. Note that the CM impedance of the motor is represented with a CM capacitance C_{CM} only; this is a useful approximation which will be discussed in *Section 5.3.4*. The respective switched CM and DM waveforms are shown in **Fig. 5.2(c)** for a small section of the sinusoidal output voltage references $v_{\mathrm{out,ref}}$. Thereby, the CM voltage $v_{\mathrm{CM,tot}}$ attains values between $\pm V_{\mathrm{DC}}/6 = \pm 133\,\mathrm{V}$.

5.2.2 2L-SSC

The 2L-SSC in **Fig. 5.1(b)** consists of two standard three-phase 2L inverters (i.e., hereinafter called inverter A (blue in **Fig. 5.1(b)**) and inverter B (green) connected in series at the DC side such that each 2L inverter is supplied with half the total DC-Link voltage. Consequently, the same transistor count as in the 3L-FCC results, and the transistor blocking voltages are identical, too. The two inverters drive a dual-winding-set motor with two three-phase winding systems: The first three-phase winding is connected to inverter A and the second to inverter B. Both inverters provide the same output phase current levels as the 3L-FCC but at only half of the 3L-FCC's phase voltages. Thus, in total, the same output power and torque as in the single three-phase winding machine driven by the 3L-FCC results.

A balanced DC-Link voltage mid-point (marked with "0" in **Fig. 5.1(b)**) is a necessary condition for the successful operation of the 2L-SSC throughout the motoring and generating mode of the PMSM. When employing Common-Duty-Ratio Control [112], i.e., only the output currents of inverter A are actively controlled and inverter B uses the identical switching pattern, the DC-Link voltage mid-point is asymptotically stable for initial voltage offsets and DC-Link voltage steps. However, in the case of slightly asymmetric machine parameters (i.e., especially minor differences in motor inductance and/or back-EMF of 1%-2%) the steady-state DC-Link voltage will have an offset, and, even more problematic, the open-loop currents in inverter B will not necessarily generate the expected output torque anymore. Consequently, active balancing is of interest, where the DC-Link midpoint voltage can be regulated over a shift in output power from one inverter to the other [105,113,114]. In Field-Oriented Control (FOC), this can be achieved by altering the otherwise identical q-current component references of the two inverters, which will result in slightly different output voltage references. Note, however, that due to substantially symmetrical industrial motor designs, the required shift in power, i.e., the variation of output voltage reference, is expected to be small.

In **Fig. 5.2(b)**, the corresponding equivalent circuit using the switched output voltages is shown with separated CM and DM contributions. Again, as will be discussed later, the motor CM impedance is capacitive for the frequency range of interest. Thereby, the motor CM capacitances are split into $C_{\mathrm{CM,A}}$, $C_{\mathrm{CM,B}}$ (taking into account the direct coupling between the two adjacent stator winding systems) and C'_{CM} (taking into account the coupling of these windings via the rotor, and the coupling to the motor housing/earth) [111]. Deriving the total CM voltage from the CM voltages of inverter A ($v_{\mathrm{CM,A}}$) and

of inverter B ($v_{CM,B}$) yields

$$v_{CM,tot}(t) = \frac{v_{CM,A}(t) + v_{CM,B}(t)}{2}. \tag{5.1}$$

The CM equivalent circuit in **Fig. 5.2(b.iii)** follows directly, with the total motor CM capacitance C_{CM} representing the series connection of ($C_{CM,A}$ + $C_{CM,B}$) and C'_{CM}.

Consequently, in order to achieve mutual CM cancellation, i.e., $v_{CM,tot}(t) = 0$, inverter A and inverter B must be driven by complementary output voltage references $v_{out,ref}$, which result in complementary switching patterns that lead to $v_{CM,A}(t) = -v_{CM,B}(t)$ as shown **Fig. 5.2(d)**. As a side effect, the phase currents of inverter B flow in the opposite direction compared to those of inverter A. This requires that one of the motor's winding systems is connected with reversed winding direction (indicated by dots representing the respective winding start in the schematics of **Fig. 5.1(b)**) such that both windings generate torque components in the same direction.

5.2.3 Quantitative Comparison of Resulting CM Voltages

In order to put the generated output CM voltages of the 3L-FCC and the 2L-SSC quantitatively into perspective, the total RMS value $V_{CM,rms}$ can be computed over a fundamental output voltage period. For comparison, a state-of-the-art six-switch 2L inverter with conventional Space Vector PWM (SVPWM) leads to a total CM RMS voltage [115] of

$$V_{CM,rms,2L} = \sqrt{\frac{(3 \cdot \pi - 4 \cdot \sqrt{3} \cdot M) \cdot V_{DC}^2}{12 \cdot \pi}}, \tag{5.2}$$

whereas equivalent considerations for the 3L-FCC with conventional PSPWM result in

$$V_{CM,rms,3L} = \sqrt{\frac{(2 - \sqrt{3}) \cdot M \cdot V_{DC}^2}{6 \cdot \pi}}; \tag{5.3}$$

both RMS voltages vary with the modulation index M (i.e., $M = V_{out}/(V_{DC}/2)$ with V_{out} as the phase output voltage amplitude referenced to the DC-midpoint (marked with "o" in **Fig. 5.1(a)**). Thanks to the higher number of output voltage levels, a remarkable reduction in $V_{CM,rms}$ of the 3L-FCC compared to a 2L inverter is achieved, which is visualized in **Fig. 5.4(a)** when operated with a DC-Link voltage of $V_{DC} = 800\,V$ according to **Table 1.1**. Especially for low

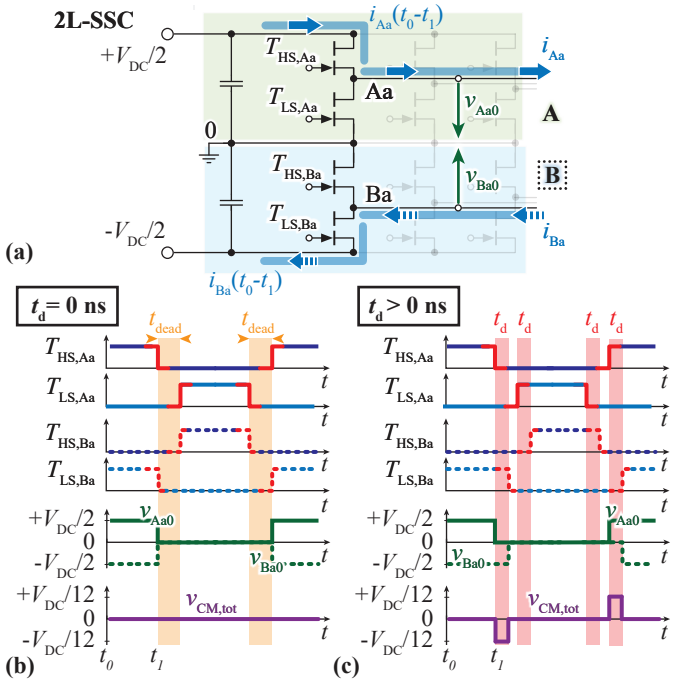


Fig. 5.3: (a) 2L-SSC circuit with the amplitude-wise identical but 180° phase shifted phase currents i_{Aa} and i_{Ba}. The current flowing through the semiconductors is shown for the time interval t_0 to t_1 for the respective switching states defined in **(b)** and **(c)**. **(b)** Inverted on/off signals (e.g., $T_{\mathrm{HS,Aa}}$ and inverted $T_{\mathrm{HS,Ba}}$) required for CM cancellation, and resulting switch-node voltages (v_{Aa0} and v_{Ba0}) and total CM voltage ($v_{\mathrm{CM,tot}}$). The dead time t_{dead} does not lead to a misalignment of the switch node voltage transitions, and hence, (ideal) CM cancellation is possible. **(c)** Switching signals and resulting voltages when a delay $t_{\mathrm{d}} > 0$ ns between inverter A and inverter B occurs, i.e., all on/off signal transitions of inverter B lag inverter A by t_{d}. The resulting misalignment of the switch node voltage transitions leads to a non-zero CM voltage $v_{\mathrm{CM,tot}}$ with a CM voltage spike of duration t_{d} at each transition. Note that the same dead time t_{dead} as in **(b)** is used.

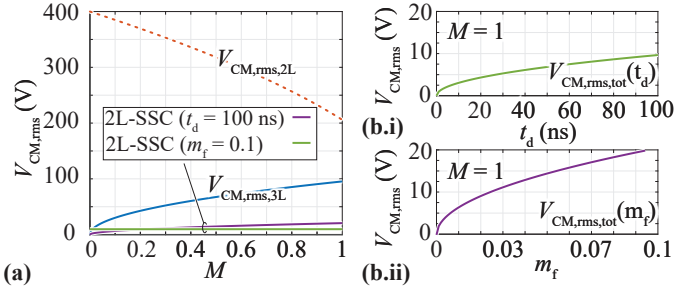


Fig. 5.4: (a) Analytically derived total CM RMS voltages $V_{\mathrm{CM,rms}}$ for a fundamental output voltage period over varying modulation index M for $V_{\mathrm{DC}} = 800\,\mathrm{V}$ and $f_{\mathrm{sw}} = 35\,\mathrm{kHz}$: State-of-the-art 2L inverter, 3L-FCC, and two curves for 2L-SSCs with non-ideal CM cancellation (one features a delay of inverter B's gate signals by 100 ns compared to inverter A, and the other requires a balancing correction factor of $m_{\mathrm{f}} = 0.1$). **(b.i)** Sensitivity of $V_{\mathrm{CM,rms}}$ of the 2L-SSC with respect to varying delays of inverter B's gate signals compared to A for a fixed M. **(b.ii)** Sensitivity of $V_{\mathrm{CM,rms}}$ of the 2L-SSC with respect to a varying balancing correction factor m_{f} for a fixed M.

M, the third output voltage level of the 3L-FCC enables a massive reduction in $V_{\mathrm{CM,rms}}$.

In the 2L-SSC, theoretically ideal CM voltage cancellation is possible as shown in **Fig. 5.2(d)**. It is important to note that the introduction of dead times t_{dead} (interlock delay times needed between turning off a first of the half bridge's transistors and turning on the complementary transistor of the bridge-leg) has (ideally) no impact on the CM voltage cancellation capability of the 2L-SSC. The output currents in both inverters are nearly identical in amplitude but 180° out of phase, which ensures aligned switching transitions of the switch-node voltages of inverters A and B despite the dead time. This is exemplarily shown in **Fig. 5.3(b)** for the current directions indicated in **Fig. 5.3(a)**.

However, a certain delay t_{d} of the gate signals of inverter B compared to inverter A (e.g., as a consequence of differences in PCB layout and/or component propagation delays) will result in a non-zero $v_{\mathrm{CM,tot}}$ as depicted in **Fig. 5.3(c)**: $v_{\mathrm{CM,tot}}$ contains a voltage spike of duration t_{d} and amplitude $\pm V_{\mathrm{DC}}/12$ at every misaligned switching transition of inverter A and inverter B, which leads to a total CM RMS voltage of

$$V_{\mathrm{CM,rms,tot}}(t_{\mathrm{d}}) = \sqrt{\frac{t_{\mathrm{d}} \cdot f_{\mathrm{sw}} \cdot V_{\mathrm{DC}}^2}{24}}. \tag{5.4}$$

Alternatively, non-ideal CM cancellation occurs when the DC-Link needs to be balanced by unequal distribution of the output power between inverter A and inverter B. Thereby, e.g., the output current of inverter A is slightly increased and the output current of inverter B slightly decreased, which, as a first approximation, requires a marginal increase/decrease of the respective output voltage references by the correction factor m_f. With the adjusted modulation indices of $M_\mathrm{A} = M \cdot (1 + m_\mathrm{f}/2)$ and $M_\mathrm{B} = M \cdot (1 - m_\mathrm{f}/2)$ for inverter A and B respectively, a total CM RMS voltage of

$$V_{\mathrm{CM,rms,tot}}(m_\mathrm{f}) = \sqrt{\frac{M \cdot |m_\mathrm{f}| \cdot V_\mathrm{DC}^2}{48 \cdot \pi}} \tag{5.5}$$

results. Note that the modulation index M in case of the 2L-SSC is defined as $M = V_\mathrm{out}/((V_\mathrm{DC}/2)/2)$ with V_out as the phase output voltage amplitude referenced to the virtual midpoint of the DC-Link input voltage of inverter A (resp. B). However, despite these two non-ideal CM cancellation scenarios, the resulting CM voltage of the 2L-SSC is considerably lower than for the 3L-FCC. This is clearly visible in **Fig. 5.4(a)** for a large delay of $t_\mathrm{d} = 100\,\mathrm{ns}$ or a large balancing factor of $m_\mathrm{f} = 0.1$. **Fig. 5.4(b)** highlights how a the total CM RMS voltage of the 2L-SSC further reduces with shorter delays t_d or lower balancing correction factor m_f, i.e., approaching ideal cancellation.

5.3 Design Considering Short-Term Overload Capability

In order to compare the two topologies in terms of achievable power densities and efficiencies, both, the 3L-FCC and the 2L-SSC are designed for the same specifications given in **Table 1.1** and **Table 5.1**, i.e., identical DC-Link voltage, total output power, short-term overload capability and accepted peak CM voltage $v_\mathrm{x,max}$ at the motor terminals. Note that the short-term overload requirement (i.e., three times nominal current during 3 s) is targeted for a broad range of inverter output frequencies f_out, i.e., from motor standstill ($f_\mathrm{out} = 0\,\mathrm{Hz}$) to ($f_\mathrm{out} = f_\mathrm{out,max} = 300\,\mathrm{Hz}$). The important design aspects of semiconductors, capacitors, and CM choke are summarized in the following and the key stress metrics for the main components are compiled in **Table 5.2**.

5.3.1 Semiconductors

The required blocking capabilities $V_{\mathrm{b,nom}} = 400\,\mathrm{V}$ of the semiconductors in the 3L-FCC and 2L-SSC are identical and equal half the total DC-Link voltage. Furthermore, given the same output power, both topologies result in the same RMS current stress for the semiconductors.
Assuming identical device switching frequencies, f_{sw}, the 3L-FCC's switch-node voltage shows an effective switching frequency of $f_{\mathrm{eff}} = 2 \cdot f_{\mathrm{sw}}$, i.e., twice that of the 2L-SSC's switch-node voltages (cf. **Fig. 5.5**). Consequently, the device switching frequency of the 3L-FCC could be reduced to half the value of the 2L-SSC for the same effective switching frequency at the switch node. This, however, increases the required HF DC-Link capacitor volume, the FC volume, and the CM choke volume; all discussed in more detail later. Hence, identical device switching frequencies are maintained for both topologies in this chapter, and the increased effective switching frequency f_{eff} of the 3L-FCC is used to minimize the FC and the CM choke volumes.
With identical device switching frequencies, equal semiconductor losses (conduction plus switching losses) occur in both converters, especially as for typical DM motor phase inductances in the order of several hundred µH to several mH, the difference in motor current ripple is negligible for the considered switching frequency. This leads to an identical choice of semiconductors for the two topologies, i.e., the same semiconductor count and total chip area.

In order to account for voltage overshoots during switching transitions, as well as for Flying Capacitor and/or DC-Link voltage ripple, 650 V power transistors are used. The impact of the overload capability on the selection of semiconductors available on the market has been discussed in detail in [83]. The large currents during overload operation lead to dominating conduction losses, and thus, only semiconductors with low R_{dson} values (i.e., large die areas) and good cooling performance (low R_{th} and large cooling pad) are feasible. This leads to an implementation of a single switch with two parallel top-cooled 650 V GaN HEMTs (GS66516-T, 25 mΩ, [62]) for both, the 3L-FCC and the 2L-SSC. Detailed switching loss data of these devices are also provided in [83].

5.3.2 Flying Capacitors

The 3L-FCC has one FC per phase with a bias voltage of half the DC-Link voltage, while there are no FCs in the 2L-SSC. As discussed in Section 5.2.1, the charging and discharging of the FCs with the respective bridge-leg output

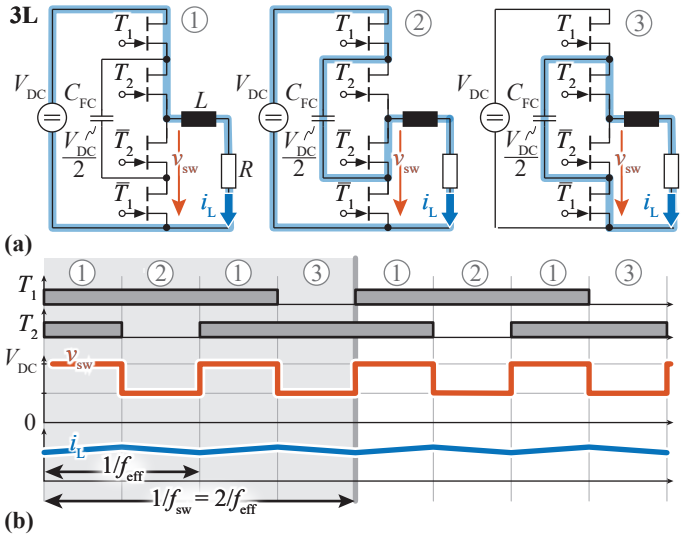


Fig. 5.5: **(a)** Exemplary conduction states for a 3L-FCC phase leg with an output voltage $v_{sw} \in [V_{DC}/2, V_{DC}]$. **(b)** Respective gate signals (i.e., T_1 and T_2) and resulting characteristic output voltage waveform v_{sw} and inductor current i_L. The effective switching frequency f_{eff} seen at the output is double the device switching frequency f_{sw}.

phase current leads to a minimum required capacitance of

$$C_{\mathrm{FC}} = \frac{i_{\mathrm{out}}}{f_{\mathrm{eff}} \cdot \Delta V_{\mathrm{FC,max}}} \tag{5.6}$$

for the worst-caste duty cycle of $d = 0.5$ [50] and a specified peak-to-peak FC voltage ripple $\Delta V_{\mathrm{FC,max}}$ in **Table 5.1**. Thereby, the short-term overload capability of three times the nominal current determines C_{FC} since then $i_{\mathrm{out}} = I_{\mathrm{out,OL}}$ [83][2].
Besides the voltage ripple criterion, a minimum number of paralleled capacitors is required in order to not exceed the maximum rated temperature of the chosen capacitors due to the ESR losses. Especially during overload operation, the worst-case RMS current (for $d = 0.5$) of $I_{\mathrm{FC,rms}} = i_{\mathrm{out}} = I_{\mathrm{out,OL}}$ needs to be accounted for.
Finally, for implementation, 450 V X6S ceramic capacitors are chosen (C5750X6S2W225K250KA, 2.2 µF, [116]) because of their high capacitance density per volume (including the capacitance derating with applied bias voltage). It results in a minimum of 24 paralleled ceramic capacitors for the FC stage per phase.

5.3.3 High Frequency (HF) DC-Link Capacitors

The DC-Link capacitors are designed to restrict the HF DC-Link voltage ripple $\Delta V_{\mathrm{DC,max}}$ to a maximum peak-to-peak value as specified in **Table 5.1**.

- **3L-FCC:** Only the switching states of the two complementary semiconductors next to the DC-Link capacitor (cf. T_1 and $\overline{T_1}$ in **Fig. 5.5(a)**) define the HF component of the DC-Link current regardless of the switching state of the other semiconductors (cf. T_2 and $\overline{T_2}$ **Fig. 5.5(a)**). Consequently, the HF DC-Link voltage ripple (contrary to the FC voltage ripple) is directly related to the device switching frequency f_{sw} (and not the effective switching frequency f_{eff} at the switch nodes). Hence, as seen from the DC-Link, the inverter behaves like a standard three-phase 2L inverter. For the design, in a first-step approximation only a single phase leg is considered. It can then be assumed that the full HF current is covered by the HF DC-Link capacitors, which leads

[2] Note, that the Flying Capacitor volume, as well as the HF DC-Link volume (for both, the 3L-FCC and the 2L-SSC), could be reduced by increasing the switching frequency during overload as done in [83]. However,it leads to an increased implementation effort and is not further considered here.

to a required capacitance value of

$$C = \frac{1}{4} \cdot \frac{i_{\text{out}}}{f_{\text{sw}} \cdot \Delta v_{\text{pp}}} \tag{5.7}$$

for a duty cycle of $d = 0.5$ with a desired peak-to-peak voltage ripple of $\Delta v_{\text{pp}} = \Delta V_{\text{DC,max}}$ [117]. Similar to the FCs, overload operation with $i_{\text{out}} = I_{\text{out,OL}}$ determines the required capacitance.

Two series connected rows of in total 176 X6S ceramic capacitors (C5750X6S2W225K250KA, 2.2 µF, [116]), each rated for 450 V, can be used for the implementation (i.e., every row with a value of $C'_{\text{DC}} = 2 \cdot C_{\text{DC}}$ to account for the series connection). Furthermore, to comply with the thermal limitation of the capacitors, the total RMS current of $I_{\text{DC,rms}} = I_{\text{out,OL}}/\sqrt{2}$ based on a 2L motor drive derived in [118], must be taken into account. According to **Fig. 5.1(a)**, the DC-midpoint (marked with "o") can be used as ground reference but remains completely unloaded.

- **2L-SSC:** The 2L-SSC consists of two stacked three-phase 2L-inverters, each with their own HF DC-Link capacitor C'_{DC} at half the DC-Link voltage. Due to the inverted switching patterns and phase currents, the currents drawn from their respective HF DC-Link capacitors C'_{DC} are identical for both inverters A and B. Thus the HF voltage ripple limitation can be applied to inverter A and inverter B independently. Using the same single-phase approximation introduced above for the 3L-FCC, the required capacitance per stacked inverter can be approximated with (5.7) and $\Delta v_{\text{pp}} = \Delta V_{\text{DC,max}}/2$ (since the respective voltage ripples will be summed up directly due to the identical DC-Link currents of inverter A and inverter B). All in all, the series connection of the two C'_{DC} results in an identical total DC-Link capacitance value C_{DC} as for the 3L-FCC. Hence, it can be built in the same way and for identical RMS current loading.

[3]During standstill overload, no back-EMF occurs, and hence a low phase output voltage with approximately 0.5 duty cycle is required. In the worst-case scenario, one phase carries the full overload current for 3 s, i.e., $I_{\text{out,OL}} = 45$ A. Thereby, the current flows 50% of the time in the high-side semiconductors and 50% in the low-side semiconductors, leading to a factor of $1/\sqrt{2}$ in the RMS current.

Tab. 5.2: Worst-case design parameters considering short-term standstill overload operation (i.e., $f_{out} = 0\,Hz$) with three times nominal output current for 3 s.

	3L-FCC	**2L-SSC**
Inverter Output		
ΔV_{step}	$V_{DC}/2$	
f_{eff}	$2 \cdot f_{sw}$	f_{sw}
Semiconductors		
$V_{b,nom}$	$V_{DC}/2$	
$I_{rms,max}$	$I_{out,OL}/\sqrt{2}$ (3)	
DC-Link Cap.		
V_{bias}	V_{DC}	
$\Delta V_{DC,max}$	$I_{out,OL}/(4 \cdot C_{DC} \cdot f_{sw})$ [117]	
$I_{rms,max}$	$I_{out,OL}/\sqrt{2}$ [118]	
Flying Cap.		
V_{bias}	$V_{DC}/2$	-
$\Delta V_{FC,max}$	$I_{out,OL}/(C_{FC} \cdot f_{eff})$ [50]	-
$I_{rms,max}$	$I_{out,OL}$ [50]	-

5.3.4 Exemplary CM Choke Designs

The goal of the proposed CM choke designs is to reduce the CM voltages at the motor to a maximum value of $v_{x,max}$ specified in **Table 5.1** such that destructive EDM of the motor bearings is mitigated. In the case at hand, a configurable multi-winding PMSM (designed for an 800 V DC-Link with similar rated power as in **Table 1.1** and six configurable three-phase winding sets; shown briefly in [119]) is considered for the 3L-FCC and 2L-SSC design, as it can be configured with either a single or with two winding systems.

Derivation of the CM Model

In **Fig. 5.6(a.i)** the equivalent CM circuit of the motor (i.e., represented by a single CM capacitance C_{CM}) is shown, together with the CM choke (impedance $\underline{Z}_{CMC}$) to be designed. The CM circuit of the motor is derived from the impedance measured of the configurable multi-winding PMSM presented in **Fig. 5.6(a.ii)**, where the machine behaves purely capacitive up to several multiples of the specified 35 kHz device switching frequency, and, consequently, can be modeled for this range with $C_{CM} = 4.4\,nF$. As shown in the circuit derivation of **Fig. 5.2(a)** and **(d)**, the resulting CM model of **Fig. 5.6(a.i)** is valid

for both, the 3L-FCC and the 2L-SSC, given that the same symmetric motor is used with altered winding connections. In the **Appendix B**, this is underlined by additional impedance measurements performed on the configurable multi-winding-set PMSM for single and dual winding-set configuration.

The impedance of a practical CM choke $\underline{Z}_{\mathrm{CMC}}$ can be typically represented by the model depicted in **Fig. 5.7(b)** [120]. When neglecting the parasitic capacitance C_{p} of the windings, as well as the relatively small winding resistance $R_{\mathrm{w}}(f)$, the choke impedance can be calculated as

$$\underline{Z}_{\mathrm{CMC,calc}}(f) = i \cdot 2\pi f \cdot L_{\mathrm{CMC}}(f) + R_{\mathrm{CMC}}(f), \tag{5.8}$$

including a frequency-dependent inductance,

$$L_{\mathrm{CMC}}(f) = A_{\mathrm{L}} \cdot N_{\mathrm{L}}^2 \cdot \frac{\mu^{'}(f)}{|\underline{\mu}(f = 0\,\mathrm{Hz})|}, \tag{5.9}$$

and a frequency-dependent resistor modeling the core losses,

$$R_{\mathrm{CMC}}(f) = A_{\mathrm{L}} \cdot N_{\mathrm{L}}^2 \cdot 2\pi f \cdot \frac{\mu^{''}(f)}{|\underline{\mu}(f = 0\,\mathrm{Hz})|}, \tag{5.10}$$

where N_{L} is the number of turns, A_{L} the initial inductance per turn squared (i.e., for f close to 0 Hz) and $\underline{\mu}(f) = \mu^{'}(f) + \mu^{''}(f) \cdot i$ the complex (relative) permeability of the core material provided in datasheets (with i as the imaginary unit).

Worst-Case CM Voltage Design Criteria

For both topologies, the generated CM voltage pattern $v_{\mathrm{CM,tot}}$ varies over an output period. However, the charging/discharging (which needs to be limited to prevent EDM) of the motor's CM capacitance, C_{CM}, takes place within a switching period/effective switching period. This means that the *local* worst-case CM voltage pattern is relevant for the CM choke design.

- **3L-FCC:** In conventional PSPWM, the worst-case $v_{\mathrm{CM,tot}}$ occurs for sinusoidal modulation (i.e., with a modulation limit of $M = 1$, without third harmonic CM voltage injection) when one of the phases passes through the peak output voltage with, e.g., phase leg duty cycles of $d_{\mathrm{a}} = 1$, $d_{\mathrm{b}} = d_{\mathrm{c}} = 0.25$. The resulting CM voltage is shown in **Fig. 5.6(b.i)**, together with its dominating first harmonic component at f_{eff} with a maximum amplitude of $V_{\mathrm{CM,(1)}} = (\pi/4) \cdot V_{\mathrm{DC}}/6 = (\pi/4) = 170\,\mathrm{V}$. In

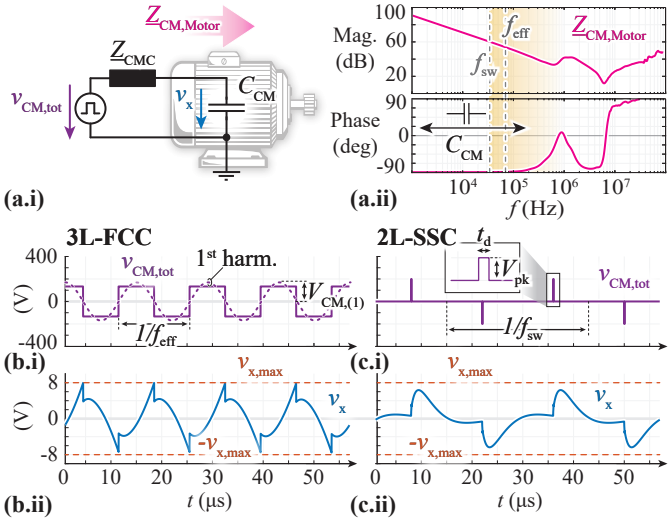
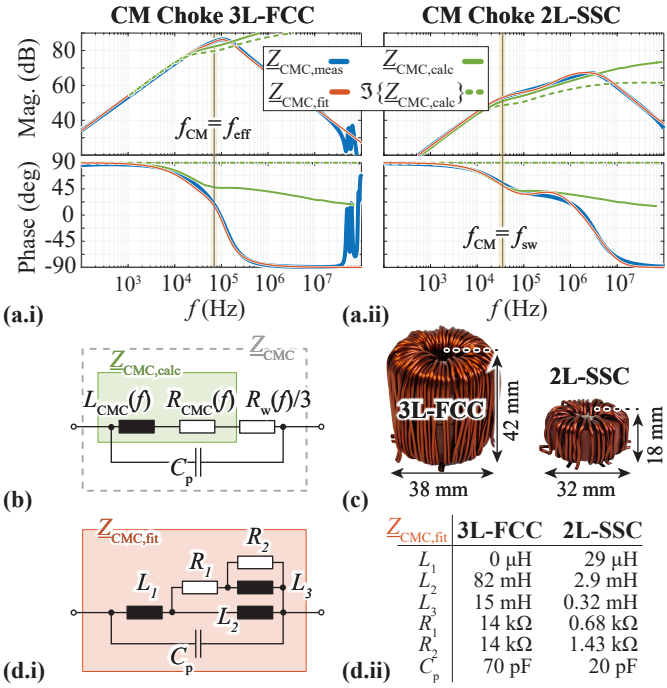


Fig. 5.6: (a.i) Equivalent CM circuit of a PMSM with a purely capacitive motor CM impedance C_{CM} around a switching frequency of $f_{\mathrm{sw}} = 35\,\mathrm{kHz}$ (relevant for the 2L-SSC) and $f_{\mathrm{eff}} = 2 \cdot 35\,\mathrm{kHz}$ (relevant for 3L-FCC). This model is based on the impedance measurement in **(a.ii)** of the configurable multi-winding PMSM presented briefly in [119]. As shown in **Fig. 5.2(a),(b)** this model is valid for both, the single winding-set machine configuration used for the 3L-FCC, as well as the dual winding-set machine configuration used for the 2L-SSC. **(b.i)** Worst-case CM voltage $v_{\mathrm{CM,tot}}$ for the 3L-FCC, which occurs with sinusoidal modulation for a modulation index of $M = 1$ when one phase voltage goes through the maximum (i.e., phase-leg duty cycles of, e.g., $d_{\mathrm{a}} = 1$, $d_{\mathrm{b}} = d_{\mathrm{c}} = 0.25$). The first harmonic is indicated with a peak amplitude of $V_{\mathrm{CM,(1)}}$ (dashed purple line) as it is relevant for the CM choke design. **(b.ii)** Simulated voltage v_{x} at the motor C_{CM} when the measured impedance of the 3L-FCC choke design of **Fig. 5.7(c)** is used. The maximum values are below the specified limits (dashed red line). **(c.i)** Worst-case CM voltage $v_{\mathrm{CM,tot}}$ for the 2L-SSC, which occurs for a modulation index of $M = 0$ (i.e., at motor standstill), when all bridge-legs switch simultaneously with a duty cycle of $d = 0.5$. **(c.ii)** Simulated voltage v_{x} at C_{CM} when the (measured) impedance of the CM choke realized for the 2L-SSC, shown in **Fig. 5.7(c)**, is used.



$\underline{Z}_{CMC,fit}$	3L-FCC	2L-SSC
L_1	0 µH	29 µH
L_2	82 mH	2.9 mH
L_3	15 mH	0.32 mH
R_1	14 kΩ	0.68 kΩ
R_2	14 kΩ	1.43 kΩ
C_p	70 pF	20 pF

Fig. 5.7: Comparison of measured $\underline{Z}_{CMC,meas}$, calculated $\underline{Z}_{CMC,calc}$ and fitted $\underline{Z}_{CMC,fit}$ impedances of the two CM choke designs for the **(a.i)** 3L-FCC and **(a.ii)** 2L-SSC shown in **(c)**. **(b)** Equivalent model of a CM choke $\underline{Z}_{CMC}$, where the green highlighted part $\underline{Z}_{CMC,calc}$ can be calculated with frequency-dependent parameters and is used during the design process; note that the contribution of the inductive component can be directly seen in **(a)** in the imaginary part $\Im(\underline{Z}_{CMC,calc})$. **(d.i)** Equivalent model $\underline{Z}_{CMC,fit}$ fitted to the measurement of **(a)** with parameters given in **(d.ii)**. This model is used for circuit simulations.

order to comply with the given design specifications, the excitation of the first harmonic has to be attenuated to a maximum peak amplitude of $v_{\mathrm{x,max}}$ over C_{CM} (red dashed line in **Fig. 5.6(b.ii)**). All higher-order harmonics are not explicitly addressed with this approach, as they are, first, of lower amplitude in the first place, and, second, attenuated ideally substantially stronger than the first harmonic (characteristic of a low-pass filter formed by the motor CM capacitance C_{CM} and the CM choke impedance $\underline{Z}_{\mathrm{CMC}}$). Consequently, a CM choke design with an impedance $\underline{Z}_{\mathrm{CMC}}$ satisfying

$$\left|\frac{v_{\mathrm{x,max}}}{V_{\mathrm{CM},(1)}}\right| = \frac{1}{|i \cdot 2\pi f_{\mathrm{eff}} \cdot C_{\mathrm{CM}} \cdot \underline{Z}_{\mathrm{CMC}} + 1|} \tag{5.11}$$

is required for the 3L-FCC. For the design process $\underline{Z}_{\mathrm{CMC}}$ can be modeled with (5.8) as $\underline{Z}_{\mathrm{CMC,calc}}(f_{\mathrm{eff}})$.

- **2L-SSC:** As discussed in **Section 5.2.2**, a significant reduction of the total CM voltage can be achieved thanks to CM cancellation. Thereby, if the two stacked inverters do not switch simultaneously (cf. **Fig. 5.3(c)**), only small CM voltage spikes remain, which is, e.g., the case for a delay t_{d} between the switching transitions of inverter A and B as a result of propagation delay mismatches and/or active DC-Link balancing actions with correction factor m_{f}. As every single one of these voltage spikes charges the motor CM capacitance C_{CM}, the CM choke has to be designed to limit the increase in voltage during those CM spikes. Thereby, the largest voltage-time-area (i.e., the longest spike duration with the highest spike amplitude) defines the worst-case, and thus, the required choke impedance $\underline{Z}_{\mathrm{CMC}}$.

  In the case at hand, a delay of the corresponding switching actions in the 2L-SSC between inverter A and inverter B of $t_{\mathrm{d}} = 100\,\mathrm{ns}$ is assumed. This is a very conservative upper limit, given that typical propagation delay (mismatches) are in the order of a few ten nanoseconds if high-quality ICs and PCB layouts are used. However, choosing this excessively large t_{d} also accounts for CM voltage spikes caused by potential active DC-Link balancing (i.e., m_{f} in **Section 5.2.2**).

  Then, in general, six voltage spikes of duration $t_{\mathrm{d}} = 100\,\mathrm{ns}$ and of amplitude $\pm V_{\mathrm{DC}}/12 = \pm 66.7\,\mathrm{V}$ result per switching period. The largest instantaneous voltage-time-area (i.e., the worst-case scenario) occurs for $M = 0$ (i.e., all bridge-legs operate with a duty cycle $d = 0.5$). In this

operating point, the six voltage spikes are temporally aligned/superimposed such that only two CM voltage spikes per switching period with amplitudes $V_{\mathrm{pk}} = \pm 3 \cdot V_{\mathrm{DC}}/12 = \pm 200\,\mathrm{V}$ remain as depicted in **Fig. 5.6(c.i)**[4].

In contrast to the 3L-FCC above, the first harmonic component does not sufficiently characterize the CM voltage spikes. Therefore, the following approach is suggested: Only the inductive part of the choke, i.e., $L_{\mathrm{CMC}}(f)$, is considered, which is still a significant part of the impedance at $f = f_{\mathrm{sw}}$, reducing the CM model of **Fig. 5.6(a.i)** to a simple LC (resonant) circuit. During the voltage spike of duration t_{d}, essentially the full spike voltage is applied over the choke (given that v_{x} is small by design), giving rise to a current increase and hence an accumulation of stored energy in the CM choke. After the CM voltage spike, this energy is transferred to C_{CM}, leading to a peak voltage amplitude of v_{x}. The subsequently expected characteristic oscillation of an LC resonant circuit is strongly damped in reality thanks to the (so far) neglected $R_{\mathrm{CMC}}(f)$, i.e. the peak voltage is expected to be slightly lower and the oscillation is finished before the next voltage spike occurs. Consequently, with this approach, the design criterion of $\underline{Z}_{\mathrm{CMC}}$ (i.e., L_{CMC}) is deduced via the energy balance as

$$L_{\mathrm{CMC}} = \frac{1}{C_{\mathrm{CM}}} \cdot \left(\frac{V_{\mathrm{pk}} \cdot t_{\mathrm{d}}}{v_{\mathrm{x}}} \right)^2 . \tag{5.12}$$

CM Choke Realization

Nanocrystalline materials such as VITROPERM 500 [121] offer high relative permeability (up to 100 000), high saturation flux density (up to 1.2 T) and highly resistive core-loss characteristics for frequencies above several tens of kilohertz, which facilitates well-damped filter designs. Hence, they are an ideal candidate for the realization of the CM chokes.

In order to meet the requirements for short-term overload capacity, the high phase currents (i.e., 45 A) must be taken into account when dimensioning the CM choke:

[4]Note, that $M = 0$ coincides mostly with motor standstill operation (i.e, no back-EMF hence low/no inverter output voltage amplitude), where the bearings show a resistive instead of capacitive behavior [111]. However, it is a valid worst-case scenario, which accounts for all possible operating points.

- Possible core saturation caused by the leakage flux (corresponding to a leakage inductance of several µH, depending on the inductor design) can be considered already in the design phase [120].

- The core and winding temperatures should be maintained below 155 °C [121] (coinciding with NEMA motor insulation temperature rating Class F [19]). With the majority of the losses originating from the winding, i.e., copper losses, the choke can, e.g., be pressed to the motor housing/inverter baseplate using a TIM to achieve sufficient conductive heat transfer. Therefore, a straightforward thermal model consists of a parallel connection of a thermal capacitance (copper winding) and a thermal resistance (cooling path through the copper windings to the side of choke contacting the TIM and then the path through the TIM itself onto the motor housing/inverter baseplate). Starting from the nominal operating point (defined by the thermal resistance only) the choke should not overheat within the 3 s overload operation, despite the strongly increased winding losses during this period.

Together with the design criteria discussed above, commercially available VITROPERM 500 cores and different solid wire diameters were considered (DC winding losses are strongly dominating due to the small output current ripple), and the best-performing design for a semiconductor device switching frequency of 35 kHz in terms of overall efficiency/power density is selected. Thereby, the three-phase (3L-FCC) and six-phase (2L-SSC) CM chokes shown in **Fig. 5.7(c)** result with construction details provided in **Table 5.3**. Their measured impedances are shown in **Fig. 5.7(a)**, together with the calculated impedance $\underline{Z}_{\mathrm{CMC,calc}}$ of (5.8), which was used for the 3L-FCC design (cf. **Fig. 5.7(b)**), and the imaginary part of $\underline{Z}_{\mathrm{CMC,calc}}$ (i.e., $2\pi f \cdot L_{\mathrm{CMC}}$), which was used for the 2L-SSC design. In order to simulate the resulting voltage v_{x} over the motor CM capacitance C_{CM} by means of circuit simulation software (PLECS [122]), the measured CM impedances of the choke designs are represented by the fitted *LCR*-network of **Fig. 5.7(d)**.

In **Fig. 5.6(b.ii),(c.ii)** the resulting v_{x} are plotted for the respective worst-case $v_{\mathrm{CM,tot}}$ excitations of **Fig. 5.6(b.i),(c.i)**. As can be seen, for both choke designs the voltage v_{x} over the motor CM capacitance C_{CM} remains below the limits (dashed red lines), validating the chosen approaches. Nevertheless, the choke design of the 3L-FCC is more critical due to the large parasitic winding capacitance C_{p}, which was not included in the design process. It has a visible influence on the resulting v_{x} as higher frequency voltage components bypass

the CM choke, which consequently leads to sharp spikes at the switching transitions.

5.3.5 Resulting IMD Designs

For the specifications given in **Table 1.1** and **Table 5.1** and the presented CM chokes, the final volume breakdown and required PCB area are shown in **Fig. 5.8(a)** and **Fig. 5.8(b)**, respectively. Thereby, the dimensions are based on a realized 3L-FCC/7L-FCC hardware presented in [83] (considered PCB areas are recapitulated in **Table 5.3**[5]). As expected, the semiconductor and gate drive area/volume is identical for both topologies, and the main difference in the overall area/volume originates from the larger CM choke of the 3L-FCC compared to the 2L-SSC (cf. **Fig. 5.7(c)**), and the FCs, which are only required in the 3L-FCC.

The loss breakdowns at the nominal operating point shown in **Fig. 5.8(d)** show identical semiconductor losses for both topologies and, due to the large required die area for overload capability, are dominated by switching losses [83]. However, the total losses of the 2L-SSC are expected to be lower compared to the 3L-FCC, thanks to the small required CM impedance which results in a CM choke design with a slim core and few winding turns. As can be observed in **Fig. 5.8(c.i),(c.ii)**, this results in an expected efficiency of 99.05 % for the 3L-FCC and a slightly higher efficiency of 99.2 % for the 2L-SSC during nominal operation (cf. red circles). For lower output current amplitudes $i_{\text{out,peak}}$, the efficiencies of the 3L-FCC and 2L-SSC converge, since the winding conduction losses of the choke, which causes the main loss difference, are reduced. On the other hand, during overload, the (short-term) total losses of the 3L-FCC strongly exceed those of the 2L-SSC, due to higher winding losses in its CM choke.

5.4 Comparative Evaluation

With the expected volumes and efficiencies of both topologies presented in the previous section, an overall comparison of the two possible IMD implementations becomes feasible. Accordingly, the radar plot from **Fig. 5.9** provides a visual summary of the main performance characteristics of the

[5]Note that also heatsink volumes for the semiconductors and the chokes are accounted for as discussed in [83]. Thereby, the thickness of the baseplate, where the semiconductor PCBs are mounted, is varied to achieve a maximum temperature of 100 °C below the semiconductors, i.e., an increase of 10 °C compared to the motor housing.

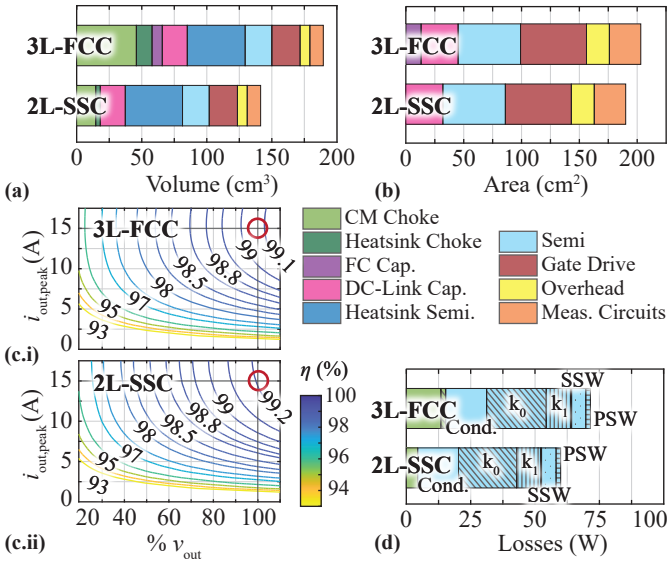


Fig. 5.8: (a) Volume breakdown and **(b)** PCB area breakdown expected from the two IMD designs. **(c.i)**, **(c.ii)** Calculated efficiencies for nominal and partial load operation at a **bp!** temperature of 100 °C for the 3L-FCC and the 2L-SSC, respectively. The red circle highlights the nominal operating point (i.e., $i_{\text{out,peak}} = 15\,\text{A}$ and a phase voltage of $v_{\text{out}} = 330\,\text{V} = 100\,\%$ at $f_{\text{out}} = 300\,\text{Hz}$), where the design target of a minimum efficiency of 99 % is defined. The output frequency is linearly reduced with v_{out} (i.e., starting from 300 Hz at 100 % v_{out}), which in a first step corresponds to a practically relevant scenario, where a constant torque at reduced rotational speed is provided. **(d)** Calculated loss breakdown for the nominal operating point (red circles in **(c)**) for the 3L-FCC and 2L-SSC. The semiconductor losses are colored in light blue with the pattern indicating the distinction between conduction losses ("Cond."), the HSW ("k_0", "k_1") according to $P_{\text{sw}} = k_0 + k_1 \cdot i_{\text{sw}} + k_2 \cdot i_{\text{sw}}^2$ [83], the Partial-Hard Switching ("PHSW") losses, and the Soft Switching ("SSW") losses.

Tab. 5.3: Main power components used in the 3L-FCC and 2L-SSC designs.

3L-FCC	2L-SSC
Power Transistors	
GaN Systems GS66516T (650 V, 25 mΩ), 2 x parallel per position; 27.2 mm^2 device chip area [123]	
Gate Driver and Gate Drive Insulator	
Infineon 1EDN7511B Analog Devices ADuM121N	
CM Choke $\underline{Z}_{CMC}$	
VITROPERM 500F L2030-W514, 2x stacked; 3x 19 turns of solid copper wire (A_{cu} = 1.3 mm^2); L_{CMC}(70 kHz) = 13 mH, R_{CMC}(70 kHz) = 17.3 kΩ	VITROPERM 500F L2025-W380, 1x stacked; 6x 6 turns of solid copper wire (A_{cu} = 1.2 mm^2); L_{CMC}(35 kHz) = 1.6 mH, R_{CMC}(70 kHz) = 0.25 kΩ
DC-Link Capacitors C_{DC}	
Min. 20 µF, 176 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V), i.e., two rows of 88 caps in series	
Flying Capacitors C_{FC}	
11 µF, 24 x C5750X6S2W225K250KA (X6S, 2.2 µF, 450 V) per phase	
Required PCB Areas according to [83]	
Paralleled semiconductors per half-bridge: 9.0 cm^2 Gate drive circuit per half-bridge: 9.5 cm^2 Overhead per half-bridge: 3.3 cm^2 Single voltage/current measurement circuit: 4.5 cm^2	

3L-FCC and 2L-SSC equipped with CM chokes for mitigating EDM bearing currents, which serves as a basis for the following comparison and discussion.

Mechanical Realization Effort

As mentioned in **Section 5.3**, the realization effort of the 3L-FCC and the 2L-SSC is identical in terms of required switches (and gate drives), as well as regarding the total semiconductor chip area defined by the overload capability. Similarly, the total required (HF) DC-Link capacitance, its voltage rating, and RMS current capability are the same for the 3L-FCC and 2L-SSC, with the only difference of a mandatory (internal) DC-Link midpoint in the case of the 2L-SSC.
Note, that despite the identical total semiconductor chip area of the two topologies, the 2L-SSC benefits from a possible standard six-pack semiconductor arrangement, whereas the 3L-FCC requires a more dedicated bridge-leg design, which is a clear advantage of the 2L-SSC that is not captured in the **Fig. 5.9**.

A clearly visible key benefit of the 2L-SSC is the elimination of the FCs, which leads to a reduction of the required PCB area (cf. **Fig. 5.8 (b)**) and of the number of discrete components placed in the system. Furthermore, thanks to the possibility of CM cancellation and the subsequently improved CM output voltage quality, the CM choke of the 2L-SSC is considerably smaller in volume, even in the case of non-ideal cancellation with the assumed worst-case misalignment of $t_d = 100$ ns between inverter A and B. Note that the CM choke volume of the 2L-SSC can be minimized even further when a low t_d can be guaranteed as indicated with green arrows in **Fig. 5.9**.

All in all, the elimination of the FC and the considerably smaller CM choke volume lead to a smaller possible system realization (i.e., smaller boxed volume) of the 2L-SSC compared to the 3L-FCC.

Losses and Overload Capability

The switching and conduction losses in the semiconductors of the 3L-FCC and 2L-SSC are the same based on the chosen identical device switching frequencies (i.e., the increased effective switching frequency of the 3L-FCC is used to minimize its FC and CM choke volume) combined with the negligible phase current ripple in the relatively large motor phase inductances. However, thanks to the required lower CM choke impedance of the 2L-SSC, the CM choke design results in a smaller total winding length (i.e., all six windings together) and the associated winding copper losses are reduced compared

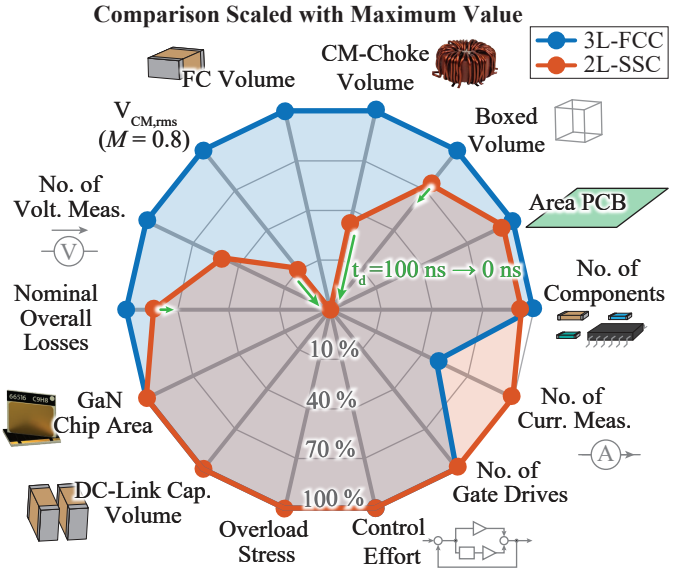


Fig. 5.9: Radar plot of key characteristics of the 3L-FCC (blue) and the 2L-SSC (red) designed for the same IMD specifications given in **Table 1.1** and **Table 5.1**. The 100% values correspond to the maximum value of each category. For a complete IMD implementation, these maximum values are given in the following: CM Choke Volume = 0.046 dm^3, Boxed Volume = 0.19 dm^3, PCB Area = 2.03 dm^2, No. of Components = 1068, No. of Current Measurements = 4, No. of Gate Drives = 12, Control Effort = 5 (quantified as number of energy storage elements to be controlled), Overload Stress = 95% of $T_{j,max}$ (quantified as utilization of the maximum allowed semiconductor junction temperature (i.e., $T_{j,max}$ = 150 °C) when the peak current is provided during standstill overload), DC-Link Capacitor Volume = 0.02 dm^3, GaN Chip Area = 653 mm^2, Nominal Overall Losses = 71.4 W, No. of Voltage Measurements = 4, $V_{CM,rms}$ = 86.9 V (total RMS CM voltage over an output frequency period with $M = 0.8$) and FC Volume = 0.0078 dm^3. The influence on the 2L-SSC design for a reduction of the assumed worst-case misalignment of the switching transitions of inverter A and B from t_d = 100 ns to t_d = 0 ns is indicated with green arrows.

to the 3L-FCC despite the slightly smaller solid wire cross-section of the optimal design. This can be seen in the overall loss breakdown presented in **Fig. 5.8(d)**.

During overload operation, an equal stress increase is expected for the key components of both topologies. This characteristic is quantified in [123] (with temperature-critical semiconductors in the forefront) and shows the utilization of the maximum allowed semiconductor junction temperature after a 3 s standstill overload operation with 45 A peak current in one phase. The junction temperature evaluation considers a transient dynamic thermal model with non-ideal heat spreading in the baseplate, on which the PCB with the semiconductors is mounted [83]. Consequently, with identical semiconductor devices and identical overload losses, the same junction temperatures, and hence the same overload stresses, are expected[6].

Measurement Effort

The number of necessary voltage and current measurement circuits represents an adequate quantification of the measurement effort of a three-phase IMD implementation. In the case at hand, both the 3L-FCC and the 2L-SSC require six measurement units in total. Thereby, for the 3L-FCC four voltage measurements, one for the full DC-Link and one for each Flying Capacitor[7] are accounted for. Furthermore, at least two output phase current measurements are needed for the operation of a single three-phase machine winding system (in open-star configuration).
Meanwhile, the 2L-SSC only relies on two voltage measurements (full DC-Link voltage and DC-midpoint) but requires four output current measurements for the dual three-phase winding system.

[6]Note that also for the designed chokes a similar temperature increase (remaining below 155 °C) is expected within the 3 s overload. Thereby, the reduced copper mass of the 2L-SSC choke offers less thermal capacitance to buffer the short-term surge of (mainly) winding losses compared to the design of the 3L-FCC. On the other hand, these winding losses are significantly lower in the 2L-SSC and the overall smaller size of the choke allows a better thermal connection to the motor housing for cooling, which finally leads to a similar thermal behavior in the event of overload.

[7]Note that advanced Flying Capacitor balancing techniques as suggested in [88], which rely on manipulation of the switching pattern based on the current ripple (i.e., omit the direct measurement of the Flying Capacitor voltages) are substantially more complicated, especially when considering, that (1) the ripple might be small when a large motor inductance defines the ripple instead of a dedicated output filter inductance and (2) the three-phase currents are coupled in an open-star configured machine without DC-side referenced output filter capacitors, which has also a direct impact on the ripple.

Control Effort

The measurements are used to actively control the respective energy storage units of the system (i.e., the voltage of capacitors and the currents in the motor phase inductances). Consequently, the number of these energy storage units can be used to describe the control effort featured in **Fig. 5.9**. In the present case, it is identical for both topologies with five energy storage units each:
For the 3L-FCC, the single three-phase winding PMSM in dq-frame (as used in Field-Oriented Control) accounts for two units to be controlled, i.e., d-current and q-current component, while the actively balanced Flying Capacitor voltages of every phase contribute the remaining three units. Contrary to the 2L-SSC, the DC-Link midpoint voltage is not connected and, therefore, only requires passive balancing resistors for potential leakage current variations among series-connected capacitors as used here, see **Fig. 5.1(a)**.
In the 2L-SSC, considering non-idealities, only the DC-Link midpoint voltage needs active balancing. However, the dual-winding PMSM features two sets of dq-currents [124], i.e., four units to be controlled.

Yet, when considering control *complexity*, the 2L-SSC might offer a certain advantage, which is not represented in **Fig. 5.9**: The dq-frame-based current controller (despite potential coupling in the dual three-phase winding set machine [105]) is rather standard, while the balancing of the FCs is a less known concept for industrial drive systems. Furthermore, e.g., during start-up, special initialization procedures are required to charge the FCs equally, which is not necessary for the split DC-Link voltage of the 2L-SSC. Said split DC-Link capacitor of the 2L-SSC could also be more easily equipped with a larger capacitance than strictly required for the HF voltage ripple limitation, which facilitates the voltage balancing in the case of the 2L-SSC further.
Overall, balancing a single DC-Link midpoint voltage and controlling two three-phase current systems seems less complex than balancing three FC voltages and a single three-phase current system, and consequently, the 2L-SSC has a certain advantage over the 3L-FCC regarding the control aspect.

5.4.1 Alternate Scenario: Low Motor Phase Inductance

The presented comparison has been conducted under the assumption that the PMSM has a significant motor phase inductance, i.e., the motor current ripple is small. The radar plot of **Fig. 5.9** clearly indicates that in this case an IMD implementation with the 2L-SSC is superior to the 3L-FCC in various

aspects. It increases the performance by reducing the total inverter losses and achieves an overall smaller volume. The considerably less bulky CM choke volume facilitates motor integration and allows a more compact and flexible design for various motor shapes.

However, the motor phase inductance might be considerably lower for, e.g., high-speed machines with low turn counts of the stator windings [125]. For identical motor current ripples in the case of the 2L-SSC and the 3L-FCC, the device switching frequency f_{sw} of the 2L-SSC must be doubled compared to the 3L-FCC to achieve the same *effective* switching frequency f_{eff} at the switch node. If one also takes into account that the phase inductance of the dual-winding motor is likely to be around half that of a single-winding motor for the same power/torque specifications, the device switching frequency required to achieve a similar output current ripple would actually quadruple for the 2L-SSC, and thus increase the expected inverter losses considerably. For such a system, the higher effective switching frequency offered by the 3L-FCC is a clear advantage.

5.4.2 Alternate Scenario: Full Sine-Wave Output Filter

So far, only a CM filter was targeted to mitigate EDM bearing current damages. However, for the 2L-SSC the presented analysis relies on a symmetric motor design; if symmetry in the mechanical setup is not present, the CM cancellation approach does not completely prevent the buildup of voltages across the bearings despite the CM choke (see **Appendix A** for a brief discussion). Consequently, in order to mitigate EDM bearing currents in such cases, or, more generally, to maximize the inverter's motor-friendliness and, in non-IMD applications, the compatibility with long motor cables, a combined DM and CM output voltage filter as shown in **5.10 (a)** (i.e., a DC-midpoint referred full sine-wave *LC* filter stage highlighted in yellow) has to be employed. This full sine-wave filter eliminates HF motor losses and completely protects the motor from the power electronics (e.g., from high $\mathrm{d}v/\mathrm{d}t$ and CM voltages) [32]. This approach has been thoroughly discussed in [83] for the 3L-FCC and is here briefly extended to the 2L-SSC.

The total volume of such an *LC* filter in an 2L-SSC is inherently doubled compared to the 3L-FCC even when assuming an identical effective switching frequency at the switch node (i.e., the 2L-SSC requires twice the device switching frequency compared to the 3L-FCC): Although this leads to identical voltage-time areas over the respective filter inductors in both topologies, the two winding systems of the 2L-SSC require two separate sets

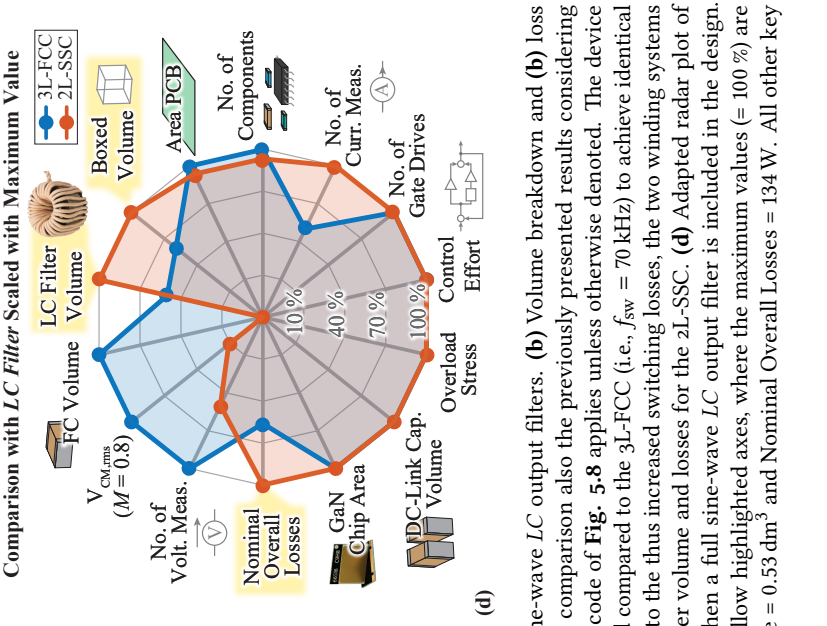


Fig. 5.10: **(a)** Schematics of the 3L-FCC and 2L-SSC with full sine-wave *LC* output filters. **(b)** Volume breakdown and **(b)** loss breakdown of the 3L-FCC and 2L-SSC with *LC* output filter. For comparison also the previously presented results considering only a CM choke (see **Fig. 5.8 (a)**) are shown; the color/pattern code of **Fig. 5.8** applies unless otherwise denoted. The device switching frequency of the 2L-SSC with *LC* output filter is doubled compared to the 3L-FCC (i.e., f_{sw} = 70 kHz) to achieve identical voltage-time area stress of the output filter inductors. In addition to the thus increased switching losses, the two winding systems each require an output filter, which leads to twice the output filter volume and losses for the 2L-SSC. **(d)** Adapted radar plot of key characteristics of the 3L-FCC (blue) and the 2L-SSC (red) when a full sine-wave *LC* output filter is included in the design. The introduction of a *LC* output filter design mainly alters the yellow highlighted axes, where the maximum values (= 100 %) are updated as follows: CM Choke Volume = 0.36 dm^3, Boxed Volume = 0.53 dm^3 and Nominal Overall Losses = 134 W. All other key characteristics remain (nearly) identical.

of filter inductors, each designed for the same nominal/overload current as for the 3L-FCC. Consequently, a doubling of the filter volume and filter losses results, in addition to the doubling of the switching losses due to the doubled device switching frequency), which is shown in the volume comparison in **Fig. 5.10 (b)** and the loss comparison in **Fig. 5.10 (c)**, together with the previously discussed volume/losses of the CM choke design for reference (cf. **Fig. 5.8 (a),(d)**)[8]. The clearly larger volume and the higher losses of the 2L-SSC compared to the 3L-FCC are reflected in the comparative radar plot from **Fig. 5.10 (d)**, where the axes affected by the *LC* filter (compared to the CM choke case in **Fig. 5.9**) are marked in yellow. All in all, the 3L-FCC has a clear advantage over the 2L-SSC if a full sine-wave *LC* output filter is needed, thanks to its increased effective switching frequency, three-level output voltage characteristic, and compatibility with motors with a single winding system.

As a side remark: For passive $\mathrm{d}v/\mathrm{d}t$ filters (e.g., $\mathrm{d}v/\mathrm{d}t$-*LC*-filters [92]), also twice the volume and losses result for the 2L-SSC compared to the 3L-FCC due to the need for a motor with two winding systems. However, if *active* $\mathrm{d}v/\mathrm{d}t$ filters (e.g., gate-driver based $\mathrm{d}v/\mathrm{d}t$ limitation [92]) are employed, which act on each transistor individually, both the 3L-FCC and 2L-SSC have the same volume/losses due to the identical number of transistors for identical device switching frequency f_{sw}.

5.5 Summary

This chapter presents a comprehensive comparison between a 7.5 kW motor-integrated three-phase 3L-FCC and a two 2L-SSC, which are both designed for a high short-term overload capability. Advantageously, the 2L-SSC consists of two standard six-switch three-phase inverters with half the total DC input voltage. Thus, standard techniques and components such as power modules, are applicable, but a non-standard motor with two three-phase winding systems is needed; however, considering motor-integration, this seems of limited importance as no additional external machine terminals are required. In contrast, the 3L-FCC requires more intricate bride-leg structures with FCs (additional components) whose voltages must be actively balanced (increased control complexity), but is compatible with standard motors.

[8] The output filter capacitors of the 2L-SSC as shown **Fig. 5.10 (a.ii)** experience a DC-bias voltage differently from the 3L-FCC in **Fig. 5.10 (a.i)**. However, their contribution to the filter volume and losses is marginal compared to the filter inductor and thus not discussed further.

Both topologies facilitate realizations with same power semiconductor effort (count, chip area); specifically, 650 V GaN HEMTs are applicable despite the 800 V DC-Link voltage. Further, assuming a sufficiently large motor inductance, there is little benefit from doubling the 2L-SSC's switching frequency to match the effective switching frequency of the 3L-FCC, $f_{\mathrm{eff}} = 2 \cdot f_{\mathrm{sw}}$, and thus both systems show identical semiconductor conduction and switching losses.

To mitigate EDM damages to the motor bearings, the maximum CM voltage at the motor must be limited, which can be achieved by employing a CM choke that forms a voltage divider with the CM impedance of the motor itself. The CM voltage generated by the inverter ultimately defines size and losses of the CM choke, whereby the 2L-SSC offers the possibility of (ideally) mutual canceling of the CM voltages generated by the two stacked three-phase two-level inverters. Even under conservative assumptions regarding non-ideal alignment of the two inverters' switching transitions and hence non-ideal CM voltage cancellation, the resulting CM choke features only about 30% of the volume and 30% of the (nominal) losses compared to the CM choke needed for the 3L-FCC (even though the 3L-FCC's CM choke design benefits from the doubling of the device switching frequency, $f_{\mathrm{eff}} = 2 \cdot f_{\mathrm{sw}}$, concerning formation of the output voltage). For such a scenario, the 2L-SSC is clearly the preferable solution. On the other hand, in case full sine-wave filtering of the inverter output voltages is desired to maximize motor-friendliness and/or to cope with long motor cables in non-motor-integrated applications, the 3L-FCC benefits from the inherent doubling of the device switching frequency at the switch node, whereas the 2L-SSC suffers from the need for two sets of filter elements (inductors and capacitors) due to the two separate winding systems. Thus, identical voltage quality at the motor implies, for example, twice the semiconductor switching losses and twice the filter volume and losses for the 2L-SSC compared to the 3L-FCC.

Finally, the 2L-SSC's advantages in terms of realization from standardized building blocks like six-pack modules, and the absence of specialized control considerations like for voltage balancing of FCs, remain interesting and relevant from an industrial perspective.

6 Conclusion and Outlook

In recent years a strong interest in Integrated Motor Drives (IMDs) has emerged, where the power electronics (active/passive rectifier front-end and inverter output stage) is directly integrated into the motor unit, eliminating expensive shielded cables and allowing a space-saving installation of the system. This trend is favored by the fact that a shift towards DC supplied VSDs is developing in the industry at the same time, which reduces the number of components to be integrated into the motor to the inverter stage only.

Key challenges of such an IMD are (1) maintaining the existing motor sizes as far as possible despite inverter integration, (2) limiting the additional cooling effort and/or limiting the self-heating of the power electronics in the already high ambient temperatures of the motor, and, especially for IMDs in servo application, (3) providing a high short-term overload capability.

This thesis addresses the aforementioned criteria through a comprehensive evaluation and comparison of different promising Multi-Level (ML) topologies for motor integration. Their performance is analyzed based on realized hardware, which is designed for the exemplary system outlined in **Table 1.1**, i.e., with the specific objectives of achieving a 99% inverter efficiency at 7.5 kW nominal output power and a three seconds overload capability providing three times the nominal torque/current.

In the following sections the key contributions of this thesis are recapitulated and an outlook on future work is given.

6.1 Results of this Thesis

Returning to the initially stated challenges for motor-integrated drive systems, the key contributions of this thesis can be summarized and discussed as follows:

- **Limited Space for Power Electronics — *High Power Density***
  A small inverter volume can considerably facilitate the integration into the motor housing, and hence, it is an important aspect to consider throughout the design.
  For all three realized hardware demonstrators with full sine-wave *LC* output filter, i.e. the 7L-Flying Capacitor inverter (FCi), the 7L-Hybrid Active Neutral-Point Clamped Converter (7L-HANPC) and the 3L-FCi, the required volume distributions, as well as the expected Printed Circuit Board (PCB) areas, are presented in **Fig. 4.2**, and they closely match the actively used areas of the built phase modules shown in **Fig. 4.3**. Thereby, the overall component volumes in both the 7L Si and the 3L GaN FCi are found to be comparable. While the PCB with semiconductors, gate drivers and Flying Capacitors (FCs) is the predominant part of the 7L Si FCi, the output filter inductors considerably contribute to the volume of the 3L-FCi realization. These pure FCi topologies are outperformed by the 7L-HANPC in terms of achievable power density (i.e., almost 20% higher than the 3L GaN FCi) thanks to its combination of small output filter and reduced number of (higher voltage) FC stages compared to the 7L-FCi.

  Shown in **Fig. 5.10**, a smaller total volume of the 3L-FCi can be achieved when opting for a Common Mode (CM) choke instead of a full sine-wave *LC* output filter (i.e., in the case at hand, to limit the maximum CM voltage at the motor for mitigating Electric Discharge Machining (EDM) bearing currents). Doing so, the volume of the 3L GaN FCi is reduced by 40% for the same device switching frequency. Furthermore, when the machine is reconfigured to a dual three-phase winding machine, a Stacked Polyphase Bridge Inverter (SPBI), or more specifically a Series-Stacked Two-Level three-phase Converter (2L-SSC), can be used with identical semiconductor effort, but without FCs and with a reduced CM choke size thanks to a minimal required CM choke impedance when CM cancellation is employed. Hence, the overall volume of the 2L-SSC diminishes by an additional 25% compared to the 3L GaN FCi with CM choke at identical device switching frequency. However, if for maximum motor-friendliness a full sine-wave *LC* filter is desired in

combination with the 2L-SSC, a substantial increase in volume results, i.e., the 2L-SSC surpasses the volume of the 3L-FCi with *LC* filter by 70%. This is due to the two three-phase systems in the motor, which each require a filter-set, combined with the absent effective switching frequency f_{eff} increase typical for FCi topologies.

All in all, the presented inverter component volumes provide a solid baseline for comparison. However, ultimately, the *effective* increase in total motor size matters when integrating the drive into the motor. This is strongly affected by the form factor of the inverter and the motor itself: In the case at hand, e.g., the 7L Si and the 3L GaN FCi have very similar total component volumes, but the required PCB area for the 3L-FCi is considerably smaller. Consequently, the 3L-FCi can be arranged as shown in **Fig. 4.9** around the encoder without additional mechanical structures. On the other hand, for the 7L Si FCi realization (as well as for the 7L-HANPC), a comparable setup as shown in **Fig. 3.1** with several stacked baseplates for mounting the power stage PCBs is required, which adds to the total volume and is not accurately captured in the presented volume distribution[1].

- **Elevated Motor Temperatures — *High Inverter Efficiency***
  A high nominal inverter efficiency of minimum 99% is targeted for the IMD at hand in order to limit the self-heating of the power electronic components in the already high ambient temperatures in the close proximity of the motor. For the three realized hardware demonstrators the efficiencies are experimentally verified and the measurements align closely with the nominal target mark (i.e., 98.9% for the 7L-FCi, 99.11% for the 7L-HANPC and 98.94% for the 3L-FCi, cf. **Fig. 4.5**). The same calculation base is used for the 3L-FCi and the 2L-SSC with a CM-choke design, where nominal efficiencies of 99.05% and 99.2% are expected, cf. **Fig. 5.8**. With these inverter efficiencies during nominal operation, the semiconductor junction temperatures are only elevated by 2-3°C compared to the baseplate where they are mounted (which is in the present case at 100 °C).

- **Short-Term Overload Capability — *Good Transient Cooling Performance & Limited Overload Losses***
  The high short-term overload capability requirement results in high transient current stresses, and consequently, in a momentary increase in

[1]The semiconductor heatsink volume represents a part of these mechanical structures, see **Section 3.2.2**.

the total inverter (and motor) losses. Thereby, the conduction losses in, e.g., the semiconductors and the windings of the filter inductors/choke, dominate, as they increase with current squared.
This is particularly critical for the semiconductor devices, as they have (1) only a small mass and consequently, only a small thermal capacitance to temporarily absorb the losses, (2) a limited surface area that can be utilized for cooling, and (3) a maximum allowed junction temperature (e.g., 150 °C for the used GaN and 175 °C for the used Si devices), which cannot be exceeded. Consequently, semiconductors featuring low on-state resistance and good cooling interfaces have to be chosen for the realization of the IMD.

Experimental verification on the built hardware demonstrators confirms the overload capability of the 7L-FCi, the 7L-HANPC, and the 3L-FCi, even for the worst-case standstill overload where one phase provides full output current continuously for 3 s, cf. **Fig. 4.7**. A comparable overload capability is also expected from the 2L-SSC with CM choke based on its resemblance to the 3L-FCC in terms of semiconductor devices and semiconductor losses for identical device switching frequency.

Not to underestimate is the limited heat spreading capability of, e.g., the baseplate, where the power stage PCBs are mounted for cooling, as it can significantly impact the semiconductor junction temperatures for high transient losses[2]. Hence, it has to be accounted for as part of a dynamic transient thermal model, which allows to anticipate the junction temperatures and/or overload capability of the system. Utilizing such a transient thermal model, it is shown that even a low inverter output frequency (e.g., of 1 Hz) results in a significant stress reduction (compared to standstill) during overload operation. For example, when targeting a maximum allowed junction temperature of 130 °C for the 3L-FCi, an overload factor (i.e., the ratio by which a maximum allowed overload current exceeds the nominal current) of about 2.2 is allowed for 0 Hz inverter output frequency (i.e., standstill). It increases to 2.7 for 1 Hz inverter output frequency. and finally, reaches the full target factor 3 for 10 Hz inverter output frequency.

In the present case, the overload operation is more challenging for the 3L-FCi (and consequently, also for the 2L-SSC) than for the 7L-FCi: first

[2] In the case at hand for the 3L-FCi the restricted heat spreading in the aluminum baseplate causes a transient temperature increase of around +30 °C in the baseplate directly under the semiconductors.

of all, the losses are more concentrated on a smaller PCB area compared to the 7L-FCi, and second, the currently available GaN devices have with 150 °C a lower maximum junction temperature rating than the available Si MOSFETs with 175 °C.
On the other hand, the compact PCB size of the 3L-FCi presents the opportunity for a more direct mounting of the power PCBs on the motor housing in an IMD realization (cf. **Fig. 4.9**). This facilitates the cooling of the critical semiconductors compared to, e.g., the 7L-FCi, which needs to be arranged on severaL PCBs on stacked baseplates as depicted in **Fig. 3.1**.

- **Further Aspects — *Reliability & Control Effort***
  Besides the aforementioned and discussed key criteria, further aspects addressed in this thesis merit a quick consideration:

  Foremost, the examined topologies lack redundancy. Hence, a direct correlation between a higher total component count and diminished reliability is established, as each of these components has the potential to fail during operation. In this regard, the 3L-FCC stands out as significantly superior to the evaluated 7L inverters. It is surpassed only by the 2L-SSC featuring a single CM-choke and no critical Flying Capacitors. On the other hand, said 2L-SSC design lacks full output voltage filtering, which leads to higher voltage stresses in the motor insulation and increased HF motor losses, and consequently, decreases the long-term reliability of the motor itself.

  A similar outcome is evident for the experienced control effort, where the smaller number of FC stages of the 3L-FCi reduces the control effort (and also the risk of control failure) considerably compared to the 7L-FCi. The presented 2L-SSC eliminates all FCs and only a single split DC-Link voltage needs to be controlled, which can be more easily equipped with a larger capacitance value to reduce the dynamics of the system.

All in all, the realization of an IMD with a 3L-FCC and full sine-wave output *LC* filter is deemed to offer the best overall trade-offs in terms of performance and complexity at maximum motor-friendliness. The concept of a 2L-SSC with CM choke, therefore, is an interesting alternative from an industrial point of view, especially thanks to its more standardized building blocks (i.e., six-pack semiconductor modules) and the absence of special control considerations for FC voltage balancing.

6.2 Outlook and Future Research

This thesis evaluates several ML concepts for motor-integrated Variable Speed Drive (VSD) systems with high short-term overload capability and presents the merits and drawbacks of a realization as 7L-FCC, 7L-HANPC, 3L-FCC and 2L-SSC. For potential future research and development, the following aspects should be considered:

- Throughout this work, the primary emphasis was placed on the power electronics rather than on the motor design. However, as seen from the example of the 2L-SSC, where the motor is reconfigured from a single three-phase to a dual three-phase winding-set system, new advantages like CM cancellation and elimination of the FCs emerge, even if the motor is only to a minimal extent included in the design process. A more in-depth co-design of motor and inverter along with thermal and electrical analyses, as well as the efficiency evaluation as a single unit, holds the potential for superior structural and functional motor integration.

- Moreover, from a semiconductor device point-of-view, additional effort in developing modules and packages promises to facilitate motor-integration considerably. While Wide Bandgap (WBG) devices can theoretically operate at considerably higher temperatures than Si devices, the junction temperatures of currently available transistors are strongly limited by the packaging. Further development in this direction should be accompanied with focus on a good package cooling capability, as well as integration of gate driver and level-shifter in a single housing with the power transistor. These are key enablers for more straightforward and reliable hardware designs, which can unlock the full potential of WBG semiconductors in IMD applications.

- During the comparison of the different ML topologies this work has completely omitted economic aspects. This is mainly because component prices may fluctuate over time, and, in particular, do not necessarily have any deterministic relation to prices actually paid by large customers, which are almost entirely based on individual contractual arrangements. Nevertheless, it is worth mentioning that due to the different large quantities of specific component types/materials used in the considered topologies (e.g., the high number of capacitors and semiconductors in the 7L inverters and the large filter inductor in the 3L GaN FCi solution), the economical advantage or disadvantage of

one topology over another can change abruptly based on cost trends affecting its major components.

- A further aspect, that was so far neglected in the comparison, is the environmental impact of the different converter designs, e.g., by employing a Life-Cycle Assessment (LCA). As with the above-discussed pricing, the large quantities of fundamentally different materials in the considered topologies can result in a very contrasting environmental footprint of the IMD.
  From this perspective, also the extent/degree of motor integration has to be scrutinized: For instance, tightly integrating power electronics into the motor can significantly complicate the recycling process. Moreover, power electronic components in an IMD must withstand elevated temperatures and risk increased mechanical stresses, such as vibrations and shocks, in contrast to their counterparts housed in physically separated dedicated cabinets. This can diminish their lifetime, and consequently, negatively affect the LCA of the IMD system, especially if they are arranged in such a way that no easy repair/exchange of the faster aging components is possible.

Therefore, beyond extending the co-design of the motor and inverter stage, it becomes essential to introduce new performance criteria based on the environmental footprint for future Integrated Motor Drives.

Appendices

A

Asymmetries in the Motor

The discussed CM cancellation in **Chapter 5** achievable with the 2L-SSC relies on the basic assumption of a symmetric motor design, i.e., two sets of symmetric motor windings and symmetric capacitive couplings to the rotor and frame. However, in reality, mechanical tolerances must be expected, which can lead to asymmetries in the motor. Their influence on the suggested CM cancellation is briefly discussed in the following with a focus on the parasitic motor capacitances.

A more physical representation of the CM/DM model of the 2L-SSC in **Fig. 5.2(b)** (but shown without the CM choke Z_{CMC}) is given in **Fig. A.1(a)** [111] with separation into the total CM voltage $v_{\mathrm{cm,tot}}$ in **Fig. A.1(b.i)** and the two remaining winding-set-specific CM voltages (i.e., $v_{\mathrm{cm,A}} - v_{\mathrm{cm,tot}} \approx v_{\mathrm{cm,A}}$ and $v_{\mathrm{cm,B}} - v_{\mathrm{cm,tot}} \approx v_{\mathrm{cm,B}}$; due to the small CM voltage spikes of $v_{\mathrm{cm,tot}}$) in **Fig. A.1(b.ii)**. The voltage over the bearing V_{b} can be seen across the rotor-frame capacitance C_{rf}. Note that the bearing capacitance itself is not explicitly drawn here, as it is comparatively small and in parallel to C_{rf}. The other physical parasitic capacitances occurring in a motor are represented by C_{wr} (winding-rotor), C_{wf} (winding-frame), and C_{ww} (winding-winding).

Note that the model of **Fig. 5.2(b)** can be derived from the more physical representation in **Fig. A.1(a)** with

$$C_{\mathrm{cm,A}} = C_{\mathrm{cm,B}} = C_{\mathrm{wf}} + C_{\mathrm{wr}} + 2 \cdot C_{\mathrm{ww}} \tag{A.1}$$

and

$$\begin{aligned} C_{\mathrm{cm}} = [2 \cdot (C_{\mathrm{rf}} \cdot C_{\mathrm{wf}} + C_{\mathrm{rf}} \cdot C_{\mathrm{wr}} + C_{\mathrm{wf}} \cdot C_{\mathrm{wr}}) \\ \cdot (C_{\mathrm{wf}} + C_{\mathrm{wr}} + 2 \cdot C_{\mathrm{ww}})] / \\ (C_{\mathrm{wr}}^2 + 2 \cdot C_{\mathrm{ww}} \cdot C_{\mathrm{wr}} + 2 \cdot C_{\mathrm{rf}} \cdot C_{\mathrm{ww}}) \end{aligned} \tag{A.2}$$

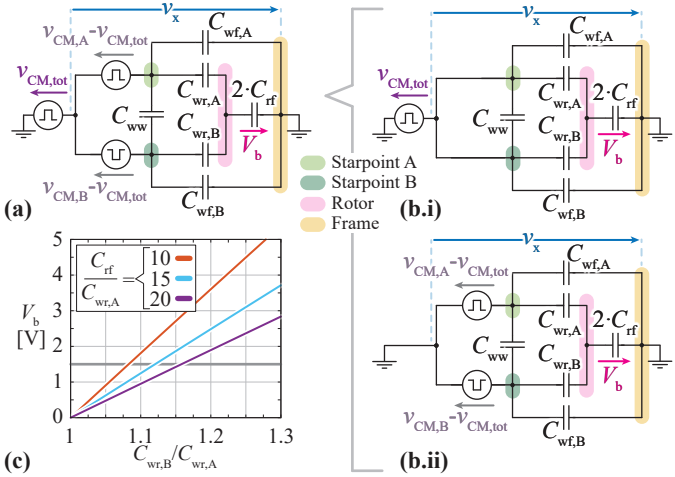


Fig. A.1: (a) More physical equivalent circuit model of the 2L-SSC with dual winding motor. **(b.i)** Separation into $v_{CM,tot}$ contribution and **(b.ii)** the remaining winding set CM voltages ($v_{CM,A} - v_{CM,tot}$ and $v_{CM,B} - v_{CM,tot}$). **(c)** Potentially occuring voltages over bearing V_b in the case of asymmetric $C_{wr,A}$ and $C_{wr,B}$.

if both motor winding systems are identical, e.g., $C_{wr,A} = C_{wr,B}$, i.e., for a perfectly symmetric motor.

Looking at the total CM voltage equivalent part of the model in **Fig. A.1(b.i)**, one can clearly see that the voltage over the bearing V_b is zero if $v_{CM,tot}$ is zero (i.e., ideal CM cancellation with no delays t_d, etc.). In case of a delay (i.e., $v_{cm,tot} \neq 0$ as in **Fig. 5.6(c.i)**), V_b is approximately 1/10th to 1/20th of v_x due to the capacitive divider ratio of $C_{rf}/C_{wr} \approx 10...20$ [111], as mentioned previously. For this purpose, a CM choke Z_{CMC} was designed in this paper to limit v_x to a small specified value of $v_{x,max}$.
Slight asymmetries in the depicted motor capacitances only marginally vary this capacitive voltage divider ratio of v_x, and hence, do not notably impact V_b originating from $v_{cm,tot} \neq 0$.

However, looking at the remaining winding-set-specific CM voltages of **Fig. A.1 (b.ii)** (i.e., $v_{cm,A} - v_{cm,tot}$ and $v_{cm,B} - v_{cm,tot}$) a difference in, e.g., $C_{wr,A}$ and $C_{wr,B}$ directly results in a voltage $V_b \neq 0$ across the bearing. This also occurs for ideal CM cancellation, where the voltages $v_{cm,A}$ and $v_{cm,B}$ as shown in **Fig. 5.2(d)** are directly applicable to **Fig. A.1(b.ii)** since $v_{cm,tot} = 0$. The resulting offset voltage peak value over C_{rf} can be calculated with

superposition as

$$V_{\mathrm{b}} = \frac{(1-n)\cdot C_{\mathrm{wr}}}{(1-n)\cdot C_{\mathrm{wr}} + 2\cdot C_{\mathrm{rf}}} \cdot V, \tag{A.3}$$

where, e.g., $C_{\mathrm{wr,A}} = C_{\mathrm{wr}}$ and $C_{\mathrm{wr,B}} = n \cdot C_{\mathrm{wr}}$ with worst-case $V = |\max(v_{\mathrm{CM,A}} - v_{\mathrm{CM,tot}})| = 400\,\mathrm{V}$ (cf. **Fig. 5.2(d)**). Note that the designed CM choke Z_{CMC} (which is not drawn in **Fig. A.1(b.ii)**) has a negligible impact on this resulting V_{b}, as the CM choke is only dimensioned for small CM voltage spikes and not for the dominant switching frequency harmonics from $v_{\mathrm{cm,A}} - v_{\mathrm{cm,tot}} \approx v_{\mathrm{cm,A}}$.

The resulting V_{b} values are plotted for three different capacitive divider ratios of $C_{\mathrm{rf}}/C_{\mathrm{wr}}$ in **Fig. A.1(c)**. Assuming a lower limit for EDM bearing current occurrence at $V_{\mathrm{b}} = 1.5\,\mathrm{V}$ [111], an approximately 10% difference between $C_{\mathrm{wr,A}}$ and $C_{\mathrm{wr,B}}$ is allowed, which has to be considered during the motor design.

B

Additional Motor Impedance Measurements

The equivalent CM circuit of a configurable multi-winding Permanent Magnet Synchronous Motor (PMSM) is used in **Chapter 5** (**Section 5.3.4**) to design the respective CM chokes for the 3L-Flying Capacitor Converter (3L-FCC) and 2L-SSC. This Appendix shows the CM impedance measurements performed on the motor in more detail: In **Fig. B.1(a)** $\underline{Z}_{\text{single}}$ is obtained for the single winding-set configuration of the PMSM (cf. **Fig. B.1(b.i)**). For the dual winding-set configuration (cf. **Fig. B.1(b.i)**) $\underline{Z}_{\text{dual,PE}}$ and $\underline{Z}_{\text{dual,OPEN}}$ are measured. Thereby, $\underline{Z}_{\text{dual,PE}}$ is obtained when the winding-set of inverter B is connected to PE, i.e., the earth connection of the machine housing, and $\underline{Z}_{\text{dual,OPEN}}$ when the winding-set of inverter B is unconnected (= "OPEN"). Since the measured CM impedances are capacitive for the frequency range of interest, i.e., $f_{\text{sw}} = 35\,\text{kHz}$ and $f_{\text{eff}} = 2 \cdot f_{\text{sw}}$, these three measurements can be used to determine the capacitances C_{W} between the winding-sets (orange in **Fig. B.1(b)**, $C_{\text{W}} = 0.51\,\text{nF}$) and the capacitances C_{PE} from the winding sets to earth (blue in **Fig. B.1(b)**, $C_{\text{PE}} = 0.74\,\text{nF}$); note that already two out of the three measurements suffice for this. The resulting CM equivalent circuit of the single winding system is shown in **Fig. B.1(c.i)** with $C_{\text{CM}} = 6 \cdot C_{\text{PE}} = 4.4\,\text{nF}$. From **Fig. B.1(b.ii)**, the capacitive CM machine model is directly derived for the dual winding-set configuration in **Fig. B.1(c.ii)**, which is identical to the CM machine model already derived for the single winding-set configuration.

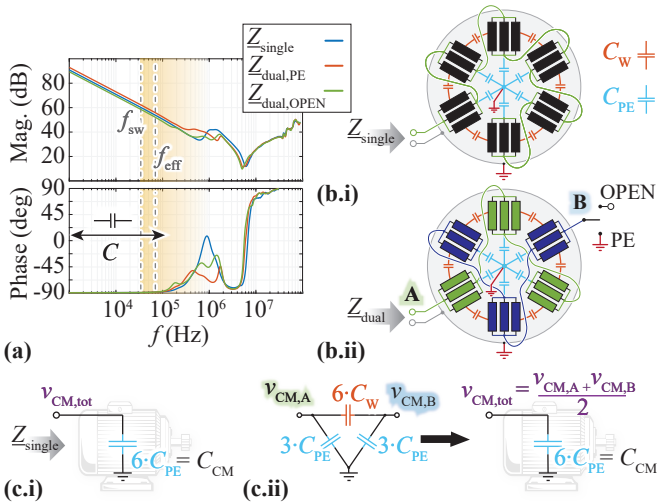


Fig. B.1: (a) Measured motor CM impedances with the single (i.e., $\underline{Z}_{single}$) and dual winding-set configuration (i.e., $\underline{Z}_{dual}$) shown in **(b)**. Thereby, $\underline{Z}_{dual,PE}$ is measured with the winding-set B connected to PE, i.e., the earth connection of the machine housing, and $\underline{Z}_{dual,OPEN}$ with winding-set B unconnected (="OPEN"). **(c)** Resulting CM motor equivalent circuits, which are identical for the single and dual winding-set configuration. Consequently, this model is used for the CM choke design procedure in *Section 5.3.4*.

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