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Concepts, Modelling, and Optimal Design of Integrated Motor Drives

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Abstract

In electrical drives, the inverter and the electric motor have traditionally been designed in separate housings. This separation is eliminated by the concept of *Integrated Motor Drives* (IMD). An IMD is the combination of an electric motor with its driving inverter in one mechanical unit. This concept potentially leads to better drive systems in terms of the quality criteria power density, efficiency, cost, and reliability.
This thesis investigates how IMDs can be optimally designed with regard to these quality criteria. The focus is on IMDs with torque motors. This type of motor is particularly suitable for direct drive applications with high torques and low speeds, such as robot arm joints, electric power steering systems in cars, and printing machine rollers. A three-step methodology is used to determine optimal designs for high-torque IMDs: In a first step, concepts for IMDs known from the literature are classified and the most promising concepts for high-torque IMDs are selected. In a second step, IMDs are modelled for the selected concepts. For this purpose, models from the literature as well as models developed within the scope of this thesis are implemented. In a third step, design procedures for the optimal design of IMDs are developed on the basis of the implemented models and applied in design studies for exemplary specifications of high-torque IMDs. The results of these three steps are summarised below.

The selection of concepts for the design of IMDs is divided into thermo-mechanical integration concepts, inverter topologies, PWM schemes, and motor windings. Considerations on the available motor area for inverter integration and the focus on electronics for the industrial temperature range (85 °C) lead to the selection of a thermo-mechanical integration concept in which the inverter is axially integrated into an end cap. This end cap is passively cooled by cooling fins and is separated from the motor by a thermal insulation layer. Conventional topologies (2L, 3L-NPC, 3L-T-type) and two modular topologies are selected for the inverter topology. The modular topologies consist of n 2L 3-phase modules, which are either connected in series (2L-nM-ser,

also known as *Stacked Polyphase Bridge Converter*/SPB-C) or in parallel (2L-*n*M-par). In addition, conventional and more complex PWM schemes are selected. Double-layer tooth-coil windings are selected for the motor winding. The phase configuration of the motor winding is kept variable in order to investigate the effect of different phase configurations on the power density and efficiency of IMDs.

The implemented models include models at the inverter level, at the motor level, and at the IMD/system level. The models at the inverter level include a PWM model, a model for dimensioning the DC link capacitors, models for the semiconductor conduction and switching losses, and a model for calculating the inverter reliability. The models at the motor level include an electromechanical motor model (i.e. voltage, flux, and torque equations) for multiphase motors, winding loss models (with HF effects), and iron loss models. The models at the IMD/system level include a thermal IMD model, an IMD volume model, and an IMD cost model. The scientific contribution of this work in terms of modelling lies in particular in the iron loss modelling and in the thermal modelling. For the iron losses, the manufacturers of electrical steel sheets usually only provide data on iron loss density for frequencies up to 1 kHz. To extend the iron loss modelling to PWM frequency effects, iron loss density measurements were performed for frequencies up to 100 kHz with different excitation flux density waveforms (1: Sine, 2: Sine + DC offset). Fitting the measured loss density curves leads to a new loss density formula in the frequency domain, which is based on a modification of Bertotti's loss separation approach. As part of the thermal modelling, a thermal model of an end cap with cooling fins was developed and validated in a CFD simulation.

Three design studies are carried out to optimise the design of IMDs. The first two design studies include an optimisation of the entire IMD system. The third design study contains a separate (pre-)optimisation of the finned end cap. The results of the design studies are summarised below.
The first design study compares IMDs consisting of an SPB-C in combination with 3-, 6-, 9-, and 12-phase PMSMs. The general IMD design procedure developed for this design study includes a "2D optimisation" of power density and efficiency. The application of this design procedure to exemplary specifications of a 1.5 kW IMD shows that the

winding factors of 6, 9-, and 12-phase (multiphase) motors are on average 3.7 % higher than the winding factors of 3-phase motors with 2, 3, or 4 phase-aligned winding systems. The higher winding factor can be used to increase the maximum efficiency by 0.70 % or the maximum power density by 3.8 %. In addition, the possible motor-inverter modularity is analysed in this design study. This analysis shows that 3-phase motors with phase-aligned winding systems enable a higher degree of motor-inverter modularity compared to multiphase motors.
In the second design study, a larger design space for inverters is investigated, which includes different inverter topologies, PWM schemes, and switch technologies (Si/SiC/GaN). The general IMD design procedure developed for this design study is a "3D optimisation" of power density, efficiency, and cost. The application of this design procedure to exemplary specifications of a 1.5 kW IMD shows that the cost-optimal system configuration is given by 2L-OC-Si-3ph (2L inverter with optimally clamped PWM, Si-IGBTs, and a 3-phase winding). A pareto-optimal compromise between power density and costs can be achieved with the 2L3Mpar-OC-GaN-9ph configuration (2L-3M-par inverter with optimally clamped PWM, GaN HEMTs, and a 9-phase winding), which enables an efficiency increase of +2.26 % at 36 % higher costs compared to the cost-optimal configuration. Assuming a utilisation of 90 % and an energy price of 0.1 CHF/kWh, the higher costs are compensated for by the lower energy consumption after approximately 2 years. The reliability of the inverters is also analysed in this design study. As a result, the modular topologies 2L-3M-ser and 2L-3M-par only have an advantage over the conventional topologies (2L, 3L-NPC, 3L-T-type) if the former are designed for 2-out-of-3 redundancy, i.e. if partial load operation is possible if up to 2 modules fail.
In the third design study, the optimal design of the finned end cap, which serves as a heat sink for the inverter, is analysed. The general heat sink design procedure developed for this design study optimises the fin spacing and fin thickness and results in the maximum *Cooling System Performance Index* (CSPI) of the end cap. This CSPI can be used by system designers to determine whether a passively cooled heat sink provides sufficient cooling for an integrated inverter (assuming a maximum realistic heat sink volume) or whether another cooling technology with a higher CSPI (e.g. active cooling) is required. Applying the heat sink design procedure to exemplary specifications of high-torque IMDs with diameters between 20 cm and 100 cm results in a CSPI range of

$0.67 \ldots 1.8\,\mathrm{W\,K^{-1}\,L^{-1}}$. This relatively low CSPI range requires a relatively high ratio of diameter to power. Such ratios are characteristic of motors and loads with high torque and low speed, which should therefore be the primary "target group" for passively cooled IMDs.

Among the drive configurations considered in the first two design studies, 3-module SPB-Cs in combination with a symmetrical 9-phase winding pose a particular challenge for the drive control, especially when the inverter is connected to the DC source with a cable. This is because the cable impedance ($R_\mathrm{b}, L_\mathrm{b}$) can cause instabilities that affect the overall DC link voltage and the module voltage balance. This thesis presents a control concept that stabilises the module voltage balance via an appropriate definition of the module reference voltage. The total DC link voltage is not controlled, but the stability is ensured by sufficiently large DC link capacitors. The control concept is validated in a simulation of a 1.5 kW drive system.

Finally, a virtual prototype of a high-torque IMD based on a 3-module SPB-C and a symmetrical 9-phase winding is presented. This virtual prototype includes a PCB design for the inverter and a mechanical CAD model of the IMD. The specifications of the virtual prototype are derived from the second design study. The virtual prototype shows that the design procedure developed for this design study leads to a realistic IMD design.

Kurzfassung

In elektrischen Antrieben wurde der Wechselrichter und der Elektromotor traditionell in separaten Gehäusen entworfen. Diese Trennung wird durch das Konzept der Integrierten Motorantriebe (engl. Integrated Motor Drives, IMD) aufgehoben. Ein IMD ist die Kombination aus einem Elektromotor und einem Antriebsumrichter in einer mechanischen Einheit. Dieses Konzept führt potenziell zu besseren Antriebssystemen im Hinblick auf die Qualitätskriterien Leistungsdichte, Effizienz, Kosten und Zuverlässigkeit.
In dieser Arbeit wird untersucht, wie IMDs hinsichtlich dieser Qualitätskriterien optimal entworfen werden können. Dabei liegt der Fokus auf IMDs mit Torquemotoren. Dieser Motortyp eignet sich besonders für Direktantriebsanwendungen mit hohen Drehmomenten und niedrigen Drehzahlen, wie z. B. Roboterarmgelenke, elektrische Servolenkungen in Autos und Druckmaschinenwalzen. Zur Bestimmung optimaler Entwürfe für Hochdrehmoment-IMDs wird eine dreischrittige Methodik angewendet: In einem ersten Schritt werden aus der Literatur bekannte Konzepte für IMDs klassifiziert und die vielversprechendsten Konzepte für Hochdrehmoment-IMDs ausgewählt. In einem zweiten Schritt werden IMDs für die ausgewählten Konzepte modelliert. Dazu werden Modelle aus der Literatur sowie im Rahmen dieser Arbeit entwickelte Modelle implementiert. In einem dritten Schritt werden auf der Basis der implementierten Modelle Entwurfsverfahren für den optimalen Entwurf von IMDs entwickelt und in Entwurfsstudien für beispielhafte Spezifikationen von Hochdrehmoment-IMDs angewendet. Im Folgenden werden zunächst die Ergebnisse dieser drei Schritte zusammengefasst.

Die Auswahl von Konzepten für den Entwurf von IMDs ist aufgeteilt in thermo-mechanische Integrationskonzepte, Wechselrichtertopologien, PWM-Schemata und Motorwicklungen. Überlegungen zur verfügbaren Motorfläche für die Wechselrichterintegration und der Fokus auf Elektronik für den industriellen Temperaturbereich (85 °C) führen zur Auswahl eines thermo-mechanischen Integrationskonzepts, in dem der Wechselrichter axial in eine Endkappe integriert ist. Diese Endkappe wird

durch Kühlrippen passiv gekühlt und ist durch eine thermische Isolationsschicht vom Motor getrennt. Für die Wechselrichter-Topologie werden konventionelle Topologien (2L, 3L-NPC, 3L-T-Typ) und zwei modulare Topologien ausgewählt. Die modularen Topologien bestehen aus n 2L 3-Phasen-Modulen, die entweder in Reihe verschaltet werden (2L-nM-ser, auch bekannt als *Stacked Polyphase Bridge Converter*/SPB-C) oder parallel verschaltet werden (2L-nM-par). Darüber hinaus werden konventionelle sowie komplexere PWM-Schemata ausgewählt. Für die Motorwicklung werden zweischichtige Zahnspulenwicklungen gewählt. Die Phasenkonfiguration der Motorwicklung wird variabel gehalten, um die Auswirkung verschiedener Phasenkonfigurationen auf die Leistungsdichte und Effizienz von IMDs zu untersuchen.

Die implementierten Modelle umfassen Modelle auf der Wechselrichterebene, auf der Motorebene und auf der IMD-/Systemebene. Die Modelle auf der Wechselrichterebene umfassen ein PWM-Modell, ein Modell zur Dimensionierung der DC-Zwischenkreiskondensatoren, Modelle für die Leitungs- und Schaltverluste in Halbleitern, sowie ein Modell zur Berechnung der Wechselrichter-Zuverlässigkeit. Die Modelle auf der Motorebene umfassen ein elektromechanisches Motormodell (d. h. Spannungs-, Fluss-, und Drehmomentgleichungen) für Mehrphasenmotoren, Wicklungsverlustmodelle (mit HF-Effekten) und Eisenverlustmodelle. Die Modelle auf der IMD-/Systemebene umfassen ein thermisches IMD-Modell, ein IMD-Volumenmodell und ein IMD-Kostenmodell. Der wissenschaftliche Beitrag dieser Arbeit in Bezug auf die Modellierung liegt insbesondere in der Eisenverlustmodellierung und in der thermischen Modellierung. Für die Eisenverluste stellen die Hersteller von Elektroblechen in der Regel nur Daten zur Eisenverlustdichte für Frequenzen bis zu 1 kHz zur Verfügung. Um die Eisenverlustmodellierung auf PWM-Frequenzeffekte auszudehnen, wurden Eisenverlustdichtemessungen für Frequenzen bis zu 100 kHz mit verschiedenen Wellenformen der Erregerflussdichte (1: Sinus, 2: Sinus + DC-Offset) durchgeführt. Das Fitting der gemessenen Verlustdichtekurven führt zu einer neuen Verlustdichteformel im Frequenzbereich, die auf einer Modifikation des Verlustseparationsansatzes von Bertotti beruht. Im Rahmen der thermischen Modellierung wurde ein thermisches Modell einer Endkappe mit Kühlrippen entwickelt und in einer CFD-Simulation validiert.

Drei Entwurfsstudien zum optimalen Entwurf von IMDs werden durchgeführt. Die ersten beiden Entwurfsstudien beinhalten eine Optimierung des gesamten IMD-Systems. Die dritte Entwurfsstudie enthält eine separate (Vor-)Optimierung der gerippten Endkappe. Die Ergebnisse der Entwurfsstudien werden im Folgenden zusammengefasst.
Die erste Entwurfsstudie vergleicht IMDs, die aus einem SPB-C in Kombination mit 3-, 6-, 9- und 12-phasigen PMSMs bestehen. Das für diese Entwurfsstudie entwickelte allgemeine IMD-Entwurfsverfahren beinhaltet eine "2D-Optimierung" von Leistungsdichte und Wirkungsgrad. Die Anwendung dieses Entwurfsverfahrens auf beispielhafte Spezifikationen eines 1.5 kW IMD zeigt, dass die Wicklungsfaktoren der 6-, 9- und 12-phasigen (mehrphasigen) Motoren im Durchschnitt 3.7 % höher sind als die Wicklungsfaktoren von 3-phasigen Motoren mit 2, 3 oder 4 phasengleichen Wicklungssystemen. Der höhere Wicklungsfaktor kann genutzt werden, um den maximalen Wirkungsgrad um 0.70 % oder die maximale Leistungsdichte um 3.8 % zu erhöhen. Darüber hinaus wird in dieser Entwurfsstudie die mögliche Motor-Umrichter-Modularität analysiert. Diese Analyse zeigt, dass 3-Phasen-Motoren mit phasengleichen Wicklungssystemen im Vergleich zu mehrphasigen Motoren einen höheren Grad an Motor-Umrichter-Modularität ermöglichen.
In der zweiten Entwurfsstudie wird ein größerer Entwurfsraum für Wechselrichter untersucht, der verschiedene Wechselrichter-Topologien, PWM-Schemata und Schaltertechnologien (Si/SiC/GaN) umfasst. Das allgemeine IMD-Entwurfsverfahren, das für diese Entwurfsstudie entwickelt wurde, ist eine "3D-Optimierung" von Leistungsdichte, Effizienz und Kosten. Die Anwendung dieses Entwurfsverfahrens auf beispielhafte Spezifikationen eines 1.5 kW IMD zeigt, dass die kostenoptimale Systemkonfiguration durch 2L-OC-Si-3ph (2L-Wechselrichter mit optimal geklemmter PWM, Si-IGBTs und einer 3-phasigen Wicklung) gegeben ist. Ein pareto-optimaler Kompromiss zwischen Leistungsdichte und Kosten kann mit der Konfiguration 2L3Mpar-OC-GaN-9ph (2L-3M-par-Wechselrichter mit optimal geklemmter PWM, GaN-HEMTs und einer 9-phasigen Wicklung) erreicht werden, die eine Effizienzsteigerung von +2.26 % bei 36 % höheren Kosten im Vergleich zur kostenoptimalen Konfiguration ermöglicht. Bei einer Auslastung von 90 % und einem Energiepreis von 0,1 CHF/kWh werden die höheren Kosten durch den geringeren Energieverbrauch nach etwa 2 Jahren kompensiert. Weiterhin wird in dieser Entwurfsstudie die Zuverlässigkeit der Wechselrichter untersucht. Im Ergebnis haben die modularen

Topologien 2L-3M-ser und 2L-3M-par nur dann einen Vorteil gegenüber den konventionellen Topologien (2L, 3L-NPC, 3L-T-Typ), wenn erstere für eine 2-aus-3-Redundanz ausgelegt sind, d.h. wenn ein Teillastbetrieb bei Ausfall von bis zu 2 Modulen möglich ist.
In der dritten Entwurfsstudie wird der optimale Entwurf der gerippten Endkappe untersucht, die als Kühlkörper für den Wechselrichter dient. Das für diese Entwurfsstudie entwickelte allgemeine Kühlkörperentwurfsverfahren optimiert den Rippenabstand und die Rippendicke und ergibt den maximalen *Cooling System Performance Index* (CSPI) der Endkappe. Dieser CSPI kann von Systemingenieuren verwendet werden, um festzustellen, ob ein passiv gekühlter Kühlkörper eine ausreichende Kühlung für einen integrierten Wechselrichter bietet (unter der Annahme eines maximalen realistischen Kühlkörpervolumens) oder ob eine andere Kühltechnologie mit einem höheren CSPI (z. B. aktive Kühlung) erforderlich ist. Die Anwendung des Kühlkörperentwurfsverfahrens auf beispielhafte Spezifikationen von Hochdrehmoment-IMDs mit Durchmessern zwischen 20 cm und 100 cm ergibt einen CSPI-Bereich von $0.67 \ldots 1.8\,\mathrm{W\,K^{-1}\,L^{-1}}$. Dieser relativ niedrige CSPI-Bereich erfordert ein relativ hohes Verhältnis von Durchmesser zu Leistung. Solche Verhältnisse sind charakteristisch für Motoren und Lasten mit hohem Drehmoment und niedriger Drehzahl, die daher die primäre "Zielgruppe" für passiv gekühlte IMDs sein sollten.

Unter den Antriebskonfigurationen, die in den ersten beiden Entwurfsstudien betrachtet werden, stellen 3-modulige SPB-Cs in Kombination mit einer symmetrischem 9-Phasen-Wicklung eine besondere Herausforderung für die Antriebssteuerung dar, insbesondere wenn der Umrichter über ein Kabel mit der Gleichstromquelle verbunden ist. Dies liegt daran, dass die Kabelimpedanz ($R_\mathrm{b}, L_\mathrm{b}$) Instabilitäten verursachen kann, die sich auf die Gesamt-Zwischenkreisspannung und die Spannungsbalance der Module auswirken. In dieser Arbeit wird ein Regelungskonzept vorgestellt, das die Modulspannungsbalance durch eine geeignete Definition der Modulreferenzspannung stabilisiert. Die Gesamt-Zwischenkreisspannung wird nicht geregelt, sondern die Stabilität wird durch ausreichend große Zwischenkreiskondensatoren sichergestellt. Das Regelungskonzept wird in einer Simulation eines 1.5 kW-Antriebssystems validiert.

Schließlich wird ein virtueller Prototyp eines Hochdrehmoment-

IMDs auf der Grundlage eines 3-moduligen SPB-Cs und einer symmetrischen 9-Phasen-Wicklung vorgestellt. Dieser virtuelle Prototyp umfasst einen PCB-Entwurf für den Wechselrichter und ein mechanisches CAD-Modell des IMDs. Die Spezifikationen des virtuellen Prototyps ergeben sich aus der zweiten Entwurfsstudie. Der virtuelle Prototyp zeigt, dass das für diese Entwurfsstudie entwickelte Entwurfsverfahren zu einem realistischen IMD-Entwurf führt.

Abbreviations

AC	...	Alternating Current
BLAC	...	Brushless AC (Motor)
BLDC	...	Brushless DC (Motor)
BSC	...	Bottom-Side Cooled
CAD	...	Computer Aided Design
CSPI	...	Cooling System Performance Index
DC	...	Direct Current
DOF	...	Degree Of Freedom
GND	...	Ground
HF	...	High-Frequency
IMD	...	Integrated Motor Drive
IMMD	...	Integrated Modular Motor Drive
LF	...	Low-Frequency
LPTN	...	Lumped Parameter Thermal Network
LUT	...	Lookup Table
MMF	...	Magnetomotive Force
PCB	...	Printed Circuit Board
PE	...	Power Electronics
PMSM	...	Permanent Magnet Synchronous Motor
PWM	...	Pulse-Width Modulation
SD	...	Semiconductor Device
SDG	...	Semiconductor Device Group
SDU	...	Switch-Diode Unit
SPB-C	...	Stacked Polyphase Bridge Converter
SSM	...	State Space Model
THD	...	Total harmonic distortion
TSC	...	Top-Side Cooled
TRIAC	...	Triode for Alternating Current

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1 Introduction

Electrical drives play an important role in our daily lives and in the global economy, as for example in the mobility sector, in the industry, and in households. In the mobility sector, significant parts of the public transport are already based on electrical drives such as trains and tramways. Climate change and the need for decreasing greenhouse gas emissions lead to increasing efforts for further electrification of the public and private transport, which goes along with more and more electric cars, buses, and even with the development of electric planes. In the industry, electrical drives are already omnipresent in applications like fans, pumps, conveyor systems, machine tools, etc. The same is true for households with applications like washing machines, vacuum cleaners, hairdryers, mixers, etc. General quality criteria for electrical drives are power density, efficiency, cost, and reliability.

A possible concept to improve electrical drives with regard to these criteria is the concept of Integrated Motor Drives (IMDs). An IMD combines an electric motor with its driving inverter in one mechanical unit. First steps toward IMDs date back to the development of automotive alternators in 1960, where the diodes of an uncontrolled full-wave bridge converter are mounted inside the alternator housing close to the claw-pole synchronous alternator machine [1]. IMDs that include controlled power electronics became first commercially available in 1987 with an Electronically-Commutated Motor (ECM) by GE for heating, ventilating and air conditioning applications [1]. One of the latest IMD product developments is the traction motor drive of the Tesla Model 3 that was introduced in 2017.

In the following sections of this chapter, first the motivation and challenges for IMDs are explained in section 1.1. Then, the specifications of

an electric motor that is used as a basis for concept investigation, modelling, and optimal design of IMDs is given in section 1.2. An outline of this thesis with a description of the contributions is given in section 1.3. Furthermore, the publications related to this thesis are listed in section 1.4, and an overview of parts of the thesis that were published previously is given in section 1.5.

1.1 Motivation and Challenges for Integrated Motor Drives

The basic motivation for the development of IMDs is to improve drive systems in terms of power density, efficiency, cost, and reliability:

- **Power density:** IMDs are potentially smaller and lighter than conventional motor drives as separate housings for the motor and for the inverter can be replaced by a single housing and the need of AC cables between the motor and the inverter is eliminated [1–4]. Assuming a constant distance between the DC source and the motor, shorter AC cables at the cost of longer DC cables result in less insulation material. Motor drive volume reductions of 10-20 % are possible [2, 3, 5].
- **Efficiency:** Some reviews on IMDs state that IMDs can lead to an efficiency increase of $30\,\% - 50\,\%$ compared to fixed-speed, line-fed induction motors [1, 4]. However, it is unclear whether this efficiency increase is only due to the drive integration or (which is more probable) also due to a different motor type that is assumed as a basis of the IMD. If a PMSM is assumed as a basis, an efficiency increase is already given for conventional (non-integrated) motor drives because PMSMs are more efficient than induction motors [6]. Nevertheless, IMDs can also gain in efficiency if a potential increase in power density, e.g. through less total housing material, is compensated with a larger inverter heat sink volume, which reduces the semiconductor junction temperature and hence (as the on-resistance/conduction losses decrease) increases the IMD efficiency.
- **Cost:** IMDs have the potential to reduce manufacturing costs, cost of installation, and cost of energy [1–4, 7]. Lower manufacturing costs can result from less housing material, from the

elimination of shielded AC cables, and from a single cooling system for both the motor and the inverter. In addition, economies of scale can reduce the manufacturing costs when a modular IMD structure is adopted which results in high production numbers of the same module. The cost of installation is reduced as the need for a separate installation of a motor and an inverter is eliminated. Reductions of the manufacturing and installation costs of 30-40 % are possible [3, 5]. Finally, the cost of energy can be reduced by means of a higher efficiency.

- **Reliability:** IMDs can result in a higher reliability compared to conventional motor drives in terms of a higher fault-tolerance and less electromagnetic interference (EMI) [1–4, 7]. Higher fault-tolerance can be achieved by means of modular inverter topologies and modular motor windings where one inverter/winding module can fail while the other modules provide part-load operating capability. One the one hand, EMI is reduced by eliminating long AC cables that could lead to cable reflections and inductive coupling. On the other hand, EMI is also a challenge for IMDs as described later in this section.

Despite the motivation for IMDs, there are some technical challenges that engineers have to face in order to leverage the full potential of IMDs:

- **Limited space:** The available space for an integrated inverter is limited by the motor. Depending on the motor specifications in terms of rated torque and speed, the motor outer diameter and length vary, which can favour different integration concepts and inverter module geometries. This makes scaling of IMDs over large power ranges difficult. Furthermore, a challenge is to reduce/optimise the DC link capacitor volume as this can make up 30 % of the inverter volume [8].
- **Heat dissipation:** A motor and an inverter generate heat that must be dissipated. Integrating an inverter into a motor results in two heat sources in close proximity to each other, which is a thermal management problem [1, 2, 4, 7]. Therefore, a major challenge of IMD design is to develop, model, and optimise thermo-mechanical integration concepts that efficiently dissipate the generated heat combined with a compact mechanical integration.

- **Limited thermal ruggedness of electronics:** Linked to the challenge of heat dissipation is the limited thermal ruggedness of power electronics and auxiliary electronics [1, 2, 4, 7]. Typical motor operating temperatures are up to 150..180 °C [4]. However, typical operating temperatures of industrial electronics are 70..85 °C [9]. Therefore, a cooling system must be designed that effectively limits the operating temperature of the electronics.

- **Vibrations:** In addition to high temperatures, the electronics of an IMD face a harsh mechanical environment with high vibrations [1–4]. Vibrations are a risk for electrical and thermal connections and hence for the IMD lifetime.

- **EMI:** As mentioned in the previous section, motor drive integration can lead to to positive effects with respect to EMI but is also linked to the challenge of protecting the inverter from potential parasitic electromagnetic fields in the proximity of the motor windings. [2].

In the following, two key technological aspects are emphasised that play an important role in the development of highly compact and efficient IMDs. These aspects can also be considered as design tools in a more abstract sense which can help to overcome in particular the first two challenges mentioned above (limited space and heat dissipation):

- **Wide-bandgap semiconductors:** Wide-bandgap (WBG) semiconductor materials such as silicon carbide (SiC) and gallium nitride (GaN) have superior material properties compared to silicon (Si) in terms of bandgap, dielectric strength, thermal conductivity (only SiC), and saturation electron velocity as shown in Tab. I of [1]. These advantages on the material level lead to advantages on the device level which are a higher maximum junction temperature, a lower on-state resistance (for a constant chip size and voltage rating), a lower junction-to-case thermal resistance, faster rise and fall times, and a lower gate-to-source capacitance (due to a smaller chip size assuming a constant on-state resistance) [1]. On the system level, these advantages lead to lower conduction losses, lower switching losses, and smaller heat sinks, which improves the IMD power density/efficiency [1]. However, the fast switching also poses a challenge as a high $^{\mathrm{d}v}/_{\mathrm{d}t}$ at the motor terminals can lead to winding insulation damage, motor

bearing damage, and increased EMI [4]. Possible solutions to reduce the $^{dv}/_{dt}$ are a decrease of the switching speed with larger gate resistors, the use of inverter output filters, and the use of current source inverters (CSI) [4].

- **Modularity:** Two types of modular IMDs can be distinguished which are 1) IMDs with a modular inverter and 2) IMDs with a combined modularisation of the inverter and of the motor. The latter type of IMDs was introduced as Integrated Modular Motor Drive (IMMD) in [10]. The potential benefits of a modular design are improvements with regard to fault-tolerance, manufacturability, cost, and size [1–4]. The fault tolerance is improved by means of a modular inverter topology that enables part load operation capability of (n-1) modules if one module fails [3]. The manufacturing process is simplified by splitting up the total inverter (or the combined motor-inverter system in case of an IMMD) into identical smaller modules, which also reduces the manufacturing costs. In addition, inverter modularisation favours a more compact integration into the motor as inverter modules can be distributed on the curved/round motor surfaces [2].

1.2 Specifications of the Project Motor

A motor type that is particularly suitable for drive integration is the torque motor which is characterised by a relatively high rated torque and a low rated speed. As the motor volume scales with its rated torque, torque motors provide relatively large outer surfaces which favour a drive integration. Torque motors are typically used for applications that require a high torque and a high positioning accuracy such as rotary tables, servo presses, and servo valves.
To use this advantage of torque motors and to investigate their full potential for IMDs, the IMD design procedures presented in this thesis (in chapter 4) are primarily developed for torque motors and are applied to the specifications of an exemplary torque motor which is called project motor in the following. The specifications of the project motor are given in Tab. 1.1.

Nominal/Rated speed n_{N} [rpm]	300
Nominal/Rated torque M_{N} [Nm]	48
Nominal/Rated power P_{N} [W]	1508
Nominal/Rated current I_{N} [A]	2.9
Stall torque M_0 [Nm]	50
Stall current I_0 [A]	3
Maximum torque M_{max} [Nm]	173
Maximum current I_{max} [A]	18.2
Maximum speed n_{max} [rpm]	1200
Torque constant K_{T} [$\mathrm{N\,m\,A^{-1}}$]	16.8
Voltage constant K_{E} [V/1000 rpm]	1015.78
Stator resistance $R_{2\mathrm{ph}}$ [Ω]	10.88
Stator inductance $L_{2\mathrm{ph}}$ [mH]	82.57
Number of pole pairs p	12
Number of stator slots N	27
Electrical time constant t_{el} [ms]	7.6
Thermal time constant t_{therm} [min]	50
Moment of inertia J [$\mathrm{kg\,cm^2}$]	409
Weight without brake m [kg]	33
Diameter d [mm]	230
Length l [mm]	275

Table 1.1: Specifications of an exemplary torque motor, referred to as project motor.

Considered General Drive System Configuration

The considered general drive system configuration from the grid to the motor is shown in Fig. 1.1. The scope of this thesis includes the inverter and the motor, as indicated by the dotted line in Fig. 1.1. The focus of this thesis is on IMDs with a DC voltage at the inverter input of 800 V which could for example be provided by an active PFC rectifier. However, also other DC link voltages are considered in the design studies presented in chapter 4.

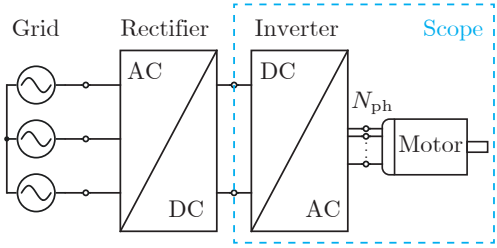


Figure 1.1: Considered general drive system configuration and scope of this thesis.

1.3 Thesis Outline and Contributions

This section gives an overview of the chapters and of the contributions of this thesis.

- **Chapter 1** introduces the concept of IMDs and its motivation in terms of improved drive system power density, efficiency, costs, and reliability. An overview of major technical challenges is given and important IMD "design tools" such as WBG devices and modularity are highlighted. In addition, the specifications of a 1.5 kW torque motor are given which are used for the application of IMD design procedures presented in this thesis.

- **Chapter 2** is the result of a literature research on IMD design concepts. These concepts are divided into the concept categories 1) thermo-mechanical integration concepts, 2) inverter topologies, 3) PWM schemes, and 4) motor windings. For each of these concept categories, the most relevant concepts are identified, classified, and evaluated with regard to their suitability for an IMD design for torque motors. For each concept category, the most suitable concepts are selected for the modelling presented in chapter 3 and for the optimal design procedures presented in chapter 4. The contribution of chapter 2 is the overview over possible IMD design concepts with a relatively broad scope and the identification of concepts particularly suited for high-torque IMDs.

- **Chapter 3** is a collection of models that can be used in procedures for the optimal design of IMDs as for example the IMD design procedures that are presented in chapter 4. Chapter 3

includes models at the inverter level, at the motor level, and at the IMD/system level. The models at the inverter level include a PWM model, a model for dimensioning the DC link, models for the semiconductor conduction and switching losses, and a model for calculating the inverter reliability. The models at the motor level include an electromechanical motor model (i.e. voltage, flux, and torque equations) for multiphase motors, winding loss models (with HF effects) and iron loss models. The models at the IMD/system level include a thermal IMD model, an IMD volume model and an IMD cost model. The scientific contribution of this chapter lies in particular in the iron loss modelling and in the thermal modelling. For the iron losses, the manufacturers of electrical steel typically provide data on iron loss density for frequencies only up to 1 kHz. To extend the iron loss modelling to PWM frequency effects, iron loss density measurements were performed for frequencies up to 100 kHz with different excitation flux density waveforms (1: Sine, 2: Sine + DC offset). Fitting the measured loss density curves leads to a new loss density formula in the frequency domain which is based on a modification of Bertotti's loss separation approach. As part of the thermal modelling, a thermal model of an end cap with cooling fins was developed and validated in a CFD simulation.

- **Chapter 4** presents three design studies each of which includes a general design procedure for the optimal design of IMDs or of an IMD component and the application of this design procedure to exemplary specifications of high-torque IMDs. The contribution of chapter 4 particularly lies in the developed general design procedures. These include 1) an IMD design procedure based on a 2D-optimisation with regard to power density and efficieny, 2) an IMD design procedure based on a 3D-optimisation with regard to power density, efficiency, and costs for a larger inverter design space, and 3) a design procedure for a finned inverter heat sink/end cap suitable for IMDs.

- **Chapter 5** presents a control concept for a drive system consisting of a 9-phase PMSM and of a stacked polyphase bridge converter (SPB-C) under consideration of a DC source impedance (R_b, L_b). When the converter is connected to the DC source with a cable, the cable impedance represents a source impedance that

could cause instabilities affecting the total DC link voltage and the module voltage balance. In this chapter, a control concept is presented for stabilising the module voltage balance via an appropriate definition of the module reference voltage. The total DC link voltage is not controlled but stability is ensured by sufficiently large DC link capacitors. The complete drive controller concept is validated in a simulation of a 1.5 kW drive system. The contribution of chapter 5 lies in the extension of an existing control concept [11] to the consideration of the DC source impedance.

- **Chapter 6** presents a virtual prototype of an IMD consisting of a 9-phase PMSM and of an SPB-C. This virtual prototype includes a PCB design for the inverter and a mechanical CAD model of the IMD. The specifications of the virtual prototype are derived from the design study presented in section 4.2. The virtual prototype shows that the design procedure developed for this design study leads to a realistic IMD design.
- **Chapter 7** draws a conclusion on the thesis and gives an outlook on potential future research topics.

1.4 List of Publications

The following publications resulted from this research project, listed in chronological order.

1. T. Bringezu and J. Biela, "Comparison of optimized motor-inverter systems using a Stacked Polyphase Bridge Converter combined with a 3-, 6-, 9-, or 12-phase PMSM," *22nd European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Lyon, France, 2020, pp. P.1-P.11

2. T. Bringezu and J. Biela, "Cooling limits of passively cooled integrated motor drives," *23rd European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Ghent, Belgium, 2021, pp. P.1-P.11

3. T. Bringezu and J. Biela, "Optimal design of integrated motor drives - Comparison of topologies (2L/3L/modular), PWM

variants, and switch technologies (Si/SiC/GaN)," *24th European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Hanover, Germany, 2022, pp. P.1-P.11.

4. T. Bringezu and J. Biela, "Control of a 9-Phase PMSM with Stacked Polyphase Bridge Converter including DC Source Impedance," *25th European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Aalborg, Denmark, 2023, pp. 1-12

1.5 Parts of Thesis Published Previously

Some parts of this thesis have already been published (completely or in essence) in the international conference proceedings listed in section 1.4. Tab. 1.2 gives an overview of these parts.

Table 1.2: Parts of the thesis that have been published previously. Numbering of the publications according to the order of publications in section 1.4.

Part of the thesis	Publication
Sections: 3.2 (parts on 2L-SPWM), 3.6, 4.1 Figures: 3.16, 3.19a, 3.20, 4.1-4.4	① ©2020 IEEE
Sections: 2.1.2, 3.10, 4.3 Figures: 2.8-2.11, 3.53-3.56, 4.11-4.13	② ©2021 IEEE
Sections: 3.8.3 (part on MLSE5+BPG), 3.12, 3.5, 4.2 Figures: 3.36, 4.5-4.10	③ ©2022 IEEE
Sections: 5 Figures: 5.1-5.12	④ ©2023 IEEE

2 Concepts for Integrated Motor Drives

This chapter gives an overview of existing design concepts for IMDs resulting from a literature research including scientific papers and patents. The concepts are divided into thermo-mechanical integration concepts, inverter topologies, PWM schemes, and motor windings. For each of these concept categories, the most relevant concepts are identified, classified, and evaluated with regard to their suitability for an IMD design based on the torque motor specifications given in section 1.2. The most suitable concepts are selected for the modelling presented in chapter 3 and for the optimal design procedures presented in chapter 4.

2.1 Thermo-Mechanical Integration Concepts

Two main challenges of IMD design are, as mentioned in section 1.1, the little space that is available in a motor housing for an integrated inverter and the dissipation of heat that is generated by the inverter and by the motor. Solving these two challenges is the purpose of a thermo-mechanical integration concept. Such a concept defines the mechanical/structural integration, i.e. where the power electronics are placed in/on the motor housing and also the thermal/cooling concept, i.e. whether the inverter and the motor are cooled separately or with a combined heat sink and what kind of cooling technology is used. The mechanical and the thermal concepts are considered together within one thermo-mechanical integration concept because the position

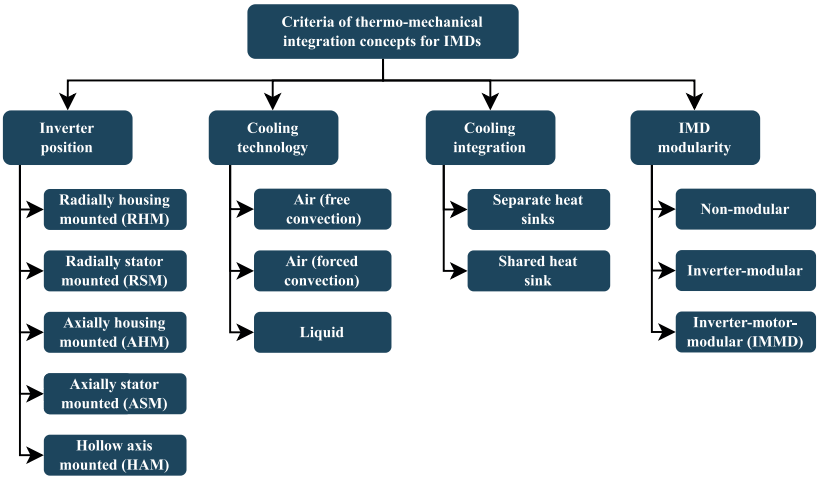


Figure 2.1: Classification of thermo-mechanical integration concepts of IMDs.

of the power electronics also defines the position of one of the main heat sources and hence a requirement for the cooling concept to ensure sufficient heat dissipation from that position to a heat sink. In the following, first an overview of thermo-mechanical integration concepts known from literature is given based on a classification of concepts. Then, the thermo-mechanical integration concept that is used for the IMD modelling and design in chapter 3 & 4 is presented.

2.1.1 Classification of Concepts

Fig. 2.1 shows a possible classification of thermo-mechanical integration concepts of IMDs. Therein, the characteristic criteria by which IMD concepts are classified are the inverter position, the cooling technology, the degree of cooling integration, and the IMD modularity. The different thermo-mechanical integration concepts that can be distinguished within each of these criteria are described in the following.

Inverter position concepts

In most of the IMDs mentioned in literature the inverter is positioned radially or axially on the motor housing or on the stator iron within the motor housing. These most common inverter positions are conceptualised in [3] as 1) radially housing-mounted (RHM), 2) axially housing-mounted (AHM), 3) radially stator iron-mounted, and 4) axially stator iron-mounted (ASM), as shown in Fig. 2.2 (from [3]). Example designs of radially housing/stator mounted (RHM/RSM) IMDs and of axially housing/stator mounted (AHM/ASM) IMDs are shown in Fig. 5 & Fig. 6 of [3], respectively. The advantages and disadvantages of the different inverter positioning concepts are summarised in Tab. 2.1 and are explained in the following.
Whether radial or axial integration is more suitable primarily depends on the motor dimensions. Motors with a large length-to-diameter ratio, which are typically high-speed motors, provide more space on the radial motor surface and hence favour radial integration (RHM & RSM). Inversely, motors with a large diameter-to-length ratio, which are typically high-torque motors, provide more space on the axial surface and therefore favour axial integration (AHM & ASM) [3]. A disadvantage of radial integration is the curved radial motor surface which must be transformed into segments of flattened surfaces for inverter integration, resulting in more iron or housing material.
The stator-iron mounted concepts (RSM & ASM) lead to more compact IMDs than the housing mounted concepts (RHS & AHM) as addi-

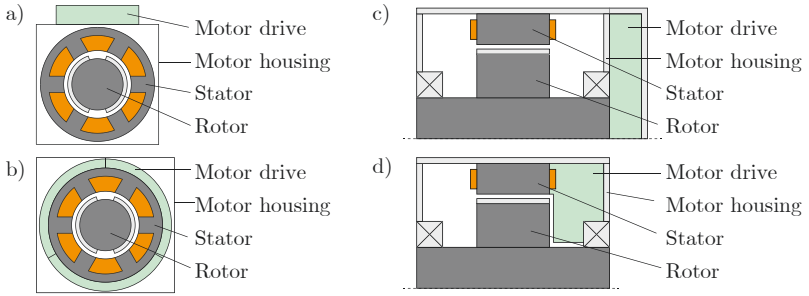


Figure 2.2: Most common inverter positioning concepts of IMDs reported in literature [3]. (a) RHM. (b) RSM. (c) AHM. (d) ASM.

Table 2.1: Advantages and disadvantages of different IMD positioning concepts.

Inverter position	Advantages	Disadvantages
Radially mounted (RHM & RSM)	• Much space for an inverter in high-speed motors • Axial surfaces stay free for gearbox/fan	• Little space for an inverter in high-torque motors • Curved surface
Axially mounted (AHM & ASM)	• Much space for an inverter in high-torque motors • Flat surface	• Little space for an inverter in high-speed motors • Little space for axial gearbox/fan
Housing mounted (RHM & AHM)	• Simple design • More inverter space • Simple cooling • Less EMI • Easy maintenance	• Less compact • Less efficient cooling
Stator-iron mounted (RSM & ASM)	• More compact • More efficient cooling	• Complex design • Limited inverter space • Requires sophisticated cooling • More EMI • Difficult maintenance

tional inverter housing material is eliminated [3]. However, stator-iron mounted inverters require a more complex design due to the limited space and the high temperatures within the motor housing [3]. A sophisticated cooling system is required that limits the ambient temperature of the electronics. Further disadvantages or challenges of the stator iron-mounted concepts (RSM & ASM) are larger EMI due to the proximity of the power electronics to the motor windings and higher maintenance costs due to the higher integration level which makes for example the replacement of defect electronics more difficult.
In this research project, efforts were made to develop a new positioning concept beyond the four concepts from Fig. 2.2 with the motivation to further increase the integration level and power density of stator iron-mounted IMDs. Ideally, such a concept should completely merge the inverter volume and the motor volume instead of adding extra volume to the motor. This consideration lead to the concept of a hollow axis-mounted (HAM) inverter that is however already protected by [12, 13]. The concept of a HAM inverter is shown in Fig. 2.3 in two variants. The first variant (Fig. 2.3a) is based on an inner-rotor PMSM, whereas the second variant (Fig. 2.3b) is based on an outer-rotor PMSM. In

both variants the inverter is placed inside the cavity of a non-moving part inside the motor axis. In the inner-rotor variant, this non-moving part is connected to the rotor through a roller bearing. In the outer-rotor variant, such a roller bearing is not necessary as the non-moving part providing the cavity for the inverter is already given by the stator. The outer-rotor is connected to the stator in the same way as conventional (non-integrated) outer-rotor PMSMs, i.e. via ball bearings at the motor front and back.

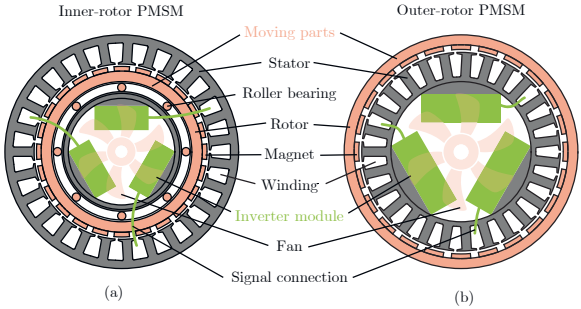


Figure 2.3: Concept of a hollow axis-mounted (HAM) inverter. (a) For an inner-rotor PMSM. (b) For an outer-rotor PMSM.

Cooling concepts

With regard to cooling, IMDs mentioned in literature can be classified according to the used cooling technology and the degree of cooling system integration. Among the used cooling technologies are active cooling systems and passive cooling systems [2]. Active cooling systems use fans or pumps for forced air cooling or liquid cooling, whereas passive cooling systems are based on natural convective air cooling, conduction, and radiation. The list of existing IMDs in Tab. I of [3] shows that most IMDs mentioned in literature employ an active cooling system, i.e. active/forced air cooling or liquid cooling.
Active air cooling is predominantly used in IMDs with axial inverter integration, whereas liquid cooling is predominantly used in IMDs with radial inverter integration. In the following, first air cooling concepts are described. Secondly, liquid cooling concepts are described.

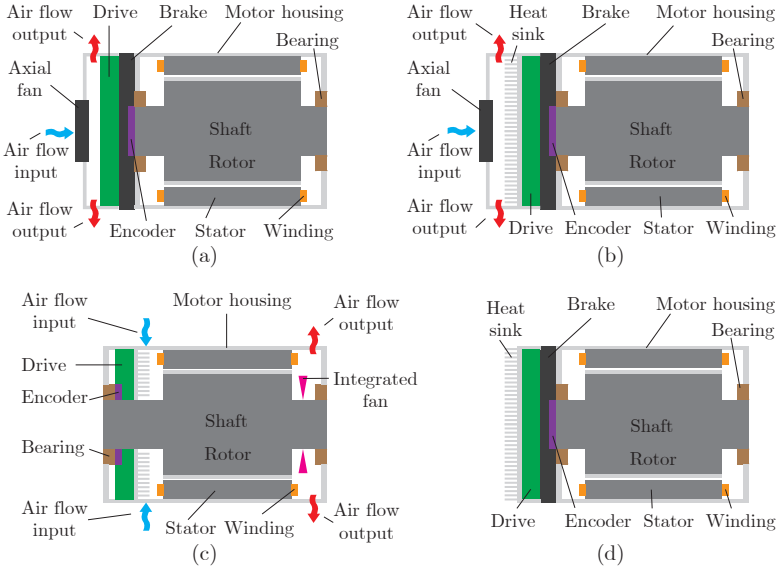


Figure 2.4: Thermo-mechanical integration concepts of air-cooled IMDs [14]. (a) Active cooling with the power electronics (PE) in an open end chamber of the motor housing. (b) Active cooling with the PE in a closed end chamber of the motor housing. (c) Active cooling with the PE inside the motor housing. (d) Passive cooling with the PE inside a closed end chamber of the motor housing.

Fig. 2.4a-c (from [14]) show possible thermo-mechanical integration concepts of (axially integrated) IMDs with active air cooling. These concepts are a selection of concepts suggested in [14] for which prototypes or even commercialised products are known from the literature. References related to these prototypes/products are included in the following description of the different concepts.
In Fig. 2.4a the inverter is located in an end chamber/cap of the motor housing and cooled by the air flow that enters the end cap through an axial fan and leaves the end cap through air slots in radial direction. An IMD prototype based on this concept is presented in [14]. A disadvantage of this concept is that the inverter is exposed to dust and moisture from the outer air.

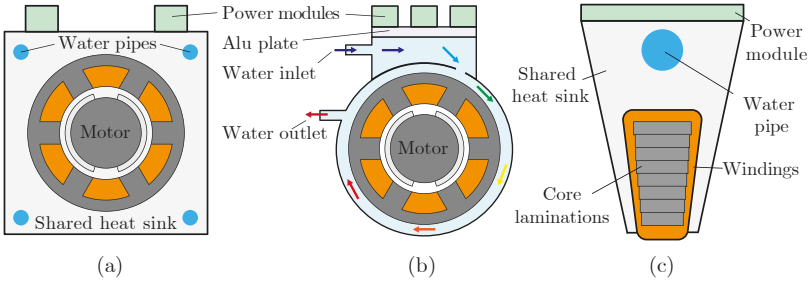


Figure 2.5: Thermo-mechanical integration concepts of liquid-cooled IMDs [7]. (a) Water-cooled thermal design based on a square motor housing [7, 18]. (b) Cylindrical motor housing cooling design [7, 19]. (c) Water-cooled stator-tooth module, multiple of which must be arranged in a circular pattern to form the stator. [7, 20].

This problem is solved with the concept shown in Fig. 2.4b, where the inverter is located in a closed inner end cap formed by a heat sink that is cooled by the fan. A similar concept is used in [15] where also a prototype of the heat sink is presented.
Another concept of active air cooling is shown in Fig. 2.4c, where the inverter is located inside the motor housing, i.e. there is no separation through a break/encoder housing, and the inverter is realised with less PCBs. The motivation of this concept is to increase the IMD power density [14]. However, it must be noted that this change also comes at the cost of less braking functionality as the break was removed. A prototype based on this cooling concept is presented in [10].
In contrast to Fig. 2.4a-c, which show active air cooling concepts, Fig. 2.4d shows a possible passive cooling concept which basically corresponds to the concept from Fig. 2.4b without the fan. The protection capability against dust and moisture is kept but the thermal resistance of the heat sink increases, which limits the suitability of this concept for higher power ratings. A few IMDs using passive cooling systems already exist as commercialised products such as the *ACOPOSmotor* by B&R [16] or the *KSM02* by Bosch Rexroth [17].

Fig. 2.5 shows possible thermo-mechanical integration concepts of liquid-cooled IMDs [7]. The concept shown in Fig. 2.5a is suggested in [18] and consists of a square shaped cross-section of the motor housing

with water pipes in the corners of the housing. The power modules of the inverter are placed on top of the motor housing and close to the water pipes.
Fig. 2.5b shows another liquid-cooled IMD concept, suggested in [19], in which the water flow first cools the power modules mounted on top of the motor and then flows around the motor housing forming a "cooling jacket".
Furthermore, Fig. 2.5c shows one combined stator-inverter module of a so-called circumscribing polygon IMD for axial flux motor drives introduced in [21]. The stator-inverter module in Fig. 2.5c consists of a shared heat sink with a water pipe that cools the power module and the motor winding module at the same time.
Fig. 2.5 only shows a selection of liquid-cooled IMD concepts mentioned in the literature to highlight the basic ideas. Nevertheless, the fact that all concepts from Fig. 2.5 use a shared heat sink for the motor and for the inverter is representative for most liquid-cooled IMDs. This can be explained by the motivation to avoid the extra volume and cost that a second liquid cooling circuit including a second heat exchanger would cause. In contrast to liquid-cooled IMDs, air-cooled IMDs include either one shared cooling system or separate cooling systems for the motor and for the inverter. Indeed, the air-cooled IMD concept from Fig. 2.4c includes a shared cooling system as the air first flows past the inverter and then through the motor. The other concepts from Fig. 2.4a/b/d do not have such shared air flow path, hence the motor requires a separate cooling path, for example a flange connection to a larger machinery housing.

Modularity concepts

With regard to modularity, IMDs mentioned in the literature can be classified as 1) non-modular IMDs, 2) IMDs with a modular inverter, and 3) IMDs with a combined motor-inverter modularity.
Non-modular IMDs are typically combined with the concepts of axially or radially housing-mounted IMDs (AHM & RHM) which consist of a conventional (non-modular) motor and of a conventional inverter whose housings are mounted on top of each other.
IMDs with a modular inverter are typically combined with the concepts of axially or radially stator iron-mounted IMDs (ASM & RSM) in which the modularisation of the inverter favours a compact system design as the inverter modules can be distributed around the stator within the

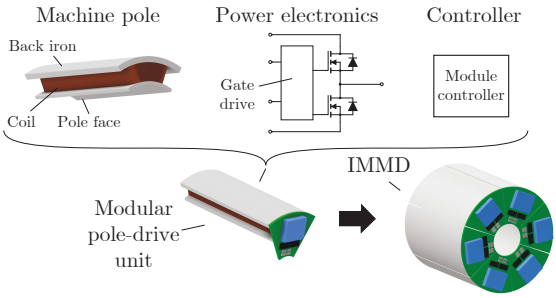


Figure 2.6: Integrated Modular Motor Drive (IMMD) concept introduced in [10]. Also mentioned in [1, 22].

motor housing.
The concept of IMDs with a combined motor-inverter modularity was introduced as Integrated Modular Motor Drive (IMMD) in [10]. The basic IMMD concept is shown in Fig. 2.6.
It must be noted that the IMMD concept, as it was introduced in [10], has a single phase and a single stator tooth per motor-inverter module, which is called modular pole-drive unit in Fig. 2.6. However, the term IMMD, as it is used in the literature, also comprises motor-inverter modules independent of the number of phases and of the number of stator teeth per module. For example, also IMMDs with three-phase modules are considered in [8].
As already mentioned in section 1.1, the potential benefits of IMMDs are improvements with regard to fault-tolerance, manufacturability, cost, and size [1–4].

2.1.2 Concept Used for Modelling and Design

The previous section has shown that a significant number of thermo-mechanical integration concepts for IMDs already exist which are more or less suitable depending on the type of motor. In this section, a thermo-mechanical integration concept suitable for high-torque motors such as the considered project motor (section 1.2) is derived based on considerations regarding the inverter position and the cooling system. These considerations start with a discussion of radial vs. axial integration and of active vs. passive cooling for high-torque motors, resulting

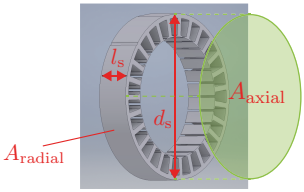


Figure 2.7: Radial surface area $A_{radial} = \pi d_s l_s$ and axial surface area $A_{axial} = \pi(d_s/2)^2$ of the stator of the torque motor *8LTA93* with the stator length $l_s = 5\,cm$ and the stator diameter $d_s = 25\,cm$.

in the choice of axial integration and of passive cooling. Then, two different axially integrated IMD concepts are compared, where the inverter is either integrated on the encoder-side of the motor or on the load-side, resulting in the choice of encoder-side integration. Furthermore, the benefit of a thermal insulation layer between the motor and the inverter is explained and two different concepts for realizing such a thermal insulation layer are compared.

Radial vs. Axial Integration and Active vs. Passive Cooling

As mentioned in section 2.1.1, torque motors usually have a high diameter-to-length ratio and hence usually provide a larger surface for inverter integration on the axial motor surface than on the radial motor surface. This comparison of surface areas is applied to the project motor as shown in Fig. 2.7. As expected, the comparison shows that the axial surface area ($A_{axial} = 491\,cm^2$) is larger than the radial surface area ($A_{radial} = 393\,cm^2$). In addition, integrating a central control unit in a compact (symmetrical) way is more difficult with radial integration than with axial integration where such control unit can be placed in the motor axis. Furthermore, axial integration is suitable for both an inverter design for a given motor (as the IMD design is limited to the redesign of the motor end cap) as well as for a combined motor-inverter design. These considerations lead to the choice of axial integration.
In terms of cooling, passive cooling for the inverter is chosen for two reasons: 1) The considered project motor (section 1.2) has a relatively low power-rating of 1.5 kW and the motor itself is passively cooled (via a mounting flange). Therefore, passive cooling also for the inverter is expected (and is shown in this thesis) to be sufficient for this power

rating. 2) The thermal design and the performance limits of passively cooled IMDs have not yet been investigated, which is therefore done in this thesis.
With regard to the choice between a stator iron-mounted IMD and a housing-mounted IMD, the motivation was first to use the more compact concept, i.e. the concept of axially stator-mounted (ASM) instead of axially housing-mounted (AHM). However, the considerations in the following sections regarding the temperature ratings of electronics and the use of a thermal insulation layer lead to a concept that is similar to an axially housing-mounted IMD.
In summary, the previous considerations lead to the narrowing down of suitable thermo-mechanical integration concepts to a concept combining axial integration and passive cooling. In the following, it is investigated which of the two axial motor sides is more suitable for inverter integration.

Encoder-side vs. Load-side Integration

Fig. 2.8 shows two thermo-mechanical inverter integration concepts, called IMD concepts *C1* and *C2*. Both concepts are based on the same motor which is a passively cooled surface permanent magnet synchronous motor (SPMSM) for high-torque applications such as the considered project motor. The motor is flange-mounted, i.e. the flange contact on the front end cap is attached to an external frame or housing of the load, which is a common mounting type for electrical motors. In concept *C1*, the inverter is integrated into the rear/encoder-sided end cap, whereas in concept *C2*, the inverter is integrated into the front/load-sided end cap. In both concepts, the power electronic part of the inverter is considered to be modular with modules that are arranged around the shaft, whereas the control part is considered to be non-modular and is therefore located on a separate PCB. In both concepts, the IMD housing is closed to achieve a protection rating of IP54 or higher.
The advantage of concept *C1* compared to concept *C2* is that the encoder and the inverter are next to each other, which results in short encoder cables. Also, the available space for the inverter in radial direction between the bearing and the motor housing is larger on the encoder side compared to the load side. This is because the shaft has a larger diameter on the load side due to mechanical stiffness. Another advantage of concept *C1* is that the finned heat sink on the end cap

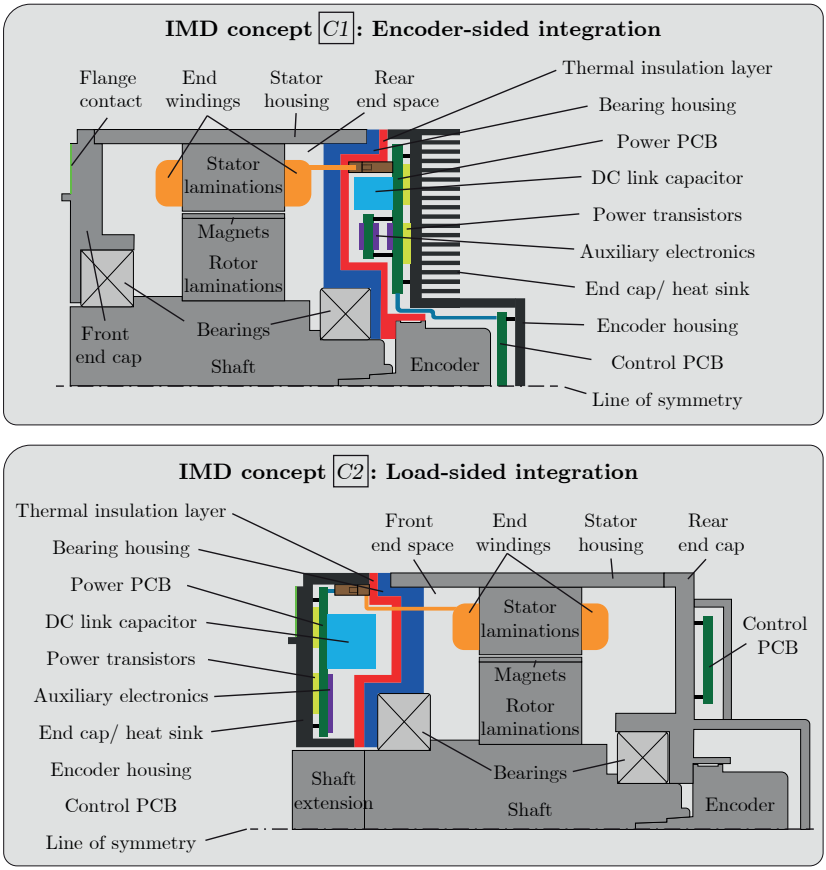


Figure 2.8: Two thermo-mechanical concepts for integrating an inverter into a flange-mounted SPMSM for high-torque applications. The inverter consists of the shown PCBs, the DC link capacitors, the power transistors, and the auxiliary electronics such as gate driver circuits, sensors, and connectors.

does not increase the overall system length as long as the fins are not longer than the encoder housing. Finally, concept *C1* does not require any shaft extension as concept *C2* does. A shaft extension may lead to an increase of the required shaft diameter on the load side for mechanical stiffness.

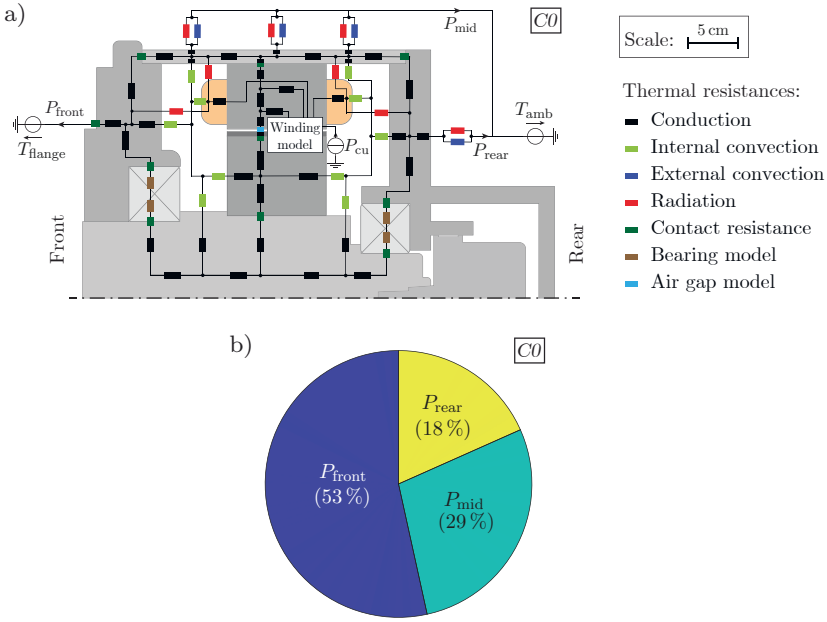


Figure 2.9: a) IMD concept *C0*: An exemplary high-torque, low-speed motor ($P_N = 1.5\,kW$, $n_N = 300\,rpm$, $I_N = 2.86\,A$). The LPTN of *C0* is used to calculate the heat flow distribution shown in Fig. 2.9b and the results shown in Fig. 2.10. The LPTN is based on [23]. b) Distribution of the heat flow in IMD concept *C0* among the front, mid, and rear section under rated load.

Despite the advantages of concept *C1*, there is also a motivation for concept *C2*, which is that the flange contact provides a good thermal connection between the front end cap and the external frame or housing of the load machinery. This external frame or housing typically has a relatively low temperature ($< 70\,°C$) and can therefore be used as an external heat sink. The share of the heat flow through the flange in the total heat flow from the motor to ambient is calculated using IMD concept *C0*, shown in Fig. 2.9a. This concept is an exemplary motor which serves as a best case approximation as no inverter losses are considered. The motor dimensions (see scale in Fig. 2.9a) correspond to that of a typical high-torque, low-speed motor. The heat flow distribu-

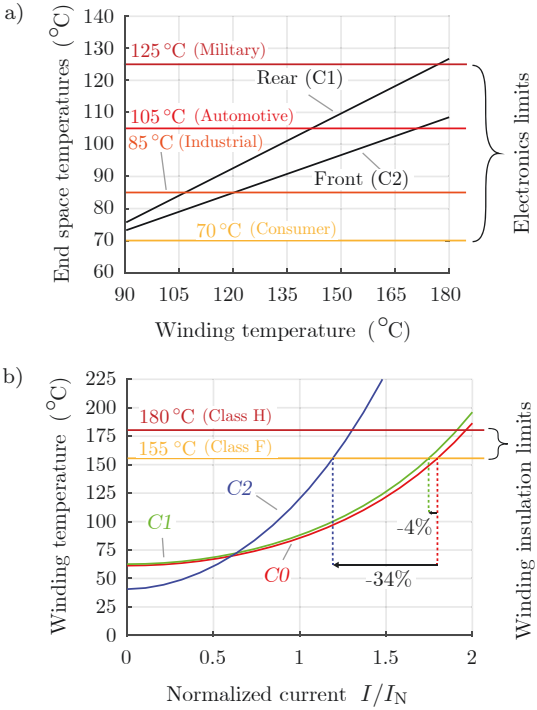


Figure 2.10: a) End space air temperatures for winding temperatures (hot spot) from 90 to 180 °C, compared to the maximum allowed electronics ambient temperature $T_{e,amb,max}$ for different temperature grades. b) Comparison of the concepts *C0*, *C1*, and *C2* regarding the motor winding temperature as a function of the motor current I normalized to the rated motor current I_N. For concepts *C1* and *C2*, an ideal thermal insulation between the motor and the converter is assumed.

tion calculated with the lumped parameter thermal network (LPTN) of *C0* (Fig. 2.9a) is shown in Fig. 2.9b, indicating that the front surface with the flange contact dissipates the main share (53 %) of the motor losses.

Benefit of a Thermal Insulation

The ambient temperature of the inverter $T_{\mathrm{e,amb}}$ must not exceed the maximum allowed temperature of the components' temperature grade $T_{\mathrm{e,amb,max}}$. Common temperature grades of electronic components are 70 °C (commercial), 85 °C (industrial), 105 °C (automotive), and 125 °C (military) [9]. The rotor movement causes the air in the front/rear end space to circulate, which results in a more homogeneous temperature distribution in each end space. Therefore, the ambient temperature of the electronics approximately corresponds to the air temperature in one of the motor end spaces if no thermal insulation is used. The end space air temperature at the front/rear of a typical high-torque, low-speed motor is calculated using the LPTN of concept *C0* (Fig. 2.9a) for winding temperatures from 90 °C to 180 °C. The result given in Fig. 2.10a is compared to $T_{\mathrm{e,amb,max}}$, indicating that the end space air temperature exceeds $T_{\mathrm{e,amb,max}}$ in case of commercial or industrial grade electronics and winding temperatures above 120 °C. Industrial grade components are preferred due to cost and availability considerations. Therefore, to reduce the ambient temperature of the electronics, a thermal insulation is required.
With a thermal insulation, concept *C2* has the disadvantage that a complete thermal isolation of the converter from the motor is not possible without a significant derating of the motor because the motor loss dissipation via the flange is reduced. This is validated in Fig. 2.10b where an ideal thermal insulation (i.e. no power flow from the motor to the converter) is assumed, which leads to a worst case derating of 34 % for concept *C2* vs. only 4 % for concept *C1*. To avoid a large derating, concept *C2* would require the dissipation of both converter losses and motor losses via the flange while thermally insulating the converter from the motor, which is more complex and voluminous. Given this consideration and the previously listed advantages of concept *C1*, *C2* is not further considered in the following.

Selection of an Insulation Concept with regard to Material Limits

A basic insulation concept, called *I1*, is shown in Fig. 2.11a. The concept consists of a single layer of a thermally insulating material between the (rear) motor end space and the converter ambient. The simplified

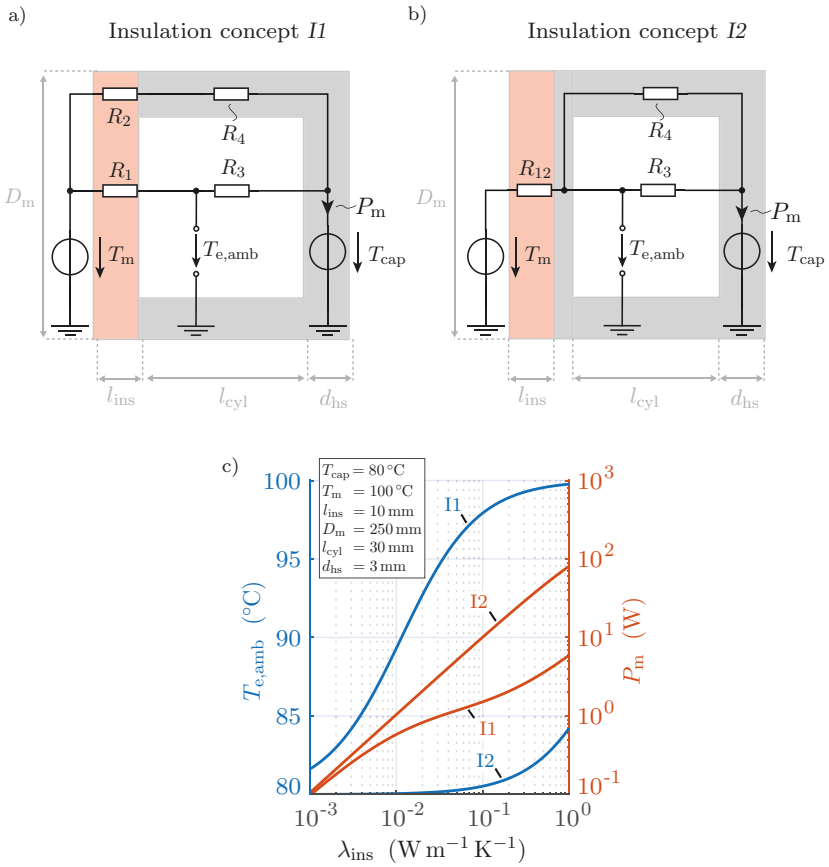


Figure 2.11: a) Insulation concept *I1*: An insulation layer (red) without any additional aluminium layer on top of the insulation layer. b) Insulation concept *I2*: An insulation layer (red) with an additional aluminium layer on top of the insulation layer. c) Effect of the thermal conductivity λ_{ins} of the insulation layer in *I1* & *I2* on the electronics ambient temperature $T_{\mathrm{e,amb}}$ and on the heat flow through the insulation layer P_{m}.

LPTN in Fig. 2.11a assumes a unidirectional heat flow of the motor loss fraction P_{m} from the motor, that is modelled as a constant temper-

ature source T_m, through the insulation layer (red) and the converter ambient (white) towards the right end cap surface (grey). This surface is assumed to be cooled to the temperature $T_\mathrm{cap} < T_\mathrm{m}$ by a finned heat sink (not shown). All thermal resistances R_1-R_4 in Fig. 2.11a are based on conductive heat transfer, i.e. a convective heat transfer through the inner air is neglected. Based on the LPTN in Fig. 2.11a, it can be concluded that the condition $^{R1}/_{R3} \gg 1$ must be fulfilled in order to effectively insulate the converter ambient temperature $T_\mathrm{e,amb}$ from the motor temperature (i.e. to keep $T_\mathrm{e,amb}$ close to T_cap). This results in the condition $^{\lambda_\mathrm{air}}/_{\lambda_\mathrm{ins}} \gg 1$ with the thermal conductivity of air $\lambda_\mathrm{air} \approx 0.03\,\mathrm{W\,m^{-1}\,K^{-1}}$ [24]. Hence, concept *C1* requires so-called superinsulations, i.e. materials with $\lambda_\mathrm{ins} < \lambda_\mathrm{air}$ [24], which might be disadvantageous in terms of costs, availability and mechanical robustness. This is the motivation for the insulation concept shown in Fig. 2.11b, called concept *I2*.

In *I2*, an additional metal layer is added onto the thermal insulation layer. This way, the highly thermally resistive path through the converter air (R_3) is bypassed by a low thermally resistive path (R_4), so that $T_\mathrm{e,amb}$ decreases compared to concept *I1*. This advantage comes at the cost of an increased power flow from the motor to the converter because the additional metal layer decreases the overall thermal resistance between the motor and the end cap. Therefore, *I2* has an advantage over *I1* only as long as the increase in heat flow is negligible or less critical than a smaller thermal conductivity.

These general considerations are validated by an exemplary calculation solving the LPTN-models in Fig. 2.11a & 2.11b for $T_\mathrm{e,amb}$ and P_m as a function of λ_ins for a set of example specifications. The specifications and the results are given in Fig. 2.11c. The results for $T_\mathrm{e,amb}$ show that concept *I1* requires a very low thermal conductivity of $\lambda_\mathrm{ins} < 0.004\,\mathrm{W\,m^{-1}\,K^{-1}}$ to achieve a sufficient temperature insulation for industrial grade components ($T_\mathrm{e,amb} < 85\,^\circ\mathrm{C}$). Using concept *I2*, λ_ins can be increased to $0.1\,\mathrm{W\,m^{-1}\,K^{-1}}$ if the increase in P_m is, for example, limited to 10 W.

Based on these considerations, the thermo-mechanical integration concept selected for the IMD modelling and design is IMD concept *C1* from Fig. 2.8, combined with insulation concept *I2* from Fig. 2.11b.

2.2 Inverter Topologies

In this section, first the state of research on existing inverter topologies for electrical drives is presented. Then, a selection of the most relevant inverter topologies is presented based on an evaluation of the suitability of the inverter topologies for IMDs.

2.2.1 Classification of Inverter Topologies

In this section, the state of research on existing inverter topologies for electrical drives is presented.
Fig. 2.12 shows a classification of voltage source inverter (VSI) topologies from the literature which are suitable for electrical drives.

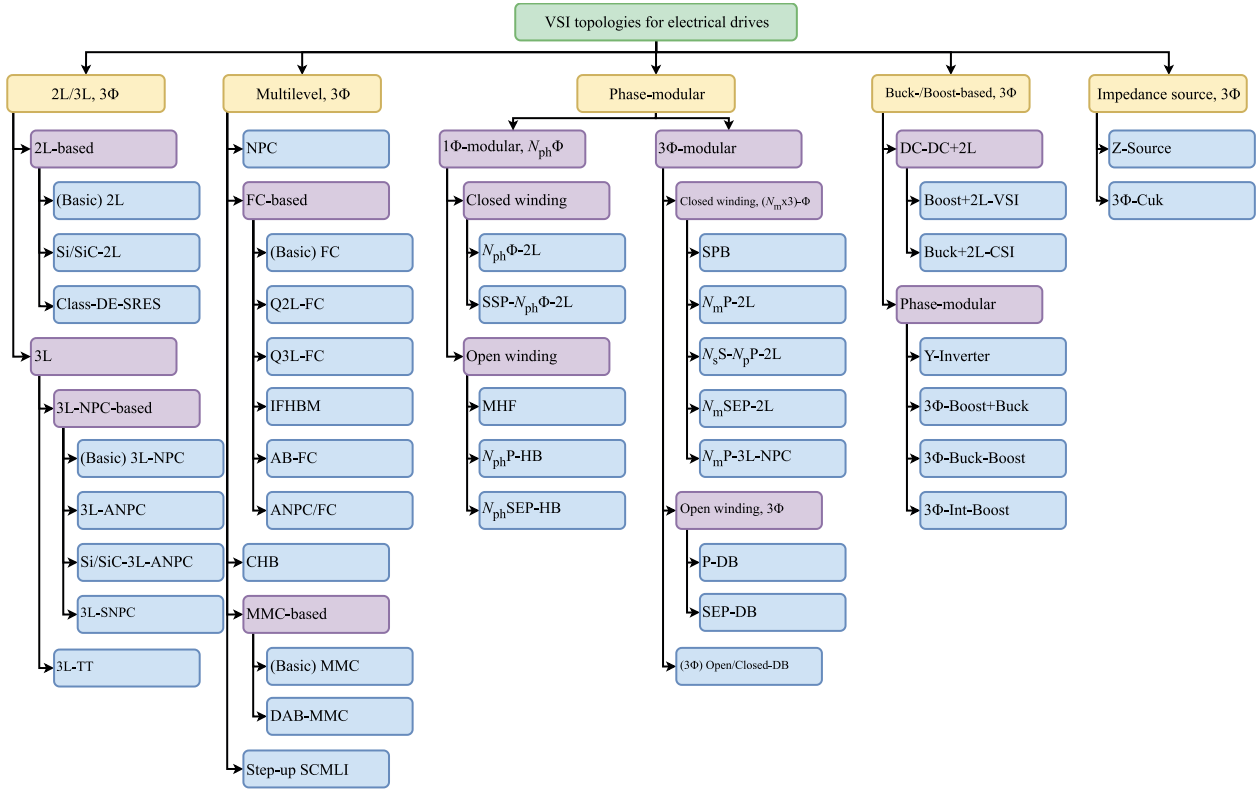


Figure 2.12: Classification of VSI topologies suitable for electrical drives.

Therein, the topologies are classified into five major groups which are 1) 2-level/3-level (2L/3L) topologies, 2) multilevel topologies, 3) phase-modular topologies, 4) buck-/boost-converter based topologies, and 5) impedance source based topologies.
With regard to the number of phases, all topologies shown in Fig. 2.12, except for the phase-modular topologies, are 3-phase (3Φ) topologies. The group of phase-modular topologies contains 3-phase and general N_{ph}-phase topologies.
With regard to the notation of topologies and converters used in this thesis, topologies are referred to by the abbreviations in Fig. 2.12, whereas a converter of a certain topology is referred to as *Top*-C, where *Top* is the considered inverter topology. For example, *SPB-C* designates a stacked polyphase bridge converter.
For each major group of topologies from Fig. 2.12, the topologies that belong to this group are described in the following in terms of their structure, their advantages, and their disadvantages.

2-Level/3-Level Inverter Topologies

This section describes the group of 2-level/3-level 3-phase inverter topologies (2L/3L, 3Φ in Fig. 2.12) which contains the most basic inverter topologies. This group is split into 2L-topologies and 3L-topologies. The 2L-topologies from Fig. 2.12 are shown in Fig. 2.13a-c. Therein, Fig. 2.13a shows the basic 2L-VSI topology. In this thesis, this topology is just referred to as 2L. The 2L topology is the most basic and a widely used topology due to its low complexity, low switch count, and hence low cost.
Fig. 2.13b shows a 2L-based inverter topology that consists of two 2L-C modules connected in parallel, one of which uses Si-IGBTs and the other uses SiC-MOSFETs [25]. In this thesis, this topology is referred to as Si/SiC-2L. The concept of combining conventional Si-IGBTs with WBG devices is called WBG fractional power processing (WFPP) in [25], and an optimisation strategy for the power sharing with this concept is presented in [35]. The motivation of WFPP is to combine the benefits of the low cost of Si-IGBTs with the low switching losses of WBG devices. Thus, for a given power rating, a Si/SiC-2L-C is less expensive and less efficient than a 2L-C that only uses SiC-IGBTs (SiC-2L-C) [25]. A disadvantage of the Si/SiC-2L topology is that the parallel connection of the 2L-C modules lead to circulating currents that produce additional losses. To limit the circulating current, output inductors are required,

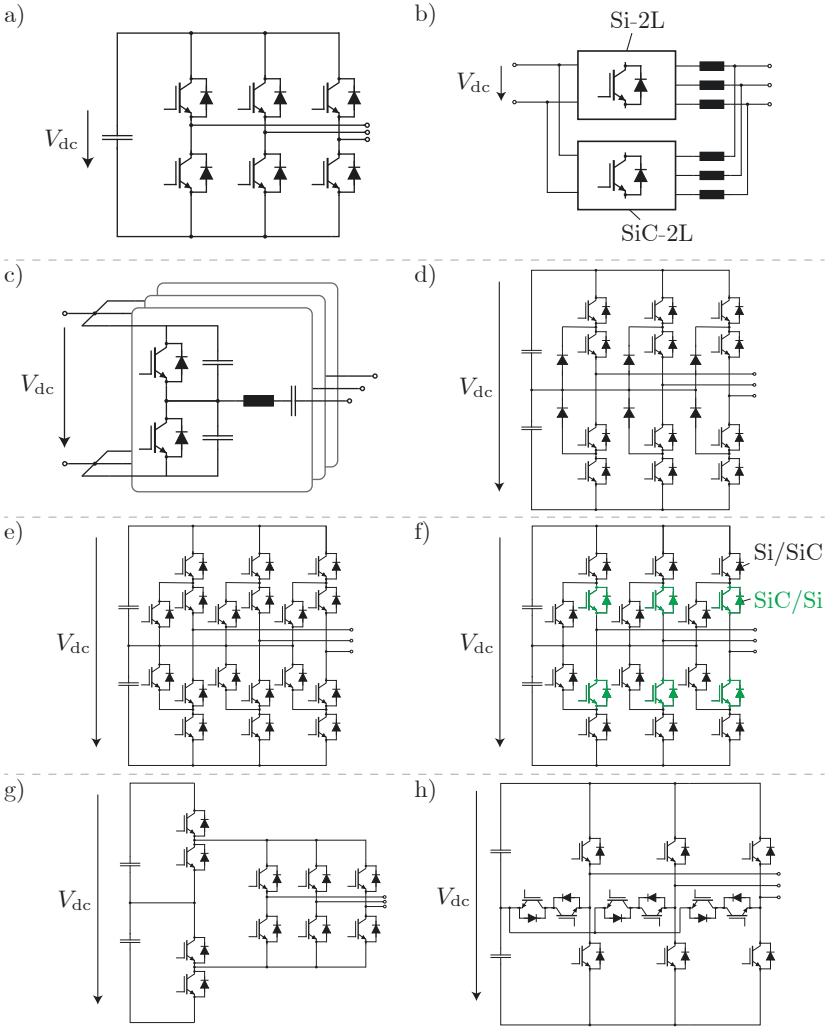


Figure 2.13: 2-/3-level 3-phase VSI topologies. a) (Basic) 2L. b) Si/SiC-2L [25]. c) Class-DE-SRES [26, 27]. d) (Basic) 3L-NPC [28, 29]. e) 3L-ANPC [30]. f) Si/SiC-3L-ANPC [31, 32]. g) 3L-SNPC [33]. h) 3L-TT [34].

as shown in Fig. 2.13b, which increase the system volume.
Fig. 2.13c shows the topology of a class DE series resonant (Class-DE-SRES) inverter [26, 27], also called class DE power amplifier. In general, power amplifiers can provide the same functionality as VSIs but the term power amplifier is more commonly used in the context of audio applications, whereas the term VSI is more commonly used in the context of drive applications. Power amplifiers are classified as class A, B, C, etc., where the class is an indication of the operating principle and efficiency of the amplifier [36]. The Class-DE-SRES topology in Fig. 2.13c combines zero voltage switching (typical for class D amplifiers) with a zero voltage slope during switching (typical for class E amplifiers). This is achieved through so-called shunting capacitors in parallel to the semiconductor devices and an LC series connected resonant tank at the output of each inverter phase-leg, as shown in Fig. 2.13c. Consequently, an advantage of this topology is a relatively high efficiency through low switching losses. A disadvantage of this topology are the additionally required components and the related increase in cost and volume compared to the 2L topology.
The 3L-inverter topologies from Fig. 2.12 are split into topologies that are based on the (basic) 3L-neutral-point-clamped (3L-NPC) topology and into the 3L-T-type topology (3L-TT). Fig. 2.13d shows the (basic) 3L-NPC topology [28, 29]. One phase-leg of this topology consists of four active semiconductor devices (switches) and of two diodes that are connected to the middle potential of the DC link.
Fig. 2.13e shows a modified variant of the 3L-NPC topology, called 3L-active-NPC (3L-ANPC), in which the diodes are replaced by switches [30]. The benefit of this modification in combination with a loss balancing modulation scheme is a more even/balanced loss distribution of the semiconductors compared to the 3L-NPC topology [30]. A more balanced loss distribution leads to a more balanced junction temperature distribution and, as the inverter power rating is limited by the junction temperatures, a higher power rating [30] of the inverter. This comes at the disadvantage of (slightly) higher costs and of a larger complexity of the modulation scheme.
Fig. 2.13f shows a SiC/Si-hybrid variant of the 3L-NPC topology which uses SiC MOSFETs and Si-devices (IGBTs/MOSFETs) within one phase-leg of the inverter [31, 32]. This topology variant is called SiC/Si-3L-ANPC in the following. Two specific sub-variants are suggested and analysed in the literature: 1) In [31], the topology consists

of 2 SiC MOSFETs and of 4 Si devices (IGBTs/MOSFETs) per half bridge, which is here called 2SiC/4Si-3L-ANPC. 2) In [32], another variant with 4 SiC MOSFETs and 2 Si devices per half bridge is analysed, which is here called 4SiC/2Si-3L-ANPC. The benefit of using both SiC MOSFETs and Si-devices in one 3L-ANPC half bridge is a compromise between high efficiency (through the use of SiC MOSFETs that have low switching losses) and low costs (through the use of Si devices) [32].
Fig. 2.13g shows a simplified/sparse 3L-NPC (3L-SNPC) inverter topology [33]. In contrast to the (basic) 3L-NPC topology that has one 3-level half bridge per phase-leg, the 3L-SNPC has a single 3-level stage for all phases which is connected to a 2L-C. Consequently, the advantage of the 3L-SNPC is a lower semiconductor device count and hence lower costs. However, the 3L-SNPC topology also requires a non-standard 3-level modulation scheme as the 3L-SNPC topology has less switching states than the 3L-NPC topology [37]. A GaN/Si-hybrid variant of the 3L-SNPC topology using GaN HEMTs and Si IGBTs is suggested in [38], which again results in a compromise between high efficiency and low costs as was the case for the SiC/Si-3L-ANPC topology.
Fig. 2.13h shows the 3-level T-type (3L-TT) inverter topology [34]. An advantage of the 3L-TT topology compared to the 3L-NPC topology is the lower semiconductor device count: The 3L-TT topology requires 12 switches, whereas the 3L-NPC topology requires 12 switches and 6 diodes. Another advantage of the 3L-TT topology is a lower number of isolated gate signals and hence of isolated gate driver supply circuits: The 3L-TT topology requires 5 isolated gate signals, whereas the 3L-NPC topology requires 10 isolated gate signals [39]. In terms of semiconductor losses, the 3L-TT topology leads to lower conduction losses than the 3L-NPC topology because the current from the positive/negative DC link rail to the output only passes one semiconductor device instead of two. However, a disadvantage of the 3L-TT topology compared to the 3L-NPC topology are higher switching losses because the semiconductor devices between the positive/negative DC link rail have to block the full DC link voltage and have therefore slower switching characteristics [39].

Multilevel Inverter Topologies

This section describes the group of multilevel inverter topologies from Fig. 2.12. As 3-level inverter topologies were already considered in the previously described group, the multilevel inverter topologies in Fig.

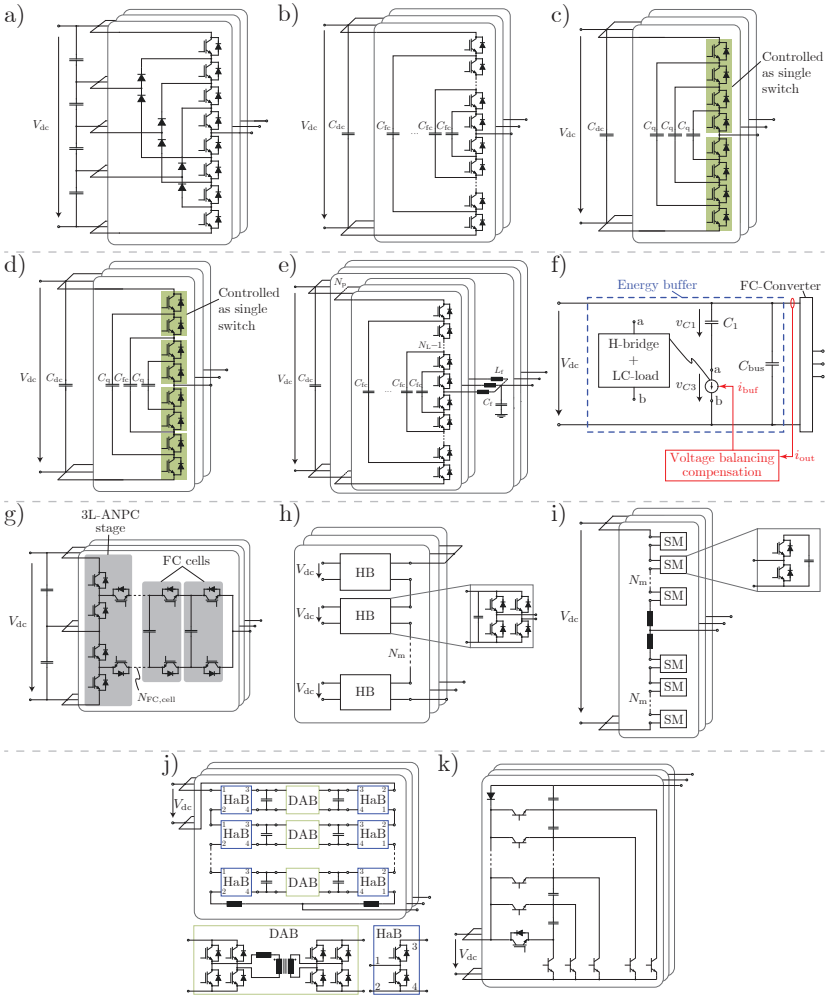


Figure 2.14: Multilevel 3-phase VSI topologies. a) NPC [40]. b) (Basic) FC [41]. c) Q2L-FC [42]. d) Q3L-FC [42]. e) IFHBM [43]. f) AB-FC [44]. g) ANPBC/FC [45]. h) CHB [46]. i) (Basic) MMC [47]. j) DAB-MMC [48]. k) Step-up SCMLI [49].

2.12 are considered with a general number of (output voltage) levels N_L with $N_\mathrm{L} > 3$. The most important multilevel inverter topologies in Fig. 2.12 are the neutral-point-clamped (NPC) topology, the flying capacitor (FC) topology, the cascaded H-bridge (CHB) topology, the modular multilevel converter (MMC) topology, and the switched capacitor multilevel inverter (SCMLI) topology. These topologies as well as modified FC-based and MMC-based topologies from the literature are briefly described in this section. General advantages of multilevel inverters are a low output voltage harmonic distortion and $\mathrm{d}v/\mathrm{d}t$, a low distortion of the input current, a smaller common-mode (CM) voltage leading to reduced wear of the motor bearings, and operability at low switching frequencies [50]. General disadvantages are a high semiconductor device count and a high complexity of the control [34].
One of the earliest multilevel inverter topologies with more than 3 levels is the extension of the 3L-NPC topology to N_L levels [40], here just called NPC topology. This topology is shown in Fig. 2.14a for 5 levels ($N_\mathrm{L} = 5$). A disadvantage of the NPC topology is the relatively high semiconductor device count for a given number of levels.
Fig. 2.14b shows the (basic) flying capacitor (FC) inverter topology [41]. An FC half bridge with N_s semiconductor devices has $N_\mathrm{L} = N_\mathrm{s}/2 + 1$ output voltage levels. The capacitors C_k with $k = 1, 2, \ldots$ are initially charged up to the voltages $kV_\mathrm{dc}/(N_\mathrm{s}/2)$. The output voltage then corresponds to the number of blocking switches on the low side multiplied by $V_\mathrm{dc}/(N_\mathrm{s}/2)$ [41]. The FC topology requires less (semiconductor and passive) devices than the NPC topology for the same number of levels. Furthermore, the FC topology is relatively simple to control [41].
Different modified variants of the FC topology are described in the literature which are shown in Fig. 2.14c-g. Among these, Fig. 2.14c shows the quasi-2-level flying capacitor (Q2L-FC) inverter topology [42] which corresponds to a 5-level FC inverter topology operated as a 2-level topology. This is achieved by controlling each of the two series connections of four switches (green boxes in Fig. 2.14c) as a single switch. A disadvantage of the Q2L-FC topology is the lost capability of producing multiple voltage output levels. However, the Q2L-FC topology also has advantages which are a reduction of the required capacitance, less voltage balancing issues, a reduced $\mathrm{d}v/\mathrm{d}t$, and the ability to connect also fast switching WBG semiconductor devices in series [42].
Fig. 2.14d shows the quasi-3-level flying capacitor (Q3L-FC) inverter topology [42] which corresponds to a 5-level FC inverter topology op-

erated as a 3-level topology. This is achieved by controlling each of the four series connections of two switches (green boxes in Fig. 2.14d) as a single switch. This topology is a compromise between having multiple voltage levels (property of the FC topology) and keeping the control complexity low (property of the Q2L-FC topology) [42].
Fig. 2.14e shows another FC based inverter topology, called integrated filter half bridge module (IFHBM) topology [43]. One half bridge module of the IFHBM topology consists of a N_{L}-level FC half bridge connected to an LC filter (e.g. for $\mathrm{d}v/\mathrm{d}t$- or full sinewave-filtering) at its output. One phase-leg of the IFHMB topology consists of N_{p} of such half bridge modules connected in parallel. Due to the inductors of the integrated LC filters, parallel interleaving of the half bridge modules is possible. The combination of such parallel interleaving, the multiple output levels of the FC topology, and high switching frequencies allows very small LC filter volumes, which is a main benefit of the IFHBM topology [43]. Disadvantages are the particularly large number of semiconductor devices and the associated control complexity.
Fig. 2.14f shows another modified FC based inverter, here called active buffer flying capacitor (AB-FC) topology, in which the DC link/buffer capacitor C_{dc} of the basic FC topology (Fig. 2.14b) is replaced by an active buffer [44]. This concept is theoretically also applicable to other inverter topologies with a single DC link capacitor. The motivation of using an active buffer is to increase the inverter power density by replacing the conventionally used relatively bulky DC link capacitors. As shown in Fig. 2.14f, the active buffer is realised with a single-phase full bridge (H-bridge) converter with an LC load which is connected in series with the capacitor C_1. The full bridge converter is controlled so that the voltage v_{C3} compensates the AC component of v_{C1} in order to keep the DC link voltage V_{dc} constant [44]. Disadvantages of such an active buffer are the higher complexity and the higher costs compared to a (passive) DC link capacitor.
Fig. 2.14g shows the hybrid active neutral-point-clamped/flying capacitor (ANPC/FC) inverter topology [45]. This topology consists of a 3L-ANPC input stage and an FC output stage with $N_{\mathrm{FC,cell}}$ FC cells. For the positive output voltage half wave, the 3L-ANPC stage is switched so that the FC stage inputs are connected to the positive DC link rail and the DC link neutral point. For the negative output voltage half wave, the 3L-ANPC stage is switched so that the FC stage inputs are connected to the DC link neutral point and the negative DC link rail.

Consequently, the number of output voltage levels N_{L} of an ANPC/FC inverter with $N_{\mathrm{FC,cell}}$ FC cells is given by $2N_{\mathrm{FC,cell}} + 1$ [45]. The advantage of this inverter topology is a smaller capacitance requirement and lower switch count compared to the (basic) FC topology [45].
Fig. 2.14h shows the cascaded H-bridge (CHB) inverter topology [46]. This topology consists of N_{m} H-bridge (HB) modules whose outputs are cascaded/connected in series and whose inputs are supplied by separate DC sources. In [46] these sources are provided by an isolation transformer with as many isolated secondary windings as HB modules. The main advantage of the CHB topology is its modularity which enables relatively simple scalability to higher voltage/power ratings, low costs due to economies of scale, and redundancy. A disadvantage of the CHB topology is the requirement of multiple separate DC sources.
Fig. 2.14i shows the modular multilevel converter (MMC) topology [47]. Each phase-leg of the MMC topology consists of two arms that each consists of N_{m} series connected submodules (SM) and an arm inductor. The submodules can have different topologies. The usually used submodule topologies are the half bridge topology shown in Fig. 2.14i or the full bridge/H-bridge topology shown in Fig. 2.14h. In terms of advantages/disadvantages, the MMC topology has the same modularity related advantages as the CHB topology. An advantage that the MMC topology has over the CHB topology is that the MMC topology only requires one DC source. Drawbacks of the MMC topology include the need for relatively large capacitance values of the submodules, the complexity of the control system, and the difficulties related to the design of an efficient and compact auxiliary supply for the control circuits of the submodules. Solutions for these drawbacks are addressed in [51].
Fig. 2.14j shows a modified variant of the MMC topology which is introduced in [48] and in which each submodule of the top arm is connected to one submodule of the bottom arm with a dual active bridge (DAB). The motivation for this modification is to keep the voltage ripple of the submodule capacitors small, even at very low capacitance values [48]. This comes at the cost of more semiconductor devices and passive components which are required for the DABs.
Fig. 2.14k shows the step-up switched capacitor multilevel inverter (step-up SCMLI) topology which is introduced in [49]. The main advantages of this relatively new topology are its low component count and lower costs compared to other multilevel inverter topologies [49].

Phase-Modular Inverter Topologies

This section describes the group of phase-modular inverter topologies from Fig. 2.12. This group can be divided into two subgroups: 1) Single-phase-modular (1Φ-modular) topologies. There, each inverter module is connected to one motor phase winding. 2) 3-phase-modular (3Φ-modular) topologies. There, each inverter module is connected to three motor phase windings. Both 1Φ-modular and 3Φ-modular inverter topologies can be further divided into inverter topologies that are either suited for 1) closed motor windings or for 2) open motor windings. The former are motor windings in which the phase windings are connected on one end to form one or multiple star points. The latter are motor windings in which both ends of the phase windings are connected to the inverter.
The relation between the number of phases N_{ph}, i.e. the number of motor phase windings, and the number of inverter modules N_{m} is given by: 1) $\{N_{\mathrm{ph}} = N_{\mathrm{m}},\ N_{\mathrm{m}} = 1, 2, \ldots\}$ for 1Φ-modular inverter topologies. 2) $\{N_{\mathrm{ph}} = 3 \cdot N_{\mathrm{m}},\ N_{\mathrm{m}} = 1, 2, \ldots\}$ for 3Φ-modular inverter topologies that are suited for closed motor windings. 3) $\{N_{\mathrm{ph}} = 3,\ N_{\mathrm{m}} = 2\}$ for 3Φ-modular inverter topologies that are suited for open motor windings.
All phase-modular inverter topologies share the advantage of modularity which is related to lower costs (through economies of scale) and to a potentially higher redundancy.

The 1Φ-modular inverter topologies from Fig. 2.12 are shown in Fig. 2.15. Thereof, the topologies suited for closed motor windings are shown in Fig. 2.15a-b, and the topologies suited for open motor windings are shown in Fig. 2.15c-e.
Fig. 2.15a shows the N_{ph}Φ-2L inverter topology which results from a generalisation of the (3-phase) 2L topology to a general number of N_{ph} phases. The advantages of the N_{ph}Φ-2L topology are, as already for the case of $N_{\mathrm{ph}} = 3$, its low complexity and low costs. Furthermore, due to its modular structure given by half bridge modules, the topology can be used in IMMDs. For example, the authors of [10] present an IMMD design that is based on a 5Φ-2L inverter.
A modified variant of the N_{ph}Φ-2L topology with an additional half bridge for a switched star point (SSP) is shown in Fig. 2.15b. This topology, which is here called SSP-N_{ph}Φ-2L, corresponds to a generalisation of the four-leg inverter [52] for 3-phase motors to a general num-

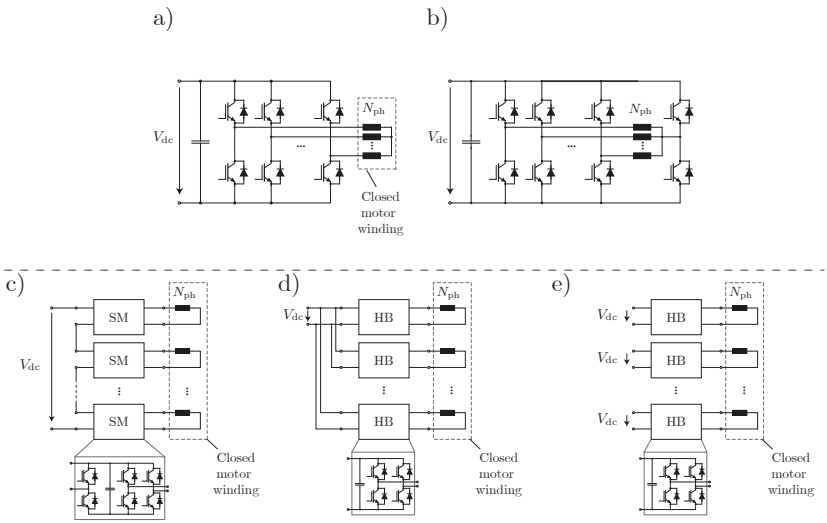


Figure 2.15: Single-phase-modular N_{ph}-phase VSI topologies. a) $N_{ph}\Phi$-2L, given in [10] for $N_{ph} = 5$. b) SSP-$N_{ph}\Phi$-2L, given in [52] for $N_{ph} = 3$. c) MHF [53]. d) N_{ph}P-HB, given in [54] for $N_{ph} = 3$. e) N_{ph}SEP-HB, given in [54] for $N_{ph} = 3$.

ber of N_{ph} phases. The advantage of the four-leg inverter is its fault-tolerance: The four-leg inverter provides a single-phase open-circuit and a single-switch open-circuit fault tolerance [3].

Among the inverter topologies suited for an open motor winding, Fig. 2.15c shows the modular high-frequency (MHF) converter topology [53]. This topology consists of N_m series connected switching modules (SM) that share one DC source. There, each SM consists of a step-up DC-DC converter and an H-bridge. The benefit of the step-up DC-DC converter is to keep the capacitors in the modules small by compensating the single-phase power fluctuation in each module [55].

A similar inverter topology, here called N_{ph}P-HB, is shown in Fig. 2.15d, in which the switching modules are half bridge (HB) modules that are connected in parallel to the DC source. This topology corresponds to a generalisation of the so-called six-leg inverter topology with 3 phases, which is introduced in Fig. 4 of [54], to a general number of N_{ph} phases. As for the four-leg inverter, the advantage of the six-leg

inverter is its fault-tolerance: The six-leg inverter topology has a motor short-circuit and a single-switch open-circuit fault tolerance [3]. The fault tolerance can be further increased through the use of triodes for alternating current (TRIACs) [3, 56].
If the inputs of the HB modules in the N_{ph}P-HB topology are not connected in parallel but are fed by separate DC sources, the topology shown in Fig. 2.15e results. This topology, which is here called N_{ph}SEP-HB, is a generalisation of the so-called three single-phase inverter topology introduced in Fig. 1 of [54] to a general number of N_{ph} phases. On the one hand, the separate DC sources are an advantage because they provide a DC link capacitor fault tolerance. On the other hand, they are also a disadvantage with regard to a higher component count and thus with regard to costs due to the separate DC sources.

The 3Φ-modular inverter topologies from Fig. 2.12 are shown in Fig. 2.16. Thereof, the topologies suited for a closed motor winding are shown in Fig. 2.16a-e and the topologies suited for an open motor winding are shown in Fig. 2.16f-h.
Fig. 2.16a shows the stacked polyphase bridge (SPB) inverter topology. The introduction of this topology is claimed by the authors of [55] (2013) and [8] (2015). In addition, this topology is patented in [57] by the author of [8]. The SPB topology consists of N_{m} series connected 2L-C modules which are also called SPB-modules in this thesis. Each of these SPB-modules is connected to a 3-phase motor winding of a multi star point motor. The advantages of the SPB topology are the following: 1) Low-voltage semiconductor devices can be used. For the same chip cost, the total $R_{\mathrm{ds,on}}$ of a series connection of low-voltage semiconductor devices is potentially lower than the $R_{\mathrm{ds,on}}$ of a single high voltage semiconductor device [42], which leads to lower conduction losses at the given cost. This was shown in [42] based on a cost study of 100 V/150 V/200 V/600 V SiC MOSFETs . 2) The $\mathrm{d}v/\mathrm{d}t$ on the motor winding insulation is reduced, which extends the motor lifespan [8] or reduces the required $\mathrm{d}v/\mathrm{d}t$-filter volume. 3) The instantaneous 3-phase power transfer is constant and does not fluctuate like the single-phase power transfer in the MHF topology (Fig. 2.15c). Therefore, the SPB topology does not require any DC-DC conversion stage to limit the DC link voltage ripple. However, a disadvantage of the SPB topology is that it requires DC link voltage balancing due to the series connection of switching modules.

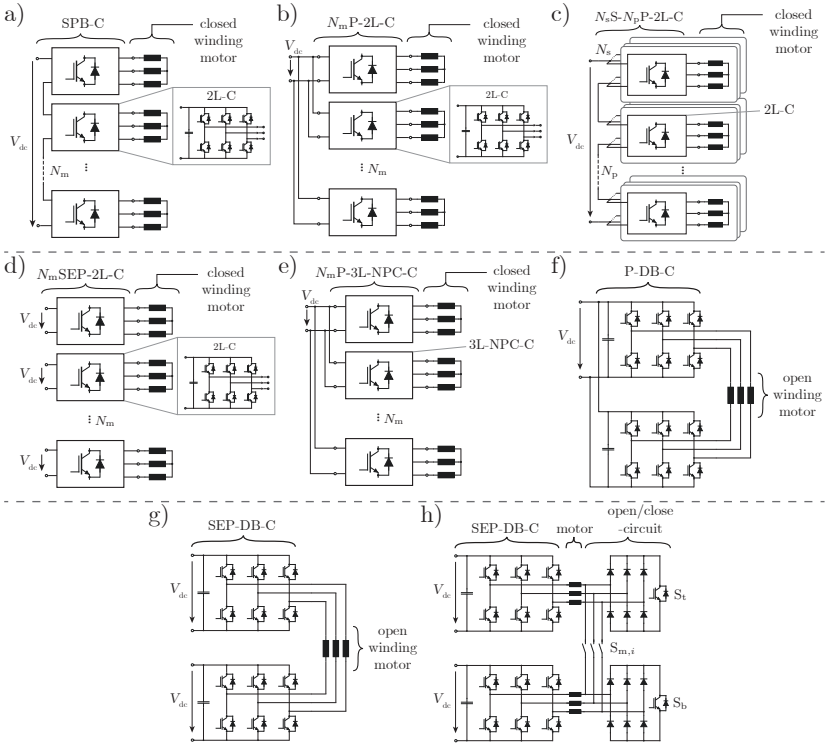


Figure 2.16: 3-phase-modular VSI topologies. a) SPB [8, 55, 57]. b) N_mP-2L [13, 58]. c) N_sS-N_pP-2L, given in [59] for $N_s = N_p = 2$. d) N_mSEP-2L [60]. e) N_mP-3L-NPC, given in [59] for $N_m = 2$. f) P-DB [54, 61, 62]. g) SEP-DB [3, 54, 63]. h) Open/Closed-DB [64].

Fig. 2.16b shows a similar inverter topology, here called N_mP-2L, in which the 2L-C modules are connected in parallel. This topology is part of the patent [13] and corresponds to a generalisation of the dual-inverter introduced in [58] to a general number of N_m modules. The advantages of the N_mP-2L topology are 1) that it does not require any voltage balancing and 2) that gate signal interleaving can be used to reduce the DC link voltage ripple. The disadvantages of this topology are: 1) For the same DC link voltage, the N_mP-2L topology cannot employ the same low-voltage semiconductor devices with low $R_{ds,on}$ as

the SPB topology, which leads to higher conduction losses. 2) The $^{\mathrm{d}v}/_{\mathrm{d}t}$ on the motor windings is higher, which lowers the motor lifespan or requires a larger $^{\mathrm{d}v}/_{\mathrm{d}t}$-filter.
Fig. 2.16c shows the N_sS-N_pP-2L topology, in which the 2L-C modules are series- and parallel-connected with N_s modules in series and N_p modules in parallel. This topology is a generalisation of the 2L 2-series 2-parallel VSI topology from [59] to general numbers for N_s and N_p. In terms of advantages/disadvantages, this topology is a compromise between the SPB topology and the N_mP-2L topology.
Fig. 2.16d shows the N_mSEP-2L inverter topology, in which the 2L-C modules have separate DC link sources. This topology is introduced in [60]. Therein, the separate DC sources are realised with separate rectifiers that are fed by a transformer with multiple three-phase secondary windings. As was the case for the N_phSEP-HB topology (Fig. 2.15e), the advantage of separate DC sources is a DC link capacitor fault tolerance which comes at the cost of a higher component count for the DC front end.
The inverter topologies in Fig. 2.16a-d have 2L-C modules as switching modules. However, also other 3-phase inverter topologies can be used as a switching module. For example, a parallel connection of two 3L-NPC-C modules is suggested in [59]. This topology, generalised to N_m switching modules, is shown in Fig. 2.16e and is here called N_mP-3L-NPC topology. With this topology, gate signal interleaving and multiple output voltage levels can be achieved at the cost of a relatively high component count.
The previously described topologies from Fig. 2.16a-e can have $N_\mathrm{m} = 1, 2, \ldots$ inverter modules and are suited for $(3 \cdot N_\mathrm{m})$-phase closed motor windings. In the following, the inverter topologies shown in Fig. 2.16f-h are described which have two inverter modules ($N_\mathrm{m} = 2$) and are suited for 3-phase open motor windings.
Fig. 2.16f shows the double bridge topology with parallel-connected DC link capacitors (P-DB) [54, 61, 62]. An advantage of this topology is that it requires only half the DC supply voltage that is required by the (basic) 2L topology to generate the same motor phase voltages [62]. Therefore, the P-DB topology is particularly suitable for motor drives that are supplied by a fuel cell whose output voltage can fluctuate significantly depending on the load [62].
Fig. 2.16g shows a similar inverter topology, here called SEP-DB, in which the front ends of the two inverter modules are supplied by sepa-

rate isolated DC sources [3, 54, 63]. The advantage of the two isolated DC link capacitors is that no zero-sequence current control is required [3, 54]. Yet, separate DC sources are likely to cause higher costs compared to a single source due to a higher component count.
Fig. 2.16h shows a hybrid open/closed double bridge (Open/Closed-DB) inverter topology that is introduced and patented in [64]. This topology consists of a SEP-DB-C, a motor with two 3-phase windings, and an open/close-circuit with a top switch S_t, a bottom switch S_b, and middle switches $S_{m,i}$ with $i = 1, 2, 3$. In a first operating mode (S_t & S_b open, $S_{m,i}$ closed) the motor winding is an open winding and the drive system (inverter + motor) is the same as in Fig. 2.16g. In a second operating mode (S_t & S_b closed, $S_{m,i}$ open) the motor winding is a closed winding and the drive system (inverter + motor) is the same as in Fig. 2.16d with $N_m = 2$. The advantage of the Open/Closed-DB topology is twofold: 1) The topology allows to improve the motor efficiency depending on the operating point by changing the winding configuration [64]. 2) The inverter can continue in part load operation even if one inverter module fails [64]. These features come at the cost and volume of the added open/close-circuit.

Buck-/Boost-based Inverter Topologies

This section describes the group of buck/boost-based 3-phase inverter topologies from Fig. 2.12. This group of topologies can be divided into two groups: 1) Inverter topologies that consist of a buck/boost DC-DC converter connected to a 2L-C. 2) Phase-modular buck/boost-based inverter topologies.
The topologies of the first group (DC-DC + 2L) are shown in Fig. 2.17a-b. Therein, Fig. 2.17a shows the Boost+2L-VSI topology which consists of a boost converter stage and a 2L-VSI [43, 65]. As is the case for the P-DB topology (Fig. 2.16f), the Boost+2L-VSI topology is particularly suitable for motor drives that are powered by DC sources with a fluctuating source voltage such as fuel cells [62, 67]. However, the Boost+2L-VSI topology leads to a worse power density/efficiency than the P-DB topology because the P-DB topology results in 50 % lower losses and volume compared to the Boost+2L-VSI topology [62].
Fig. 2.17b shows the Buck+2L-CSI topology which consists of a buck converter stage and a 2-level current source inverter (2L-CSI) [43, 66]. CSIs are suggested as a promising candidate for IMDs in [4], which is

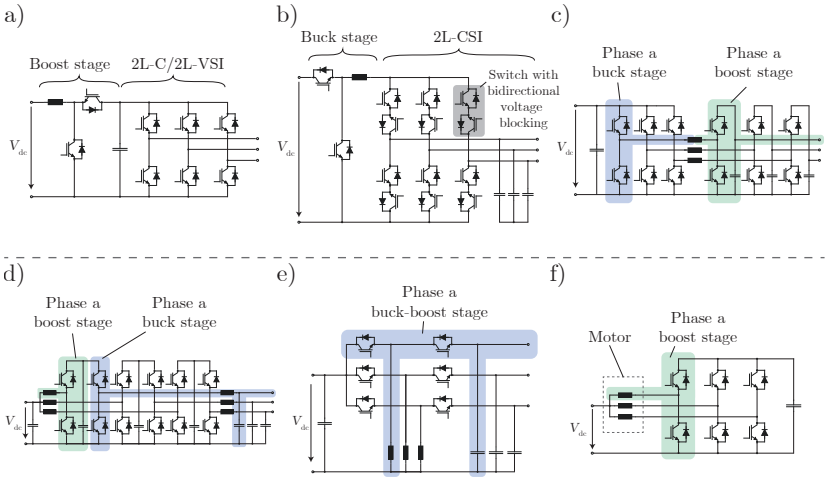


Figure 2.17: Buck-/boost-based 3-phase VSI topologies. a) Boost+2L [43, 65]. b) Buck+2L [43, 66]. c) Y-Inverter [43, 66, 67]. d) 3Φ-Boost+Buck [66]. e) 3Φ-Buck-Boost [66]. f) 3Φ-Int-Boost [43, 68].

based on the following advantages of CSIs given in [4]: 1) High switching frequencies, that are achievable with WGB devices, enable a small DC link inductor and small output capacitors. 2) CSIs provide nearly sinusoidal output voltages and motor currents, which eliminates the need for an additional $^{dv}/_{dt}$-filter. 3) CSIs cause low EMI. 4) CSIs have an improved high-temperature capability compared to VSIs that use electrolytic or film DC link capacitors. 5) CSIs have a higher tolerance against PM machine faults due to the DC link inductor which enables a smaller $^{di}/_{dt}$ and thus a longer detection time of fault currents. However, there are also significant disadvantages of CSIs: 1) CSIs with a high switching frequency require WBG devices with bidirectional voltage blocking capability which are not available on the market [4]. Therefore such devices would have to be realised with two conventional WBG devices (SiC MOSETs/GaN HEMTs) connected in opposite direction as shown in Fig. 2.17b. 2) In addition, a buck converter stage is required to make a CSI compatible with standard voltage sources (grid+rectifier/battery/fuel cell/solar cell), which adds volume and cost

compared to a 2L-VSI [4].
The phase-modular buck-/boost-based inverter topologies are shown in Fig. 2.17c-f. Thereof, Fig. 2.17c shows the Y-Inverter topology [43, 66, 67]. For each phase this topology corresponds to the combination of a buck converter stage and a boost converter stage. The advantages of this topology are the following [66]: 1) A Y-Inverter has almost sinusoidal output voltages and currents due to the integrated LC-filter. 2) The buck-/boost-operation allows for a wide input/output range. 3) The Y-Inverter can be operated with zero voltage switching (ZVS), which enables a high power density. These advantages come at the cost of a higher component count compared to a 2L-C.
If the order of the buck/boost stages of the Y-Inverter is reversed, the 3Φ-Boost+Buck inverter topology results which is shown in Fig. 2.17d [66]. This change in the order of the buck/boost stages does not change the inverter functionality but only results in a higher component count because the buck/boost stages cannot share a common inductor. Therefore, the Y-Inverter is the preferred topology compared to the 3Φ-Boost+Buck topology.
Fig. 2.17e shows another phase-modular inverter topology, here called 3Φ-Buck-Boost topology, which consists of a buck-boost module for each phase. This topology has a low component count but leads to a relatively high component stress and is therefore only suitable for low power applications [66].
An even lower component count is achieved by the inverter topology shown in Fig. 2.17f, called 3-phase inverter-integrated DC-DC boost topology (3Φ-Int-Boost) [43, 68]. The advantage of this inverter topology is that the motor windings are used as boost inductors, so that no additional boost inductors are required. However, this inverter topology requires access to the motor star point and a specific motor design [43].

Impedance Source based Inverter Topologies

This section describes the group of impedance source based 3-phase inverter topologies from Fig. 2.12. These topologies are given by the Z-Source inverter topology and by the three-phase Cuk inverter topology which are shown in Fig. 2.18. Both topologies consist of a DC voltage source, an impedance network (Z-source/Cuk-circuit), and a 2L-C. There, the impedance network provides the inverter with the characteristics of a buck-boost converter. As already mentioned in the previous

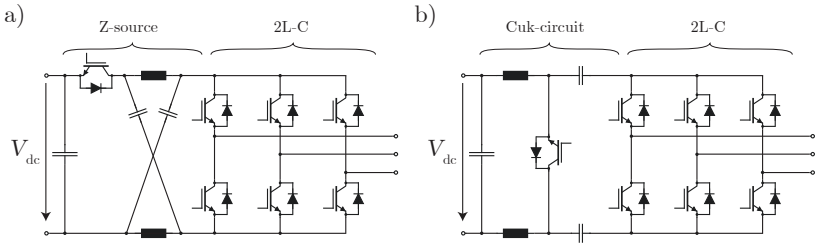


Figure 2.18: Impedance source based 3-phase VSI topologies. a) Z-Source [43]. b) 3Φ-Cuk [43].

section, this feature is useful for variable DC voltage sources like renewable energy sources (fuel-cells or photovoltaics). The disadvantages of impedance source based inverter topologies are that they typically result in high component stress, high complexity, and relatively low performance [43]. Nevertheless, these topologies are mentioned here to give a comprehensive overview of inverter topologies.

2.2.2 Topologies Selected for Modelling and Design

From the large number of inverter topologies presented in the previous section, the five most promising topologies for an IMD based on the considered project motor (section 1.2) are selected in this section. Therefore, in a first step of the topology selection, a preselection of promising topologies is determined based on the following criteria:

- *Criterion C1:* The 2L inverter topology should be included in the selection as a reference concept which is cost-effective and widely used in the industry.
- *Criterion C2:* The most promising 3L inverter topology/topologies should be included in the selection as they combine the benefits of multilevel inverters and still a relatively low amount of semiconductor devices.
- *Criterion C3:* Modular topologies are preferred over non-modular topologies due to the benefits of modularity which are lower costs due to economies of scale and a potentially higher redundancy.

- *Criterion C4:* Phase-modular inverter topologies are preferred over modular multilevel inverter topologies because the former rather allows for a combined motor-inverter modularisation than the latter.

- *Criterion C5:* The selected inverter topologies must be suitable for a PFC rectifier at the inverter front end. This leads to two subcriteria: 1) The inverter topologies must have one single voltage source. 2) As the PFC rectifier output voltage is controlled, an additional power converter stage that compensates for any DC voltage fluctuations is not necessary. Therefore, inverter topologies with a single power conversion stage are preferred over topologies with multiple power conversion stages, such as buck-/boost-based and impedance source based inverter topologies.

Applying these criteria to the inverter topologies presented in the previous section (Fig. 2.12) results in the following preselection of nine inverter topologies: 1) 2L, 2) 3L-NPC, 3) 3L-TT, 4) $N_{\mathrm{ph}}\Phi$-2L, 5) MHF, 6) N_{ph}P-HB, 7) SPB, 8) N_{m}P-2L, 9) N_{s}S-N_{p}P-2L.
So far, this preselection of inverter topologies is independent of any specific slot-pole-phase configuration of the driven motor, i.e. independent of the parameters $\{N, p, m\}$, where N is the number of stator slots, p is the pole pair number, and m is the number of phases per *base winding* (explained later in section 2.4). In a second step of the topology selection, the preselection of nine inverter topologies is further narrowed down based on the following two assumptions on the considered motors: 1) For the slot-pole combination $\{N, p\}$, the slot-pole combination of the project motor (Tab. 1.1) is assumed, i.e. $\{N, p\} = \{27, 12\}$. 2) For the type of winding, double-layer tooth-coil windings are assumed (which are described later in section 2.4). With these assumptions, the following additional criteria are applied to the preselection of inverter topologies:

- *Criterion C6:* Inverter topologies with a lower number of switches are preferred over topologies with a higher number of switches. The motivation of this criterion is to focus on cost-efficiency and low complexity, which benefits a large scale production for industry applications.

- *Criterion C7:* Inverter topologies suitable for a motor winding with a higher winding factor are preferred over inverter topologies

suitable for a motor winding with a lower winding factor. The winding factor determines the effective number of stator winding turns which are coupled with the rotor flux, as will be explained more in detail in section 3.6.3. A higher winding factor has a positive impact on the drive system in terms of efficiency/power density as will be shown in section 4.1.

To illustrate the application of the criteria C6 & C7, Tab. 2.2 shows a comparison of feasible inverter-winding-combinations with regard to the number of switches N_{sw} and the winding factor k_{w}. In addition to N_{sw} and k_{w}, Tab. 2.2 also indicates the motor stage (defined later in section 2.4.2), the number of phases per base winding m, the phase number N_{ph}, and the winding configuration (open/closed) for each inverter-winding-combination. Based on Tab. 2.2, the criterion C6 is applied by only selecting the inverter topologies with $N_{\mathrm{sw}} \leq 18$, resulting in the topologies in the first seven rows of Tab. 2.2. To further narrow down the selection to five topologies, the criterion C7 is applied by limiting the selection of modular topologies to the SPB topology and the N_{m}P-2L topology which enable a higher winding factor ($k_{\mathrm{w}} = 0.985$) compared to the N_{ph}P-HB topology and the MHF topology ($k_{\mathrm{w}} = 0.945$).
Overall, the second step of the topology selection based on the criteria C6 & C7 results in the following inverter topologies: 1) 2L, 2) 3L-NPC, 3) 3L-TT, 4) SPB, 5) N_{m}P-2L. These inverter topologies are selected for the modelling of IMDs in chapter 3 and for the optimal design of IMDs in chapter 4. There, the SPB topology with N_{m} modules is also referred to as 2L-N_{m}M-ser and the N_{m}P-2L topology as 2L-N_{m}M-par. An overview of the selected topologies is shown in Fig. 2.19.

Motor stage	m	N_{ph}	Winding	k_{w}	Inverter topology	N_{sw}
MS1	3	3	closed	0.945	2L	6
MS1	3	3	closed	0.945	3L-NPC	12
MS1	3	3	closed	0.945	3L-TT	12
MS2	3	3	open	0.945	N_{ph}P-HB	12
MS2	3	3	open	0.945	MHF	18
MS2	3	9	closed	0.945	N_{m}P-2L	18
MS2	3	9	closed	0.945	SPB	18
MS2	9	9	closed	0.985	N_{m}P-2L	18
MS2	9	9	closed	0.985	SPB	18
MS2	9	9	open	0.985	N_{ph}P-HB	36
MS2	9	9	open	0.985	MHF	54
MS2	9	27	closed	0.985	N_{m}P-2L	54
MS2	9	27	closed	0.985	SPB	54
MS2	9	27	open	0.985	N_{ph}P-HB	108
MS2	9	27	open	0.985	MHF	162

Table 2.2: Comparison of inverter-winding-combinations based on a preselection of inverter topologies and feasible double-sided tooth-coil windings with $\{N, p\} = \{27, 12\}$.

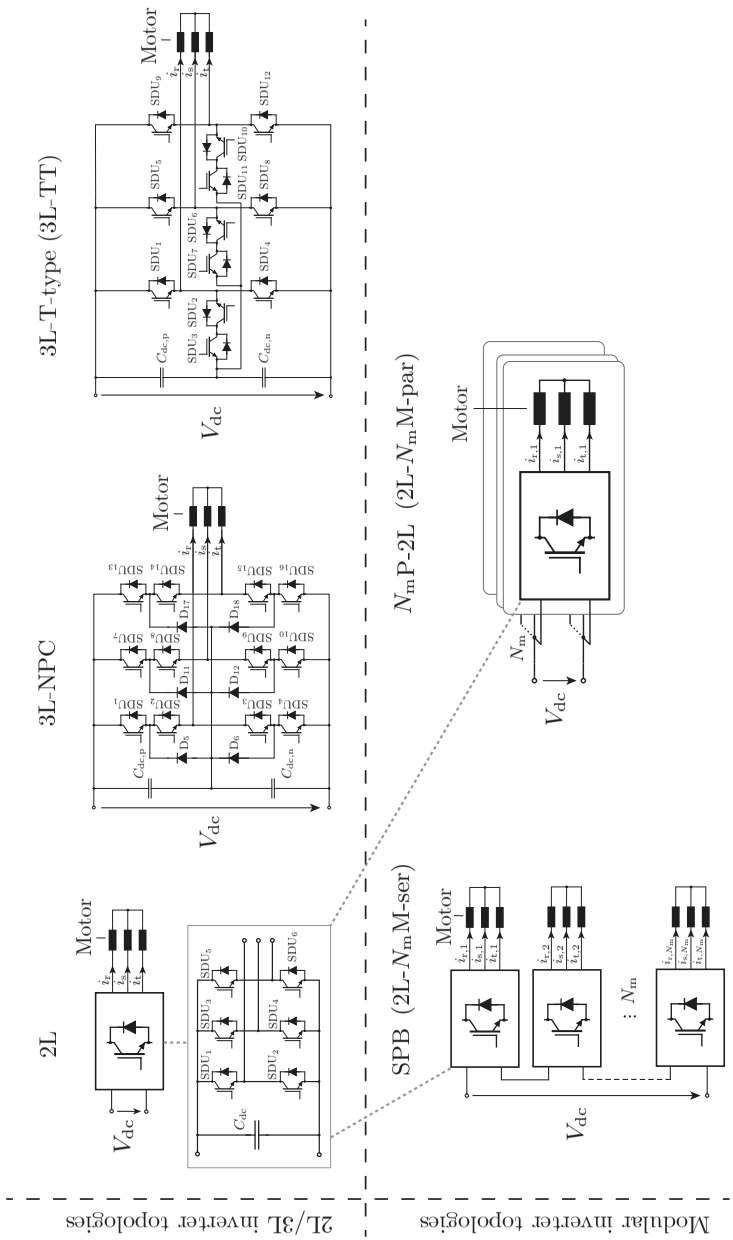


Figure 2.19: Inverter topologies selected for the IMD modelling in chapter 3 and for the optimal design in chapter 4.

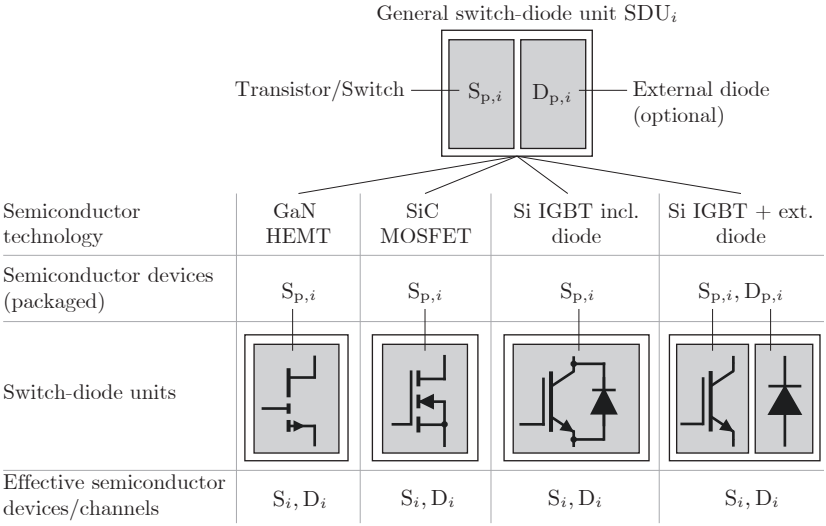


Figure 2.20: Considered types of *switch-diode units* (SDUs).

The transistors of the topologies in Fig. 2.19 are IGBTs. However, also other semiconductor device technologies are considered in this thesis. For this purpose, a generic *switch-diode unit* (SDU) is introduced as an abstract object for different semiconductor device configurations. In general, one SDU consists of one (packaged/discrete) transistor/switch (S_p) and optionally one (packaged/discrete) anti-parallel diode (D_p). The considered specific types of SDUs are shown in Fig. 2.20 and are given by 1) a GaN HEMT, 2) a SiC MOSFET, 3) a Si-IGBT with an anti-parallel diode in the same package, and 4) a Si-IGBT with an anti-parallel diode in a separate package. Furthermore, two so-called *effective semiconductor devices* are defined for each SDU: An *effective transistor/switch* (S) and an *effective diode* (D) which are defined as the forward conducting channel and the reverse conducting channel of an SDU, respectively. The motivation for the definition of SDUs and of effective semiconductor devices is that they allow for the development of generic models for the inverter. The semiconductor conduction/switching loss model and the thermal inverter model, which are presented in chapter 3, are such generic models.

2.3 PWM Schemes

In this section, first a classification of pulse-width modulation (PWM) schemes resulting from a literature research is given. Then, the PWM schemes that are selected for the IMD modelling in chapter 3 and for the optimal design of IMDs in chapter 4 are described.

2.3.1 Classification of PWM Schemes

Fig. 2.21 shows a classification of PWM schemes based on three main groups of PWM schemes which are commonly distinguished in the literature [69]: Carrier-based PWM, space vector modulation (SVM), and programmed PWM. The rows of Fig. 2.21 contain criteria in which the PWM schemes differ between these groups (primarily) and within each group. As the criteria (voltage signal domain, switching time determination, etc.) already indicate, the main difference of carrier-based PWM, SVM, and programmed PWM is related to the PWM implementation but not necessarily to the generated output voltage.
In the following, first the classification of PWM schemes according to the criteria in Fig. 2.21 is explained with a focus on the differences and the different types of carrier-based PWM, SVM, and programmed PWM. Then, the equivalence of SVM and regularly sampled carrier-based PWM in terms of the generated switched output is explained.

Carrier-Based PWM

Carrier-based PWM schemes are based on the comparison of a (real/non-complex) reference voltage signal with a periodic high-frequency carrier signal. To determine the switching times, there are three basic types of carrier-based PWM [70]: 1) Naturally sampled PWM, 2) Regularly sampled PWM, 3) Direct PWM. With naturally sampled PWM, switching takes place at the intersection of an analogue/non-sampled reference voltage and the carrier signal. With regularly sampled PWM, switching takes place at the intersection of a regularly sampled reference voltage and the carrier signal. With direct PWM, the switching times are determined in such a way that the integrated area of the reference voltage over the carrier/switching period is equal to the integrated area of the switched output voltage. The most common variant in today's systems is regularly sampled PWM, as it is suitable for digital signal processing on a DSP (in contrast to naturally sampled PWM) and less complex to

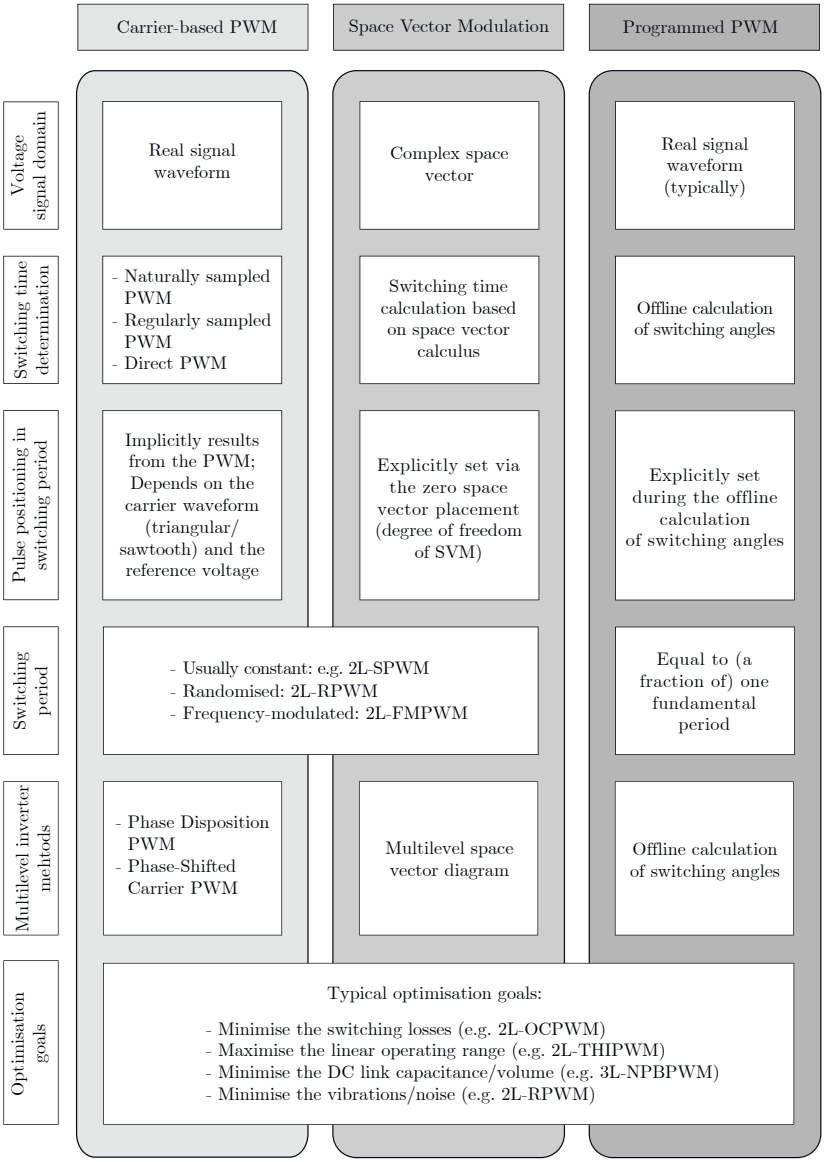


Figure 2.21: Classification of PWM schemes [69].

implement than direct PWM. In addition, direct PWM does not result in a lower Total Harmonic Distortion (THD) in the currents compared to regularly sampled PWM [70].
The position of the voltage pulses within a switching period T_{PWM} is not explicitly set in carrier-based PWM schemes but implicitly results from the carrier waveform and the reference voltage waveform. Typical carrier waveforms include a triangle and a sawtooth waveform.
The carrier/switching period T_{PWM} of the high-frequency carrier and thus the carrier/switching frequency $f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}}$ are typically constant in carrier-based PWM schemes. This is also the case in the standard sine-triangle PWM for 2L inverters (2L-SPWM). Other more particular PWM schemes have a randomised switching frequency (2L-RPWM) or a frequency-modulated switching frequency (2L-FMPWM), which can for example be used to reduce motor vibrations [69].
Carrier-based PWM can also be used for multilevel inverters. Standard methods include phase disposition PWM and phase-shifted carrier PWM which are explained in [71].
In order to reach certain inverter design goals, different advanced PWM schemes can be found in the literature. The design goals include for example low switching losses, a large linear operating range, a low DC link capacitance/volume, and low motor vibrations/noise. Corresponding PWM schemes are for example: 1) Two-level optimal clamping PMW (2L-OCPWM) described in [39], 2) Third-harmonic injection PWM (2L-THIPWM) described in section 5.3 of [70], 3) Three-level neutral point balanced PWM (3L-NPBPWM) described in [39], and 4) 2L-RPWM described in [69]. As indicated in Fig. 2.21, these PWM schemes are not only assigned to the group of carrier-based PWM schemes as they can also be implemented as a SVM scheme or as a programmed PWM scheme.

Space Vector Modulation

The voltage signal domain of space vector modulation (SVM) is the complex space vector plane. The switching times are calculated using closed form analytical equations ((6.5) & (6.6) in [70]). These equations are derived from the condition that the short time average of two inverter output voltage space vectors over one switching period T_{PWM} must correspond to the reference voltage space vector. This reference voltage space vector is regularly calculated once/twice (for symmetrically/asymmetrically sampled PWM) per switching period, which re-

sults in a regularly sampled reference voltage similar to the one used in carrier-based regularly sampled PWM.
In contrast to carrier-based PWM, SVM allows to position the switching pulses arbitrarily within one switching period T_{PWM} by explicitly setting the durations of the inactive/zero space vectors. This is often referred to as an additional degree of freedom of SVM compared to carrier-based PWM [71]. However, carrier-based PWM has actually an analogue degree of freedom which is the common mode (CM) component of a 3-phase reference voltage.
The concept of SVM can also be applied to multilevel inverters. The basic concept of calculating the switching state durations of two active space vectors from the space vector diagram is the same as for 2L SVM. But, multilevel space vector diagrams are more complex than the 2L space vector diagram due to the larger amount of possible switching states. A common method for multilevel SVM is the decomposition method described in section 12.3 of [70]. With this method a multilevel space vector diagram is split up/decomposed into multiple 2L space vector diagrams.

Programmed PWM

Programmed PWM schemes represent a special group of PWM schemes in which the switching times over one switching period are determined offline in advance for a much larger switching period (typically set by cycle symmetry requirements) compared to carrier-based PWM or SVM (section 9 of [70]). The switching time calculation is based on the minimisation of an objective function which is typically given by the system losses [70]. The switching period of a programmed PWM scheme varies with the fundamental frequency. Programmed PWM is included in the classification for the sake of completeness but is not further considered in this thesis. For more details on programmed PWM schemes it is referred to chapter 9 of [70].

Equivalence of Space Vector Modulation and Regularly Sampled Carrier-Based PWM

As follows from the previous sections, SVM and regularly sampled carrier-based PWM are different in terms of their implementation. How-

ever, they are equivalent in terms of their generated output voltage. This equivalence can be explained by first splitting up the output voltage of SVM into two pieces of information: 1) The relative durations of the switching states and 2) the order/sequence of the switching states. Now, the equivalence of the output voltages generated with SVM and the output voltages generated with regularly sampled carrier-based PWM is explained separately for each piece of information below.

The first piece of information of the SVM-generated output voltage, i.e. the relative switching state durations (e.g. δ_0, δ_2, δ_6, and δ_7 in (7) of [72]), is equivalent to the half bridge duty cycles (α_R, α_S, and α_T in (5) of [72]) and to the phase modulation functions (m_R, m_S, and m_T in (5) of [72]) which are used for carrier-based PWM. Especially, a particular distribution pattern of the zero space vectors belonging to the zero states {000} and {111} in SVM corresponds to a particular common mode (CM) offset of the phase modulation functions used for carrier-based PWM. This CM offset is usually a triplen harmonic of the fundamental wave but can also have a DC component. For example, SVM with equal time shares for the zero states is equivalent to carrier-based 2L-THIPWM which has a modulation function consisting of the fundamental and a superimposed third harmonic with $\hat{u}_3 = \hat{u}_3/6$ (sections 5.3, 6.1, and 6.2 of [70]).

The second piece of information of the SVM-generated output voltage, i.e. the switching state sequence for example in the first sextant of the space vector diagram, is usually defined as {000}-{100}-{110}-{111}-{111}-{110}-{100}-{000}. Using carrier-based PWM this is achieved through a triangular carrier signal. Alternatively, the sequence {000}-{100}-{110}-{111} could be realized with a sawtooth carrier. Therefore, the order of states chosen by SVM is equivalent to a particular choice of a carrier signal used for carrier-based PWM.

Consequently, SVM and regularly sampled PWM are equivalent in terms of the generated output voltage and they only differ in their implementation. This leads to two important aspects: 1) For the calculation of switched inverter output voltages in an analytical PWM-model, both quantities related to SVM (switching states and switching state durations) and quantities related to carrier-based PWM (half bridge duty cycles and phase modulation functions) can be used. 2) The distinction between SVM and carrier-based PWM has no impact on the switching/conduction losses that result from a PWM scheme. Therefore, this distinction is not made for the selection of PWM schemes for the IMD

modelling and design which is presented in the following section.

2.3.2 PWM Schemes Selected for Modelling and Design

In this section, the PWM schemes selected for the IMD modelling in chapter 3 and for the optimal IMD design in chapter 4 are described. The selection of PWM schemes should include basic and advanced PWM schemes for each of the inverter topologies selected in section 2.2.2, i.e. for 1) the 2L, 2) the 3L-NPC, 3) the 3L-TT, 4) the SPB, and 5) the N_{m}P-2L inverter topology. With regard to the PWM, these inverter topologies can be split up into two PWM specific inverter topology groups, in which the topologies can be combined with the same PWM schemes:

- *PWM specific inverter topology group 1:* 2L based inverter topologies (consisting of 2L inverter modules) which require a 2L-PWM scheme for each module: 2L, SPB, N_{m}P-2L
- *PWM specific inverter topology group 2:* 3L inverter topologies which require a 3L-PWM scheme: 3L-NPC, 3L-TT

For the first group of inverter topologies, 2L sinusoidal PWM (2L-SPWM) is selected as a basic PWM scheme and 2L optimal clamping PWM (2L-OCPWM) is selected as an advanced PWM scheme. For the second group of inverter topologies, 3L-SPWM is selected as a basic PWM scheme and 3L neutral point balanced PWM (3L-NPBPWM) is selected as an advanced PWM scheme. The basic concepts of the selected PWM schemes including their advantages and disadvantages are described in the following, whereas the detailed modelling is given in section 2.3.

2L Sinusoidal PWM

2L sinusoidal PWM (2L-SPWM) is the most basic PWM scheme for 2L inverters. A carrier-based implementation of 2L-SPWM is based on sinusoidal reference output voltage waveforms. In an SVM-based implementation of 2L-SPWM, the zero space vector durations are chosen in such a way that the average CM voltage over one switching period T_{PWM} is zero [39]. The advantage of 2L-SPWM is its simplicity and

hence its low implementation effort. The disadvantage of 2L-SPWM is that it results in relatively high switching losses due to a relatively high average switching frequency per switch of $f_{\mathrm{s,avg,2L\text{-}SPWM}} = f_{\mathrm{PWM}}$ [39].

2L Optimal Clamping PWM

In 2L optimal clamping PWM (2L-OCPWM) the phase/half bridge with the highest current is clamped to either the positive or negative DC rail [39]. In a carrier-based implementation of 2L-OCPWM, this is achieved by setting the half bridge duty cycle to zero/one for the sixth of the fundamental period in which the corresponding phase current is the highest current. In an SVM-based implementation of 2L-OCPWM, this is equivalent to using only one of the inactive zero switching states {000} or {111} during one sixth of the fundamental period. The advantage of 2L-OCPWM is that it results in relatively low switching losses due to a relatively low average switching frequency per switch of $f_{\mathrm{s,avg,2L\text{-}OCPWM}} = {}^{2}\!/_{3} f_{\mathrm{PWM}}$ [39].

3L Sinusoidal PWM

3L sinusoidal PWM is the most basic PWM scheme for 3L inverters. A carrier-based implementation of 3L-SPWM is based on sinusoidal reference output voltage waveforms. In an SVM-based implementation, similar to 2L-SPWM, the 3L zero space vector durations are chosen in such a way that the average CM voltage over one switching period T_{PWM} is zero [39]. As is the case for 2L-SPWM, the advantage of 3L-SPWM is its simplicity. The disadvantages of 3L-SPWM are relatively high switching losses (with $f_{\mathrm{s,avg,3L\text{-}SPWM}} = {}^{f_{\mathrm{PWM}}}\!/_{2}$) and a relatively large required DC link capacitance because 3L-SPWM does not actively balance the DC link [39].

3L Neutral Point Balanced PWM

In 3L neutral point balanced PWM (3L-NPBPWM), the half bridges are switched in such a way that the DC link voltage is actively balanced [39]. This PWM scheme requires the measurement of the motor output currents in order to control the average (over T_{PWM}) current that flows into the DC link midpoint to zero. Such a balancing is possible because the current flowing into the DC link midpoint has

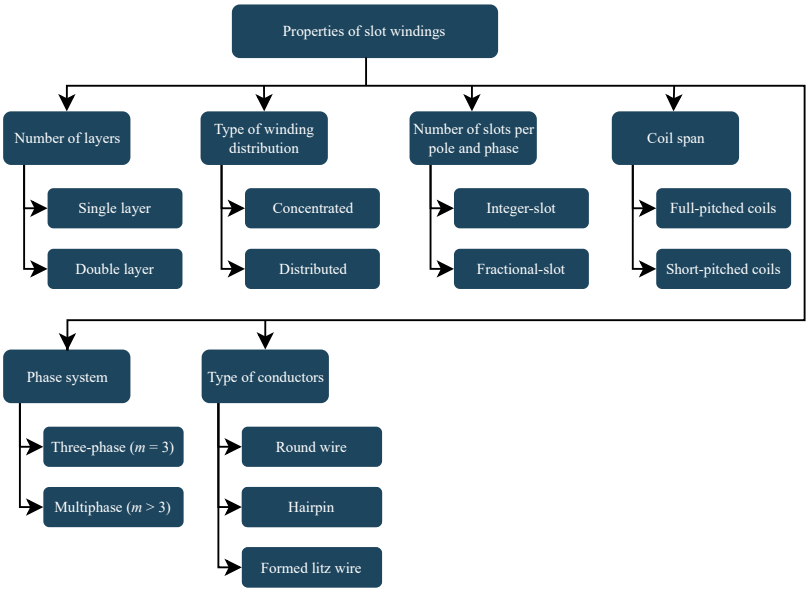


Figure 2.22: Classification of slot windings.

a different sign depending on the 3L zero space vectors. The advantage of 3L-NPBPWM is that a smaller DC link capacitance is required compared to 3L-SPWM. The disadvantage is a higher complexity. In terms of switching losses, similar switching losses as with 3L-SPWM occur because the average switching frequency per switch is given by $f_{\mathrm{s,avg,3L\text{-}NPBPWM}} = f_{\mathrm{PWM}}/2$, as in the case of 3L-SPWM [39].

2.4 Motor windings

In this section, first a classification of motor windings based on a literature research is given in subsection 2.4.1. Based on this classification, a selection of motor windings for the IMD modelling and design is presented in subsection 2.4.2.

Table 2.3: Slot winding parameters.

N	Number of stator slots
p	Pole pair number
m	Number of phases per base winding [73]
N_{ph}	Number of phase windings ($m \cdot a_{\mathrm{p}}$)
n_{l}	Number of winding layers
a_{p}	Number of phase-aligned winding axes

2.4.1 Classification of Motor Windings

The type of motor considered in this thesis are permanent magnet synchronous machines (PMSMs) with surface-mounted permanent magnets which are also referred to as SPMSMs. The windings of PMSMs are rotating-field stator windings, also called slot windings. Fig. 2.22 shows an overview of the various types of slot windings that are commonly distinguished in the literature, sorted by general properties of slot windings (Number of layers, type of winding distribution, etc.). These properties and the corresponding types of slot windings are explained in the following subsections. The slot winding parameters that are mentioned in these subsections are summarised in Tab. 2.3.

Number of Layers

The first slot winding property in Fig. 2.22 is the number of layers of a slot winding which corresponds to the number of coil sides within each stator slot. Typically, slot windings have either one or two coil sides within each slot, which is referred to as single-layer winding and as double-layer winding, respectively. An exemplary single-layer winding is shown in Fig. 2.23a and an exemplary double-layer winding is shown in Fig. 2.23b. For single-layer windings n_{l} is equal to 1 and for double-layer windings n_{l} is equal to 2. Double-layer windings are usually preferred over single-layer windings because 1) they enable an easier short-pitching of coils (explained later), 2) they offer more degrees of freedom in the winding design, and 3) they can be combined with formed coils/hairpin windings (section 1.2 of [74]). The use of single-layer windings is mainly limited to small induction machines (section 1.2 of [74]).

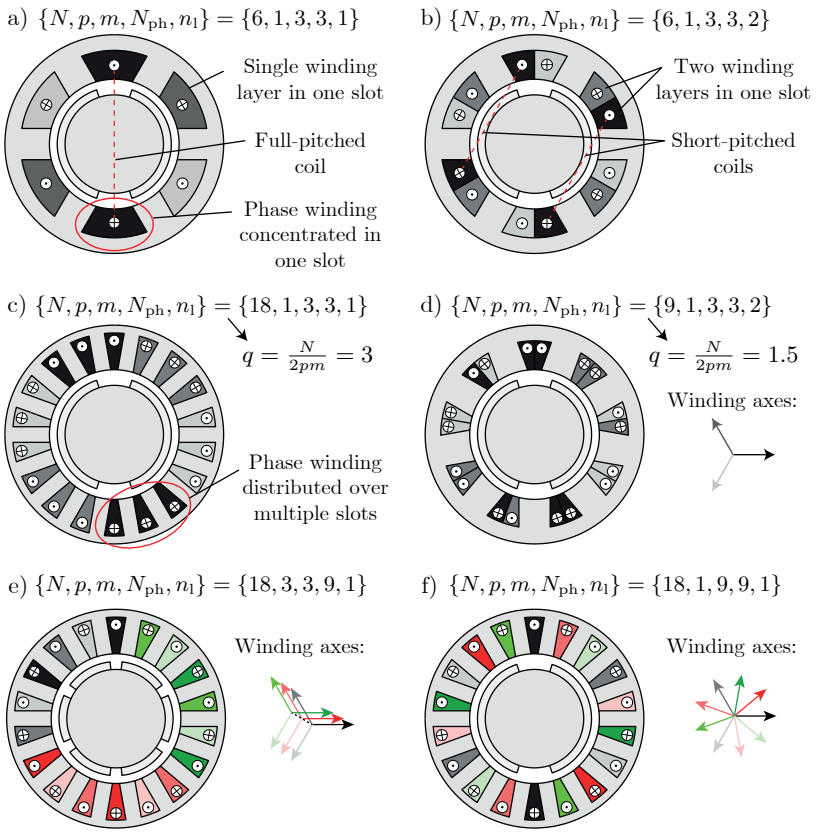


Figure 2.23: Exemplary winding schemes of slot windings based on schematic cross-sections of different SPMSMs.

Type of Winding Distribution

The second slot winding property in Fig. 2.22 is the type of winding distribution. Two typically distinguished typical types of winding distributions are concentrated windings and distributed windings. It is noted that the term *concentrated winding* is used differently in the literature. In this thesis, which is also in accordance with [75] (section 3.4.4) and [76], a concentrated winding is a winding that has only one coil per phase per pole pair, i.e. only one coil side per phase per pole ($n_{\mathrm{l}} \cdot N / 2pm = 1$). In contrast, a distributed winding has multiple

coils per phase per pole pair, i.e. multiple coil sides per phase per pole ($n_1 \cdot N/2pm \in \{2, 3, \ldots\}$). An example for a concentrated winding and an example for a distributed winding are shown in Fig. 2.23a and Fig. 2.23c, respectively. Distributed windings lead to a more sinusoidal stator magnetomotive force (MMF) distribution along the air gap, which is characteristic for brushless AC (BLAC) motors. In contrast, concentrated windings lead to a trapezoidal MMF distribution along the air gap, which is characteristic for brushless DC (BLDC) motors. A sinusoidal MMF distribution typically leads to a higher efficiency and a lower torque ripple compared to a trapezoidal MMF at the cost of a higher complexity for the control of sinusoidal currents.

Number of Slots per Pole and Phase

The third slot winding property in Fig. 2.22 is the number of slots per pole and phase (section 1.2.1.1 of [74]):

$$q = \frac{N}{2pm} \tag{2.1}$$

which is the most important property of a slot winding according to [74]. As the number of slots N is equal to the number of coil sides per winding layer, q also corresponds to the number of coil sides per winding layer per pole and phase. These coil sides per winding layer per pole and phase are typically placed adjacent to each other and then called a coil group (section 1.1.1.1 of [74]). With this definition, q corresponds to the average (over all coil groups) number of coil sides within one coil group. In integer slot windings ($q \in \mathbb{N}$), each coil group has the same number of coil sides which is equal to q. In contrast, in fractional-slot windings ($q \notin \mathbb{N}$), the coil groups have different numbers of coils (section 1.2.1.2). An example for an integer-slot winding with $q = 3$ is shown in Fig. 2.23c. There, all coil groups have three coil sides. An example for a fractional-slot winding with $q = 1.5$ is shown in Fig. 2.23d. There, each winding layer of each phase winding has two coil groups: One coil group with two coil sides and one coil group with just one coil side, resulting in an average of $q = 1.5$. According to section 2.8 of [73], fractional slot windings have several advantages over integer slot windings: 1) Large freedom of choice with respect to the number of slots. 2) Multiple alternatives for short-pitching (explained later). 3) If the number of slots is predetermined, the fractional-slot winding can

be applied to a wider range of the pole pair number. A disadvantage of fractional-slot windings is that, depending on q, they can lead to spatial subharmonics in the stator MMF waves (section 2.8 of [73]).

Coil Span

The fourth slot winding property in Fig. 2.22 is the coil span. The coil span W is defined as the mid-to-mid distance between the two coil sides of a coil of a phase winding, measured along the circumference with the inner stator radius $r_{\mathrm{s,i}}$ (section 1.1.1.1 of [74]). Typically, two basic types of coils are distinguished with regard to the coil span: Full-pitched coils and short-pitched coils. In full-pitched coils the coil span W is equal to one pole pitch $\tau_{\mathrm{p}} = {}^{2\pi r_{\mathrm{s,i}}}/_{2p}$. In short-pitched coils, the coil span is smaller/shorter than one pole pitch. Examples of winding schemes with full-pitched and short-pitched coils are shown in Fig. 2.23a and Fig. 2.23b, respectively. A particular type of short-pitched coils are tooth-coils which are wound around a single stator tooth and hence have a coil span of one slot pitch $\tau_{\mathrm{n}} = {}^{2\pi r_{\mathrm{s,i}}}/_{N}$. The advantages of short-pitched coils compared to full-pitched coils are (section 2.6 of [73]): 1) The end windings are shorter which reduces copper losses. 2) A more sinusoidal MMF distribution along the air gap can be achieved. The disadvantage of short-pitched coils is that the flux linkage of the fundamental flux density wave with the coil is reduced, requiring more turns to keep the flux linkage constant. More turns increase the copper losses again. However, the effect of the shorter end windings on the losses is typically more significant (section 2.6 of [73]).

Phase system

The fifth slot winding property from Fig. 2.22 is the phase system. Before explaining what this property refers to, it is noted that the term *phase* is used with different meanings in the literature, depending on the context: In the context of power electronics for electrical drives, *the phase number* typically refers to the number of output terminals of a converter which are connected to motor windings, also called phase windings. For this number, the parameter N_{ph} is defined in this thesis. In contrast, in the context of motor design, *the phase number* typically refers to the number of phase windings (and winding axes) per so-called

base winding (dt. Urwicklung) which is the smallest independent symmetrical section of a winding [73, 74]. This *phase number* is referred to as m in this thesis, in accordance with the standard literature on motor theory [73, 74]. To avoid any ambiguity that might result from this dual use of the term *phase*, what parameter is meant by this term is indicated with (m) or (N_{ph}) in this thesis, unless the meaning is clear from the context.
Coming back to the phase system, this property defines the number of phases per base winding, i.e. m, and their phase shifts to each other. This is typically represented by a vector diagram indicating the magnetic axis configuration of the phases (m) ([73], Tab. 2.4]). With regard to the phase system, slot windings are typically divided into three-phase slot windings ($m = 3$) and multiphase slot windings ($m > 3$).
Three-phase slot windings ($m = 3$) represent the most common type of slot winding. General advantages of three-phase slot windings are their low complexity, low cost, and relatively simple controllability. Typically, a three-phase slot winding ($m = 3$) also has three phase windings/motor terminals, i.e. $N_{\mathrm{ph}} = m = 3$. An exemplary winding scheme with this $\{N_{\mathrm{ph}}, m\}$-configuration and the corresponding well-known winding axis configuration are shown in Fig. 2.23d. The disadvantage of this $\{N_{\mathrm{ph}}, m\}$-configuration is that it can only be used with three-phase inverter topologies ($N_{\mathrm{ph}} = 3$). To use three-phase slot windings ($m = 3$) in combination with modular converters such as the SPB-C, a phase winding number of $N_{\mathrm{ph}} = 3N_{\mathrm{m}}$ is required, where N_{m} is the number of SPB-modules. To achieve this, the base windings of a slot winding are not all connected in series/parallel, which would result in the typical case of $N_{\mathrm{ph}} = m$. Instead, the base windings (or a partial series/parallel connection of them) are designed as separate phase systems (N_{ph}), i.e. with separate motor terminals [77]. By designing a_{p} base windings as separate phase systems, an $\{N_{\mathrm{ph}}, m\}$-configuration with $m = 3$ and $N_{\mathrm{ph}} = a_{\mathrm{p}} \cdot m$ is achieved. Therefore, by setting a_{p} equal to N_{m}, it is possible to use three-phase slot windings ($m = 3$) with an N_{m}-module SPB-C. As all base windings have identical phase systems, a winding with $N_{\mathrm{ph}} = a_{\mathrm{p}} \cdot m$ has a_{p} phase aligned winding systems/axes. An exemplary winding scheme with such an $\{N_{\mathrm{ph}}, m\}$-configuration and the corresponding winding axis configuration are shown in Fig. 2.23e for $\{N_{\mathrm{ph}}, m\} = \{9, 3\}$. There, the phase-aligned winding axes are indicated by diagonally displaced vectors.
In contrast to three-phase slot windings ($m = 3$), slot windings can also

be designed with more than three phases per base winding ($m > 3$). Such windings are typically referred to as multiphase windings. Multiphase windings ($m > 3$) have some advantages compared to three-phase windings ($m = 3$), including [78]: 1) A higher torque ripple frequency. 2) A higher order of the lowest spatial MMF harmonics (in BLAC motors). 3) A lower power per phase ratio, which enables the use of semiconductor devices with lower voltage/current ratings. (This is also valid for 3-phase windings ($m = 3$) with phase-aligned winding systems.) 4) An increased fault tolerance. 5) A higher torque density through torque enhancement by stator current harmonic injection when concentrated windings are used. At the same time, multiphase slot windings also have disadvantages, including significant low-order harmonic currents and the requirement for more complex control algorithms [79]. An exemplary winding scheme of a multiphase winding and the corresponding winding axis configuration are shown in Fig. 2.23f for $m = 9$. This winding axis configuration is also referred to as *symmetrical 9-phase* configuration as the winding axes form a symmetrical star with an angle of $2\pi/9$ between each winding axis/phase vector. For an overview of phase axis configurations with other phase numbers (m), it is referred to Tab. 2.4 of [73]. To combine multiphase slot windings with the considered modular inverter topologies, multi-three-phase slot windings ($m = 6$, 9, 12, etc.) are of particular interest.

Type of Conductors

The last slot winding property in Fig. 2.22 is the type of conductors. Three different types of conductors, which are compared in [80] with regard to their suitability for high-speed motors, are round wire, hairpin conductors, and formed litz wire. A schematic representation of one stator slot with each of these conductor types is shown in Fig. 2.24. Therein, Fig. 2.24a shows a round wire winding which is also called pull-in winding or stranded winding. Round wire windings have the disadvantage of a relatively low copper fill factor of 40 % to 45 % and additional losses caused by circulating currents that may occur in parallel connected strands [80]. Such circulating currents are caused by small asymmetries in the conductor arrangement of parallel strands in a wild winding, where the position of each wire is not strictly defined [80]. The advantages of round wire windings are their simplicity, their flexible use for different slot geometries, and the maturity of the technology. In addition, these advantages favour low production costs, in

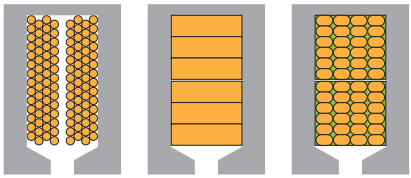


Figure 2.24: Schematic representation of different types of conductors for slot windings based on [80]. a) Round wire. b) Hairpin winding. c) Formed litz wire.

particular where a high number of turns is required, which is the case in low-speed motors.
Fig. 2.24b shows a hairpin winding which consists of solid copper bars with a separate insulation. An advantage of hairpin windings is a relatively high copper fill factor of over 50 % [80]. In addition, as the position of the copper bars is strictly defined, there are practically no circulating currents in parallel strands. A disadvantage of hairpin windings is their relatively complex manufacturing process including bending, cutting, and inserting of the solid conductors (hairpins) into the stator slots, which has a negative impact on manufacturing costs. Furthermore, hairpin windings are based on a relatively small amount of conductors per slot, which is not suitable for high turn numbers required for low-speed motors. The relatively large conductor cross-section additionally leads to higher AC losses through the skin/proximity effect.
Fig. 2.24c shows formed litz wire which consists of bars that are made from compressed twisted bundles of parallel connected strands [80]. The advantages of formed litz wire are a relatively high winding factor which is comparable to that of hairpin windings, a defined strand position which ensures low circulating currents in parallel strands, and a small strand diameter which minimises AC losses through the skin/proximity effect [80]. A disadvantage of formed litz wire is its relatively complex structure which is expected to lead to higher production costs compared to round wire windings. While this higher complexity and cost might be justified to limit the AC losses in high-speed motors, they are not necessary for low-speed motors, where the advantage of litz wire in terms of a lower phase resistance is relatively small (Fig. 5 of [80]).

2.4.2 Motor Windings Selected for Modelling and Design

The previous section has shown that there is a large variety of slot windings among which an IMD system designer can select. Theoretically, all properties of slot windings from Fig. 2.22 could be considered as IMD design parameters in an IMD design routine. However, to limit the modelling and computational effort, the modelled slot windings are narrowed down to windings that are particularly suitable for high-torque low-speed motors, such as the considered project motor (section 1.2), based on the following slot winding properties from Fig. 2.22:

- *Coil span*: Tooth-coil windings, whose coil span is equal to one slot pitch, are selected because of their short end windings. The effect of the end winding length on the copper losses is particularly important for high-torque motors that have a relatively high diameter-to-length ratio.
- *Type of conductors*: Round wire windings are selected because of their suitability and cost-effectiveness for a relatively large number of turns which is typically required for low-speed motors.
- *Number of layers*: Double-layer windings are selected because of the simpler short-pitching of coils compared to single-layer windings.
- *Type of winding distribution*: The type of winding distribution is not limited to concentrated or distributed windings because this would exclude a large number of potentially interesting fractional-slot windings such as that of the project motor with the winding parameters $\{N, p, m, n_\mathrm{l}\} = \{27, 12, 3, 2\}$.

The other slot winding properties from Fig. 2.22 (the number of slots per pole and phase $q = {}^{N}/_{2pm}$ and the phase system related parameters N_ph and m), the number of turns per coil n_t, and the conductor diameter d_c are considered as IMD design parameters which are either defined as constants or as variables for the IMD design, depending on the considered degree of generality of the motor. The following degrees of generality of the motor, also referred to as *motor stages*, are defined:

- *Motor stage MS1:* The motor corresponds to the project motor (section 1.2).

- *Motor stage MS2:* The motor has the same stator and rotor as the project motor, i.e. $\{N, p\} = \{27, 12\}$, but the slot winding is considered to be variable/general with regard to different winding parameters:
  - *Motor stage MS2a:* Consider all windings that can be achieved by reconnecting the original slot winding of the project motor. Hence the phase system parameters N_{ph} and m are design variables.
  - *Motor stage MS2b:* Consider all windings that can be achieved by replacing the original slot winding with a new winding. Hence, the phase system parameters N_{ph} and m, the number of turns n_{t}, and the conductor diameter d_{c} are design variables.
- *Motor stage MS3:* The motor results from a general motor design, where also the number of stator slots N and the number of pole pairs p are design variables.

Tab. 2.4 summarises which motor parameters are considered constants or variables in the different motor stages.

Table 2.4: Considered degrees of generality of the motor, referred to as *motor stages* (MS), for the IMD modelling and design.

Motor parameter		MS1	MS2a	MS2b	MS3
Number of stator slots	N	27	27	27	variable
Pole pair number	p	12	12	12	variable
Number of turns per coil	n_{t}	118	118	variable	variable
Conductor diameter (mm)	d_{c}	0.85	0.85	variable	variable
Number of phase windings	N_{ph}	3	variable	variable	variable
Number of phases per base winding	m	3	variable	variable	variable
Number of slots per pole and phase	$q = N/2pm$	0.375	variable	variable	variable

3

Modelling of Integrated Motor Drives

In this chapter, models for the calculation of the target quantities power density, efficiency, cost, and reliability of IMDs are presented, where the IMDs are based on the concepts selected in chapter 2. These models can be used in IMD design procedures such as the IMD design procedures presented in chapter 4.

The calculation of the target quantities involves the calculation of several intermediate quantities for which the respective models are given in the sections of this chapter: First, models for the calculation of inverter-related quantities are presented in section 3.1-3.5. This includes a PWM model in section 3.1, a DC link dimensioning model in section 3.2, a semiconductor conduction loss model in section 3.3, a semiconductor switching loss model in section 3.4, and an inverter reliability model in section 3.5.

Next, models for the calculation of motor-related quantities are presented in section 3.6-3.8. This includes a scalable motor model for multiphase non-salient PMSMs in section 3.6, a motor winding loss model in section 3.7, and motor iron loss models in section 3.8.

Finally, models for the calculation of IMD-/system-related quantities are presented in section 3.9-3.12. This includes a thermal IMD model in section 3.9, a separately developed thermal model of a finned heat sink in section 3.10, two IMD volume models in section 3.11, and an IMD cost model in section 3.12.

3.1 PWM Model

The purpose of the PWM model presented in this section is to calculate the switched inverter output voltages for the inverter topologies and PWM schemes selected in chapter 2. This model is based on the analytical switching state duty cycle functions from section 2.2 of [39]. What is not given in [39] and therefore given in this thesis is a formalism for the derivation and application of such switching state duty cycle functions for the calculation of switched output voltages.
This section is structured as follows: First, general definitions of the PWM model are given in subsection 3.1.1. Then, the specifications of the PWM schemes selected in chapter 2 are given in subsection 3.1.2. Finally, a procedure to calculate the switched output voltages is given in subsection 3.1.3.

3.1.1 General Definitions

This subsection provides general definitions that are used in the PWM model. This includes a definition of the switching frequency, the modulation index, the frequency modulation ratio, and 2L-/3L-inverter switching sequence representations.

Switching Frequency

Following common conventions, the switching frequency in this thesis refers to the PWM frequency $f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}}$, where T_{PWM} is one switching period. This switching frequency should not be confused with the average switching frequency of a single switch $f_{\mathrm{s,avg}}$ which in general depends on f_{PWM} and the individual PWM scheme (section 2.2 of [44]).

Modulation Index

The modulation index used for this PWM model is defined as

$$M := \frac{\sqrt{6} V_{\mathrm{ref}}}{V_{\mathrm{dc,m}}}, \tag{3.1}$$

where V_{ref} is the RMS amplitude of the reference voltage space vector that the PWM should set at the output of each inverter module, assuming steady state operation. $V_{\mathrm{dc,m}}$ is the module DC link voltage given

by $V_{\mathrm{dc}}/N_{\mathrm{s}}$, where N_{s} is the number of series connected (three-phase) inverter modules. N_{s} is equal to 1 for the inverter topologies 2L, 3L-NPC, 3L-TT, and N_{m}P-2L, and kept general ($N_{\mathrm{s}} \in \mathbb{N}$) for the SPB-inverter topology.

Frequency Modulation Ratio

The frequency modulation ratio M_{f} is defined as the ratio between the switching frequency and the fundamental frequency of the produced output voltage ((2.10) of [81]):

$$M_{\mathrm{f}} = \frac{f_{\mathrm{PWM}}}{f_{\mathrm{fw}}} \tag{3.2}$$

If M_{f} has an integer value, the carrier signal of carrier-based PWM is synchronised with the fundamental reference voltage, which is also called synchronous PWM/switching. Analogue to this, the PWM or the switching is called asynchronous if M_{f} has a non-integer value (section 8.2.1 of [82]). According to [82], asynchronous switching leads to subharmonics which are harmonics below the fundamental frequency. Subharmonics cause additional losses in AC motors and should therefore be avoided. However, according to section 5.6.2 of [70], subharmonics are not caused by asynchronous switching but by intermodulation effects between the fundamental frequency of the reference output voltage and a DC link voltage ripple caused by the inverter front end, for example by a six-pulse rectifier.
In this thesis, the output voltage of the inverter front is assumed to be sufficiently damped so that subharmonics can be neglected. Nevertheless, M_{f} is constrained to multiples of 6 in order to be able to determine a full fundamental period of the switched output voltage by only calculating a 60°-wide fraction of a period.

2L-Inverter Switching Sequence Representations

In the calculation procedure for the switched inverter output voltage, which is described later in section 3.1.3, the following two types of representing/defining a 2L-inverter switching sequence within one switching period T_{PWM} are used:

- *2L-inverter switching sequence representation based on inverter switching states:* Sequence of inverter switching states ss_1-ss_2-

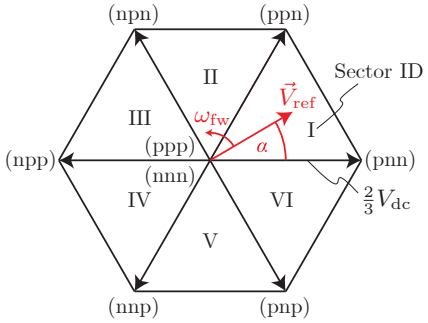


Figure 3.1: Space vector diagram for a 2L-converter with a reference voltage vector $\vec{V}_{\mathrm{ref}}$ which rotates with the fundamental frequency ω_{fw} [39].

ss_3-ss_4-ss_3-ss_2-ss_1 and the corresponding inverter switching state duty cycles $\{\delta_{ss_1}, \delta_{ss_2}, \delta_{ss_3}, \delta_{ss_4}\}$.

- *2L-inverter switching sequence representation based on half bridge duty cycles:* Half bridge p-state duty cycles $d_{h,\mathrm{p}}$ and half bridge p-state phase shifts $phsh_{h,\mathrm{p}}$ for all half bridges/phases $h \in \{\text{"r"}, \text{"s"}, \text{"t"}\}$.

The 2L-inverter switching sequence representation based on inverter switching states corresponds to the representation used in SVM. In general, the inverter switching states ss_1 to ss_4 can take as values any of the switching states of the 2L space vector diagram that is shown in Fig. 3.1. There, each switching state, as for example (pnn), indicates the half bridge switching states hss_h for each half bridge $h \in \{\text{"r"}, \text{"s"}, \text{"t"}\}$, where hss_h can take the value "p" (switched high) or "n" (switched low). The specific inverter switching state sequence and the corresponding inverter switching state duty cycles depend on the individual PWM schemes, which are specified later in section 3.1.3.
The 2L-inverter switching sequence representation based on half bridge duty cycles is based on the property of all considered PWM schemes that each half bridge is either switched on and off once per switching period or is not switched at all. With this assumption, the half bridge

p-state switching signal $s_{h,\mathrm{p}}(t)$, which is defined as

$$s_{h,\mathrm{p}}(t) = \begin{cases} 1, & hss_h(t) = \text{"p"} \\ 0, & \text{else} \end{cases}, h \in \{\text{"r"}, \text{"s"}, \text{"t"}\}, \tag{3.3}$$

has either a single pulse within one switching period or is constant. In case of a pulse, this pulse can have two basic types of pulse waveforms depending on the initial half bridge switching state $hss_h(t = 0)$ at the beginning of a switching period: 1) If $hss_h(t = 0) = \text{"n"}$, the pulse of $s_{h,\mathrm{p}}(t)$ is centred within the switching period. 2) If $hss_h(t = 0) = \text{"p"}$, the pulse of the inverse signal $\bar{s}_{h,\mathrm{p}}(t)$ is centred within the switching period. Based on these possible waveforms, the half bridge p-state switching signal over one switching period, i.e. for $t \in [0, T_{\mathrm{PWM}}]$, for each half bridge $h \in \{\text{"r"}, \text{"s"}, \text{"t"}\}$ can be expressed as

$$s_{h,\mathrm{p}}(t) = \begin{cases} 1, & t \in [0, \frac{phph_{h,\mathrm{p}} + d_{h,\mathrm{p}} - 1}{f_{\mathrm{PWM}}}] \vee t \in [\frac{phph_{h,\mathrm{p}}}{f_{\mathrm{PWM}}}, \frac{phph_{h,\mathrm{p}} + d_{h,\mathrm{p}}}{f_{\mathrm{PWM}}}] \\ 0, & \text{else} \end{cases} \tag{3.4}$$

With (3.4), $d_{h,\mathrm{p}}$ and $phph_{h,\mathrm{p}}$ fully specify the half bridge p-state switching signal $s_{h,\mathrm{p}}$ over one switching period, where $d_{h,\mathrm{p}}$ corresponds to the duty cycle of $s_{h,\mathrm{p}}$ and $phph_{h,\mathrm{p}}$ corresponds to the duration between $t = 0$ and the rising edge of $s_{h,\mathrm{p}}$, normalised to T_{PWM}.
For a better understanding of the two 2L-inverter switching sequence representations, Fig. 3.2a-b show an exemplary 2L-inverter switching sequence using the representation based on inverter switching states (Fig. 3.2a) and the corresponding representation based on half bridge duty cycles (Fig. 3.2b).
As explained in the following section, the 3L-inverter switching sequence representation based on half bridge duty cycles requires the additional parameters $d_{h,\mathrm{n}}$ and $phph_{h,\mathrm{n}}$ to define an additional half bridge n-state switching signal $s_{h,\mathrm{n}}$. For a 2L-inverter, $s_{h,\mathrm{n}}$ already corresponds to $\bar{s}_{h,\mathrm{p}}$, and therefore $d_{h,\mathrm{n}}$ and $phph_{h,\mathrm{n}}$ theoretically do not need to be considered. However, these parameters are considered in the calculation procedure for switched output voltages presented in section 3.1.3 as this leads to a generic calculation procedure that can be used for both 2L- and 3L-inverters.

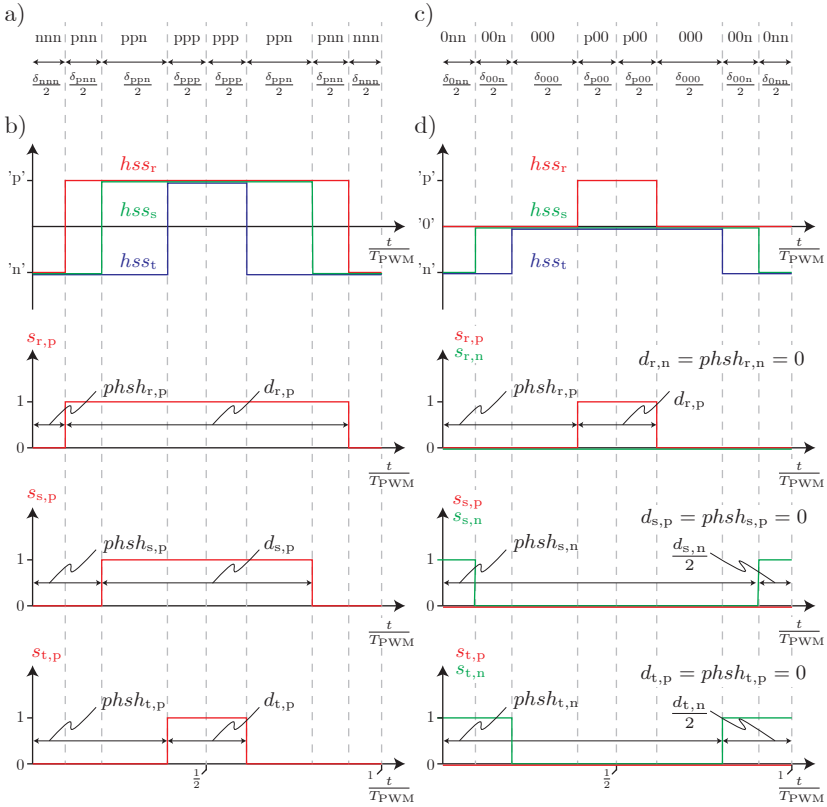


Figure 3.2: Example of a 2L-inverter switching sequence which is represented a) based on inverter switching states and b) based on half bridge duty cycles. Example of a 3L-inverter switching sequence which is represented c) based on inverter switching states and d) based on half bridge duty cycles.

3L-Inverter Switching Sequence Representations

In the calculation procedure for the switched inverter output voltage, which is described later in section 3.1.3, the following two types of representing/defining a 3L-inverter switching sequence within one switching period T_{PWM} are used:

- *3L-inverter switching sequence representation based on inverter*

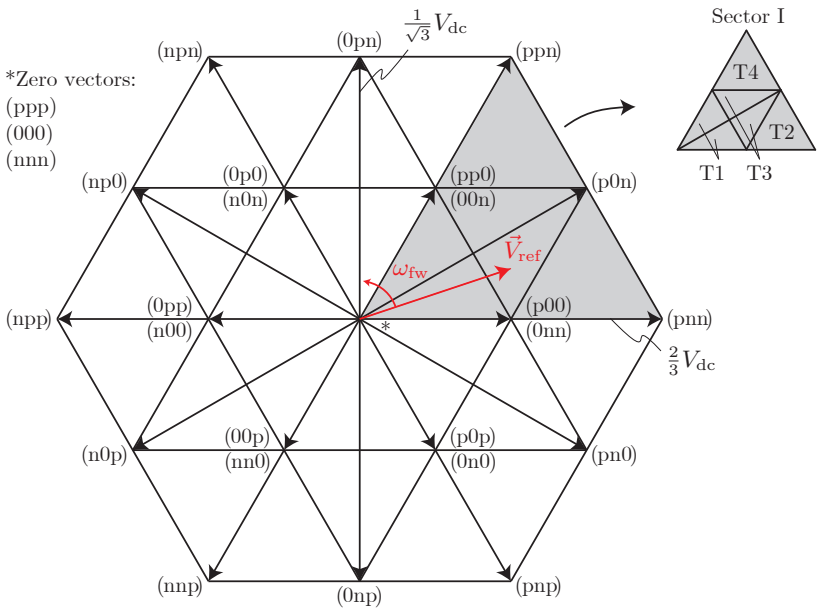


Figure 3.3: Space vector diagram for a 3L-converter with a reference voltage vector $\vec{V}_{\text{ref}}$ which rotates with the fundamental frequency ω_{fw} [39], including the definition of triangles T1, T2, T3, and T4 of sector I.

switching states: Sequence of inverter switching states ss_1-ss_2-ss_3-ss_4-ss_3-ss_2-ss_1 and the corresponding inverter switching state duty cycles $\{\delta_{ss_1}, \delta_{ss_2}, \delta_{ss_3}, \delta_{ss_4}\}$.

- *3L-inverter switching sequence representation based on half bridge duty cycles:* Half bridge p- & n-state duty cycles $d_{h,\text{p}}$ & $d_{h,\text{n}}$ and half bridge p- & n-state phase shifts $phsh_{h,\text{p}}$ & $phsh_{h,\text{n}}$ for all half bridges/phases $h \in \{\texttt{"r"}, \texttt{"s"}, \texttt{"t"}\}$.

The 3L-inverter switching sequence representation based on inverter switching states is basically the same as in the case of the 2L-inverter. The only difference is the space of available switching states ss_1 to ss_4 which, for a 3L-inverter, is given by the 3L space vector diagram that is shown in Fig. 3.3. In addition to the half bridge switching states "p" (switched high) and "n" (switched low), the half bridge switching states

hss_{h} for each half bridge $h \in \{\text{"r","s","t"}\}$ can also have the value "0" (switched to the DC link mid point).
Due to this additional available half bridge switching state, the 3L-inverter switching sequence representation based on half bridge duty cycles consists of two duty cycles $d_{h,\mathrm{p}}$ & $d_{h,\mathrm{n}}$ and two phase shifts $phsh_{h,\mathrm{p}}$ & $phsh_{h,\mathrm{n}}$ for each half bridge $h \in \{\text{"r","s","t"}\}$. Of these parameters, the parameters $d_{h,\mathrm{p}}$ and $phsh_{h,\mathrm{p}}$ indicate the duty cycle and the pulse position of the half bridge switching signal $s_{\mathrm{h,p}}$ and, analogously, the parameters $d_{h,\mathrm{n}}$ & $phsh_{h,\mathrm{n}}$ indicate the duty cycle and the pulse position of the half bridge switching signal $s_{\mathrm{h,n}}$. The signal $s_{\mathrm{h,p}}$ is already defined in (3.3). The signal $s_{\mathrm{h,n}}$ is analogously defined as:

$$s_{h,\mathrm{n}}(t) = \begin{cases} 1, & hss_h(t) = \text{"n"} \\ 0, & \text{else} \end{cases} \quad , h \in \{\text{"r", "s", "t"}\} \tag{3.5}$$

With the property of the considered 3L-PWM schemes that each half bridge is either only switched back and forth between "p" and "0", or between "n" and "0", or not at all within one switching period, both $s_{h,\mathrm{p}}$ and $s_{h,\mathrm{n}}$ can be expressed with (3.4). There, to express $s_{h,\mathrm{n}}$ with (3.4), only "p" has to be replaced by "n" in all parameter indices.
For a better understanding of the two 3L-inverter switching sequence representations, Fig. 3.2c-d show an exemplary 3L-inverter switching sequence using the representation based on inverter switching states (Fig. 3.2c) and the corresponding representation based on half bridge duty cycles (Fig. 3.2d).

3.1.2 PWM Scheme Specifications

In this section, the PWM scheme specifications are given for the PWM schemes selected in section 2.3.2 (2L-SPWM, 2L-OCPWM, 3L-SPWM, and 3L-NPBPWM). These PWM scheme specifications are used in the procedure for calculating the switched inverter output voltages which is described later in section 3.1.3.

2L-SPWM

The specifications of 2L-SPWM are given below:

- *Inverter switching state sequence in sector I (Fig. 3.1) within half a switching period* ss_1-ss_2-ss_3-ss_4*:* (nnn)-(pnn)-(ppn)-(ppp)

- *Condition on the switching state duty cycles of the zero states* δ_{nnn} *and* δ_{ppp}: The average CM voltage over one switching period must be equal to zero, i.e. $\sum_{i=1}^{4} \delta_{ss_i} \cdot \vec{v}_{\text{CM},ss_i} = 0$

2L-OCPWM

The specifications of 2L-OCPWM are given below:

- *Inverter switching state sequence in sector I (Fig. 3.1) within half a switching period* ss_1-ss_2-ss_3-ss_4*:* As one phase is always clamped during T_{PWM}, the switching sequence has only three switching states, i.e. ss_1-ss_2-ss_3. If phase R is clamped, the switching sequence (pnn)-(ppn)-(ppp) is used. If phase T is clamped, the switching sequence (nnn)-(pnn)-(ppn) is used.

- *Condition on the switching state duty cycles of the zero states* δ_{nnn} *and* δ_{ppp}: Depending on whether the phase R or the phase T is clamped, δ_{nnn} or δ_{ppp} is zero. The condition on when to clamp phase R/T in sector I is given by:

$$\text{"clamped phase"} = \begin{cases} R, f_{\text{bool,nnn}}(\alpha, \Psi(\phi)) = 0 \\ T, f_{\text{bool,nnn}}(\alpha, \Psi(\phi)) = 1 \end{cases} \tag{3.6}$$

  There, $f_{\text{bool,nnn}}$ is a Boolean function indicating whether the switching state (nnn) is used ($f_{\text{bool,nnn}} = 1$) or whether the switching state (ppp) is used ($f_{\text{bool,nnn}} = 0$). This function is given by

$$f_{\text{bool,nnn}}(\alpha, \Psi(\phi)) = \begin{cases} 1, & \alpha \in (I_u + \Psi(\phi)) \\ 0, & \text{else} \end{cases} \tag{3.7}$$

  There, I_u designates the union of intervals $[\frac{\pi}{6}, \frac{\pi}{2}] \cup [\frac{5\pi}{6}, \frac{7\pi}{6}] \cup [\frac{3\pi}{2}, \frac{11\pi}{6}]$, where both the length of each interval and the distance between the intervals is $\pi/3$. The function $f_{\text{bool,nnn}}(\alpha, \Psi(\phi))$ is shown in Fig. 3.4 for three different values of Ψ, where the white sectors correspond to $f_{\text{bool,nnn}} = 1$ and the grey sectors correspond to $f_{\text{bool,nnn}} = 0$. As Fig. 3.4 shows, Ψ corresponds to an angular shift of all sectors. The function $\Psi(\phi)$ that leads to optimal clamping in terms of minimal switching losses is shown in

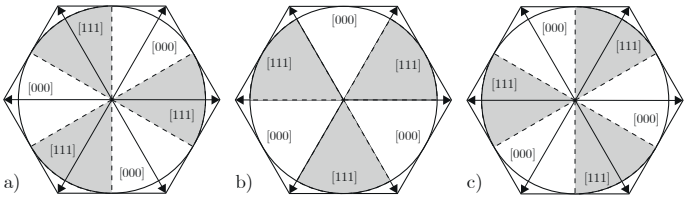


Figure 3.4: Boolean function $f_{\text{bool,nnn}}(\alpha, \Psi)$ for a) $\Psi = 0$, b) $\Psi = \pi/6$, and c) $\Psi = \pi/3$.

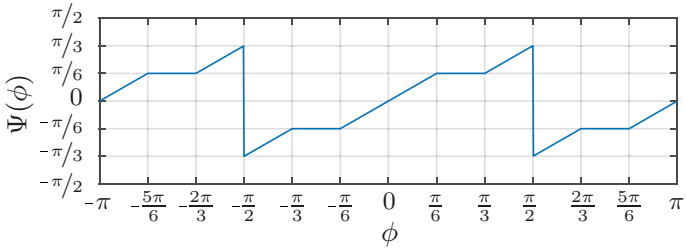


Figure 3.5: Clamping sector angle Ψ as a function of the voltage-current phase shift angle ϕ in 2L-OCPWM.

Fig. 3.5. This function corresponds to the function derived in [83] for $\phi \in [-\pi/2, \pi/2]$, symmetrically extended to $\phi \in [-\pi, \pi]$.

3L-SPWM

The specifications of 3L-SPWM are given below:

- *Inverter switching state sequence in sector I (Fig. 3.3) within half a switching period ss_1-ss_2-ss_3-ss_4:* The different sequences for the different triangles of sector I are given in Tab. 3.1. There, whether to use the variant a or b for triangle T1/T3, is determined by the condition on the CM voltage which is given in the following.
- *Condition on the CM voltage*: The average CM voltage over one switching period must be equal to zero, i.e. $\sum_{i=1}^{4} \delta_{ss_i} \cdot \vec{v}_{\text{CM},ss_i} = 0$

3L-NPBPWM

The specifications of 3L-NPBPWM are given below:

Triangle	Variant	Switching state sequence
T1	a	(0nn)-(00n)-(000)-(p00)
T1	b	(00n)-(000)-(p00)-(pp0)
T2	-	(0nn)-(pnn)-(p0n)-(p00)
T3	a	(0nn)-(00n)-(p0n)-(p00)
T3	b	(00n)-(p0n)-(p00)-(pp0)
T4	-	(00n)-(p0n)-(ppn)-(pp0)

Table 3.1: 3L-inverter switching state sequence used in 3L-SPWM and 3L-NPBPWM within half a switching period for each triangle in sector I of the 3L space vector diagram (Fig. 3.3). For the triangles T1 and T3, there are two variants called a/b.

Switching state ss_i	(000)	(p00)	(0nn)	(pp0)	(00n)	(pnn)	(p0n)	(ppn)
$i_{\mathrm{dc,out},0}(ss_i)$	0	$-i_{\mathrm{r}}$	i_{r}	i_{t}	$-i_{\mathrm{t}}$	0	i_{s}	0

Table 3.2: Current flowing out of the DC link midpoint $i_{\mathrm{dc,out},0}$ for each available switching state ss_i in sector I of the 3L space vector diagram (Fig. 3.3).

- *Inverter switching state sequence in sector I (Fig. 3.3) within half a switching period ss_1-ss_2-ss_3-ss_4:* The different sequences for the different triangles of sector I are given in Tab. 3.1. There, whether to use the variant a or b for triangle T1/T3, is determined by the condition on the current flowing out of the DC link midpoint which is given in the following.

- *Condition on the current flowing out of the DC link midpoint*: The average current flowing out of the DC link midpoint over one switching period must be equal to zero, i.e. $\sum_{i=1}^{4} \delta_{ss_i} \cdot i_{\mathrm{dc,out},0}(ss_i) = 0$. There, the current flowing out of the DC link midpoint $i_{\mathrm{dc,out},0}$ for each available switching state ss_i of sector I is given in Tab. 3.2.

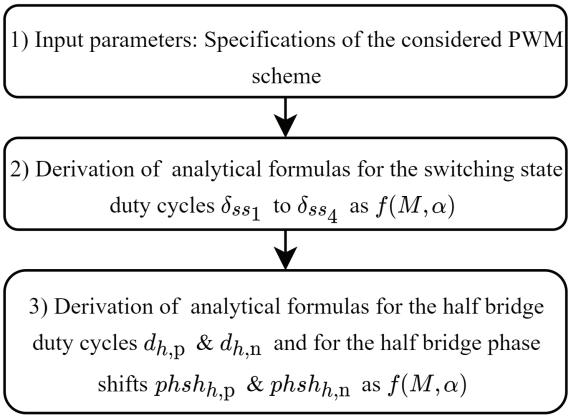


Figure 3.6: Offline procedure for the derivation of analytical functions of half bridge duty cycles and half bridge phase shifts.

3.1.3 Calculation of Switched Inverter Output Voltages

In this section, a procedure for calculating the switched inverter output voltages with any of the PWM schemes selected in section 2.3.2 (2L-SPWM, 2L-OCPWM, 3L-SPWM, 3L-NPBPWM) is described. This procedure is based on the analytical switching state duty cycle functions given in chapter 2.2 of [39]. As it is not clear from [39] how these analytical switching state functions are derived and how the switched inverter output voltages are calculated based on these functions, this is explained in this thesis. The complete procedure for calculating the switched inverter output voltages, including the derivation of the analytical switching state functions, can be split up into an *offline procedure* for deriving the required analytical functions and an *online procedure* for calculating the switched output voltages based on these analytical functions. These two procedures are explained in the following.

Offline Procedure

The offline procedure is shown in Fig. 3.6. In the first step of this procedure, the input parameters are defined which are given by the spec-

ifications of the considered PWM scheme. These specifications were already described in section 3.1.2.
In the second step of the offline procedure, analytical formulas for the inverter switching state duty cycles as a function of the modulation index M and the reference voltage angle α are derived. As the parameters M and α define the reference voltage space vector $\vec{v}_{\mathrm{ref}} = M \cdot {}^{V_{\mathrm{dc}}}/_{\sqrt{3}} \cdot \mathrm{e}^{\mathrm{j}\alpha}$, these formulas allow to calculate the inverter switching state duty cycles for each reference voltage vector $\vec{v}_{\mathrm{ref}}$ within sector I of the 2L/3L space vector diagram (Fig. 3.1/Fig. 3.3). In order to understand the origin of these formulas, their derivation is demonstrated here for example for 2L-SPWM (for a 2L-C): The derivation is based on the 2L-SPWM specifications given in section 3.1.2 and the following standard PWM conditions that apply to all considered PWM schemes:

$$\sum_{i=1}^{4} \delta_{ss_i} \cdot \vec{v}_{ss_i} = \vec{v}_{\mathrm{ref}} \tag{3.8}$$

$$\sum_{i=1}^{4} \delta_{ss_i} = 1 \tag{3.9}$$

There, (3.8) corresponds to the condition that the average voltage space vector over one switching period must be equal to the reference voltage space vector and (3.9) corresponds to the condition that the duration of the switching states ss_1 to ss_4 is limited by one switching period. Now, as known from the specifications of 2L-SPWM, the inverter switching state sequence in sector I within half a switching period ss_1-ss_2-ss_3-ss_4 is given by (nnn)-(pnn)-(ppn)-(ppp). Inserting these inverter switching states into (3.8) and inserting the zero space vectors $\vec{v}_{\mathrm{nnn}} = \vec{v}_{\mathrm{ppp}} = 0$ leads to the following equation:

$$\delta_{\mathrm{pnn}}\vec{v}_{\mathrm{pnn}} + \delta_{\mathrm{ppn}}\vec{v}_{\mathrm{ppn}} = \vec{v}_{\mathrm{ref}} \tag{3.10}$$

Inserting $\vec{v}_{\mathrm{pnn}} = {}^{2}/_{3}V_{\mathrm{dc}}$, $\vec{v}_{\mathrm{ppn}} = {}^{2}/_{3}V_{\mathrm{dc}}\mathrm{e}^{\mathrm{j}\pi/3}$, and $\vec{v}_{\mathrm{ref}} = M \cdot {}^{V_{\mathrm{dc}}}/_{\sqrt{3}} \cdot \mathrm{e}^{\mathrm{j}\alpha}$ into (3.10) results in an equation system with two equations (given by the real and the imaginary part of (3.10)), two unknowns (δ_{pnn} and δ_{ppn}), and two parameters (M and α). Solving this equation system for δ_{pnn} and δ_{ppn} results in the analytical duty cycle functions of the active states (pnn) and (ppn):

$$\delta_{\mathrm{pnn}} = M \cdot \cos\left(\frac{\pi}{6} + \alpha\right) \tag{3.11}$$

$$\delta_{\mathrm{ppn}} = M \cdot \sin(\alpha) \tag{3.12}$$

Now, the analytical duty cycle functions of the zero states (nnn) and (ppp) are derived based on the following two equations:

$$\delta_{\mathrm{nnn}} v_{\mathrm{CM,nnn}} + \delta_{\mathrm{pnn}} v_{\mathrm{CM,pnn}} + \delta_{\mathrm{ppn}} v_{\mathrm{CM,ppn}} + \delta_{\mathrm{ppp}} v_{\mathrm{CM,ppp}} = 0 \quad (3.13)$$

$$\delta_{\mathrm{nnn}} + \delta_{\mathrm{pnn}} + \delta_{\mathrm{ppn}} + \delta_{\mathrm{ppp}} = 1 \quad (3.14)$$

There, (3.13) corresponds to the condition from the 2L-SPWM specifications that the average CM voltage over one switching period must be equal to zero. In addition, (3.14) corresponds to the standard PWM condition (3.9) with inserted switching states. The CM voltage is given by the following weighted sum of the inverter half bridge output voltages v_h (terminal to DC link midpoint) for all half bridges $h \in \{\text{"r","s","t"}\}$:

$$v_{\mathrm{CM}} = \frac{1}{3}(v_{\mathrm{r}} + v_{\mathrm{s}} + v_{\mathrm{t}}) \quad (3.15)$$

There, the inverter half bridge output voltage v_h depending on the half bridge switching state hss_h is given by

$$v_h = \begin{cases} \frac{V_{\mathrm{dc}}}{2}, & hss_h = \text{"p"} \\ -\frac{V_{\mathrm{dc}}}{2}, & hss_h = \text{"n"} \end{cases} \quad , h \in \{\text{"r","s","t"}\} \quad (3.16)$$

With (3.15) and (3.16), the CM voltages in (3.13) result in $v_{\mathrm{CM,nnn}} = -V_{\mathrm{dc}}/2$, $v_{\mathrm{CM,pnn}} = -V_{\mathrm{dc}}/6$, $v_{\mathrm{CM,ppn}} = V_{\mathrm{dc}}/6$, and $v_{\mathrm{CM,nnn}} = V_{\mathrm{dc}}/2$. Inserting these CM voltages, (3.11), and (3.12) into (3.13), and solving the equation system given by (3.13) and (3.14) results in the analytical duty cycle functions for the zero states (nnn) and (ppp):

$$\delta_{\mathrm{nnn}} = \frac{1}{2} - \frac{M}{\sqrt{3}} \cdot \cos(\alpha) \quad (3.17)$$

$$\delta_{\mathrm{ppp}} = \frac{1}{2} - \frac{M}{\sqrt{3}} \cdot \sin\left(\frac{\pi}{6} + \alpha\right) \quad (3.18)$$

The equations (3.11), (3.12), (3.17), and (3.18) correspond to the analytical switching state duty cycle functions given in Tab. 2.1 of [39] whose derivation thus has been shown.

In the third step of the offline procedure (Fig. 3.6), these analytical switching state duty cycle functions are used to derive analytical formulas for the half bridge duty cycles $d_{h,\mathrm{p}}$ & $d_{h,\mathrm{n}}$ and for the half bridge phase shifts $phsh_{h,\mathrm{p}}$ and $phsh_{h,\mathrm{n}}$ which were defined in section 3.1.1. This is here demonstrated based on the same exemplary switching sequence of 2L-SPWM: The duty cycle $d_{h,\mathrm{p}}$, for example for the

half bridge h = "r", i.e. $d_{\mathrm{r,p}}$, corresponds to the sum of those inverter switching state duty cycles (among all duty cycles $\delta_{\mathrm{nnn}}, \delta_{\mathrm{pnn}}, \delta_{\mathrm{ppn}}, \delta_{\mathrm{ppp}}$) that fulfil hss_{r} = "p":

$$d_{\mathrm{r,p}} = \delta_{\mathrm{pnn}} + \delta_{\mathrm{ppn}} + \delta_{\mathrm{ppp}} \tag{3.19}$$

Inserting (3.11), (3.12), and (3.18) into (3.19), and simplifying the equation leads to $d_{\mathrm{r,p}}$ as a function of M and α:

$$d_{\mathrm{r,p}} = \frac{1}{2} + \frac{M}{\sqrt{3}} \cdot \cos(\alpha) \tag{3.20}$$

The phase "s"/"t" half bridge p-state duty cycles $d_{\mathrm{s,p}}$ and $d_{\mathrm{t,p}}$ as well as the half bridge n-state duty cycles $d_{h,\mathrm{n}}$ for all half bridges $h \in \{$"r","s","t"$\}$ are calculated in an analogue manner. The half bridge p-state phase shift $phsh_{h,\mathrm{p}}$, for example for the half bridge h = "r", i.e. $phsh_{\mathrm{r,p}}$, is derived from the type of pulse waveform of the phase "r" p-state switching signal $s_{\mathrm{r,p}}$. As explained in section 3.1.1, this signal can basically have two types of pulse waveforms: 1) If $hss_r(t = 0)$ = "n", the pulse of $s_{r,\mathrm{p}}(t)$ is centred within the switching period. 2) If $hss_r(t = 0)$ = "p", the pulse of the inverse signal $\bar{s}_{r,\mathrm{p}}(t)$ is centred within the switching period. In the considered example, the first inverter switching state is (nnn), i.e. $hss_r(t = 0)$ = "n", and consequently the pulse of $s_{\mathrm{r,p}}$ is centred within the switching period. This also corresponds to the type of waveform of $s_{\mathrm{r,p}}$ shown in Fig. 3.2b which is based on the same exemplary switching sequence that is considered here (i.e. (nnn)-(pnn)-(ppn)-(ppp)). For this type of waveform of $s_{\mathrm{r,p}}(t)$, $phsh_{\mathrm{r,p}}$ is given by

$$phsh_{\mathrm{r,p}} = \frac{1}{2} - \frac{d_{\mathrm{r,p}}}{2} \tag{3.21}$$

Inserting (3.20) into (3.21) finally leads to $phsh_{\mathrm{r,p}}$ as a function of M and α:

$$phsh_{\mathrm{r,p}} = \frac{1}{4} - \frac{M}{2\sqrt{3}} \cdot \cos(\alpha) \tag{3.22}$$

The phase "s"/"t" half bridge p-state phase shifts $phsh_{\mathrm{s,p}}$ and $phsh_{\mathrm{t,p}}$ as well as the half bridge n-state phase shifts $phph_{h,\mathrm{n}}$ for all half bridges $h \in \{$"r","s","t"$\}$ are calculated in an analogue manner.

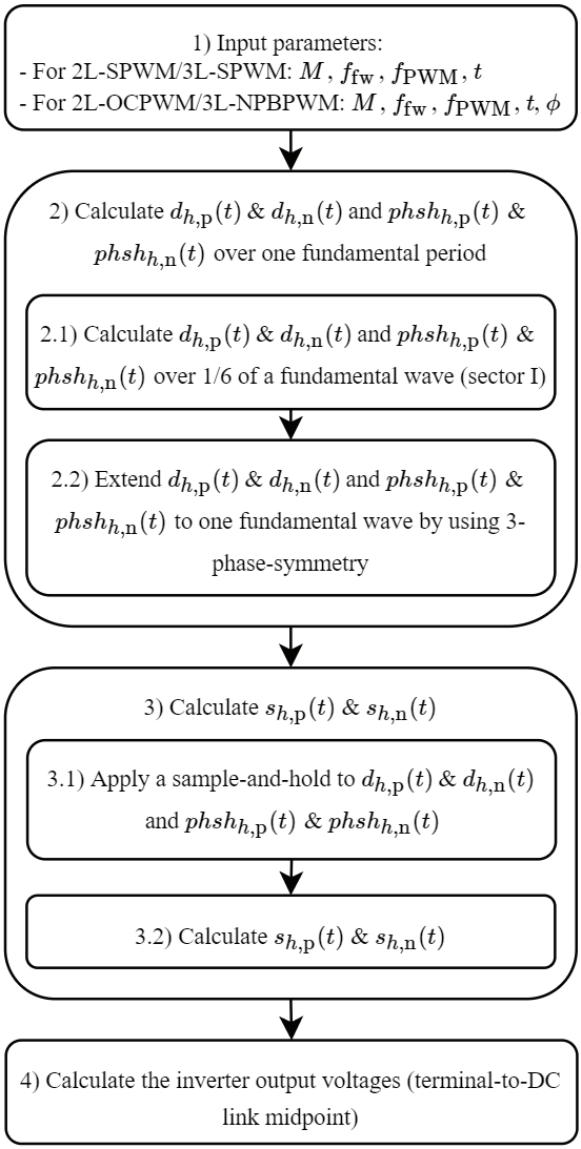


Figure 3.7: Online procedure for calculating the switched inverter output voltages (terminal-to-DC link midpoint) for the selected inverter topologies (2L, 3L-NPC, 3L-TT, SPB, N_{m}P-2L) and the selected PWM schemes (2L-SPWM, 2L-OCPWM, 3L-SPWM, 3L-NPBPWM).

Online Procedure

The online procedure for calculating the switched inverter output voltages is shown in Fig. 3.7. Step 1) of this procedure is the definition of input parameters which are given by the modulation index M, the fundamental frequency f_{fw}, the switching frequency f_{PWM}, and a quasi-continuous (discrete but of relatively high time resolution of approximately $\geq$100 points within T_{PWM}) time vector t. In addition, the PWM schemes 2L-OCPWM and 3L-NPBPWM also require the voltage-current phase shift angle ϕ as input parameter.
Step 2) of the online procedure is to calculate the half bridge p- & n-state duty cycles $d_{h,\mathrm{p}}$ & $d_{h,\mathrm{n}}$ and phase shifts $phph_{h,\mathrm{p}}$ & $phph_{h,\mathrm{n}}$ over one fundamental period $T_{\mathrm{fw}} = 1/f_{\mathrm{fw}}$ in the sub-steps 2.1) and 2.2). In sub-step 2.1), the functions $d_{h,\mathrm{p}}(t)$, $d_{h,\mathrm{n}}(t)$, $phph_{h,\mathrm{p}}(t)$, and $phph_{h,\mathrm{n}}(t)$ are first calculated over sector I of the 2L/3L space vector diagram (2L: Fig. 3.1, 3L: Fig. 3.3). For this calculation, the time vector t is converted into the angle vector $\alpha = 2\pi f_{\mathrm{fw}} t$ and the analytical formulas for $d_{h,\mathrm{p}}$, $d_{h,\mathrm{n}}$, $phph_{h,\mathrm{p}}$, and $phph_{h,\mathrm{n}}$, that result from the offline procedure described in section 3.1.3, are evaluated for α, M, and ϕ, where ϕ is only required for 2L-OCPWM and 3L-NPBPWM. Next, in sub-step 2.2), the functions $d_{h,\mathrm{p}}(t)$, $d_{h,\mathrm{n}}(t)$, $phph_{h,\mathrm{p}}(t)$, and $phph_{h,\mathrm{n}}(t)$ are extended from sector I to all sectors I-VI, i.e. to one fundamental period by using 3-phase-symmetry.
In step 3) of the online procedure, the half bridge p- & n-state switching signals $s_{h,\mathrm{p}}(t)$ & $s_{h,\mathrm{n}}(t)$ are calculated in the sub-steps 3.1) and 3.2). In sub-step 3.1) the half bridge p- & n-state duty cycles $d_{h,\mathrm{p}}$ & $d_{h,\mathrm{n}}$ and phase shifts $phph_{h,\mathrm{p}}$ & $phph_{h,\mathrm{n}}$ are sampled in the middle of each switching period and held constant within each switching period. This corresponds to symmetrically regularly sampled PWM with a triangular carrier signal and phase delayed sampling as described in section 3.6 of [70]. In sub-step 3.2), the half bridge p- & n-state switching signals $s_{h,\mathrm{p}}(t)$ & $s_{h,\mathrm{n}}(t)$ are then calculated using (3.4) for $s_{h,\mathrm{p}}(t)$ and using its analogue variant for $s_{h,\mathrm{n}}(t)$, in which "p" only has to be replaced by "n" in all parameter indices.
Finally, in step 4) of the online procedure, the inverter output voltages (terminal-to-DC link midpoint) are calculated for all half bridges $h \in \{\text{"r","s","t"}\}$ and all 3-phase inverter modules $i = 1, \ldots, N_{\mathrm{m}}$ using:

$$v_{h,i} = v_{\mathrm{mid},i} + \frac{V_{\mathrm{dc,m}}}{2} \cdot s_{h,\mathrm{p}}(t) - \frac{V_{\mathrm{dc,m}}}{2} \cdot s_{h,\mathrm{n}}(t) \tag{3.23}$$

There, $v_{\mathrm{mid},i}$ is the voltage between the module DC link midpoint of the i-th inverter module and the (overall) DC link midpoint of the inverter. This voltage is given by

$$v_{\mathrm{mid},i} = \begin{cases} 0, & N_\mathrm{s} = 1 \\ V_\mathrm{dc} \cdot \left(\frac{1}{2} - \frac{1}{N_\mathrm{s}} \cdot \left(i - \frac{1}{2} \right) \right), & N_\mathrm{s} \in \mathbb{N} \end{cases} \tag{3.24}$$

3.2 DC Link Dimensioning

In this section, a model for dimensioning the DC link capacitors of the inverter topologies selected in section 2.2.2 (2L, 3L-NPC, 3L-TT, SPB, N_mP-2L) is presented.

For the 2L-based inverter topologies (2L, SPB, N_mP-2L), the capacitor that needs to be dimensioned depends on the considered DC link topology. Two DC link topologies for 2L-based inverter topologies are covered by the presented model: 1) A *single-capacitor DC link topology* shown in Fig. 3.8a which consists of one capacitor C_dc per 3-phase inverter module. 2) A *split-capacitor DC link topology* shown in Fig. 3.8b which consists of two capacitors $C_\mathrm{dc,h}$ & $C_\mathrm{dc,l}$ (with $C_\mathrm{dc,h} = C_\mathrm{dc,l}$) in series per 3-phase inverter module. The motivation for the split-capacitor DC link topology is to provide a terminal for the (overall) DC link midpoint of an SPB-inverter which can be used for grounding.

For the 3L-inverter topologies (3L-NPC, 3L-TT), the DC link capacitor that needs to be dimensioned is $C_\mathrm{dc,p}$ ($= C_\mathrm{dc,n}$) which is shown in the 3L DC link topology in Fig. 3.8c.

The dimensioning of a DC link capacitor ($C_\mathrm{dc}/C_\mathrm{dc,h}/C_\mathrm{dc,p}$) can in general be split up into two steps: 1) Determining the capacitor requirements. 2) Selecting or designing a capacitor (or a series-parallel connection of capacitors) that fulfils these requirements. The DC link capacitor requirements can further be split up into: 1) The required rated voltage, 2) the required capacitance to limit the DC link voltage ripple to a defined maximum voltage ripple, and 3) the required RMS current capability.

In the following, first an overview of different inverter module numbers that are used for the DC link dimensioning is given in section 3.2.1. In section 3.2.2, a model for the required rated capacitor voltage is given. The capacitance required to keep the DC link voltage ripple below a defined maximum voltage ripple is separately determined for static load conditions and for dynamic load conditions in section 3.2.3

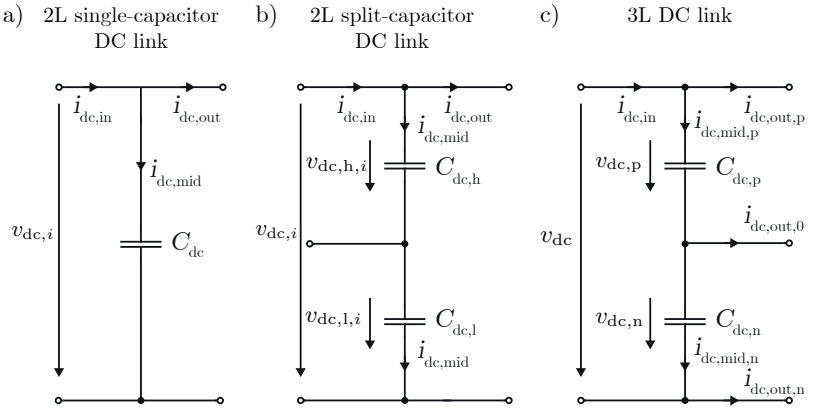


Figure 3.8: DC link topologies considered for the DC link dimensioning.

and 3.2.4, respectively. The RMS current requirement is described in section 3.2.5. Finally, the DC link capacitor selection/design, which is based on the DC link capacitor requirements from the sections 3.2.2-3.2.5, is explained in section 3.2.6.

3.2.1 Definition of Module Numbers

The following three module numbers are used for the DC link dimensioning for the considered inverter topologies (2L, 3L-NPC, 3L-TT, SPB, N_{m}P-2L): 1) The number of 3-phase inverter modules N_{m}. 2) The number of series-connected 3-phase inverter modules N_{s}. 3) The number of parallel-connected 3-phase inverter modules N_{p}. For the considered inverter topologies, these module numbers are given by:

$$N_{\mathrm{m}} \begin{cases} = 1, & \text{for a 2L-/3L-NPC-/3L-TT-inverter} \\ \in \mathbb{N}, & \text{for a SPB-/}N_{\mathrm{m}}\text{P-2L-inverter} \end{cases} \tag{3.25}$$

$$N_{\mathrm{s}} \begin{cases} = N_{\mathrm{m}}, & \text{for a SPB-inverter} \\ = 1, & \text{for a 2L-/}N_{\mathrm{m}}\text{P-2L-/3L-NPC-/3L-TT-inverter} \end{cases} \tag{3.26}$$

$$N_{\mathrm{p}} \begin{cases} = N_{\mathrm{m}}, & \text{for a } N_{\mathrm{m}}\text{P-2L-inverter} \\ = 1, & \text{for a 2L-/SPB-/3L-NPC-/3L-TT-inverter} \end{cases} \tag{3.27}$$

3.2.2 Rated Voltage Requirement

The minimum required voltage rating of the capacitor $C_{\mathrm{dc}}/C_{\mathrm{dc,h}}$ of the considered 2L-based inverter topologies (2L, SPB, N_{m}P-2L) with single-/split-capacitor DC link is referred to as $V_{\mathrm{dc,min}}/V_{\mathrm{dc,h,min}}$ and corresponds to the maximum voltage occurring over $C_{\mathrm{dc}}/C_{\mathrm{dc,h}}$. This maximum is estimated based on the mean DC link voltage V_{dc}, the reference maximum DC link voltage ripple (pk-to-pk) for steady load conditions $\Delta v^*_{\mathrm{dc,s,max}}$, and the reference maximum DC link voltage ripple (pk-to-pk) for dynamic load conditions $\Delta v^*_{\mathrm{dc,d,max}}$, resulting in:

$$V_{\mathrm{dc,min}} = \frac{1}{N_{\mathrm{s}}}\left(V_{\mathrm{dc}} + \frac{\Delta v^*_{\mathrm{dc,s,max}}}{2} + \frac{\Delta v^*_{\mathrm{dc,d,max}}}{2}\right) \tag{3.28}$$

$$V_{\mathrm{dc,h,min}} = \frac{V_{\mathrm{dc,min}}}{2} \tag{3.29}$$

In an analogue manner, the minimum required voltage rating of the capacitor $C_{\mathrm{dc,p}}$ of the considered 3L-inverter topologies (3L-NPC, 3L-TT) is referred to as $V_{\mathrm{dc,p,min}}$ and corresponds to the maximum voltage over $C_{\mathrm{dc,p}}$. This maximum is also estimated based on V_{dc}, $\Delta v^*_{\mathrm{dc,s,max}}$, and $\Delta v^*_{\mathrm{dc,d,max}}$. In addition, as the PWM scheme 3L-SPWM leads to a low-frequency (LF) oscillation/ripple of the voltage over $C_{\mathrm{dc,p}}$, a corresponding reference maximum LF (pk-to-pk) ripple $\Delta v^*_{\mathrm{dc,p,s,max}}$ must be taken into account for 3L-SPWM. These considerations result in the following equation for $V_{\mathrm{dc,p,min}}$

$$V_{\mathrm{dc,p,min}} = \frac{1}{2}\left(V_{\mathrm{dc}} + \frac{\Delta v^*_{\mathrm{dc,s,max}} + \Delta v^*_{\mathrm{dc,d,max}}}{2} + b_{\mathrm{PWM}}\Delta v^*_{\mathrm{dc,p,s,max}}\right) \tag{3.30}$$

where b_{PWM} is a Boolean parameter that takes the dependency on the PWM scheme into account:

$$b_{\mathrm{PWM}} = \begin{cases} 1, \text{for 3L-SPWM} \\ 0, \text{for 3L-NPBPWM} \end{cases} \tag{3.31}$$

3.2.3 Capacitance Requirement for Static Load

In this subsection, the equations for the dimensioning of the DC link capacitance under static load conditions, i.e. for steady state, are derived for the different PWM schemes selected in section 2.3.2 and thus for the inverter topologies of the PWM specific inverter topology groups

defined in that section.
In [39], such DC link dimensioning is done for the standard converter topologies (2L, 3L-NPC, 3L-TT) with the assumption of a unity power factor, i.e. $\cos(\phi) = 1$ and hence $\phi = 0$, which is valid for the PFC converter that is primarily considered in [39]. However, the power factor resulting from the output voltages and currents of a drive inverter generally deviates from unity due to the partially inductive motor load. The voltage-current phase shift angle ϕ depends on the motor operating point and can for example range from 0° to approximately 40° for the considered project motor. Therefore, the capacitance equations in this section are derived taking the case of $\phi \neq 0$ into account.
For a general notation of inverter output voltages and currents, all selected inverter topologies (2L, 3L-NPC, 3L-TT, SPB, N_mP-2L) are considered as a series-parallel connection of N_m 3-phase inverter modules with N_s modules in series and N_p modules in parallel, where the values of N_m, N_s, and N_p for each inverter topology are given in (3.25)-(3.27). The notation used in this section for the inverter output voltages of the i-th 3-phase inverter module is given by

$$\vec{v}_{\mathrm{term},i} \approx \vec{v}_{\mathrm{ref},i} = \sqrt{2} V_\mathrm{ref} e^{\mathrm{j}\alpha_i} = \frac{M}{\sqrt{3}} V_{\mathrm{dc,m}} e^{\mathrm{j}\alpha_i}, \tag{3.32}$$

where $\vec{v}_{\mathrm{term},i}$ and $\vec{v}_{\mathrm{ref},i}$ are the space vectors of the 3-phase inverter module output voltages and of the corresponding reference voltages, respectively. The 3-phase inverter module DC link voltage $V_{\mathrm{dc,m}}$ is given by $v_\mathrm{dc}/N_\mathrm{s}$. The output line currents of the 3-phase inverter module are assumed to be sinusoidal and to have the RMS amplitude I_conv, resulting in

$$\begin{aligned} i_{\mathrm{r},i}(t) &= \sqrt{2} I_\mathrm{conv} \cos(\alpha_i - \phi) \\ i_{\mathrm{s},i}(t) &= \sqrt{2} I_\mathrm{conv} \cos(\alpha_i - \phi - 2\pi/3) \\ i_{\mathrm{t},i}(t) &= \sqrt{2} I_\mathrm{conv} \cos(\alpha_i - \phi - 4\pi/3). \end{aligned} \tag{3.33}$$

In the following, the required DC link capacitances are derived for the selected PWM schemes, i.e. for 2L-SPWM, 2L-OCPWM, 3L-SPWM, and 3L-NPBPWM. The following sections on 2L-SPWM/2L-OCPWM apply to all considered 2L-based inverter topologies (2L, SPB, N_mP-2L) and the following sections on 3L-SPWM/3L-NPBPWM apply to all considered 3L-inverter topologies (3L-NPC, 3L-TT).

Table 3.3: Current $i_{\mathrm{dc,out}}$ for all switching states of a 2L-inverter module.

Switching state	$i_{\mathrm{dc,out}}$
nnn	0
pnn	i_{r}
ppn	$-i_{\mathrm{t}}$
npn	i_{s}
npp	$-i_{\mathrm{r}}$
nnp	i_{t}
pnp	$-i_{\mathrm{s}}$
ppp	0

2L-SPWM

For 2L-SPWM, first the single-capacitor DC link topology shown in Fig. 3.8a is considered. There, the input current $i_{\mathrm{dc,in}}$ flows from the DC source to the DC link. This current is assumed to be constant in steady state because the power flowing into the motor is approximately constant in steady state and the DC link voltage ripple is assumed to be relatively small. The output current of the DC link $i_{\mathrm{dc,out}}$ changes with the switching state of the 2L-inverter module according to Tab. 3.3. The requirement for the DC link voltage is that the peak-to-peak DC link voltage ripple Δv_{dc} must not exceed a reference maximum peak-to-peak ripple of the (total) DC link voltage $\Delta v^*_{\mathrm{dc,s,max}}$ that is defined by the designer in order to minimise the error between the reference and the actual inverter output voltages:

$$\Delta v_{\mathrm{dc}} \overset{!}{\leq} \Delta v^*_{\mathrm{dc,s,max}} \tag{3.34}$$

This criterion corresponds to the following criterion for the DC link capacitance C_{dc}:

$$C_{\mathrm{dc}} \overset{!}{\geq} C_{\mathrm{dc,min,s}} = \frac{\Delta Q_{\mathrm{max}}}{\Delta v^*_{\mathrm{dc,m,s,max}}} \tag{3.35}$$

where ΔQ_{max} denotes the charge ripple of the capacitor and $\Delta v^*_{\mathrm{dc,m,s,max}}$ is the reference maximum peak-to-peak ripple of the DC link voltage of one 2L-inverter module which is given by $\Delta v^*_{\mathrm{dc,s,max}}/N_{\mathrm{s}}$. The charge ripple is equal to the maximum integral of the current flowing into the

capacitor $i_{\mathrm{dc,mid}} = i_{\mathrm{dc,in}} - i_{\mathrm{dc,out}}$ between two arbitrary time instants t_1 and t_2 within one switching period T_{PWM}:

$$\Delta Q_{\max} = \max \int_{t_1}^{t_2} \frac{P_{\mathrm{out},i}}{V_{\mathrm{dc,m}}} - i_{\mathrm{dc,out}} \mathrm{d}t \tag{3.36}$$

In this equation, $P_{\mathrm{out},i}/V_{\mathrm{dc,m}}$ was inserted for $i_{\mathrm{dc,in}}$, where $P_{\mathrm{out},i}$ is the output power delivered by one 2L-inverter module to the motor and $V_{\mathrm{dc,m}}$ is the mean DC link voltage of one 2L-inverter module. With the definition of the converter output voltages in (3.32) and of the converter output currents in (3.33), the output power $P_{\mathrm{out},i}$ results in:

$$P_{\mathrm{out},i} = 3 V_{\mathrm{ref}} I_{\mathrm{conv}} \cos(\phi) \tag{3.37}$$

Inserting the definition of the modulation index from (3.1) into (3.37) leads to:

$$P_{\mathrm{out},i} = 3 \frac{M V_{\mathrm{dc,m}}}{\sqrt{6}} I_{\mathrm{conv}} \cos(\phi) \tag{3.38}$$

In order to calculate the capacitance requirement $C_{\mathrm{dc,min,s}}$, first (3.36) must be solved. In this respect, it is important to note that $i_{\mathrm{dc,out}}$ in (3.36) depends on the active switching state according to Tab. 3.3. Different reference voltage angles α_i of the reference voltage space vector $\vec{v}_{\mathrm{ref},i} = \sqrt{2} V_{\mathrm{ref}} \cdot e^{\mathrm{j}\alpha_i}$ lead to different partitionings of T_{PWM} among these switching states in Tab. 3.3. Therefore, the contribution of $i_{\mathrm{dc,out}}$ to the integral in (3.36) depends on α_i. In case of a unity power factor, i.e. $\cos(\phi) = 1$, [39] has shown that there is a critical reference voltage angle $\alpha_{\mathrm{crit}} = 0°$ which delivers the solution of (3.36). Moreover, [39] shows that the charge ripple $\Delta Q_{\max}$ is caused only by the switching state (ppp) at this critical angle. A numerical analysis of the more general case considered here, given by $\cos(\phi) \neq 1$, shows that the critical reference voltage angle α_{crit} depends on the voltage-current phase shift angle ϕ and on the modulation index M. The resulting critical angle $\alpha_{\mathrm{crit}}(\phi, M)$ is shown in Fig. 3.9. 2D curve fitting allows for an analytical approximation of $\alpha_{\mathrm{crit}}(\phi, M)$ resulting in

$$\alpha_{\mathrm{crit}}(\phi, M) \approx \begin{cases} 0, & (\phi, M) \in A_1 \\ a\phi^3 + b\phi^2 + cM\phi + d\phi + eM + f, & (\phi, M) \in A_2 \end{cases} \tag{3.39}$$

where the parameters a-f are given in Tab. 3.4. In (3.39), A_1 and A_2 denote the areas in which either 0 or the polynomial are valid. These

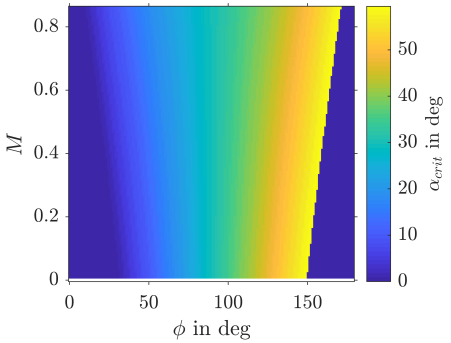


Figure 3.9: Critical reference voltage angle α_{crit} vs. M and ϕ for 2L-SPWM.

Table 3.4: Coefficients of the polynomial in (3.39) for α_{crit} in radian.

Coefficient	Value	Coefficient	Value
a	0.03408	d	0.7286
b	−0.1606	e	0.3360
c	−0.2139	f	−0.3567

areas are given by

$$\begin{aligned} A_1 &= A_{\text{tot}} \cap \{\phi < 30^\circ \wedge M < -\phi/25^\circ + 1.2 \\ &\qquad \vee \phi > 150^\circ \wedge M < \phi/25^\circ - 6\} \\ A_2 &= A_{\text{tot}} \setminus A_1 \\ A_{\text{tot}} &= \{\phi \in [0, \pi) \wedge M \in [0, \sqrt{3}/2]\} \end{aligned} \tag{3.40}$$

There, the total modulation index interval is limited by $\sqrt{3}/2$ because this is the maximum possible modulation index of 2L-SPWM in the linear operating range [81]. The polynomial from (3.39) is only valid for phase shift angles ϕ within the interval $[0, \pi)$. However, the critical angle can also be computed for negative phase shifts using the symmetry

$$\alpha_{\text{crit}}(\phi, M) = \alpha_{\text{crit}}(\phi + \pi, M), \quad \text{for } \phi \in [-\pi, 0) \tag{3.41}$$

Although α_{crit} depends on ϕ and M, the numerical analysis shows that the critical switching state sequence that causes the maximum charge

ripple is always the same, namely (nnn)-(pnn). The maximum charge ripple is therefore given by

$$\Delta Q_{\max} = |\Delta Q_{\mathrm{nnn}}(\alpha_{\mathrm{crit}}) + \Delta Q_{\mathrm{pnn}}(\alpha_{\mathrm{crit}})| \tag{3.42}$$

There, $\Delta Q_{\mathrm{nnn}}(\alpha_{\mathrm{crit}})$ and $\Delta Q_{\mathrm{pnn}}(\alpha_{\mathrm{crit}})$ are the charges that flow into the DC link capacitor during the active time of the switching states (nnn) and (pnn), respectively. These charges can be expressed by the product of the active times and the current flowing into the capacitor, which results in

$$\Delta Q_{\mathrm{nnn}}(\alpha_{\mathrm{crit}}) = \left(\frac{P_{\mathrm{out},i}}{V_{\mathrm{dc,m}}} - i_{\mathrm{dc,out}}(\mathrm{nnn}, \alpha_{\mathrm{crit}})\right) \delta_{\mathrm{nnn}}(\alpha_{\mathrm{crit}}) T_{\mathrm{PWM}} \tag{3.43}$$

$$\Delta Q_{\mathrm{pnn}}(\alpha_{\mathrm{crit}}) = \left(\frac{P_{\mathrm{out},i}}{V_{\mathrm{dc,m}}} - i_{\mathrm{dc,out}}(\mathrm{pnn}, \alpha_{\mathrm{crit}})\right) \delta_{\mathrm{pnn}}(\alpha_{\mathrm{crit}}) T_{\mathrm{PWM}} \tag{3.44}$$

Using Tab. 3.3, the current $i_{\mathrm{dc,out}}$ in (3.43) and (3.44) is given by

$$i_{\mathrm{dc,out}}(\mathrm{nnn}, \alpha_{\mathrm{crit}}) = 0 \tag{3.45}$$

$$i_{\mathrm{dc,out}}(\mathrm{pnn}, \alpha_{\mathrm{crit}}) = i_{\mathrm{r},i}(\alpha_{\mathrm{crit}}) = \sqrt{2} I_{\mathrm{conv}} \cos(\alpha_{\mathrm{crit}} - \phi) \tag{3.46}$$

Inserting (3.38)-(3.46) into (3.35) leads to the following formula for the minimum required DC link capacitance for static load conditions for 2L-SPWM:

$$\begin{aligned} C_{\mathrm{dc,min,s}} = \frac{I_{\mathrm{conv}}}{\Delta v^*_{\mathrm{dc,m,s,max}} f_{\mathrm{PWM}}} \Bigg| & \sqrt{\frac{3}{2}} M \cos(\phi)(\delta_{\mathrm{nnn}}(\alpha_{\mathrm{crit}}) \\ & + \delta_{\mathrm{pnn}}(\alpha_{\mathrm{crit}})) - \sqrt{2} \cos(\alpha_{\mathrm{crit}} - \phi) \delta_{\mathrm{pnn}}(\alpha_{\mathrm{crit}}) \Bigg| \end{aligned} \tag{3.47}$$

Therein, the duty cycles $\delta_{\mathrm{nnn}}(\alpha_{\mathrm{crit}})$ and $\delta_{\mathrm{pnn}}(\alpha_{\mathrm{crit}})$ are calculated by evaluating the duty cycle functions in (3.48) and (3.49) from [39] for $\alpha_i = \alpha_{\mathrm{crit}}$.

$$\delta_{\mathrm{nnn}}(\alpha_i) = \frac{1}{2} - \frac{M}{\sqrt{3}} \cos(\alpha_i) \tag{3.48}$$

$$\delta_{\mathrm{pnn}}(\alpha_i) = M \cos\left(\frac{\pi}{6} + \alpha_i\right) \tag{3.49}$$

Thus, the complete set of equations to calculate $C_{\mathrm{dc,min,s}}$ is given by (3.47), (3.48), (3.49), and (3.39).

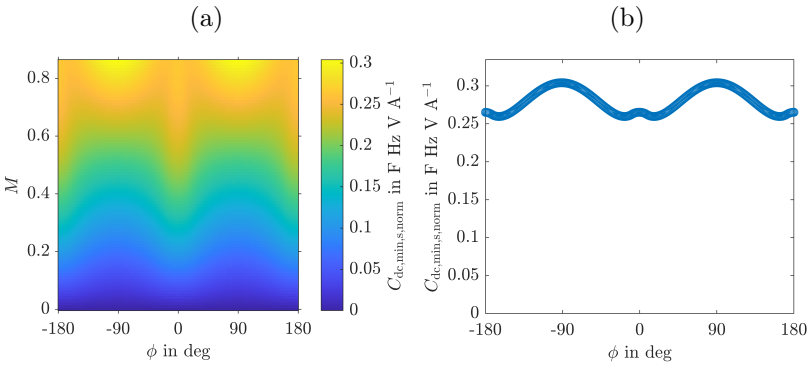


Figure 3.10: a) Normalised minimum DC link capacitance for static load conditions $C_{\mathrm{dc,min,s,norm}}$ as a function of the phase shift angle ϕ and the modulation index M for 2L-SPWM. b) Maximum of $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ over M.

For a more compact expression of (3.47), the term within the absolute value bars in (3.47) is defined as normalised minimum DC link capacitance under static load conditions $C_{\mathrm{dc,min,s,norm}}$:

$$C_{\mathrm{dc,min,s,norm}}(\phi, M) = \left| \sqrt{\frac{3}{2}} M \cos(\phi)(\delta_{\mathrm{nnn}}(\alpha_{\mathrm{crit}}) + \delta_{\mathrm{pnn}}(\alpha_{\mathrm{crit}})) - \sqrt{2}\cos(\alpha_{\mathrm{crit}} - \phi)\delta_{\mathrm{pnn}}(\alpha_{\mathrm{crit}}) \right| \tag{3.50}$$

With this definition, (3.47) can be written in the more compact form

$$C_{\mathrm{dc,min,s}} = C_{\mathrm{dc,min,s,norm}}(\phi, M) \cdot \frac{I_{\mathrm{conv}}}{\Delta v^{*}_{\mathrm{dc,m,s,max}} f_{\mathrm{PWM}}} \tag{3.51}$$

The normalised DC link capacitance $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ is shown in Fig. 3.10a for the complete phase shift angle range, i.e. $\phi \in [-180°, 180°]$, and for the complete linear modulation index range of 2L-SPWM, i.e. $M \in [0, \sqrt{3}/2]$. With the assumption that the inverter module uses the complete modulation index range (related to the speed range), $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ in (3.51) is replaced by the maximum of $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ in the dimension of M. This maximum is shown

Table 3.5: Coefficients of the polynomial in (3.53) for α_{crit} in radian.

Coefficient	Value	Coefficient	Value
a	0.09504	f	0.4326
b	0.009878	g	0.1607
c	−0.4479	h	0.5632
d	−0.1023	i	0.05722
e	−0.04655	j	−0.2845

in Fig. 3.10b. Fig. 3.10b shows that ϕ has a significant effect on the necessary DC link capacitance, as the maximum and minimum value of the capacitance differ by 16 %. The maximum capacitance is necessary at $\phi = \pm 90°$. An interesting result is that there is an optimal phase shift angle of $\pm 18°$ where the necessary DC link capacitance is minimal. The capacitance formula (2.19) in [39], derived for the case of $\phi = 0$, can be used as long as ϕ does not exceed $\pm 32.5°$. Beyond this value, the necessary DC link capacitance is larger than the capacitance at $\phi = 0$, and hence the equation (3.47) derived above must be used.
So far, the single-capacitor DC link topology (Fig. 3.8a) with the capacitor C_{dc} was considered. If the split-capacitor DC link topology (Fig. 3.8b) is used, the minimum required DC link capacitance under static load conditions for the upper/high capacitor $C_{\text{dc,h}}$ is given by

$$C_{\text{dc,h,min,s}} = 2 \cdot C_{\text{dc,min,s}} \tag{3.52}$$

The capacitance requirement $C_{\text{dc,min,s}}/C_{\text{dc,h,min,s}}$ for the single-/split capacitor DC link topology is used as an input parameter of the DC link module design procedure described later in section 3.2.6.

2L-OCPWM

As mentioned in section 2.3.2, the 2-level optimal clamping modulation scheme (2L-OCPWM) is a PWM scheme aiming at a switching loss reduction by clamping the phase with the highest current. This PWM scheme is considered in [39] for the case of a unity power factor ($\cos(\phi) = 1 \Leftrightarrow \phi = 0$). In this thesis, the PMW scheme 2L-OCPWM is considered for the more general case of $\phi \in [-180°, 180°]$.
A numerical analysis, analogue to the analysis performed for 2L-SPWM, is performed for 2L-OCPWM (with the single-capacitor DC link topol-

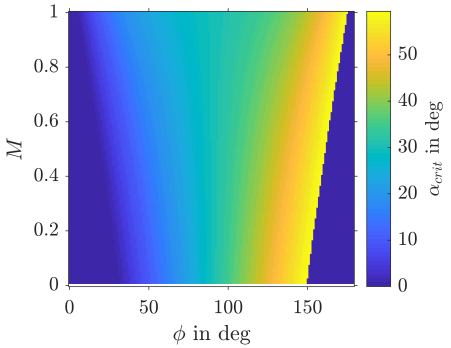


Figure 3.11: Critical reference voltage angle α_{crit} vs. M and ϕ for 2L-OCPWM.

ogy) to determine the critical reference voltage angle and the critical switching sequence which lead to the maximum DC link charge ripple and hence to the solution of (3.36). Fig. 3.11 shows the resulting critical reference voltage angle $\alpha_{\text{crit}}(\phi, M)$. This plot of $\alpha_{\text{crit}}(\phi, M)$ for 2L-OCPWM looks similar to the plot of $\alpha_{\text{crit}}(\phi, M)$ for 2L-SPWM from Fig. 3.9. However, the results are different with regard to two aspects: 1) The maximum value of M in the linear operating range is 1 for 2L-OCPWM, whereas it is $\sqrt{3}/2$ for 2L-SPWM. Therefore, the M-axis in Fig. 3.11 and the M-axis in Fig. 3.9 have different maximum values. 2) The 2D curve fitting of $\alpha_{\text{crit}}(\phi, M)$ for 2L-OCPWM (Fig. 3.11) results in a polynomial of the fourth order ($M\phi^3$), whereas the curve fitting of $\alpha_{\text{crit}}(\phi, M)$ for 2L-SPWM resulted in a polynomial of the third order (ϕ^3) for the same level of accuracy ($RMSE < 0.5\,\%$). The polynomial of the fourth order for $\alpha_{\text{crit}}(\phi, M)$ is given by

$$\alpha_{\text{crit}}(\phi, M) \approx \begin{cases} 0, & (\phi, M) \in A_1 \\ aM\phi^3 + b\phi^3 + cM\phi^2 + dM^2\phi + e\phi^2 + \\ fM\phi + gM^2 + h\phi + iM + j, & (\phi, M) \in A_2 \end{cases} \tag{3.53}$$

where the parameters a-j are given in Tab. 3.5. In (3.53), the (ϕ, M)-areas A_1 and A_2 are the same as the corresponding areas for 2L-SPWM which are defined in (3.40), except for the expression of the total (ϕ, M)-area A_{tot} from (3.40) which is replaced by

$$A_{\text{tot}} = \{\phi \in [0, \pi) \wedge M \in [0, 1]\} \tag{3.54}$$

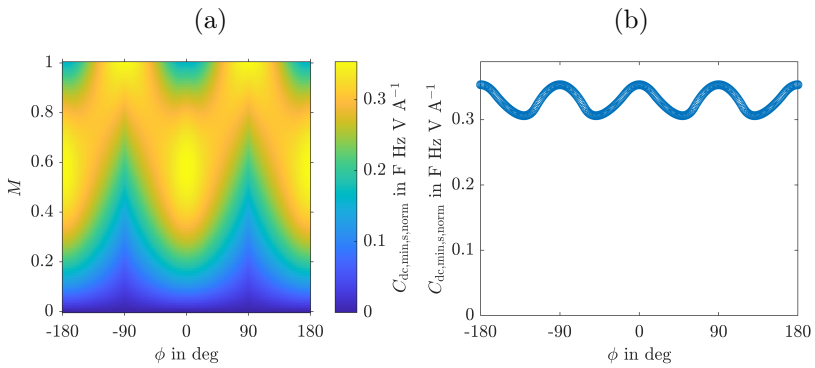


Figure 3.12: a) Normalised minimum DC link capacitance for static load conditions $C_{\mathrm{dc,min,s,norm}}$ as a function of the phase shift angle ϕ and the modulation index M for 2L-OCPWM. b) Maximum of $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ over M.

The critical switching sequence for 2L-OCPWM is (nnn)-(pnn), which is the same as for 2L-SPWM. Therefore, the minimum required DC link capacitance under static load conditions $C_{\mathrm{dc,min,s}}$ for 2L-OCPWM also results from (3.47). In addition, the more compact expression of $C_{\mathrm{dc,min,s}}$ using the normalised DC link capacitance $C_{\mathrm{dc,min,s,norm}}$ in (3.50)-(3.51) is valid for 2L-OCPWM, as well. But, instead of the duty cycle functions (3.48) and (3.49), the following functions must be evaluated at $\alpha_i = \alpha_{\mathrm{crit}}$ and inserted into (3.47) and (3.50):

$$\delta_{\mathrm{pnn}}(\alpha_i) = M \cos\left(\frac{\pi}{6} + \alpha_i\right) \tag{3.55}$$

$$\delta_{\mathrm{nnn}}(\alpha_i) = \left(1 - M \cos\left(\frac{\pi}{6} - \alpha\right)\right) f_{\mathrm{bool,nnn}}(\alpha_i, \Psi(\phi)) \tag{3.56}$$

There, $f_{\mathrm{bool,nnn}}(\alpha_i, \Psi(\phi))$ is the Boolean function that determines which of the two zero states (nnn) and (ppp) is used within a switching period T_{PWM}, as defined in (3.7) in section 3.1.2.
Analogue to Fig. 3.10a for 2L-SPWM, Fig. 3.12a shows the result for the normalised DC link capacitance $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ for 2L-OCPWM for $\phi \in [-180°, 180°]$ and for the linear modulation index range of 2L-OCPWM, i.e. $M \in [0, 1]$. Analogue to Fig. 3.10b for 2L-SPWM, Fig. 3.12b shows the maximum of $C_{\mathrm{dc,min,s,norm}}(\phi, M)$ in the dimension of M for 2L-OCPWM. This result shows that the maximum

necessary capacitance occurs at phase shift angles ϕ of 0°, ±90°, and 180°. The minimum capacitance occurs at the phase shift angles of ±50° and ±130°. The difference between both extremes is 15 % of the lower capacitance value. Following a conservative design approach, it is sufficient to dimension the DC link capacitance only for the case $\phi = 0°$ (as it is done in [39]) because of the absolute maximum of $C_{\mathrm{dc,min,s,norm}}$ at $\phi = 0$ in Fig. 3.12b. This is different compared to 2L-SPWM, for which $C_{\mathrm{dc,min,s,norm}}$ in Fig. 3.10b does not show an absolute maximum at $\phi = 0$.

3L-SPWM

For the 3L-PWM schemes 3L-SPWM and 3L-NPBPWM, the 3L DC link topology (Fig. 3.8c) is considered. This topology consists of two capacitors $C_{\mathrm{dc,p}}$ and $C_{\mathrm{dc,n}}$. As in the 2-level case, the input current $i_{\mathrm{dc,in}}$ flows from the DC source to the DC link capacitors. This current is assumed to be constant in steady state operation because the power flow into the motor is approximately constant in steady state and the DC link voltage ripple is assumed to be relatively small. The 3-level DC link has three output connections through which the currents $i_{\mathrm{dc,out,p}}$, $i_{\mathrm{dc,out,0}}$, and $i_{\mathrm{dc,out,n}}$ flow towards the motor. The currents flowing into the capacitors are denoted as $i_{\mathrm{dc,mid,p}}$ and $i_{\mathrm{dc,mid,n}}$, and the corresponding voltages are denoted as $v_{\mathrm{dc,p}}$ and $v_{\mathrm{dc,n}}$. As in the 2-level case, the DC link capacitance is dimensioned so that a maximum allowed voltage ripple in the DC link capacitors is not exceeded. However, in the 3-level case, there are two voltage ripple criteria because both the partial DC link voltages $v_{\mathrm{dc,p}}$ and $v_{\mathrm{dc,n}}$, and the total DC link voltage v_{dc} should be kept approximately constant to minimise the error between the reference and the actual inverter output voltages. These voltage ripple criteria are expressed as

$$\text{Criterion 1} : \Delta v_{\mathrm{dc,p}} \overset{!}{\leq} \Delta v^{*}_{\mathrm{dc,p,s,max}} \tag{3.57}$$

$$\text{Criterion 2} : \Delta v_{\mathrm{dc}} \overset{!}{\leq} \Delta v^{*}_{\mathrm{dc,s,max}} \tag{3.58}$$

There, $\Delta v^{*}_{\mathrm{dc,p,s,max}}$ is the reference maximum peak-to-peak ripple of the partial DC link voltage $v_{\mathrm{dc,p}}$ and $\Delta v^{*}_{\mathrm{dc,s,max}}$ is the reference maximum peak-to-peak ripple of the (total) DC link voltage v_{dc}. Analogue to (3.35), the criteria in (3.57)-(3.58) lead to the following criteria for the

DC link capacitance $C_{\mathrm{dc,p}}$:

$$\text{Criterion 1}: C_{\mathrm{dc,p}} \overset{!}{\geq} C_{\mathrm{dc,p,min,s1}} = \frac{\Delta Q_{\mathrm{p,max}}}{\Delta v^{*}_{\mathrm{dc,p,s,max}}} \tag{3.59}$$

$$\text{Criterion 2}: C_{\mathrm{dc,p}} \overset{!}{\geq} C_{\mathrm{dc,p,min,s2}} = \frac{(\Delta Q_{\mathrm{p}} + \Delta Q_{\mathrm{n}})_{\mathrm{max}}}{\Delta v^{*}_{\mathrm{dc,s,max}}} \tag{3.60}$$

where ΔQ_{p} and ΔQ_{n} denote the peak-to-peak charge ripples of the capacitors $C_{\mathrm{dc,p}}$ and $C_{\mathrm{dc,n}}$, respectively. In the following, (3.59) and (3.60) are developed into formulas that only depend on known operating parameters.

First, criterion 1 from (3.59) is considered. In order to derive the maximum charge ripple $\Delta Q_{\mathrm{p,max}}$, the current $i_{\mathrm{dc,mid,p}}$ flowing into the upper DC link capacitor $C_{\mathrm{dc,p}}$ is expressed as:

$$i_{\mathrm{dc,mid,p}} = i_{\mathrm{dc,in}} - i_{\mathrm{dc,out,p}} \tag{3.61}$$

By expressing $i_{\mathrm{dc,in}}$ as $P_{\mathrm{out}}/V_{\mathrm{dc}}$ and by inserting (3.38) for P_{out}, $i_{\mathrm{dc,in}}$ is expressed as a function of the operating point parameters M, I_{conv}, and ϕ:

$$i_{\mathrm{dc,in}} = \sqrt{\frac{3}{2}} M I_{\mathrm{conv}} \cos(\phi) \tag{3.62}$$

Finding an analytical expression for the current $i_{\mathrm{dc,out,p}}$ in (3.61) is more difficult as $i_{\mathrm{dc,out,p}}$ depends on the rapidly changing switching state of the inverter. This difficulty is solved by applying the following approach: According to [39], the voltage ripples $\Delta v_{\mathrm{dc,p}}$ and $\Delta v_{\mathrm{dc,n}}$ oscillate sinusoidally with the third harmonic frequency $3f_{\mathrm{fw}}$, when the ripple over each switching period is neglected. This is a valid approximation as long as relatively high switching frequencies are considered. In that case, it is sufficient to consider only the mean current over one switching period $\bar{i}_{\mathrm{dc,out,p}}$ instead of $i_{\mathrm{dc,out,p}}$. Due to the periodicity and half-wave symmetry of $\bar{i}_{\mathrm{dc,out,p}}$, this current must only be calculated over an α-interval that covers half a period of $\bar{i}_{\mathrm{dc,out,p}}$ (i.e. $\pi/3$) in order to know $\bar{i}_{\mathrm{dc,out,p}}$ for all possible values of $\alpha \in [0, 2\pi)$. The chosen α-interval is $[-\pi/6, \pi/6)$ because $i_{\mathrm{dc,out,p}}$ only takes on the values 0 and i_{r} in this interval (cf. Tab. 3.6), which leads to the following equation for $\bar{i}_{\mathrm{dc,out,p}}$:

$$\bar{i}_{\mathrm{dc,out,p}} = \delta_{\mathrm{p00,S1T1a}} i_{\mathrm{r}} = \sqrt{\frac{8}{3}} M I_{\mathrm{conv}} \cos(\alpha) \cos(\alpha - \phi) \tag{3.63}$$

Table 3.6: $i_{\mathrm{dc,out,p}}$ of the 3-level switching states with voltage space vector angles $\alpha \in [-\pi/6, \pi/6)$.

Switching state	$i_{\mathrm{dc,out,p}}$
000	0
pn0	i_{r}
p00	i_{r}
0nn	0
pnn	i_{r}
p0n	i_{r}

As expected, inserting $\phi = 0$ into (3.63) leads to (2.26) from [39], which shows that (3.63) is a generalisation of (2.26) from [39] to $\phi \in [-\pi, \pi]$. The middle term of (3.63), i.e. $\delta_{\mathrm{p00,S1T1a}} i_{\mathrm{r}}$, applies to the particular case that the reference vector $\vec{v}_{\mathrm{ref}}$ lies in the triangle T1 of sector I of the 3L space vector diagram (Fig. 3.3). However, the resulting term on the right side of (3.63) is the same for all cases of $\alpha \in [-\pi/6, \pi/6)$ and $M \in [0, \sqrt{3}/2]$. Using (3.61)-(3.63) and the half-wave symmetry of $\bar{i}_{\mathrm{dc,mid,p}}$, the following analytical expression for $\bar{i}_{\mathrm{dc,mid,p}}$ is derived:

$$\bar{i}_{\mathrm{dc,mid,p}} = \begin{cases} MI_{\mathrm{conv}} \left(\frac{1}{\sqrt{6}} \cos\phi - \sqrt{\frac{2}{3}} \cos\left(2\alpha - \phi\right) \right), & \alpha \in [\frac{-\pi}{6}, \frac{\pi}{6}) \\ MI_{\mathrm{conv}} \left(\frac{-1}{\sqrt{6}} \cos\phi + \sqrt{\frac{2}{3}} \cos\left(2(\alpha - \frac{\pi}{3}) - \phi\right) \right), & \alpha \in [\frac{\pi}{6}, \frac{\pi}{2}) \end{cases} \tag{3.64}$$

This expression must be inserted into the following expression for the maximum charge ripple $\Delta Q_{\mathrm{p,max}}$:

$$\Delta Q_{\mathrm{p,max}} = \left| \int_{\alpha_{0,low}}^{\alpha_{0,high}} \bar{i}_{\mathrm{dc,mid,p}}(\alpha) \frac{\mathrm{d}\alpha}{2\pi f_{\mathrm{fw}}} \right| \tag{3.65}$$

where $\alpha_{0,low}$ and $\alpha_{0,high}$ denote the zeros of $\bar{i}_{\mathrm{dc,mid,p}}(\alpha)$ which are given by

$$\begin{aligned} \alpha_{0,low} &= \frac{1}{2} \left(\phi - \mathrm{sign}(\phi) \arccos\left(\frac{\cos\left(\phi\right)}{2} \right) \right) \\ \alpha_{0,high} &= \alpha_{0,low} + \frac{\pi}{3} \end{aligned} \tag{3.66}$$

There, the sign-function is defined so that $\mathrm{sign}(0) = 1$. Inserting (3.61)-(3.66) into (3.59) and introducing the normalised DC link capacitance

$C_{\mathrm{dc,p,min,s1,norm}}(\phi, M)$ for a more compact notation leads to the following expression for $C_{\mathrm{dc,p,min,s1}}$:

$$C_{\mathrm{dc,p,min,s1}} = C_{\mathrm{dc,p,min,s1,norm}}(\phi, M) \cdot \frac{I_{\mathrm{conv}}}{f_{\mathrm{fw}} \Delta v^{*}_{\mathrm{dc,p,s,max}}} \tag{3.67}$$

Therein, the normalised DC link capacitance $C_{\mathrm{dc,p,min,s1,norm}}$ is given by

$$C_{\mathrm{dc,p,min,s1,norm}}(\phi, M) = M \left| [I_1(\alpha, \phi)]_{\alpha=\alpha_{0,low}}^{\alpha=\frac{\pi}{6}} + [I_2(\alpha, \phi)]_{\alpha=\frac{\pi}{6}}^{\alpha=\alpha_{0,high}} \right| \tag{3.68}$$

where $I_1(\alpha, \phi)$ and $I_2(\alpha, \phi)$ are auxiliary terms which result from the integral in (3.65) and which are given by

$$I_1(\alpha, \phi) = \frac{1}{2\pi\sqrt{6}} \left(\cos(\phi) \cdot \alpha - \sin(2\alpha - \phi) \right) \tag{3.69}$$

$$I_2(\alpha, \phi) = -\frac{1}{2\pi\sqrt{6}} \left(\cos(\phi) \cdot \alpha + \sin(2\alpha - \phi + \frac{\pi}{3}) \right) \tag{3.70}$$

Thus, the complete set of equations to calculate $C_{\mathrm{dc,p,min,s1,norm}}(\phi, M)$ is given by (3.66) and (3.67)-(3.70). The result for $C_{\mathrm{dc,p,min,s1,norm}}(\phi, M)$ is shown in Fig. 3.13a for the complete phase shift angle range, i.e. $\phi \in [-180°, 180°]$, and for the complete linear modulation index range of 3L-SPWM, i.e. $M \in [0, \sqrt{3}/2]$. In analogue manner to the previous sections on 2L-SPWM/2L-OCPWM, Fig. 3.13b shows the maximum values of $C_{\mathrm{dc,p,min,s1,norm}}(\phi, M)$ from Fig. 3.13a in the dimension of M. This result shows that the maximum necessary capacitance occurs at $\phi = \pm 90°$, and that the minimum capacitance occurs at $\phi = 0$. The difference between both extreme values is 46 % of the lower capacitance value. For a realistic case of $\phi = 30°$ for the considered project motor, still 15 % more capacitance is required compared to the case of $\phi = 0°$, which underlines the relevance of this analysis. Furthermore, as $C_{\mathrm{dc,p,min,s1}}$ in (3.67) is inversely proportional to f_{fw}, $C_{\mathrm{dc,p,min,s1}}$ theoretically becomes infinitely large when the motor is at standstill ($f_{\mathrm{fw}} = 0$). Therefore, the PWM scheme 3L-SPWM can only be used in combination with additional passive balancing of the DC link voltages $v_{\mathrm{dc,p}}$ and $v_{\mathrm{dc,n}}$.

For criterion 2 in (3.60), the required capacitance $C_{\mathrm{dc,p,min,s2}}(\phi, M)$ can in a similar way be expressed based on a normalised capacitance,

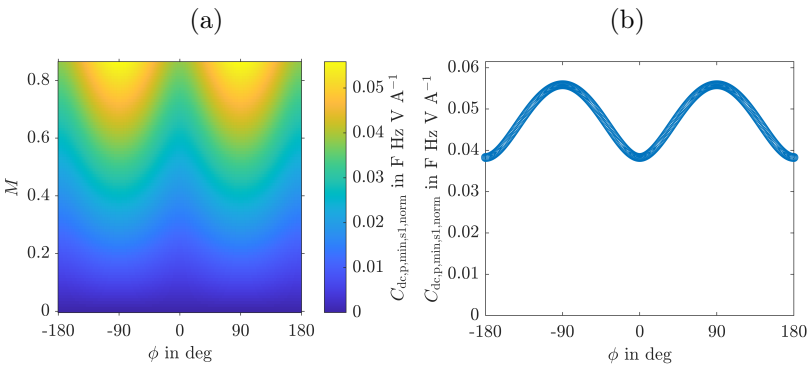


Figure 3.13: a) Normalised minimum DC link capacitance for static load conditions $C_{\mathrm{dc,p,min,s1,norm}}$ as a function of the phase shift angle ϕ and the modulation index M for 3L-SPWM. b) Maximum of $C_{\mathrm{dc,p,min,s1,norm}}(\phi, M)$ over M.

called $C_{\mathrm{dc,p,min,s2,norm}}$, which is scaled with the parameters I_{conv}, f_{PWM}, and $\Delta v^*_{\mathrm{dc,s,max}}$:

$$C_{\mathrm{dc,p,min,s2}} = C_{\mathrm{dc,p,min,s2,norm}}(\phi, M) \cdot \frac{I_{\mathrm{conv}}}{f_{\mathrm{PWM}} \Delta v^*_{\mathrm{dc,s,max}}} \tag{3.71}$$

The function $C_{\mathrm{dc,p,min,s2,norm}}(\phi, M)$ in (3.71) is calculated numerically and the result is shown in Fig. 3.14a. An analytical expression for $C_{\mathrm{dc,p,min,s2}}(\phi, M)$, analogue to (3.47) for 2L-SPWM, could not be found because the function $\alpha_{\mathrm{crit}}(\phi, M)$ is more complex for 3L-SPWM than for 2L-SPWM. However, $C_{\mathrm{dc,p,min,s2}}$ is expressed analytically for the worst case ($\phi = 0$ in Fig. 3.14b), resulting in

$$C_{\mathrm{dc,p,min,s2}} = 0.354\,\mathrm{F\,Hz\,V\,A^{-1}} \cdot \frac{I_{\mathrm{conv}}}{f_{\mathrm{PWM}} \Delta v^*_{\mathrm{dc,s,max}}}. \tag{3.72}$$

The overall minimum required DC link capacitance under static load conditions $C_{\mathrm{dc,p,min,s}}$ for 3L-SPWM corresponds to the larger required capacitance between $C_{\mathrm{dc,p,min,s1}}$ and $C_{\mathrm{dc,p,min,s2}}$:

$$C_{\mathrm{dc,p,min,s}} = \max\{C_{\mathrm{dc,p,min,s1}}, C_{\mathrm{dc,p,min,s2}}\} \tag{3.73}$$

Comparing (3.67) to (3.72) results in $C_{\mathrm{dc,p,min,s1}} > C_{\mathrm{dc,p,min,s2}}$ for typically used frequency modulation ratios ($f_{\mathrm{PWM}} \gg f_{\mathrm{fw}}$). Consequently, (3.73) typically results in $C_{\mathrm{dc,p,min,s}} = C_{\mathrm{dc,p,min,s1}}$.

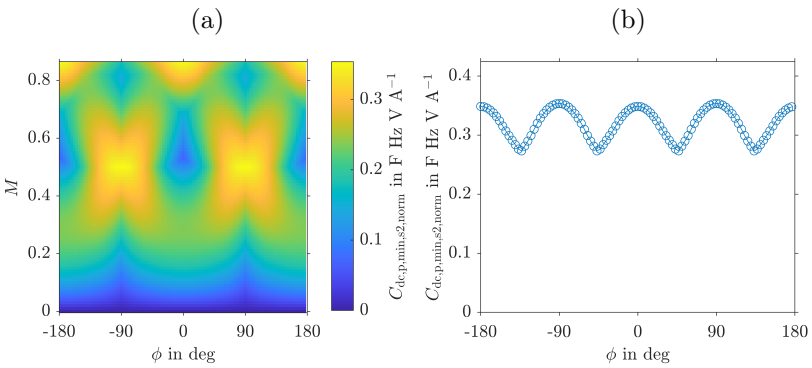


Figure 3.14: a) Normalised minimum DC link capacitance for static load conditions $C_{\mathrm{dc,p,min,s2,norm}}$ as a function of the phase shift angle ϕ and the modulation index M for 3L-SPWM. b) Maximum of $C_{\mathrm{dc,p,min,s2,norm}}(\phi, M)$ over M.

3L-NPBPWM

With the PWM scheme 3L-NPBPWM, the DC link voltages $v_{\mathrm{dc,p}}$ and $v_{\mathrm{dc,n}}$ are already balanced ($v_{\mathrm{dc,p}} \approx v_{\mathrm{dc,n}}$) through the PWM and therefore do not need to be balanced by means of the DC link capacitors. Therefore, only the total DC link voltage ripple must be limited by the DC link capacitors, which corresponds to criterion 2 in (3.60). Following the same method as for 3L-SPWM, this criterion results in the following expression for the minimum capacitance:

$$C_{\mathrm{dc,p,min,s}} = C_{\mathrm{dc,p,min,s,norm}}(\phi, M) \cdot \frac{I_{\mathrm{conv}}}{f_{\mathrm{PWM}} \Delta v^{*}_{\mathrm{dc,s,max}}} \tag{3.74}$$

The normalised capacitance $C_{\mathrm{dc,p,min,s,norm}}(\phi, M)$ in (3.74) is determined numerically and the result is shown in Fig. 3.15a for $\phi \in [-180°, 180°]$ and for the linear modulation index range of 3L-NPBPWM. This range depends on ϕ (cf. Fig. 9 of [84]), which is why Fig. 3.15a only shows capacitance values for a limited set/area of (ϕ,M)-points. Fig. 3.15b shows the maximum capacitance from Fig. 3.15a in the dimension of M, analogously to the previously considered PWM schemes. Similar to 3L-SPWM, an analytical formula for the normalised capacitance $C_{\mathrm{dc,p,min,s,norm}}$ shown in Fig. 3.15a was not found due to the complexity of the function. Instead, for a fast evaluation of (3.74) in

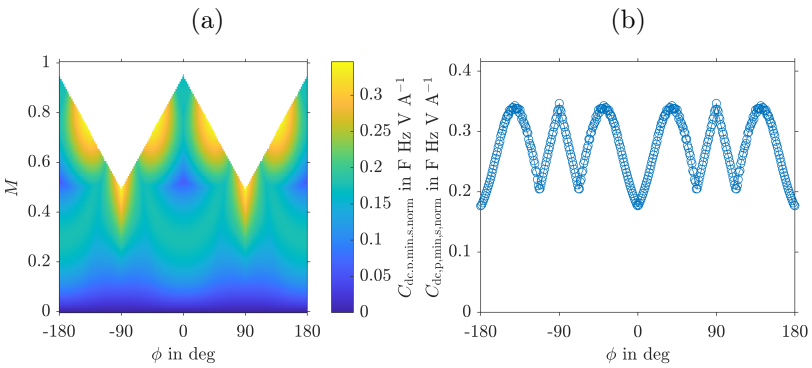


Figure 3.15: a) Normalised minimum DC link capacitance for static load conditions $C_{\mathrm{dc,p,min,s,norm}}$ as a function of the phase shift angle ϕ and the modulation index M for 3L-NPBPWM. b) Maximum of $C_{\mathrm{dc,p,min,s,norm}}(\phi, M)$ over M.

IMD design procedures, $C_{\mathrm{dc,p,min,s,norm}}(\phi, M)$ is stored in a lookup table (LUT), called C_{LUT}. Due to the symmetry of $C_{\mathrm{dc,p,min,s,norm}}(\phi, M)$ along ϕ, the LUT only needs to be stored for $\phi \in [0°, 90°]$. For any $\phi \in [-180°, 180°]$, $C_{\mathrm{dc,p,min,s,norm}}(\phi, M)$ can then be evaluated with

$$C_{\mathrm{dc,p,min,s,norm}}(\phi, M) = \begin{cases} C_{\mathrm{LUT}}(\phi + 180°, M), & \phi \in [-180^{\circ}, -90°] \\ C_{\mathrm{LUT}}(-\phi, M), & \phi \in [-90°, 0] \\ C_{\mathrm{LUT}}(\phi, M), & \phi \in [0, 90°] \\ C_{\mathrm{LUT}}(180° - \phi, M), & \phi \in [90°, 180°] \end{cases} \tag{3.75}$$

3.2.4 Capacitance Requirement for Dynamic Load

If cables are used to connect the IMD to the DC source, load steps lead to an additional ripple of the DC link voltage due to the resonance of the cable inductance with the DC link capacitance. To limit this voltage ripple to a given reference maximum voltage ripple $\Delta v^{*}_{\mathrm{dc,d,max}}$, a minimum DC link capacitance under dynamic load conditions is required. A model for calculating this capacitance is presented in the following, first for the considered inverter topologies that are based on 2L-modules (2L, SPB, and N_{m}P-2L), and subsequently for the considered 3L-inverter topologies (3L-NPC and 3L-TT).

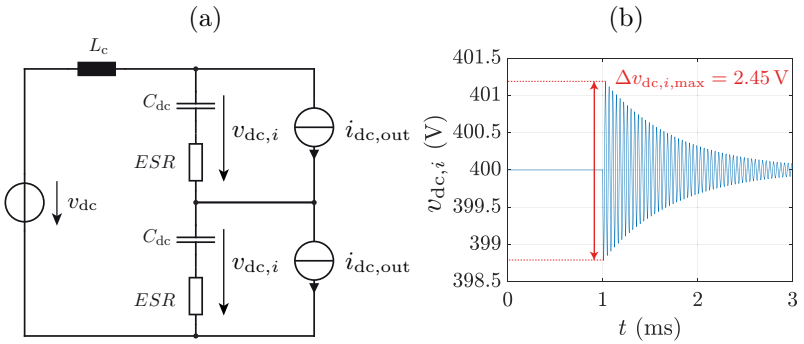


Figure 3.16: a) Model of a 2-module SPB-C with converter modules modelled as current sources. b) Module DC link voltage $v_{\mathrm{dc},i}$ for an exemplary load step of $\Delta i_{\mathrm{dc,out}} = 2\,\mathrm{A}$ at $t = 1\,\mathrm{ms}$ with $L_c = 7.5\,\mu\mathrm{H}$, $C_{\mathrm{dc}} = 10\,\mu\mathrm{F}$, $ESR = 10\,\mathrm{m}\Omega$, and $v_{\mathrm{dc}} = 800\,\mathrm{V}$.

2L-based Inverter Topologies (2L, SPB, N_{m}P-2L)

For the SPB-inverter topology, the effect of a load step on the DC link voltage is analysed using a simplified model of an SPB-inverter with for example 2 SPB-modules ($N_{\mathrm{m}} = 2$) which is shown in Fig. 3.16a. There, the SPB-modules are modelled with controlled current sources $i_{\mathrm{dc,out}}$. The PWM-induced current ripple is neglected so that $i_{\mathrm{dc,out}} = {}^{3}\!/_{4} M \hat{i}_{\mathrm{conv}} \cos(\phi)$. The circuit in Fig. 3.16a is simulated with the exemplary parameters $\Delta i_{\mathrm{dc,out}} = 2\,\mathrm{A}$, $L_c = 7.5\,\mu\mathrm{H}$, $C_{\mathrm{dc}} = 10\,\mu\mathrm{H}$, and $ESR = 10\,\mathrm{m}\Omega$. The load step $\Delta i_{\mathrm{dc,out}}$ is applied at $t = 1\,\mathrm{ms}$. The simulation result for the module DC link voltage $v_{\mathrm{dc},i}$ is shown in Fig. 3.16b. This result shows a constant voltage up to the time $t = 1\,\mathrm{ms}$, after which the load step causes a voltage ripple in form of a damped oscillation with a maximum (peak-to-peak) amplitude $\Delta v_{\mathrm{dc},i,\mathrm{max}}$ of 2.45 V. The simplified model of the SPB-inverter with 2 modules in Fig. 3.16a is generalised to N_{m} modules and then used to derive an analytical formula for the minimum module DC link capacitance $C_{\mathrm{dc,min,d}}$ that is required to limit the (total) DC link voltage ripple Δv_{dc} to the reference maximum voltage ripple $\Delta v^{*}_{\mathrm{dc,d,max}}$ for a maximum driven load step $\Delta i_{\mathrm{dc,out,max}}$. This derivation is based on the Laplace transforma-

tion and results in

$$C_{\mathrm{dc,min,d}} = \frac{4N_{\mathrm{m}}L_{\mathrm{c}}\Delta i_{\mathrm{dc,out,max}}^2}{\Delta v_{\mathrm{dc,d,max}}^{*\,2}}. \tag{3.76}$$

For the N_{m}P-2L-inverter topology, an analogue derivation results in the same equation. For the 2L-inverter topology $C_{\mathrm{dc,min,d}}$ results from (3.76) with $N_{\mathrm{m}} = 1$ as the 2L-inverter corresponds to an SPB-inverter with one module. Thus, (3.76) applies to all of the considered 2L-based inverter topologies (2L, SPB, N_{m}P-2L).
If an alternative modelling approach is used in which a maximum reference voltage ripple for the module DC link voltages $\Delta v_{\mathrm{dc,m,d,max}}^*$ is imposed instead of the maximum reference voltage ripple for the total DC link voltage $\Delta v_{\mathrm{dc,d,max}}^*$ considered so far, $C_{\mathrm{dc,min,d}}$ for the SPB-topology is expressed by inserting $\Delta v_{\mathrm{dc,d,max}}^* = N_{\mathrm{m}} \cdot \Delta v_{\mathrm{dc,m,d,max}}^*$ into (3.76), which results in

$$C_{\mathrm{dc,min,d}} = \frac{4L_{\mathrm{c}}\Delta i_{\mathrm{dc,out,max}}^2}{N_{\mathrm{m}}\Delta v_{\mathrm{dc,m,d,max}}^{*\,2}}. \tag{3.77}$$

For the N_{m}P-2L-inverter topology, the module DC link voltage is equal to the total DC link voltage, hence $C_{\mathrm{dc,min,d}}$ for the N_{m}P-2L-topology still results from (3.76) by replacing $\Delta v_{\mathrm{dc,d,max}}^*$ with $\Delta v_{\mathrm{dc,m,d,max}}^*$.
The capacitance requirements $C_{\mathrm{dc,min,d}}$ from (3.76) and (3.77) are based on the single-capacitor DC link topology (Fig. 3.8a). If the split-capacitor DC link topology (Fig. 3.8b) is used, the minimum required capacitance of the upper/lower capacitor $C_{\mathrm{dc,h}}/C_{\mathrm{dc,l}}$ under dynamic load conditions is called $C_{\mathrm{dc,h,min,d}}$ and results from (3.76)/(3.77), where only a factor of 2 must be applied as in (3.52). Only the subscript s (for static) in (3.52) needs to be replaced by d (for dynamic).

3L-Inverter Topologies (3L-NPC, 3L-TT)

For the considered 3L-inverter topologies (3L-NPC and 3L-TT), the capacitance requirement for dynamic load conditions is derived in a similar way as for the 2L-based inverter topologies: Assuming that DC link balancing is ensured (actively by the PWM or passively), the 3L-inverters are modelled as a controlled current source $i_{\mathrm{dc,out,p}}$ between the positive and the negative DC link rail. As in the 2L-case, the PWM-induced current ripple is neglected so that $i_{\mathrm{dc,out,p}} = {}^3\!/_4 M \hat{i}_{\mathrm{conv}} \cos(\phi)$.

With this inverter model, the minimum DC link capacitance that is required to limit the (total) DC link voltage ripple Δv_{dc} to the reference maximum voltage ripple $\Delta v^*_{\mathrm{dc,d,max}}$ for a maximum driven load step $\Delta i_{\mathrm{dc,out,p,max}}$ results in

$$C_{\mathrm{dc,p,min,d}} = \frac{8 L_{\mathrm{c}} \Delta i^2_{\mathrm{dc,out,p,max}}}{\Delta v^{*\,2}_{\mathrm{dc,d,max}}}. \tag{3.78}$$

3.2.5 RMS Current Requirement

The DC link capacitors must withstand a certain RMS current without overheating, which is referred to as RMS current requirement. For this requirement, the RMS current and the maximum allowed capacitor temperature must be specified. In this section, a formula for the RMS current is given. The maximum allowed temperature is considered later in section 3.2.6.

For the considered 2L-based inverter topologies (2L, SPB, and N_{m}P-2L), the RMS value of the current $i_{\mathrm{dc,mid}}$ that is flowing into the DC link capacitor of one 2L-inverter module (Fig. 3.8a/b) is calculated based on the following equation that is based on (28) from [85]:

$$I_{\mathrm{dc,mid}} = I_{\mathrm{conv}} \sqrt{2 \left(\frac{2}{\sqrt{3}} M \right) \left(\frac{\sqrt{3}}{4\pi} + \cos\phi^2 \left(\frac{\sqrt{3}}{\pi} - \frac{9}{16} \left(\frac{2}{\sqrt{3}} M \right) \right) \right)} \tag{3.79}$$

There, the factor $2/\sqrt{3}$ in front of M is not given in [85], but is used here to account for the different modulation index definitions used in [85] and in this thesis.

The formula in (3.79) is equally valid for both considered 2L-PWM schemes (2L-SPWM, 2L-OCPWM). This can be explained by the fact that these PWM schemes only differ in the durations of the zero states (nnn) and (ppp) both of which lead to the same current $i_{\mathrm{dc,out}}$ flowing out of the DC link and hence to the same capacitor current $i_{\mathrm{dc,mid}}$, as shown in Tab. 3.3.

For the considered 3L-PWM schemes (3L-SPWM, 3L-NPBPWM), the RMS current $I_{\mathrm{dc,mid,p}}$ flowing into the DC link capacitor $C_{\mathrm{dc,p}}$ of the 3L DC link (Fig. 3.8c) can also be calculated with (3.79). This was verified in a numerical calculation of $I_{\mathrm{dc,mid,p}}(\phi, M)$, resulting in a good agreement with the currents predicted with (3.79).

3.2.6 DC Link Capacitor Selection/Design

Based on the DC link requirements described in the previous sections 3.2.2-3.2.5, a DC link capacitor can be either selected from a series of existing DC link capacitors or optimally designed, where this section focuses on the latter. In this section, a procedure for the optimal design of a so-called DC link module is described. This procedure minimises the axial capacitor height for a given footprint area in order to minimise the inverter volume and the overall system/IMD volume. With regard to the DC link capacitor technology, film capacitors are considered as they are well suited for the high temperatures occurring in IMDs [8]. This section is divided into two parts: In the first part, the requirements from the previous sections 3.2.2-3.2.5 are summarised which serve as input parameters for the DC link capacitor design. In the second part, the developed DC link module design procedure is described which results in the DC link capacitor volume and (axial) height.

Summary of the DC Link Requirements from the Previous Sections

The DC link requirements resulting from the previous sections 3.2.2-3.2.5 are summarised below:

- Requirements for the capacitor C_{dc} of one 2L-inverter module of the considered 2L-based inverter topologies (2L, SPB, N_{m}P-2L) including the single-capacitor DC link topology: $V_{\mathrm{dc,min}}$, $C_{\mathrm{dc,min,s}}$, $C_{\mathrm{dc,min,d}}$, $I_{\mathrm{dc,mid}}$
- Requirements for the capacitor $C_{\mathrm{dc,h}}$ of one 2L-inverter module of the considered 2L-based inverter topologies (2L, SPB, N_{m}P-2L) including the split-capacitor DC link topology: $V_{\mathrm{dc,h,min}}$, $C_{\mathrm{dc,h,min,s}}$, $C_{\mathrm{dc,h,min,d}}$, $I_{\mathrm{dc,mid}}$
- Requirements for the capacitor $C_{\mathrm{dc,p}}$ of the considered 3L-inverter topologies (3L-NPC and 3L-TT): $V_{\mathrm{dc,p,min}}$, $C_{\mathrm{dc,p,min,s}}$, $C_{\mathrm{dc,p,min,d}}$, $I_{\mathrm{dc,mid,p}}$

Furthermore, the capacitance requirements under static load conditions ($C_{\mathrm{dc,min,s}}/C_{\mathrm{dc,h,min,s}}/C_{\mathrm{dc,p,min,s}}$) and the capacitance requirements under dynamic load conditions ($C_{\mathrm{dc,min,d}}/C_{\mathrm{dc,h,min,d}}/\ C_{\mathrm{dc,p,min,d}}$) are summarised to the (overall) voltage ripple related capacitance requirements

$C_{\mathrm{dc,min,v}}/C_{\mathrm{dc,h,min,v}}/\ C_{\mathrm{dc,p,min,v}}$ with

$$C_{\mathrm{dc,min,v}} = \max\{C_{\mathrm{dc,min,s}}, C_{\mathrm{dc,min,d}}\} \tag{3.80}$$

$$C_{\mathrm{dc,h,min,v}} = \max\{C_{\mathrm{dc,h,min,s}}, C_{\mathrm{dc,h,min,d}}\} \tag{3.81}$$

$$C_{\mathrm{dc,p,min,v}} = \max\{C_{\mathrm{dc,p,min,s}}, C_{\mathrm{dc,p,min,d}}\}. \tag{3.82}$$

Thus, the requirements for the capacitors $C_{\mathrm{dc}}/C_{\mathrm{dc,h}}/C_{\mathrm{dc,p}}$ can be further summarised as follows:

- Requirements for C_{dc}: $V_{\mathrm{dc,min}}$, $C_{\mathrm{dc,min,v}}$, $I_{\mathrm{dc,mid}}$
- Requirements for $C_{\mathrm{dc,h}}$: $V_{\mathrm{dc,h,min}}$, $C_{\mathrm{dc,h,min,v}}$, $I_{\mathrm{dc,mid}}$
- Requirements for $C_{\mathrm{dc,p}}$: $V_{\mathrm{dc,p,min}}$, $C_{\mathrm{dc,p,min,v}}$, $I_{\mathrm{dc,mid,p}}$

These requirements are input parameters of the DC link module design procedure that is described in the following part.

DC Link Module Design Procedure

The goal of the DC link design procedure is to calculate the minimum required axial height of the DC link capacitor $C_{\mathrm{dc}}/C_{\mathrm{dc,h}}/C_{\mathrm{dc,p}}$ and the corresponding capacitor volume. This is achieved by means of a general (topology-independent) DC link module design procedure. A DC link module is defined as a DC link capacitor on a PCB segment shaped like an annulus segment of inner radius $r_{\mathrm{s,i}}$, outer radius $r_{\mathrm{s,o}}$, and angle $\alpha_{\mathrm{s,c,mod}}$, which is shown schematically for an exemplary 3-module SPB-C in Fig. 3.17. The capacitance of a DC link module is in general referred to as $C_{\mathrm{dc,mod}}$. The different steps of the DC link module design procedure are shown in Fig. 3.18 and are explained in the following.
In step S1, five sets of input parameters are defined: 1) The minimum required rated operating voltage $V_{\mathrm{dc,mod,min}}$. 2) The minimum required capacitance $C_{\mathrm{dc,mod,min,v}}$ to limit the voltage ripple. 3) Parameters of the RMS current requirement: The maximum temperature difference between the capacitor and the heat sink should be limited to $\Delta T_{\mathrm{c-hs,max}}$ for an RMS current of $I_{\mathrm{dc,mod}}$. The frequency content of the RMS current is approximated by the major frequency component $f_{\mathrm{Irms}} \approx f_{\mathrm{PWM}}$. 4) Parameters of the spatial requirement: The capacitor should fit onto a PCB segment shaped like an annulus segment of inner radius $r_{\mathrm{s,i}}$, outer radius $r_{\mathrm{s,o}}$, and angle $\alpha_{\mathrm{s,c,mod}}$. 5) Parameters of a selected series of DC link capacitors: Coefficients $k_{\mathrm{vol,1}}$-$k_{\mathrm{vol,4}}$ for the capacitor

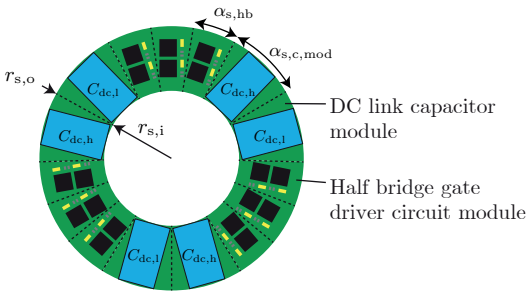


Figure 3.17: Schematic representation of the power PCB (top-side/motor-side) of a 3-module SPB-C with the split-capacitor DC link topology, resulting in six DC link capacitor modules.

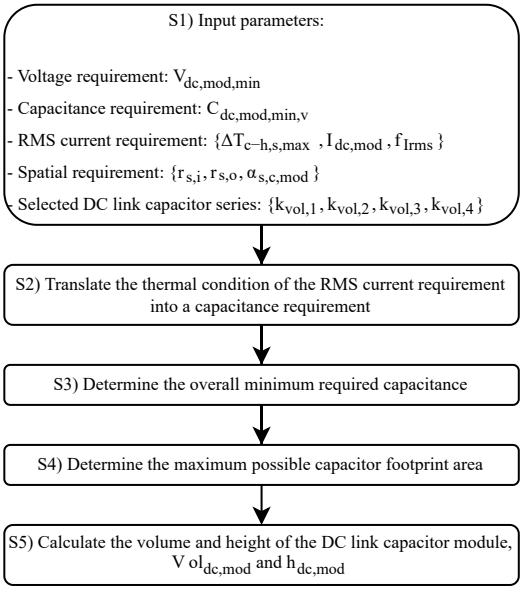


Figure 3.18: DC link module design procedure.

volume formula given later in this section.

In step S2, the thermal condition of the RMS current requirement

$$\Delta T_{\mathrm{c-hs}} \overset{!}{\leq} \Delta T_{\mathrm{c-hs,max}} \tag{3.83}$$

is translated into another capacitance requirement given by

$$\begin{aligned} C_{\mathrm{dc,mod}} \overset{!}{\geq} C_{\mathrm{dc,mod,min,th}}(&I_{\mathrm{dc,mod}}, f_{\mathrm{Irms}}, V_{\mathrm{dc,mod,min}}, \\ &\Delta T_{\mathrm{c-hs,max}}, r_{\mathrm{s,i}}, r_{\mathrm{s,o}}, \alpha_{\mathrm{s,c,mod}}), \end{aligned} \tag{3.84}$$

where $C_{\mathrm{dc,mod,min,th}}$ is numerically determined based on data sheet values of a selected capacitor series.
In step S3, the overall minimum required capacitance $C_{\mathrm{dc,mod,min}}$, and hence the designed capacitance $C_{\mathrm{dc,mod}}$, is determined with

$$C_{\mathrm{dc,mod}} = C_{\mathrm{dc,mod,min}} = \max\{C_{\mathrm{dc,mod,min,v}}, C_{\mathrm{dc,mod,min,th}}\}. \tag{3.85}$$

In step S4, the surface area of the capacitor footprint $A_{\mathrm{dc,mod}}$ is determined with

$$A_{\mathrm{dc,mod}} = A_{\mathrm{rect,max}}(\alpha_{\mathrm{s,c,mod}}, r_{\mathrm{s,i}}, r_{\mathrm{s,o}}), \tag{3.86}$$

where $A_{\mathrm{rect,max}}$ is the maximum possible rectangular surface area that fits into an annulus segment with the inner radius $r_{\mathrm{s,i}}$, the outer radius $r_{\mathrm{s,o}}$, and the segment angle $\alpha_{\mathrm{s,c,mod}}$. This geometrical problem is solved with a semi-analytical/numerical approach.
In step S5, the volume of the DC link module capacitor is calculated with the following equation from [39]:

$$\begin{aligned} Vol_{\mathrm{dc,mod}}(C_{\mathrm{dc,mod}}, V_{\mathrm{dc,mod}}) = {} & k_{\mathrm{vol,1}} C_{\mathrm{dc,mod}} V_{\mathrm{dc,mod}}^2 \\ & + k_{\mathrm{vol,2}} C_{\mathrm{dc,mod}} V_{\mathrm{dc,mod}} \\ & + k_{\mathrm{vol,3}} V_{\mathrm{dc,mod}} + k_{\mathrm{vol,4}} \end{aligned} \tag{3.87}$$

There, the coefficients $k_{\mathrm{vol,1}}$-$k_{\mathrm{vol,4}}$ are determined from a curve fitting of the capacitor volume against the capacitance and rated capacitor voltage from the data sheet of a selected DC link capacitor series. Based on $Vol_{\mathrm{dc,mod}}$ calculated with (3.87) and $A_{\mathrm{dc,mod}}$ calculated with (3.86), the (axial) height of the capacitor results in

$$h_{\mathrm{dc,mod}} = \frac{Vol_{\mathrm{dc,mod}}}{A_{\mathrm{dc,mod}}}. \tag{3.88}$$

This DC link module design procedure is applied to the dimensioning of the capacitor $C_{\mathrm{dc}}/C_{\mathrm{dc,h}}/C_{\mathrm{dc,p}}$ by parametrising the input parameters (from step S1) $V_{\mathrm{dc,mod,min}}$, $C_{\mathrm{dc,mod,min,v}}$, and $I_{\mathrm{dc,mod}}$ with the corresponding requirements of $C_{\mathrm{dc}}/C_{\mathrm{dc,h}}/C_{\mathrm{dc,p}}$ which were summarised in the previous part of this subsection.
The DC link capacitor height $h_{\mathrm{dc,mod}}$ resulting from the DC link module design procedure serves as an input parameter of the IMD volume model which is described in section 3.11.

3.3 Semiconductor Conduction Loss Model

In this section, a semiconductor conduction loss model is presented which can be used in IMD design procedures such as the IMD design procedures presented in chapter 4. This section is divided into three parts: First, a summary of the model approach is given. Then, the used definition of the *chip size* is given. In the last part, the model is explained in detail using the model equations.

3.3.1 Summary of the Model Approach

The semiconductor conduction loss model presented here is based on the model from [86] but uses a different scaling of the $R_{\mathrm{ds,on}}$. Instead of scaling the $R_{\mathrm{ds,on}}$ with the chip area as in [86], $R_{\mathrm{ds,on}} \propto {}^{1}/_{I_{\mathrm{r}}}$ is assumed, where I_{r} is the rated current of a semiconductor device, and I_{r} is scaled with the relative semiconductor cost $K_{\mathrm{sc,rel}}$.
The motivation for this modification of the approach in [86] is that the chip area usually serves as a qualitative indicator for the chip cost, but the chip cost is explicitly considered in this thesis. In addition, the current rating is provided in the data sheets of semiconductor devices, which is typically not the case for the chip area.

3.3.2 Definition of the *Chip Size*

In this thesis, the term *chip size* is used as an abstract/collective term for three closely related quantities which are the chip area, the chip cost, and the rated chip current I_{r}. As the chip area is proportional to the chip cost [86], and as I_{r} increases with the chip cost (cf. 4.1.3), an increase in any of the three mentioned quantities leads to an increase in

the other two quantities. Therefore, any of these three quantities can be used as a chip size indicator. The model in [86] uses the chip area as chip size indicator, whereas the model presented here uses the chip cost and the rated current, which is explained more in detail in the following section by means of the model equations.

3.3.3 Model Equations

The following equations from [86] are used for calculating the conduction losses of the i-th power semiconductor device of any considered inverter topology, considering MOSFETs, HEMTs, IGBTs, and diodes:

$$P_{\mathrm{cond},i,\mathrm{MOSFET/HEMT}} = R_{\mathrm{ds,on},i} \cdot I^2 \tag{3.89}$$

$$P_{\mathrm{cond},i,\mathrm{IGBT}} = V_{\mathrm{f,T},i} \cdot I + R_{\mathrm{on,T},i} \cdot I^2 \tag{3.90}$$

$$P_{\mathrm{cond},i,\mathrm{diode}} = V_{\mathrm{f,D},i} \cdot I + R_{\mathrm{on,D},i} \cdot I^2 \tag{3.91}$$

All on-resistances in the equations above are in general referred to as $R_{\mathrm{ds,on},i}$ in the following. These on-resistances are made temperature dependent and chip size/cost dependent with the following formula which is different to the equation for $R_{\mathrm{ds,on}}$ used in [86]:

$$R_{\mathrm{ds,on},i} = \frac{1}{sf_i} \left(R_{\mathrm{ds,on,25°C},i} + (T_{\mathrm{jct},i} - 25) \cdot \left(\mathrm{d}R_{\mathrm{ds,on}} / \mathrm{d}T_{\mathrm{jct}} \right)_i \right) \tag{3.92}$$

Therein, the parameters $R_{\mathrm{ds,on,25°C},i}$ and $\left(\mathrm{d}R_{\mathrm{ds,on}} / \mathrm{d}T_{\mathrm{jct}} \right)_i$ are taken from the data sheet of a reference semiconductor device. The junction temperature $T_{\mathrm{jct},i}$ in (3.92) can for example be calculated with the thermal IMD model described in section 3.9. The parameter sf_i in (3.92) is referred to as (device specific) chip size scaling factor and is defined as

$$sf_i = \frac{I_{\mathrm{r},i}}{I_{\mathrm{r,ref},i}}, \tag{3.93}$$

where $I_{\mathrm{r},i}$ is the rated current of the scaled semiconductor device and $I_{\mathrm{r,ref},i}$ is the rated current of the corresponding reference device. The reference device is selected as the semiconductor device with the highest rated current from a series of available devices with the same package. In general, this leads to different values for $I_{\mathrm{r,ref},i}$ for different types of semiconductor devices within one topology (e.g. for the transistors and diodes in the 3L-NPC-inverter topology). In order to scale all

semiconductor devices with a single scaling factor, a universal chip size scaling factor sf_{univ} is defined as

$$sf_{\mathrm{univ}} = \frac{I_{\mathrm{r,univ}}}{I_{\mathrm{r,ref,univ}}}. \tag{3.94}$$

Therein, $I_{\mathrm{r,ref,univ}}$ is a universal reference rated current (of a virtual reference device) that is arbitrarily chosen, and $I_{\mathrm{r,univ}}$ is a universal rated current that all semiconductor devices of a considered inverter topology are scaled to by setting $I_{\mathrm{r},i} = I_{\mathrm{r,univ}}$ and by inserting (3.94) into (3.93). This results in the following expression for the device specific chip size scaling factor:

$$sf_i = sf_{\mathrm{univ}} \cdot \frac{I_{\mathrm{r,ref,univ}}}{I_{\mathrm{r,ref},i}}. \tag{3.95}$$

It must be noted that, with this universal chip size scaling, only the total chip size of an inverter can be optimised but not the chip size distribution among the different devices of an inverter. The motivation for this universal chip size scaling is to reduce the number of free design parameters in order to keep the optimisation run time within reasonable limits.

So far, the conduction losses are dependent on the junction temperature $T_{\mathrm{jct},i}$ and on the universal rated current $I_{\mathrm{r,univ}}$. In a next step, the latter is made dependent on the (total) semiconductor cost of an inverter K_{sc}. To do so, K_{sc} is generally (for all considered inverter topologies) expressed as

$$K_{\mathrm{sc}}(I_{\mathrm{r,univ}}) = \sum_{j}^{N_{\mathrm{sc,t}}} N_{\mathrm{sc},j} \cdot K_{\mathrm{sc},j,1}(I_{\mathrm{r}})|_{I_{\mathrm{r}}=I_{\mathrm{r,univ}}} \cdot k_{\mathrm{o}}(N_{\mathrm{o}}), \tag{3.96}$$

where $N_{\mathrm{sc,t}}$ is the number of different types of semiconductor devices in the considered inverter topology. For example, a 3L-NPC-inverter, in which the switch-diode units SDU_i (Fig. 2.19) are MOSFETs, has two different types of semiconductors ($\mathrm{S_{p,1}}$ and $\mathrm{D_{p,5}}$), hence $N_{\mathrm{sc,t}} = 2$. Furthermore, $N_{\mathrm{sc},j}$ in (3.96) is the number of semiconductor devices of the j-th device type in the considered topology, and $K_{\mathrm{sc},j,1}(I_{\mathrm{r}})$ is the cost of one semiconductor device of the j-th device type, scaled to I_{r}. The factor $k_{\mathrm{o}}(N_{\mathrm{o}})$ in (3.96) accounts for an order volume related cost decrease, where N_{o} is the number of ordered devices. The cost study of semiconductor devices, which is presented later in section 4.1.3 (Fig.

4.7), shows that $K_{\mathrm{sc},j,1}(I_\mathrm{r})$ can be approximated as

$$K_{\mathrm{sc},j,1}(I_\mathrm{r}) = a_j \cdot I_\mathrm{r} + b_j. \tag{3.97}$$

Inserting (3.97) into (3.96) and solving for $I_{\mathrm{r,univ}}$ results in the following expression for $I_{\mathrm{r,univ}}$ as a function of the semiconductor cost:

$$I_{\mathrm{r,univ}}(K_\mathrm{sc}) = \frac{{}^{K_\mathrm{sc}}/_{k_\mathrm{o}} - \sum_j^{N_\mathrm{sc,t}} b_j \cdot N_{\mathrm{sc},j}}{\sum_{j=1}^{N_\mathrm{sc,t}} a_j \cdot N_{\mathrm{sc},j}}. \tag{3.98}$$

This expression is inserted for $I_{\mathrm{r,univ}}$ in the definition of the universal chip size scaling factor sf_univ in (3.94) which then also depends on the semiconductor cost. Finally, to obtain a model that is based on relative cost instead of absolute cost, the relative semiconductor cost is defined as

$$K_{\mathrm{sc,rel}} = \frac{K_\mathrm{sc}}{K_{\mathrm{sc,ref}}}, \tag{3.99}$$

where $K_{\mathrm{sc,ref}}$ is the semiconductor cost of a reference IMD which in general can be arbitrarily defined for comparison purposes.
Overall, (3.89)-(3.99) constitute the model for the conduction losses of one semiconductor device $P_{\mathrm{cond},i}$. The total inverter conduction losses P_cond simply result from the sum over $P_{\mathrm{cond},i}$, where symmetries in the operating conditions of the semiconductor devices are used to reduce the calculation effort. For the mentioned example of the 3L-NPC-inverter, it is sufficient to calculate the conduction losses for the semiconductor devices $\mathrm{S_{p,1}}$, $\mathrm{S_{p,2}}$, and $\mathrm{D_{p,5}}$ (Fig. 2.19).

3.4 Semiconductor Switching Loss Model

In this section, a semiconductor switching loss model for the inverter topologies selected in section 2.2.2 is presented which can be used in IMD design procedures such as the IMD design procedures described in chapter 4.
In this section, the terms "semiconductor device"/"switch"/"diode" without any indication as reference device, refer to the *effective* semiconductor device/switch/diode, as defined in section 2.2.2. This definition allows for a generic formulation of the model which includes all types of switch-diode units defined in Fig. 2.20.
This section is divided into the following parts: First a summary of the

model approach is given in section 3.4.1. Then, the model is explained in detail in terms of the model equations in section 3.4.2. Finally, topology-specific parameters, which are required to apply the switching loss model to the considered inverter topologies (2L, 3L-NPC, 3L-TT, SPB, N_mP-2L) are presented in section 3.4.3.

3.4.1 Summary of the Model Approach

For the considered 2L-based inverter topologies (2L, SPB, N_mP-2L), only one 2L-inverter module is evaluated based on the switching loss model from [83, 86] which includes a scaling of switching energies with the switched current and with the switched voltage. For a 2L-inverter module, the four switching energies $E_{\mathrm{S}_1,\mathrm{on}}$, $E_{\mathrm{S}_1,\mathrm{off}}$, $E_{\mathrm{D}_1,\mathrm{on}}$, $E_{\mathrm{D}_1,\mathrm{off}}$ are considered which are the turn-on/-off energies of a switch-diode unit in a 2L-inverter half bridge. These switching energies (except for $E_{\mathrm{D}_1,\mathrm{on}} \approx 0$) are typically given in data sheets of the considered semiconductor devices.
For the 3L-inverter topologies (3L-NPC, 3L-TT), more than four switching energies are considered due to the larger number of possible switching transition types and semiconductor devices [87, 88]. In [87], the switching losses of a 3L-NPC-converter are determined for all possible transitions between switching states. In the switching loss model presented here, this concept from [87] is used and generalised to all considered inverter topologies. The equations of this general switching loss model are presented in the following section.

3.4.2 Model Equations

The total switching losses of an inverter with any of the considered inverter topologies are given by

$$P_\mathrm{sw} = 6 \cdot N_\mathrm{m} \sum_i P_{\mathrm{sw},SD_i}. \tag{3.100}$$

There, P_{sw,SD_i} are the switching losses occurring in the semiconductor device SD_i, and N_m is the number of 3-phase modules of the considered inverter topology. Due to the symmetries in the considered inverter topologies and in the switched current waveforms (assuming a symmetrical load), a separate calculation of the switching losses for each semiconductor device of an inverter is not necessary. Therefore,

the set of effective semiconductor devices SD_i to be considered in the summation in (3.100) corresponds to a reduced set of semiconductors. This reduced set of semiconductors depends on the inverter topology and is specified for all considered inverter topologies later in section 3.4.3. What these topology-specific sets of semiconductor devices have in common, is that they include one sixth of all semiconductor devices per 3-phase inverter module, which explains the factor 6 in (3.100). The switching losses P_{sw,SD_i} in (3.100) result from

$$P_{\mathrm{sw},SD_i} = f_{\mathrm{fw}} \cdot \sum_j \sum_k E_{SD_i,\mathrm{ST}_j}(t_{k,j}). \tag{3.101}$$

There, $f_{\mathrm{fw}} = {}^1/_{T_{\mathrm{fw}}}$ is the fundamental frequency, and $E_{SD_i,\mathrm{ST}_j}(t_{k,j})$ is the switching energy that is dissipated in the semiconductor device SD_i due to the so-called switching transition type ST_j at the time instant $t_{k,j}$. The set of index values j to be considered in the outer summation in (3.101) corresponds to the set of switching transition types ST_j that cause losses in the semiconductor device SD_i. This set depends on the inverter topology and is specified for all considered inverter topologies later in section 3.4.3. The set of index values k to be considered in the inner summation in (3.101) corresponds to the set of time instants in which the switching transitions of the switching transition type ST_j occur within one fundamental period. These time instants can be determined from the half bridge switching signals that result from the PWM model described in section 3.1.
The switching energies $E_{SD_i,\mathrm{ST}_j}(t_{k,j})$ in (3.101) result from a scaling of so-called *topology-specific reference switching energies* $E_{SD_i,\mathrm{ST}_j,0}$ with the switched current i_{SD_i} and the module DC link voltage $V_{\mathrm{dc,m}}$:

$$E_{SD_i,\mathrm{ST}_j}(t_{k,j}) = E_{SD_i,\mathrm{ST}_j,0} \cdot \frac{i_{SD_i}(t_{k,j})}{I_0} \cdot \frac{V_{\mathrm{dc,m}}}{V_{\mathrm{dc,mod},0}}. \tag{3.102}$$

There, I_0 and $V_{\mathrm{dc,mod},0}$ are the reference switched current and the reference module DC link voltage of the topology-specific reference energies $E_{SD_i,\mathrm{ST}_j,0}$. These energies can be determined either by numerical simulation (or measurement) of an inverter half bridge of the considered inverter topology or by analytical approximation. The focus of this model is on an analytical approximation which is based on data sheet values of selected reference semiconductor devices. This approximation involves an additional scaling formula that is given by

$$E_{SD_i,\mathrm{ST}_j,0} = E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}} \cdot a_{SD_i,\mathrm{ST}_j}, \tag{3.103}$$

where the energies $E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$ are referred to as a *2L-based reference switching energies*. These are defined differently based on the type of SD_i as explained in the following.
For semiconductor devices SD_i that belong to the same switch-diode unit (i.e. transistors and their freewheeling diodes), in general called SDU_m, the energies $E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$ in (3.103) are defined as the switching energies of selected reference semiconductor devices arranged in a 2L half bridge configuration. Such switching energies, here referred to as $E_{\mathrm{S}_m,\mathrm{on},0}$, $E_{\mathrm{S}_m,\mathrm{off},0}$, $E_{\mathrm{D}_m,\mathrm{on},0}$, and $E_{\mathrm{D}_m,\mathrm{off},0}$, are typically available in the data sheets of semiconductor devices (except for $E_{\mathrm{D}_m,\mathrm{on},0} \approx 0$) for an arbitrary reference switched current $I_{0,2\mathrm{L},\mathrm{SD}_m}$ and reference switched voltage $V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_m}$.
The only semiconductor devices SD_i that do not belong to any switch-diode unit are the clamping diodes of the 3L-NPC-topology. These diodes are considered to be approximately lossless in this model which is a valid approximation for Schottky diodes. To also account for reverse recovery losses in the clamping diodes, the model could be extended for example by using reverse recovery losses from the data sheet of the considered diode for the definition of $E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$ in (3.103).
The scaling factor a_{SD_i,ST_j} in (3.103) accounts for the scaling between the reference switched current/voltage related to $E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$ (i.e. $I_{0,2\mathrm{L},\mathrm{SD}_m}$/ $V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_m}$) and the reference switched current/voltage related to $E_{SD_i,\mathrm{ST}_j,0}$ (i.e. I_0/ $V_{\mathrm{dc,mod},0}$). In addition, to take the effect of commutations between semiconductor devices of different ratings in 3L-inverter topologies into account, a_{SD_i,ST_j} can include measurement based correction factors. Such correction factors are for example known for the 3L-TT-topology [91,44] and are given in the following section.

3.4.3 Topology-Specific Model Parameters

To apply the previously described general switching loss model to the inverter topologies considered in this thesis (2L, 3L-NPC, 3L-TT, SPB, N_{m}P-2L), some topology-specific model parameters are required which are presented in this section.
Tab. 3.7 shows the topology-specific sets of semiconductor devices SD_i whose switching losses must be considered in the summation in (3.100). These sets are referred to as $\{SD_i\}_{\mathrm{P_{sw}}}$. In addition, Tab. 3.7 shows the topology-specific sets of reference semiconductor devices which are required for (3.103). These sets are referred to as $\{SD_i\}_{\mathrm{ref}}$.

Inverter topology	$\{SD_i\}_{\mathrm{P_{sw}}}$	$\{SD_i\}_{\mathrm{ref}}$
2L-based (2L, SPB, N_{m}P-2L)	$\mathrm{S_1}$, $\mathrm{D_1}$	$\mathrm{S_{p,1}}$, $\mathrm{D_{p,1}}$
3L-NPC	$\mathrm{S_1}$, $\mathrm{D_1}$, $\mathrm{S_2}$, $\mathrm{D_2}$, $\mathrm{D_5}$	$\mathrm{S_{p,1}}$, $\mathrm{D_{p,1}}$, $\mathrm{D_{p,5}}$
3L-TT	$\mathrm{S_1}$, $\mathrm{D_1}$, $\mathrm{S_2}$, $\mathrm{D_2}$	$\mathrm{S_{p,1}}$, $\mathrm{D_{p,1}}$, $\mathrm{S_{p,2}}$, $\mathrm{D_{p,2}}$

Table 3.7: Set of semiconductor devices whose switching losses are part of the sum in (3.100), i.e. $\{SD_i\}_{\mathrm{P_{sw}}}$, and set of required reference semiconductor devices, i.e. $\{SD_i\}_{\mathrm{ref}}$, for all considered inverter topologies.

j ST_j	E_{SD_i,ST_j}
1 p $\rightarrow$ n, $i_{\mathrm{r}} < 0$	$E_{\mathrm{D_1,off,ST_1}}$
2 n $\rightarrow$ p, $i_{\mathrm{r}} < 0$	$E_{\mathrm{D_1,on,ST_2}}$
3 p $\rightarrow$ n, $i_{\mathrm{r}} > 0$	$E_{\mathrm{S_1,off,ST_3}}$
4 n $\rightarrow$ p, $i_{\mathrm{r}} > 0$	$E_{\mathrm{S_1,on,ST_4}}$

Table 3.8: List of all possible switching transition types ST_j and the respectively caused switching energies E_{SD_i,ST_j} of a 2L-inverter half bridge.

Tab. 3.8 - Tab. 3.9 show all possible switching transition types ST_j and the respectively caused switching energies E_{SD_i,ST_j} for all considered inverter topologies. By means of these tables, the set of index values j to be considered in the outer summation in (3.101) can be determined: This set of index values corresponds to the set of switching transition types ST_j that cause switching losses in the semiconductor device SD_i according to the respective table.
Tab. 3.10 - Tab. 3.12 show the 2L-based reference switching energies $E_{SD_i,\mathrm{ST}_j,0,\mathrm{2L}}$ and the scaling factors a_{SD_i,ST_j} to be inserted into (3.103), for all considered inverter topologies.
With regard to the 2L-based inverter topologies (2L, SPB, N_{m}P-2L) it must be noted that the scaling in (3.103) with the reference energies from Tab. 3.10 only corresponds to a change of reference switching energies. Such a change of reference is only useful if multiple inverter topologies are considered within one inverter/IMD design procedure because this allows to use only one set of values for the reference parameters $\{I_0, V_{\mathrm{dc,mod,0}}\}$ from (3.102) for all considered inverter topologies. Otherwise, if only one 2L-based inverter topology is considered, (3.103)

j	ST_j	3L-NPC E_{SD_i,ST_j}	3L-TT E_{SD_i,ST_j}
1	$0 \rightarrow \mathrm{p},\ i_\mathrm{r} < 0$	$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_1},\ E_{\mathrm{D}_2,\mathrm{on},\mathrm{ST}_1}$	$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_1}$
2	$\mathrm{p} \rightarrow 0,\ i_\mathrm{r} < 0$	$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_2},\ E_{\mathrm{D}_2,\mathrm{off},\mathrm{ST}_2}$	$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_2}$
3	$0 \rightarrow \mathrm{n},\ i_\mathrm{r} < 0$	-	$E_{\mathrm{D}_2,\mathrm{off},\mathrm{ST}_3}$
4	$\mathrm{n} \rightarrow 0,\ i_\mathrm{r} < 0$	-	$E_{\mathrm{D}_2,\mathrm{on},\mathrm{ST}_4}$
5	$0 \rightarrow \mathrm{p},\ i_\mathrm{r} > 0$	$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_5},\ E_{\mathrm{D}_5,\mathrm{off},\mathrm{ST}_5}$	$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_5}$
6	$\mathrm{p} \rightarrow 0,\ i_\mathrm{r} > 0$	$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_6},\ E_{\mathrm{D}_5,\mathrm{on},\mathrm{ST}_6}$	$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_6}$
7	$0 \rightarrow \mathrm{n},\ i_\mathrm{r} > 0$	$E_{\mathrm{S}_2,\mathrm{off},\mathrm{ST}_7},\ E_{\mathrm{D}_5,\mathrm{off},\mathrm{ST}_7}$	$E_{\mathrm{S}_2,\mathrm{off},\mathrm{ST}_7}$
8	$\mathrm{n} \rightarrow 0,\ i_\mathrm{r} > 0$	$E_{\mathrm{S}_2,\mathrm{on},\mathrm{ST}_8},\ E_{\mathrm{D}_5,\mathrm{on},\mathrm{ST}_8}$	$E_{\mathrm{S}_2,\mathrm{on},\mathrm{ST}_8}$
9	$\mathrm{p} \rightarrow \mathrm{n},\ i_\mathrm{r} < 0$	$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_9},\ E_{\mathrm{D}_2,\mathrm{off},\mathrm{ST}_9}$	$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_9}$
10	$\mathrm{n} \rightarrow \mathrm{p},\ i_\mathrm{r} < 0$	$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_{10}},\ E_{\mathrm{D}_2,\mathrm{on},\mathrm{ST}_{10}}$	$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_{10}}$
11	$\mathrm{p} \rightarrow \mathrm{n},\ i_\mathrm{r} > 0$	$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_{11}},\ E_{\mathrm{S}_2,\mathrm{off},\mathrm{ST}_{11}}$	$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_{11}}$
12	$\mathrm{n} \rightarrow \mathrm{p},\ i_\mathrm{r} > 0$	$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_{12}},\ E_{\mathrm{S}_2,\mathrm{on},\mathrm{ST}_{12}}$	$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_{12}}$

Table 3.9: List of all possible switching transition types ST_j and the respectively caused switching energies E_{SD_i,ST_j} of a 3L-NPC-/3L-TT-inverter half bridge.

$E_{SD_i,\mathrm{ST}_j,0}$	$E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$	a_{SD_i,ST_j}
$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_1,0}$	$E_{\mathrm{D}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_2,0}$	$E_{\mathrm{D}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_3,0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_4,0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$

Table 3.10: 2L-based reference switching energies $E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$ and corresponding scaling factors a_{SD_i,ST_j} to be inserted into (3.103) to calculate each topology-specific reference switching energy $E_{SD_i,\mathrm{ST}_j,0}$ of a 2L-inverter module. The switching energies $E_{\mathrm{S}_1,\mathrm{on},0}$, $E_{\mathrm{S}_1,\mathrm{off},0}$, $E_{\mathrm{D}_1,\mathrm{on},0}$, and $E_{\mathrm{D}_1,\mathrm{off},0}$ are typically provided in the data sheets of the considered reference semiconductor devices $\mathrm{S}_{\mathrm{p},1}$ & $\mathrm{D}_{\mathrm{p},1}$, for an arbitrary reference current $I_{0,2\mathrm{L},\mathrm{SD}_1}$ and reference voltage $V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_1}$. The scaling factors include the voltage scaling factor $x_\mathrm{V} = {}^{V_{\mathrm{dc},\mathrm{mod},0}}/_{V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_1}}$ and the current scaling factor $x_\mathrm{I} = {}^{I_0}/_{I_{0,2\mathrm{L},\mathrm{SD}_1}}$.

$E_{SD_i,\mathrm{ST}_j,0}$	$E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$	a_{SD_i,ST_j}
$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_1,0}$	$E_{\mathrm{D}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_2,\mathrm{on},\mathrm{ST}_1,0}$	0	0
$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_2,0}$	$E_{\mathrm{D}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_2,\mathrm{off},\mathrm{ST}_2,0}$	0	0
$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_5,0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_5,\mathrm{off},\mathrm{ST}_5,0}$	0	0
$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_6,0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_5,\mathrm{on},\mathrm{ST}_6,0}$	0	0
$E_{\mathrm{S}_2,\mathrm{off},\mathrm{ST}_7,0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_5,\mathrm{off},\mathrm{ST}_7,0}$	0	0
$E_{\mathrm{S}_2,\mathrm{on},\mathrm{ST}_8,0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_5,\mathrm{on},\mathrm{ST}_8,0}$	0	0
$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_9,0}$	$E_{\mathrm{D}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_2,\mathrm{off},\mathrm{ST}_9,0}$	$E_{\mathrm{D}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_{10},0}$	$E_{\mathrm{D}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{D}_2,\mathrm{on},\mathrm{ST}_{10},0}$	$E_{\mathrm{D}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_{11},0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{S}_2,\mathrm{off},\mathrm{ST}_{11},0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_{12},0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$
$E_{\mathrm{S}_2,\mathrm{on},\mathrm{ST}_{12},0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$x_\mathrm{V} \cdot x_\mathrm{I}$

Table 3.11: 2L-based reference switching energies $E_{SD_i,\mathrm{ST}_j,0,2\mathrm{L}}$ and corresponding scaling factors a_{SD_i,ST_j} to be inserted into (3.103) to calculate each topology-specific reference switching energy $E_{SD_i,\mathrm{ST}_j,0}$ of a 3L-NPC-inverter. The switching energies $E_{\mathrm{S}_1,\mathrm{on},0}$, $E_{\mathrm{S}_1,\mathrm{off},0}$, $E_{\mathrm{D}_1,\mathrm{on},0}$, and $E_{\mathrm{D}_1,\mathrm{off},0}$ are typically provided in the data sheets of the considered reference semiconductor devices $\mathrm{S}_{\mathrm{p},1}$ & $\mathrm{D}_{\mathrm{p},1}$, for an arbitrary reference current $I_{0,2\mathrm{L},\mathrm{SD}_1}$ and reference voltage $V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_1}$. The scaling factors include the voltage scaling factor $x_\mathrm{V} = {}^{V_{\mathrm{dc,mod},0}}\!/_{2V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_1}}$ and the current scaling factor $x_\mathrm{I} = {}^{I_0}\!/_{I_{0,2\mathrm{L},\mathrm{SD}_1}}$.

can be omitted by setting I_0 and $V_{\mathrm{dc,mod},0}$ in (3.102) equal to $I_{0,2\mathrm{L},\mathrm{SD}_1}$ and $V_{\mathrm{dc},0,2\mathrm{L},\mathrm{SD}_1}$, respectively.

$E_{SD_i,\mathrm{ST}_j,0}$	$E_{SD_i,\mathrm{ST}_j,0,\mathrm{2L}}$	a_{SD_i,ST_j}
$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_1,0}$	$E_{\mathrm{D}_1,\mathrm{on},0}$	$x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_2,0}$	$E_{\mathrm{D}_1,\mathrm{off},0}$	$1.01 \cdot x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{D}_2,\mathrm{off},\mathrm{ST}_3,0}$	$E_{\mathrm{D}_2,\mathrm{off},0}$	$0.83 \cdot x_{\mathrm{V},2} \cdot x_{\mathrm{I},2}$
$E_{\mathrm{D}_2,\mathrm{on},\mathrm{ST}_4,0}$	$E_{\mathrm{D}_2,\mathrm{on},0}$	$x_{\mathrm{V},2} \cdot x_{\mathrm{I},2}$
$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_5,0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$0.76 \cdot x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_6,0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$0.95 \cdot x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{S}_2,\mathrm{off},\mathrm{ST}_7,0}$	$E_{\mathrm{S}_2,\mathrm{off},0}$	$1.06 \cdot x_{\mathrm{V},2} \cdot x_{\mathrm{I},2}$
$E_{\mathrm{S}_2,\mathrm{on},\mathrm{ST}_8,0}$	$E_{\mathrm{S}_2,\mathrm{on},0}$	$1.94 \cdot x_{\mathrm{V},2} \cdot x_{\mathrm{I},2}$
$E_{\mathrm{D}_1,\mathrm{off},\mathrm{ST}_9,0}$	$E_{\mathrm{D}_1,\mathrm{off},0}$	$x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{D}_1,\mathrm{on},\mathrm{ST}_{10},0}$	$E_{\mathrm{D}_1,\mathrm{on},0}$	$x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{S}_1,\mathrm{off},\mathrm{ST}_{11},0}$	$E_{\mathrm{S}_1,\mathrm{off},0}$	$x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$
$E_{\mathrm{S}_1,\mathrm{on},\mathrm{ST}_{12},0}$	$E_{\mathrm{S}_1,\mathrm{on},0}$	$x_{\mathrm{V},1} \cdot x_{\mathrm{I},1}$

Table 3.12: 2L-based reference switching energies $E_{SD_i,\mathrm{ST}_j,0,\mathrm{2L}}$ and corresponding scaling factors a_{SD_i,ST_j} to be inserted into (3.103) to calculate each topology-specific reference switching energy $E_{SD_i,\mathrm{ST}_j,0}$ of a 3L-TT-inverter. The switching energies $E_{\mathrm{S}_m,\mathrm{on},0}$, $E_{\mathrm{S}_m,\mathrm{off},0}$, $E_{\mathrm{D}_m,\mathrm{on},0}$, and $E_{\mathrm{D}_m,\mathrm{off},0}$ for $m \in \{1,2\}$ are typically provided in the data sheets of the considered reference semiconductor devices $\mathrm{S}_{\mathrm{p},m}$ & $\mathrm{D}_{\mathrm{p},m}$, for arbitrary reference currents $I_{0,\mathrm{2L},\mathrm{SD}_m}$ and reference voltages $V_{\mathrm{dc},0,\mathrm{2L},\mathrm{SD}_m}$. The scaling factors a_{SD_i,ST_j} include the voltage scaling factors $x_{\mathrm{V},m} = {V_{\mathrm{dc},\mathrm{mod},0}}/{2V_{\mathrm{dc},0,\mathrm{2L},\mathrm{SD}_m}}$, the current scaling factors $x_{\mathrm{I},m} = {I_0}/{I_{0,\mathrm{2L},\mathrm{SD}_m}}$, and the measurement based correction factors from [88].

3.5 Inverter Reliability Model

In this section, a model for the reliability of inverters is presented, considering the inverter topologies that were selected in section 2.2.2. The model description in the following paragraph was previously published in section 3.6 of [89]. There, the SPB-topology with n SPB-modules is referred to as 2L-nM-ser and the N_{m}P-2L-topology is referred to as 2L-nM-par with $n = N_{\mathrm{m}}$.

2L-nM-ser- & 2L-nM-par-converters can be designed with a k-out-of-n-redundancy, which means that up to k 2L-modules can fail while the system can still operate (in part-load). On the one hand, such re-

dundancy improves the system reliability. On the other hand, the higher component count of the modular topologies compared to a 2L-converter degrades the system reliability due to the higher risk of component failure. Given these contrary effects, the question is, if the modular topologies 2L-nM-ser & 2L-nM-par overall have an advantage over the 2L- and 3L-topologies in terms of reliability. To answer this question, a reliability model is built that is based on the following three definitions according to [90].

1. The *reliability* $R(t)$ of an item is defined as the probability that an item can perform a required function under given conditions for a given time interval $[0, t]$.

2. The *failure rate* $\lambda(t)$ of an item is defined as the average number of failing items per time unit normalised to the total number of still good/working items at the time instant t.

3. The *Mean-Time-To-Failure MTTF* is defined as $\int_0^\infty R(t)dt$.

To calculate the reliability of a system consisting of multiple items, the reliabilities of these items are combined in one of the following two ways depending on the type of redundancy: 1) If the items are non-redundant, their reliability functions (i.e. probabilities of working) are multiplied. 2) If the items are redundant, the overall reliability corresponds to the sum of the probabilities of all working combinations. This concept is applied to all considered converter topologies (Fig. 2.19), where the items are given by the power semiconductor devices. Considering a constant failure rate over time for each device, the reliability of a single device, e.g. the switch $S_{p,1}$ of the 2L-topology, is given by $R_{S1} = e^{-\lambda_{S1} \cdot t}$ [90]. The resulting formulas for calculating the converter reliability are summarized in Tab. 3.13. The reliability results for a specific number of modules and for a specific failure rate are given in section 4.2.

3.6 Scalable Motor Model for Multiphase Non-Salient PMSMs

In this section, a scalable motor model for multiphase (including 3-phase, i.e. $m \geq 3$) non-salient PMSMs (i.e. SPMSMs) is presented which can be used for IMD design procedures such as the IMD design

Table 3.13: Formulas for calculating the converter reliability for the converter topologies shown in Fig. 2.19. The used reliability functions of the power semiconductor devices $S_{p,1}/S_{p,2}/D_{p,5}$ from Fig. 2.19 are given by $R_{S1} = e^{-\lambda_{S1} \cdot t}$, $R_{S2} = e^{-\lambda_{S2} \cdot t}$, and $R_{D5} = e^{-\lambda_{D5} \cdot t}$. The value pair $\{k, n\}$ defines the k-out-of-n redundancy for the modular topologies with $k \in [0, n-1]$.

Topology	Reliability
2L	$R_{S1}^6 =: R_{2L}$
3L-NPC	$R_{S1}^{12} \cdot R_{D5}^6$
3L-TT	$R_{S1}^6 \cdot R_{S2}^6$
2L-nM-ser-k / 2L-n-par-k	$\sum_{i=0}^{k} \binom{n}{i} (R_{2L})^{(n-i)} (1 - R_{2L})^i$

procedures that are described in chapter 4. The term *scalable* refers to the fact that the model presented in this section can be applied to a general design of a multiphase non-salient PMSM (i.e. motor stage MS3), including a variable/scalable motor length, diameter, number of poles, number of slots, and winding scheme. The motor parameters that are used in this model are summarised in Tab. 3.14.
The scalable motor model includes different parts which are presented in the following subsections: First, an electromechanical motor model is given in section 3.6.1. This model includes equations for the motor voltages, the motor flux linkages, and the motor torque. Subsequently, the equations for calculating the motor parameters that are part of the electromechanical motor model (R, L_{dqk}, and ψ_{PM1}) are given in section 3.6.2. Finally, different criteria for the evaluation of slot-pole combinations are given in section 3.6.3.

3.6.1 Electromechanical Motor Model

An electromechanical motor model comprising a voltage equation, a flux equation, and a torque equation in dq-coordinates is given in (5.9) of [79] for electrically excited salient multiphase (including 3-phase, i.e. $m \geq 3$) synchronous machines. This model is adapted to non-salient PMSMs by replacing the product of the excitation current and the main inductance with the magnet flux linkage ψ_{PMk} and by setting the

Table 3.14: Used motor parameters.

$A_{\mathrm{c,skin}}(f)$	Effective conductor cross sectional area	m	Number of phases per base winding
A_δ	Air gap area ($2\pi r_\mathrm{g} l_\mathrm{m}$)	μ_0	Vacuum permeability
α	Angular position on the stator	N	Number of stator slots
$\alpha_{N[-\pi,\pi]}$	El. angle between adjacent slots in $[-\pi,\pi]$	$N_i(\alpha)$	Winding function of the i-th phase
α_sys	Angle between winding axes	N_l	Number of tooth-coils
α_z	Angle between phasors in the star of slots	n_l	Number of winding layers (1 or 2)
a_p	Number of phase-aligned winding axes	n_n	Rated speed
$\hat{B}_{\delta,1}$	Fundamental air gap flux density	n_t	Number of turns per tooth-coil
b_s	Slot opening	ω	Electrical angular frequency
D	Outer stator diameter	$p_\mathrm{Cu,loss}$	Copper loss density (related to motor surface)
δ	Air gap length	PF	Power factor
h_M	Length of rotor magnets in radial direction	p	Number of pole pairs
$\vec{i}_{\mathrm{dq}k}$	Motor current in the k-th dq-subspace	$\vec{\psi}_{\mathrm{dq}k}$	Motor flux linkage in the k-th dq-subspace
J	Current density in the stator winding	$\vec{\psi}_{\mathrm{PM}k}$	Magnet flux linkage in the k-th dq-subspace
k_fill	Copper fill factor	$R(f)$	AC phase resistance
k_p	Pole embrace of rotor magnets	r_g	Air gap radius
k_w	Winding factor	ρ_Cu	Copper conductivity
$L_{\mathrm{dq}k}$	Motor inductance in the k-th dq-subspace	T	Electromagnetic torque
L_{ij}	(i,j)-th motor inductance matrix entry	T_n	Rated torque
l_m	Motor length	t	Winding periodicity number
l_t	Mean length of one winding turn	$\vec{v}_{\mathrm{dq}k}$	Motor voltage in the k-th dq-subspace

inductance in the d-axis equal to the inductance in the q-axis. These adaptations result in the following set of equations:

$$\vec{v}_{\mathrm{dq}k} = R\vec{i}_{\mathrm{dq}k} + \mathrm{j}k\omega\vec{\psi}_{\mathrm{dq}k} + \frac{\mathrm{d}\vec{\psi}_{\mathrm{dq}k}}{\mathrm{d}t} \tag{3.104}$$

$$\vec{\psi}_{\mathrm{dq}k} = L_{\mathrm{dq}k}\vec{i}_{\mathrm{dq}k} + \vec{\psi}_{\mathrm{PM}k} \tag{3.105}$$

$$T_\mathrm{m} = \frac{m}{2}p\sum_{k=1,3,\ldots}^{k_\mathrm{max}} k\psi_{\mathrm{PM}k}i_{\mathrm{q}k} \overset{!}{=} \frac{m}{2}p\psi_{\mathrm{PM}1}i_{\mathrm{q}1}, \tag{3.106}$$

for $k = 1, 3, \ldots k_\mathrm{max}$ with $k_\mathrm{max} = m - 2$, if m is odd and $k_\mathrm{max} = m - 1$, if m is even. In multiphase machines ($m > 3$), different harmonics of phase voltages, currents, and flux linkages are mapped into $k_\mathrm{max} > 1$ dq-subspaces [79], in contrast to 3-phase machines ($m = 3$) where $k_\mathrm{max} = 1$. In this thesis, harmonic current injection is not considered ($i_{\mathrm{q}k} \approx 0$ for $k > 1$) so that only the first summand in (3.106) remains.
The motor model equations (3.104)-(3.106) allow the modelling of motors with $m \geq 3$, but they imply $N_\mathrm{ph} = m$, i.e. motors without phase-aligned winding systems. In order to consider also motors with phase-aligned winding systems ($N_\mathrm{ph} = a_\mathrm{P} \cdot m$), a theoretical reference motor with $m_0 = m$ phases per base winding and $N_{\mathrm{ph},0} = m$ phase windings is defined, in which each phase winding has a_P parallel paths. Each of these parallel paths then represents a phase winding of the considered

motor with $N_{\mathrm{ph}} = a_{\mathrm{P}} \cdot m$. The theoretical reference motor is in the following referred to as reduced motor, and its phase windings as reduced phase windings. With this modelling approach, the motor phase currents of a motor with $N_{\mathrm{ph}} = a_{\mathrm{P}} \cdot m$ are calculated by first solving (3.104) for the currents in the reduced motor and then dividing by a_{P}. It must be noted that this modelling approach implies the assumption that the same voltage drops over phase-aligned phase windings. For motors with phase-aligned three-phase winding systems, this assumption is fulfilled as long as each three-phase winding system is supplied with the same DM voltage at the motor terminals, which corresponds to steady-state operation.
Alternatively to (3.106), the motor torque can be calculated from the induced phase voltages (back electromotive forces) and phase currents with the following equation:

$$T_{\mathrm{m}} = \sum_{i=1}^{N_{\mathrm{m}}} T_{\mathrm{m},i} = \frac{1}{\omega_{\mathrm{mech}}} \sum_{i=1}^{N_{\mathrm{m}}} (v_{\mathrm{bemf,r},i} i_{\mathrm{r},i} + v_{\mathrm{bemf,s},i} i_{\mathrm{s},i} + v_{\mathrm{bemf,t},i} i_{\mathrm{t},i}). \tag{3.107}$$

There, $v_{\mathrm{bemf,r},i}$ and $i_{\mathrm{r},i}$ are the phase r back electromotive force and the phase r current of the i-th 3-phase inverter module, respectively.
The motor torque ripple is defined as the peak-to-peak ripple of $T_{\mathrm{m}}(t)$, where $T_{\mathrm{m}}(t)$ results from either (3.106) or (3.107):

$$\Delta T_{\mathrm{m}} = \max\left(T_{\mathrm{m}}(t)\right) - \min\left(T_{\mathrm{m}}(t)\right). \tag{3.108}$$

3.6.2 Motor Parameters R, $L_{\mathrm{dq}k}$, and ψ_{PM1}

The electromechanical motor model given in the previous section contains the motor phase winding resistance R, the motor inductances $L_{\mathrm{dq}k}$, and the motor excitation flux linkage ψ_{PM1}. These parameters are calculated with

$$R(f) = \frac{n_{\mathrm{t}} N_{\mathrm{l}}}{m a_{\mathrm{p}}^2} \rho_{\mathrm{Cu}} \frac{\bar{l}_{\mathrm{t}}}{A_{\mathrm{c,skin}}(f)} \tag{3.109}$$

$$L_{ij} = \frac{\mu_0 r_{\mathrm{g}} l_{\mathrm{m}}}{\delta} \int_0^{2\pi} N_i(\alpha) N_j(\alpha) d\alpha + L_{ij,\mathrm{slot}} \tag{3.110}$$

$$\psi_{\mathrm{PM1}} = k_{\mathrm{w}} \frac{n_{\mathrm{t}} N_{\mathrm{l}}}{m a_{\mathrm{p}}} l_{\mathrm{m}} \frac{2 r_{\mathrm{g}}}{p} \hat{B}_{\delta,1}. \tag{3.111}$$

The inductance L_{ij} in (3.110) is the (i,j)-th entry of the winding inductance matrix. The integral term corresponds to the main and the leakage harmonic inductance [91]. The slot leakage inductance $L_{ij,\mathrm{slot}}$ is calculated based on section 4.4.3 of [92]. The inductance $L_{\mathrm{dq}k}$ is obtained from the k-th diagonal entry of the matrix $[T]_m [L_{ij}] [T]_m^{-1}$ where $[T]_m$ is the dq-transformation matrix for an m-phase system derived from [93].
The model equations (3.109)-(3.111) can be used if the IMD design procedure includes a new motor design. According to the definition of *motor stages* in section 2.4.2, this corresponds to motor stage MS3. If only the winding scheme and the number of turns of a given reference motor are changed, which corresponds to motor stage MS2b, the excitation flux linkage can also be calculated based on the following scaling formula:

$$\psi_{\mathrm{PM1}} = \psi_{\mathrm{PM1,0}} \cdot \frac{k_{\mathrm{w}}}{k_{\mathrm{w,0}}} \cdot \frac{n_{\mathrm{t}}}{n_{\mathrm{t,0}}} \cdot \frac{m_0}{m} \cdot \frac{a_{\mathrm{p,0}}}{a_{\mathrm{p}}} \tag{3.112}$$

There, the index "0" indicates the parameters of the considered reference motor. The advantage of using (3.112) compared to (3.111) is that (3.112) requires less motor parameters and less calculation effort.

3.6.3 Criteria for the Evaluation of Slot-Pole Combinations

In this section, different criteria for evaluating and selecting a slot-pole combination, i.e. a combination of the number of stator slots N and of the number of rotor pole pairs p, are described. Although the main focus of this thesis with regard to motor windings is on double-layer tooth-coil windings, single-layer tooth-coil windings are also included in these criteria as both types of windings can be analysed with similar means.
The criteria are summarized in Tab. 3.15 and are explained in the following. Criteria C1 to C5 are commonly used in motor design, while criterion C6 is particularly added to determine how suitable a slot-pole combination is for an integrated modular motor-converter system.
C1: An m-phase, n_{l}-layer tooth-coil winding for a motor with N stator slots, p rotor pole pairs, and a_{p} phase-aligned winding systems is feasible if the two conditions C1a and C1b are fulfilled. **C1a** ensures that the number of stator slots can be equally shared among all phase windings and that α_{sys} matches an integer multiple of the electrical distance of

Table 3.15: Criteria C1-C6 for evaluating/selecting a slot-pole combination.

C1 Winding feasibility	C4 $\gcd(N_\mathrm{l}, 2p) > 1$ to avoid unbalanced magnetic pull
C2 High winding factor k_w	C5 High $\mathrm{lcm}(N, 2p)$ for low cogging torque
C3 Low rotor loss indicator $p_\mathrm{r,loss}$	C6 High degree of modularity

slots along the stator circumference. **C1b** ensures that a_p phase-aligned winding systems are possible. The analytical expressions for C1a and C1b in (3.113)-(3.115) are valid for single and for double layer tooth-coil windings. The expressions are derived based on [74] and [94] by defining the number of layers n_l (1 for single layer, 2 for double layer windings) and the number of tooth-coils $N_\mathrm{l} := {}^{n_\mathrm{l}N}/_{2}$.

$$\mathbf{C1a}: \frac{\alpha_\mathrm{sys} N_\mathrm{l}}{2\pi t} \in \mathbb{N} \tag{3.113}$$

$$\mathbf{C1b}: \frac{a_\mathrm{p,max}}{a_\mathrm{p}} \in \mathbb{N} \tag{3.114}$$

$$\text{with } a_\mathrm{p,max} = \begin{cases} 2t, & \text{if } \frac{N_\mathrm{l}}{mt} \text{ is even} \\ t, & \text{if } \frac{N_\mathrm{l}}{mt} \text{ is odd} \end{cases} \tag{3.115}$$

The winding periodicity number t in (3.115) is given by the greatest common divider (gcd) of N_l and p. This number indicates how often a so-called base winding is repeated along the stator circumference.

C2: The fundamental winding factor $k_\mathrm{w,1}$, further called winding factor k_w, can be defined as ${}^{\psi_\mathrm{PM1}}/_{w\phi_\mathrm{PM1}}$, where w is the number of turns in series per phase of the stator winding and ϕ_PM1 is the fundamental air gap flux of one rotor magnet [95]. Therefore, the product $k_\mathrm{w} \cdot w$ describes the effective number of turns linked to the complete rotor flux ϕ_PM1. If the torque, the speed, and the available motor voltage are imposed, a higher winding factor can be used to reduce the number of turns or to reduce the flux by decreasing the motor size. These changes have an impact on efficiency and/or power density as will be shown later. Here, the winding factor is determined using the method of the star of slots [74, 94], illustrated in Fig. 3.19 for one example configuration. The "star" in Fig. 3.19a consists of so-called slot phasors indicating the voltages induced by the rotating excitation field in the coil sides of one layer of one base winding. The phasors are placed at an angular distance of $\alpha_\mathrm{z} = {}^{2\pi t}/_{N_\mathrm{l}}$ resulting in a number of $n_\mathrm{e} := {}^{N_\mathrm{l}}/_{t}$

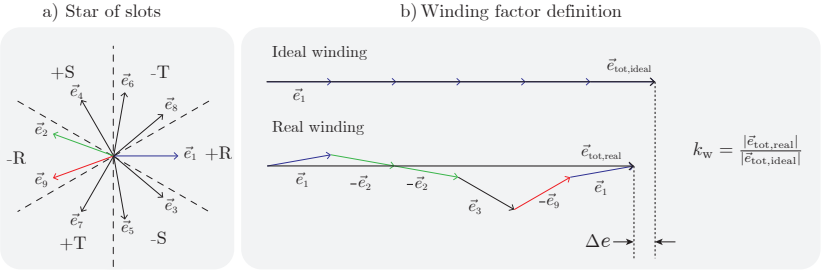


Figure 3.19: a) Star of slots for an example winding with $m = 3$, $n_l = 2$, $N = 27$ and $p = 12$. b) Derivation of the winding factor from the star of slots.

phasors. Each of the slot phasors, denoted by $\vec{e}_i$, is assigned to one phase with a positive or negative sign s_i according to the zones labelled +R, -T, etc. that are defined by the considered winding axis configuration. Then, the winding factor is calculated as the ratio of the total induced phase voltage to the induced phase voltage of an ideal reference winding whose slot phasors lie on the same axis, as shown in Fig. 3.19b. There, the coil pitch and the winding distribution are inherently taken into account [74].

C3: Eddy currents in the rotor magnets and in the rotor iron due to parasitic stator magnetomotive force harmonics should be negligible. In this thesis, a relative indicator $p_{r,loss}$ derived in [77, 96] is used to take this loss component into account. Slot-pole combinations with $p_{r,loss} > 100$ are discarded.

C4 & **C5**: As a further criterion, $\gcd(N_l, 2p) > 1$ should be applied in order to avoid unbalanced magnetic pull that can lead to motor vibration and noise [97]. Furthermore, a high value of the lowest common multiple (lcm) of N and $2p$ indicates low cogging torque [97]. Here, $\mathrm{lcm}(N, 2p) > 50$ is chosen.

C6: To evaluate how suitable a winding is for an integrated modular motor-converter system, three degrees of modularity for motor-converter systems are defined which are shown in Fig. 3.20. There, an SPB-inverter with 3 SPB-/inverter modules is used as an example. In general, the following considerations apply to all inverter topologies that consist of 3-phase inverter modules. The three degrees A, B, and C define to what extend the stator and the converter can be modularised into motor-converter modules. In Fig. 3.20, coils of the same colour

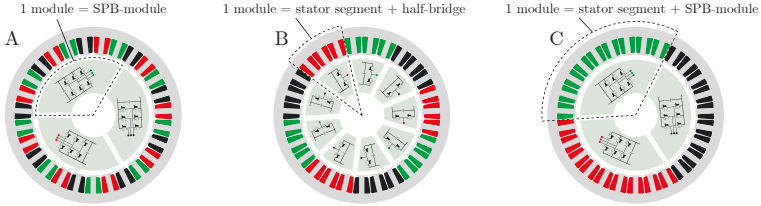


Figure 3.20: Defined degrees of modularity A, B, and C of motor-converter systems using the SPB-C and tooth-coil windings for exemplary motors with $N = 27$, $a_\mathrm{p} = a_\mathrm{p,max} = 3$, $n_\mathrm{l} = 2$ and A: $p = 1$ & $m = 9$, B: $p = 13$ & $m = 9$, and C: $p = 12$ & $m = 3$. Windings of the same colour (green/red/black) are connected to the same SPB-module.

are connected to the same SPB-module. Modularity degree A means that only converter modules but no combined motor-converter modules are possible because the coils connected to one SPB-module (i.e. one colour in Fig. 3.20) are spread around the stator. Degree B means that combined motor-converter modules are possible where each module consists of one stator segment and one half bridge of the SPB-C. Degree C means that motor-converter modules are possible where each module consists of one stator segment and one complete SPB-module. The disadvantage of degree B compared to C is that half bridges of the same three-phase SPB-module are spread around the stator, which requires wiring across converter modules. For each degree of modularity, conditions on the slot-pole combination are analysed. For modularity degree A, no condition applies. For modularity degree B, the conditions in (3.116) are derived based on the method of the star of slots where $\alpha_{N[-\pi,\pi]} := {}^{2\pi p}/_{N_\mathrm{l}}$ is the electrical angle between two mechanically adjacent slots in case of a double layer winding and between every second slot in case of a single layer winding. For modularity degree C, it is found that (3.116) must be fulfilled and that the winding axes of phases connected to one SPB-module must be adjacent. Among the winding axis configurations of 3-, 6-, 9-, and 12-phase motors investigated in [98], this is only the case for 3-phase motors ($m = 3$). Hence, the multiphase-motors with $m = 6/9/12$ cannot reach the highest de-

gree of modularity.

$$\begin{cases} a_\mathrm{p} = a_\mathrm{p,max} \wedge \left(\frac{N_\mathrm{l}}{mt} = 2 \vee \alpha_{N[-\pi,\pi]} = \pm\alpha_\mathrm{z} \vee \alpha_{N[-\pi,\pi]} = \pm(\frac{N_\mathrm{l}}{2t} - 1)\alpha_\mathrm{z}\right), \\ \qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad\qquad \text{if } \frac{N_\mathrm{l}}{mt} \text{ is even} \\ a_\mathrm{p} = a_\mathrm{p,max} \wedge \left(\frac{N_\mathrm{l}}{mt} = 1 \vee \alpha_{N[-\pi,\pi]} = \pm(\frac{N_\mathrm{l}}{2t} - \frac{1}{2})\alpha_\mathrm{z}\right), \quad \text{if } \frac{N_\mathrm{l}}{mt} \text{ is odd} \end{cases} \tag{3.116}$$

3.7 Motor Winding Loss Models

In this section, motor winding loss models are presented which can be used in IMD design procedures such as the IMD design procedures presented in chapter 4. Two models are presented in the following: 1) A relatively simple motor winding loss model that takes the skin effect into account. 2) A more complex motor winding loss model that takes the skin effect and the proximity effect into account.

3.7.1 Motor Winding Loss Model Including the Skin Effect

This model is based on a relatively simple adaptation of the DC phase resistance from (4.99) of [92], given by

$$R_\mathrm{dc} = \frac{n_\mathrm{t} N_\mathrm{l}}{m a_\mathrm{p}^2} \rho_\mathrm{Cu} \frac{\bar{l}_\mathrm{t}}{A_\mathrm{c}}, \tag{3.117}$$

to an AC phase resistance by replacing the conductor cross-sectional area A_c with the effectively current-carrying area $A_\mathrm{c,skin}(f)$, resulting in (3.109) which is here given again:

$$R(f) = \frac{n_\mathrm{t} N_\mathrm{l}}{m a_\mathrm{p}^2} \rho_\mathrm{Cu} \frac{\bar{l}_\mathrm{t}}{A_\mathrm{c,skin}(f)}. \tag{3.118}$$

Therein, the current-carrying area $A_\mathrm{c,skin}(f)$ is approximated based on the skin depth:

$$A_\mathrm{c,skin}(f) = \pi \left(\frac{d_\mathrm{c}}{2}\right)^2 - \pi \cdot \left(\frac{d_\mathrm{c} - 2 \cdot d_\mathrm{skin}(f)}{2}\right)^2 \tag{3.119}$$

$$d_\mathrm{skin}(f) = \frac{1}{\sqrt{\pi f \sigma_\mathrm{Cu} \mu_0}} \tag{3.120}$$

Using the AC phase resistance that results from (3.118)-(3.120), the motor winding losses are calculated with

$$P_{\mathrm{Cu}} = m \sum_i R(f_i) I_{\mathrm{r,par}}(f_i)^2, \tag{3.121}$$

where $I_{\mathrm{r,par}}(f_i)$ is the RMS amplitude spectrum of the current flowing in the reduced phase winding of phase r which was defined in section 3.6.1.

3.7.2 Motor Winding Loss Model Including the Skin Effect and the Proximity Effect

With this model, the motor winding losses are calculated with

$$P_{\mathrm{Cu}} = P_{\mathrm{Cu,skin}} + P_{\mathrm{Cu,prox}}, \tag{3.122}$$

where $P_{\mathrm{Cu,skin}}$ are the winding losses including the skin effect which are calculated with (3.121). $P_{\mathrm{Cu,prox}}$ are the additional winding losses due to the proximity effect which are referred to as proximity losses. The used proximity loss model to calculate $P_{\mathrm{Cu,prox}}$ is based on an application of the general model for proximity losses in round conductors from [99] to double-layer tooth-coil motor windings. This application requires additional modelling steps including a model of the conductor arrangement in the stator slots and a formulation of the magnetic field surrounding the conductors in each stator slot. The proximity loss model including these additional modelling steps is explained in the following.

The proximity losses in a round conductor of the length l_{s} can be calculated with (6.42) from [99], given by

$$P_{\mathrm{Cu,prox,1}}(f) = R_{\mathrm{dc,1}} G r(f) \hat{H}(f)^2 \tag{3.123}$$

with

$$Gr(f) = -\frac{\xi\pi^2 d^2}{2\sqrt{2}} \cdot \left(\frac{K_{Ber}(2,\xi)K_{Ber}(1,\xi) + K_{Ber}(2,\xi)K_{Bei}(1,\xi)}{K_{Ber}(0,\xi)^2 + K_{Bei}(0,\xi)^2} + \frac{K_{Bei}(2,\xi)K_{Bei}(1,\xi) - K_{Bei}(2,\xi)K_{Ber}(1,\xi)}{K_{Ber}(0,\xi)^2 + K_{Bei}(0,\xi)^2} \right) \quad (3.124)$$

$$R_{\mathrm{dc},1} = \frac{4l_{\mathrm{s}}}{\sigma\pi d_{\mathrm{c}}^2} \quad (3.125)$$

$$\xi = \frac{d_{\mathrm{c}}}{\sqrt{2}d_{\mathrm{skin}}}. \quad (3.126)$$

Therein, $R_{\mathrm{dc},1}$ is the DC resistance of a single conductor, $Gr(f)$ is a frequency-dependent factor, and $\hat{H}(f)$ is the peak amplitude of the external magnetic field surrounding the conductor. In (3.124), K_{Bei} is the Bei-Kelvin function and K_{Ber} is the Ber-Kelvin function [99]. Based on this proximity loss model for a single conductor, the proximity losses for a complete double-layer tooth-coil motor winding are calculated with

$$P_{\mathrm{Cu,prox}} = \sum_q P_{\mathrm{Cu,prox}}(f_q) \quad (3.127)$$

$$P_{\mathrm{Cu,prox}}(f) = N_{\mathrm{bw}} \cdot R_{\mathrm{dc},1} \cdot 4 \cdot Gr(f) \sum_{k=1}^{N_{\mathrm{s,bw}}} \sum_{i=1}^{n_{\mathrm{t}}} H_{i,k}(f)^2. \quad (3.128)$$

Therein, $P_{\mathrm{Cu,prox}}(f)$ are the proximity losses for a single frequency component and $P_{\mathrm{Cu,prox}}$ are the total proximity losses. In (3.128), N_{bw} is the number of base windings, $N_{\mathrm{s,bw}} = {}^{N_{\mathrm{s}}}/_{N_{\mathrm{bw}}}$ is the number of stator slots per base winding, and n_{t} is the number of turns per tooth-coil. Furthermore, $H_{i,k}(f)$ in (3.128) is the RMS amplitude spectrum of the external magnetic field that surrounds the i-th conductor/turn of each of the two coil-sides that lie within the k-th stator slot of one base winding. A formulation for $H_{i,k}(f)$ is determined based on a simplified model of the conductor arrangement within one stator slot which is shown in Fig. 3.21.

Applying Ampère's law with the integration curve C from Fig. 3.21 and assuming a relatively large number of turns, $H_{i,k}(f)$ can be approximated with the linear expression given by

$$H_{i,k}(f) = \frac{n_{\mathrm{t}} y_i}{h_{\mathrm{t}} \bar{w}_{\mathrm{slot}}} \cdot I_{1,2,k}(f). \quad (3.129)$$

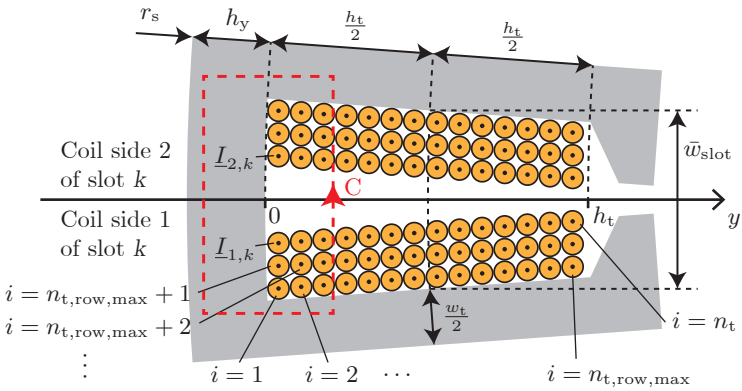


Figure 3.21: Simplified model of the conductor arrangement within the k-th stator slot of a motor with a double-layer tooth-coil winding.

Therein, h_t and $\bar{w}_\mathrm{slot}$ are the tooth/slot height and the mean slot width, respectively, as shown in Fig. 3.21. The parameter y_i in (3.129) is the y-coordinate of the position of the i-th conductor of each of the two coil sides within the stator slot. The mean slot width $\bar{w}_\mathrm{slot}$ is given by the following equations which result from basic trigonometric calculations:

$$\bar{w}_\mathrm{slot} = 2r_\mathrm{w,s} \cdot \sin\left(\frac{\alpha_\mathrm{w,s}}{2}\right) \tag{3.130}$$

$$r_\mathrm{w,s} = r_\mathrm{s} - \left(h_\mathrm{y} + \frac{h_\mathrm{t}}{2}\right) \tag{3.131}$$

$$\alpha_\mathrm{w,s} = \frac{2\pi}{N} - 2 \cdot \arcsin\left(\frac{w_\mathrm{t}}{2r_\mathrm{w,s}}\right). \tag{3.132}$$

Therein, $r_\mathrm{w,s}$ and $\alpha_\mathrm{w,s}$ are auxiliary geometrical parameters that depend on the outer stator radius r_s, the yoke height h_y, and the tooth width h_t. These motor geometry parameters (r_s, h_y, and h_t) are input parameters of the proximity loss model.
Furthermore, with the row-wise numbering of conductors as indicated

in Fig. 3.21, the coordinate y_i in (3.129) is given by

$$y_i = (n_{\mathrm{t,row},i} - 1) \cdot d_\mathrm{c} + \frac{d_\mathrm{c}}{2} \tag{3.133}$$

$$n_{\mathrm{t,row},i} = i - N_{\mathrm{rows,full},i} \cdot n_{\mathrm{t,row,max}} \tag{3.134}$$

$$N_{\mathrm{rows,full},i} = \left\lfloor \frac{i-1}{n_{\mathrm{t,row,max}}} \right\rfloor \tag{3.135}$$

$$n_{\mathrm{t,row,max}} = \left\lfloor \frac{h_\mathrm{t}}{d_\mathrm{c}} \right\rfloor. \tag{3.136}$$

Therein, $n_{\mathrm{t,row},i}$ is the number of the conductors that are placed in the same row as the i-th conductor on its left/outer side including the i-th conductor itself. $N_{\mathrm{rows,full},i}$ is the number of fully populated rows of conductors underneath the i-th conductor, and $n_{\mathrm{t,row,max}}$ is the maximum number of conductors that fit into one row of conductors. The current $I_{1,2,k}(f)$ in (3.129) is given by

$$I_{1,2,k}(f) = |\underline{I}_{1,k}(f) + \underline{I}_{2,k}(f)|, \tag{3.137}$$

where $\underline{I}_{1,k}(f)$ and $\underline{I}_{2,k}(f)$ are the complex RMS spectra/phasors of the currents that flow in the conductors of the coil side 1 and 2 of the k-th stator slot, respectively. By defining $\underline{I}_{\mathrm{c},j}(f)$ as the complex RMS spectrum of the current flowing in one conductor of the j-th coil side for all coil sides in one base winding, i.e. for $j = 1, 2, \ldots, 2 \cdot N_{\mathrm{s,bw}}$, the current spectra $\underline{I}_{1,k}(f)$ and $\underline{I}_{2,k}(f)$ can be expressed as

$$\underline{I}_{1,k}(f) = \underline{I}_{\mathrm{c},j=2k-1}(f), \quad k = 1, 2, \ldots, N_{\mathrm{s,bw}} \tag{3.138}$$

$$\underline{I}_{2,k}(f) = \begin{cases} \underline{I}_{\mathrm{c},j=2k-2}(f), & k = 2, 3, \ldots, N_{\mathrm{s,bw}} \\ \underline{I}_{\mathrm{c},j=2N_{\mathrm{s,bw}}}(f), & k = 1. \end{cases} \tag{3.139}$$

where the current spectra $\underline{I}_{\mathrm{c},j}(f)$ for $j = 1, 2, \ldots, 2 \cdot N_{\mathrm{s,bw}}$ depend on the motor winding scheme and on the motor phase currents as follows:

$$\underline{I}_{\mathrm{c},j}(f) = -\mathrm{sign}(BWS_{\mathrm{num}}(j)) \cdot \frac{\underline{I}_{\mathrm{par},x(j)}(f)}{a_\mathrm{eff}}. \tag{3.140}$$

Therein, $\underline{I}_{\mathrm{par},x(j)}(f)$ is the complex RMS spectrum of the motor phase current of the reduced motor phase $x(j)$ to which the j-th coil side belongs. The parameter a_eff in (3.140) is the number of parallel paths of each reduced motor phase winding. Furthermore, $BWS_{\mathrm{num}}(j)$ in

Table 3.16: Input parameters of the proximity loss model given by (3.124)-(3.141)

$\underline{I}_{\mathrm{par},x}(f)$	Motor phase current spectrum for all reduced phases $x = 1, \ldots, m$
N	Number of stator slots
N_{bw}	Number of base windings of the motor winding
$BWS_{\mathrm{num}}(j)$	Numerical base winding scheme
a_{eff}	Number of parallel paths of the reduced phase windings
n_{t}	Number of turns of one tooth-coil
d_{c}	Conductor diameter
σ	Conductivity of the winding material
l_{s}	Stator stack length
r_{s}	Stator outer radius
h_{t}	Stator tooth/slot height
h_{y}	Stator yoke height
w_{t}	Stator tooth width

(3.140) for $j = 1, 2, \ldots, 2 \cdot N_{\mathrm{s,bw}}$ is the a numerical representation of the base winding scheme which is defined as a series of signed integer values whose absolute values indicate the phase index $x(j)$. Thus, $x(j)$ is given by

$$x(j) = |BWS_{\mathrm{num}}(j)|. \tag{3.141}$$

The sign of $BWS_{\mathrm{num}}(j)$ in (3.140) indicates the winding direction of the j-th coil side via the sign of the conductor current $i_{\mathrm{c},j}$ (i.e. $\underline{I}_{1,k}(f)$/ $\underline{I}_{2,k}(f)$ from Fig. 3.21 in the time domain) for negative phase currents ($i_{\mathrm{par},x(j)} < 0$): It is defined that $BWS_{\mathrm{num}}(j) > 0$ indicates $i_{\mathrm{c},j} > 0$ and vice versa. With this definition and with the reference direction of the conductor currents defined in Fig. 3.21, $BWS_{\mathrm{num}}(j) > 0$ indicates a conductor current flowing out of the plane and vice versa.
Overall, the proximity loss model is given by (3.124)-(3.141). A summary of the input parameters of this model is given in Tab. 3.16.
If $BWS_{\mathrm{num}}(j)$ in Tab. 3.16 is not given but if a graphical motor winding scheme is given instead, which is typically used in motor design, such a graphical winding scheme must first be transformed into $BWS_{\mathrm{num}}(j)$. Fig. 3.22 shows this transformation for an exemplary motor winding, starting with the graphical motor winding scheme in Fig. 3.22a. Extracting the winding part that repeats itself along the stator circumference in mathematically positive direction and that starts at the stator top results in the graphical base winding scheme that is shown in Fig. 3.22b. Then, transforming the symbolic phase IDs (R, S, T) into numer-

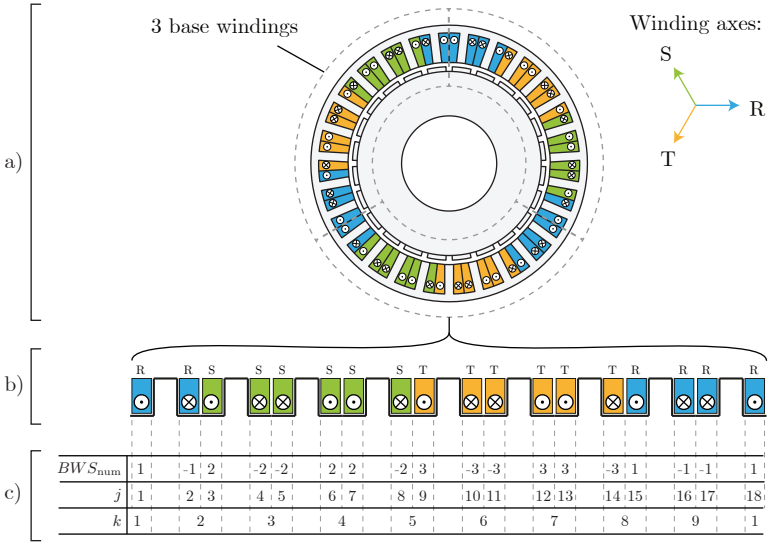


Figure 3.22: Transformation of a) the graphical motor winding scheme into b) the graphical base winding scheme and into c) the numerical base winding scheme $BWS_{\mathrm{num}}(j)$ of an exemplary double-layer tooth-coil motor winding.

ical phase IDs (1, 2, 3) and transforming the current direction symbols into signs ($\cdot \rightarrow +$, $\times \rightarrow -$) leads to the numerical base winding scheme $BWS_{\mathrm{num}}(j)$ that is given in Fig. 3.22c.

3.8 Motor Iron Loss Models

Iron losses represent another contribution to the motor losses in addition to the winding/copper losses. The iron losses in an electric motor vary with the switching frequency of the inverter: By decreasing the switching frequency from 20 kHz to 2 kHz the iron losses can double (Fig. 8 of [100]). At the same time, increasing the switching frequency leads to higher switching losses. To incorporate this trade-off in an IMD design procedure, fast and accurate iron loss models are required.
To first obtain an overview of already existing models, the state of research on iron loss modelling for electric motors was investigated which is presented in section 3.8.1. This includes a relatively large number of

iron loss density models which resulted from previous research. In order to provide a data base for the validation of existing models and for the development of improved models, iron loss density measurements with silicon steel samples were performed. The corresponding measurement results are presented in section 3.8.2. The models that were implemented for a validation against the measurement results, including existing and developed models, are presented in section 3.8.3.

3.8.1 State of Research

In this section, the state of research on iron loss modelling for electric motors is presented. The section is structured as follows: First, the scope of research is defined. Then, an overview of core loss density models from the literature is given. The most relevant core loss density models for inverter driven PMSMs are identified and the corresponding model equations are given. Finally, open research questions of the given state of research are pointed out.

Scope of Research

The research topic of iron loss modelling for electric motors is a part of the more general research topic of core loss modelling for all kinds of electrical engineering applications, also including power electronic applications such as transformers and inductors. Having a look at this larger picture of applications is beneficial because core loss models developed for other applications can also be relevant for electric motors as will be pointed out in this section.
Fig. 3.23 shows a classification of typical electrical engineering applications that require core loss modelling. The classification is based on devices, core materials, excitation waveforms, and frequency ranges. The typical devices that require core loss modelling include electrical machines (motors & generators), transformers, and inductors. Possible core materials include silicon steel, amorphous materials, nanocrystalline materials, powders, and ferrites [101]. The excitation waveform refers to the form of the magnetic flux density (B-field) and can be classified itself by the number of magnetisation axes and by the waveform of the B-field along each magnetisation axis. The predominant number of magnetisation axes in magnetic devices is one. This means that the B-field alternates along only one magnetisation axis, which is

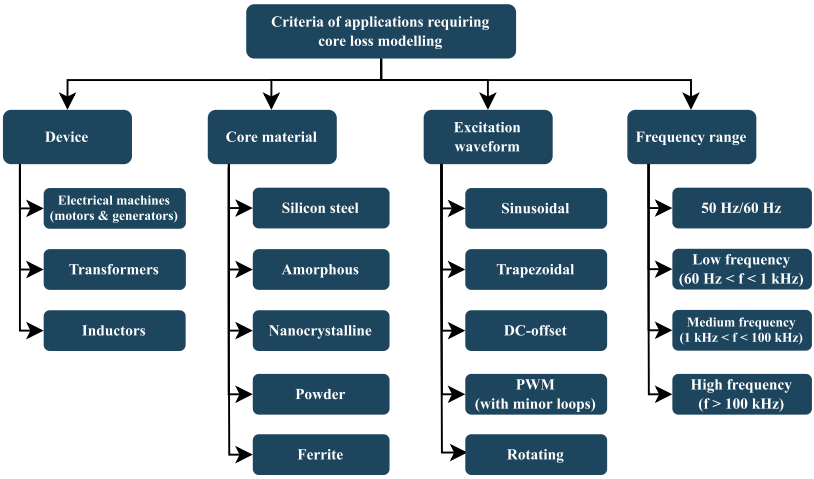


Figure 3.23: Classification of typical electrical engineering applications that require core loss modelling.

also called a uniaxial field. The field in some spots in the stator of electric machines alternates along two magnetisation axes, which is called a biaxial or rotating field [102]. Typical waveforms along one magnetisation axis include sinusoidal waves, trapezoidal waves, waves with a DC-offset, and waves consisting of a fundamental, harmonics, and minor hysteresis loops that result from the inverter operation using a PWM. This large variety in excitation waveforms goes along with a large variety in core loss models in literature as will be discussed later. Besides the variety of waveforms, there is also a variety of frequency ranges which is considered in the context of core loss modelling. The frequency ranges include 50 Hz/60 Hz for grid transformers, low frequencies ($60\,\mathrm{Hz} < f < 1\,\mathrm{kHz}$) for typical motor fundamental frequencies, medium frequencies ($1\,\mathrm{kHz} < f < 100\,\mathrm{kHz}$) as typical switching frequencies in inverter driven motors, and high frequencies ($f > 100\,\mathrm{kHz}$) in high-frequency transformers e.g. for radio transmitters.
In terms of devices and materials, the focus of the presented state of research is on core loss models for electric machines with a core (stator/rotor) made of laminated silicon steel. As silicon steel is an iron based alloy, silicon steel cores are also referred to as iron cores and the corresponding core loss models as iron loss models. Silicon steel

is widely used for electrical machines produced in large volumes due to its cost-effectiveness and its relatively high saturation flux density. However, the models presented in the next section are not strictly limited to models originally developed for motors with an iron/silicon steel core but can also include core loss density models that have been developed for inductors or transformers of different materials (e.g. the iGSE). The motivation for this is to simplify the development of better iron loss models by a possible transfer of models across different materials. Despite the fact that different core materials have different material properties, the phenomena of eddy currents and hysteresis can be identified as basic universal phenomena that lead to core losses in any core material.
In terms of waveforms, the focus and goal of the presented state of research is to identify the most relevant models suitable for inverter driven PMSMs, hence for PWM waveforms. Therefore, an overview of iron loss models from the literature is presented in the following section, including a comparison of models with regard to the covered waveforms. Based on this comparison the most relevant models suitable for inverter driven PMSMs are identified and discussed in the subsequent section.

Overview of Iron Loss Models from the Literature

Fig. 3.24 shows a classification of iron loss models for electric motors from the literature. The models can be separated into global iron loss models and local iron loss models.
In global iron loss models, the iron losses are calculated from the motor phase voltages that result from the entire/global magnetic field distribution in the motor. An example for a global iron loss model is the harmonic loss factor method [103]. The harmonic loss factor is defined as the frequency dependent ratio between the iron losses caused by each voltage harmonic and the square of the harmonic voltage amplitude. The harmonic loss factor curves over the harmonic frequency are determined based on motor loss measurements and are motor specific as can be seen in Fig. 4 of [103]. Therefore, the harmonic loss factor method can be useful for two cases: 1) To accurately predict iron losses for an already existing motor prototype. 2) To roughly estimate iron losses of motors in the design phase using the harmonic loss factor curves of a similar motor. However, the harmonic loss factor method is not useful for an accurate prediction of iron losses of motors in the motor/IMD design phase. This use case requires local iron loss models.

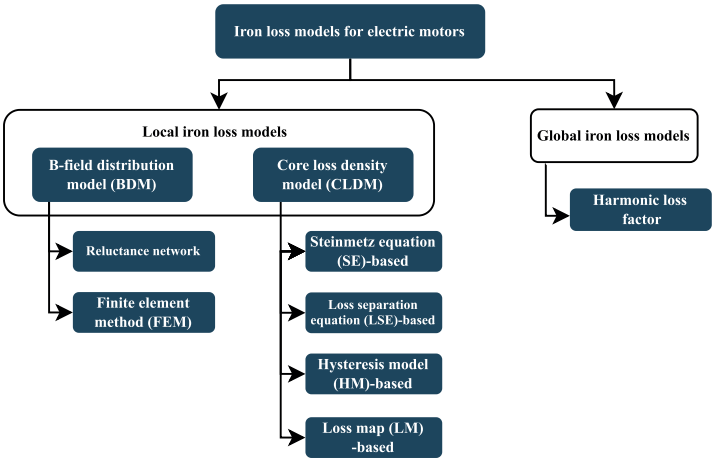


Figure 3.24: Classification of iron loss models for electric motors.

In local iron loss models, the iron losses are calculated in three steps: 1) The B-field distribution in the motor is calculated using a B-field distribution model (BDM). 2) The local iron/core loss density is calculated using a core loss density model (CLDM). 3) The iron/core loss density is integrated over the core (stator/rotor) volume resulting in the iron losses.

BDMs can be separated into reluctance network models and models based on the finite element method (FEM). Reluctance network models are based on the division of the magnetic core (stator/iron) into flux tubes in which the magnetic field (B/H) is assumed to be uniform and uniaxial. No such assumption is made using FEM that however requires a larger computational effort than reluctance network models. An important property of each BDM is the used B(H)-model (BHM). Commonly used BHMs are 1) a linear BH-curve corresponding to a constant permeability, 2) a non-linear BH-curve accounting for saturation, and 3) hysteresis models.

CLDMs are the predominant topic in the literature about core/iron loss modelling. A relatively large number of CLDMs exists which can be separated into four categories [104] that are shown in Fig. 3.24: 1) CLDMs based on the Steinmetz equation (SE). 2) CLDMs based on the

loss separation equation (LSE). 3) CLDMs based on a hysteresis model (HM). 4) CLDMs based on a measured loss map (LM). Similar classifications of CLDMs can be found in review papers on iron/core loss modelling [101, 105]. The first two model categories are considered the most important categories for fast and accurate iron loss modelling in the motor/IMD design phase because they typically require less computational effort than hysteresis models such as Preisach or Jiles-Atherton and less measurement effort than loss maps. Therefore, the following presentation of CLDMs focuses on SE- and LSE-based CLDMs.
The SE in its commonly used form [106–108] is given by

$$p_{\mathrm{c,SE}} = k f^{\alpha} B_{\mathrm{m}}^{\beta}. \tag{3.142}$$

There, $p_{\mathrm{c,SE}}$ is the core loss density in $\mathrm{W\,kg^{-1}}$, f is the frequency, B_{m} is the peak flux density and k, α, and β are the Steinmetz parameters. The original LSE, also called Bertotti equation as it was introduced by Bertotti in [109], is given by

$$p_{\mathrm{c,LSE}} = k_{\mathrm{h}} f B_{\mathrm{m}}^{\alpha} + k_{\mathrm{cl}} f^2 B_{\mathrm{m}}^2 + k_{\mathrm{ex}} f^{1.5} B_{\mathrm{m}}^{1.5}. \tag{3.143}$$

There, the core loss density $p_{\mathrm{c,LSE}}$ is separated into hysteresis losses, classical eddy current losses, and excess (eddy current) losses, described by the corresponding loss coefficients k_{h} and α, k_{cl}, and k_{ex}.
When the SE and the LSE are compared, the LSE is used more often for laminated steel, whereas the SE is typically used for ferrites [110]. Both, SE and LSE, are typically used as empirical approaches by fitting the loss coefficients to measurement results. However, the LSE approach is the more physical approach due to the loss separation by physical phenomena. The hysteresis losses result from the phenomenon of magnetic domain wall movement described by the Barkhausen jumps. The classical eddy current losses result from ohmic losses. The cause of excess losses, mainly investigated for laminated steel, is less evident and different explanations are given in the literature. One explanation is that the excess losses are due to additional eddy currents caused by magnetic domain wall bowing [111–113]. Another explanation is that the excess losses are due to the non-uniform magnetic field distribution resulting from the skin effect and the non-linear diffusion of magnetic flux from the boundary to the inside of a lamination [114].
The SE and the LSE are only suitable for loss modelling with sinusoidal uniaxial excitation waveforms at a constant temperature. Therefore, more advanced SE-based and LSE-based CLDMs have been developed

Table 3.17: Overview and comparison of CLDMs from the literature. SoI: Source where the CLDM was introduced (source of introduction). YoI: Year in which the CLDM was introduced (year of introduction). SoV: Additional source(s) in which the CLDM is validated/compared against other CLDMs (source of validation).

Name	Included loss effects						SoI	YoI	SoV
	Harmonics	DC bias	Minor loops	Rotation	Relaxation	Temperature			
SE	✗	✗	✗	✗	✗	✗	[106].(2.74)	1988	[115, 116]
MSE	✓	✓	✗	✗	✗	✗	[117].(5,7)	2001	[115, 116]
GSE	✓	✓	✗	✗	✗	✗	[118].(12)	2001	-
iGSE	✓	✗	✓	✗	✗	✗	[119].(9-10)	2002	[115, 116]
EEL-SE	✓	✓	✓	✗	✗	✗	[110].(15-17)	2004	-
RC-EEL-SE	✓	✓	✓	✓	✗	✗	[110].(15-17,21)	2004	[116]
WcSE	✓	✗	✗	✗	✗	✗	[120].(7)	2008	[115, 116]
i^2GSE	✓	✗	✓	✗	✓	✗	[104].(15-17)	2012	-
iGSE+SPG	✓	✓	✓	✗	✗	✓	[121].Fig10	2012	-
LSE	✗	✗	✗	✗	✗	✗	[109].(11)	1988	[122]
LSE2	✓	✗	✗	✗	✗	✗	[123]	1992	[122]
LSE3	✗	✗	✗	✗	✗	✗	[124].(5, Tab.III)	2003	[122]
EEL-LSE	✓	✓	✓	✗	✗	✗	[110].(5,9-14)	2004	-
RC-EEL-LSE	✓	✓	✓	✓	✗	✗	[110].(5,9-14,18-20)	2004	-
RM-LSE4	✓	✗	✓	✓	✗	✗	[102].(1-7,"P1P2")	2005	-
LSE5	✗	✗	✗	✗	✗	✗	[125].(3)	2007	[122]
LSE6	✗	✗	✗	✗	✗	✓	[126].(9)	2015	[122]
LSE7	✓	✗	✗	✗	✗	✗	[127].(Tab6.4, row 4)	2016	-
LSE8	✗	✓	✗	✗	✗	✓	[128].(7-8)	2017	[122]
RM-LSE9	✓	✗	✓	✓	✗	✓	[100].(4-7, 9)	2017	[122]
LSE10	✗	✗	✗	✗	✗	✓	[129].(6)	2018	[122]
RM-LSE11	✓	✓	✓	✓	✗	✓	[130].(7.17-7.22)	2018	-
RC-LSE10	✗	✗	✗	✓	✗	✓	[122].(11,12)	2019	-
RM-LSE10	✗	✗	✗	✓	✗	✓	[122].(11,13)	2019	-
LSE12	✗	✓	✗	✗	✗	✗	[122](14,15)	2019	-
LSE13	✓	✗	✗	✗	✗	✗	[131].(23)	2020	[132]
LSE14	✓	✓	✗	✗	✗	✗	[132].(18,27-28)	2021	-
LSE15	✓	✓	✗	✗	✗	✗	[132].(18,20-28)	2021	-

in the literature which are considered in the following.
Tab. 3.17 shows an overview of CLDMs from the literature, separated into SE-based CLDMs and LSE-based CLDMs. For each of these categories, the CLDMs are sorted by the year in which the CLDMs were introduced, given in the column *YoI*. The CLDMs are compared with regard to the loss effects that are covered by the models. The following loss effects are considered in Tab. 3.17:

- *Harmonics:* The earliest CLDMs such as the SE and the LSE consider only sinusoidal B-field waveforms. However, with the emergence of inverter driven machines and switched power electronic converters, the excitation currents and B-fields usually consist of multiple harmonics. These harmonics cause additional eddy current losses which are taken into account by most of the more recently introduced CLDMs as shown in Tab. 3.17.

- *DC bias:* Iron losses can increase by 50 % due to a DC bias in the B-field waveform [121]. Typical applications with a DC-biased B-field waveform are DC-DC converters as for example boost converters. In contrast, in electrical machines the typical current waveform and hence the typical B-field waveform is a fundamental at low frequency ($60\,\mathrm{Hz} < f < 1\,\mathrm{kHz}$) with additional harmonics at medium frequency ($1\,\mathrm{kHz} < f < 100\,\mathrm{kHz}$) due to the PWM. As the change of the fundamental component of the current/B-field is small during one period of the medium frequency components, the fundamental component can be considered as a slowly changing DC bias.

- *Minor loops:* In inverter driven machines, low switching frequencies lead to minor hysteresis loops (further called minor loops) in the B-/H-field which lead to additional hysteresis losses [100]. The most common approach to model the effect of minor loops on the iron losses is to apply a minor loop detection procedure in the time domain, as for example described in [119]. This is also the case for the CLDMs in Tab. 3.17, for which the minor loop effect is marked as included. An alternative approach is to calculate hysteresis losses for each harmonic component without a minor loop detection procedure [131]. This approach is expected to have less computational effort at the cost of lower accuracy because not all harmonic components of a B-field waveform cause minor loops.

- *Rotation:* In most parts of the stator of an electrical machine, i.e. in the stator teeth and the stator yoke between the teeth, the flux density is approximately uniaxial as it is oriented in the direction of the teeth or in the direction of the yoke. However, in the area of the yoke above the teeth, the flux density can be biaxial/rotating , which leads to additional iron losses [102]. In Tab. 3.17, the CLDMs that include this rotation related loss effect have the prefix *RC* or *RM*, where the former indicates that the rotational B-field is expressed in Cartesian coordinates and the latter indicates that the rotational B-field is expressed in a local coordinate system defined by the minor/major axes of a B-field ellipsis [102].

- *Relaxation:* A common assumption in the development of SE-based CLDMs is that iron/core losses are linked to the rate of change of the flux density $\mathrm{d}B/\mathrm{d}t$. However, [104] shows that losses also occur at $\mathrm{d}B/\mathrm{d}t = 0$, which is explained by a relaxation effect in the core material. This finding leads to the introduction of the i^2GSE [104].

- *Temperature:* Iron losses in electrical machines are significantly influenced by the temperature due to the temperature dependency of the conductivity and of the magnetic permeability [131]. As shown in Tab. 3.17, the temperature effect on iron losses is covered by more LSE-based CLDMs than by SE-based CLDMs.

In terms of accuracy, most CLDMs from Tab. 3.17 are evaluated based on measurements in [115, 116, 122, 132]. This is also indicated in the column *SoV* in Tab. 3.17. The results can be summarised as follows:

- *Results of [116]:* Predicted core losses using the CLDMs SE, MSE, iGSE, RC-EEL-SE, and WcSE are compared to measured losses in Fig. 12 of [116]. The measurement is made with a transformer consisting of C-cores of the amorphous material Metglas AMCC-1000 POWERLITE and a square wave voltage waveform, resulting in a trapezoidal B-field, with the frequency $f = 1\,\mathrm{kHz}$ and a peak magnetic flux density of $B_\mathrm{m} = 0.6\,\mathrm{T}$. The relative ranking of CLDMs in terms of accuracy is as follows:

$$\text{iGSE} > \text{MSE} > \text{EEL-SE} > \text{WcSE} \gg \text{SE}$$

Hence, iGSE is the most accurate CLDM according to [116]. It must be noted that the measurement reported in [116] does not include any rotating fields. Therefore, the CLDM RC-EEL-SE must only be evaluated in one direction that is the direction of the magnetisation. Hence, the results presented in [116] do not allow any conclusion on the accuracy of modelling the loss effect of rotating fields.

- *Results of [115]:* Predicted core losses using the CLDMs SE, MSE, iGSE, and WcSE are compared to measured losses that result from a ring specimen test with two different applied voltage waveforms with a variable duty cycle: 1) A 2-level square voltage waveform, resulting in a triangular B-field waveform. 2) A 3-level square voltage waveform, resulting in a trapezoidal B-field waveform. In both cases the core is made of the nanocrystalline material FT-3KS. The results for two applied waveforms are shown in Fig. 6 and Fig. 7 of [115], respectively, which can be summarised by the following relative ranking in terms of accuracy:

$$\text{iGSE} > \text{MSE} > \text{WcSE} \gg \text{SE}$$

  This result is in accordance with the results from [116] presented before.

- *Results of [122]:* Different groups of CLDMs are considered separately, where each group consists of CLDMs that include the same core loss effects. To evaluate/compare the CLDMs within the different groups, different measurement setups are used by [122], called MEASS1 and MEASS2 in the following: MEASS1) Ring specimen test with adjustable temperature in the range of $40\,^{\circ}\text{C} - 100\,^{\circ}\text{C}$. MEASS2) Machine loss test based on an interior permanent magnet synchronous machine (IPMSM), where the magnets are removed and the rotor is locked to avoid any mechanical loss and any magnet eddy current loss. In both test setups, the core material is the laminated steel V300-35A.

  - *CLDMs including sinusoidal excitation:* This group of CLDMs consists of LSE1, LSE2, LSE3, and LSE5. Predicted core losses using these CLDMs are compared to measured losses that are obtained with the measurement setup MEASS1 at a constant temperature. The relative ranking of

CLDMs in terms of accuracy, resulting from Fig. 6 in [122], is as follows:

$$\text{LSE5} > \text{LSE1} \approx \text{LSE2} \approx \text{LSE3}$$

- *CLDMs including temperature:* This group of CLDMs consists of LSE6 and LSE10. Predicted losses using these CLDMs are compared to measured losses that are obtained with the measurement setup MEASS1 using the full temperature range. The relative ranking of CLDMs in terms of accuracy, resulting from Fig. 7 in [122], is as follows:

$$\text{LSE10} > \text{LSE6}$$

- *CLDMs including rotating field:* This group of CLDMs consists of RC-LSE10 and RM-LSE10. Predicted losses using these CLDMs are compared to measured losses that are obtained with the measurement setup MEASS2. The relative ranking of CLDMs in terms of accuracy, resulting from Fig. 17 in [122], is as follows:

$$\text{RM-LSE10} > \text{RC-LSE10}$$

- *CLDMs including DC bias:* This group of CLDMs consists of LSE8 and LSE12. Predicted losses using these CLDMs are compared to measured losses that are obtained with the measurement setup MEASS2. The relative ranking of CLDMs in terms of accuracy, resulting from Fig. 19 in [122], is as follows:

$$\text{LSE8} > \text{LSE12}$$

- *CLDMs including minor loops:* The only CLDM considered in [122] which includes minor loops is RM-LSE9. The CLDM RM-LSE10 does not include minor loops, but it is included in the comparison to measurement results in [122]. The relative ranking of CLDMs in terms of accuracy, resulting from Fig. 22 in [122] and measurement setup MEASS2, is as follows:

$$\text{RM-LSE9} > \text{RM-LSE10}$$

- *Results of [132]:* Predicted core losses using the CLDMs LSE13, LSE14, and LSE15 are compared to measured losses. The measurement is based on a dual transformer system consisting of

two identical ring core samples made of electrical steel of 0.5 mm thickness (lamination type not specified). The relative ranking of CLDMs in terms of accuracy, resulting from Fig. 21 of [132] is as follows:

$$\text{LSE15} > \text{LSE14} > \text{LSE13}$$

Based on the given overview of CLDMs in terms of the included loss effects and in terms of relative accuracy, the most relevant models for inverter driven PMSMs are determined in the following section.

Most Relevant Models Suitable for Inverter Driven PMSMs

The most relevant CLDMs suitable for inverter driven PMSMs should 1) include as many loss effects from Tab. 3.17 as possible, 2) have a relatively high accuracy, and 3) have a relatively low computational effort.
With regard to the included loss effects, Tab. 3.17 shows that no CLDM covers all six considered loss effects. In particular, only one model (i^2GSE) includes the relaxation loss effect. Five of six loss effects are covered by the model RM-LSE11 and four of six loss effects are covered by the models RC-EEL-SE, iGSE+SPG, RC-EEL-LSE, and RM-LSE9.
With regard to the accuracy, the relative accuracy comparison in the previous section has shown that EEL-SE is less accurate than iGSE. As the models RC-EEL-SE and RC-EEL-LSE are based on the same approach of the equivalent elliptical loop (EEL) [110], they are assumed to be less accurate than the model iGSE+SPG.
With regard to the computational effort, the literature on iron loss modelling provides only little information. Hence, this in an open field of research. A low computational effort is important for design procedures in which the iron losses of a large number of potential designs must be evaluated.
Based on the previous considerations, the most relevant CLDMs suitable for inverter driven PMSMs are iGSE+SPG, RM-LSE9, and RM-LSE11 which are summarised in the following:

- *iGSE+SPG:* This CLDM corresponds to the improved generalised Steinmetz equation (iGSE) [119], extended by the concept of the Steinmetz premagnetisation graph (SPG) [121]. With this

CLDM, the core loss density is given by

$$p_{\mathrm{c,iGSE+SPG}} = \frac{k_{\mathrm{i}}(H_{\mathrm{DC}},\vartheta)}{T}\int_0^T \left|\frac{dB}{dt}\right|^{\alpha(H_{\mathrm{DC}},\vartheta)} \cdot |\Delta B|^{\beta(H_{\mathrm{DC}},\vartheta)-\alpha(H_{\mathrm{DC}},\vartheta)}\,dt. \quad (3.144)$$

There, T is the period of the periodic B-field waveform and ΔB is the peak-to-peak flux density of the innermost minor hysteresis loop. The sequence of values for ΔB can be determined based on the minor loop detection procedure described in [119]. The parameters $k_{\mathrm{i}}(H_{\mathrm{DC}},\vartheta)$, $\alpha(H_{\mathrm{DC}},\vartheta)$, and $\beta(H_{\mathrm{DC}},\vartheta)$ in (3.144) are the iGSE parameters from [119], extended by their dependency on the DC bias of the magnetic field H_{DC} and on the temperature ϑ [121]. An SPG is a graph that shows this dependency of the iGSE parameters, as for example shown in Fig. 10 of [121]. In an SPG, the $(H_{\mathrm{DC}},\vartheta)$-dependent iGSE parameters are typically normalised to the (original) iGSE parameters $k_{\mathrm{i},0}$, α_0, and β_0 which are obtained at zero DC bias and at an arbitrary reference temperature. The parameter $k_{\mathrm{i},0}$, as defined in [119], is given by

$$k_{\mathrm{i},0} = \frac{k_0}{2^{\beta_0-\alpha_0}(2\pi)^{\alpha_0-1}\int_0^{2\pi}|\cos\theta|^{\alpha_0}}. \quad (3.145)$$

The parameters k_0, α_0, and β_0 are the same parameters as in the SE.

- *RM-LSE9:* With this CLDM, introduced in [100], the core loss density is given by

$$p_{\mathrm{c,RM-LSE9}} = p_{\mathrm{c,maj}} + p_{\mathrm{c,min}} \quad (3.146)$$

There, $p_{\mathrm{c,maj}}$ and $p_{\mathrm{c,min}}$ are the core loss densities in the major axis and in the minor axis of the local B-field. The major axis is defined as the magnitude weighted mean direction of the biaxial/2D B-field [100, 102]. The minor axis is the orthogonal axis. The core loss density in the major axis is given by

$$p_{\mathrm{c,maj}} = k_{\mathrm{minloop,maj}}k_{\mathrm{h}}(f_1,B_{\mathrm{maj,m}},\vartheta)f_1B_{\mathrm{maj,m}}^2 + \sum_i k_{\mathrm{e}}(f_i,B_{\mathrm{maj,m}},\vartheta){f_i}^2B_{\mathrm{maj,m}}^2. \quad (3.147)$$

There, f_1 is the fundamental frequency, f_i is the i-th harmonic frequency, $B_{\mathrm{maj,m}}$ is the B-field in the major axis, ϑ is the temperature, and $k_{\mathrm{h}}(f, B_{\mathrm{maj,m}}, \vartheta)$ and $k_{\mathrm{e}}(f, B_{\mathrm{maj,m}}, \vartheta)$ are the hysteresis loss coefficient and the eddy current loss coefficient, respectively. These coefficients are defined frequency-, flux density-, and temperature-dependent and are determined from standard loss measurements with sinusoidal excitation. The factor $k_{\mathrm{minloop,maj}}$ takes the effect of minor loops (in the major B-field axis) into account and is given by

$$k_{\mathrm{minloop,maj}} = 1 + k \frac{1}{B_{\mathrm{m,maj}}} \sum_{j=1}^{N_{\mathrm{maj}}} \Delta B_{j,\mathrm{maj}}. \tag{3.148}$$

There, $B_{\mathrm{m,maj}}$ is the peak flux density, N_{maj} is the number of minor loops, and $\Delta B_{j,\mathrm{maj}}$ is the peak-to-peak flux density of the j-th minor loop in the major axis, as for example shown in Fig. 1 of [100]. The parameter k can be used as a fitting factor and has a value between 0.6 and 0.7 for most laminated steels [100]. The core loss density in the minor axis $p_{\mathrm{c,min}}$ in (3.146) is calculated in an analogue manner.

- *RM-LSE11:* With this CLDM, introduced in [130] as stator iron loss model, the core loss density is given by

$$p_{\mathrm{c,RM-LSE11}} = p_{\mathrm{h}} + p_{\mathrm{cl}} + p_{\mathrm{ex}}. \tag{3.149}$$

There, p_{h} is the hysteresis loss component, p_{cl} is the classical eddy current loss component, and p_{ex} is the excess loss component. The hysteresis loss component is calculated with

$$p_{\mathrm{h}} = p_{\mathrm{h,maj}} + p_{\mathrm{h,min}} \cdot \left(R_{\mathrm{h}}(\tilde{J}_{\mathrm{maj}}) - 1 \right). \tag{3.150}$$

There, $p_{\mathrm{h,maj}}$ and $p_{\mathrm{h,min}}$ are the hysteresis loss contributions of the B-field components in the major/minor axis. The major axis in RM-LSE11 is defined as the B-field axis, in which the B-field has its maximum. The minor axis is the orthogonal axis. Furthermore, the rotational loss factor $R_{\mathrm{h}}(\tilde{J}_{\mathrm{maj}})$ is used that takes the additional losses due to a rotating field into account and that depends on the half-amplitude (peak-to-DC) of the magnetic polarisation $\tilde{J}_{\mathrm{maj}}$. For the definition of $R_{\mathrm{h}}(\tilde{J}_{\mathrm{maj}})$, it is referred to

(7.18) of [130] to keep this model summary short.
The hysteresis loss density in the major axis $p_{\mathrm{h,maj}}$ in (3.150) is given by

$$p_{\mathrm{h,maj}} = \frac{1}{T} \cdot \left(W_{\mathrm{h}}(\tilde{J}_{\mathrm{maj}}, J_{\mathrm{maj,DC}}) + \sum_{i=1}^{N} W_{\mathrm{h}}(\tilde{J}_{\mathrm{maj},i}, J_{\mathrm{maj,DC},i}) \right). \tag{3.151}$$

There, the first W_{h}-term accounts for the hysteresis loss energy of the major loop and the second W_{h}-term accounts for the hysteresis loss energies of the minor loops. Both terms use the same loss formula for the hysteresis losses which is given by

$$W_{\mathrm{h}}(\tilde{J}, J_{\mathrm{DC}}) = F_{\mathrm{D}}(J_{\mathrm{DC}}) \cdot W_{\mathrm{h}}(\tilde{J}). \tag{3.152}$$

There, $W_{\mathrm{h}}(\tilde{J})$ is the hysteresis loss energy at zero DC bias and $F_{\mathrm{D}}(J_{\mathrm{DC}})$ is a displacement factor that takes the hysteresis loss dependency on the polarisation DC bias J_{DC} into account. To determine $W_{\mathrm{h}}(\tilde{J})$ and $F_{\mathrm{D}}(J_{\mathrm{DC}})$, hysteresis curves at different values for the polarisation DC bias J_{DC} and for the polarisation peak-to-DC amplitude $\tilde{J}$ must be measured. The resulting hysteresis loss energies/loop areas are then used for a curve fitting to express $W_{\mathrm{h}}(\tilde{J})$ and $F_{\mathrm{D}}(J_{\mathrm{DC}})$ with the following analytical curve equations:

$$W_{\mathrm{h}}(\tilde{J}) = \sum_{n=1}^{N} k_{\mathrm{h,n}} \tilde{J} \tag{3.153}$$

$$F_{\mathrm{D}}(J_{\mathrm{DC}}) = 1 + k_{\mathrm{DC}} J_{\mathrm{DC}}^{\beta} + k_{\mathrm{l}} J_{\mathrm{DC}}^{2}. \tag{3.154}$$

There, the coefficients $k_{\mathrm{h,n}}$, k_{DC}, β, and k_{l} result from the curve fitting.
The hysteresis loss density in the minor axis $p_{\mathrm{h,min}}$ in (3.150) is calculated in an analogue manner.
The classical eddy current losses p_{cl} in (3.149) are given by

$$p_{\mathrm{cl}} = F_{\mathrm{s}}(\gamma_{\mathrm{eq}}) \cdot \frac{\sigma(\vartheta) \cdot d^2}{12 \cdot \rho_{\mathrm{m}}} \cdot \frac{1}{T} \cdot \int_0^T \left(\left(\frac{\mathrm{d}B_{\mathrm{maj}}}{\mathrm{d}t} \right)^2 + \left(\frac{\mathrm{d}B_{\mathrm{min}}}{\mathrm{d}t} \right)^2 \right) \mathrm{d}t. \tag{3.155}$$

There, $F_\mathrm{s}(\gamma_\mathrm{eq})$ is a factor that takes the skin effect into account and that depends on the equivalent normalised skin depth γ_eq that is defined in (7.20) of [130]. The parameters $\sigma(\vartheta)$, d, and ρ_m in (3.155) are the temperature-dependent conductivity, thickness, and density of the steel laminations, respectively.
The excess losses p_ex in (3.149) are given by

$$p_\mathrm{ex} = p_\mathrm{ex,maj} + p_\mathrm{ex,min} \cdot \left(R_\mathrm{ex}(\tilde{J}_\mathrm{maj}) - 1 \right). \tag{3.156}$$

Similar to the rotational loss factor R_h in (3.150), the factor R_ex incorporates the additional excess losses due to a rotating field. For the definition of $R_\mathrm{ex}(\tilde{J}_\mathrm{maj})$, it is referred to (7.22) of [130]. The excess loss density in the major axis $p_\mathrm{ex,maj}$ is given by

$$p_\mathrm{ex,maj} = k_\mathrm{ex}(\tilde{J}) \cdot \frac{1}{T} \cdot \int_0^T \left| \frac{\mathrm{d}J_\mathrm{maj}}{\mathrm{d}t} \right|^{1.5}. \tag{3.157}$$

There, k_ex is the excess loss coefficient that is determined from standard sinusoidal loss measurements. The excess loss density in the minor axis $p_\mathrm{ex,min}$ in (3.156) is calculated in an analogue manner.

Open Research Questions Resulting from the Literature Review

The previous sections have shown that a lot of approaches for iron loss modelling in electrical machines and for core loss modelling in general are given in literature. Nevertheless, the following points require further investigation:

- As shown in Tab. 3.17, no CLDM is found in the literature which includes all of the considered core loss effects (harmonics, DC bias, minor loops, rotational fields, relaxation losses, and temperature).
- An evaluation of the CLDMs with regard to the computational effort is missing. A low computational effort is important for design procedures in which a relatively large number of virtual designs must be evaluated.
- The previously identified most relevant CLDMs for inverter driven PMSMs (iGSE+SPG, RM-LSE9, RM-LSE11) certainly represent an improvement compared to previous CLMDs. However, they remain suboptimal with regard to the following aspects:

- *iGSE+SPG:* In [121], where the CLDM iGSE+SPG is introduced, this CLDM is only validated based on measurements with ferrites. According to [121], measurements with silicon steel are performed but a comparison of predicted losses and measured losses for silicon steel is not shown. Hence, an evaluation of the model accuracy for silicon steel is missing.
- *RM-LSE9:* In general, minor hysteresis loops can occur at any B-field value of the low-frequency fundamental that defines the slowly changing DC bias. In the CLDM RM-LSE9, introduced in [100], the DC bias is not taken into account individually for each minor loop but for all minor loops in total by means of the factor k in (3.148). Therefore, it is questionable weather the single factor k leads to accurate results also for different amplitudes of the B-field fundamental, i.e. for different load points of a machine.
- *RM-LSE11:* The validation of the CLDM RM-LSE11, introduced in [130], is limited to frequencies $\leq 1\,\mathrm{kHz}$. Hence, a validation for typical PWM frequencies ($1\,\mathrm{kHz} < f < 100\,\mathrm{kHz}$) is missing. Furthermore, a validation for rotating fields is missing as the measurements reported in [130] are based on the Epstein frame test, i.e. on uniaxial fields. In addition, only the eddy current losses in RM-LSE11 are considered to be temperature-dependent. Hence, no temperature dependency of the hysteresis losses or of the excess losses is taken into account.

3.8.2 Performed Iron Loss Measurements

To validate existing iron loss models and to develop improved models, three series of iron loss density measurements were performed which are referred to as MeasSin, MeasSinDC, and Meas-STx in the following. The different measurement series were done using different excitation waveforms and ring samples of different types of silicon steel sheets. An overview of all the silicon steel sheet types used in the different measurement series is given in Tab. 3.18.
The used excitation waveforms are 1) sinusoidal and 2) sinusoidal with a DC bias. An overview of the performed measurement series with the respectively used sheet types and excitation waveforms is given in Tab. 3.19.

Table 3.18: Overview of silicon steel sheet types (ST) used for different iron loss density measurements.

x: ID of sheet type	Grade	Manufacturer
1	M330-35A	n.a.
2	M470-50A	n.a.
3	M330-35A	Wälzholz
4	M235-35A	Wälzholz
5	M270-50A	Wälzholz
6	M400-50AP	ThyssenKrupp
7	M530-50A	Wälzholz
8	M800-50A	Wälzholz
9	NO10	Wälzholz
10	NO20-15	Wälzholz

Table 3.19: Overview of the performed measurement series.

ID of measurement series	Excitation waveform	ID of used sheet type
MeasSin	Sinusoidal	1
MeasSinDC	Sinusoidal with DC bias	1
Meas-STx	Sinusoidal with/without DC bias	2-10 ($= x$)

For each of these measurement series, the used measurement setup and the measurement results are presented in the following.

Iron Loss Measurements with Sinusoidal Excitation (MeasSin)

Fig. 3.25 shows the used core loss measurement setup. The setup consists of a *SY-8219* B-H analyser by IWATSU, a *SY-5001* power amplifier by IWATSU, and a *SU-242* temperature chamber by Espec. Fig. 3.25 also shows a DC bias extension that consists of a *SY-960* DC bias tester, a *SY-961* DC bias source, and a *SY-962* AC blocker by IWATSU. The DC bias extension is not used for this first measurement series.
The core loss measurement concept is based on the known two-coil method, in which a primary winding magnetises a core and a secondary winding, that is wound around the same core, is used to determine the flux density in the core via the secondary voltage. The iron losses re-

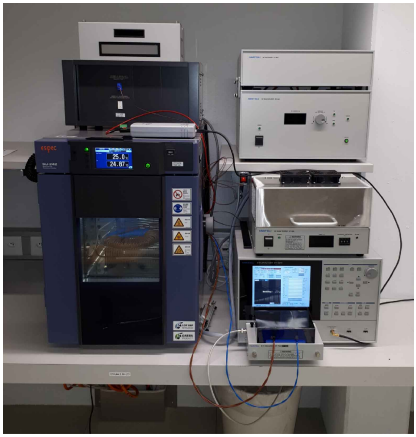
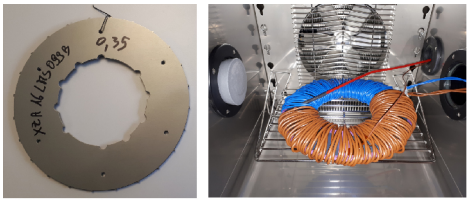


Figure 3.25: Core loss measurement setup.



(a) (b)

Figure 3.26: Sample used for iron loss measurements. a) Sample core consisting of a stack of silicon steel sheets. b) Wound sample within the temperature chamber.

sult from the measured secondary voltage and the measured primary current.

Fig. 3.26a shows the used sample core that consists of five stacked sheets of the silicon steel M330-35a. These sheets are rotor sheets that are normally used for laminated rotors of PMSMs. Such rotor sheets were chosen because they have no air gap (which would lead to an undesired fringing field) and because they were readily available from electrical machine manufacturers. Fig. 3.26b shows the wound sample with the (brown) primary winding and the (blue) secondary winding within the temperature chamber. Fig. 3.26b also shows the cables of

Table 3.20: Specifications of the sample used for iron loss measurements.

Material	M330-35a
Sheet thickness	0.35 mm
Number of sheets	5
Mean length	394 mm
Mean cross-sectional area	69 mm^2
Weight	218 g
Primary turn number	100
Secondary turn number	100

two temperature sensors that are mounted on the surface of the sample core. The sample specifications are summarised in Tab. 3.20.
Manufacturers of silicon steel usually provide iron loss density curves for frequencies in the low frequency range ($\leq$ 1 kHz) in the material data sheets. However, typical PWM frequencies are in the range of 1 kHz to 100 kHz. Therefore, this frequency range was chosen for the iron loss measurements that were performed with the described test setup.
Fig. 3.27a shows the measured iron loss density curves over the peak flux density B_m for all considered frequencies that are in the range of 50 Hz to 100 kHz. Fig. 3.27b shows a zoom on the iron loss density curves at high frequencies (10 kHz $\leq f \leq$ 100 kHz). For each iron loss curve at a given frequency, the maximum measured peak flux density is limited by the setup specifications ($V_\mathrm{out,max} = 150\,\mathrm{V}$, $i_\mathrm{out,max} = 6\,\mathrm{A}$) and by the thermal constraint that the temperature increase of the sample due to the iron losses is kept below 5 °C.
The measured iron loss density curves are used for the comparison and the development of iron loss density models, which is presented in section 3.8.3.

Iron Loss Measurements with Sinusoidal + DC Bias Excitation (MeasSinDC)

Iron loss measurements with DC-biased sinusoidal B-field waveforms were performed with the core loss measurement setup shown in Fig. 3.25, including the DC bias extension (*SY-960* DC bias tester, *SY-961* DC bias source, *SY-962* AC blocker). The specifications of the DC bias extension impose a minimum waveform frequency of 10 kHz for the superimposed sinusoidal component.

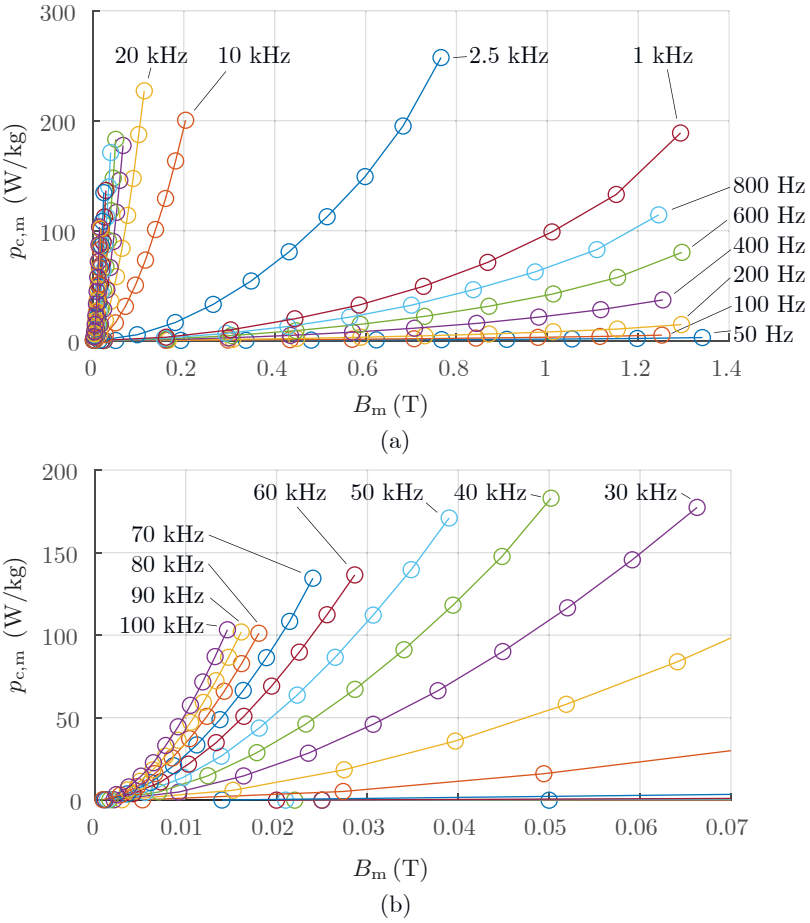


Figure 3.27: Measured iron loss density curves with sinusoidal excitation at $\vartheta = 25\,°\mathrm{C}$. a) Measurement results for all considered frequencies. b) Zoom on the higher frequencies.

Fig. 3.28 shows the measured iron loss density curves at 25 °C for DC bias values between 0 T and 1 T in steps of 0.2 T and for frequencies between 10 kHz and 100 kHz in steps of 10 kHz. From Fig. 3.28, it can be concluded that the basic form of the iron loss density curves does not change with different DC bias values. To investigate the impact

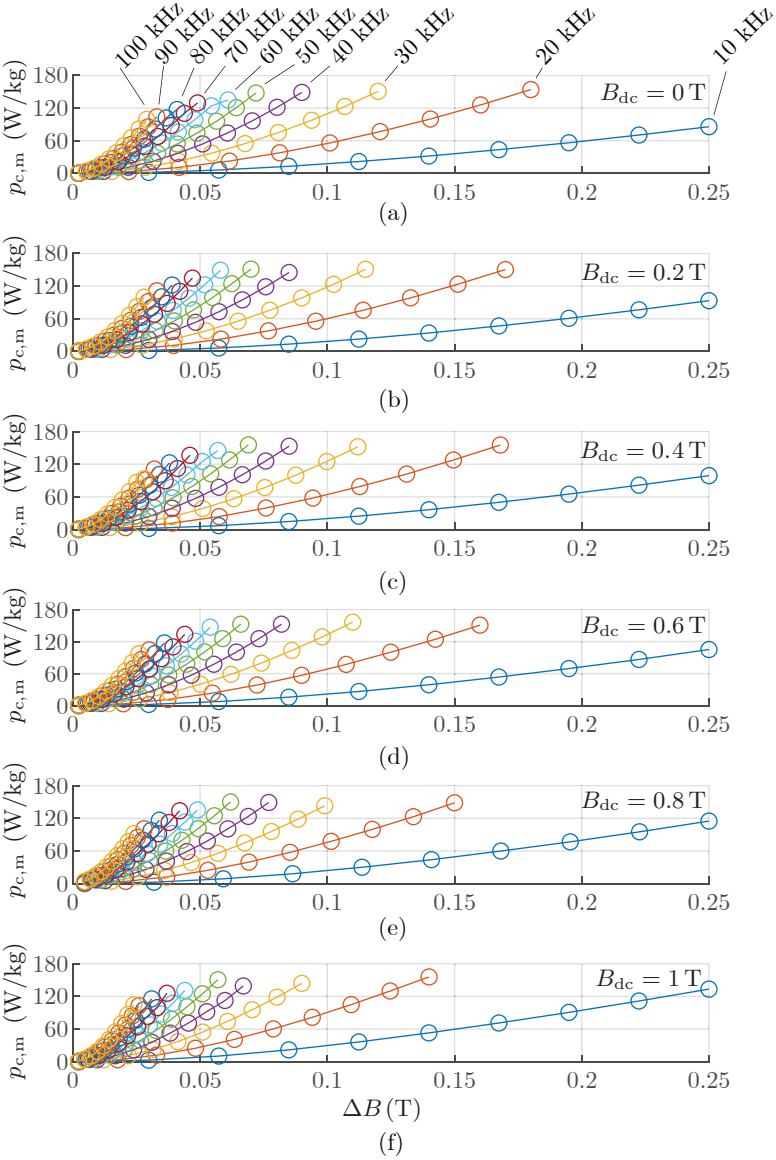


Figure 3.28: Measured iron loss density curves with sinusoidal + DC bias excitation at $\vartheta = 25\,°C$. a)-f) Different DC bias values as indicated.

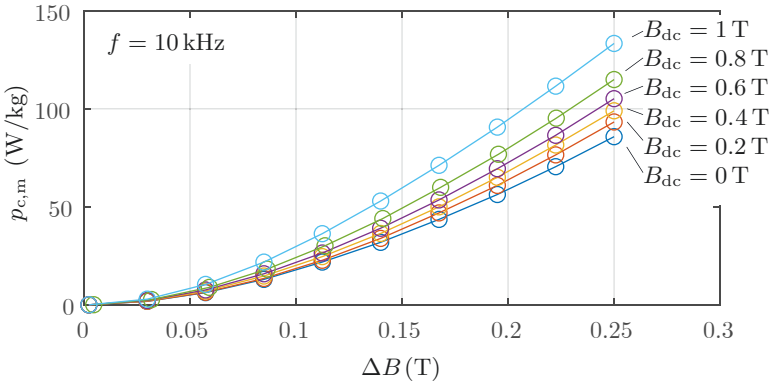


Figure 3.29: Measured iron loss density curves with sinusoidal + DC bias excitation at $\vartheta = 25\,^{\circ}\mathrm{C}$ and $f = 10\,\mathrm{kHz}$ for different values of the DC bias ΔB.

of the DC bias more closely, Fig. 3.29 compares the iron loss density curves for the different DC bias values at a single frequency (10 kHz). As expected with [121], Fig. 3.29 shows that the iron loss density increases with the DC bias. Such an increase is found for all considered frequencies.
To investigate the impact of the temperature as well, the measurement series is repeated at 60 °C (limited by the cable insulation). Based on the core loss density curves at 25 °C from Fig. 3.28 and analogue curves at 60 °C, the average increase in the iron loss density with the DC bias was calculated and the result is shown in Fig. 3.30. This result shows that the DC bias B_{dc} has a significant impact on the iron loss density with loss density increases between 8 % and 55 % for B_{dc} between 0.2 T and 1 T. In addition, Fig. 3.30 shows that the loss density increase with B_{dc} does not change significantly between 25 °C and 60 °C.
The measured iron loss density curves are used for the comparison and the development of iron loss density models, which is presented in section 3.8.3.

Iron Loss Measurements for Various Sheet Types (Meas-STx)

With the measurement series Meas-STx, the iron loss measurements were extended to a number of different types of silicon steel sheets which

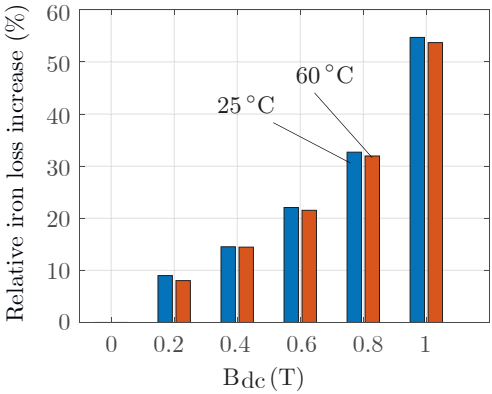


Figure 3.30: Average increase of the measured iron loss density with the DC bias B_{dc} at different temperatures.

Table 3.21: Parameters of the measurement series MeasSin-STx and MeasSinDC-STx.

	MeasSin-STx
Frequencies f (kHz)	0.01, 0.05, 0.2, 0.4, 0.6, 0.8, 1, 1.5, 2, 2.5, 3, 4, 6, 8
Flux densities B_{m} (0-to-pk)	10 equidistant points in $[B_{\mathrm{m,min}}(x), B_{\mathrm{m,max}}(x)]$
Temperature	(25 ± 1)°C
Ring core samples	LF-sample with sheet type x (Tab. 3.22)
	MeasSinDC-STx
Frequencies f (kHz)	$10, 20, \ldots, 100$
DC bias flux densities B_{dc} (T)	$[0, 0.2, 0.4, \ldots, B_{\mathrm{dc,max}}(x)]$
AC flux densities ΔB (pk-to-pk)	10 equidistant points in $[\Delta B_{\mathrm{min}}(x), \Delta B_{\mathrm{max}}(x)]$
Temperature	(25 ± 1)°C
Ring core samples	HF-sample with sheet type x (Tab. 3.22)

are given by the sheet types $x = 2, 3, \ldots, 10$ (Tab. 3.18). Meas-STx consists of two sub-series: 1) A sub-series using sinusoidal excitation, referred to as MeasSin-STx. 2) A sub-series using DC-biased sinusoidal excitation, referred to as MeasSinDC-STx. The measurement setups of these two sub-series correspond to the measurement setups of the previously described measurement series MeasSin and MeasSinDC, respectively. The measurement parameters of MeasSin-STx and MeasSinDC-STx are summarised in Tab. 3.21.
In Tab. 3.21, $B_{\mathrm{m,min}}/\Delta B_{\mathrm{min}}$ is the lowest measurable AC flux density

Table 3.22: Specifications of the ring core samples used for the measurement series MeasSin-STx (LF-samples) and MeasSinDC-STx (HF-samples).

	LF-samples	HF-samples
Sheet type x (Tab. 3.18)	$2, 3, \ldots, 10$	$2, 3, \ldots, 10$
Number of sheets	5	5
Primary turn number	100	25
Secondary turn number	100	25

which depends on the used sample and which is limited by the sensitivity of the current/voltage sensors of the measurement setup. Similarly, $B_{\mathrm{m,max}}/\Delta B_{\mathrm{max}}$ in Tab. 3.21 is the maximum measurable AC flux density which depends on the used sample and which is limited by the setup specifications ($V_{\mathrm{out,max}} = 150\,\mathrm{V}$, $i_{\mathrm{out,max}} = 6\,\mathrm{A}$) and by the thermal constraint that the temperature increase of the sample due to the iron losses is kept below $1\,^{\circ}\mathrm{C}$. Furthermore, $B_{\mathrm{dc,max}}$ also depends on the sample and is limited by the maximum admissible primary current which is limited by the primary conductor cross-sectional area.
The specifications of the ring core samples used for MeasSin-STx and MeasSinDC-STx are given in Tab. 3.22. The number of primary/ secondary turns is chosen as a compromise with regard to the trade-off that more turns allow for a larger measurable flux density range but increase the parasitic capacitances of the sample. The parasitic capacitance at the primary terminals is expected to deteriorate the measurement accuracy at high frequencies. Therefore, two types of samples are defined: 1) LF-samples with 100 turns for the use in MeasSin-STx and 2) HF-samples with a smaller turn number of 25 for the use in MeasSinDC-STx. Fig. 3.31 shows an example of an LF-sample and of an HF-sample.
For the loss curves resulting from MeasSin-STx and MeasSinDC-STx, it is referred to section 3.8.3. At this point it should only be noted that these loss curves have the same basic form as the loss curves resulting from MeasSin (Fig. 3.27) and MeasSinDC (Fig. 3.28), respectively.

a) b)

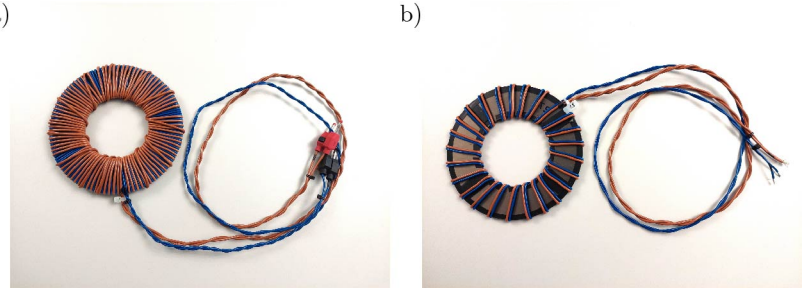


Figure 3.31: Examples of ring core samples. a) Example of an LF-sample. b) Example of an HF-sample.

3.8.3 Implemented Models including Existing and Developed Models

In this section, the implemented CLDMs are presented and compared with regard to their accuracy. This includes three existing/known CLDMs that are parametrised with the measurement results from section 3.8.2 and three modified/new CLDMs that have been developed in this project. The following list gives an overview of the implemented CLDMs:

- *iGSE-LF:* This CLDM corresponds to the known iGSE, parametrised with the iron loss density curves for low frequencies ($f \leq 1\,\mathrm{kHz}$) which result from the measurement series MeasSin.
- *iGSE-LFHF:* This CLDM corresponds to the known iGSE, parametrised with the iron loss density curves for low and high frequencies ($50\,\mathrm{Hz} \leq f \leq 100\,\mathrm{kHz}$) which result from the measurement series MeasSin.
- *LSE-LF:* This CLDM corresponds to the known LSE, parametrised with the iron loss density curves for low frequencies ($f \leq 1\,\mathrm{kHz}$) which result from the measurement series MeasSin.
- *MLSE5:* This CLDM corresponds to a modified version of the known LSE5. The LSE5 is based on a loss separation into two components (hysteresis losses and eddy current losses) with frequency- and flux density-dependent coefficients. In contrast,

the MLSE5 is based on a loss separation into the three loss components from the original LSE (hysteresis losses, classical eddy current losses, excess losses) and frequency-dependent coefficients. The CLDM is parametrised with the iron loss density curves that result from the measurement series MeasSin.

- *MLSE5+BPG:* This CLDM corresponds to a new combination of the known basic concept of the Steinmetz premagnetisation graph (SPG) and the MLSE5. This combination leads to the introduction of the *Bertotti premagnetisation graph* (BPG). The CLDM is parametrised with the iron loss density curves that result from the measurement series MeasSinDC.

- *M2LSE5+BPG:* This CLDM corresponds to a modified version of the MLSE5+BPG with an additional frequency-dependent model parameter (α). The CLDM is parametrised with the iron loss density curves that result from the measurement series Meas-STx.

How these implemented CLDMs are related to the CLDMs that were identified as the most relevant CLDMs from the literature (iGSE+SPB, RM-LSE9, and RM-LSE11) in section 3.8.1, is summarised in the following:

- *iGSE+SPG:* The models iGSE-LF and iGSE-LFHF can serve as the iGSE-part of the model iGSE+SPG. However, the complete model iGSE+SPG is not implemented because the prediction accuracy of both models, iGSE-LF and iGSE-LFHF, is lower than the prediction accuracy of the model MLSE5.

- *RM-LSE9:* As mentioned in section 3.8.1, the model RM-LSE9 is expected to be inaccurate when the amplitude of the B-field fundamental changes, due to the *average-like* DC bias modelling approach followed by the model RM-LSE9. Therefore, the model RM-LSE9 is not implemented. Instead, the model MLSE5+BPG is developed which uses a different DC bias modelling approach.

- *RM-LSE11:* As mentioned in section 3.8.1, the parametrisation of the model RM-LSE11 is based on low frequency measurements ($f < 1\,\mathrm{kHz}$) and the CLDM was not validated with any measurements including higher frequencies [130]. Hence, the model RM-LSE11 is considered less relevant than the models iGSE+SPG and RM-LSE9 and is therefore not implemented.

Table 3.23: SE parameters resulting from a curve fitting of the SE to the measured iron loss density curves (in $\mathrm{W\,kg^{-1}}$) from Fig. 3.27, including only low frequencies ($f \leq 1\,\mathrm{kHz}$).

k	0.001115
α	1.651
β	2.288

The following sections present the details of the implemented CLDMs in terms of the parametrisation based on curve fitting results, the prediction error, and the model equations (only given for the modified/new models).

Model iGSE-LF

As mentioned at the beginning of section 3.8.3, the CLDM iGSE-LF corresponds to the known iGSE, parametrised with the iron loss density curves for low frequencies ($f \leq 1\,\mathrm{kHz}$) from the measurement series MeasSin.
The parametrisation of the iGSE is based on the curve fitting of the SE in (3.142) to the measured iron loss density curves. The SE parameters resulting from this curve fitting are summarised in Tab. 3.23. Fig. 3.32 shows the comparison of the predicted iron loss density curves, using the iGSE-LF, to the measured iron loss density curves from Fig. 3.27. This comparison shows that the iGSE-LF is relatively accurate at the low frequencies for which the model was fitted but very inaccurate at high frequencies with a root-mean-square error ($RMSE$) of 43.92. Consequently, the low frequency loss density curves, as typically provided by silicon steel manufacturers, are not sufficient for an accurate iron loss prediction at high frequencies with the iGSE.

Model iGSE-LFHF

To improve the model accuracy compared to the iGSE-LF, the iGSE-LFHF is implemented. As mentioned at the beginning of section 3.8.3, this CLDM corresponds to the known iGSE, parametrised with the iron loss density curves for low and high frequencies ($50\,\mathrm{Hz} \leq f \leq 100\,\mathrm{kHz}$) from the measurement series MeasSin.
The SE parameters of the corresponding curve fitting are summarised

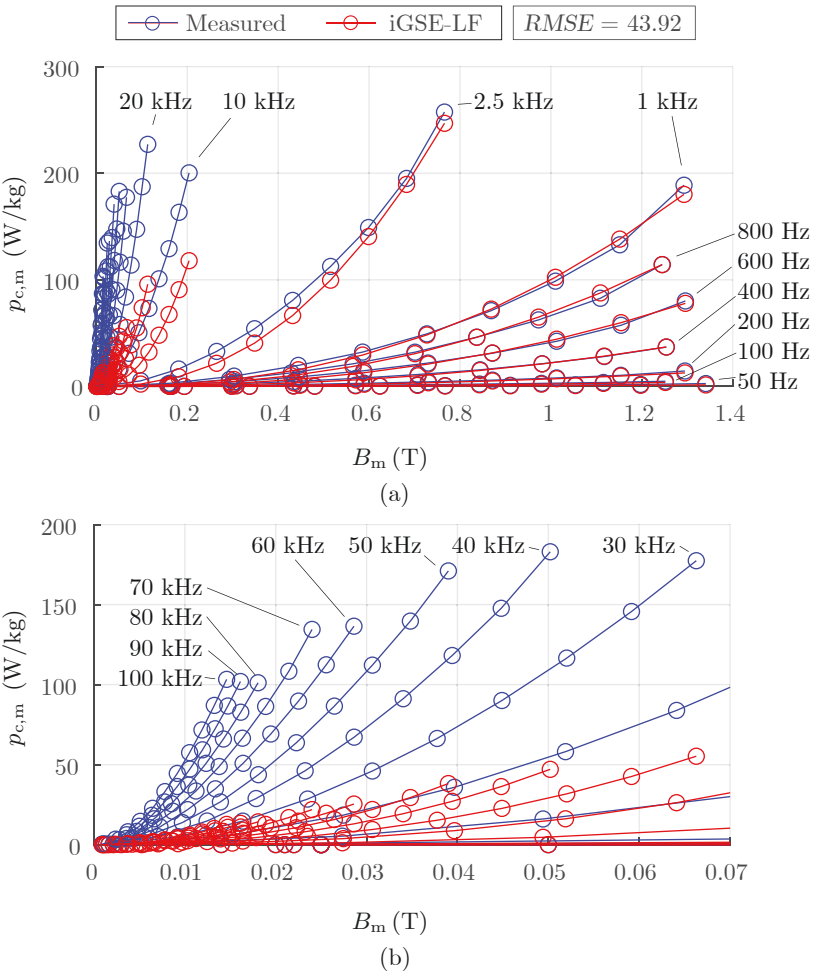


Figure 3.32: Comparison of the predicted iron loss density curves, using the iGSE-LF, to the measured iron loss density curves from Fig. 3.27. a) Results for all measured frequencies. b) Zoom on the higher frequencies.

in Tab. 3.24. Fig. 3.33 shows the comparison of the predicted iron loss density curves, using the iGSE-LFHF, to the measured iron loss density curves from Fig. 3.27. This comparison shows that the pre-

Table 3.24: SE parameters resulting from a curve fitting of the SE to the measured iron loss density curves (in $\mathrm{W\,kg^{-1}}$) from Fig. 3.27, including all measured frequencies (up to 100 kHz).

k	0.00259
α	1.518
β	1.66

Table 3.25: LSE parameters resulting from a curve fitting of the LSE to the measured iron loss density curves (in $\mathrm{W\,kg^{-1}}$) from Fig. 3.27, including only low frequencies ($f \leq 1\,\mathrm{kHz}$).

k_h	0.02879
k_cl	6.781e-5
k_ex	0

diction accuracy of the iGSE-LFHF ($RMSE = 6.51$) could be significantly improved compared to the prediction accuracy of the iGSE-LF ($RMSE = 43.92$).

Model LSE-LF

The LSE-LF is the LSE-based analogue model to the iGSE-LF. As mentioned at the beginning of section 3.8.3, the LSE-LF corresponds to the known LSE, parametrised with the iron loss density curves for low frequencies ($f \leq 1\,\mathrm{kHz}$) which result from the measurement series MeasSin.
The parametrisation of the LSE is based on the curve fitting of the LSE in (3.143) to the measured iron loss density curves. The LSE parameters resulting from this curve fitting are summarised in Tab. 3.25. Fig. 3.34 shows the comparison of the predicted iron loss density curves, using the LSE-LF, to the measured iron loss density curves from Fig. 3.27. This comparison shows that, as expected, the model prediction is relatively good at low frequencies for which the model is fitted. For higher frequencies the prediction error is relatively large with an $RMSE$ of 27.7. Therefore, low-frequency loss curves that are typically provided by silicon steel manufacturers are not sufficient to accurately predict the losses at higher frequencies with the LSE, which

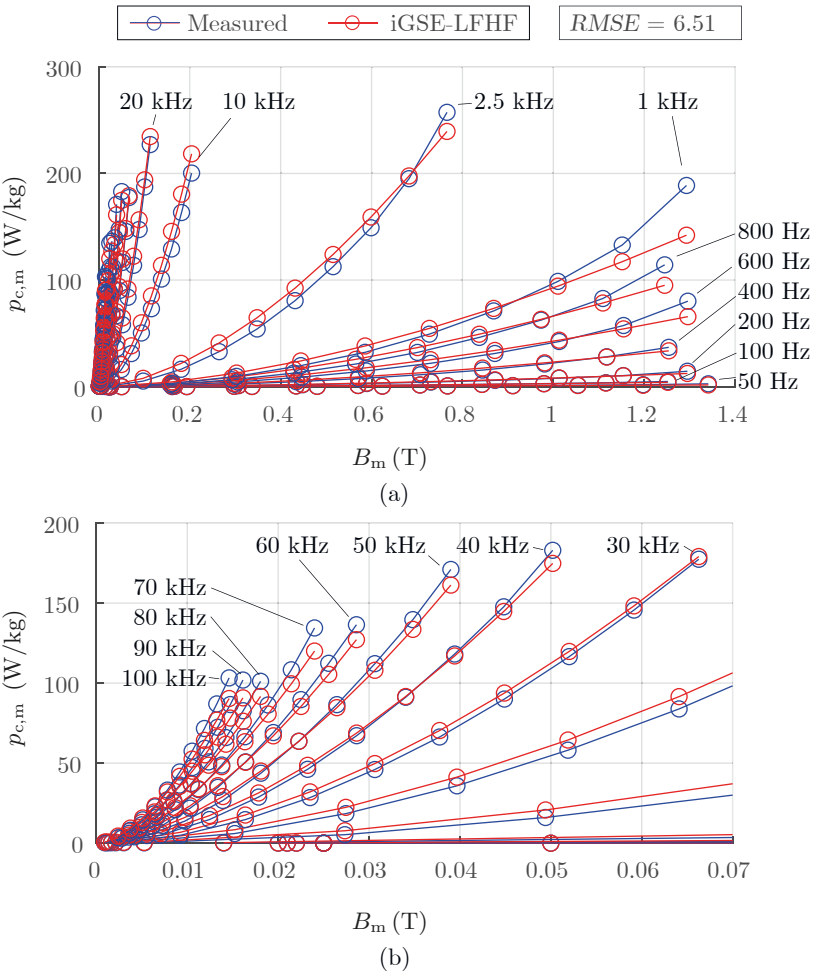


Figure 3.33: Comparison of the predicted iron loss density curves, using the iGSE-LFHF, to the measured iron loss density curves from Fig. 3.27. a) Results for all measured frequencies. b) Zoom on the higher frequencies.

was also the case with the iGSE.

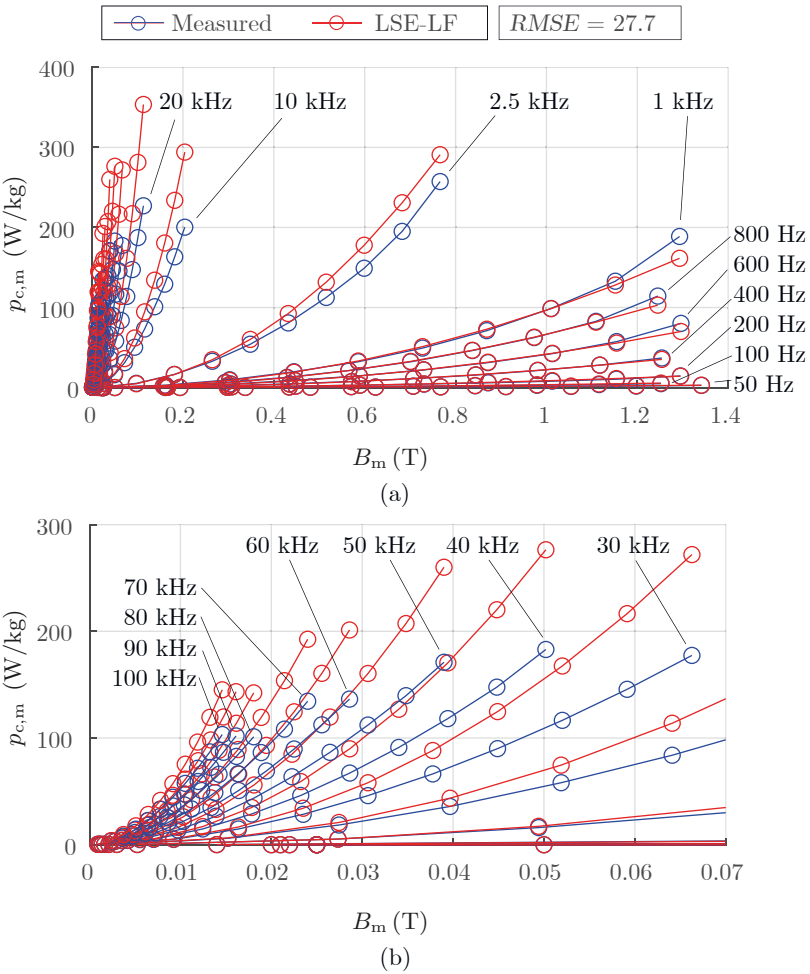


Figure 3.34: Comparison of the predicted iron loss density curves, using the LSE-LF, to the measured iron loss density curves from Fig. 3.27. a) Results for all measured frequencies. b) Zoom on the higher frequencies.

Model MLSE5

Based on the model LSE-LF described in the previous section, there are two possibilities to improve the model accuracy: 1) Include the high-

frequency measurements into the curve fitting, analogue to the iGSE-based model iGSE-LFHF. 2) Make the LSE-parameters frequency-dependent. The latter possibility is already included in the known model LSE5 which is a two-term variant of the LSE with variable loss coefficients. This approach is extended to the (three-term) LSE, resulting in the *modified LSE5* (MLSE5) with the following equation for the core/iron loss density:

$$p_{\mathrm{c,m}} = k_{\mathrm{h}}(f) B_{\mathrm{m}}^2 f + k_{\mathrm{cl}}(f) B_{\mathrm{m}}^2 f^2 + k_{\mathrm{ex}}(f) B_{\mathrm{m}}^{1.5} f^{1.5}. \tag{3.158}$$

In general, the frequency-dependent LSE-parameters $k_{\mathrm{h}}(f)$, $k_{\mathrm{cl}}(f)$, and $k_{\mathrm{ex}}(f)$ can be determined by splitting up the iron loss density curves into multiple frequency intervals, for which separate curve fittings are performed. To keep the number of model parameters low, only few frequency intervals should be defined.
In this model, two frequency intervals are defined: A low-frequency (LF) interval $[f_{\min}, f_{\mathrm{t},1}]$ and a high-frequency (HF) interval $[f_{\mathrm{t},2}, f_{\max}]$, where $f_{\min}/f_{\max}$ is the minimum/maximum frequency of the measurements, and where $f_{\mathrm{t},1}$ and $f_{\mathrm{t},2}$ are so-called transition frequencies. In the transition frequency interval $[f_{\mathrm{t},1}, f_{\mathrm{t},2}]$, the LSE-parameters are linearly interpolated to ensure a smooth transition of the LSE-parameters between the LF-interval and the HF-interval. This results in the following definition of the LSE-parameters $k_{\mathrm{h}}(f)$, $k_{\mathrm{cl}}(f)$, and $k_{\mathrm{ex}}(f)$, where these parameters are generally expressed as $k_{\mathrm{x}}(f)$:

$$k_{\mathrm{x}}(f) = \begin{cases} k_{\mathrm{x,LF}}, & f < f_{\mathrm{t},1} \\ \frac{f_{\mathrm{t},2}-f}{f_{\mathrm{t},2}-f_{\mathrm{t},1}} k_{\mathrm{x,LF}} + \frac{f-f_{\mathrm{t},1}}{f_{\mathrm{t},2}-f_{\mathrm{t},1}} k_{\mathrm{x,HF}}, & f_{\mathrm{t},1} < f < f_{\mathrm{t},2} \\ k_{\mathrm{x,HF}}, & f > f_{\mathrm{t},2}. \end{cases} \tag{3.159}$$

For the parametrisation of the model MLSE5 with the measured iron loss density curves from Fig. 3.27, the transition frequencies $f_{\mathrm{t},1}$ and $f_{\mathrm{t},2}$ are parametrised with 1 kHz and 2.5 kHz, respectively. The two sets of LSE-parameters that result from the separate curve fittings for the LF-interval and for the HF-interval are given in Tab. 3.26. Fig. 3.35 shows the comparison of the predicted iron loss density curves, using the MLSE5, to the measured iron loss density curves from Fig. 3.27. This comparison shows the best fit between the predicted and the measured iron loss density among all previously described implemented CLDMs with an $RMSE$ of 3.1. This improvement in accuracy is due to the incorporated frequency-dependency of the loss coefficients/LSE-parameters.

Table 3.26: LSE-parameters resulting from two curve fittings of the LSE to the measured iron loss density curves (in $\mathrm{W\,kg^{-1}}$) from Fig. 3.27: One for an LF-interval ($[50\,\mathrm{Hz}, 1\,\mathrm{kHz}]$) and one for an HF-interval ($[2.5\,\mathrm{kHz}, 100\,\mathrm{kHz}]$).

$k_{\mathrm{h,LF}}$	0.02879	$k_{\mathrm{h,HF}}$	0.04975
$k_{\mathrm{cl,LF}}$	6.781e-5	$k_{\mathrm{cl,HF}}$	3.111e-05
$k_{\mathrm{ex,LF}}$	0	$k_{\mathrm{ex,HF}}$	0.0006039

Model MLSE5+BPG

The previously described implemented models were fitted to the results of the measurement series with sinusoidal excitation waveforms (MeasSin), where the model MLSE5 showed the best accuracy. Therefore, this model is used as a basis for the model MLSE5+BPG that takes the DC bias into account. This is achieved by a transfer of the concept of the Steinmetz premagnetisation graph (SPG, [107]) to the LSE, which is introduced in this thesis as Bertotti premagnetisation graph (BPG). As explained in section 3.8.1, the concept of the SPG adds a DC bias- (and temperature-) dependency to the iGSE-parameters. In an analogue manner, the BPG concept adds a DC bias-dependency to the LSE-parameters. The corresponding core loss density equation of the model MLSE5+BPG is given by

$$p_{\mathrm{c,m}} = K_{\mathrm{h,dc}}(H_{\mathrm{dc}})K_{\mathrm{h,0}}(f)B_{\mathrm{m}}^2 f + K_{\mathrm{c,dc}}(H_{\mathrm{dc}})K_{\mathrm{c,0}}(f)(B_{\mathrm{m}}f)^2 + K_{\mathrm{e,dc}}(H_{\mathrm{dc}})K_{\mathrm{e,0}}(f)(B_{\mathrm{m}}f)^{1.5} \quad (3.160)$$

There, the parameters $K_{\mathrm{h/c/e,0}}(f)$ take into account the frequency dependency of the iron loss density and the parameters $K_{h/c/e,\mathrm{dc}}(H_{\mathrm{dc}})$, that define the BPG, take into account the DC bias.
Fig. 3.36a-b show the parameters $K_{\mathrm{h/c/e,0}}(f)$ and $K_{h/c/e,\mathrm{dc}}(H_{\mathrm{dc}})$ which result from curve fittings of (3.160) to the measurement results from Fig. 3.28. In accordance with the curve fitting approach used for the MLSE5, the frequency-dependent parameters $K_{\mathrm{h/c/e,0}}(f)$ shown in Fig. 3.36a are constant within the LF-interval $[50\,\mathrm{Hz}, 1\,\mathrm{kHz}]$ and within the HF-interval $[2.5\,\mathrm{kHz}, 100\,\mathrm{kHz}]$, and show a continuous transition in between.
Fig. 3.37 shows the comparison of the iron loss density curves that are

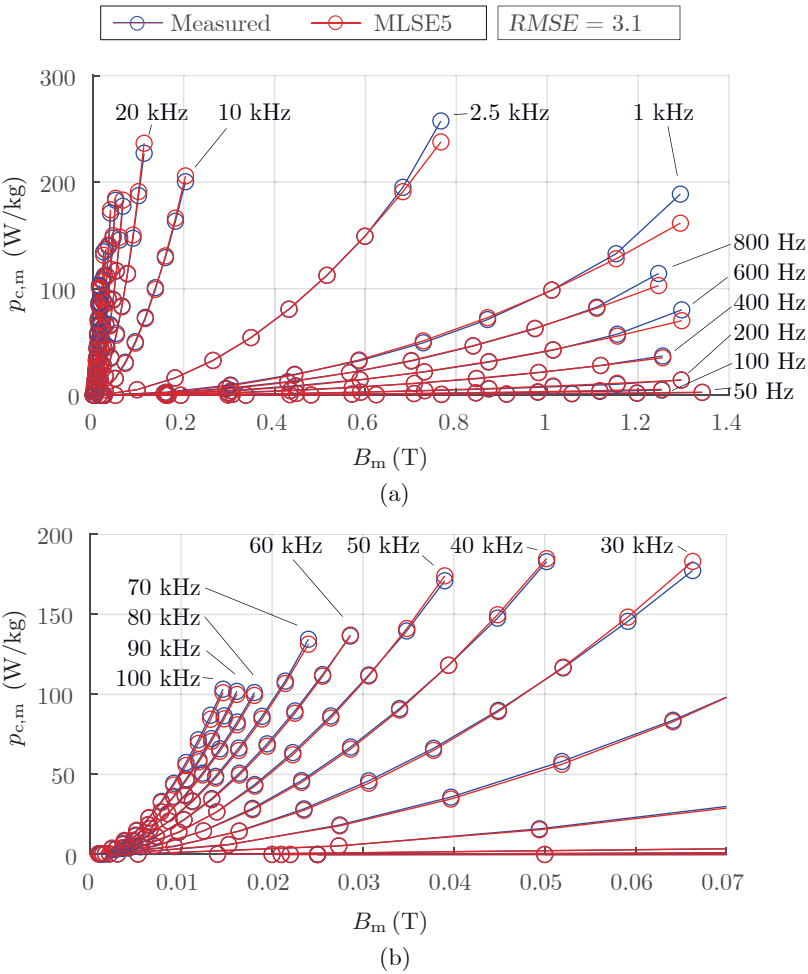


Figure 3.35: Comparison of the predicted iron loss density curves, using the MLSE5, to the measured iron loss density curves from Fig. 3.27. a) Results for all measured frequencies. b) Zoom on the higher frequencies.

predicted with the model MLSE5+BPG to the measured iron loss density curves from Fig. 3.28. This result shows a relatively good match between the model prediction and the measurement results with an

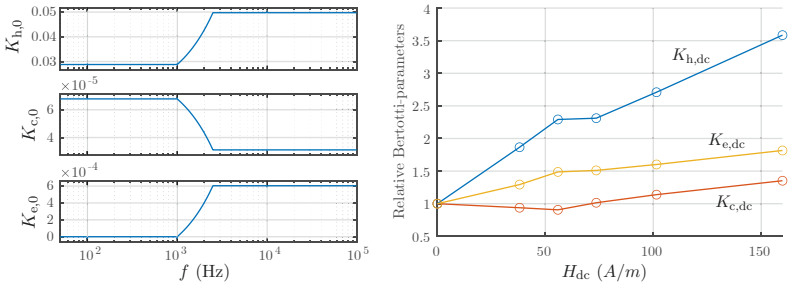


Figure 3.36: Parameters of the model MLSE5+BPG resulting from fitting the curve defined by (3.160) to the measured iron loss density curves (in $\mathrm{W\,kg^{-1}}$) from Fig. 3.28. a) Frequency dependent parameters. b) DC bias dependent parameters/Bertotti premagnetisation graph (BPG).

$RMSE$ of 1.7.

In order to apply the model MLSE5+BPG to flux density waveforms that typically occur in motors, the model is generalised by applying two modifications:
1) To take harmonics into account which are typically present in the magnetic flux density in inverter-driven motors, the iron loss density is calculated for each harmonic and the total iron loss density is calculated by the summation of the loss densities at each harmonic. It is noted that such a superposition-based approach is expected to overestimate the hysteresis losses because only some harmonics cause a minor hysteresis loop and hence hysteresis losses. However, detecting minor hysteresis loops, e.g. based on the approach desribed in section II.B of [119], increases the computation time. In order to use the iron loss density model in optimisations, which implies to execute the model many times, this is avoided in the suggested approach at the cost of overestimating the hysteresis losses.
2) A second modification is linked to the DC bias. In electric motors the "DC bias" is given by the fundamental wave excitation ($H_1(t)$) and hence (slowly) varies over time. This is taken into account by calculating so-called effective DC bias weighting factors $\bar{K}_{h/c/e,\mathrm{dc}}$ from an averaging of the DC bias weighting factors at the actual DC excitation $K_{h/cl/e,\mathrm{dc}}(H_{\mathrm{dc}} = H_1(t))$. To limit the error introduced by this

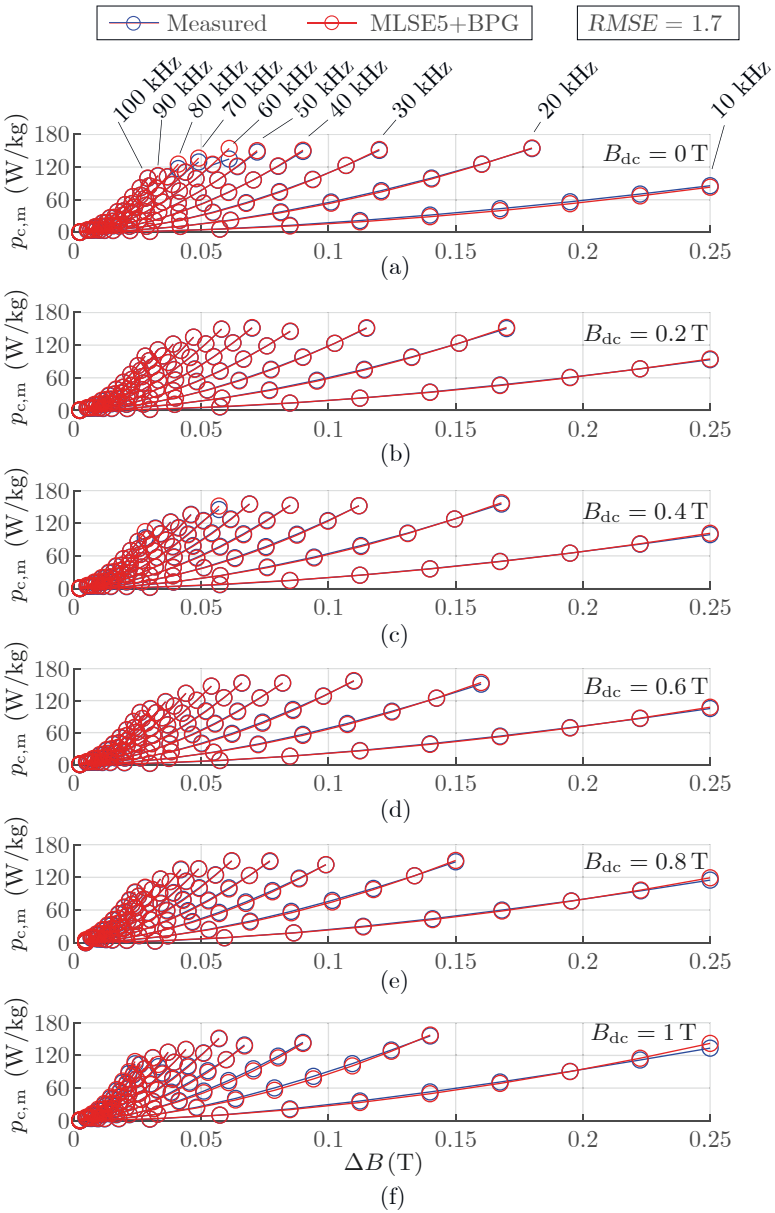


Figure 3.37: Comparison of the predicted iron loss density curves, using the model MLSE5+BPG, to the measured iron loss density curves from Fig. 3.28.

modification, only harmonics with frequencies f that are significantly larger than the fundamental frequency f_1 are considered to be DC-biased ($f > 10f_1$). These two modifications lead to the following iron loss density model for arbitrary flux density waveforms, which is called GMLSE5+BPG:

$$p_\mathrm{m} = \sum_f p_\mathrm{m}(f) \tag{3.161}$$

$$p_\mathrm{m}(f) = \bar{K}_\mathrm{h,dc} K_\mathrm{h,0}(f) B_\mathrm{m}^2 f + \bar{K}_\mathrm{c,dc} K_\mathrm{c,0}(f) (B_\mathrm{m} f)^2 \tag{3.162}$$

$$+ \bar{K}_\mathrm{e,dc} K_\mathrm{e,0}(f) (B_\mathrm{m} f)^{1.5} \tag{3.163}$$

$$\bar{K}_{h/c/e,\mathrm{dc}} = \begin{cases} \frac{1}{N} \sum_{k=1}^{N} K_{h/c/e,\mathrm{dc}}(H_\mathrm{dc}(t_k)), f > 10f_1 \\ 1, f < 10f_1. \end{cases} \tag{3.164}$$

Model M2LSE5+BPG

So far, the implemented models were parametrised with results of the measurement series MeasSin and MeasSinDC which were made using one silicon steel sheet type, namely sheet type 1 (Tab. 3.19). An analysis of the results of the measurement series Meas-STx, which covers multiple sheet types (sheet types 2-10, cf. Tab. 3.19), has shown that a similar model accuracy as the model accuracy of the MLSE5+BPG in terms of the $RMSE$ can be achieved if two modifications are made to the MLSE5+BPG: 1) The constant exponent 2 of B_m in the hysteresis loss component in (3.160) is replaced by a frequency-dependent loss coefficient $K_{\alpha,0}(f)$. 2) The frequency-dependent loss coefficients are defined to be constant over a general number of N_IC frequency intervals, where N_IC can be larger than 2. These modifications lead to a model which is called M2LSE5+BPG and in which the iron loss density is given by

$$p_\mathrm{c,m} = K_\mathrm{h,dc}(H_\mathrm{dc}) K_\mathrm{h,0}(f) B_\mathrm{m}^{K_{\alpha,0}(f)} f + K_\mathrm{c,dc}(H_\mathrm{dc}) K_\mathrm{c,0}(f) (B_\mathrm{m} f)^2 + K_\mathrm{e,dc}(H_\mathrm{dc}) K_\mathrm{e,0}(f) (B_\mathrm{m} f)^{1.5}. \tag{3.165}$$

This formula is the same as (3.160) except for the coefficient $K_{\alpha,0}(f)$. The frequency-dependent loss coefficients of (3.165) are given by $K_\mathrm{h,0}(f)$, $K_\mathrm{c,0}(f)$, $K_\mathrm{e,0}(f)$, and $K_{\alpha,0}(f)$. These coefficients are generally ex-

pressed as $K_{x,0}(f)$ and defined as follows:

$$K_{x,0}(f) = K_{x,0,\mathrm{IC}_1} + \sum_{i=1}^{N_\mathrm{IC}-1} m_{x,i} \cdot k_{\mathrm{aux},i}(f) \tag{3.166}$$

$$m_{x,i} = \frac{K_{x,0,\mathrm{IC}_{i+1}} - K_{x,0,\mathrm{IC}_i}}{f_{\mathrm{IC}_{i+1},\mathrm{LB}} - f_{\mathrm{IC}_i,\mathrm{UB}}} \tag{3.167}$$

$$k_{\mathrm{aux},i}(f) = \frac{f - f_{\mathrm{IC}_i,\mathrm{UB}}}{1 + e^{a\cdot(f - f_{\mathrm{IC}_i,\mathrm{UB}})}} - \frac{f - f_{\mathrm{IC}_{i+1},\mathrm{LB}}}{1 + e^{a\cdot(f - f_{\mathrm{IC}_{i+1},\mathrm{LB}})}} \tag{3.168}$$

These equations result in a function for $K_{x,0}(f)$ which consists of an alternating sequence of two types of frequency intervals: 1) Frequency intervals $[f_{\mathrm{IC}_j,\mathrm{LB}}, f_{\mathrm{IC}_j,\mathrm{UB}}]$ for $j = 1, 2, \ldots, N_\mathrm{IC}$ in which $K_{x,0}(f)$ is approximately constant and equal to $K_{x,0,\mathrm{IC}_j}$. These intervals are also referred to as ICs. 2) Frequency intervals $[f_{\mathrm{IC}_i,\mathrm{UB}}, f_{\mathrm{IC}_{i+1},\mathrm{LB}}]$ for $i = 1, 2, \ldots, N_\mathrm{IC} - 1$ in which $K_{x,0}(f)$ has a smooth transition between the values of the adjacent ICs. These intervals are also referred to as ITs. N_IC is the number of ICs and $(N_\mathrm{IC} - 1)$ is the number of ITs. $m_{x,i}$ in (3.167) is a parameter that sets the slope of $K_{x,0}(f)$ in the i-th IT. $k_{\mathrm{aux},i}(f)$ in (3.168) is an auxiliary function which is approximately equal to 0 at $f = 0\,\mathrm{Hz}$ and which has a slope that is close to 1 within the i-th IT and close to 0 outside of it. The smoothness of $K_{x,0}(f)$ in the ITs can be adjusted with the parameter a in (3.168), where a useful default value is given by $a = -1$.

The DC bias-dependent loss coefficients in (3.165), i.e. $K_{\mathrm{h,dc}}(H_\mathrm{dc})$, $K_{\mathrm{c,dc}}(H_\mathrm{dc})$, and $K_{\mathrm{e,dc}}(H_\mathrm{dc})$ are evaluated by means of linear interpolation of the corresponding measured curves of the BPG. An analytical expression for these coefficients as for the frequency-dependent coefficients is not developed because the resulting number of model parameters would not result in a significant reduction of model parameters compared to the number of measured points.

The M2LSE5+BPG was parametrised based on a parameter fitting to the measurement results of Meas-STx, including MeasSin-STx and MeasSinDC-STx, for each of the considered sheet types $x = 2, 3, \ldots, 10$. For this model parametrisation, $N_\mathrm{IC} = 3$ was chosen as this choice resulted in a model prediction $RMSE$ that is similar to the $RMSE$ achieved with the MLSE5+BPG. The model parameters resulting from the parametrisation, for example for sheet type 2, are given in Tab. 3.27, Fig. 3.38, and Fig. 3.39.

Fig. 3.40 and Fig. 3.41 show the comparison of the predicted iron loss

Table 3.27: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST2.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	4.4123e-2	1.4321e-4	2.2337e-14	3
IC_2	1500	9000	1.1119e-1	5.2392e-5	1.1029e-3	2.4161
IC_3	10000	100000	3.1505e-1	4.2652e-5	1.3105e-9	1.7803

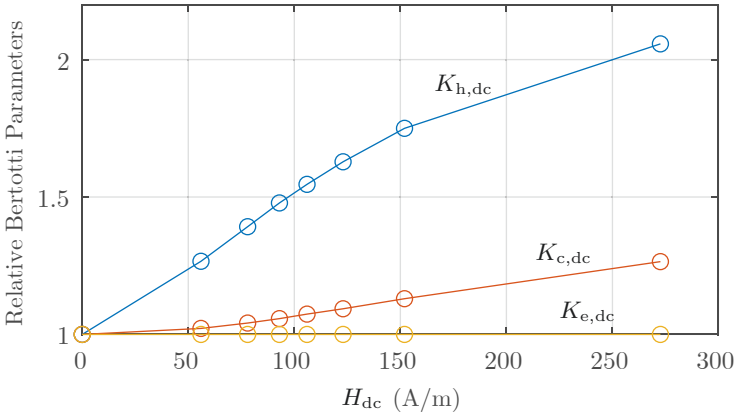


Figure 3.38: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST2.

density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST2 and MeasSinDC-ST2, respectively. These figures show a good match between the model-predicted curves and the measurements with an $RMSE$ of 1.68 and 1.21, respectively.

For the other sheet types used in Meas-STx, i.e. sheet types 3-10 (Tab. 3.18), analogue results for the model parameters and for the comparison of model-predicted and measured iron loss density curves are given in chapter B of the appendix. To summarise these results, Tab. 3.28 shows an overview of the model prediction error in terms of the $RMSE$ for all sheet types used in Meas-STx. Overall, Tab. 3.28 shows that the suggested iron loss density model M2LSE5+BPG achieves a similarly

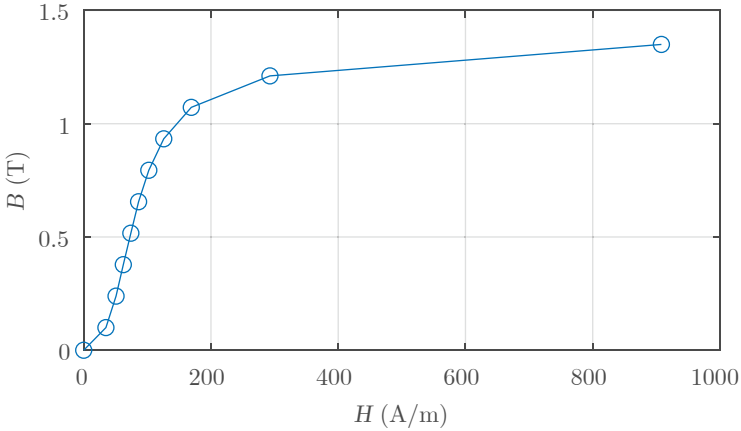


Figure 3.39: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST2.

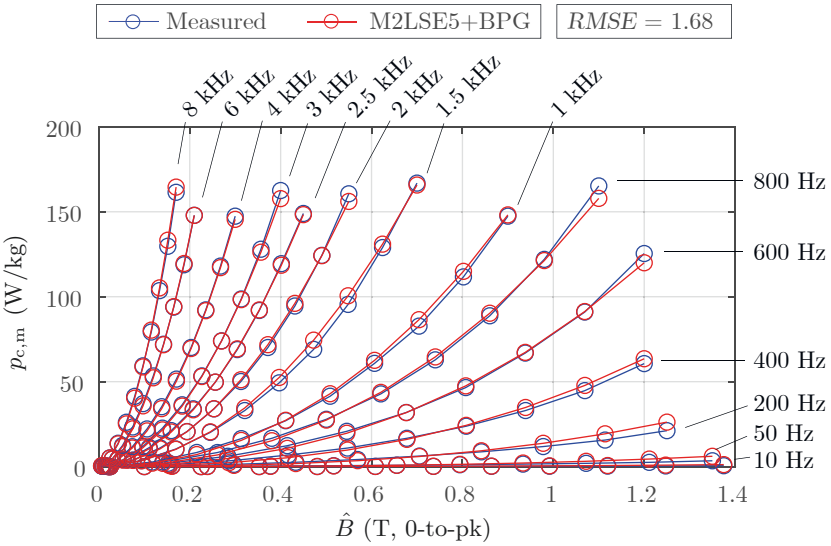


Figure 3.40: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST2.

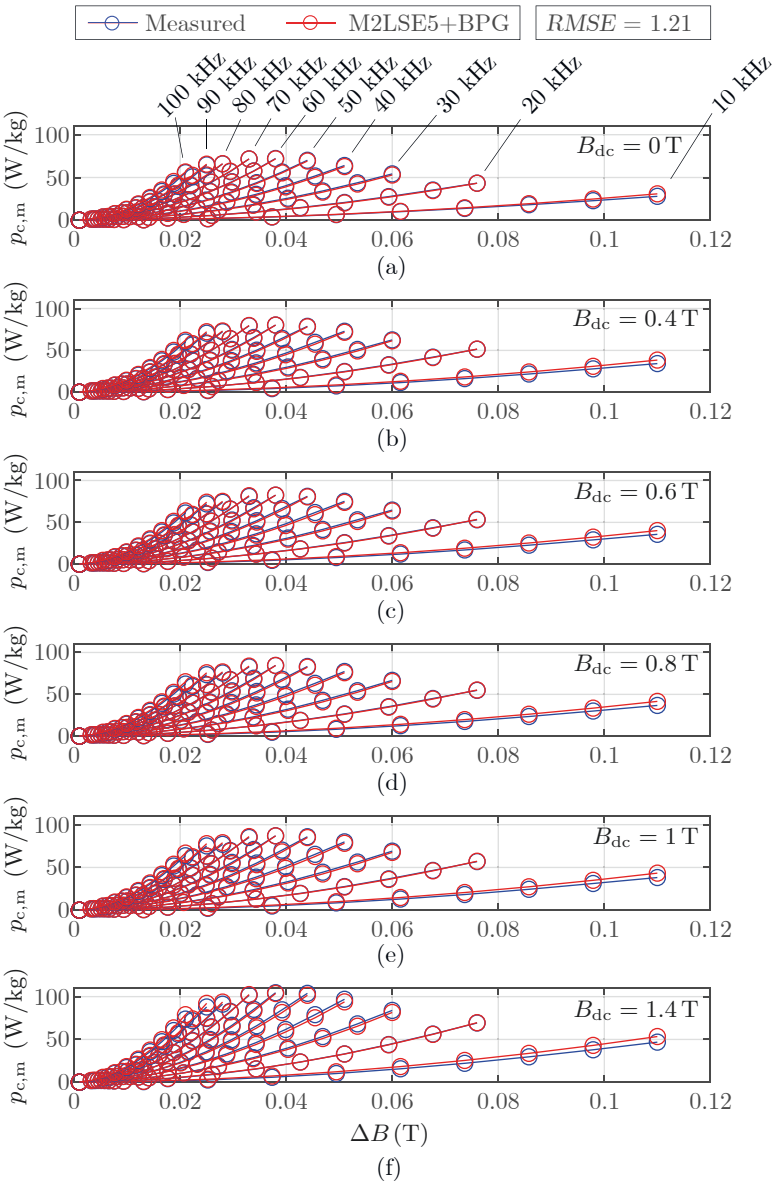


Figure 3.41: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST2.

Table 3.28: Prediction error between the iron loss density model M2LSE5+BPG and the measurement results of the measurement series MeasSin-STx and MeasSinDC-STx for all considered sheet types $x = 2, 3, \ldots, 10$. All $RMSE$ values are given in $\mathrm{W\,kg^{-1}}$.

x	Grade	$RMSE$ (MeasSin-STx)	$RMSE$ (MeasSinDC-STx)	$RMSE$ (Overall)
2	M470-50A	1.68	1.21	1.29
3	M330-35A	1.31	0.50	0.69
4	M235-35A	1.24	0.27	0.54
5	M270-50A	1.71	0.61	0.86
6	M400-50AP	1.77	0.40	0.75
7	M530-50A	2.04	0.88	1.13
8	M800-50A	1.81	0.93	1.10
9	NO10	0.88	0.20	0.40
10	NO20-15	0.72	0.23	0.35

good model accuracy for all investigated sheet types.

The same generalisation that was made from the MLSE5+BPG to the GMLSE5+BPG, which was explained previously in section 3.8.3, can be applied to the M2LSE5+BPG, resulting in a model that is analogously called GM2LSE5+BPG. This generalised model can be applied to arbitrary flux density waveforms. The model equations of the GM2LSE5+BPG are the same as the model equations of the GMLSE5+BPG which are given in (3.161)-(3.164), except for the term B_{m}^2 in (3.162) which needs to be replaced by $B_{\mathrm{m}}^{K_{\alpha,0}(f)}$.

3.9 Thermal Model of an Integrated Motor Drive

In this section, a thermal IMD model is presented which can be used in IMD design procedures such as the IMD design procedure presented later in section 4.2.
This section is divided into the following parts: First, in section 3.9.1, a temperature calculation procedure is described which is an iterative procedure to calculate the temperature distribution in an IMD and which represents the outer framework of the thermal IMD model. This temperature calculation procedure has a relatively large number of input parameters which are separately defined in section 3.9.2. Finally, in section 3.9.3, a lumped parameter thermal network (LPTN) for IMDs is described which constitutes the main element of the thermal IMD model.

3.9.1 Temperature Calculation Procedure

The developed temperature calculation procedure is shown in Fig. 3.42 and consists of the following steps: In step S1, the input parameters of the temperature calculation procedure are parametrised which primarily define the considered IMD design. As the number of input parameters is relatively large, Fig. 3.42 only shows a list of input parameter groups which will be defined separately in section 3.9.2. In step S2, the thermal conductance matrix is calculated which is required to solve the LPTN using nodal analysis. Calculating the conductance matrix includes the calculation of the thermal resistances of the LPTN. In step S3 of the procedure, the LPTN is solved through nodal analysis resulting in the temperatures at the LPTN nodes which are referred to as node temperatures in the following. As the LPTN includes temperature dependent thermal resistances (convection/radiation) and temperature dependent losses (motor copper losses & inverter conduction losses), solving the LPTN is an iterative process which is given by the steps S3-S5. Therein, in step S4, the node temperature variation between the last two LPTN solutions, called ΔT_i, is compared against a temperature convergence limit $\Delta T_{\max}$. The temperature dependent losses and thermal resistances are updated (step S5) and the LPTN is solved again (step S3) until all node temperatures fulfil the convergence criterion ($\Delta T_i < \Delta T_{\max}$) or until a maximum number of iterations is reached.

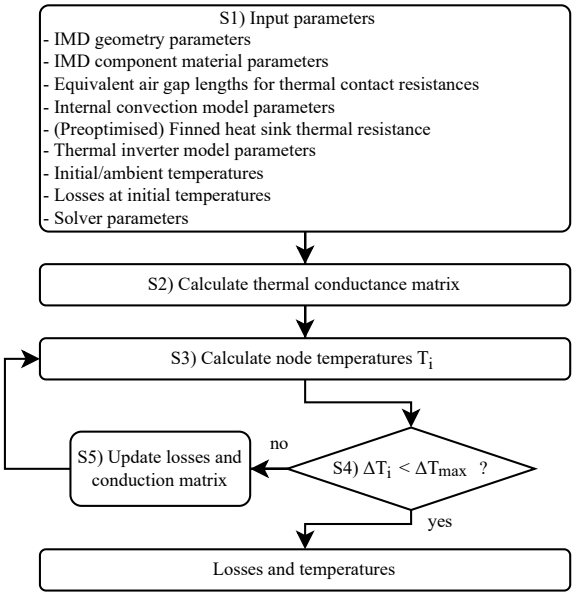


Figure 3.42: Temperature calculation procedure of the thermal IMD model.

Finally, when the convergence criterion is fulfilled, the temperature calculation procedure results in the LPTN node temperatures and in the updated losses.

3.9.2 Input Parameters of the Temperature Calculation Procedure

In this section, the parameters of the input parameter groups that are parametrised in step S1 of the temperature calculation procedure from Fig. 3.42 are defined. This section is divided into two parts: In a first part on the underlying mechanical IMD model, the *IMD geometry parameters* from Fig. 3.42 are defined. In a second part, the other parameter groups from Fig. 3.42 (*IMD component material parameters*, *Equivalent air gap lengths*, etc.) are defined.

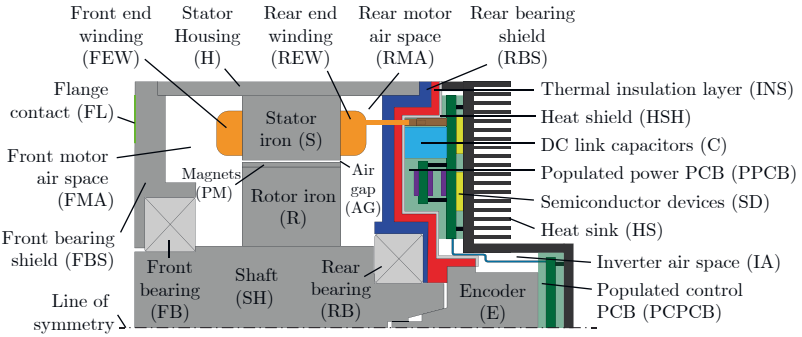


Figure 3.43: IMD integration concept used for the thermal IMD model, including the definition of IMD parts/components.

Underlying Mechanical IMD Model

In this section, the mechanical IMD model is presented which is the basis for the thermal IMD model. This mechanical IMD model defines the IMD geometry parameters that are set in step S1 of the temperature calculation procedure from Fig. 3.42. The mechanical IMD model is based on the thermo-mechanical integration/insulation concepts selected in chapter 2 which are the thermo-mechanical integration concept C1 (Fig. 2.8) and the thermal insulation concept I2 (Fig. 2.11). The resulting integration concept which combines these partial concepts is shown in Fig. 3.43.

For this IMD integration concept, the mechanical IMD model defines a set of independent geometry parameters, which defines the modelled IMD geometry, including any dependent geometry parameters that are used in the thermal model. Fig. 3.44 shows the defined independent and dependent geometry parameters of the axial-cross section of the mechanical IMD model.

The complete set of independent IMD geometry parameters, including parameters outside of the axial cross-section, is given in Tab. 3.29 - Tab. 3.31. Within these tables, the IMD geometry parameters are structured by the IMD parts defined in Fig. 3.43 (Stator iron, rotor iron, etc.).

The purpose of the cavity in the rear bearing shield (RBS, Fig. 3.43), whose axial length is defined by $l_{\mathrm{RBS,cav}}$ in Fig. 3.44, is to reduce the

overall IMD system volume for the case that an inverter is designed for a given motor including a given stator housing, i.e. for the motor stages MS1 & MS2 defined in section 2.4.2. However, incorporating such a cavity in the IMD modelling and design would significantly increase the modelling/design complexity because the power PCB surface area that is available for PCB components to fit into such a cavity would depend on multiple design parameters (the thickness of the RBS d_{RBS}, the thickness of the thermal insulation layer l_{ins}, and the thickness of the heat shield d_{HSH} in Fig. 3.44). Therefore, to limit the complexity of the modelling and design, no such cavity is considered in the following which corresponds to the assumption of $l_{\mathrm{RBS,cav}} = 0$ in Fig. 3.44. For the case of a combined motor-converter design, i.e. for motor stage MS3 defined in section 2.4.2, a cavity in the RBS should anyways be omitted because the same IMD system volume that would be achieved with such a cavity can be achieved without such a cavity and with less material effort by designing the stator housing (H) with an axially shorter rear section, i.e. by reducing $l_{\mathrm{H,r}}$ in Fig. 3.44.

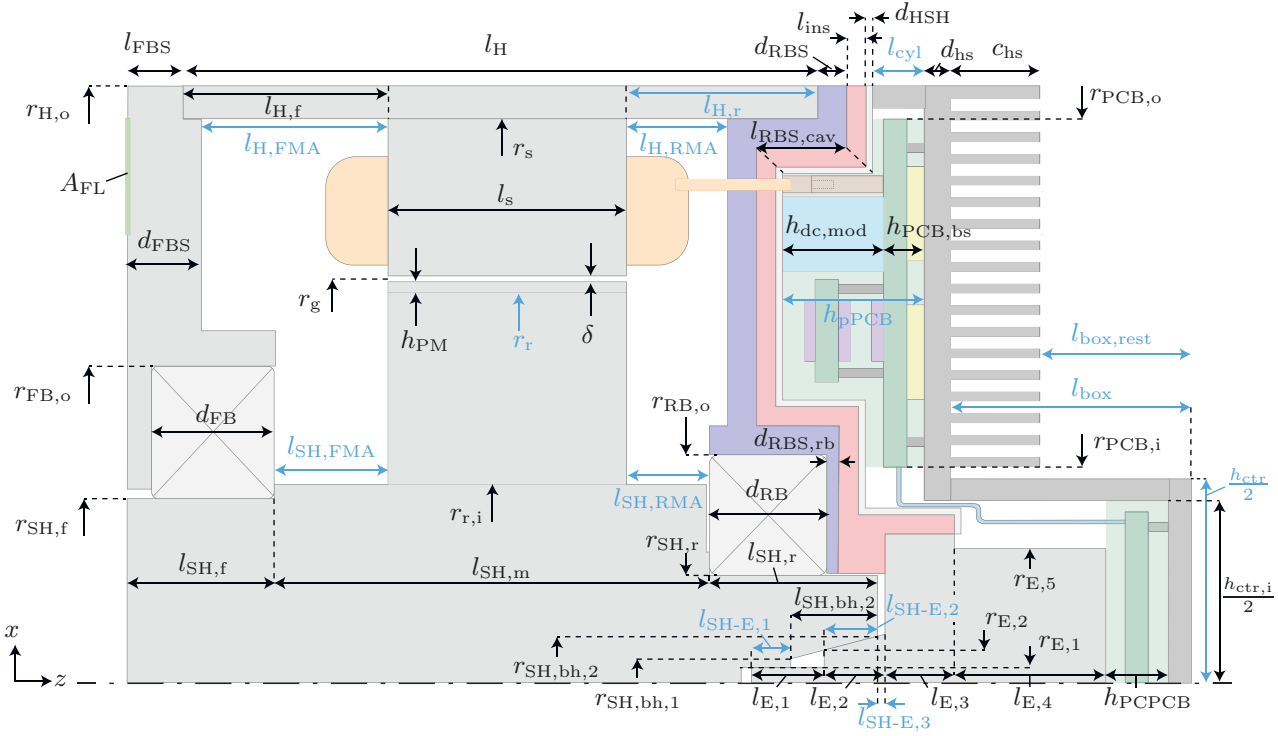


Figure 3.44: Independent (black) and dependent (blue) geometry parameters of the axial cross-section of the mechanical IMD model.

Table 3.29: Independent IMD geometry parameters of the mechanical IMD model including the IMD geometry input parameters of the temperature calculation procedure shown in Fig. 3.42. Continued in Tab. 3.30 - Tab. 3.31.

Variable	Parameter definition	Unit
Stator iron (S), rotor iron (R), and permanent magnets (PM)		
N	Number of stator slots	-
l_s	Stator length (axial)	m
r_s	Stator outer radius	m
h_y	Stator yoke height	m
w_t	Stator tooth width	m
h_tt1	Stator tooth tip height 1	m
h_tt2	Stator tooth tip height 2	m
α	Stator tooth tip angle	rad
$r_\mathrm{r,i}$	Rotor inner radius	m
r_g	Radius to the air gap middle	m
δ	Air gap length (radial)	m
k_stack	Stator/rotor iron stacking factor	-
h_PM	PM height (radial)	m
Core/Front end/Rear end winding (CW/FEW/REW)		
n_t	Number of turns per tooth-coil	-
d_c	Conductor diameter	m
w_sl	Slot liner thickness	m
d_wa	Winding area to slot middle distance	m
Stator Housing (H)		
$r_\mathrm{H,o}$	Housing outer radius	m
l_H	Housing length (axial)	m
$l_\mathrm{H,f}$	Housing front to stator front distance (axial)	m
Front/Rear bearing (FB/RB)		
$r_\mathrm{FB,o}$	Front bearing outer radius	m
$r_\mathrm{RB,o}$	Rear bearing outer radius	m
d_FB	Front bearing length (axial)	m
d_RB	Rear bearing length (axial)	m

Table 3.30: Continuation of Tab. 3.29.

Variable	Parameter definition	Unit
	Shaft (SH)	
$l_{\mathrm{SH,f}}$	Front shaft section length (axial)	m
$l_{\mathrm{SH,m}}$	Middle shaft section length (axial)	m
$l_{\mathrm{SH,r}}$	Rear shaft section length (axial)	m
$r_{\mathrm{SH,f}}$	Front shaft section radius	m
$r_{\mathrm{SH,r}}$	Rear shaft section radius	m
$r_{\mathrm{SH,bh,1}}$	Conical shaft bore hole front radius	m
$r_{\mathrm{SH,bh,2}}$	Conical shaft bore hole rear radius	m
$l_{\mathrm{SH,bh,2}}$	Conical shaft bore hole length (axial)	m
	Encoder (E)	
$r_{\mathrm{E,1}}$	Encoder shaft screw radius	m
$r_{\mathrm{E,2}}$	Encoder shaft cone front radius	m
$r_{\mathrm{E,5}}$	Encoder rear radius	m
$l_{\mathrm{E,1}}$	Encoder shaft screw length (axial)	m
$l_{\mathrm{E,2}}$	Encoder shaft cone length (axial)	m
$l_{\mathrm{E,3}}$	Encoder section length of max. radius (axial)	m
$l_{\mathrm{E,4}}$	Encoder rear section length (axial)	m
	Front/rear bearing shield (FBS/RBS)	
d_{FBS}	FBS thickness (axial)	m
l_{FBS}	FBS length to the housing front (axial)	m
A_{FL}	Flange contact area	m^2
d_{RBS}	RBS thickness (axial)	m
$d_{\mathrm{RBS,rb}}$	RBS thickness on the RB rear side	m
$l_{\mathrm{RBS,cav}}$	RBS cavity length (axial)	m
	Thermal insulation layer (INS) and heat shield (HSH)	
l_{ins}	Thermal insulation layer thickness (axial)	m
r_{SCR}	Heat sink to housing screw radius	m
d_{BL}	Thermally insulating screw blind thickness	m
N_{SCR}	Number of screws (heat sink to housing)	-
d_{HSH}	Heat shield thickness (axial)	m

Table 3.31: Continuation of Tab. 3.30.

Variable	Parameter definition	Unit
	Populated power PCB (PPCB)	
$h_{\mathrm{PCB,bs}}$	PPCB bottom side length (axial, incl. d_{PCB})	m
$h_{\mathrm{pPCB,min}}$	PPCB height lower bound (axial)	m
$h_{\mathrm{dc,mod}}$	DC link module height (axial)	m
$r_{\mathrm{PCB,o}}$	PCB outer radius	m
$r_{\mathrm{PCB,i}}$	PCB inner radius	m
d_{PCB}	PCB thickness (axial)	m
d_{via}	Thermal via outer diameter	m
$d_{\mathrm{Cu,via}}$	Thermal via copper wall thickness	m
p_{via}	Thermal via pitch	m
d_{TIM}	Gap pad thickness (PPCB-to-HS/C_{dc}-to-HSH)	m
$N_{\mathrm{cl,PCB}}$	Number of PCB copper layers	-
$d_{\mathrm{cl,PCB}}$	PCB copper layer thickness	m
A_{cap}	Total footprint area of the DC link capacitors	m^2
	Populated control PCB (PCPCB)	
h_{PCPCB}	PCPCB height (axial)	m
$h_{\mathrm{ctr,i}}$	Inner heat sink encoder housing height	m
	Inverter heat sink/end cap (HS)	
d_{hs}	Heat sink plate/cap thickness	m
c_{hs}	Heat sink fin length (axial)	m

Further Input Parameters of the Temperature Calculation Procedure

With the previous section, the parameters of the input parameter group *IMD geometry parameters* of the temperature calculation procedure (Fig. 3.42) are defined. In this section, the parameters of the other input parameter groups of this procedure (*IMD component material parameters*, *Equivalent air gap lengths*, etc.) are defined.
This parameter definition is given in Tab. 3.32 - Tab. 3.38 for all other input parameter groups except for the *(Preoptimised) Finned heat sink thermal resistance*. How the parameters from Tab. 3.32 - Tab. 3.38 are used is explained in section 3.9.3 on the IMD LPTN.
The *Preoptimised Finned heat sink thermal resistance* (Fig. 3.42) must

be provided as a function $R_{\mathrm{HS_b\text{-}amb}}(c_{\mathrm{hs}}, l_{\mathrm{cyl}}, l_{\mathrm{box}})$, where c_{hs}, l_{cyl}, and l_{box} are heat sink dimensions (axial fin length, cylinder length, and encoder box length) which are also shown in Fig. 3.44. This function can for example be determined through a preoptimisation of the heat sink fin spacing and of the fin thickness based on the heat sink model that is presented separately in section 3.10.

Table 3.32: IMD component material parameters that are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42.

Variable	Parameter definition	Unit
	Thermal conductivities	
k_{H}	Housing thermal conductivity	
$k_{\mathrm{S,she}}/k_{\mathrm{R,she}}$	Stator/Rotor sheet thermal conductivity	
$k_{\mathrm{R,ins}}$	Rotor sheet insulation thermal conductivity	
$k_{\mathrm{W,ins}}$	Winding insulation thermal conductivity	
$k_{\mathrm{W,c}}$	Winding conductor thermal conductivity	
$k_{\mathrm{W,sl}}$	Winding slot liner thermal conductivity	
$k_{\mathrm{FBS}}/k_{\mathrm{RBS}}$	Font/Rear bearing shield thermal conductivity	
k_{SH}	Shaft thermal conductivity	
k_{HS}	Heat sink thermal conductivity	
k_{HSH}	Heat shield thermal conductivity	
k_{eag}	Equivalent air gap thermal conductivity	$\mathrm{W\,m^{-1}\,K^{-1}}$
k_{PM}	Permanent magnet thermal conductivity	
k_{via}	Thermal via thermal conductivity	
$k_{\mathrm{TIM,eff}}$	Effective gap pad thermal conductivity (Effective: Including thermal contact resistances)	
$k_{\mathrm{PCB,c}}$	PCB copper layer thermal conductivity	
$k_{\mathrm{PCB,s}}$	PCB substrate thermal conductivity	
k_{SCR}	Screw (heat sink to housing) thermal conductivity	
k_{INS}	Insulation layer thermal conductivity	
$k_{\mathrm{E,sh}}$	Encoder shaft thermal conductivity	
	Emissivities and temperature coefficients	
ϵ_{H}	Housing surface emissivity	
ϵ_{EW}	Front/rear end winding surface emissivity	
$\epsilon_{\mathrm{FBS}}/\epsilon_{\mathrm{RBS}}$	Front/Rear bearing shield surface emissivity	-
ϵ_{HS}	Heat sink surface emissivity	
$\alpha_{\rho,\mathrm{Wc}}$	Winding resistivity temperature coefficient	
	Air gap properties	
μ_{AG}	Dynamic viscosity of the air in the air gap	$\mathrm{Pa\,s}$
k_{AG}	Thermal conductivity of the air in the air gap	$\mathrm{W\,m^{-1}\,K^{-1}}$
	Ambient air properties	
β_{amb}	Coefficient of cubical expansion of the ambient air	$\mathrm{K^{-1}}$
ρ_{amb}	Density of the ambient air	$\mathrm{kg\,m^{-3}}$
μ_{amb}	Dynamic viscosity of the ambient air	$\mathrm{Pa\,s}$
$c_{\mathrm{p,amb}}$	Specific heat of the ambient air	$\mathrm{J\,kg^{-1}\,K^{-1}}$
k_{amb}	Thermal conductivity of the ambient air	$\mathrm{W\,m^{-1}\,K^{-1}}$

Table 3.33: Equivalent air gap lengths (l_{eq}) for thermal contact resistances which are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42.

Variable	Parameter definition	Unit
$l_{\mathrm{eq,H-S}}$	l_{eq} between the housing and the stator	
$l_{\mathrm{eq,H-FBS}}$	l_{eq} between the housing and the front bearing shield	
$l_{\mathrm{eq,H-RBS}}$	l_{eq} between the housing and the rear bearing shield	
$l_{\mathrm{eq,R-PM}}$	l_{eq} between the rotor iron and the permanent magnets	
$l_{\mathrm{eq,R-SH}}$	l_{eq} between the rotor iron and the shaft	
$l_{\mathrm{eq,FBS-FB}}$	l_{eq} between the front bearing shield and the front bearing	m
$l_{\mathrm{eq,RBS-RB}}$	l_{eq} between the rear bearing shield and the rear bearing	
$l_{\mathrm{eq,SH-FB}}$	l_{eq} between the shaft and the front bearing	
$l_{\mathrm{eq,SH-RB}}$	l_{eq} between the shaft and the rear bearing	
$l_{\mathrm{eq,SH-E}}$	l_{eq} between the shaft and the encoder	
$l_{\mathrm{eq,HSH-HS}}$	l_{eq} between the heat shield and the (inverter) heat sink	
$l_{\mathrm{eq,FL}}$	l_{eq} for the flange contact (motor to external machinery)	
$l_{\mathrm{eq,B}}$	l_{eq} for the front/rear ball bearing contacts	

Table 3.34: Internal convection model parameters that are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42. vel_{AG} is the air velocity in the air gap at the outer surface of the PMs, and $\mathrm{H_{fri}}$, $\mathrm{H_{rri}}$, etc. are nodes of the LPTN given in Fig. 3.45.

Variable	Parameter definition	Unit
$k_{\mathrm{icvm,1}}$	Internal convection model curve fit coefficient 1	$\mathrm{W\,m^{-2}\,K^{-1}}$
$k_{\mathrm{icvm,2}}$	Internal convection model curve fit coefficient 2	-
$k_{\mathrm{icvm,3}}$	Internal convection model curve fit coefficient 3	-
$k_{\mathrm{vel,H_{fri}}}$	Ratio of the air velocity at the node $\mathrm{H_{fri}}$ to vel_{AG}	-
$k_{\mathrm{vel,H_{rri}}}$	Ratio of the air velocity at the node $\mathrm{H_{rri}}$ to vel_{AG}	-
$k_{\mathrm{vel,FEW_o}}$	Ratio of the air velocity at the node $\mathrm{FEW_o}$ to vel_{AG}	-
$k_{\mathrm{vel,REW_o}}$	Ratio of the air velocity at the node $\mathrm{REW_o}$ to vel_{AG}	-
$k_{\mathrm{vel,FEW_m}}$	Ratio of the air velocity at the node $\mathrm{FEW_m}$ to vel_{AG}	-
$k_{\mathrm{vel,REW_m}}$	Ratio of the air velocity at the node $\mathrm{REW_m}$ to vel_{AG}	-
$k_{\mathrm{vel,FEW_i}}$	Ratio of the air velocity at the node $\mathrm{FEW_i}$ to vel_{AG}	-
$k_{\mathrm{vel,REW_i}}$	Ratio of the air velocity at the node $\mathrm{REW_i}$ to vel_{AG}	-
$k_{\mathrm{vel,FBS_r}}$	Ratio of the air velocity at the node $\mathrm{FBS_r}$ to vel_{AG}	-
$k_{\mathrm{vel,RBS_f}}$	Ratio of the air velocity at the node $\mathrm{RBS_f}$ to vel_{AG}	-

Table 3.35: Inverter thermal model parameters that are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42. Abbreviations: SDU: Switch-diode unit, SD_p: (Packaged) Semiconductor device, TSC: Top-side cooled, BSC: Bottom-side cooled.

Variable	Parameter definition	Unit
i_{top}	Inverter topology ID (1: 3L-TT, 2: 3L-NPC, 3: 2L, 4: 2L-3M-ser, 5: 2L-3M-par)	-
$I_{\text{r,ref,univ}}$	Reference value for the chip scaling factor sf_{univ}	A
	For the 2L-based inverter topologies ($i_{\text{top}} = 3/4/5$)	
SDU_1	SDU-class object for the upper SDU of one inverter half bridge (Fig. 2.19)	-
	For the 3L-NPC inverter topology ($i_{\text{top}} = 2$)	
SDU_1	SDU-class object for the upper SDU of one inverter half bridge (Fig. 2.19)	-
$D_{p,5}$	SD_p-class object for the upper neutral point clamping diode of one inverter half bridge (Fig. 2.19)	-
	For the 3L-TT inverter topology ($i_{\text{top}} = 1$)	
SDU_1	SDU-class object for the upper SDU of one inverter half bridge (Fig. 2.19)	-
SDU_2	SDU-class object for the SDU on the neutral point path (output side) of one inverter half bridge (Fig. 2.19)	-
	Properties of each SDU-class object $SDU_j \in \{SDU_1, SDU_2\}$	
$i_{\text{SDU-typ},j}$	SDU type ID (1: Transistor, 2: Transistor + external diode)	-
$S_{p,j}$	SD_p-class object for the transistor/switch of SDU_j	-
$D_{p,j}$	SD_p-class object for the optional external diode of SDU_j.	-
	Properties of each SD_p-class object $SD_{p,j} \in \{S_{p,1}, S_{p,2}, D_{p,1}, D_{p,2}, D_{p,5}\}$	
$I_{\text{r,ref},SD_{p,j}}$	$SD_{p,j}$ reference device rated current	A
$i_{\text{PACK-typ},SD_{p,j}}$	$SD_{p,j}$ reference device package cooling type ID (1: TSC, 2: BSC)	
$R_{\text{th,jc},SD_{p,j}}(I_{\text{r}})$	Fitting function of the junction-to-case thermal resistance of $SD_{p,j}$ vs. the rated current I_{r} of $SD_{p,j}$	K W^{-1}
$A_{\text{hs},SD_{p,j}}(I_{\text{r}})$	Fitting function of the thermal pad (top-side) surface area vs. the rated current I_{r} of $SD_{p,j}$	m^2
$A_{\text{pad},SD_{p,j}}(I_{\text{r}})$	Fitting function of the electrical pad (bottom-side) surface area vs. the rated current I_{r} of $SD_{p,j}$	m^2
$l_{SD_{p,j}}$	SD_j reference device package length	m
$w_{SD_{p,j}}$	SD_j reference device package width	m

Table 3.36: Initial/Ambient temperatures that are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42.

Variable	Parameter definition	Unit
$T_{\circ\mathrm{C,H,0}}$	Initial housing temperature	°C
$T_{\circ\mathrm{C,W,0}}$	Initial winding temperature	
$T_{\circ\mathrm{C,HS,0}}$	Initial heat sink temperature	
$T_{\circ\mathrm{C,BS,0}}$	Initial front/rear bearing shield temperature	
$T_{\circ\mathrm{C,amb}}$	Ambient air temperature	
$T_{\circ\mathrm{C,fl}}$	Flange contact temperature	

Table 3.37: Losses at initial temperatures which are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42. Abbreviation SDG: Semiconductor device group.

Variable	Parameter definition	Unit
$P_{\mathrm{Cu,0}}$	Motor copper/winding losses at $T_{\circ\mathrm{C,W,0}}$	W
$P_{\mathrm{Fe,S_t}}/P_{\mathrm{Fe,S_y}}$	Motor iron losses in the stator teeth/yoke	
$P_{\mathrm{SDG}_i\mathrm{,0}}$	SDG_i (total) losses for $i = 1, 2, \ldots, 5$ at an initial junction temperature	
$P_{\mathrm{SDG}_i\mathrm{,sw}}$	SDG_i switching losses for $i = 1, 2, \ldots, 5$	
$P_{\mathrm{C_{dc}}}$	Inverter DC link capacitor losses	
$P_{\mathrm{FB}}/P_{\mathrm{RB}}$	Front/rear bearing losses	

Table 3.38: Solver parameters that are parametrised in step S1 of the temperature calculation procedure shown in Fig. 3.42.

Variable	Parameter definition	Unit
$N_{\mathrm{NA,it,max}}$	Max. number of nodal analysis iterations	-
ΔT_{max}	Max. allowed deviation of the LPTN node temperatures between two nodal analyis results to reach convergence	K

3.9.3 IMD Lumped Parameter Thermal Network (LPTN)

In this section, the IMD LPTN is presented. This includes a description of the model structure and an overview of the key model equations. This section is divided into the following parts: In the first part, the top-level LPTN is presented. In the subsequent three parts, three multi-port sub-models of the LPTN are described: The thermal winding model (second part), the thermal inverter model (third part), and the thermal screw connection model (fourth part). In the last part, the 2-port sub-models of the LPTN are described.

Top-Level LPTN

Fig. 3.45 shows the top-level LPTN of the thermal IMD model with the underlying mechanical/geometry model from Fig. 3.44. The nets between any thermal resistances of the LPTN in Fig. 3.45 are referred to as LPTN nodes or thermal nodes. Each thermal node has a node ID ($\mathrm{FBS_f}$, $\mathrm{FBS_c}$, etc. in Fig. 3.45) and in general models the temperature of a point, line, surface, or body of one of the IMD parts that are defined in Fig. 3.43. The IMD part to which a thermal node belongs is indicated with a capital letter in the respective thermal node ID. For example, the thermal nodes SH_x with any subscript x are modelling different sections of the shaft. The subscripts of the thermal node IDs further indicate the position of the node with respect to the modelled part (e.g. i: inner, o: outer, f: front, r: rear, c: centre).
By naming the nodes of the LPTN, a separate naming of its thermal resistances is not necessary and hence not shown in Fig. 3.45. Instead, any thermal resistance between two thermal nodes with the general node IDs i and j is referred to as $R_{i\text{-}j}$. For example, the thermal resistance between the thermal nodes $\mathrm{FBS_f}$ and $\mathrm{FBS_c}$ is referred to as $R_{\mathrm{FBS_f}\text{-}\mathrm{FBS_c}}$.

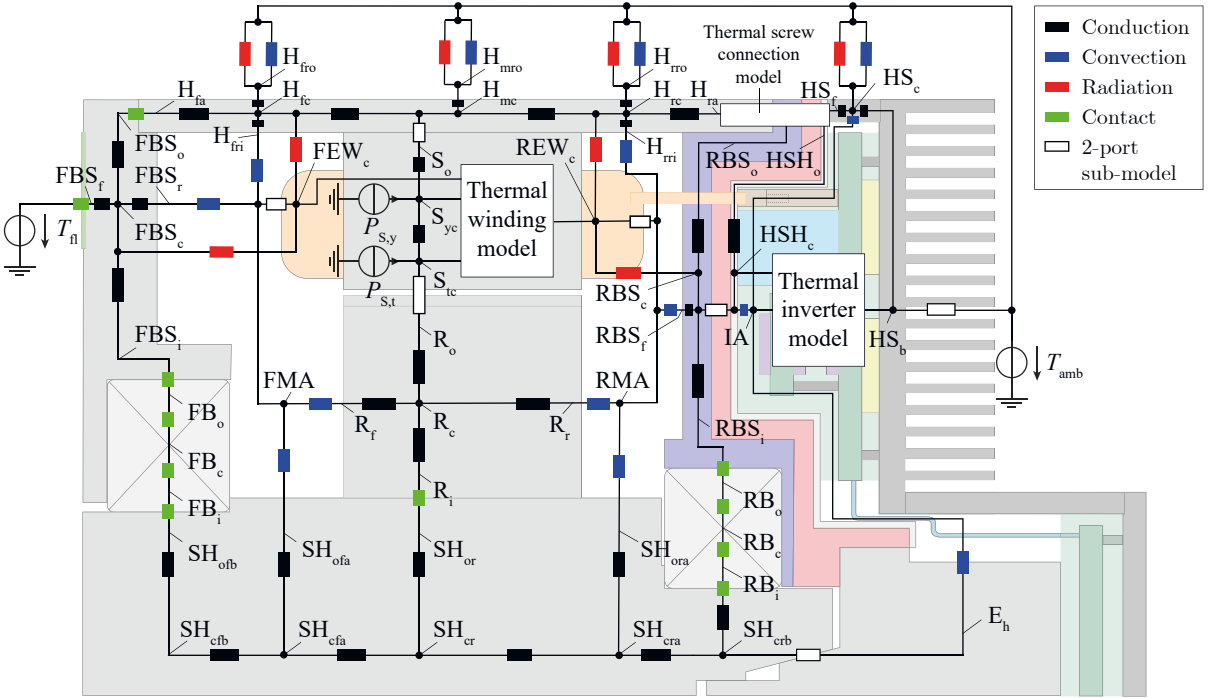


Figure 3.45: Top-level LPTN of the thermal IMD model.

The colours of the thermal resistances in Fig. 3.45 indicate the involved heat transfer mechanisms, i.e. conduction, convection, radiation, and heat transfer through contact surfaces. The formulas for the calculation of the thermal resistances result from an application of general thermal resistance formulas for basic geometries (cylinders, horizontal/vertical surfaces, etc.) to the mechanical IMD model from section 3.9.2. These general formulas are known from the literature on heat transfer theory. An overview of the used general formulas with references to the respective literature is given in the following for each of the four heat transfer mechanisms (conduction, convection, radiation, contact).

The **conductive** thermal resistances of the IMD LPTN (Fig. 3.45) are calculated with the following general formulas which result from section E1 of [24]:

$$R_{\mathrm{cd,A,cst}}(l,k,A) = \frac{l}{k \cdot A} \tag{3.169}$$

$$R_{\mathrm{cd,hcyl,r}}(r_\mathrm{o}, r_\mathrm{i}, k, l) = \ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right) \cdot \frac{1}{2\pi \cdot k \cdot l} \tag{3.170}$$

$$R_{\mathrm{cd,hcyls,r}}(r_\mathrm{o}, r_\mathrm{i}, k, l, \alpha) = \ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right) \cdot \frac{1}{\alpha \cdot k \cdot l} \tag{3.171}$$

$$R_{\mathrm{cd,cyl,r}}(l,k) = \frac{\ln(2)}{2\pi \cdot k \cdot l}. \tag{3.172}$$

There, $R_{\mathrm{cd,A,cst}}(l,k,A)$ in (3.169) is the thermal resistance of a body of the length l, the thermal conductivity k, and the (constant) cross-sectional area A.
$R_{\mathrm{cd,hcyl,r}}(r_\mathrm{o}, r_\mathrm{i}, k, l)$ in (3.170) is the thermal resistance in the radial direction of a hollow-cylinder with the outer radius r_o, the inner radius r_i, the thermal conductivity k, and the axial length l.
$R_{\mathrm{cd,hcyls,r}}(r_\mathrm{o}, r_\mathrm{i}, k, l, \alpha)$ in (3.171) is the thermal resistance in the radial direction of a hollow-cylinder segment with the same hollow-cylinder dimensions that are used in (3.170) and with the additional segment angle α.
$R_{\mathrm{cd,cyl,r}}(l,k)$ in (3.172) is the thermal resistance in the radial direction of a cylinder of radius r between the middle radius $r/2$ and the radius r. This formula results from evaluating $R_{\mathrm{cd,hcyl,r}}(r_\mathrm{o}, r_\mathrm{i}, k, l)$ from (3.170) with $r_\mathrm{o} = r$ and $r_\mathrm{i} = r/2$.

The **convective** thermal resistances of the IMD LPTN (Fig. 3.45) are calculated with separate models for external and internal convective thermal resistances. External convective thermal resistances are given by the blue thermal resistances in Fig. 3.45 that are connected to the thermal node of the constant ambient air temperature T_{amb}. The other blue thermal resistances in Fig. 3.45 are internal convective thermal resistances.
The external convective thermal resistances are calculated with the following general equations for the convective thermal resistance of a horizontal cylinder with the diameter d, the surface area A, and the surface temperature T, according to section 8.3.1 of [133]:

$$Gr_{\mathrm{d}} = \frac{\beta_{\mathrm{amb}} \cdot g \cdot (T - T_{\mathrm{amb}}) \cdot \rho_{\mathrm{amb}}^2 \cdot d^3}{\mu_{\mathrm{amb}}} \tag{3.173}$$

$$Pr = \frac{c_{\mathrm{p,amb}} \cdot \mu_{\mathrm{amb}}}{k_{\mathrm{amb}}} \tag{3.174}$$

$$\overline{Nu}_{\mathrm{d}} = \begin{cases} 0.525 \cdot (Gr_{\mathrm{d}} \cdot \mathrm{Pr})^{0.25}, Gr_{\mathrm{d}} \cdot \mathrm{Pr} < 10^9 \\ 0.129 \cdot (Gr_{\mathrm{d}} \cdot \mathrm{Pr})^{0.33}, Gr_{\mathrm{d}} \cdot \mathrm{Pr} > 10^9 \end{cases} \tag{3.175}$$

$$h_{\mathrm{cv,cyl,h}} = \frac{\overline{Nu}_{\mathrm{d}} \cdot k}{d} \tag{3.176}$$

$$R_{\mathrm{cv,cyl,h}} = \frac{1}{h_{\mathrm{cv,cyl,h}} \cdot A}. \tag{3.177}$$

There, Gr_{d} is the Grashof number, Pr is the Prandtl number, $\overline{Nu}_{\mathrm{d}}$ is the Nusselt number averaged over the cylinder surface, and $h_{\mathrm{cv,cyl,h}}$ is the convective heat transfer coefficient at the cylinder surface. The parameters β_{amb}, ρ_{amb}, μ_{amb}, $c_{\mathrm{p,amb}}$, and k_{amb} are fluid properties of the ambient air which were defined in Tab. 3.32 of the previous section.
The internal convective thermal resistances are calculated with the following general equation for the convective thermal resistance of a surface within a motor end space with the surface area A [23]:

$$h_{\mathrm{icvm}} = k_{\mathrm{icvm,1}}(1 + k_{\mathrm{icvm,2}} \cdot vel^{k_{\mathrm{icvm,3}}}) \tag{3.178}$$

$$R_{\mathrm{icvm}} = \frac{1}{h_{\mathrm{icvm}} \cdot A}. \tag{3.179}$$

Therein, h_{icvm} is the heat transfer coefficient for internal convection. The parameters $k_{\mathrm{icvm,1}}$, $k_{\mathrm{icvm,2}}$, and $k_{\mathrm{icvm,3}}$ are curve fit coefficients for a curve expressing the heat transfer coefficient of an internal surface of

a motor end space as a function of the local air velocity *vel* at that surface. Several of such curves, resulting from testing or CFD simulations, are shown in Fig. 9 of [23], which allows for a reasonable parametrisation of $k_{\mathrm{icvm},1}$, $k_{\mathrm{icvm},2}$, and $k_{\mathrm{icvm},3}$. The term $k_{\mathrm{icvm},1}$ in (3.178) accounts for the natural convection, whereas the term $k_{\mathrm{icvm},1} \cdot k_{\mathrm{icvm},2} \cdot (vel)^{k_{\mathrm{icvm},3}}$ accounts for the forced convection due to moving/rotating surfaces [23]. The local air velocity at an internal surface *vel* in (3.178) is approximated by one of in general three methods, depending on the internal air space (FMA/RMA/IA from Fig. 3.39) that is adjacent to the internal surface, and depending on the local surface velocity. These three methods are briefly summarised below.
1) For moving internal surfaces of the front/rear motor air space (FMA/RMA), such as the surfaces of the shaft and of the rotor iron, *vel* is approximated by the average surface speed.
2) For static internal surfaces of the front/rear motor air space with the general thermal node ID i, the local air velocity *vel* is approximated by $vel = k_{\mathrm{vel},i} \cdot vel_{\mathrm{AG}}$. There, vel_{AG} is the peripheral rotor speed and $k_{\mathrm{vel},i}$ is an estimation factor in the range of 0.1-1 which takes different exposures of the internal surfaces to the air gap opening into account.
3) For the internal surfaces of the inverter air space (IA), there is no contribution from forced convection because the inverter air space is separated from the moving air of the rear motor air space through the rear bearing shield. Therefore, the forced convection term of (3.178) is set to zero by setting *vel* to zero.

The **radiative** thermal resistances of the IMD LPTN (Fig. 3.45) are calculated with separate models for external/internal radiative thermal resistances. The definition of external/internal radiative thermal resistances is analogue to that of the external/interval convective thermal resistances.
The external radiative thermal resistances are calculated with the general formula for the thermal resistance between two grey radiating surfaces A_1 and A_2 with the temperatures T_1 and T_2, where the surface

A_1 is assumed to be in a large room, i.e. $A_1 \ll A_2$ (section K1 of [24]):

$$h_{rad} = \frac{\sigma \epsilon_1 (T_1^4 - T_2^4)}{T_1 - T_2} \tag{3.180}$$

$$\sigma = 5.67 \times 10^{-8}\,\mathrm{W\,m^{-2}\,K^{-4}} \tag{3.181}$$

$$R_{\mathrm{rad}} = \frac{1}{h_{rad} \cdot A_1}. \tag{3.182}$$

In (3.180), the ambient temperature T_{amb} must be inserted for T_2, and the parameters σ and ϵ_1 are the Stefan-Boltzmann constant and the emissivity of the surface A_1. All considered parameters for emissivities of IMD part surfaces are given in Tab. 3.32. The parametrisation of these parameters depends on the material selection for each IMD component which is kept general in this model.
The internal radiative thermal resistances are estimated with the following general formulas for the thermal resistance between two grey radiating surfaces A_1 and A_2 enclosed by adiabatic and reflecting surfaces (section K1 of [24]):

$$C_{12} = \frac{1}{\frac{1}{\tilde{\varphi}_{12}} + \left(\frac{1}{\epsilon_1} - 1\right) + \frac{A_1}{A_2} \cdot \left(\frac{1}{\epsilon_2} - 1\right)} \tag{3.183}$$

$$h_{\mathrm{rad,int}} = \frac{\sigma \cdot C_{12} \cdot (T_1^4 - T_2^4)}{T_1 - T_2} \tag{3.184}$$

$$R_{\mathrm{rad}} = \frac{1}{h_{\mathrm{rad,int}} \cdot A_1}. \tag{3.185}$$

There, C_{12} is the so-called radiation exchange factor and $h_{\mathrm{rad,int}}$ is the heat transfer coefficient for internal radiation. In (3.183), $\tilde{\varphi}_{12}$ is the modified view factor, and ϵ_1 and ϵ_2 are the surface emissivities of A_1 and A_2, respectively. The modified view factor depends on the spatial orientation between the two radiating surfaces. To limit the model complexity, heat transfer by internal radiation is only considered for parallel internal surfaces ($\tilde{\varphi}_{12} = 1$). An extension of this model to other surfaces is possible with the relations given in section K1 of [24].

The **contact** thermal resistances of the IMD LPTN (Fig. 3.45) are modelled with so-called equivalent air gaps, which corresponds to the modelling approach described in section II of [23]. With this approach,

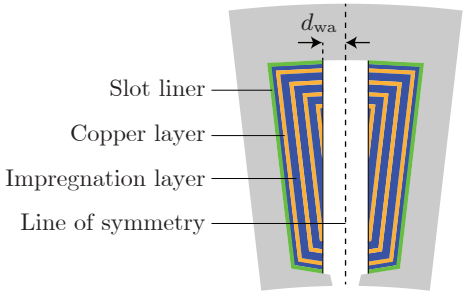


Figure 3.46: Layered winding model from [23], adapted to double-layer tooth-coil windings, shown for a single stator slot.

the thermal resistance of a contact area A is calculated with

$$R_{\mathrm{eag}} = \frac{l_{\mathrm{eq}}}{k_{\mathrm{eag}} \cdot A}, \tag{3.186}$$

where l_{eq} is the equivalent air gap length of the contact area and k_{eag} is the thermal conductivity of the air in the voids of the contact area. These voids are due to the imperfections of the surfaces in contact. Typical values for the equivalent air gap length l_{eq} for different combinations of materials can be found in the literature, e.g. in Tab. I and Tab. II of [23]. Based on a given material selection for the IMD components, such tables can be used to parametrise all equivalent air gap lengths that are considered in the thermal IMD model which are defined in Tab. 3.33.

Thermal Winding Model

The thermal winding model is a multi-port sub-model of the top-level LPTN (Fig. 3.45). This model is based on the layered winding model from Fig. 3 of [23], adapted to double-layer tooth-coil windings. The adapted winding model for one stator slot and hence for two coil-sides is shown in Fig. 3.46. The layered winding model is based on the assumption that conductors with approximately equal temperature have a similar distance from the stator [23]. Hence, the conductors can be represented by copper layers that are parallel to the slot walls, as shown in Fig. 3.46. The number of the copper and impregnation layers and the respective layer thicknesses are determined with the method described

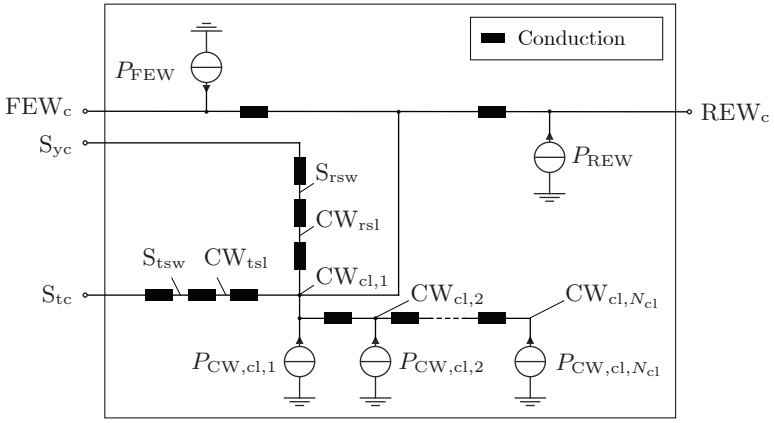


Figure 3.47: LPTN of the thermal winding model.

in [23].
The layered winding model shown in Fig. 3.46 is limited to the winding part that lies inside the stator slots. This winding part is referred to as core winding (CW) in distinction to the front/rear end winding (FEW/REW). The LPTN of the multi-port sub-model that is referred to as *thermal winding model* in the top-level LPTN (Fig. 3.45) is shown in Fig. 3.47 and includes the layered winding model of the CW and a connection to the FEW/REW.
With regard to the layered winding model of the CW, Fig. 3.47 shows the heat sources $P_{\mathrm{CW_{cl},}i}$ with $i = 1, 2, \ldots, N_{\mathrm{cl}}$ which indicate the copper losses that are dissipated in the i-th copper layer of the CW. This heat flows from the copper layer that is furthest away from the slot walls ($\mathrm{CW_{cl,}}N_{\mathrm{cl}}$) to the copper layer that is closest to the slot walls ($\mathrm{CW_{cl,1}}$). From there, the heat flows to the stator yoke/tooth centre ($\mathrm{S_{yc}}/\mathrm{S_{tc}}$).
With regard to the FEW/REW, Fig. 3.47 shows the copper losses dissipated in the FEW/REW ($P_{\mathrm{FEW}}/P_{\mathrm{REW}}$) and the connection between the CW and the thermal nodes of the FEW/REW via copper layer 1 ($\mathrm{CW_{cl,1}}$). Another part of the thermal FEW/REW model which includes the convective heat transfer to the front/rear motor air space is given later in the section on *Thermal 2-port sub-models*.

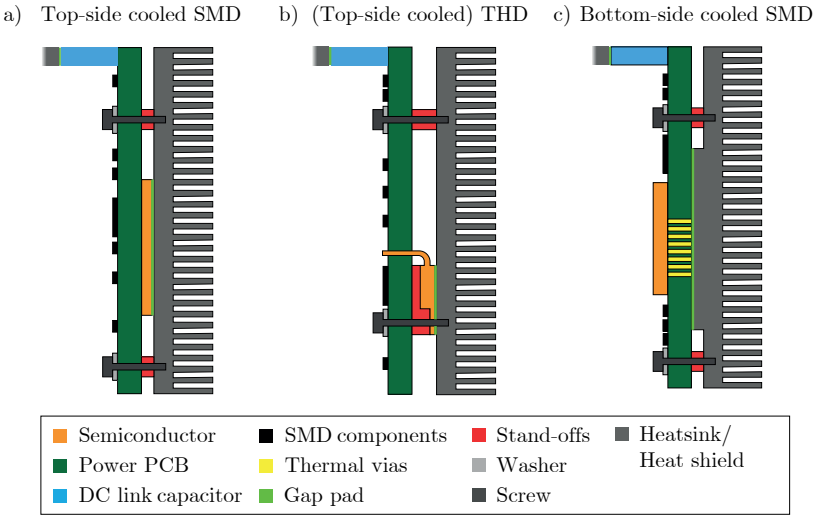


Figure 3.48: Semiconductor device mounting concepts for three common semiconductor package types.

Thermal Inverter Model

For the thermal inverter model, three common types of semiconductor packages are considered: 1) Top-side cooled (TSC) SMD packages. 2) (TSC) THD packages. 3) Bottom-side cooled (BSC) SMD packages. Fig. 3.48 shows the considered semiconductor device mounting concept for each of these semiconductor package types. In the mounting concept for TSC SMD packages (Fig. 3.48a) and in the mounting concept for THD packages (Fig. 3.48b), the semiconductor device is located between the PCB and the heat sink, and the thermal contact between the semiconductor device and the heat sink is realised with a gap pad. In the mounting concept for BSC SMD packages (Fig. 3.48c), the semiconductor device is located on the top side of the PCB, and the heat is dissipated from the the bottom side of the semiconductor device through thermal vias in the PCB and through a gap pad to the heat sink.
Based on the semiconductor device mounting concepts from Fig. 3.48, LPTNs of so-called semiconductor device groups (SDGs) are developed, as explained in the following. For any considered inverter topology, an SDG is defined as a group of identical semiconductor devices that pro-

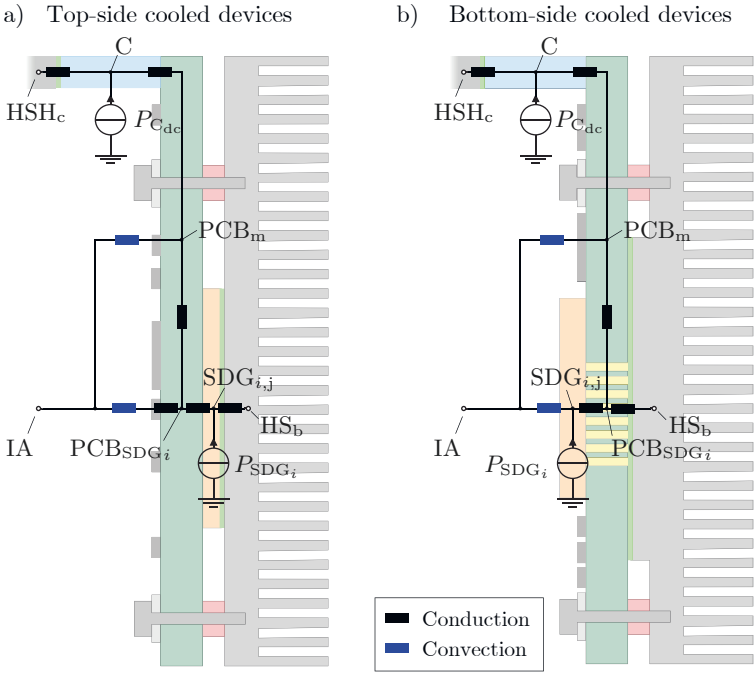


Figure 3.49: LPTN of a semiconductor device group (SDG$_i$) and of the inverter DC link capacitors for a) TSC semiconductor devices and b) BSC semiconductor devices.

duce the same losses over one fundamental period, assuming symmetrical output currents. As separate LPTNs for each semiconductor device within an SDG would consist of identical thermal resistances and lead to the same (average) node temperatures, the thermal resistances of such separate LPTNs can be parallel connected. This (theoretical) parallel connection results in a single LPTN for the SDG. Such an LPTN for a general SDG, referred to as SDG$_i$, is shown in Fig. 3.49a for TSC semiconductor devices and in Fig. 3.49b for BSC semiconductor devices. There, the two TSC device mounting concepts from Fig. 3.48a and Fig. 3.48b are modelled with the same LPTN from 3.49a due to the similar mechanical structure of these concepts.
The two LPTNs in Fig. 3.49 are similar as both LPTNs include the same thermal nodes at the model interface to the top-level LPTN

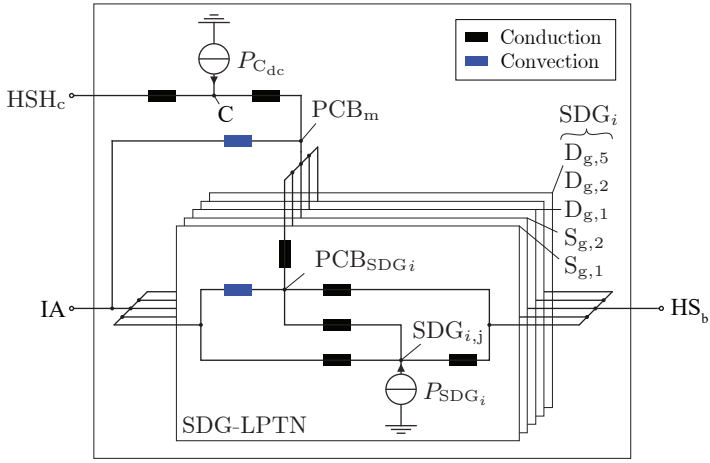


Figure 3.50: Thermal inverter model.

(HSH$_c$: Heat shield centre, IA: Inverter air, HS$_b$: Heat sink base), the same internal thermal nodes (SDG$_{i,j}$: Junctions of the SDs of SDG$_i$, PCB$_{SDG_i}$: PCB areas underneath the SDs of SDG$_i$ in the PCB middle plane, C: DC link capacitors of the inverter, PCB$_m$: PCB node with the mean PCB temperature), and the same heat sources (P_{SDG_i}: Losses of SDG$_i$, $P_{C_{dc}}$: DC link capacitor losses). Only which thermal resistances are considered between the thermal nodes, is different in these LPTNs. Due to this similarity between the LPTNs from Fig. 3.49, these LPTNs are summarised into one generic LPTN that is referred to as SDG-LPTN. To account for all considered inverter topologies (2L, 3L-NPC, 3L-TT, SPB, N_mP-2L), five of such SDG-LPTNs are connected in parallel, which results in the thermal inverter model in Fig. 3.50. For each considered inverter topology, the relevant SDGs are defined in Tab. 3.39, including the assignment of SDs to SDGs.

The thermal inverter model in Fig. 3.50 is generic as it can be adapted to any of the considered inverter topologies from Tab. 3.39 and to a TSC or BSC semiconductor device package type through the parametrisation of the model.

For example, to adapt the thermal inverter model in Fig. 3.50 to a 3L-TT inverter, only the SDG-LPTNs of the SDGs that are listed in Tab. 3.39 for the 3L-TT inverter topology (S$_{g,1}$, S$_{g,2}$, D$_{g,1}$, and D$_{g,2}$) are parametrised based on thermal semiconductor device parameters.

Table 3.39: Definition of semiconductor device groups (SDGs) for each considered inverter topology. The numbering of semiconductor devices corresponds to the numbering of the corresponding SDUs defined Fig. 2.19.

Inverter topology	SDG_i	Semiconductor devices
2L	$S_{g,1}$	$S_{p,1}$, $S_{p,2}$, …, $S_{p,6}$
	$D_{g,1}$ (optional)	$D_{p,1}$, $D_{p,2}$, …, $D_{p,6}$
3L-NPC	$S_{g,1}$	$S_{p,1}$, $S_{p,4}$, $S_{p,7}$, $S_{p,10}$, $S_{p,13}$, $S_{p,16}$
	$D_{g,1}$ (optional)	$D_{p,1}$, $D_{p,4}$, $D_{p,7}$, $D_{p,10}$, $D_{p,13}$, $D_{p,16}$
	$S_{g,2}$	$S_{p,2}$, $S_{p,3}$, $S_{p,8}$, $S_{p,9}$, $S_{p,14}$, $S_{p,15}$
	$D_{g,2}$ (optional)	$D_{p,2}$, $D_{p,3}$, $D_{p,8}$, $D_{p,9}$, $D_{p,14}$, $D_{p,15}$
	$D_{g,5}$	$D_{p,5}$, $D_{p,6}$, $D_{p,11}$, $D_{p,12}$, $D_{p,17}$, $D_{p,18}$
3L-TT	$S_{g,1}$	$S_{p,1}$, $S_{p,4}$, $S_{p,5}$, $S_{p,8}$, $S_{p,9}$, $S_{p,12}$
	$D_{g,1}$ (optional)	$D_{p,1}$, $D_{p,4}$, $D_{p,5}$, $D_{p,8}$, $D_{p,9}$, $D_{p,12}$
	$S_{g,2}$	$S_{p,2}$, $S_{p,3}$, $S_{p,6}$, $S_{p,7}$, $S_{p,10}$, $S_{p,11}$
	$D_{g,2}$ (optional)	$D_{p,2}$, $D_{p,3}$, $D_{p,6}$, $D_{p,7}$, $D_{p,10}$, $D_{p,11}$
SPB	$S_{g,1}$	$S_{p,1}$, $S_{p,2}$, …, $S_{p,6N_m}$
	$D_{g,1}$ (optional)	$D_{p,1}$, $D_{p,2}$, …, $D_{p,6N_m}$
N_mP-2L	$S_{g,1}$	$S_{p,1}$, $S_{p,2}$, …, $S_{p,6N_m}$
	$D_{g,1}$ (optional)	$D_{p,1}$, $D_{p,2}$, …, $D_{p,6N_m}$

In the other SDG-LPTNs ($D_{g,5}$ in the given example), the thermal resistances are set to $\infty/0$ so that these SDG-LPTNs have no effect on the temperature distribution. In an analogue manner the SDG-LPTNs in the thermal inverter model in Fig. 3.50 can be adapted to a TSC semiconductor package or to a BSC semiconductor package.

Thermal Screw Connection Model

The finned end cap/heat sink is connected to the stator housing with N_{SCR} screws that are evenly distributed around the heat sink circumference. The corresponding thermal screw connection model, which is indicated with a sub-model box in the top-level LPTN in Fig. 3.45, is shown in Fig. 3.51.
Therein, in order to obtain a conservative approximation of the thermal insulating capability of the screw connection, the thermal contact resis-

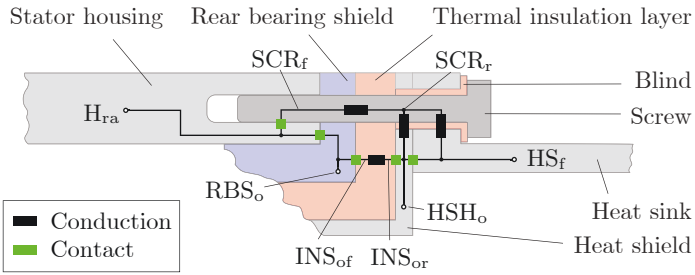


Figure 3.51: Thermal screw connection model.

tances $R_{\mathrm{H_{ra}\text{-}SCR_f}}$, $R_{\mathrm{RBS_o\text{-}INS_{of}}}$, and $R_{\mathrm{INS_{or}\text{-}HSH_o}}$ in Fig. 3.51 are set to zero. The other thermal resistances are calculated using the given basic thermal resistance formulas for conductive/contact thermal resistances with the mechanical model parameters from Tab. 3.30.

Thermal 2-Port Sub-Models

In this section, the thermal 2-port sub-models are presented which are indicated with a white resistance symbol in the top-level LPTN in Fig. 3.45. The (sub-level) LPTNs of these 2-port sub-models are given in Fig. 3.52 and are explained in the following.
Fig. 3.52a/b shows the part of the thermal model of the front/rear end winding (FEW/REW) which models the heat transfer to the front/rear motor air space (FMA/RMA). The black thermal resistances in Fig. 3.52a/b account for the thermal conduction between the temperature node of the FEW/REW centre (FEWc/REWc) and the temperature nodes of the outer/inner/middle end winding surfaces ($\mathrm{FEW_o}$/$\mathrm{FEW_i}$/ $\mathrm{FEW_m}$; analogue for the REW). The blue thermal resistances in Fig. 3.52a/b account for the convective heat transfer from the end winding surfaces to the front/rear motor air space (FMA/RMA).
Fig. 3.52c shows the LPTN of the connection between the motor shaft (SH) and the encoder (E). This connection is realised with a screw that lies in the rotational axis of the encoder shaft and that pulls the conical section of the encoder shaft against the conical bore hole of the motor shaft. Hence, there are two shaft-to-encoder contact surfaces whose thermal contact resistances are modelled with the green thermal resistances in Fig. 3.52c. The black thermal resistances in Fig. 3.52c account for the thermal conduction resistance of the encoder shaft screw

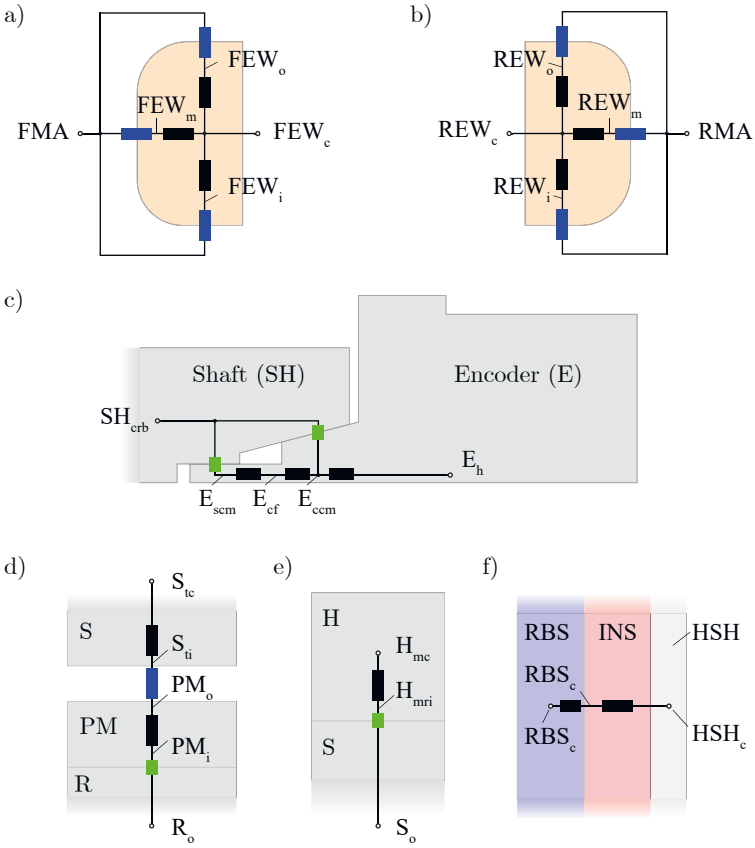


Figure 3.52: LPTNs of the 2-port sub-models of the following thermal resistances indicated in the top-level LPTN in Fig. 3.45 with a white resistance symbol: a) $R_{\mathrm{FEW_c\text{-}FMA}}$, b) $R_{\mathrm{REW_c\text{-}RMA}}$, c) $R_{\mathrm{SH_{crb}\text{-}E_h}}$, d) $R_{\mathrm{R_o\text{-}S_{tc}}}$, e) $R_{\mathrm{S_o\text{-}H_{mc}}}$, f) $R_{\mathrm{RBS_c\text{-}HSH_c}}$.

and of the conical encoder shaft section. The LPTN in Fig. 3.52c implies the simplifying assumption that the thermal contact between the encoder shaft and the encoder housing is ideal. With regard to the temperature limit of the electronics/inverter air, this simplifying assumption is also conservative because the temperature at the encoder

housing temperature node (E_h) and hence the temperature of the inverter air space (IA) is rather overestimated than underestimated.
Fig. 3.52d-f show the LPTNs of the 2-port sub-models from the top-level LPTN (Fig. 3.45) that are given by simple series-connections. For the thermal air gap resistance, indicated with a blue resistance symbol in Fig. 3.52d, the model from section VI of [23] is used. For the other thermal resistances from Fig. 3.52d-f, the already given general formulas for conductive/convective/contact thermal resistances are used.

3.10 Thermal Model of a Finned Heat Sink

This section presents a thermal model for the finned heat sink/end cap of the considered IMD concept C1 (Fig. 2.8). This model can for example be used to calculate the thermal resistance of the finned heat sink which is required for the thermal IMD model that was presented in the previous section.
In the following, first the structure of the developed heat sink model is presented in section 3.10.1. In section 3.10.2, the equations for calculating the thermal resistances of the model are given and explained. Finally, the model is validated through the results of a numerical simulation in section 3.10.3. The following sections 3.10.1-3.10.3 were previously published in essence in [134].

3.10.1 Model Structure

Fig. 3.53a shows the considered heat sink/end cap geometry. There, the parameters written in black in Fig. 3.53a are defined as independent parameters. The parameter written in blue in Fig. 3.53a is a dependent parameter $l_{box} = \max\{0, l_{ctr} - (l_{cyl} + d_{hs})\}$ defining the axial length of the encoder housing/box. The model covers different inverter sizes via the parameter l_{cyl}: When l_{cyl} is increased, the available inverter volume increases. The shape of the end cap changes depending on $(l_{cyl} + d_{hs})$. The different end cap shapes/types and the corresponding intervals of $(l_{cyl} + d_{hs})$ are given in Fig. 3.53b.
The developed thermal model is based on the LPTN shown in Fig. 3.54. The fin distribution is considered to be axis-symmetric, so that only half of the total number of fins N_f is considered in the LPTN, and so that the thermal resistances linked to these fins are multiplied by the factor 1/2. The temperature of the base plate that is in contact with the

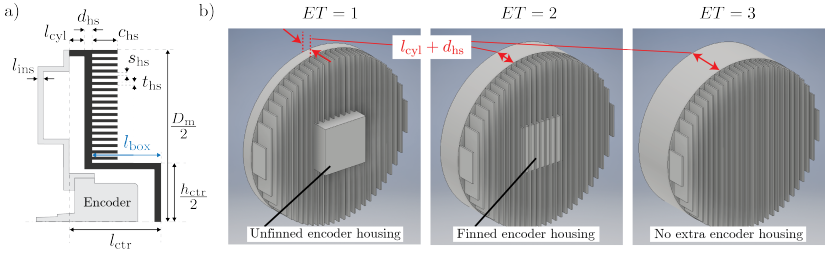


Figure 3.53: a) Cross section of an encoder-sided inverter-integrated end cap. The cross section matches to concept *C1* in Fig. 2.8. b) Different end cap shapes/types ET depending on $(l_{cyl} + d_{hs})$. Unfinned encoder housing ($ET = 1$): $(l_{cyl} + d_{hs}) \in [0, l_{ctr} - c_{hs}]$. Finned encoder housing ($ET = 2$): $(l_{cyl} + d_{hs}) \in [l_{ctr} - c_{hs}, l_{ctr}]$. No extra encoder housing/interior encoder ($ET = 3$): $(l_{cyl} + d_{hs}) \in [l_{ctr}, \infty]$.

power semiconductors in Fig. 3.54 is assumed to be constant and equal to T_{base}. Starting from this base plate, the dissipated semiconductor losses $P_{c,loss}$ are transferred to the ambient via three main surfaces: 1) Finned heat sink, 2) cylinder surface, and 3) encoder housing.
The total thermal resistance of the end cap R_{tot} is defined as $(T_{base} - T_{amb})/P_{c,loss}$ with $T_{base} = T_{e,amb,max}$. R_{tot} is determined by iteratively solving the non-linear system of equations given by the nodal equations of the LPTN in Fig. 3.54. The non-linearity is due to the temperature dependence of the convective and radiative thermal resistances in Fig. 3.54.

3.10.2 Model of Thermal Resistances

In the following, equations for calculating the thermal resistances of the LPTN in Fig. 3.54 are presented. All thermal resistances are considered except for the thermal resistances accounting for the surfaces next to the first fin ($R_{cv,eb}$, $R_{rad,eb}$, $R_{cv,es}$, $R_{rad,es}$) as these surfaces are usually small and therefore have a negligible contribution to the total thermal resistance. The geometry parameters used in this section are defined in Fig. 3.53 & Fig. 3.55.

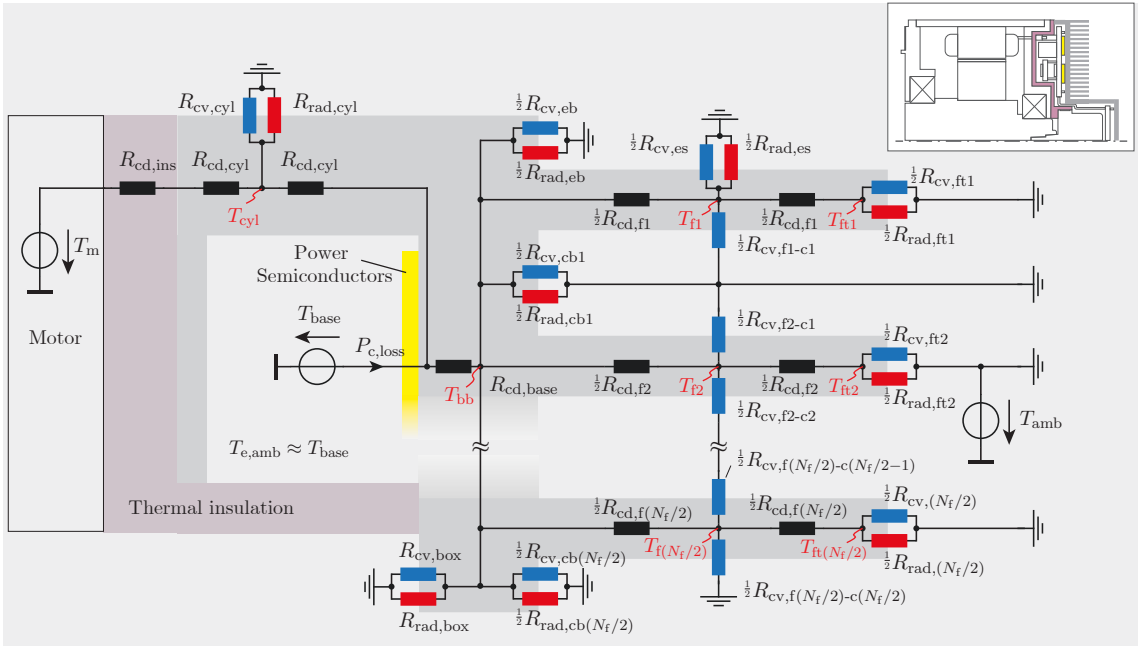


Figure 3.54: Lumped parameter thermal network (LPTN) of the heat sink for IMD concept *C1*, i.e. of a finned end cap with N_{f} fins (N_{f} is even) and with an encoder housing. The cross section of IMD concept *C1* from Fig. 2.8 is shown in the top right corner where the thermally modelled parts are colour-coded. The LPTN contains conductive, convective, and radiative thermal resistances indicated by the subscripts 'cd'/'cv'/'rad' and by the colours black/blue/red.

Conductive Thermal Resistances of the LPTN

For a compact notation, all conductive thermal resistances ($R_{\mathrm{cd},...}$) in Fig. 3.54 are expressed in terms of the function defined in (3.187) with the function parameters length l, cross-section area A and thermal conductivity λ.

$$R_{\mathrm{cd}}\{l, A, \lambda\} = \frac{l}{\lambda A} \tag{3.187}$$

$\boldsymbol{R_{\mathrm{cd,ins}}}$, the thermal resistance of the thermal insulation layer in Fig. 3.54, is calculated by evaluating (3.187) for the parameters given in (3.188).

$$R_{\mathrm{cd,ins}} = R_{\mathrm{cd}}\{l_{\mathrm{ins}}, \pi(\mathrm{D}_m/2)^2, \lambda_{\mathrm{ins}}\} \tag{3.188}$$

$\boldsymbol{R_{\mathrm{cd,cyl}}}$, the thermal resistance of the cylindrical part of the end cap in Fig. 3.54, is calculated by evaluating (3.187) for the parameters given in (3.189).

$$R_{\mathrm{cd,cyl}} = R_{\mathrm{cd}}\{{}^{l_{\mathrm{cyl}}}/_2, \pi((\mathrm{D}_m/2)^2 - (\mathrm{D}_m/2 - d_{\mathrm{hs}})^2), \lambda_{\mathrm{hs}}\} \tag{3.189}$$

$\boldsymbol{R_{\mathrm{cd,base}}}$, the thermal resistance of the finned base plate in Fig. 3.54, is calculated using (3.187) & (3.190)-(3.195). The calculation in (3.190) is based on an area-weighted average of the thermal resistance next to the encoder box $R_{\mathrm{cd,base,bb}}$ and of the thermal resistance on the encoder box ($R_{\mathrm{cd,base,ob}}$). The areas A_{bb} and A_{ob} used in (3.190)-(3.194) are defined in Fig. 3.55a.

$$R_{\mathrm{cd,base}} = \frac{A_{\mathrm{bb}}}{A_{\mathrm{tot}}} R_{\mathrm{cd,base,bb}} + \frac{A_{\mathrm{ob}}}{A_{\mathrm{tot}}} R_{\mathrm{cd,base,ob}} \tag{3.190}$$

$$A_{\mathrm{bb}} = \pi(\mathrm{D}_m/2)^2 - h_{\mathrm{ctr}}^2 \tag{3.191}$$

$$A_{\mathrm{ob}} = h_{\mathrm{ctr}}^2 \tag{3.192}$$

$$A_{\mathrm{tot}} = A_{\mathrm{bb}} + A_{\mathrm{ob}} \tag{3.193}$$

$$R_{\mathrm{cd,base,bb}} = R_{\mathrm{cd}}\{d_{\mathrm{hs}}, A_{\mathrm{bb}}, \lambda_{\mathrm{hs}}\} \tag{3.194}$$

$$R_{\mathrm{cd,base,ob}} = {}^1/_4 R_{\mathrm{cd}}\{{}^{h_{\mathrm{ctr}}}/_4, h_{\mathrm{ctr}} d_{\mathrm{hs}}, \lambda_{\mathrm{hs}}\} + {}^1/_4 R_{\mathrm{cd}}\{l_{\mathrm{box}}, h_{\mathrm{ctr}} d_{\mathrm{hs}}, \lambda_{\mathrm{hs}}\} \tag{3.195}$$

$\boldsymbol{R_{\mathrm{cd,f}i}}$, the thermal resistance of the i-th cooling fin in Fig. 3.54, is calculated using (3.187) & (3.196)-(3.200). $R_{\mathrm{cd,f}i}$ depends on the end cap type ET (Fig. 3.53b) and on the fin type FT_i (Fig. 3.55c), because these variables influence the fin geometry. In (3.196)-(3.200), $l_{\mathrm{f}i}$ is the

Table 3.40: Fluid flow properties of air.

Thermal conductivity of air	λ_{air}
Thermal expansion coefficient of air	β_{air}
Kinematic viscosity of air	ν_{air}
Prandtl number of air	Pr_{air}

vertical fin length of the i-th fin (Fig. 3.55a) and $c_{\mathrm{hs,avg}i}$ is an area-weighted average of the horizontal fin length used in the case of a finned encoder housing ($ET = 2$, Fig. 3.53b).

$$R_{\mathrm{cd,f}i} = \begin{cases} R_{\mathrm{cd}}\{{}^{c_{\mathrm{hs}}}/_{2}, l_{\mathrm{f}i} t_{\mathrm{hs}}, \lambda_{\mathrm{hs}}\} & \text{if } FT_i = 0 \vee ET = 3 \\ R_{\mathrm{cd}}\{{}^{c_{\mathrm{hs}}}/_{2}, (l_{\mathrm{f}i} - h_{\mathrm{ctr}}) t_{\mathrm{hs}}, \lambda_{\mathrm{hs}}\} & \text{if } FT_i = 1 \wedge ET = 1 \\ R_{\mathrm{cd}}\{{}^{c_{\mathrm{hs,avg}i}}/_{2}, l_{\mathrm{f}i} t_{\mathrm{hs}}, \lambda_{\mathrm{hs}}\} & \text{if } FT_i = 1 \wedge ET = 2 \end{cases} \tag{3.196}$$

$$c_{\mathrm{hs,avg}i} = \frac{A_{\mathrm{f,bb}i}}{A_{\mathrm{f,tot}i}} c_{\mathrm{hs}} + \frac{A_{\mathrm{f,ob}}}{A_{\mathrm{f,tot}i}} (c_{\mathrm{hs}} - l_{\mathrm{box}}) \tag{3.197}$$

$$A_{\mathrm{f,bb}i} = (l_{\mathrm{f}i} - h_{\mathrm{ctr}}) c_{\mathrm{hs}} \tag{3.198}$$

$$A_{\mathrm{f,ob}} = h_{\mathrm{ctr}} (c_{\mathrm{hs}} - l_{\mathrm{box}}) \tag{3.199}$$

$$A_{\mathrm{f,tot}i} = A_{\mathrm{f,bb}i} + A_{\mathrm{f,ob}} \tag{3.200}$$

With the equations above, the model is given for all conductive thermal resistances of the LPTN in Fig. 3.54. In the following, the convective thermal resistances of the LPTN are determined.

Convective Thermal Resistances of the LPTN

All convective thermal resistances ($R_{\mathrm{cv,...}}$) in Fig. 3.54 are calculated based on (3.201). There, h_{cv} is the convective heat transfer coefficient and A is the surface area of the convective heat transfer. In (3.201), h_{cv} is replaced by ${}^{(Nu\lambda_{\mathrm{air}})}/_{l_{\mathrm{crit}}}$ where Nu is the Nusselt number that describes the ratio of convective to conductive heat transfer at a wall surface. Heat transfer theory provides geometry-specific Nusselt number correlation functions $Nu(Ra)$ where Ra is the Rayleigh number that describes the flow regime of natural convective flow. The Rayleigh number, given in (3.202), depends on the temperature difference between the wall surface and ambient ($T_{\mathrm{w}} - T_{\mathrm{amb}}$), a geometry-specific critical length l_{crit}, the gravitational acceleration g, and different fluid

properties of air that are summarized in Tab. 3.40. These properties (λ_{air}, β_{air}, ν_{air}, Pr_{air}) are calculated at the so-called film temperature $^{(T_{\mathrm{w}}+T_{\mathrm{amb}})}/_{2}$ using curve fitting functions based on [24].

$$R_{\mathrm{cv}}\{Nu, A\} = \frac{1}{h_{\mathrm{cv}}A} = \frac{l_{\mathrm{crit}}}{Nu\lambda_{\mathrm{air}}A} \tag{3.201}$$

$$Ra\{l_{\mathrm{crit}}, T_{\mathrm{w}}, T_{\mathrm{amb}}\} = \frac{g\beta_{\mathrm{air}}(T_{\mathrm{w}} - T_{\mathrm{amb}})l_{\mathrm{crit}}^3 Pr_{\mathrm{air}}}{\nu_{\mathrm{air}}^2} \tag{3.202}$$

Three different geometry-specific Nusselt number correlation functions are used: Nu_{pl} for vertical plates [135], Nu_{cyl} for horizontal cylinders [135], and Nu_{ch} for channels between vertical plates [136], given in (3.203)-(3.205).

$$Nu_{\mathrm{pl}}\{l_{\mathrm{crit}}, T_{\mathrm{w}}, T_{\mathrm{amb}}\} = \left(\left(\frac{2}{\ln(1 + {}^{2}/_{(C_{\mathrm{l}}Ra^{1/4})})}\right)^6 + \left(C_{\mathrm{t,V}}\frac{Ra^{1/3}}{1 + 1.4e9 \cdot {}^{Pr_{\mathrm{air}}}/_{Ra}}\right)^6\right)^{1/6} \tag{3.203}$$

$$Nu_{\mathrm{cyl}}\{l_{\mathrm{crit}}, T_{\mathrm{w}}, T_{\mathrm{amb}}\} = \left(\left(\frac{2f}{\ln(1 + {}^{2f}/_{(0.772C_{\mathrm{l}}Ra^{1/4})})}\right)^{10} + \left(0.103Ra^{1/3}\right)^{10}\right)^{1/10} \tag{3.204}$$

$$Nu_{\mathrm{ch}}\{l_{\mathrm{crit}}, l_{\mathrm{c}}, T_{\mathrm{w}}, T_{\mathrm{amb}}\} = \left(\frac{576}{(Ra \cdot {}^{l_{\mathrm{crit}}}/_{l_{\mathrm{c}}})^2} + \frac{2.873}{(Ra \cdot {}^{l_{\mathrm{crit}}}/_{l_{\mathrm{c}}})^{1/2}}\right)^{-1/2} \tag{3.205}$$

The constants used in (3.203)-(3.204) are given in (3.206)-(3.208).

$$C_{\mathrm{l}} = \frac{0.671}{(1 + ({}^{0.492}/_{Pr_{\mathrm{air}}})^{9/16})^{4/9}} \tag{3.206}$$

$$C_{\mathrm{t,V}} = \frac{0.13Pr_{\mathrm{air}}^{0.22}}{(1 + 0.61Pr_{\mathrm{air}}^{0.81})^{0.42}} \tag{3.207}$$

$$f = 1 - \frac{0.13}{(0.772C_l Ra^{1/4})^{0.16}} \tag{3.208}$$

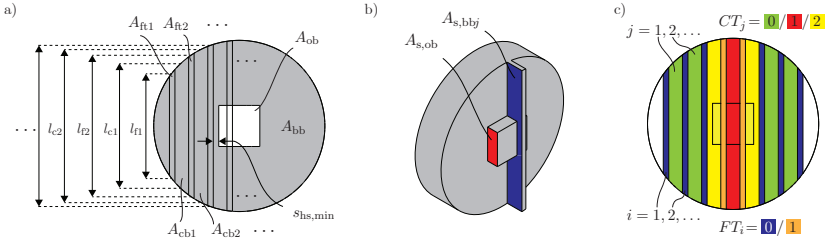


Figure 3.55: Definition of parameters used for calculating the thermal resistances of the LPTN in Fig. 3.54 based on an exemplary finned end cap. a) Front view with geometry parameters. b) Side view with geometry parameters where only one fin and the encoder box are shown for better visibility of the defined surfaces. c) Front view with a definition of channel types (CT_j) and fin types (FT_i). Channel types: Channel next to the encoder box area ($CT_j = 0$), channel overlaying the encoder box area ($CT_j = 1$), channel containing one vertical edge of the encoder box area ($CT_j = 2$). Fin types: Fin next to the encoder box area ($FT_i = 0$), fin (at least partly) overlaying the encoder box area ($FT_i = 1$).

The Nusselt number correlation functions in (3.203)-(3.205) are written for a general vertical plate, horizontal cylinder, or vertical channel. There, the critical length l_{crit} is given by a vertical plate length, a cylinder diameter, and a channel width, respectively. In addition, Nu_{ch} in (3.205) depends on a vertical channel length l_{c}. In the following, for defining the thermal resistances of specific surfaces from Fig. 3.54, l_{crit} is replaced by the critical lengths of these surfaces and the wall temperature T_{w} is replaced by the node temperatures of the LPTN nodes (Fig. 3.54) of the respective surfaces.

$\boldsymbol{R_{\mathrm{cv,f}i\text{-}cj}}$, the thermal resistance between the i-th fin and the j-th channel in Fig. 3.54, is calculated based on the Nusselt number correlation function in (3.205). This function as well as other models for finned heat sinks from literature such as [137–139] were developed for heat sinks with a rectangular base plate (rectangular heat sinks). In this thesis, the model from [136] is adapted to heat sinks with a circular base plate (called circular heat sinks) by approximating a circular heat sink as a parallel connection of different rectangular heat sinks, each of which consists of only one cooling channel. Therefore, $R_{\mathrm{cv,f}i\text{-}cj}$ is

not constant for all fin sides as would be the case in a rectangular heat sink. Instead, $R_{\mathrm{cv,f}i\text{-}\mathrm{c}j}$ is calculated individually for each fin side using (3.209)-(3.214). In (3.209), $l_{\mathrm{c}j}$ is the vertical length of the j-th channel as defined in Fig. 3.55a. Depending on the end cap type ET (Fig. 3.53b) and on the channel type CT_j (Fig. 3.55c), the encoder box can decrease the surface area $A_{\mathrm{fc}j}$ for convective heat transfer from a fin side as specified in (3.210) and the effective fin spacing $s_{\mathrm{fc}j}$ as specified in (3.211)-(3.214). The minimum fin spacing $s_{\mathrm{hs,min}}$ and the surface areas $A_{\mathrm{s,ob}}$ & $A_{\mathrm{s,bb}j}$, which are used in (3.211)-(3.214), are shown in Fig. 3.55a & 3.55b.

$$R_{\mathrm{cv,f}i\text{-}\mathrm{c}j} = R_{\mathrm{cv}}\{Nu_{\mathrm{ch}}\{s_{\mathrm{fc}j}, l_{\mathrm{c}j}, T_{\mathrm{f}i}, T_{\mathrm{amb}}\}, A_{\mathrm{fc}j}\} \quad \text{for} \quad i = 1 \ldots {}^{N_{\mathrm{f}}}\!/_{2},\ j = \{i-1, i\} | j > 0 \tag{3.209}$$

$$A_{\mathrm{fc}j} = \begin{cases} c_{\mathrm{hs}} l_{\mathrm{c}j} & \text{if } CT_j \in \{0,2\} \vee (CT_j = 1 \wedge ET = 3) \\ c_{\mathrm{hs}}(l_{\mathrm{c}j} - h_{\mathrm{ctr}}) & \text{if } CT_j = 1 \wedge ET = 1 \\ c_{\mathrm{hs}} l_{\mathrm{c}j} - h_{\mathrm{ctr}} l_{\mathrm{box}} & \text{if } CT_j = 1 \wedge ET = 2 \end{cases} \tag{3.210}$$

$$s_{\mathrm{fc}j} = \begin{cases} s_{\mathrm{hs}} & \text{if } CT_j \in \{0,1\} \vee ET = 3 \\ \frac{A_{\mathrm{s,ob}}}{A_{\mathrm{s,tot}j}} s_{\mathrm{hs,min}} + \frac{A_{\mathrm{s,bb}j}}{A_{\mathrm{s,tot}j}} s_{\mathrm{hs}} & \text{if } CT_j = 2 \wedge ET \in \{1,2\} \end{cases} \tag{3.211}$$

$$A_{\mathrm{s,ob}} = \begin{cases} h_{\mathrm{ctr}} c_{\mathrm{hs}} & \text{if } CT_j = 2 \wedge ET = 1 \\ h_{\mathrm{ctr}} l_{\mathrm{box}} & \text{if } CT_j = 2 \wedge ET = 2 \end{cases} \tag{3.212}$$

$$A_{\mathrm{s,tot}j} = l_{\mathrm{c}j} c_{\mathrm{hs}} \tag{3.213}$$

$$A_{\mathrm{s,bb}j} = A_{\mathrm{s,tot}j} - A_{\mathrm{s,ob}} \tag{3.214}$$

$\boldsymbol{R_{\mathrm{cv,cb}j}}$ and $\boldsymbol{R_{\mathrm{cv,ft}i}}$ account for the convective heat transfer through the bottom of the j-th channel and through the fin tip of the i-th fin in Fig. 3.54. These thermal resistances can be neglected for long fins (large c_{hs}) but ensure a seamless transition between R_{tot} with short fins (small c_{hs}) and R_{tot} without any fins ($c_{\mathrm{hs}} = 0$). $R_{\mathrm{cv,cb}j}$ and $R_{\mathrm{cv,ft}i}$ are calculated by evaluating (3.215)-(3.216) based on (3.201) & (3.203). The surface areas $A_{\mathrm{cb}j}$ and $A_{\mathrm{ft}i}$ used in (3.215)-(3.216) are defined in Fig. 3.55a.

$$R_{\mathrm{cv,cb}j} = R_{\mathrm{cv}}\{Nu_{\mathrm{pl}}\{l_{\mathrm{c}j}, T_{\mathrm{bb}}, T_{\mathrm{amb}}\}, A_{\mathrm{cb}j}\} \qquad \text{for } j = 1 \ldots {}^{N_{\mathrm{f}}}\!/_{2} \tag{3.215}$$

$$R_{\mathrm{cv,ft}i} = R_{\mathrm{cv}}\{Nu_{\mathrm{pl}}\{l_{\mathrm{f}i}, T_{\mathrm{ft}i}, T_{\mathrm{amb}}\}, A_{\mathrm{ft}i}\} \qquad \text{for } i = 1 \ldots {}^{N_{\mathrm{f}}}\!/_{2} \tag{3.216}$$

$\boldsymbol{R_{\mathrm{cv,box}}}$ and $\boldsymbol{R_{\mathrm{cv,cyl}}}$, the thermal resistances of the vertical sides of the encoder box and of the cylindrical part of the end cap, are calculated in

the same manner based on (3.201), (3.203)-(3.204), and (3.217)-(3.220).

$$R_{\mathrm{cv,box}} = R_{\mathrm{cv}}\{Nu_{\mathrm{pl}}\{h_{\mathrm{ctr}}, T_{\mathrm{bb}}, T_{\mathrm{amb}}\}, 2A_{\mathrm{box}}\} \tag{3.217}$$

$$R_{\mathrm{cv,cyl}} = R_{\mathrm{cv}}\{Nu_{\mathrm{cyl}}\{\mathrm{D}_m, T_{\mathrm{cyl}}, T_{\mathrm{amb}}\}, A_{\mathrm{cyl}}\} \tag{3.218}$$

$$A_{\mathrm{box}} = \max\{0, h_{\mathrm{ctr}}(l_{\mathrm{box}} - c_{\mathrm{hs}})\} \tag{3.219}$$

$$A_{\mathrm{cyl}} = \pi \mathrm{D}_m(l_{\mathrm{cyl}} + d_{\mathrm{hs}}) \tag{3.220}$$

So far, the model is given for all convective thermal resistances of the LPTN in Fig. 3.54. In the following, the radiative thermal resistances of the LPTN are determined.

Radiative Thermal Resistances of the LPTN

All thermal resistances accounting for thermal radiation ($R_{\mathrm{rad,...}}$) in Fig. 3.54 are based on (3.221) where ϵ_{hs} is the emissivity of the end cap material and σ is the Stefan-Boltzmann constant. Only surface-to-ambient radiation of surfaces whose normal vector is pointing to ambient is considered.

$$R_{\mathrm{rad}}\{A, T_{\mathrm{w}}, T_{\mathrm{amb}}\} = \frac{T_{\mathrm{w}} - T_{\mathrm{amb}}}{\epsilon_{\mathrm{hs}}\sigma(T_{\mathrm{w}}^4 - T_{\mathrm{amb}}^4)A} \tag{3.221}$$

The thermal resistances $\boldsymbol{R_{\mathrm{rad,cb}j}}$, $\boldsymbol{R_{\mathrm{rad,ft}i}}$, $\boldsymbol{R_{\mathrm{rad,box}}}$, and $\boldsymbol{R_{\mathrm{rad,cyl}}}$ in Fig. 3.54 are calculated by evaluating (3.221) with the parameters given in (3.222)-(3.225). Therein, the surface areas $A_{\mathrm{...}}$ are defined in Fig. 3.55a and (3.217)-(3.218). The temperatures $T_{\mathrm{...}}$ in (3.222)-(3.225) are the temperatures of the corresponding LPTN nodes in Fig. 3.54.

$$R_{\mathrm{rad,cb}j} = R_{\mathrm{rad}}\{A_{\mathrm{cb}j}, T_{\mathrm{bb}}, T_{\mathrm{amb}}\} \tag{3.222}$$

$$R_{\mathrm{rad,ft}i} = R_{\mathrm{rad}}\{A_{\mathrm{ft}i}, T_{\mathrm{ft}i}, T_{\mathrm{amb}}\} \tag{3.223}$$

$$R_{\mathrm{rad,box}} = R_{\mathrm{rad}}\{4A_{\mathrm{box}}, T_{\mathrm{bb}}, T_{\mathrm{amb}}\} \tag{3.224}$$

$$R_{\mathrm{rad,cyl}} = R_{\mathrm{rad}}\{A_{\mathrm{cyl}}, T_{\mathrm{cyl}}, T_{\mathrm{amb}}\} \tag{3.225}$$

For the presented analytical thermal model, a validation based on a numerical simulation is given in following section.

3.10.3 Validation

To validate the proposed analytical model, a 3D CFD simulation of an end cap of IMD concept *C1* is performed and the resulting thermal resistance is compared to the thermal resistance resulting from the

Table 3.41: End cap specifications used for the validation of the proposed thermal model.

Motor/end cap diameter	D_m	250 mm
End plate thickness	d_{hs}	3 mm
Encoder housing height	h_{ctr}	100 mm
Length of encoder + control PCB	l_{ctr}	100 mm
Fin length	c_{hs}	25 mm
Fin spacing	s_{hs}	9 mm
Fin thickness	t_{hs}	1 mm
Max. electronics temp.	$T_{\mathrm{e,amb,max}}$	85 °C
Ambient temperature	T_{amb}	40 °C
End cap th. conductivity (Al)	λ_{hs}	236 $\mathrm{W\,m^{-1}\,K^{-1}}$
End cap emissivity (black Al)	ϵ_{hs}	0.95

Table 3.42: Thermal resistance of the end cap resulting from the proposed model ($R_{\mathrm{th,model}}$) compared to the thermal resistance resulting from the simulation ($R_{\mathrm{th,sim}}$) for the end cap specifications given in Tab. 3.41.

Radiation incl. -	$R_{\mathrm{th,model}}$ [$\mathrm{K\,W^{-1}}$]	$R_{\mathrm{th,sim}}$ [$\mathrm{K\,W^{-1}}$]	Δ [%]
No	0.869	0.905	4.0
Yes	0.638	0.610	-4.6

proposed analytical model. For the validation, the end cap is considered thermally isolated from the motor and from the cylindrical part of the end cap in Fig. 3.53b in order to reduce the required simulation time. The considered end cap specifications are summarized in Tab. 3.41. The resulting thermal resistances are given in Tab. 3.42 with and without considering thermal radiation in the model and in the CFD simulation. The results show a good agreement between the analytical and the numerical solution with a deviation of $< 5\,\%$.

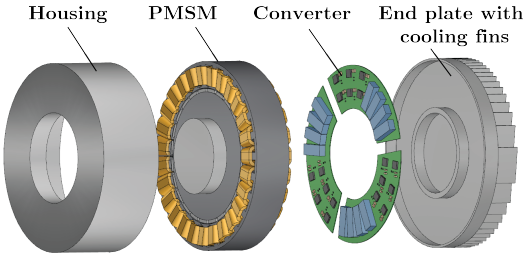


Figure 3.56: Basic concept of an integrated motor drive used for IMD volume model 1.

3.11 IMD Volume Model

In this section, two IMD volume models, referred to as IMD volume model 1/2, are described which can be used to calculate the volume and thus the power density of the overall IMD system, including the motor and the inverter.
The main difference between the two models is that they are based on mechanical models of different degrees of detail: IMD volume model 1 is based on the basic mechanical integration concept shown in Fig. 3.56, whereas IMD volume model 2 is based on the more detailed mechanical IMD model from Fig. 3.44 described in section 3.9.2.

3.11.1 IMD Volume Model 1

In this model, the system volume is given by

$$Vol_{\mathrm{sys}} = Vol_{\mathrm{conv}} + Vol_{\mathrm{mot}}, \tag{3.226}$$

where $Vol_{\mathrm{sys}}/Vol_{\mathrm{conv}}/Vol_{\mathrm{mot}}$ is the system/converter/motor volume. Based on the basic concept of an integrated motor drive from Fig. 3.56, the converter volume is approximated as the sum of the volume of the populated PCBs (PPCB) and of the heat sink volume. The PPCB volume is defined as the volume of the smallest possible cylindrical box around the PPCB which is referred to as PPCB box. This leads to the

following equations:

$$Vol_{\mathrm{conv}} = Vol_{\mathrm{ppcb}} + Vol_{\mathrm{hs}} \tag{3.227}$$

$$Vol_{\mathrm{ppcb}} = h_{\mathrm{pPCB}} \cdot A_{\mathrm{box,ppcb}} \tag{3.228}$$

$$A_{\mathrm{box,ppcb}} = \pi \cdot r_{\mathrm{PCB,o}}^2. \tag{3.229}$$

There, Vol_{ppcb} is the PPCB volume, Vol_{hs} is the heat sink volume, h_{pPCB} is the (axial) PPCB height, and $A_{\mathrm{box,ppcb}}$ is the base surface area of the PPCB box. The PPCB height is imposed by the highest component on the PCB which is expected to be given by the DC link capacitors. For small DC link capacitors, a minimum PPCB height $h_{\mathrm{pPCB,min}}$ is considered, which leads to

$$h_{\mathrm{pPCB}} = \max\{h_{\mathrm{dc,mod}} + h_{\mathrm{PCB,bs}}, h_{\mathrm{pPCB,min}}\}. \tag{3.230}$$

Therein, $h_{\mathrm{PCB,bs}}$ is the height of the PCB bottom side including the thickness of the PCB itself. The height of the DC link capacitors $h_{\mathrm{dc,mod}}$ in (3.230) is calculated with (3.88), as explained in the context of the DC link dimensioning in section 3.2.6 on the DC link capacitor design. The heat sink volume in this IMD volume model is calculated using the approach described in [39] (equations (2.14)-(2.15)). This approach is based on an estimation of the minimum heat sink volume that is required to keep the junction temperatures of the semiconductor devices below the maximum rated junction temperature. This estimation includes the assumption of a cooling system performance index (CSPI) for the considered heat sink technology. In [39], forced air cooling is considered for which a CSPI of $10\,\mathrm{W\,K^{-1}\,L^{-1}}$ is assumed. In this IMD volume model, naturally convective cooled heat sinks are considered for which a CSPI of $4.4\,\mathrm{W\,K^{-1}\,L^{-1}}$ is assumed as this value was already experimentally achieved [140].
The motor volume Vol_{mot} in (3.226) is approximated by the cylindrical stator of length l_{s} and diameter D_{s}, which results in

$$Vol_{\mathrm{mot}} = \pi \cdot \left(\frac{D_{\mathrm{s}}}{2}\right)^2 \cdot l_{\mathrm{s}}. \tag{3.231}$$

3.11.2 IMD Volume Model 2

In this model, the system volume Vol_{sys} results from the following equations, whose input parameters on the right-hand sides are given by the

independent geometry parameters of the mechanical IMD model given in Fig. 3.44 from section 3.9.2:

$$l_{\text{SH-E,2}} = (r_{\text{SH,bh,2}} - r_{\text{E,2}}) \cdot \frac{l_{\text{SH,bh,2}}}{r_{\text{SH,bh,2}} - r_{\text{SH,bh,1}}} \tag{3.232}$$

$$l_{\text{SH-E,3}} = l_{\text{E,2}} - l_{\text{SH-E,2}} \tag{3.233}$$

$$l_{\text{IMD,c,ET1}} = l_{\text{SH,f}} + l_{\text{SH,m}} + l_{\text{SH,r}} + l_{\text{SH-E,3}} + l_{\text{E,3}} + l_{\text{E,4}} + h_{\text{PCPCB}} + d_{\text{hs}} \tag{3.234}$$

$$h_{\text{pPCB}} = \max\{h_{\text{dc,mod}} + h_{\text{PCB,bs}}, h_{\text{pPCB,min}}\} \tag{3.235}$$

$$l_{\text{cyl}} = h_{\text{pPCB}} \tag{3.236}$$

$$l_{\text{IMD,full-D}} = l_{\text{FBS}} + l_{\text{H}} + d_{\text{RBS}} + l_{\text{ins}} + d_{\text{HSH}} + l_{\text{cyl}} + d_{\text{hs}} + c_{\text{hs}} \tag{3.237}$$

$$l_{\text{box,rest}} = \max\{0, l_{\text{IMD,c,ET1}} - l_{\text{IMD,full-D}}\} \tag{3.238}$$

$$h_{\text{ctr}} = h_{\text{ctr,i}} + 2 \cdot d_{\text{hs}} \tag{3.239}$$

$$Vol_{\text{sys}} = l_{\text{IMD,full-D}} \cdot \pi \cdot r_{\text{H,o}}^2 + l_{\text{box,rest}} \cdot h_{\text{ctr}}^2. \tag{3.240}$$

The left-hand side parameters in (3.232)-(3.239) are dependent geometry parameters of the IMD geometry model. The dependent parameters $l_{\text{SH-E,2}}$, $l_{\text{SH-E,3}}$, h_{pPCB}, l_{cyl}, $l_{\text{box,rest}}$, and h_{ctr} are defined in Fig. 3.44. The other left-hand side parameters, $l_{\text{IMD,c,ET1}}$ and $l_{\text{IMD,full-D}}$ from (3.234) and (3.237), are defined as the axial length of the complete IMD through the motor rotation axis and as the axial length along which the IMD has its full diameter of $2r_{\text{H,o}}$, respectively. Based on these lengths, the system volume Vol_{sys} is calculated in (3.240) as the sum of a cylinder volume (which includes the IMD from its front side to the heat sink fin tips) and a cuboid volume (which includes the part of the encoder box that stands out of the heat sink fins).
Furthermore, the following sub-volumes of the system volume Vol_{sys} are considered: 1) Motor volume, Vol_{mot}. 2) PPCB volume, Vol_{ppcb}. 3) Heat sink volume, Vol_{hs}. 4) Insulation layer volume, Vol_{ins}. 5) Heat shield volume, Vol_{hsh}. 6) Volume of the cuboid containing the encoder and the populated control PCB (PCPCB), Vol_{enc}. 7) Residual inverter air space volume, $Vol_{\text{ia,rest}}$. The calculation of these sub-volumes is based on relatively simple geometry relations which also use the independent parameters of the IMD geometry model (Fig. 3.44) as input parameters.

3.12 IMD Cost Model

In this section, an IMD cost model is briefly described which can be used in IMD design procedures that include low costs as an additional design target besides high power density/efficiency. Such an IMD design procedure is presented later in section 4.2.
The total system/IMD cost is modelled as the sum of the inverter cost and the motor cost. For the inverter cost, the cost model from [141] is used. This model incorporates the chip cost, consisting of the power semiconductor cost K_{sc} and the cost of auxiliary ICs K_{ic}, the DC link capacitor cost K_{dc}, the PCB cost K_{pcb}, and the heat sink cost K_{hs}. The motor cost K_{mot} is approximated based on the cost of the copper windings, the iron laminations (rotor and stator), and the magnets. The cost of the copper windings is calculated based on the copper volume and is hence independent of the number of turns under the assumption of a constant copper fill factor.

4

Optimal Design of Integrated Motor Drives

Based on the selected concepts for IMDs from chapter 2 and the models for IMDs from chapter 3, different design studies are performed, where each design study includes two essential parts: 1) A developed general design procedure for the optimal design of IMDs or of an IMD component. 2) The application of this design procedure to exemplary IMD specifications of a high-torque low-speed IMD. Both parts are given in this chapter for three different design studies which are described in the following.

The first design study is the *Optimal Design and Comparison of IMDs using an SPB Converter combined with a 3-, 6-, 9-, or 12-phase PMSM* which is presented in section 4.1 and which was previously published in [98]. This design study includes a general IMD design procedure for optimal power density/efficiency (2D optimisation), where only the SPB-topology is considered and where the motor design is kept variable (motor stage MS3). This IMD design procedure is referred to as *IMD-Design-Proc-1.*

The second design study is the *Optimal Design and Comparison of IMDs using different Topologies (2L/3L/modular), PWM Variants, and Switch Technologies (Si/SiC/GaN)* which is presented in section 4.2 and which was previously published in [89]. This design study includes another general IMD design procedure, which optimises power density/efficiency/cost (3D optimisation) and which covers a relatively large inverter design space including all selected inverter topologies, PWM variants, and semiconductor technologies selected in chapter 2. With regard to the motor design space, the winding scheme and the

number of turns are kept variable (motor stage M2b). This IMD design procedure is referred to as *IMD-Design-Proc-2*.
The third design study is the calculation of the *Cooling Limits of Passively Cooled IMDs* which is presented in section 4.3 and which was previously published in [134]. This design study includes a general design procedure for a finned inverter heat sink/end cap to achieve a maximum cooling system performance index (CSPI). This design procedure is referred to as *HS-Design-Proc*. It can be used to pre-optimise the thermal resistance of the inverter heat sink which is required for *IMD-Design-Proc-2*.

4.1 Optimal Design and Comparison of IMDs using an SPB Converter combined with a 3-, 6-, 9-, or 12-phase PMSM

This design study focuses on the SPB converter topology in combination with PMSMs with different phase numbers. The topology of the SPB-C is shown in Fig. 4.1a for 2, 3, and 4 SPB-modules. In this design study, each SPB-module is considered to have only one DC link capacitor and is connected to a 3-phase winding system of a motor in multi-star point connection. The main advantages of the SPB-C are: Low voltage semiconductor devices with low $R_{\mathrm{ds,on}}$ can be used due to the series connection, fault-tolerance, and modularity ensuring a compact integrated system. The latter advantage is presented in different publications that analyse converter topologies suitable for an Integrated Modular Motor Drive (IMMD) [77], [8].
Different publications, such as [77] and [59], consider the SPB-C in combination with modular three-phase motors, i.e. motors having as many phase-aligned three-phase winding systems as SPB-modules. However, the SPB-C is also suitable for motors with non-phase-aligned three-phase winding systems. In [8], the possibility of using either phase-aligned or non-phase-aligned winding systems is mentioned but the effect on the system performance is not analysed. Therefore, this analysis is presented in this thesis through this design study. Fig. 4.1b shows the magnetic winding axes for different possible alignments. The

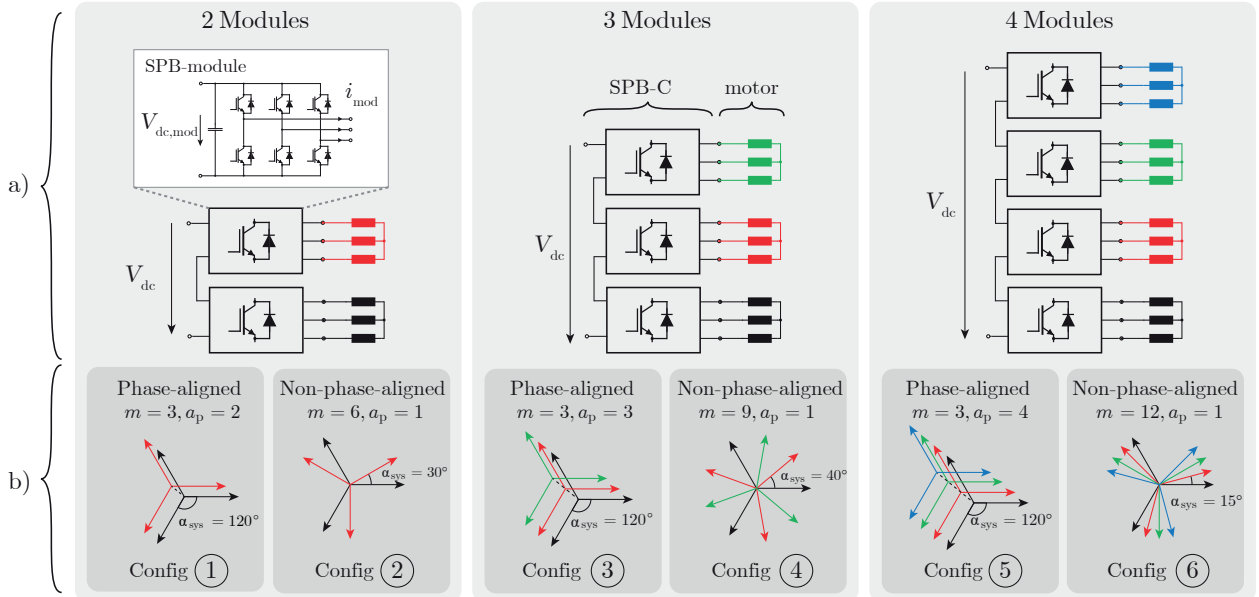


Figure 4.1: a) SPB-C with 2, 3, and 4 SPB-modules connected to motor windings [55]. b) For each SPB-C, two configurations of the magnetic winding axes are shown with m phases and a_{p} phase-aligned winding systems.

motor-converter configurations ①, ③, and ⑤ have phase-aligned three-phase winding systems resulting in 3-phase motors ($m = 3$), whereas configurations ②, ④, and ⑥ have non-aligned three-phase winding systems, resulting in a 6-, a 9-, and a 12-phase motor, respectively ($m = 6/9/12$).
The motivation for considering higher phase numbers is that higher phase numbers result in higher winding factors and consequently in systems with higher power density and/or efficiency as will be shown in this design study which is structured as follows: First, the IMD design procedure developed for this design study is presented in section 4.1.1. This IMD design procedure includes models from chapter 3, as will be specified in that section. Furthermore, the IMD design procedure includes an optimisation of motor dimensions and of electrical motor parameters which is separately explained in section 4.1.2. The results of the IMD design procedure, applied to all system configurations shown in Fig. 4.1 and to exemplary system specifications for a high-torque low-speed IMD, are presented and discussed in section 4.1.3.

4.1.1 Design Procedure

The main goal of this design study is to determine and to compare the system performance of the motor-inverter configurations ① to ⑥ (c.f. Fig. 4.1) in terms of the performance indicators efficiency, power density, and the possible degree of motor-converter modularity as defined in section 3.6.3. A focus is put on the comparison of configurations ① & ②, ③ & ④, and of ⑤ & ⑥ because these pairs have the same amount of semiconductor devices at the same ratings and thus comparable costs.
Fig. 4.2 shows the IMD design procedure *IMD-Design-Proc-1* which is used to determine IMD designs that are pareto-optimal in terms of power density/efficiency (2D optimisation) and that achieve a relatively high degree of motor-converter modularity. The different steps of this design procedure are described in the following, including an indication of the models that were presented in chapter 3 and that are used in the design procedure.
First, to parametrise *IMD-Design-Proc-1*, the system specifications are defined which consist of the rated torque, the rated speed, the DC link voltage, the selected semiconductor devices, and the considered system configuration ①/.../⑥ shown in Fig. 4.1.
For these specifications, a motor is designed in the steps S1 and S2. In

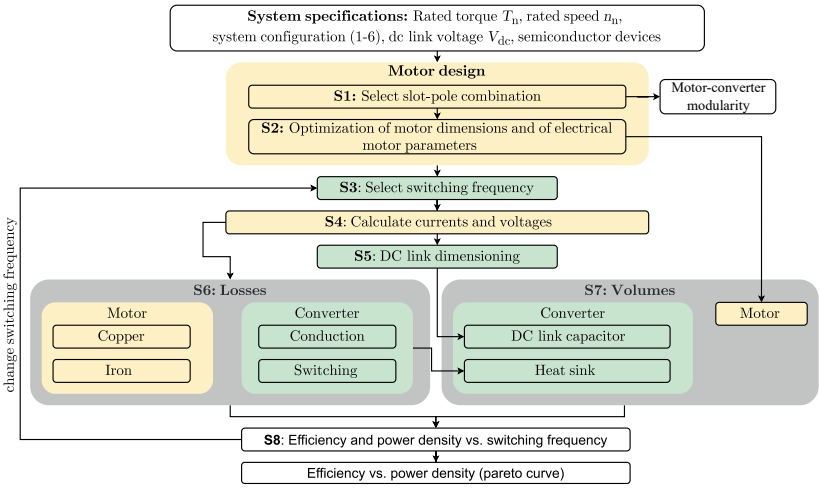


Figure 4.2: *IMD-Design-Proc-1*: Design procedure for an optimised motor-converter system using the SPB-C and a tooth-coil wound PMSM for given system specifications. Design goals: Pareto-optimal efficiency/power density and a high degree of motor-converter modularity. Yellow: Motor modelling and design steps. Green: Converter modelling and design steps.

S1, the number of stator slots and the number of rotor pole pairs are selected based on the criteria for the evaluation of slot-pole combinations which are given in section 3.6.3. This selection already determines the possible motor-converter modularity. In **S2**, the motor dimensions are optimised and electrical motor parameters are calculated using the optimisation routine presented in section 4.1.2.
In the next steps S3-S8, the switching frequency is optimised. For each switching frequency selected in **S3**, the motor/converter currents and voltages are calculated in **S4**. For the voltages, the PWM model for 2L-SPWM from section 3.1 is used. For the currents, the electromechanical motor model from section 3.6.1 is used, where the electrical motor parameters resulting from S2 are inserted.
In **S5**, the DC link is dimensioned using the DC link dimensioning model from section 3.2. There, among the different PWM-schemes and DC link topologies (single-/split-capacitor) considered in section 3.2,

2L-SPWM and the single-capacitor DC link topology are considered in this design study.
In **S6**, the system losses are calculated which include the motor losses and the converter losses. The motor losses include the copper losses in the stator winding and the iron losses in the stator. The copper losses are calculated with the motor winding loss model from section 3.7.1. For the iron loss calculation, a reluctance model is used to estimate the magnetic flux density $\hat{B}$ in the stator teeth and in the yoke elements. Then, the iron losses are calculated in the frequency domain using the Bertotti equation given in (3.143) from section 3.8.1 with $\alpha = 2$. There, the loss coefficients are fitted to loss curves provided by the data sheet of the used electrical steel. The converter/semiconductor losses (conduction and switching) are calculated using the equations (2.12)-(2.13) from [39]. The transistor switching loss energies used therein are derived based on data sheet values and based on the method described in [142].
In **S7**, the IMD/system volume is calculated using IMD volume model 1 from section 3.11.1.
Finally, in **S8**, the system volume and the sum of all losses are used to calculate the system efficiency and power density.

4.1.2 Optimisation of Motor Dimensions and of Electrical Motor Parameters

In this section, step S2 of *IMD-Design-Proc-1* is explained. For the used motor parameters it is referred to the overview of motor parameters of the scalable motor model in Tab. 3.14 from section 3.6.
In this step of *IMD-Design-Proc-1*, the motor length l_m and split ratio χ, as well as the electrical motor parameters R, $L_{\mathrm{dq}k}$, and ψ_{PM1} are determined for each of the system configurations ①-⑥ (cf. Fig. 4.1). The split ratio is defined as the ratio of rotor diameter to outer stator diameter. The following approach is chosen to compare the configurations with regard to power density and efficiency: The three-phase motors (systems ①/③/⑤ in Fig. 4.1) are designed for maximum power density. For the multiphase motors (systems ②/④/⑥ in Fig. 4.1), two variants, "a" and "b", are defined. In variant "a" ($②_\mathrm{a}$/$④_\mathrm{a}$/$⑥_\mathrm{a}$), the multiphase motors are designed for maximum power density. In variant "b" ($②_\mathrm{b}$/$④_\mathrm{b}$/$⑥_\mathrm{b}$), the multiphase motors are designed with the same outer dimensions as the three-phase motors in order to compare

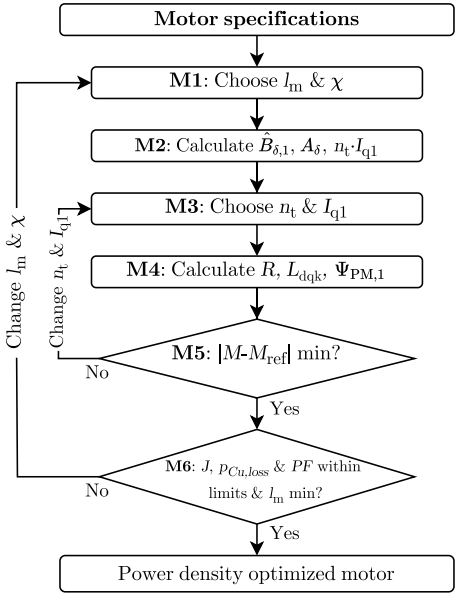


Figure 4.3: Optimisation of the motor length and split ratio for a PMSM with maximum power density and specifications given in Tab. 4.3, 4.7 & 4.4.

the achievable efficiencies when the same volume/power density is imposed.

The motor design routine for maximum power density is illustrated in Fig. 4.3. Therein, first the motor specifications are defined. The motor specifications that are used for all system configurations are summarized in Tab. 4.4. Therein, T_n, n_n, and D are selected based on application requirements. For the constraints (J_max, $p_\mathrm{Cu,loss,max}$ & PF_min) and for the other specifications in Tab. 4.4, reasonable choices are made based on literature [143] in order to limit the calculation effort. For the configuration dependent specifications, given by the DC link voltage and by the slot-pole combination, it is referred to Tab. 4.3 and Tab. 4.7.

After defining the specifications, the design routine starts in **M1** (cf. Fig. 4.3) by selecting values for l_m and χ. In **M2**, $\hat{B}_{\delta,1}$, A_δ, and $n_\mathrm{t} \cdot i_\mathrm{q1}$ are calculated using the Carter factor concept [143] and (3.106), where sinusoidal currents and $B_\mathrm{fe} \leq B_\mathrm{fe,sat}$ (no saturation) are assumed. In

Table 4.1: System specifications used for all system configurations ①-⑥ (cf. Fig. 4.1) in the design procedure (Fig. 4.2).

Rated torque	T_n	(Nm)	50
Rated speed	n_n	(rpm)	300
Heat sink	$CSPI$	($\mathrm{W\,K^{-1}\,dm^{-3}}$)	4.4
Cable inductance	L_c	(µH)	7.5
Min. PCB height	$h_\mathrm{PCB,min}$	(mm)	10
Max. DC link ripple (static)	$\Delta v^*_\mathrm{dc,m,s,max}/V_\mathrm{dc,m}$	(-)	0.02
Max. DC link ripple (dynamic)	$\Delta v^*_\mathrm{dc,m,d,max}/V_\mathrm{dc,m}$	(-)	0.02
Max. load step	$\Delta i_\mathrm{dc,out,max}/I_\mathrm{conv}$	(-)	1
Max. junction temperature	$T_\mathrm{jc,max}$	(°C)	125
Ambient temperature	T_amb	(°C)	55

M3-M5, the number of turns per tooth-coil n_t is determined in an internal iteration ensuring that the modulation index $M := {}^{2\hat{V}_\mathrm{dq1}}/_{V_\mathrm{dc,m}}$ matches the reference value M_ref in steady state, where $\hat{V}_\mathrm{dq1}$ is calculated using (3.104). In each iteration step (**M4**), the electrical model parameters R, $L_\mathrm{dq}k$, and ψ_PM1 are recalculated using (3.109)-(3.111). In **M6**, the constraints are checked and the motor with the minimum length among all valid results is returned. This motor is used for the further design steps S4-S8 of the system design procedure (cf. Fig. 4.2).

4.1.3 Application and Results

In this section, the results of applying the system design procedure in Fig. 4.2 to all system configurations ① to ⑥ (cf. Fig. 4.1) are presented. This section is divided into the following subsections: 1) First, the system specifications are given. 2) Then, the selection of the slot-pole combinations (step S1 in Fig. 4.2) is explained. 3) For the selected slot-pole combinations, the motor dimensions and the electrical motor parameters resulting from step S2 (Fig. 4.2) are given. 4) Finally, the results for the efficiency/power density resulting from the steps S3-S8 (Fig. 4.2) are presented and discussed.

System Specifications

The system specifications used for all system configurations ①-⑥ (cf. Fig. 4.1) are summarized in Tab. 4.1. GaN-HEMTs are used as semi-

Table 4.2: Specifications of the selected transistors (dimensions: $w \times h \times l$).

Transistor	$V_{\mathrm{ds,max}}$(V)	$R_{\mathrm{ds,on}}$(mΩ)	$R_{\mathrm{th,jc}}$(K/W)	w(mm)	l(mm)	h(mm)
IGOT60R070D1	600	70	1	15.9	14.2	3.5
EPC2034C	200	8	0.3	4.6	2.2	0.79

Table 4.3: Considered DC link voltages in V for each system configuration ①-⑥ (cf. Fig. 4.1) and for device blocking voltages of 200 V/600 V.

Config	$V_{\mathrm{ds,max}}$	V_{dc}	$V_{\mathrm{dc,m}}$
① & ②	200	266	133
③ & ④		400	133
⑤ & ⑥		533	133
① & ②	600	800	400
③ & ④		1000	333
⑤ & ⑥		1000	250

conductor devices to achieve low losses. To evaluate the system performance at different DC link voltage levels, device blocking voltages of 200 V and 600 V are considered. Tab. 4.2 lists the specifications of the selected GaN-HEMTs with these blocking voltages and lowest available $R_{\mathrm{ds,on}}$ values. Tab. 4.3 summarizes the DC link voltage V_{dc} and the module DC link voltage $V_{\mathrm{dc,m}}$ for each configuration ① to ⑥.

Table 4.4: Motor specifications used for all system configurations ①-⑥$_{\mathrm{a/b}}$ (cf. section 4.1.2) in the optimisation routine shown in Fig. 4.3.

T_{n}	(Nm)	50	b_{s}	(mm)	3
n_{n}	(rpm)	300	k_{fill}	(-)	0.35
M_{ref}	(-)	0.9	J_{max}	(A mm^{-2})	7
D	(mm)	250	$p_{\mathrm{Cu,loss,max}}$	(kW m^{-2})	1.1
δ	(mm)	1	PF_{min}	(-)	0.9
h_{M}	(mm)	4	Electrical steel	(-)	M330-35a
k_{p}	(-)	0.9	Magnet material	(-)	NdFeB

There, V_{dc} is limited to 1000 V to stay within low-voltage standards. The motor specifications used for step S2 are given in Tab. 4.4.

Selection of Slot-Pole Combinations

Tab. 4.5 & Tab. 4.6 show the comparison of slot-pole combinations based on the criteria described in section 3.6.3 for all configurations ①-⑥, slot numbers $N \in [1, 40]$, and pole pair numbers $p \in [1, 20]$, for single- and for double-layer windings ($n_{\mathrm{l}} = 1,\ 2$). Columns of pole pair numbers p and rows of slot numbers N with only grey entries (not feasible or $k_{\mathrm{w}} < 0.9$) are not shown for the sake of brevity. The rows are ordered in such a way that the results of the configuration pairs ① & ②, ③ & ④, and ⑤ & ⑥ lie next to each other to enable a direct comparison.
From Tab. 4.5 & Tab. 4.6, the following results: In all (N, p)- combinations where both configurations are feasible (marked with a star), the multiphase configuration (②/④/⑥) has a higher winding factor than the 3-phase configuration (①/③/⑤). On average, only considering the relevant/green combinations, the increase in k_{w} is 3.7 %. As expected, only three-phase configurations can reach the highest modularity degree C. In all cases where the multiphase configurations ensure the modularity degree B, the slot-pole combination suffers from unbalanced magnetic pull (orange) or high rotor losses (red). Therefore, combined motor-converter modularity is practically not feasible for multiphase motors with the considered slot-pole combinations. Furthermore, there are significantly less feasible slot-pole combinations for single-layer than for double-layer windings. This is due to condition C1a given in (3.113) that requires an even number of stator slots N for single-layer windings.
For the next design steps, only double-layer windings are considered and one recommended (green) slot-pole combination is chosen for each configuration ①-⑥. The selected combinations are summarized in Tab. 4.7.

Table 4.5: Winding factor k_w and degree of modularity (A/B/C) (cf. Fig. 3.20) of double-layer tooth-coil windings for slot-pole combinations with $N \in [1, 40]$, $p \in [1, 20]$, and system configurations ①-⑥ (cf. Fig. 4.1). Other criteria of Tab. 3.15 are colour-coded.

Double layer windings															
	p	4	5	7	8	10	11	12	13	14	15	16	17	19	20
N	Config	Configurations ① & ②													
12	①		0.933-C	0.933-C									0.933-C	0.933-C	
	②		0.966-A	0.966-A									0.966-A	0.966-A	
18	①			0.902-A	0.945-C	0.945-C	0.902-A								
	②														
24	①					0.933-A	0.949-C		0.949-C	0.933-A					
	②					0.966-A	0.983-A		0.983-A	0.966-A					
30	①								0.936-A	0.951-C		0.951-C	0.936-A		
	②														
36	①									0.902-A	0.933-A	0.945-A	0.953-C	0.953-C	0.945-A
	②										0.966-A		0.986-A	0.986-A	
		Configurations ③ & ④													
9	③														
	④	0.985-B	0.985-B						0.985-B	0.985-B					
18	③														
	④			0.940-A	0.985-A	0.985-A	0.940-A								
27	③							0.945-C			0.945-C				
	④					0.914-A	0.954-A	0.985-A	0.994-B	0.994-B	0.985-A	0.954-A	0.914-A		
36	③										0.933-A				
	④								0.903-A	0.940-A		0.985-A	0.992-A	0.992-A	0.985-A
		Configurations ⑤ & ⑥													
24	⑤					0.933-C				0.933-C					
	⑥						0.991-A		0.991-A						
36	⑤									0.902-A		0.945-C			0.945-C
	⑥														
Colorlegend															
		C1-C5 fulfilled		gcd(N_l, 2p) == 1		$p_{r,loss} > 100$		Not feasible		$k_w < 0.9$					

Table 4.6: Winding factor k_w and degree of modularity (A/B/C) (cf. Fig. 3.20) of single-layer tooth-coil windings for slot-pole combinations with $N \in [1, 40]$, $p \in [1, 20]$, and system configurations ①-⑥ (cf. Fig. 4.1). Other criteria of Tab. 3.15 are colour-coded.

Single layer windings															
	p	4	5	7	8	10	11	12	13	14	15	16	17	19	20
N	Config	Configurations ① & ②													
12	①		0.966-C	0.966-C									0.966-C	0.966-C	
	②														
24	①					0.966-A	0.958-C		0.958-C	0.966-A					
	②						0.991-A		0.991-A						
36	①									0.902-A	0.966-A	0.945-A	0.956-C	0.956-C	0.945-A
	②														
		Configurations ③ & ④													
18	③														
	④			0.940-B	0.985-B	0.985-B	0.940-B								
36	③										0.966-A				
	④								0.906-A	0.940-A		0.985-A	0.996-A	0.996-A	0.985-A
		Configurations ⑤ & ⑥													
24	⑤					0.966-C				0.966-C					
	⑥														
Colorlegend															
		C1-C5 fulfilled		gcd$(N_l, 2p) == 1$		$p_{r,loss} > 100$		Not feasible		$k_w < 0.9$					

Table 4.7: Selected slot-pole combinations for system configurations ①-⑥ (cf. Fig. 4.1).

Configuration	①	②	③	④	⑤	⑥
N	36	36	27	27	24	24
p	17	17	12	12	10	11
m	3	6	3	9	3	12
k_w	0.953	0.986	0.945	0.985	0.933	0.991

Motor Dimensions and Electrical Motor Parameters

The motor length and the electrical motor parameters resulting from step S2 of the system design procedure (Fig. 4.2) are summarized in Tab. 4.8, for all system configurations ①-⑥$_{\mathrm{a/b}}$ (cf. section 4.1.2). As explained in section 4.1.2, the multiphase motors of variant "b" are derived by choosing the same dimensions as those of the three-phase motors, i.e. l_m and χ are fixed for system configurations ②$_\mathrm{b}$, ④$_\mathrm{b}$, and ⑥$_\mathrm{b}$ in the optimisation routine shown in Fig. 4.3.
The motor parameters in Tab. 4.8 are used in the switching frequency optimisation (S3-S8 in Fig. 4.2), the results of which are presented in the following section.

Table 4.8: Electrical motor parameters (R, $L_{\mathrm{dq}k}$ & ψ_{PM1}), rated motor current for one SPB-module (I_mod), and motor length (l_m) resulting from the design routine in Fig. 4.3 for system configurations ①-⑥$_{\mathrm{a/b}}$ (cf. section 4.1.2) and $V_{\mathrm{ds,max}} = 600\,\mathrm{V}$.

Configuration		①	②$_\mathrm{a}$	②$_\mathrm{b}$	③	④$_\mathrm{a}$	④$_\mathrm{b}$	⑤	⑥$_\mathrm{a}$	⑥$_\mathrm{b}$
R	(Ω)	2.05	3.99	3.86	1.41	4.07	3.92	0.82	3.06	2.78
L_{dq1}	(mH)	20.4	41.2	40.3	20.0	60.6	62.0	12.5	49.9	51.0
L_{dq5}	(mH)	-	32.1	31.4	-	36.3	36.8	-	38.0	38.5
L_{dq7}	(mH)	-	-	-	-	23.4	23.4	-	29.2	29.3
L_{dq11}	(mH)	-	-	-	-	-	-	-	17.3	16.8
ψ_{PM1}	(mWb)	280	279	281	328	328	330	301	269	269
I_mod	(A)	2.47	2.48	2.47	2.00	2.00	1.99	1.96	1.99	1.99
l_m	(mm)	54	52	54	56	54	56	58	54	58

Efficiency vs. Power Density

Fig. 4.4 shows the resulting power densities and efficiencies of all considered system configurations for switching frequencies between 1 kHz and 100 kHz where each graph compares one of the 3-phase configurations ①, ③ or ⑤ to its corresponding multiphase configuration $②_{a/b}$, $④_{a/b}$ or $⑥_{a/b}$ (cf. 4.1.2). As expected, all configurations show a similar dependency on the switching frequency. At low switching frequencies f_{PWM}, large capacitance values are required to limit the voltage ripple on the DC link, leading to non-optimal power densities. Also, the efficiency is not maximum for small values of f_{PWM} as could be expected from common pareto curves. This is due to the motor inductance that is held constant in the applied design procedure (Fig. 4.2) which leads to a high current ripple and high harmonic losses in the motor for low switching frequencies. Increasing the switching frequency increases the motor efficiency but decreases the converter efficiency due to the switching losses. Also, the required capacitor volume is reduced but the heat sink volume to dissipate more switching losses increases. The curve shape near the point of maximum power density (marked with a star) is relatively abrupt for the 2-module configurations and becomes smoother with increasing amount of SPB-modules. This is due to the capacitance limit $C_{dc,min,d} \sim 1/N_m$ (cf. (3.77)) that is reached earlier (i.e. for smaller f_{PWM}) for a small number of modules compared to a large number of modules. Overall, Fig. 4.4 shows that multiphase configurations on average enable an increase of 0.70 % in maximum efficiency or an increase of 3.8 % in maximum power density compared to 3-phase configurations.

4.1.4 Conclusion

In this design study, the SPB-C combined with a 3-, 6-, 9-, or 12-phase tooth-coil wound non-salient PMSM is analysed and compared with respect to efficiency and power density based on a comprehensive system optimisation. The results show that the winding factors of the proposed 6-, 9-, and 12-phase (multiphase) motors are on average 3.7 % higher than the winding factors of 3-phase motors with 2, 3, or 4 phase-aligned winding systems. The higher winding factor can be used to increase the maximum efficiency by 0.70 % or the maximum power density by 3.8 %. Furthermore, the possible motor-converter modularity is analysed. As a result, 3-phase motors allow a higher degree of motor-converter mod-

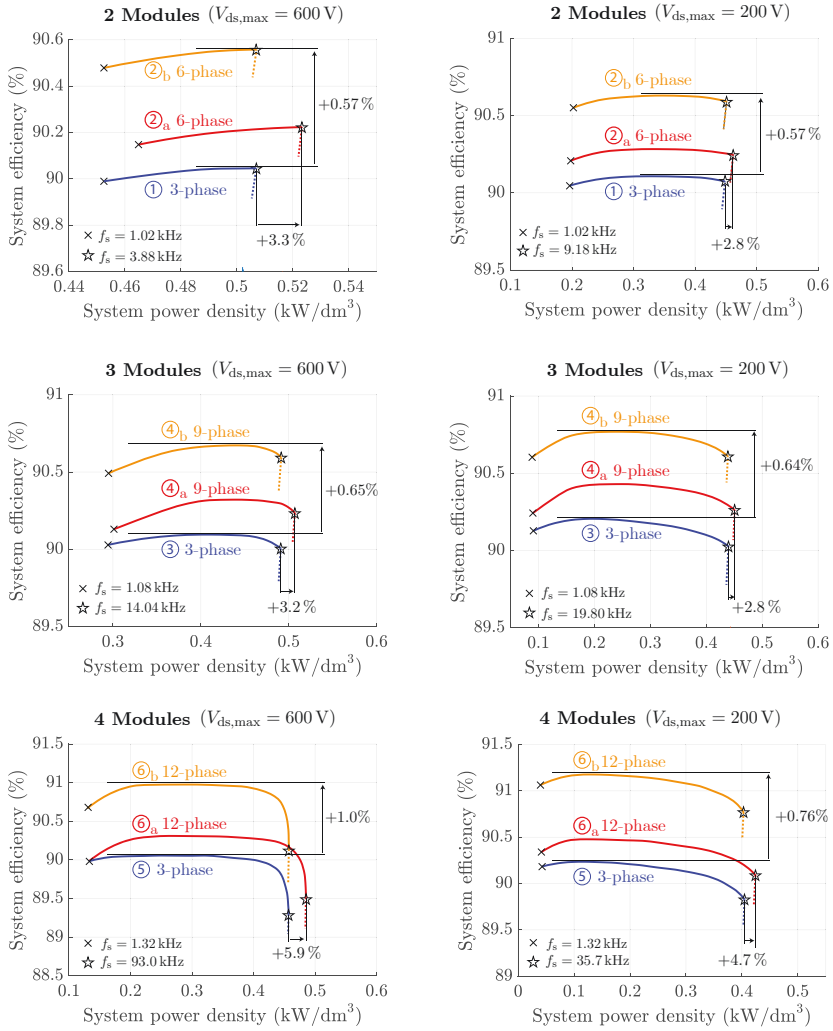


Figure 4.4: System efficiency and power density of the 3-phase and of the multiphase system configurations ① – ⑥$_{a/b}$ (cf. section 4.1.2) for transistor blocking voltages $V_{ds,max}$ = 600 V/200 V and switching frequencies f_{PWM} = 1..100 kHz. Considered losses: Motor copper and stator core losses, converter switching and conduction losses. Considered volumes: Motor, populated PCB, and heat sink.

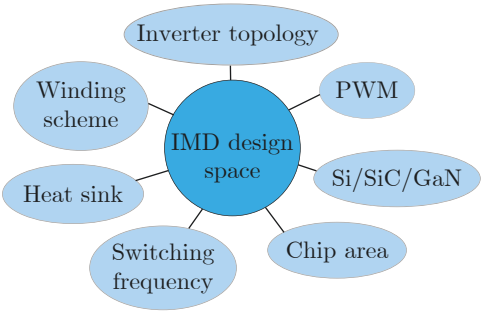


Figure 4.5: Design space considered for the optimal design of IMDs.

ularity compared to multiphase motors.

4.2 Optimal Design and Comparison of IMDs using different Topologies, PWM Variants, and Switch Technologies

In this section, a design study on the optimal design and comparison of IMDs using different topologies (2L/3L/modular), PWM variants, and switch technologies (Si/SiC/GaN) is presented.
Existing literature already covers several topology comparisons for inverters in general [55, 56, 144], and for IMDs in particular [2, 59, 145]. According to [2], modular topologies are advantageous due to their potential for higher fault-tolerance, smaller size, and lower cost. In [145], the focus is on different topologies for the rectifier whereas for the inverter always the same 2L-topology is considered and the motor has a 3-phase winding. However, [145] considers neither different topologies for the inverter, nor multiphase motor windings. In addition, a comprehensive design procedure that enables a holistic comparison of modular inverter topologies and standard 2L- and 3L-topologies is missing. A limited approach of such a comparison is given by [59], wherein standard 2L- and 3L- inverter topologies are compared to different modular inverter topologies such as a *2L-2S-VSI* (series connection of two 2L-modules) or a *3L-2P-VSI* (parallel connection of two 3L-modules). However, the approach in [59] is limited because the chip area/size is

not optimised and the analysis only focuses on efficiency, i.e. power density and cost are not included in the comparison.
To fill this gap, a design procedure for a holistic comparison of modular converter topologies and standard 2L- and 3L-topologies is presented in this thesis through this design study. In this context, "holistic" means that multiple design goals (power density/efficiency/cost/reliability) and a relatively large set of topology-related design parameters is considered. An overview of the considered design parameters (i.e. the design space), is shown in Fig. 4.5. Therein, the variable *winding scheme* indicates that also multiphase motors are considered.
In the following, first the proposed design procedure is presented in section 4.2.1. This includes references to models from chapter 3 which are used in this design procedure. In section 4.2.2, the results of applying the design procedure to an exemplary system specification of a 1.5 kW high-torque, low-speed IMD are presented and discussed. The reliability of the considered converter topologies is analysed and compared separately in section 4.2.3.

4.2.1 Design Procedure

Fig. 4.6 shows the proposed procedure, called *IMD-Design-Proc-2*, for the IMD design for a fix DC link voltage and a given PMSM which is variable in the winding scheme and in the number of turns of the stator winding. The underlying thermo-mechanical integration concept is that of an axially integrated IMD (Fig. 3.43). In the following, the design setup and the different steps of the design procedure are explained.

Design Setup - Specification, Constraints, and Design Space

To set up the design procedure in Fig. 4.6 the system specification, the design constraints, and the design space must be parametrised. The system specification comprises the DC link specification, the motor specification, and the ambient temperatures (air/flange). The design constraints for the different parameters are determined by the selected motor, the semiconductor devices, the capacitor series, the electronics temperature rating, and the thermal insulation layer.
The overall design space is split into structural degrees of freedom and operational degrees of freedom (DOFs). The structural DOFs in Fig. 4.6 define the basic system configuration, i.e. they describe a combination of an inverter topology, a PWM scheme, a semiconductor technol-

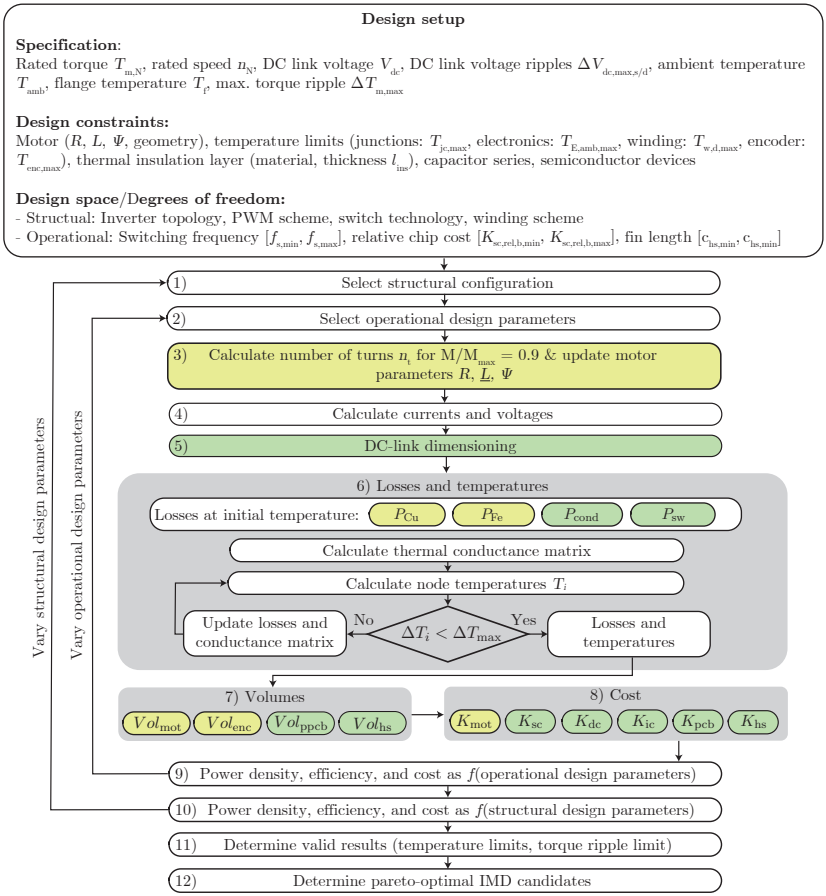


Figure 4.6: *IMD-Design-Proc-2*: Procedure for the optimal design of an IMD in terms of power density, efficiency, and cost. Yellow: Parts related to motor modelling. Green: Parts related to converter modelling.

ogy, and a winding scheme. The considered system configurations are summarized in Tab. 4.9. The procedure could be extended to other configurations as well.
The considered topologies correspond to all topologies that were selected in section 2.2.2 (Fig. 2.19). This includes standard non-modular

Table 4.9: Considered system configurations. In case a certain *PWM*-/*SC*-/*W*-variant is only combined with particular topologies, these topologies are indicated in parenthesis.

Topology *Top*	Modulation scheme *PWM*	Semiconductor technology *SC*	Winding scheme *W*
1: 2L	1: Sin-PWM (2L/3L)	1: Si	1: 3-phase ($Top = 1/2/3$)
2: 3L-NPC	2: OC-PWM ($Top = 1/4/5$)	2: SiC	2: 9-phase ($Top = 4/5$)
3: 3L-TT	3: NPB-PWM ($Top = 2/3$)	3: GaN	
4: 2L-3M-ser			
5: 2L-3M-par			

topologies (2L, 3L-NPC, 3L-TT) and modular topologies (2L-3M-ser, 2L-3M-par).
As PWM schemes, all PWM schemes that were selected in section 2.3.2 are considered. This includes standard Sinus PWM (2L/3L-SPWM) and advanced schemes such as Optimal Clamped-PWM (2L-OCPWM) and Neutral Point Balanced-PWM (3L-NPBPWM).
Regarding semiconductor technologies, Si IGBTs, SiC MOSFETs, and GaN HEMTs are considered with an overall voltage blocking capability of 1200 V for DC link voltages up to 800 V.
Concerning the winding scheme, non-modular topologies are combined with a standard 3-phase winding ($m = N_{\mathrm{ph}} = 3$) and modular topologies are combined with a symmetrical 9-phase winding ($m = N_{\mathrm{ph}} = 9$, all winding axes displaced by an angle of $2\pi/9$). This winding scheme is chosen, because for the same topology, it is already known to perform better than phase-aligned 3x3-phase windings ($m = 3$, $N_{\mathrm{ph}} = 9$) due to a higher winding factor, as shown in the previous design study in section 4.1.
The operational DOFs in Fig. 4.6 are design parameters that are linked to the relevant trade-offs in the design goals (system power density ρ_{sys}, system efficiency η_{sys}, system cost K_{sys}). These trade-offs are:

1. With increasing switching frequency the switching losses increase, but harmonic motor losses and the torque ripple are decreased in the standard case of 3-phase motors. With multiphase-motors like 9-phase motors, the switching frequency also affects the harmonic motor losses and the torque ripple but the dependency is more complex due to the fact that multiphase motors have multiple inductances for different harmonic sequences.

2. Increasing the heat sink size decreases the power density, but increases efficiency due to the temperature dependence of the conduction losses ($R_{\mathrm{ds,on}}$) and the motor losses.

3. Increasing the chip area/chip cost decreases conduction losses, but increases the system cost. Depending on the $E_{\mathrm{on}}(I)/E_{\mathrm{off}}(I)$-curves, increasing the chip area/chip cost can furthermore increase switching losses due to the larger parasitic capacitances that have to be charged/discharged during switching.

The relative chip cost $K_{\mathrm{sc,rel,b}} := {}^{K_{\mathrm{sc}}}/_{K_{\mathrm{sc,b}}}$ is used as an indicator for the chip area, where $K_{\mathrm{sc,b}}$ is a chip cost budget that is constant for all system configurations to ensure a fair comparison.

Calculation Steps of the Design Procedure

The procedure in Fig. 4.6 starts in **step 1)** with an outer loop (brute force) over the structural DOFs and continues, in **step 2)**, with an inner loop over the operational DOFs.
In each iteration, which starts in **step 3)**, the number of turns n_{t} is adapted to a relative modulation index M/M_{max} of 90 % based on basic motor theory ([74]) to achieve a good DC link utilization with 10 % margin for the control. In step 3) also the electrical motor model parameters given by the resistance R, the inductance matrix $\underline{L}$, and the PM flux linkage Ψ are calculated using (3.109)-(3.111) from section 3.6.2.
In **step 4)**, these motor parameters and the modulation index are used to calculate the switched currents and voltages. For the voltages, the PWM model from section 3.1 is used. For the currents, the electromechanical motor model from section 3.6.1 is used. In step 4), also the torque ripple is calculated using (3.107)-(3.108) from section 3.6.1.
In **step 5)**, the DC link capacitors are dimensioned using the model described in section 3.2. There, the split-capacitor DC link topology (Fig. 3.8b) is considered for the 2L-based topologies (2L, 2L-3M-ser, 2L-3M-par).
In **step 6)**, first the considered system loss components are calculated for an arbitrary initial temperature. These system loss components include the motor copper losses P_{Cu}, the motor iron losses P_{Fe}, the semiconductor conduction losses P_{cond}, and the semiconductor switching losses P_{sw}.
For the motor copper losses, the winding loss model from section 3.7.2 is used which takes the skin effect and the proximity effect into account.

For the iron losses, the iron loss density model GMLSE5+BPG from section 3.8.3 is used in combination with a linear reluctance model of the motor.
For the semiconductor conduction losses, the conduction loss model from section 3.3 is used which includes a scaling of $R_{\mathrm{ds,on}}$ with the chip cost. For the semiconductor switching losses, the model from section 3.4 is used.
The resulting losses (copper, iron, conduction, switching) at an initial temperature are used as input parameters of the thermal IMD model from section 3.9. This model includes an iterative procedure that results in the temperature distribution in the IMD and in the temperature dependent loss components, i.e. the motor copper losses and the semiconductor conduction losses.
In **step 7)**, the IMD system volume is calculated using IMD volume model 2 from section 3.11.2. There, the most relevant parts of the system volume are given by the motor volume Vol_{mot}, the volume of the populated PCB Vol_{ppcb}, the heat sink volume Vol_{hs}, and the encoder box volume Vol_{enc}.
In **step 8)**, the system costs are calculated using the cost model from section 3.12. This model includes the motor cost K_{mot}, the power semiconductor cost K_{sc}, the DC link capacitor cost K_{dc}, the auxiliary IC cost K_{ic}, the PCB cost K_{pcb}, and the heat sink cost K_{hs}.
In **step 9)-10)**, the system power density, the system efficiency, and the system costs are saved as a function of the operational and of the structural design parameters which are then updated for the next design loop starting in step 1)/step 2) until the complete design space is analysed.
In **step 11)**, the valid results are determined which must fulfil the temperature limits and the torque ripple limit defined in the design setup. Finally, the pareto-optimal designs are determined from the set of valid designs in **step 12)**.

4.2.2 Application of the Design Procedure

In this section, the application of the design procedure in Fig. 4.6 to the optimisation of a 1.5 kW IMD is presented. This section is divided into the following parts: 1) First, the design setup is given. 2) Then, in a first part on the results of the design procedure, the pareto-optimal designs are investigated. 3) In a second part on the results of the design

Table 4.10: System specifications and design constraints of a general-purpose, high-torque, low-speed IMD.

Rated power P_n	1.5 kW
Rated torque T_n	48 Nm
Rated speed n_n	300 rpm
DC link voltage V_dc	800 V
Max. static DC link voltage ripple $\Delta v^*_{\mathrm{dc,s,max}}/V_\mathrm{dc}$	0.01
Max. dynamic DC link voltage ripple $\Delta v^*_{\mathrm{dc,d,max}}/V_\mathrm{dc}$	0.125
Max. load step $\Delta i_{\mathrm{dc,out,max}}/I_\mathrm{conv}$	1
Ambient temperature T_amb	40 °C
Flange temperature T_f	65 °C
Max. junction temperature $T_\mathrm{jc,max}$	125 °C/150 °C
Max. electronics ambient temperature $T_\mathrm{e,amb,max}$	80 °C
Max. winding temperature $T_\mathrm{w,max}$	130 °C
Max. encoder temperature $T_\mathrm{enc,max}$	80 °C
Max. torque ripple $\Delta T_\mathrm{m,max}$	0.5 Nm
Min. PCB height $h_\mathrm{PCB,min}$	15 mm
Insulation layer thickness l_ins	0 mm
Semiconductor cost budget $K_\mathrm{sc,b}$	190.2 CHF

Table 4.11: Design space limits for the operational DOFs in Fig. 4.6.

Switching frequency f_s	1 kHz ... 100 kHz
Relative semiconductor cost $K_\mathrm{sc,rel,b}$	0 ... 1
Heat sink fin length c_hs	0 mm ... 30 mm

procedure, the considered semiconductor technologies, PWM schemes, and topologies are compared with regard to the maximum system efficiency at approximately equal system cost and volume.

Design Setup - Specifications, Constraints, and Design Space

The considered system specification, design constraints, and the design space limits of the operational DOFs are summarized in Tab. 4.10 & 4.11. For the sake of brevity, Tab. 4.10 does not include the detailed geometric and thermal motor specifications that are required for the thermal IMD model (Tab. 3.29-3.38), but is limited to the most im-

Table 4.12: Benchmark system parameters.

System configuration $\{Top\text{-}PWM\text{-}SC\text{-}W\}$	2L-Sin-Si-3ph
Switching frequency f_s	26.28 kHz
Relative semiconductor cost $K_\mathrm{sc,rel,b}$	0.0764
Heat sink fin length c_hs	1 mm
System power density $\rho_\mathrm{sys,ref}$	0.1291 kW L^{-1}
System efficiency $\eta_\mathrm{sys,ref}$	86.05 %
System cost $K_\mathrm{sys,ref}$	190.45 CHF
Motor cost K_mot	138.18 CHF

Table 4.13: Reference power semiconductor devices, selected as the devices with the largest current rating within each device series with the same package dimensions. Given parameters: Rated current I_r, cost parameters a_sc & b_sc, and maximum junction temperature $T_\mathrm{jc,max}$. As the switching energies $E_\mathrm{on/off}$ of the 1200V GaN HEMT are not provided in literature, it is assumed that these scale with $V_\mathrm{ds,max}$ like the switching energies of SiC MOSFETs, i.e. $E_\mathrm{on/off,T6} = E_\mathrm{on/off,T3} \cdot (E_\mathrm{on/off,T5}/E_\mathrm{on/off,T2})$.

ID	Device type/ Name	I_r (A)	a_sc (CHF/A)	b_sc (CHF)	$T_\mathrm{jc,max}$ (°C)	Source of $E_\mathrm{on/off}$
T1	600 V Si IGBT/ IKP20N60T	41	0.0443	1.097	175	Datasheet
T2	600 V SiC MOSFET/ IMZA65R027M1H	59	0.2016	2.22	150	Application note [146]
T3	600 V GaN HEMT/ GS66508T	30	0.7976	2.083	150	Datasheet
T4	1200 V Si IGBT/ IKW40T120	75	0.0802	2 .026	150	Datasheet
T5	1200 V SiC MOSFET/ IMBG120R030M1H	56	0.2063	2.778	175	Datasheet
T6	1200 V GaN HEMT/ GPIHV30DFN	30	0.7976	3.083	150	Assumption
D1	600 V SiC Diode/ IDDD20G65C6	51	0.2073	0.4457	175	-

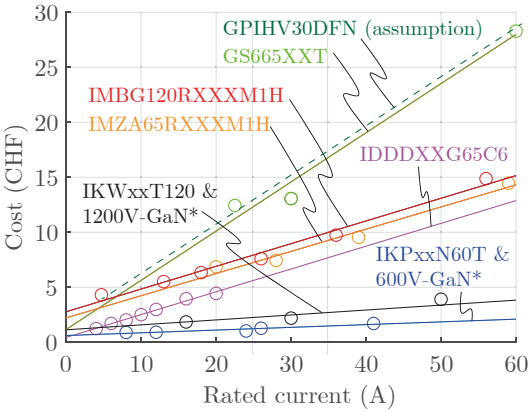


Figure 4.7: Chip cost as a function of rated current/chip size based on distributor prices for an order volume of 1000 pieces.

portant specifications. The parameters of the benchmark system used for the definition of the relative system cost $K_{\mathrm{sys,rel}} := {}^{K_{\mathrm{sys}}}/_{K_{\mathrm{sys,ref}}}$ are given in Tab. 4.12.

Tab. 4.13 shows the selected reference power semiconductor devices and the cost parameters obtained from a cost study of the corresponding device series. The results of this cost study are shown in Fig. 4.7, indicating that the considered WGB devices (SiC/GaN) are 5 to 10 times more expensive than conventional Si IGBTs of the same current rating. However, as the production of GaN devices is based on silicon substrate, the cost of GaN is expected to reach the level of Si devices in the long run. Therefore, GaN HEMTs are considered in two "cost versions": 1) Based on present costs, denoted as GaN, and 2) with future costs which are assumed to be equal to the costs of Si IGBTs as indicated in Fig. 4.7. These devices are denoted as GaN* in the following.

The iron loss density model (GMLSE5+BPG) is parametrised with the parameters given in Fig. 3.36 from section 3.8.3. These parameters were determined based on iron loss density measurements with samples of the silicon steel M330-35a.

The parameters used for the semiconductor loss models are shown in Fig. 4.8a-d. Therein, Fig. 4.8a & b show the switching energies of the reference devices which decrease from Si IGBTs to SiC MOS-

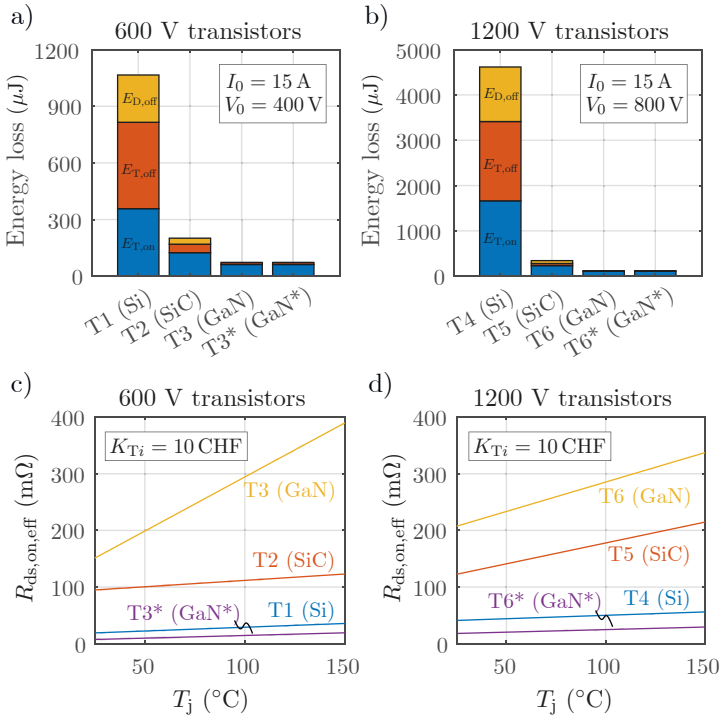


Figure 4.8: a) & b) Switching loss energies of the reference devices from Tab. 4.13, based on the scaling of one $E_x(I)$-value pair from the datasheet/application note which is scaled to the switched current I_0 and voltage V_0. c) & d) Effective on-state resistance of the reference devices over the junction temperature, scaled to the same cost per device $K_{T,i}$. The values in a)-d) are used to parametrize the semiconductor conduction/switching loss model.

FETs to GaN/GaN* HEMTs, as expected. Compared to MOSFETs and HEMTs, IGBTs have an on-state resistance with a strong dependency on the current. Therefore, in order to compare the conduction loss behaviour of MOSFETs, HEMTs, and IGBTs on the device level, an effective on-state resistance $R_{ds,on,eff}$ is defined as the on-state resistance at a typical operating current which is assumed to be equal to 1/3 of the rated current. Fig. 4.8c & d show that, for the same cost per

transistor, the static losses increase from GaN* HEMTs to Si IGBTs to SiC MOSFETs to GaN HEMTs. The fact that the effective on-state resistance of GaN* HEMTs (i.e. GaN HEMTs with future expected costs) is lower than the one of the considered Si IGBTs is due to the following two reasons: 1) As previously mentioned, it is assumed that, for the same cost per device, GaN* HEMTs have the same rated current as the considered Si IGBTs (Fig. 4.7). 2) Due to that assumption, the effective on-state resistance of the reference devices is scaled to the same rated current (using $R_{\mathrm{ds,on}} \propto {}^{1}/_{I_{\mathrm{r}}}$), for which the considered GaN HEMTs have a lower $R_{\mathrm{ds,on,eff}}$ than the Si IGBTs.

Investigation of the Pareto-Optimal Designs

Fig. 4.9a shows the pareto-front of the pareto-optimal IMD designs in the $(\rho_{\mathrm{sys}}, \eta_{\mathrm{sys}}, K_{\mathrm{sys,rel}})$-space resulting from the design procedure in Fig. 4.6, where only the present costs of semiconductor technologies Si/SiC/GaN are considered, i.e. GaN* is not considered. Fig. 4.9a, shows six pareto-optimal $\{$*Top-PWM-SC-W*$\}$-configurations (i.e. system configurations in terms of the topology, the PWM scheme, the semiconductor technology, and the winding scheme). These configurations are colour-coded by means of the coloured configuration names in Fig. 4.9a & b. The overall optimal/best configuration depends on how the design objectives $(\rho_{\mathrm{sys}}, \eta_{\mathrm{sys}}, K_{\mathrm{sys,rel}})$ are weighted. This is shown in Fig. 4.9b which displays the colour of the configuration that minimizes the scalar cost function $f_{\mathrm{s}} = w_\rho({}^{-\rho_{\mathrm{sys}}}/_{\rho_{\mathrm{sys,ref}}}) + w_\eta({}^{-\eta_{\mathrm{sys}}}/_{\eta_{\mathrm{sys,ref}}}) + w_K({}^{K_{\mathrm{sys}}}/_{K_{\mathrm{sys,ref}}})$, as a function of the weighting factors w_ρ & w_η with the constraint $w_\rho + w_\eta + w_K = 1$. To illustrate how to read Fig. 4.9b, an exemplary point at $w_\rho = 0.1$, $w_\eta = 0.2$, and $w_K = 1 - (w_\rho + w_\eta) = 0.7$ is indicated in Fig. 4.9b. The colour at that point belongs to the configuration *2L-OC-Si-3ph*, indicating that this is the overall optimal configuration for the weighting factors at the considered exemplary point. Fig. 4.9a & b show that the cost-optimal system configuration is *2L-OC-Si-3ph*, the most efficient configuration is *2L3Mpar-OC-GaN-9ph*, and the highest power density is reached by all configurations (in the case of no cooling fins). For a compromise between costs and efficiency, the least expensive IMD of the most efficient system configuration, i.e. of the configuration *2L3Mpar-OC-GaN-9ph*, is suggested as the overall optimal IMD (IMD_{sg} in Fig. 4.9a). Fig. 4.9a shows that the suggested IMD enables an efficiency increase of +2.26 % (i.e. percentage points) at the expense of 36 % higher costs compared to the cost-optimal IMD

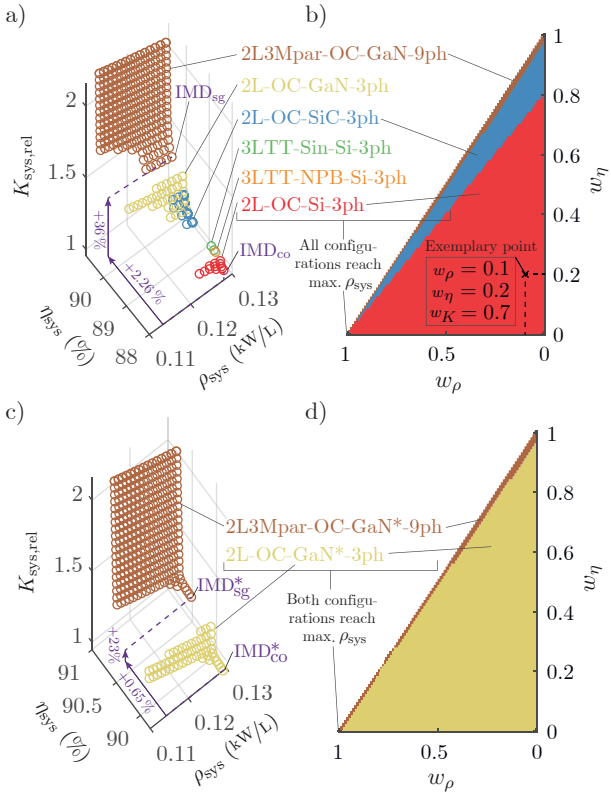


Figure 4.9: a) Pareto-front of the pareto-optimal IMD designs resulting from the design procedure in Fig. 4.6 and from the system specification in Tab. 4.10, considering present semiconductor prices (i.e. Si/SiC/GaN). b) Overall optimal system configuration as a function of the weighting factors w_ρ & w_η of the cost-function $f_s = w_\rho(-\rho_{sys}/\rho_{sys,ref}) + w_\eta(-\eta_{sys}/\eta_{sys,ref}) + w_K(K_{sys}/K_{sys,ref})$ with $w_K = 1-(w_\rho + w_\eta)$. c) & d) Analogue results to a) & b), considering expected future GaN prices (i.e. Si/SiC/GaN*).

(IMD_{co} in Fig. 4.9a).
The same analysis is performed now including the future expectation of GaN HEMT costs (GaN*). The result is shown in Fig. 4.9c & d, indicating that only two GaN*-based system configurations are on the

pareto-front. Hence, for the considered specification, GaN HEMTs are expected to outperform Si IGBTs and SiC MOSFETs in the future. As shown in Fig. 4.9c & d, the cost-optimal configuration is now *2L-OC-GaN*-3ph* and the most efficient configuration is *2L3Mpar-OC-GaN*-9ph*. The suggested IMD (IMD^*_{sg} in Fig. 4.9c) now enables 0.65 % more efficiency for 23 % more costs, compared to the future expected cost-optimal IMD (IMD^*_{co} in Fig. 4.9c).

Comparison at Equal Cost and Volume

While the previous analysis revealed the best system configurations for the given system specification, in a next step, the impact of the different semiconductor technologies, PWM schemes, and topologies on the system performance is investigated. For that purpose, all system configurations defined in Tab. 4.9 are compared with regard to maximum system efficiency/minimum system losses $P_{\mathrm{sys,loss,opt}}$ at approximately equal system cost $K_{\mathrm{sys,rel}} = 1.8 \pm 0.03$ and approximately equal system volume $Vol_{\mathrm{sys}} = 12.89\,\mathrm{L} \pm 0.17\,\mathrm{L}$. These intervals for $K_{\mathrm{sys,rel}}$ & Vol_{sys} are chosen so that all considered system configurations can be compared. In other intervals some configurations might not have a solution because the ranges of $K_{\mathrm{sys,rel}}$ & Vol_{sys} are different for each configuration.

Fig. 4.10 shows the resulting cost distribution, volume distribution, and optimal power loss distribution as bar plots, as well as a table listing the corresponding optimal design parameters ($f_{\mathrm{sw,opt}}$, $K_{\mathrm{sc,rel,b,opt}}$, $c_{\mathrm{hs,opt}}$), the efficiency gain compared to the reference system (Tab. 4.12), and the optimum type (*opttype*). The optimum type indicates what determines the optimal design parameters as explained in the following. The optimal semiconductor costs $K_{\mathrm{sc,rel,b,opt}}$ and the optimal cooling fin length $c_{\mathrm{hs,opt}}$ are determined by the upper limits of the already mentioned cost and volume intervals for all considered system configurations. However, different cases are identified for the optimal switching frequency $f_{\mathrm{sw,opt}}$: For $opttype = 1$, $f_{\mathrm{sw,opt}}$ results from an optimal balance between the switching losses and the harmonic motor losses. That is, for switching frequencies lower than $f_{\mathrm{sw,opt}}$, the harmonic motor losses increase faster than the switching losses decrease, so that the system efficiency decreases. For $opttype = 2$, $f_{\mathrm{sw,opt}}$ lies on the boundary defined by the torque ripple constraint $\Delta T_{\mathrm{m}} < \Delta T_{\mathrm{m,max}}$. That is, for switching frequencies lower than $f_{\mathrm{sw,opt}}$, the torque ripple exceeds $T_{\mathrm{m,max}}$. For $opttype = 3$, $f_{\mathrm{sw,opt}}$ lies on the boundary defined by the

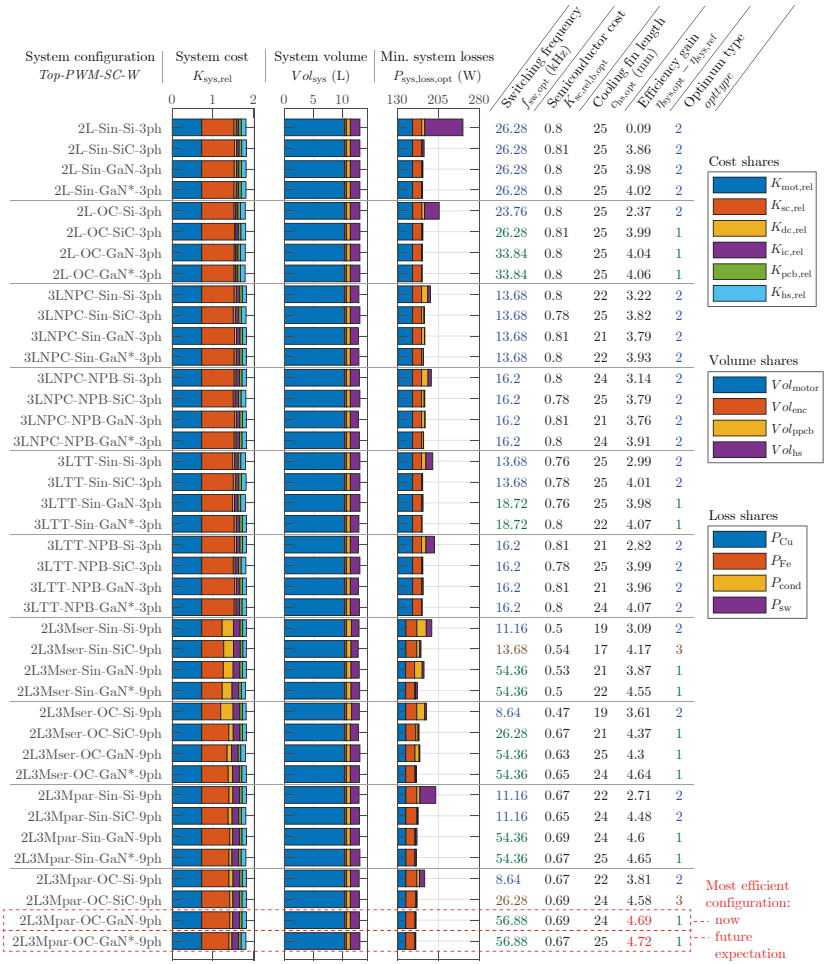


Figure 4.10: System performance resulting from the design procedure in Fig. 4.6 at approximately equal system cost $K_{\mathrm{sys,rel}}$, volume Vol_{sys}, and minimized losses $P_{\mathrm{sys,loss,opt}}$ for all system configurations defined in Tab. 4.9. Bar plots: Distribution of system cost, volume, and losses. Table on the right: Optimal design parameters ($f_{\mathrm{sw,opt}}$, $K_{\mathrm{sc,rel,b,opt}}$, $c_{\mathrm{hs,opt}}$), efficiency gain with regard to the reference system (Tab. 4.12), and the optimum type that indicates what determines the optimum design parameters.

Table 4.14: Comparison of semiconductor technologies. The most efficient variant is printed in bold.

	$\eta_{\text{sys,opt,ref}}$	$\eta_{\text{sys,opt}} - \eta_{\text{sys,opt,ref}}$		
Topology-PWM	Si	SiC	GaN	GaN*
2L-Sin	86.14	3.77	3.89	**3.93**
2L-OC	88.41	1.63	1.68	**1.70**
3LNPC-Sin	89.26	0.61	0.57	**0.72**
3LNPC-NPB	89.19	0.65	0.62	**0.77**
3LTT-Sin	89.04	1.02	0.99	**1.08**
3LTT-NPB	88.86	1.18	1.15	**1.26**
2L3Mser-Sin	89.13	1.09	0.79	**1.46**
2L3Mser-OC	89.66	0.76	0.68	**1.03**
2L3Mpar-Sin	88.76	1.77	1.89	**1.94**
2L3Mpar-OC	89.86	0.77	0.88	**0.91**

upper cost limit of this analysis $K_{\text{sys,rel}} < 1.83$. That is, for switching frequencies lower than $f_{\text{sw,opt}}$, the cost exceeds its limit (as larger and hence more expensive capacitors are required to keep the DC link voltage ripple constant). In the following, the semiconductor technologies, modulation schemes, and topologies are compared, based on the results shown in Fig. 4.10.

1) *Comparison of semiconductor technologies (Si/SiC/GaN/GaN*)* Based on the efficiency gain given in Fig. 4.10, Tab. 4.14 compares the maximum efficiency achieved with different semiconductor technologies (Si/SiC/GaN/GaN*) for each combination of topology and PWM scheme, where Si IGBTs are used as a reference. The following conclusions are drawn from Tab. 4.14: 1) For the considered specification, Si IGBTs are the least efficient, which is expected due to the high switching loss energies (Fig. 4.8a & b). 2) In general, GaN HEMTs are expected to be the most efficient technology in the future (at the same cost & volume). 3) In general, and in particular for SiC vs. GaN for the considered system specification, which semiconductor technology is more efficient cannot be determined just based on the device level characteristics. Instead, whether one technology is more efficient than the other depends on the device level characteristics (Fig. 4.8), the used combination of topology and PWM scheme (which in-

Table 4.15: Comparison of PWM schemes. The most efficient variant is printed in bold.

Topology (2L)	$\eta_{\mathrm{sys,opt,ref}}$ Sin-PWM	$\eta_{\mathrm{sys,opt}} - \eta_{\mathrm{sys,opt,ref}}$ OC-PWM
2L	90.07	**0.04**
2L3Mser	90.59	**0.10**
2L3Mpar	90.70	**0.07**
Topology (3L)	Sin-PWM	NPB-PWM
3LNPC	**89.98**	-0.02
3LTT	**90.12**	0.00

fluences the $P_{\mathrm{sw}}/P_{\mathrm{cond}}$-ratio), and the optimal switching frequency that depends on the design constraints such as the torque ripple constraint.

2) *Comparison of modulation schemes*
Based on the efficiency gain given in Fig. 4.10, Tab. 4.15 compares the maximum efficiency achieved with different PWM schemes for each topology (taking the maximum over Si/SiC/GaN/GaN*), where Sin-PWM is used as a reference. The following conclusions are drawn from Tab. 4.15: 1) For the 2L-topologies (2L, 2L3Mser, 2L3Mpar) with the considered system specification, OC-PWM is more efficient than Sin-PWM, as expected, because OC-PWM avoids switching of the phase-leg with the largest current, thereby reducing switching losses. 2) For the 3LNPC-topology and the considered specification, NPB-PWM leads to slightly higher switching losses due to an additional space vector used in every switching period. 3) For the 3LTT-topology with the considered system specification, Sin-PWM & NPB-PWM reach approximately the same efficiency because the loss-related disadvantage of the additional space vector of NPB-PWM is compensated by a lower switching frequency of 3LTT-NPB-GaN*-3ph compared to 3LTT-Sin-GaN*-3ph in Fig. 4.10. 4) In general, the most efficient PWM scheme cannot be determined just based on a simple comparison at equal switching frequency but the most-efficient PWM scheme depends also on the optimum switching frequency and hence also on the design constraints.

Table 4.16: Comparison of topologies. The most efficient variant is printed in bold.

$\eta_{\mathrm{sys,opt,ref}}$	$\eta_{\mathrm{sys,opt}} - \eta_{\mathrm{sys,opt,ref}}$				$\eta_{\mathrm{sys,opt,ref}}$	$\eta_{\mathrm{sys,opt}} - \eta_{\mathrm{sys,opt,ref}}$
2L	3LNPC	3LTT	2L3Mser	2L3Mpar	2L/3LNPC/3LTT	2L3Mser/2L3Mper
90.11	-0.13	0.01	0.58	**0.66**	90.12	**0.65**

3) *Comparison of topologies*
Based on the efficiency gain given in Fig. 4.10, Tab. 4.16 compares the maximum efficiency achieved with different topologies (taking the maximum over all combinations of Si/SiC/GaN/GaN* and PWM schemes). The following conclusions are drawn from Tab. 4.16: 1) For the considered specification, the topology 2L3Mpar has the best efficiency with +0.66 % higher efficiency than the 2L-topology. 2) For the considered specification, the modular topologies (2L3Mpar/2L3Mser) enable an efficiency increase of +0.65 % compared to the non-modular topologies (2L/3LNPC/3LTT), which is due to the higher winding factor of the 9-phase winding that reduces the motor losses. Indeed, Fig. 4.10 shows lower copper losses P_{Cu} for all configurations with modular topologies compared to the configurations with standard/non-modular topologies. The fact that the modular topologies can be combined with 9-phase windings with a higher winding factor than 3-phase windings is a general advantage of these topologies.

4.2.3 Reliability Analysis

The considered converter topologies are also compared with regard to the reliability based on the model given in section 3.5 for the reliability related system specification summarized in Tab. 4.17. For simplicity, the same failure rate of $\lambda = 500$ fit is assumed (which is chosen based on Fig. 6 in [147]) for all power semiconductor devices, where 1 fit corresponds to 1 *failure in time* with a reference time interval of 10^9 hours. The 2L-nM-ser-topology is analysed with 3 modules ($n = 3$) and for three different redundancy configurations (no redundancy ($k = 0$), 1-out-of-3-redundancy ($k = 1$), and 2-out-of-3-redundancy ($k = 2$)) to

Table 4.17: Reliability related system specification and results of the reliability analysis.

Topology	Device failure rates (fit)	Redundancy	$MTTF$ (years)	$MTTF_{\mathrm{rel,2L}}$
2L	$\lambda_{\mathrm{S1}} = 500$	-	38.1	1
3L-NPC	$\lambda_{\mathrm{S1}} = \lambda_{\mathrm{D5}} = 500$	-	12.7	$1/3$
3L-TT	$\lambda_{\mathrm{S1}} = \lambda_{\mathrm{S2}} = 500$	-	19.0	$1/2$
2L-nM-ser	$\lambda_{\mathrm{S1}} = 500$	$\{k, n\} = \{0, 3\}$	12.7	$1/3$
2L-nM-ser	$\lambda_{\mathrm{S1}} = 500$	$\{k, n\} = \{1, 3\}$	31.7	$5/6$
2L-nM-ser	$\lambda_{\mathrm{S1}} = 500$	$\{k, n\} = \{2, 3\}$	69.8	$11/6$

investigate the effect of redundancy on the reliability. The 2L-nM-par-topology is not separately listed, as the model equations in Tab. 3.13 already indicate that both modular topologies (2L-nM-ser & 2L-nM-par) have the same reliability.
Tab. 4.17 shows the results for the absolute mean time to failure $MTTF$ and for the relative mean time to failure with regard to the 2L-topology, $MTTF_{\mathrm{rel,2L}}$. Note that $MTTF$ depends on λ, whereas $MTTF_{\mathrm{rel,2L}}$ is independent of λ. The resulting values for $MTTF$ and $MTTF_{\mathrm{rel,2L}}$ show that the modular topologies without any redundancy ($k = 0$) are as reliable as the 3L-NPC but less reliable than 2L and 3L-TT. With a 1-out-of-3-redundancy, the reliability of the modular topologies increases, as expected, but is still lower than the one of the 2L-topology. This shows that for a 1-out-of-3-redundancy, the higher risk of component failure due to more components of the modular topologies outweighs the redundancy effect on the reliability. Only for a 2-out-of-3-redundancy, the modular topologies are more reliable in terms of the $MTTF$ than the 2L-topology. It should be noted that for 2L-nM-ser and for a given DC link voltage, a higher redundancy level implies a higher required voltage rating of the power semiconductor devices, whereas for 2L-nM-par, there is no such additional design requirement.

4.2.4 Conclusion

The following conclusions are drawn from the presented design study:

- A procedure for the optimal design of IMDs in terms of ρ_{sys}, η_{sys}, and K_{sys} is presented. The design procedure incorporates a new

iron loss density model (GMLSE5+BPG) and enables the comparison of modular converter topologies (2L3Mser/2L3Mpar) to standard/non-modular topologies (2L/3LNPC/3LTT) covering a large design space including different PWM variants, semiconductor technologies (Si/SiC/ GaN), and winding schemes.

- For a 1.5 kW IMD, the cost-optimal system configuration is 2L-OC-Si-3ph. Compared to this, the suggested design has the configuration 2L3Mpar-OC-GaN-9ph and enables an efficiency increase of +2.26 % at 36 % higher cost. Assuming a utilization of 90 % and an energy price of 0.1 CHF/kWh, the higher costs are compensated by the lower energy consumption after approximately 2 years.

- For a 1.5 kW IMD, different topologies, PWM schemes, and semiconductor technologies are compared with regard to maximum efficiency at equal system cost and volume. Modular topologies reach higher efficiencies than the standard topologies due to the general advantage that modular topologies can be combined with multiphase windings. The optimal PWM scheme and the optimal semiconductor technology cannot be predicted in general, as they depend on the system specification, such as the torque ripple constraint.

- A model for comparing the system reliability of standard topologies and of modular topologies is presented. The modular topologies 2L3Mser and 2L3Mpar only have an advantage over the standard 2L- and 3L-topologies, if a 2-out-of-3-redundancy is achieved.

4.3 Cooling Limits of Passively Cooled IMDs

In this section, a design study on the cooling limits of passively cooled IMDs is presented. The motivation for this design study is explained in the following.
A major design challenge of IMDs is the high ambient temperature of the power electronics due to its proximity to the motor [2–4]. Typical motor operating temperatures are up to 150..180 °C [4], which is mainly limited by the winding insulation class (class F: 155 °C, class H: 180 °C). However, typical operating temperatures of industrial electronics are 70..85 °C [9]. Therefore, a cooling system must be designed

that effectively limits the operating temperature of the electronics.
Existing literature about the thermal design of IMDs focuses on active cooling, i.e. either liquid cooling [18, 19, 148, 149] or forced air cooling [15, 150, 151]. The used thermal modelling methods are based on CFD/FEM and on lumped parameter thermal networks (LPTN). For passively cooled IMDs, design examples exist [8, 16, 152, 153], but the thermal design and the general performance limit of such IMDs has not been investigated yet. Therefore, the thermal design and the achievable cooling limits of passively cooled integrated drives are investigated in this thesis with this design study.
The proposed approach to calculate the cooling limits of an integrated drive is divided into the following three steps:

S1 *Development of a thermo-mechanical integration concept*
The thermo-mechanical integration concept was selected in section 2.1.2 and is given by the integration concept *C1* (Fig. 2.8) in combination with the insulation concept *I2* (Fig. 2.11b). The overall concept is shown in Fig. 3.43.

S2 *Thermal modelling of the IMD with heat sink*
For this design study, the LPTN-based model of a finned end cap on the rear side of the motor was developed that is described in section 3.10.

S3 *Development of a procedure to calculate the cooling performance of the heat sink*
The developed procedure is presented in this section. Therein, the chosen cooling performance indicator is the cooling system performance index (CSPI) that was introduced in [154] in order to compare the performance of different fan cooled heat sinks. In this design study, the CSPI is applied to passively cooled heat sinks of IMDs.

In the following, first the developed general design procedure for a finned end cap/heat sink with optimal fin spacing and fin thickness is presented in section 4.3.1. This procedure results in the CSPI of the optimised heat sink. In section 4.3.2, the results of applying this design procedure to exemplary specifications of high-torque IMDs are presented.

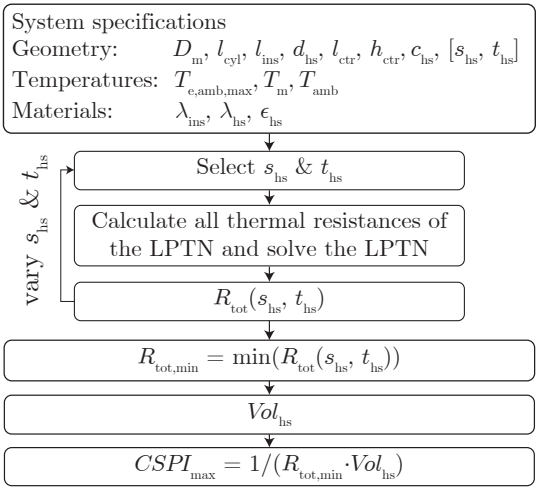


Figure 4.11: *HS-Design-Proc*: Heat sink/end cap design procedure for an encoder-sided inverter-integrated end cap (IMD concept from Fig. 3.43) with optimised cooling fin spacing (s_{hs}) and thickness (t_{hs}), resulting in the cooling system performance index ($CSPI$). The geometry parameters are defined in Fig. 3.53.

4.3.1 Heat Sink Design Procedure Resulting in the *CSPI*

The cooling system performance index $CSPI$ is defined as $1/(R_{tot} \cdot Vol_{hs})$, where R_{tot} is the thermal resistance of the heat sink and Vol_{hs} is the heat sink volume [154]. With the assumption of a constant $CSPI$, the $CSPI$ is a scaling tool for system designers to determine the heat sink volume for a required cooling power at a given temperature difference. In the following, it is shown that the heat sink dimensions and the heat sink temperature affect the $CSPI$, hence the $CSPI$ is not constant for the considered IMD. Therefore, the target is to determine a narrow range of the $CSPI$ in order to provide such scaling tool for heat sinks that are suitable for the considered thermo-mechanical integration concept.
The heat sink/end cap design procedure resulting in the $CSPI$ is shown in Fig. 4.11 and starts with the system specifications (geometry, tem-

Table 4.18: Exemplary specifications of high-torque IMDs with an encoder-sided inverter integrated end cap (IMD concept from Fig. 3.43).

Motor/end cap diameter	D_m	200..1000 mm
End cap cylinder length	l_{cyl}	0..150 mm
End plate thickness	d_{hs}	3 mm
Encoder housing height	h_{ctr}	100 mm
Length of encoder + control PCB	l_{ctr}	100 mm
Fin length	c_{hs}	25 mm
Fin spacing	s_{hs}	1..20 mm
Fin thickness	t_{hs}	1..5 mm
Insulation layer thickness	l_{ins}	10 mm
Max. electronics temp.	$T_{\mathrm{e,amb,max}}$	70/85/105/125 °C
Motor temperature	T_{m}	100 °C
Ambient temperature	T_{amb}	40 °C
Insulation thermal conductivity	λ_{ins}	0.1 $\mathrm{W\,m^{-1}\,K^{-1}}$
End cap th. conductivity (Al)	λ_{hs}	236 $\mathrm{W\,m^{-1}\,K^{-1}}$
End cap emissivity (black Al)	ϵ_{hs}	0.95

perature, and material parameters) that are required to parametrize the thermal heat sink model from section 3.10 (Fig. 3.54). Fix values are specified for all parameters except for the fin spacing s_{hs} and for the fin thickness t_{hs} for which intervals are specified (indicated by the brackets in Fig. 4.11). The procedure then iterates through these intervals in order to find the optimal fin spacing and fin thickness that minimise the total thermal resistance R_{tot}, resulting in $R_{\mathrm{tot,min}}$. For each set of s_{hs} and t_{hs} in the optimisation loop, all thermal resistances of the LPTN (Fig. 3.54) are calculated and the LPTN is solved. Solving the LPTN is an iterative process due to the non-linearity of thermal resistances that describe a convective or radiative heat transfer. After the optimisation, the heat sink volume Vol_{hs} is calculated and the $CSPI_{\mathrm{max}}$ results from Vol_{hs} and $R_{\mathrm{tot,min}}$, using the $CSPI$-definition from [154].

4.3.2 Application to Exemplary Specifications

In this section, the results of applying the design procedure shown in Fig. 4.11 to exemplary specifications of high-torque IMDs are presented. These specifications are summarized in Tab. 4.18. In the following,

first the result of the fin spacing optimisation loop from Fig. 4.11 is discussed. Then, the influence of different end cap size parameters and of the end cap temperature on the $CSPI$ are investigated. Finally, an analysis of the different heat transfer contributions is presented.

Result of the Fin Spacing Optimisation

Fig. 4.12a shows the result of optimising the fin spacing and fin thickness in the optimisation loop of the procedure in Fig. 4.11. The minimum fin thickness is limited to 1 mm to ensure mechanical stability and feasibility. However, Fig. 4.12a shows $R_{\mathrm{tot}}(s_{\mathrm{hs}}, t_{\mathrm{hs}})$ also for $t_{\mathrm{hs}} < 1\,\mathrm{mm}$ to demonstrate that this mechanical constraint has only a low impact on the value of $R_{\mathrm{tot,min}}$, even though the constraint excludes the thermally optimal fin thickness ($t_{\mathrm{hs}} = 0.5\,\mathrm{mm}$) from the specified range of feasible fin thicknesses.

CSPI Depending on the End Cap Size and Temperature

Fig. 4.12b shows the influence of the end cap diameter D_m and of the end cap cylinder length l_{cyl} on the $CSPI$ for $T_{\mathrm{e,amb,max}} = 85\,^{\circ}\mathrm{C}$. The $CSPI$ decreases with increasing D_m because the heat transfer coefficient for convective heat transfer from the fins to the cooling channels is smaller for vertically longer channels. The dependency of the $CSPI$ on l_{cyl} shows discontinuities of the slope at particular values of l_{cyl} (red lines in Fig. 4.12b). These discontinuities are due to changes in the end cap shapes ($ET = 1/2/3$) defined in Fig. 3.53b. Overall, Fig. 4.12b shows that the $CSPI$ is not constant over the end cap dimensions D_m and l_{cyl}, but a rather narrow range of $0.67..1.8\,\mathrm{W\,K^{-1}\,L^{-1}}$ is found for relatively large intervals of D_m and l_{cyl}.
Fig. 4.12c shows the influence of choosing different temperature grades of the power electronics on the $CSPI$. The $CSPI$ increases with higher temperature grades $T_{\mathrm{e,amb,max}}$ (and hence higher heat sink temperature T_{base}) because the buoyancy forces (that create natural convection) and the radiative heat transfer coefficient increase with temperature. Still, the $CSPI$ is in a relatively narrow range of $0.68..2.25\,\mathrm{W\,K^{-1}\,L^{-1}}$.

Analysis of Heat Transfer Contributions

The different heat transfer paths in the thermal heat sink model (Fig. 3.54) between the end cap and the ambient air are analysed regarding

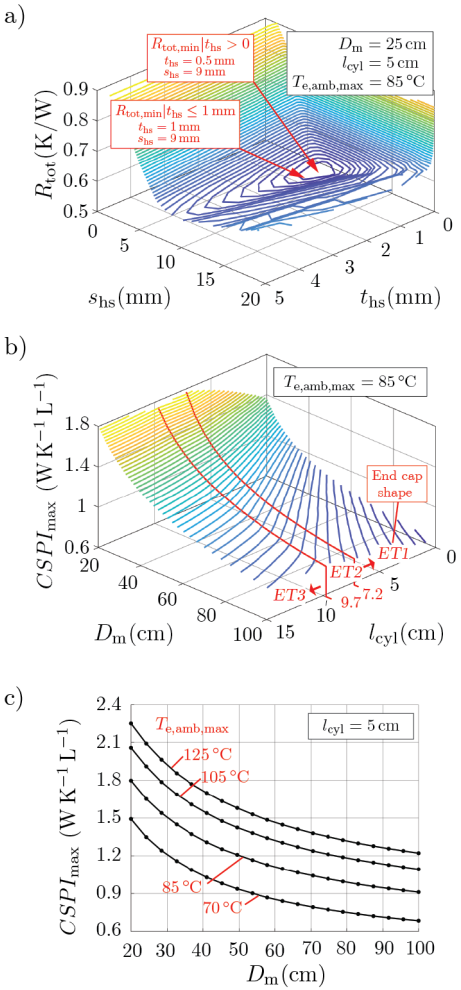


Figure 4.12: Results of applying the design procedure in Fig. 4.11 to the system specifications given in Tab. 4.18. a) Optimal fin spacing s_{hs} and fin thickness t_{hs} for a minimal thermal resistance R_{tot}. b) Influence of the IMD dimensions D_m and l_{cyl} on the cooling system performance index ($CSPI$). The red lines mark discontinuities in the slope of the $CSPI$ with l_{cyl}. c) Influence of the selected temperature grade of the power electronics $T_{\mathrm{e,amb,max}}$ on the $CSPI$.

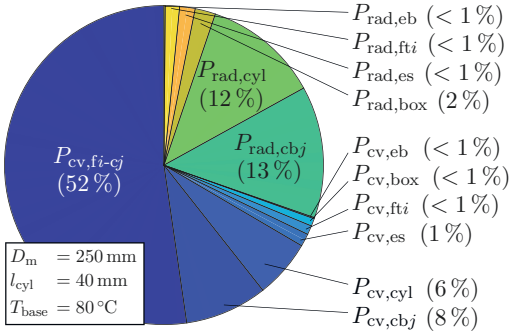


Figure 4.13: Relative distribution of the heat flow from an exemplary end cap (Tab. 4.18) to the ambient air among all possible heat transfer paths. Each heat flow contribution with a given subscript corresponds to the heat flow through the thermal resistance with the same subscript in Fig 3.54. For a compact notation, heat flow contributions with subscripts containing an index variable indicate the sum over that variable, e.g. $P_{\mathrm{rad,cb}j}$ indicates $\sum_{j=1}^{N_{\mathrm{f}}-1} P_{\mathrm{rad,cb}j}$.

their contributions to the overall heat transfer. The goal is to assess whether certain thermal resistances in the LPTN in Fig. 3.54 can be neglected. The motivation of neglecting thermal resistances is twofold: Firstly, reducing the amount of thermal resistances in any LPTN reduces the effort of its implementation and solving. Secondly, reducing the amount of parallel heat transfer paths in the LPTN increases the total thermal resistance R_{tot} which can serve as a safety margin for the end cap design.

Fig. 4.13 shows the result of this analysis for the specifications given in Tab. 4.18, indicating that some thermal resistances only contribute with $\leq 1\,\%$ to the overall heat flow. Therefore, these thermal resistances can be neglected. As expected, the fin-to-channel heat flow ($P_{\mathrm{cv,f}i\text{-}\mathrm{c}j}$ in Fig. 4.13) contributes the most (52 %) to the overall heat flow. The contributions of all convective heat flows ($P_{\mathrm{cv,...}}$ in Fig. 4.13) sum up to 70 % versus 30 % of heat flows by thermal radiation, indicating that heat transfer via thermal radiation as a whole is not negligible.

4.3.3 Conclusion

In this design study, the cooling limits of passively cooled IMDs are investigated. The underlying thermo-mechanical integration concept is the concept from section 2.1.2. As thermal heat sink model, the thermal model of a finned inverter-integrated motor end cap from section 3.10 is used. A procedure for the optimal heat sink design is presented which results in the cooling limit in terms of the $CSPI$. The heat sink design procedure can be used by system designers to determine whether passive cooling is sufficient for their system or whether active cooling is required. The procedure is applied to a set of exemplary specifications for high-torque motors (Tab. 4.18, $T_{\mathrm{e,amb,max}} = 85\,^{\circ}\mathrm{C}$) resulting in a $CSPI$ range of $0.67..1.8\,\mathrm{W\,K^{-1}\,L^{-1}}$. This relatively low $CSPI$-range requires rather high diameter to power ratios. Such ratios are characteristic for high-torque, low-speed motors and loads which therefore should be the primary "target-group" for passively cooled IMDs.

5

Control of an IMD consisting of a Stacked Polyphase Bridge Converter and a 9-phase PMSM

The previous chapter has shown that SPB-/N_{m}P-2L-converters combined with 9-phase motors have an advantage in terms of the power density/efficiency compared to standard 2L-/3L-inverters combined with 3-phase motors due to the higher winding factor that can be achieved with 9-phase windings. With regard to the control, the SPB-topology is more challenging than the N_{m}P-2L-topology due to the requirement of DC link voltage balancing. To address this challenge, the control of SPB-Cs was investigated more in detail, and an improved control concept for a drive system consisting of an SPB-C and a 9-phase PMSM under consideration of a DC source impedance was developed. Such a DC source impedance is given if DC cables are used to connect IMDs to a DC voltage source that is located with some distance to the IMDs. Possible applications for such cables are electric cars (for connecting the inverter(s) to the battery) or factories with a single DC supply connected to multiple distributed IMDs. The developed improved control concept is presented in this chapter which, in its essence, was previously published in [155].

The control of a drive system including a multiphase motor, an SPB-C, and a DC cable is a challenging task because it requires a non-standard transformation matrix for the motor current control, DC link balancing, and total DC link voltage stabilisation.
In the literature, several techniques for the current/torque control of

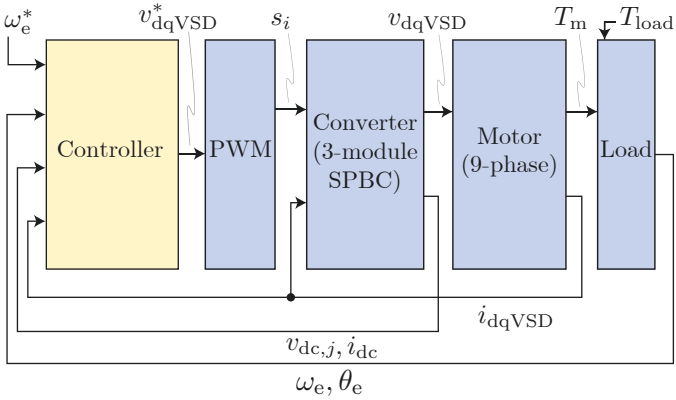


Figure 5.1: Considered drive system configuration. The system blocks in blue represent the plant of the closed loop control system.

multiphase PMSMs are presented, as reviewed in [78]. More recent contributions to such control techniques are given in [156–160]. However, the presented techniques assume inverter topologies that do not require DC link balancing. Control concepts considering both current/torque control and DC link balancing control in a modular series connected inverter are given in [11, 161–165]. However, [161–165] implicitly assume phase-aligned 3-phase winding modules without any magnetic coupling, whereas multiphase windings such as 9-phase windings consist of non-phase-aligned 3-phase winding modules that are magnetically coupled. This magnetic coupling requires a different current control concept. A control concept combining such current control with voltage balancing control is given in [11] for an induction machine with a symmetrical 9-phase winding system. However, the concept presented in [11] does not take any DC source impedance into account and does not specify any constraints on the PI controller parameters. Therefore, the open questions are:

1. How should the reference voltage for the DC link modules be defined? In [11], the total DC link voltage V_{dc} is considered constant. In that case the obvious choice is $V_{dc}/3$, as the number of 3-phase modules is 3. However, as shown in Fig. 5.2, the converter model with source impedance (R_b, L_b) has two DC link voltages, V_{dc} at

the supply and v_Σ at the converter. Hence, $V_{dc}/3$ or $v_\Sigma/3$ are potential candidates for the reference voltage. [164] shows that the choice of the reference voltage affects the system stability when all module DC link voltages are controlled. However, in [11] only two out of three module DC link voltages are controlled. Hence the results from [164] cannot directly be applied.

2. For a given definition of the module reference voltage, under what conditions is the system stable?

3. Given that the control concept from [11] involves multiple control loops in a nested structure, under what assumptions can each controller be tuned separately using standard control design techniques?

This chapter presents a controller concept based on the concept from [11], adapted to PMSMs and extended to include also the DC source impedance.
In the following, first a model of the controlled drive system, i.e. of the *plant* in terms of control theory is given in section 5.1. This includes the blue system blocks in Fig. 5.1 showing the complete drive system configuration. The structure of the controller (yellow block in Fig. 5.1) is presented in section 5.2. There, the module DC link reference voltage is defined as $v_\Sigma/3$. The closed loop stability of the voltage balancing control is analysed in section 5.3, also leading to an explanation for why $v_\Sigma/3$ is the appropriate reference voltage. Taking the resulting stability condition into account, a controller tuning method is given in section 5.4. Finally, the controller concept is validated in a drive system simulation for an exemplary 1.5 kW PMSM in section 5.5.

5.1 Model of the Controlled Plant

This section presents the models of the drive system plant, corresponding to the blue system blocks in Fig.5.1, which are required for the controller design and for the system simulation.

5.1.1 Converter Model

Fig. 5.2 shows the model of a three-module SPB-C, including the DC source impedance, modelled as resistance R_b and inductance L_b. The

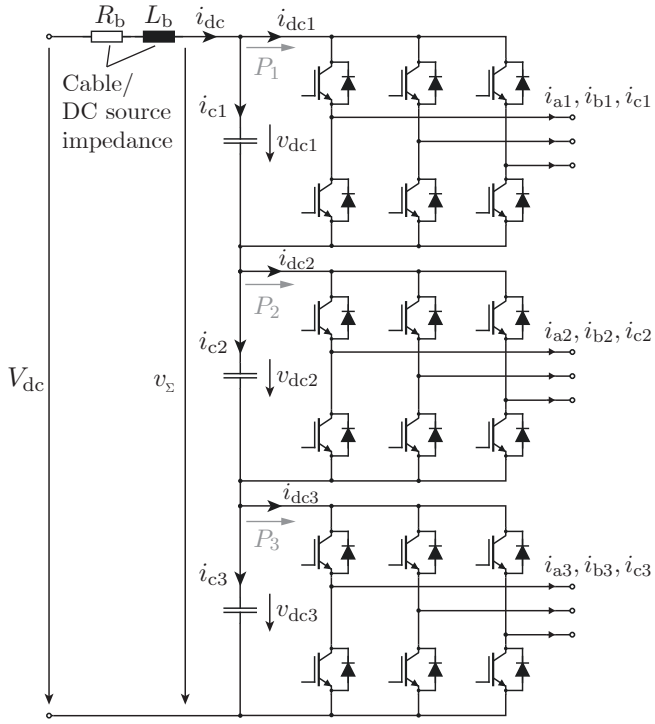


Figure 5.2: Schematic of a three-module stacked polyphase bridge converter (SPB-C) with DC cable resistance R_b and inductance L_b.

mesh equation of the voltage loop at the DC link input is given by

$$V_\mathrm{dc} = R_\mathrm{b} i_\mathrm{dc} + L_\mathrm{b} \frac{\mathrm{d}i_\mathrm{dc}}{\mathrm{d}t} + v_\Sigma. \tag{5.1}$$

There, V_dc is the constant source-side DC link voltage and v_Σ is the sum of the module DC link voltages $v_{\mathrm{dc},j}$,

$$v_\Sigma = \sum_{j=1}^{3} v_{\mathrm{dc},j}. \tag{5.2}$$

The module DC link voltages are governed by the nodal equation at the inputs of the 3-phase converter modules given by

$$C\frac{\mathrm{d}v_{\mathrm{dc},j}}{\mathrm{d}t} = i_{\mathrm{c},j} = i_{\mathrm{dc}} - i_{\mathrm{dc},j}. \tag{5.3}$$

The module DC link currents $i_{\mathrm{dc},j}$ in Fig. 5.2 can be expressed with the (non-linear) expression

$$i_{\mathrm{dc},j} = \frac{P_j}{v_{\mathrm{dc},j}}, \tag{5.4}$$

where P_j is the power flowing from the j-th DC link capacitor to the j-th 3-phase converter module. By assuming a high converter efficiency, the power P_j approximately corresponds to the power flowing into the motor. This approximation is made for the stability analysis of the closed loop voltage control which is presented later in section 5.3.

5.1.2 PWM Model

As PWM, standard third harmonic injection pulse width modulation (THIPWM, section 5.3 of [70]) is used. For the controller structure and for the controller tuning the PWM is approximated as ideal, whereas for the simulation presented in section 5.5 the PWM/switching is taken into account.

5.1.3 Motor Model and used Reference Frames

The considered symmetrical 9-phase motor model is the same as the one considered in [11] except for an adaptation from induction machines to PMSMs, which does not affect the control concept, but only the motor voltage equations. The motor voltage equations can be expressed in different reference frames, as explained in the following.
The control concept in [11] involves six different reference frames/variable spaces, which are called abc, abc1, VSD, MS, dqVSD, and dqMS. The abc-space is a phase space where the phases are sorted by increasing phase angle. The abc1-space is a phase space where the phases are sorted by groups of 3-phase winding systems. The VSD-space is a variable space in which the voltage equations of the considered 9-phase machine are decoupled. The MS-space is a variable space in which the power consumed/generated by each 3-phase module can be expressed.

The dqVSD-space and the dqMS-space are rotating reference frames in which sinusoidal VSD-/MS-space voltages/currents are constant.
The control concept presented in section 5.2 of this chapter only uses variables in the variable spaces abc, abc1, dqVSD, and dqMS. The transformation matrices required to transform voltages/currents between these variable spaces are given in the appendix in section A. In the equations of this chapter, the respective variable space used to express motor voltages/currents is indicated by subscripts using the following notation for a general 9-phase voltage/current vector $\boldsymbol{x}$ in the abc-, dqVSD-, abc1-, or dqMS-space:

$$\begin{bmatrix} \boldsymbol{x}_{\mathbf{abc}} \\ \boldsymbol{x}_{\mathbf{dqVSD}} \\ \boldsymbol{x}_{\mathbf{abc1}} \\ \boldsymbol{x}_{\mathbf{dqMS}} \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} x_{\mathrm{a}} & x_{\mathrm{ds}} & x_{\mathrm{a1}} & x_{\mathrm{d1}} \\ x_{\mathrm{b}} & x_{\mathrm{qs}} & x_{\mathrm{b1}} & x_{\mathrm{q1}} \\ x_{\mathrm{c}} & x_{\mathrm{dx1}} & x_{\mathrm{c1}} & x_{\mathrm{z1}} \\ x_{\mathrm{d}} & x_{\mathrm{qy1}} & x_{\mathrm{a2}} & x_{\mathrm{d2}} \\ x_{\mathrm{e}} & x_{\mathrm{dx2}} & x_{\mathrm{b2}} & x_{\mathrm{q2}} \\ x_{\mathrm{f}} & x_{\mathrm{qy2}} & x_{\mathrm{c2}} & x_{\mathrm{z2}} \\ x_{\mathrm{g}} & x_{\mathrm{z1}} & x_{\mathrm{a3}} & x_{\mathrm{d3}} \\ x_{\mathrm{h}} & x_{\mathrm{z2}} & x_{\mathrm{b3}} & x_{\mathrm{q3}} \\ x_{\mathrm{i}} & x_{\mathrm{z3}} & x_{\mathrm{c3}} & x_{\mathrm{z3}} \end{bmatrix} \tag{5.5}$$

The dqVSD-space is used for the current controllers presented in section 5.2. The current controllers are based on the motor voltage equations adapted to PMSMs in the dqVSD-space, resulting in (5.6)-(5.9).

$$\begin{bmatrix} v_{\mathrm{ds}} \\ v_{\mathrm{qs}} \end{bmatrix} = \begin{bmatrix} R_{\mathrm{s}} + L_{\mathrm{s}} \frac{\mathrm{d}}{\mathrm{d}t} & -\omega_{\mathrm{e}} L_{\mathrm{s}} \\ \omega_{\mathrm{e}} L_{\mathrm{s}} & R_{\mathrm{s}} + L_{\mathrm{s}} \frac{\mathrm{d}}{\mathrm{d}t} \end{bmatrix} \begin{bmatrix} i_{\mathrm{ds}} \\ i_{\mathrm{qs}} \end{bmatrix} + \begin{bmatrix} 0 \\ \omega_{\mathrm{e}} \psi_{\mathrm{PM}} \end{bmatrix} \tag{5.6}$$

$$\begin{bmatrix} v_{\mathrm{dx1}} \\ v_{\mathrm{qy1}} \end{bmatrix} = \begin{bmatrix} R_{\mathrm{s}} + L_{\mathrm{ls}} \frac{\mathrm{d}}{\mathrm{d}t} & \omega_{\mathrm{e}} L_{\mathrm{ls}} \\ -\omega_{\mathrm{e}} L_{\mathrm{ls}} & R_{\mathrm{s}} + L_{\mathrm{ls}} \frac{\mathrm{d}}{\mathrm{d}t} \end{bmatrix} \begin{bmatrix} i_{\mathrm{dx1}} \\ i_{\mathrm{qy1}} \end{bmatrix} \tag{5.7}$$

$$\begin{bmatrix} v_{\mathrm{dx2}} \\ v_{\mathrm{qy2}} \end{bmatrix} = \begin{bmatrix} R_{\mathrm{s}} + L_{\mathrm{ls}} \frac{\mathrm{d}}{\mathrm{d}t} & -\omega_{\mathrm{e}} L_{\mathrm{ls}} \\ \omega_{\mathrm{e}} L_{\mathrm{ls}} & R_{\mathrm{s}} + L_{\mathrm{ls}} \frac{\mathrm{d}}{\mathrm{d}t} \end{bmatrix} \begin{bmatrix} i_{\mathrm{dx2}} \\ i_{\mathrm{qy2}} \end{bmatrix} \tag{5.8}$$

$$v_{\mathrm{z},j} = \left(R_{\mathrm{s}} + L_{\mathrm{ls}} \frac{\mathrm{d}}{\mathrm{d}t} \right) i_{\mathrm{z},j}, \quad j = 1, 2, 3 \tag{5.9}$$

There, R_{s} is the motor winding resistance, L_{s} and L_{ls} are the main and leakage inductance, ψ_{PM} is the permanent magnet flux linkage, and ω_{e} is the electrical angular rotational frequency of the rotor, also called rotor speed in the following. It must be noted that the voltage equations in the dqVSD-space (5.6)-(5.9) assume an equal winding resistance R_{s} for

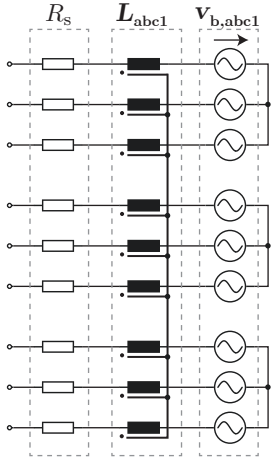


Figure 5.3: Model of a 9-phase PMSM in the abc1-phase space, including the phase resistance R_s, the inductance matrix $\boldsymbol{L}_\mathbf{abc1}$, and the back electromotive force vector $\boldsymbol{v}_\mathbf{b,abc1}$.

all phase windings and a symmetrical winding distribution. In order to test the control with disturbance given by unequal resistances, a motor model in the abc1-phase space, shown in Fig. 5.3, is used for deriving the simulation results presented in section 5.5.
The dqMS-space is used to express the power consumed by the j-th 3-phase motor winding. If a high converter efficiency is assumed, this power is approximately equal to the power P_j (Fig. 5.2) flowing out of the j-th DC link module capacitance. Assuming motor current control with maximum torque per ampere (MTPA) and a non-salient rotor, the motor current vector $\boldsymbol{i}_\mathbf{dqMS}$ only has non-zero q-components ($x_\mathrm{q1}, x_\mathrm{q2}$, and x_q3 in (5.5) where $\boldsymbol{x}$ is given by $\boldsymbol{i}$), which results in the following expression for the power P_j

$$P_j = \frac{3}{2} R_\mathrm{s} i_{\mathrm{q},j}^2 + \frac{3}{2} \psi_\mathrm{PM} i_{\mathrm{q},j} \omega_\mathrm{e}. \tag{5.10}$$

5.1.4 Load Model

The load model of the drive system in Fig. 5.1 is given by the following standard equation of motion (Tab. 3.1 of [166]),

$$J\frac{\mathrm{d}\omega_\mathrm{e}}{\mathrm{d}t} = p(T_\mathrm{m} - T_\mathrm{load}) \tag{5.11}$$

where J is the moment of inertia connected to the rotor, T_m is the mechanical motor torque, T_load is the load torque, and p is the pole pair number of the motor. As indicated in Fig. 5.1, the outputs of the load model are the rotor speed $\omega_\mathrm{e} = {}^{d\theta_\mathrm{e}}/_{dt}$ and the rotor position θ_e. In this load model, θ_e results from a double integration of (5.11). In a real system, θ_e is measured using an encoder.

5.2 Controller Structure

In this section, the structure of the proposed controller for the plant of the drive system, described in the previous section, is presented. Therefore, the top level control and its included controllers for the DC link balancing, currents, and speed are explained. The focus lies on the DC link balancing controller.

5.2.1 Top Level Control

Fig. 5.4 shows the top level structure of the drive controller, which corresponds to the top level structure proposed in [11], with the additional voltage signal v_Σ (Fig. 5.2) that is fed into the DC link balancing controller. The main concept is to control the motor torque and the module DC link voltages with current components of different dqVSD-subspaces which means different groups of vector components of the motor current vector $\boldsymbol{i}_{\mathbf{dqVSD}}$. Among all $\boldsymbol{i}_{\mathbf{dqVSD}}$-components given in (5.5), the current components i_qs & i_ds (forming a subspace called *idqs*) are used for the torque control, whereas the current components i_dx1 & i_qy1 (forming a subspace called *dqxy1*) and the current components i_dx2 & i_qy2 (forming a subspace called *dqxy2*) are used for the DC link balancing control. The currents of the subspaces dqs, dqxy1, and dqxy2 are controlled separately within the dqs-, dqxy1-, and dqxy2-current controller blocks shown in Fig. 5.4.

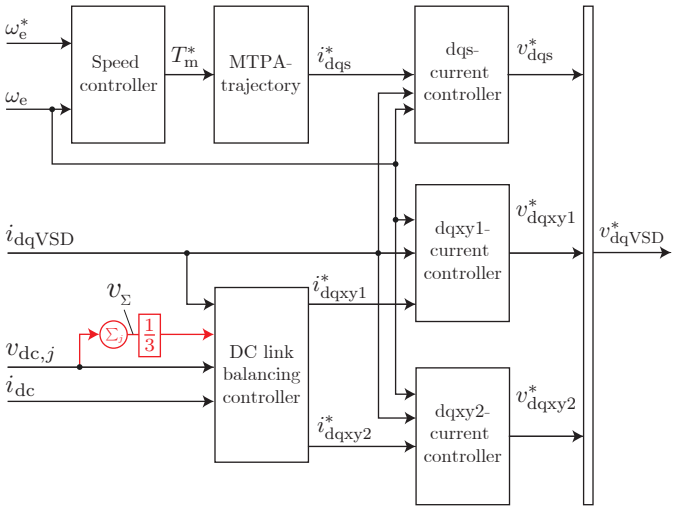


Figure 5.4: Top level structure of the drive controller based on [11], corresponding to the yellow block in Fig. 5.1. The voltage signal $v_\Sigma/3$ is added as input to the DC link balancing controller.

5.2.2 DC Link Balancing Controller

Fig. 5.5 shows the proposed DC link balancing controller. The balancing strategy from [11] is kept, which is to add a positive or negative balancing current $i_{q,j,bal}$ to $i_{q,j}$ when the module voltage $v_{dc,j}$ is larger or lower than its reference value $v_{dc,j}^*$. Hence (with (5.10)), the power drawn from the j-th module is increased or decreased, which in turn decreases or increases the module voltage $v_{dc,j}$ if the machine is operating in motor mode ($i_{dc} > 0$) and vice versa. In addition, to avoid affecting the torque, the sum of the reference balancing currents $i_{q,j,bal}^*$ for all modules ($j = 1, 2, 3$) is set equal to zero by the controller in Fig. 5.5 by only controlling two out of the three module voltages and by setting the third reference balancing current $i_{q3,bal}^*$ to $(-i_{q1,bal}^* - i_{q2,bal}^*)$.
The red parts in Fig. 5.5 show the changes with regard to [11] explained in the following:

1. In the proposed controller implementation, the current references in the dqxy(1,2)-subspaces are directly calculated in the dqMS- and in the dqVSD-space, without any intermediate step involving

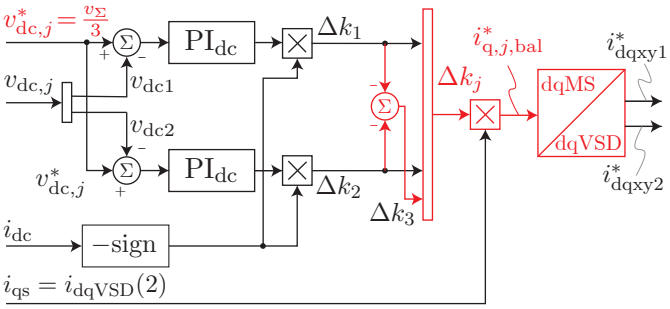


Figure 5.5: Proposed structure of the DC link balancing controller. Changes compared to [11] are marked in red: 1) The reference balancing currents $i^*_{\mathrm{q},j,\mathrm{bal}}$ are directly calculated from Δk_j without any intermediate step involving $k_j = 1 + \Delta k_j$, leading to less computational effort. 2) The appropriate module DC link reference voltage with present DC link cable impedance $(R_\mathrm{s}, L_\mathrm{s})$ is added.

variables in the VSD-space, which requires less transformations. Furthermore, the presented controller calculates the current references based on Δk_j instead of $k_j = 1 + \Delta k_j$, which is possible because the added "1" is cancelled out in the dqMS/dqVSD-transformation block in Fig. 5.5. This change also reduces the computational effort.

2. In the proposed controller implementation, the reference voltage $v^*_{\mathrm{dc},j}$ is chosen such that the effect of the source impedance $(R_\mathrm{b}, L_\mathrm{b})$ is taken into account: The reference value is set to $v_\Sigma/3$. In section 5.3, this choice for $v^*_{\mathrm{dc},j}$ is shown to be correct in the sense that it leads to an equivalent controller action on all DC link module voltages despite the fact that only two out of three voltages are controlled. It is noted that with this choice, the controller in Fig. 5.5 is a *pure balancing* controller, i.e. it does not act on the total DC link voltage v_Σ.

A total DC link voltage controller could theoretically be added with additional balancing currents $i_{\mathrm{q},j,\mathrm{bal}}$ that are defined equal for all modules $j = 1, 2, 3$ and that are set in the dqs-subspace. However, such a total DC link voltage controller, that would provide active damping

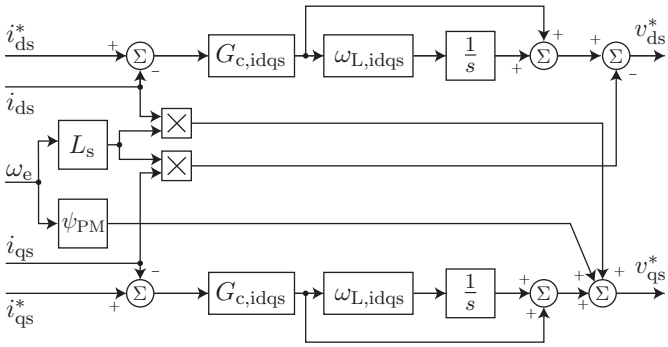


Figure 5.6: Controller for the currents i_{ds} and i_{qs} of the torque producing dqs-subspace. The controller structure corresponds to the well known PI controller with cross-coupling decoupling.

of the LC resonant circuit at the inverter input, is practically hardly feasible/useful because of the following reasons:

1. A total DC link voltage controller would have to control the total power flow out of the DC link (i.e. the total motor power) and hence the motor currents with a bandwidth of the order of magnitude of the resonance frequency $f_{\mathrm{res}} = 1/\sqrt{L_{\mathrm{b}}C/3}$. For reasonable values of L_{b} and C, e.g. using the specifications given in Tab. 5.1, the resonance frequency results in $f_{\mathrm{res}} \approx 100\,\mathrm{kHz}$. Given that the current controller bandwidth is limited by the PWM frequency f_{PWM}, a total DC link voltage control would require $f_{\mathrm{PWM}} >> 100\,\mathrm{kHz}$ and would hence result in high switching losses.

2. Controlling the total power flow of the motor leads to additional torque ripple.

For these reasons, a total DC link voltage controller is not considered further.

5.2.3 Dqs-Current Controller

Fig. 5.6 shows the dqs-current controller from Fig. 5.4, controlling the current vector components i_{ds} & i_{qs}. The structure is that of the well

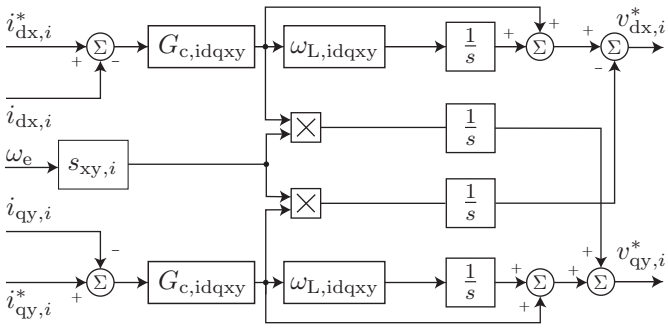


Figure 5.7: Controller for the currents $i_{\mathrm{dx},i=(1,2)}$ & $i_{\mathrm{qy},i=(1,2)}$ of the subspaces dqxy(1,2). There, $s_{\mathrm{xy},i} = \{-1, 1\}$ for $i = \{1, 2\}$. The controller is based on a complex vector PI controller [11], split up into its real and imaginary part and generalised with regard to the corner frequency $\omega_{\mathrm{L,idqxy}}$ that is kept general.

known cross-coupling decoupling controller for electrical drives, here adapted to PMSMs, which leads to the ψ_{PM}-block in Fig. 5.6.

5.2.4 Dqxy(1,2)-Current Controllers

The structure of the two dqxy(1,2)-current controllers in Fig. 5.4 is shown in Fig. 5.7. This structure incorporates two modifications compared to the complex vector PI controller given in [11]: 1) The controller from [11] is based on a block diagram using complex numbers. In contrast, the block diagram in Fig. 5.7 only uses real numbers by splitting up the complex vector PI controller into its real and imaginary part. This form of the controller is required for the implementation in a real system and for the simulation presented in section 5.5. 2) The controller shown in Fig. 5.7 has been generalised with respect to the corner frequency $\omega_{\mathrm{L,idqxy}}$ which is kept general in order to separate the controller structure from the controller tuning that is considered later in section 5.4.
The reason for using the controller from Fig. 5.7 in the dqxy(1,2)-space instead of the cross-coupling decoupling controller from Fig. 5.6 is that the dqxy(1,2)-currents depend on the relatively small leakage inductance L_{ls} and that the controller from Fig. 5.7 is less susceptible to

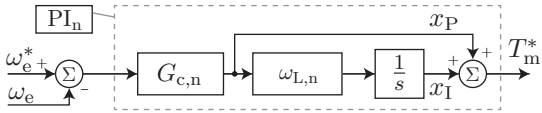


Figure 5.8: PI controller for the motor speed.

estimation errors of L_ls (section 3.6 of [167]).

5.2.5 Speed Controller

Fig. 5.8 shows the speed controller which is a simple PI controller that sets the torque reference T_m^* based on the speed error. Fig. 5.8 also serves as a model for all used PI$_x$-controllers with individual high frequency gain $G_{\mathrm{c},x}$ and corner frequency $\omega_{\mathrm{L},x}$, where x corresponds to idqs, idqxy, dc, or n, for the dqs-current controller, the dqxy(1,2)-current controllers, the DC link balancing controller, or the speed controller, respectively.

5.3 Stability Analysis

Among the controllers described in the previous section, the main focus of the current controllers (dqs, dqxy1, dqxy2) and of the speed controller is on reference tracking and disturbance rejection whereas the focus of the DC link balancing controller is on stabilisation because the converter/DC link plant model given by (5.1)-(5.4) can be open-loop unstable in motor mode ($P > 0$) [164]. The series DC link system has two groups of eigenvalues (called *instability modes* in [164]), one caused by the resonance of L_b and the total DC link capacitance $C/3$, and one caused by the instability of the module voltage balance [164]. The way to stabilise these groups of eigenvalues is determined based on the method from [164]. The required steps for the stability analysis are:

1. Linearisation of the DC link state space model (SSM) given by (5.1)-(5.4) with the states $\Delta v_{\mathrm{dc},j}$ and Δi_dc and with the inputs ΔP_j. The result of the linearisation is given in (9)-(12) of [164]. The linearisation process involves additional parameters for the equilibrium/steady state operating points for which the equations are linearised. In the following, these parameters are v_0, P_0, $i_{\mathrm{qs}0}$,

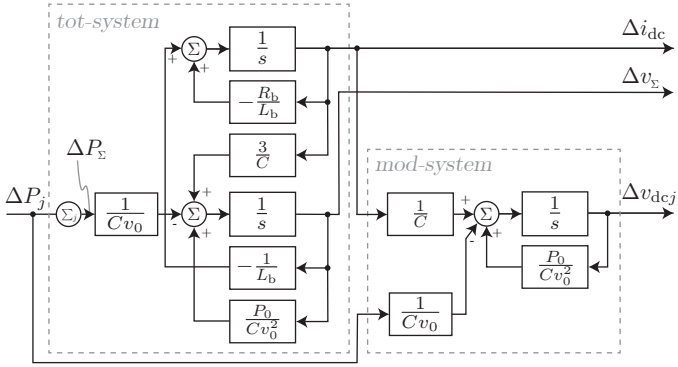


Figure 5.9: Block diagram showing the *tot-system* state space model (5.12) and the *mod-system* state space model (5.13).

and $\omega_{\mathrm{e}0}$, defining the steady state values of $v_{\mathrm{dc},j}$, P_j, $i_{\mathrm{q},j}$, and ω_{e}, respectively.

2. By adding the sum of the differential equation (5.3) for $j = 1, 2, 3$ to the system of equations from step 1, the system from step 1 is transformed into two subsystems, as shown in Fig. 5.9: 1) A *tot-system* for the total DC link voltage with the states Δv_{Σ} and Δi_{dc} and with the inputs ΔP_j. 2) A *mod-system* for the module DC link voltages with the states $\Delta v_{\mathrm{dc},j}$ and the inputs Δi_{dc} and ΔP_j. The SSM equations are given in (5.12) for the *tot-system* and in (5.13) for the *mod-system*.

$$\dot{\Delta} i_{\mathrm{dc}} = -\frac{R_{\mathrm{b}}}{L_{\mathrm{b}}} \Delta i_{\mathrm{dc}} - \frac{1}{L_{\mathrm{b}}} \Delta v_{\Sigma} \tag{5.12a}$$

$$\dot{\Delta} v_{\Sigma} = \frac{3}{C} \Delta i_{\mathrm{dc}} + \frac{P_0}{C v_0^2} \Delta v_{\Sigma} - \frac{1}{C v_0} \sum_{j=1}^{3} \Delta P_j \tag{5.12b}$$

$$\dot{\Delta} v_{\mathrm{dc},j} = \frac{P_0}{C v_0^2} \Delta v_{\mathrm{dc},j} + \frac{1}{C} \Delta i_{\mathrm{dc}} - \frac{1}{C v_0} \Delta P_j \tag{5.13}$$

3. Linearisation of the input power equation (5.10) resulting in (5.14).

$$\Delta P_j = \underbrace{\frac{3}{2} (2 R_{\mathrm{s}} i_{\mathrm{qs}0} + \omega_{\mathrm{e}0} \psi_{\mathrm{PM}})}_{:=a} \Delta i_{\mathrm{q},j} \tag{5.14}$$

4. Formulation of the *current setting strategy* by expressing $\Delta i_{\mathrm{q},j}$ as a function of the voltage error $(v^*_{\mathrm{dc},j} - v_{\mathrm{dc},j})$ as defined by the DC link controller structure, here given in Fig. 5.5, resulting in (5.15).

$$\Delta i_{\mathrm{q},j|j=1,2} = -\left(\left(\Delta v^*_{\mathrm{dc},j} - \Delta v_{\mathrm{dc},j}\right) G_{\mathrm{c,dc}} + \Delta x_{\mathrm{I},j}\right) i_{\mathrm{qs0}} \tag{5.15a}$$

$$\Delta i_{\mathrm{q3}} = -\Delta i_{\mathrm{q1}} - \Delta i_{\mathrm{q2}} \tag{5.15b}$$

$$\dot{\Delta} x_{\mathrm{I},j|j=1,2} = G_{\mathrm{c,dc}} \omega_{\mathrm{L,dc}} (\Delta v^*_{\mathrm{dc},j} - \Delta v_{\mathrm{dc},j}) \tag{5.15c}$$

There, $x_{\mathrm{I},j}$ is the output/state of the integrator of the $\mathrm{PI_{dc}}$-controller in Fig. 5.5. The condition $i_{\mathrm{dc}} > 0$ is assumed as the system can only be open-loop unstable for motor mode [164]. By defining the reference voltage $v^*_{\mathrm{dc},j}$ as $\frac{v_\Sigma}{3}$ and by inserting (5.15a) into (5.15b), (5.15) results in (5.16).

$$\Delta i_{\mathrm{q},j|\forall j} = -\left(\left(\frac{\Delta v_\Sigma}{3} - \Delta v_{\mathrm{dc},j}\right) G_{\mathrm{c,dc}} + \Delta x_{\mathrm{I},j}\right) i_{\mathrm{qs0}} \tag{5.16a}$$

$$\dot{\Delta} x_{\mathrm{I},j|\forall j} = G_{\mathrm{c,dc}} \omega_{\mathrm{L,dc}} \left(\frac{\Delta v_\Sigma}{3} - \Delta v_{\mathrm{dc},j}\right) \tag{5.16b}$$

This results in the desired behaviour because the controller balances all modules equally since the form of (5.16) is equal for all modules $j = 1, 2, 3$. Therefore $v_\Sigma/3$ is the correct choice for $v^*_{\mathrm{dc},j}$.

5. Insertion of the current setting strategy, (5.16), and of ΔP_j, (5.14), into the SSMs of the *tot-system*, (5.12) and of the *mod-system*, (5.13), and application of the Routh-Hurwitz stability criterion for each resulting closed loop SSM, called *cl-tot-system* and *cl-mod-system*. According to the Routh-Hurwitz stability criterion, asymptotic stability is given when all coefficients of the characteristic polynomial $c(s) = \det(s\boldsymbol{I} - \boldsymbol{A})$ are positive, where $\boldsymbol{A}$ is the state matrix of the considered closed loop SSM and $\boldsymbol{I}$ is the unity matrix. The results of the stability analysis are: The *cl-tot-system* is the same as the (open-loop) *tot-system* because the sum of the module powers

$$\sum_{j=1}^{3} \Delta P_j = a \underbrace{\sum_{j=1}^{3} \Delta i_{\mathrm{q},j}}_{0} \tag{5.17}$$

is zero. This result validates that the defined DC link controller does not act on the total DC link voltage Δv_Σ. Hence, the stability criterion for the total DC link stability corresponds to the open loop stability criterion given in [164],

$$C > \frac{P_0 L_\mathrm{b}}{v_0^2 R_\mathrm{b}}, \tag{5.18}$$

which means that the total DC link stability is ensured by using a large enough DC link capacitor.
For the *cl-mod-system*, the resulting SSM is different from the open-loop system and is given in matrix form in (5.19).

$$\underbrace{\begin{bmatrix}\dot{\Delta}v_{\mathrm{dc},j}\\ \dot{\Delta}x_{\mathrm{I},j}\end{bmatrix}}_{\dot{\boldsymbol{\Delta}}\boldsymbol{x}} = \underbrace{\begin{bmatrix}a_{11} & a_{12}\\ a_{21} & 0\end{bmatrix}}_{\boldsymbol{A}} \underbrace{\begin{bmatrix}\Delta v_{\mathrm{dc},j}\\ \Delta x_{\mathrm{I},j}\end{bmatrix}}_{\boldsymbol{\Delta x}} + \underbrace{\begin{bmatrix}b_{11} & b_{12}\\ 0 & b_{22}\end{bmatrix}}_{\boldsymbol{B}} \underbrace{\begin{bmatrix}\Delta i_\mathrm{dc}\\ \Delta v_\Sigma\end{bmatrix}}_{\boldsymbol{\Delta u}} \tag{5.19a}$$

$$a_{11} = \frac{1}{C v_0}\left(\frac{P_0}{v_0} - a i_{\mathrm{qs0}} G_{\mathrm{c,dc}}\right) \tag{5.19b}$$

$$a_{12} = \frac{a i_{\mathrm{qs0}}}{C v_0},\ a_{21} = -G_{\mathrm{c,dc}}\omega_{\mathrm{L,dc}} \tag{5.19c}$$

$$b_{11} = \frac{1}{C},\ b_{12} = \frac{a i_{\mathrm{qs0}} G_{\mathrm{c,dc}}}{3 C v_0},\ b_{22} = \frac{G_{\mathrm{c,dc}}\omega_{\mathrm{L,dc}}}{3} \tag{5.19d}$$

The characteristic polynomial of the state matrix $\boldsymbol{A}$ from (5.19) is then given by

$$\begin{aligned} c(s) &= \det(s\boldsymbol{I} - \boldsymbol{A}) \\ &= s^2 + s\left(\frac{a i_{\mathrm{qs0}} G_{\mathrm{c,dc}}}{C v_0} - \frac{P_0}{C v_0^2}\right) + \frac{a i_{\mathrm{qs0}} G_{\mathrm{c,dc}}\omega_{\mathrm{L,dc}}}{C v_0}. \end{aligned} \tag{5.20}$$

Applying the Routh-Hurwitz stability criterion results in the following stability condition

$$G_{\mathrm{c,dc}} > \frac{1}{v_0}\left(1 - \frac{3 R_\mathrm{s} i_{\mathrm{qs0}}}{2a}\right) \approx \frac{1}{v_0} \tag{5.21}$$

for the HF gain of the $\mathrm{PI_{dc}}$-controller $G_{\mathrm{c,dc}}$. There, the integrator has no effect on the stability, as $G_{\mathrm{c,dc}}\omega_{\mathrm{L,dc}} > 0$ is always ensured.

It must be noted that the result in (5.21) corresponds to the submodule DC link stability criterion calculated in [164]. However, the results given in [164] are not directly applied here because the controller structure is different: The presented controller uses two PI-controllers for the control of three modules, whereas [164] uses one P-controller per module.

5.4 Controller Tuning

In this section, a procedure for tuning/setting the high frequency gains $G_{\mathrm{c},x}$ and the corner frequencies $\omega_{\mathrm{L},x}$ of the involved PI-controllers PI_x is presented. As mentioned in section 5.2.5, x corresponds to idqs, idqxy, dc, or n, for the dqs-current controller, the dqxy(1,2)-current controllers, the DC link balancing controller, or the speed controller, respectively. The procedure is based on splitting the complete control system into four control loops that, via the assumption/condition of sufficiently large frequency intervals between the bandwidths of the control loops, can be independently tuned. The control loops are shown in Fig. 5.10 and these result in a nested structure as the loops in Fig. 5.10c & Fig. 5.10d are part of the control loops in Fig. 5.10a & Fig. 5.10b, respectively.
The tuning procedure is shown in Fig. 5.11. The first step of this procedure is to define the system specifications that are summarised in Tab. 5.1. Then, the control loop bandwidths $\omega_{\mathrm{c},x}$ and the corner frequencies $\omega_{\mathrm{L},x}$ are set to the following initial values:

$$\omega_{\mathrm{c,idqxy,0}} = 2\pi\frac{f_{\mathrm{PWM}}}{10}, \qquad \omega_{\mathrm{L,idqxy,0}} = \frac{R_{\mathrm{s}}}{L_{\mathrm{ls}}} \tag{5.22a}$$

$$\omega_{\mathrm{c,dc,0}} = \frac{\omega_{\mathrm{c,idqxy,0}}}{10}, \qquad \omega_{\mathrm{L,dc,0}} = \frac{\omega_{\mathrm{c,dc,0}}}{10} \tag{5.22b}$$

$$\omega_{\mathrm{c,idqs,0}} = \omega_{\mathrm{c,dc,0}}, \qquad \omega_{\mathrm{L,idqs,0}} = \frac{\omega_{\mathrm{c,idqs,0}}}{10} \tag{5.22c}$$

$$\omega_{\mathrm{c,n,0}} = \frac{\omega_{\mathrm{c,idqs,0}}}{10}, \qquad \omega_{\mathrm{L,n,0}} = \frac{\omega_{\mathrm{c,n,0}}}{10}. \tag{5.22d}$$

These initial values are chosen based on the controller conditions that are explained later in this section. In the next step, the high frequency

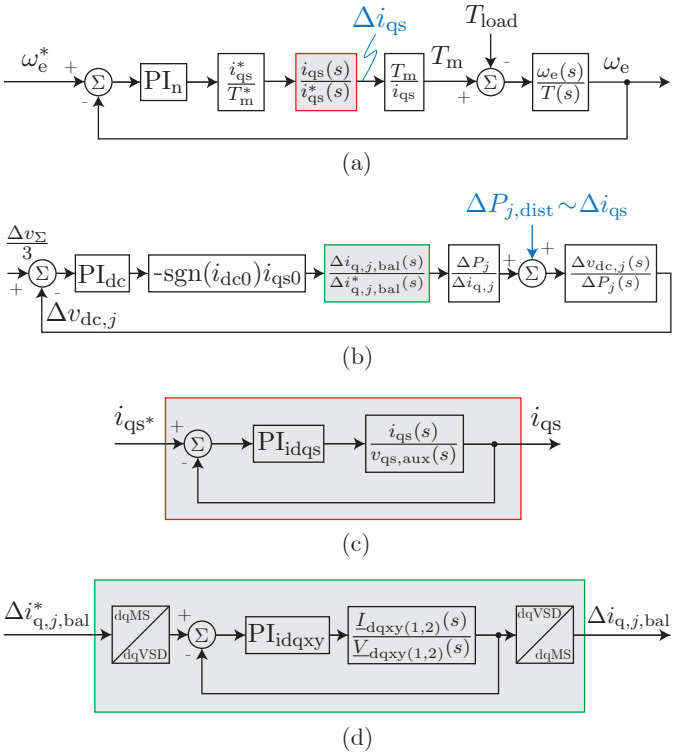


Figure 5.10: Simplified linear model of the drive system used for the controller tuning, involving four feedback control loops: (a) Speed control loop. (b) DC link balancing control loop for $v_{dc,j}$ (identical control loop for each module). (c) Idqs-current control loop. (d) Idqxy(1,2)-current control loops.

gains $G_{c,x}$ are calculated using (5.23),

$$G_{c,idqxy} = L_{ls}\omega_{c,idqxy} \tag{5.23a}$$

$$G_{c,idqs} = L_s\omega_{c,idqs} \tag{5.23b}$$

$$G_{c,n} = \frac{\omega_{c,n}J}{p} \tag{5.23c}$$

$$G_{c,dc} = \frac{2\omega_{c,dc}CV_{dc}}{9\left(2R_s i_{qs0}^2 + \psi_{PM} i_{qs0}\omega_{e0}\right)} \tag{5.23d}$$

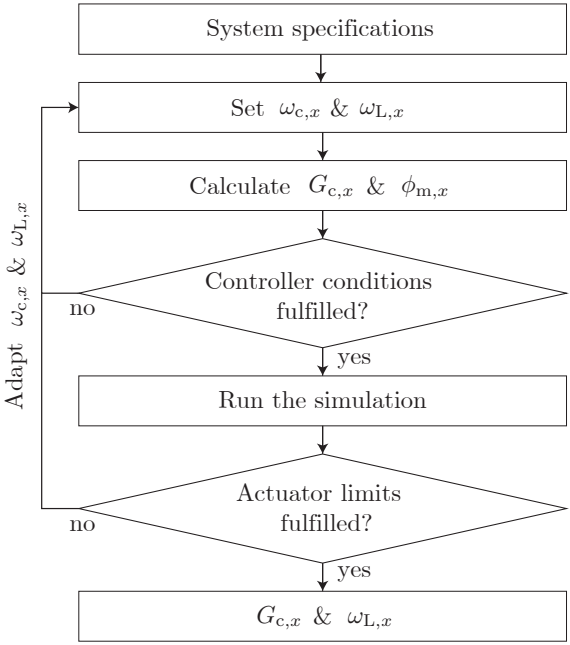


Figure 5.11: Tuning procedure for the PI-controllers of the different control loops shown in Fig. 5.10.

and the phase margins $\phi_{\mathrm{m,idqs}}$ and $\phi_{\mathrm{m,n}}$ are calculated using (5.24),

$$\phi_{\mathrm{m,idqs}} = 180^\circ + \angle T_{\mathrm{idqs}}(s)|_{s=\mathrm{j}\omega_{\mathrm{c,idqs}}} \tag{5.24a}$$

$$\phi_{\mathrm{m,n}} = 180^\circ + \angle T_{\mathrm{n}}(s)|_{s=\mathrm{j}\omega_{\mathrm{c,n}}}. \tag{5.24b}$$

There, $T_{\mathrm{idqs}}(s)$ and $T_{\mathrm{n}}(s)$ are the open loop transfer functions of the idqs-current control loop and of the speed control loop which are given by

$$T_{\mathrm{idqs}}(s) = G_{\mathrm{c,idqs}} \left(1 + \frac{\omega_{\mathrm{L,idqs}}}{s}\right) \frac{1/L_{\mathrm{s}}}{s + \frac{R_{\mathrm{s}}}{L_{\mathrm{s}}}} \tag{5.25a}$$

$$T_{\mathrm{n}}(s) = G_{\mathrm{c,n}} \left(1 + \frac{\omega_{\mathrm{L,n}}}{s}\right) \frac{p}{sJ}. \tag{5.25b}$$

In the next step, the controller parameters $G_{c,x}$ and $\omega_{L,x}$ are evaluated with regard to the following criteria:

- *Criterion 1:* The control loops should be decoupled. This criterion is fulfilled when the bandwidths of the inner control loops in Fig. 5.10c & Fig. 5.10d, $\omega_{\mathrm{c,idqs}}$ and $\omega_{\mathrm{c,idqxy}}$, are significantly larger than the bandwidths of the respective outer control loops in Fig. 5.10a & Fig. 5.10b, $\omega_{\mathrm{c,n}}$ and $\omega_{\mathrm{c,dc}}$, which is achieved by fulfilling the conditions

$$\omega_{\mathrm{c,n}} \leq \frac{\omega_{\mathrm{c,idqs}}}{10}, \quad \omega_{\mathrm{c,dc}} \leq \frac{\omega_{\mathrm{c,idqxy}}}{10}. \tag{5.26}$$

  In addition, the bandwidth of the DC link balancing control loop (Fig. 5.10b) $\omega_{\mathrm{c,dc}}$ should be larger than the bandwidth of the idqs-current control loop (Fig. 5.10a) $\omega_{\mathrm{c,idqs}}$. This ensures a sufficient rejection of the disturbance $\Delta P_{j,\mathrm{dist}}$, that results from a resistance imbalance and from the current Δi_{qs} that is set by the idqs-current control loop.

- *Criterion 2:* All control loops must be stable. The stability criterion of the DC link balancing control loop is already given in (5.21). The dqs-current control loop and the speed control loop are *single input single output* (SISO) systems that are open loop stable. Therefore, their closed loop stability can be ensured by the standard phase margin criterion for PI-control loops given by (section 9.4.1 of [168])

$$\phi_{\mathrm{m,idqs}} > 0, \quad \phi_{\mathrm{m,n}} > 0. \tag{5.27}$$

  The dqxy(1,2)-current control loops, split up into their real and imaginary parts, are *multiple input multiple output* (MIMO) systems. Therefore, the same stability analysis, that is applied to the DC link balancing controller in section 5.3, is applied to the idqxy(1,2)-current controllers. The resulting condition for stability is that the PI-parameters $G_{\mathrm{c,idqxy}}$ and $\omega_{\mathrm{L,idqxy}}$ must be positive, which is always fulfilled by definition of a PI-controller.

- *Criterion 3:* The PWM can be considered ideal. This criterion requires a sufficient margin between the bandwidths of the current control loops $\omega_{\mathrm{c,idqs}}$ & $\omega_{\mathrm{c,idqxy}}$ and the PWM frequency f_{PWM}. This margin is commonly chosen as one decade, resulting in the conditions

$$\omega_{\mathrm{c,idqs}} \leq 2\pi \frac{f_{\mathrm{PWM}}}{10}, \quad \omega_{\mathrm{c,idqxy}} \leq 2\pi \frac{f_{\mathrm{PWM}}}{10}. \tag{5.28}$$

When the above mentioned conditions are fulfilled, the simulation is executed and the simulation result is checked for the controller output limits. The output limit of the current control loops is determined by the THIPWM-unit whose output voltage magnitude $v_{\mathrm{dq},j} = \sqrt{v_{\mathrm{d},j}^2 + v_{\mathrm{q},j}^2}$ for each three-phase module ($j = 1, 2, 3$) is limited by

$$v_{\mathrm{dq},j} \leq \frac{v_{\mathrm{dc},j}}{\sqrt{3}}. \tag{5.29}$$

The speed control loop and the DC link balancer control loop are limited by a maximum allowed transient phase current $i_{\max}$ in order to stay within the inverter/motor temperature limits. This results in the condition

$$i_{\mathrm{a}}, i_{\mathrm{b}}, \ldots i_{\mathrm{i}} \leq i_{\max}. \tag{5.30}$$

If the controller conditions (5.26)-(5.28) and the controller output limits (5.29)-(5.30) are fulfilled, a valid/working set of controller parameters is found. Otherwise, the controller bandwidths $\omega_{\mathrm{c},x}$ and corner frequencies $\omega_{\mathrm{L},x}$ must be adapted in an iterative procedure as shown in Fig. 5.11. It must be noted that a valid set of controller parameters can be further adapted/optimised with regard to system dynamics, e.g. based on the methods described in [169].

5.5 Validation of the Controller

The control concept is validated in a simulation for the considered specifications summarised in Tab. 5.1. The used simulation model corresponds to the model shown in Fig. 5.1, where the converter and the motor are modelled by the electrical circuits shown in Fig. 5.2 and Fig. 5.3 and where the other parts (controller, PWM, and load) are modelled based on block diagrams. The block diagrams of the controller are given in Fig. 5.4-5.8. The block diagram of the PWM unit and of the load are not shown but the used models are explained in sections 5.1.2 & 5.1.4. The controller parameters that are used in the simulation and that result from the tuning procedure in Fig. 5.11 are summarised in Tab. 5.2. To increase the simulation speed, dead-time and measurement delays are not considered.

Fig. 5.12 shows the simulation result for a speed step from 150 rpm to 300 rpm and back to 150 rpm with a load torque of 12 N m. Similar to the approach in [11], a disturbance for the DC link voltage control is

Table 5.1: Exemplary specifications of a drive system with a high-torque low-speed PMSM.

Parameter	Symbol	Value
Rated power	$P_{\mathrm{m,r}}$	1.5 kW
Rated torque	$T_{\mathrm{m,r}}$	48 N m
Rated speed	$\omega_{\mathrm{e,r}}$	$2\pi \cdot 60$ Hz
Rated current (rms)	I_{r}	2.4 A
Max. current (pk)	$i_{\max}$	$2\sqrt{2}I_{\mathrm{r}}$
Pole pair number	p	12
DqVSD-main inductance	L_{s}	64.7 mH
DqVSD-leakage inductance	L_{ls}	12.9 mH
Winding resistance	R_{s}	1.02 Ω
Magnet flux linkage	ψ_{PM}	262 mWb
DC link voltage	V_{dc}	800 V
DC link module capacitance	C	35 µF
DC cable inductance	L_{b}	7.5 µH
DC cable resistance	R_{b}	0.86 Ω
PWM frequency	f_{PWM}	20 kHz
Power for $\mathrm{PI_{dc}}$ design	P_0	$P_{\mathrm{m,r}}/2$
Speed for $\mathrm{PI_{dc}}$ design	ω_{e0}	$\omega_{\mathrm{e,r}}/2$

Table 5.2: Controller parameters resulting from the tuning procedure in Fig. 5.11 applied to the specifications in Tab. 5.1.

Parameter	Symbol	Value
HF gain of $\mathrm{PI_{idqs}}$	$G_{\mathrm{c,idqs}}$	$45.4\,\mathrm{V\,A^{-1}}$
HF gain of $\mathrm{PI_{idqxy}}$	$G_{\mathrm{c,idqxy}}$	$158.4\,\mathrm{V\,A^{-1}}$
HF gain of $\mathrm{PI_{dc}}$	$G_{\mathrm{c,dc}}$	$85.2\,\mathrm{mV^{-1}}$
HF gain of $\mathrm{PI_n}$	$G_{\mathrm{c,n}}$	$154\,\mathrm{mN\,m\,s\,rad^{-1}}$
Corner frequency of $\mathrm{PI_{idqs}}$	$\omega_{\mathrm{L,idqs}}$	$49.1\,\mathrm{rad\,s^{-1}}$
Corner frequency of $\mathrm{PI_{idqxy}}$	$\omega_{\mathrm{L,idqxy}}$	$79.1\,\mathrm{rad\,s^{-1}}$
Corner frequency of $\mathrm{PI_{dc}}$	$\omega_{\mathrm{L,dc}}$	$614\,\mathrm{rad\,s^{-1}}$
Corner frequency of $\mathrm{PI_n}$	$\omega_{\mathrm{L,n}}$	$0\,\mathrm{rad\,s^{-1}}$

incorporated via a higher winding resistance of the second module, set to $2R_{\mathrm{s}}$. The result in Fig. 5.12 shows good reference tracking of the speed in terms of ω_{e} and of the torque producing current i_{qs}, hence of

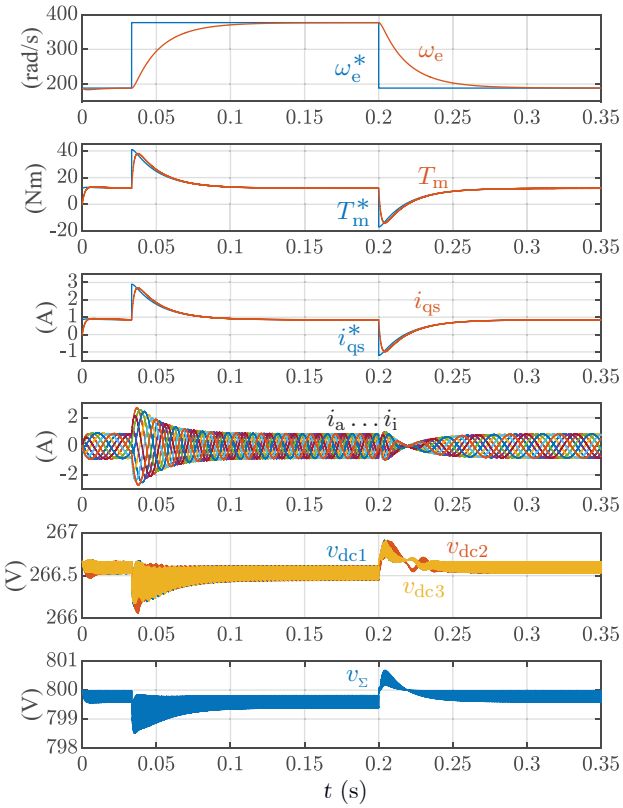


Figure 5.12: Simulation results for a drive system with the proposed control concept and the specifications from Tab. 5.1, showing (top to down) 1) the speed ω_e, 2) the torque T_m, 3) the current i_{qs}, 4) the motor currents in the abc-phase space, 5) the module DC link voltages $v_{dc,j}$, and 6) the total DC link voltage v_Σ.

the torque T_m as well. The DC link voltages $v_{dc,j}$ are well balanced. The total DC link voltage v_Σ has peaks where the speed steps occur due to the cable impedance. However, these peaks are relatively small due to a sufficiently large DC link capacitance of 35 µF (Tab. 5.1).

5.6 Conclusion

A control concept for drive systems consisting of a symmetrical 9-phase PMSM connected to an SPB-C via a cable with the impedance (R_b, L_b) is presented. The concept is based on [11], adapted to PMSMs, and extended by introducing the cable impedance that represents a source impedance of the DC source. For taking this source impedance into account, the appropriate choice for the module DC link voltage reference is found to be $v_\Sigma/3$. This choice leads to a voltage controller only acting on the balancing of the DC link module voltages, independently of fluctuations of the total DC link voltage (v_Σ) during for example load steps. The total DC link voltage is kept stable via sufficiently large DC link capacitors. Controlling also the total DC link voltage is theoretically possible with an additional voltage controller in the torque producing current subspace. However, such total DC link voltage control is not considered practically useful due to its high bandwidth requirement and due to an additionally resulting torque ripple. The stability analysis of the module DC link voltages leads to a stability condition on the high frequency gain of the DC link balancing controller. Taking the stability condition for the gain into account, the controllers of the proposed concept are tuned in the frequency domain based on the assumption/condition of sufficiently large frequency intervals between the bandwidths of the involved control loops. Using the resulting controller parameters, the complete control concept is validated in a simulation for exemplary system specifications (Tab. 5.1) based on a high-torque low-speed 1.5 kW PMSM.

6

Virtual Prototype of an IMD consisting of a Stacked Polyphase Bridge Converter and a 9-phase PMSM

In this chapter, a virtual prototype of an IMD based on an SPB-C and a 1.5 kW high-torque low-speed PMSM is presented. This virtual prototype consists of the design of inverter PCBs and of a mechanical CAD model of the total IMD system including the motor and the integrated inverter. The specifications of this prototype result from *IMD-Design-Proc-2* presented in section 4.2. The virtual prototype shows that this IMD design procedure leads to a realistic prototype design.
This chapter is structured as follows: First, the specification of the virtual prototype is given in section 6.1. Based on this specification, the inverter PCBs were designed which are described in section 6.2. Finally, the mechanical CAD model of the complete IMD system is presented in section 6.3.

6.1 Specification

The specification of the virtual prototype results from the design study presented in section 4.2 which is based on the IMD design/optimisation procedure *IMD-Design-Proc-2* (Fig. 4.6). Based on the design study result that is given by the 3D-pareto-front for future expected semicon-

Table 6.1: Optimal IMD design parameters resulting from *IMD-Design-Proc-2* (Fig. 4.6) for a 1.5 kW high-torque low-speed IMD with the constant specifications from Tab. 4.10, limited to designs with the SPB-topology.

Optimal values of structural DOFs	
PWM scheme	2L-OCPWM
Switch technology	GaN HEMT
Winding scheme	9-phase
Optimal values of operational DOFs	
Switching frequency f_s	54.36 kHz
Relative chip cost $K_\mathrm{sc,rel}$	1.4659
Fin length c_hs	0 mm
Optimal dependent design parameters	
Semiconductor rated current $I_\mathrm{r,univ}$	6.44 A
DC link capacitance $C_\mathrm{dc,h}$	22 µF
System power density ρ_sys	0.129 kW L^{-1}
System efficiency η_sys	89.79 %
Relative system cost $K_\mathrm{sys,rel}$	1.594

ductor costs (Fig. 4.9b), the optimal IMD design for the virtual prototype is determined by using equal objective weighting factors $w_\rho = w_\eta = w_K = 1/3$ for an equal weighting of system power density, efficiency, and cost, and by fixing the inverter topology to the SPB-topology. This leads to the optimal IMD design parameters given in Tab. 6.1.
The complete specification of the virtual prototype is given by the combination of the constant input parameters (Tab. 4.10) and the results (Tab. 6.1) of *IMD-Design-Proc-2*.

6.2 PCB Design

For the PCB design based on the specification defined in the previous section, first the equivalent circuit diagram of the total IMD system is considered which is shown in Fig. 6.1. This circuit diagram shows into which PCBs the inverter is divided: 3 power module PCBs (of identical

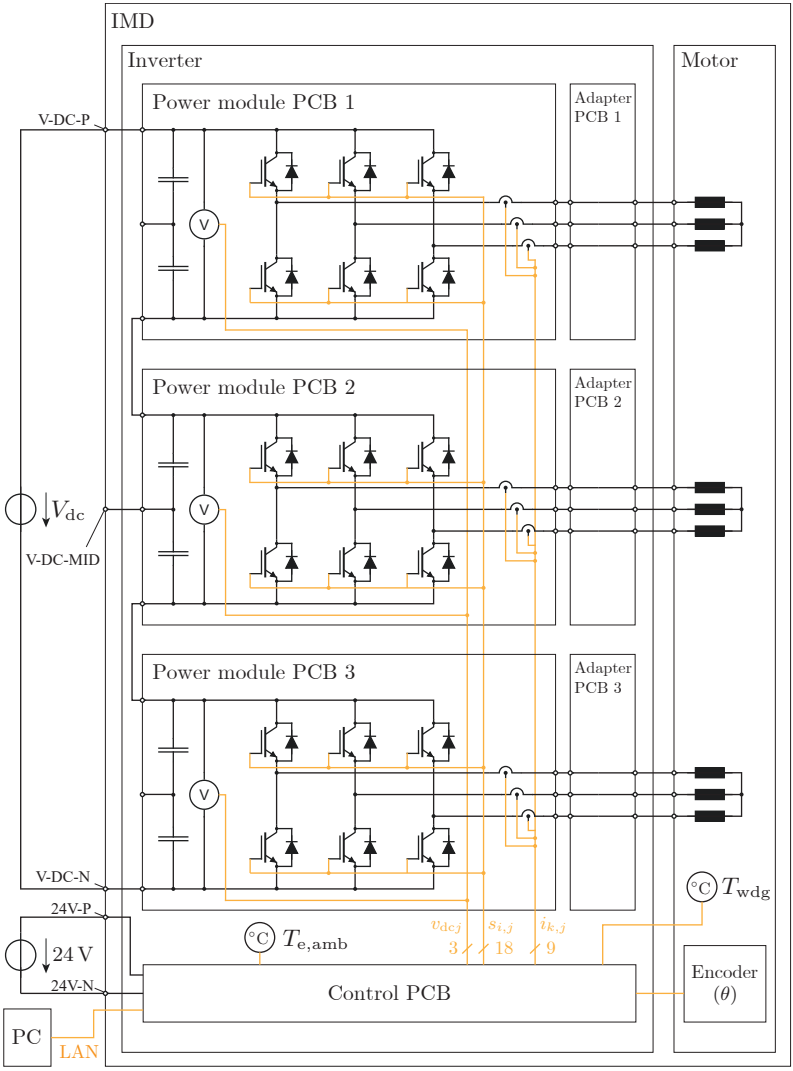


Figure 6.1: Equivalent circuit diagram for an IMD consisting of a 3-module SPB-C and a 9-phase motor, including the signal transmission concept. Signals are shown in orange.

Table 6.2: Main components on one power module PCB. Maximum rated operating temperature $T_{\mathrm{op,max}} \geq 85\,^{\circ}\mathrm{C}$.

Type of component	Number	Name	Description/Ratings
		Power circuit	
Power transistor	6	GS66506T	650 V, 22.5 A, GaN HEMT
DC link capacitor	2	C4AQJLW5220M36J	22 µF, 700 V, metallized film
Commutation capacitor	3	C3216NP02J103J160AA	10 nF, 630 V, ceramic
Bleeding resistor	8	ERJ2RKF1203X	120 kΩ, 0.1 W, SMD
		Gate driver circuit	
Gate driver	6	NCP81074ADR2G	10 A
Optocoupler	6	FOD8480	4.5..30 V (output)
Isolated DC-DC	6	R24P06S	24 V/6 V
		Voltage/current measurement circuit	
Current sensor	3	CAS5015KRA	15 A, isolated
Op-Amp	3	OPA197IDBVR	Non-isolated
Op-Amp	1	ISO224ADWVR	Isolated
ADC	4	LTC1402IGN#TRPBF	5 V, 12 bit

design), 3 adapter PCBs (of identical design), and one control PCB. The design of these PCBs is presented in the following.

One **power module PCB** contains one SPB-module including two DC link capacitors in series, three half bridges, a DC link voltage measurement circuit, and three current sensors for the three motor phase currents. It must be noted that measuring only two motor phase currents per three-phase module would be sufficient due to the star point connection. However, to achieve a more modular PCB design, each half bridge is combined with one current sensor in the presented design.
Tab. 6.2 summarises the component selection for one power module PCB. For the power transistor, the GaN HEMT from the device series GS665XXT with the smallest available rated current above 6.44 A (Tab. 6.1) is selected. With regard to the selected DC link capacitor it must be noted that the rated voltage of 700 V is significantly larger than the required rated voltage rating ($\approx V_{\mathrm{dc}}/3 = 267\,\mathrm{V}$). Nevertheless, this capacitor was selected because any available DC link capacitor with a lower voltage rating would have lead to a larger box volume of the populated PCB.
Fig. 6.2 shows a 3D model of the designed power module PCB with a view of the PCB top side (facing the motor). There, the DC link

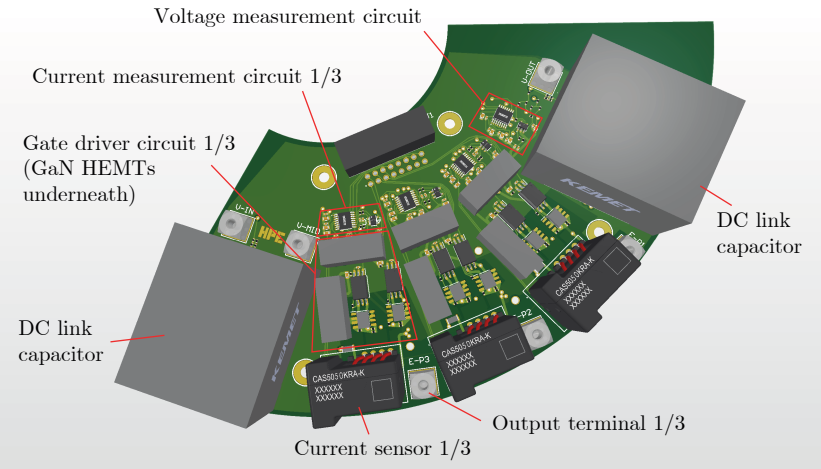


Figure 6.2: 3D model of one power module PCB.

capacitors are placed on the left and on the right side and the space in between is used for the three half bridges including their gate driver circuits and current sensors.

One **adapter PCB** realises the connection between the three half bridge output terminals of one power PCB (Fig. 6.2) and the phase windings of one 3-phase winding system of the 9-phase motor. A 3D model of one adapter PCB is shown in Fig. 6.3. The connection to the phase windings is realised with the socket *UMPT-03-01.5-L-V-S-TR* on the shown PCB top side. The connection to the power module PCB is realised with three *Würth 9Pin Bush M3* PCB terminals on the bottom side of the adapter PCB.

The **control PCB** consists of two partial PCBs, an interface PCB and an FPGA PCB, which are stacked on top of each other. The interface PCB was specifically designed for this virtual prototype, whereas the FPGA PCB is a universal control board of the laboratory for which the design was given. A 3D model of the control PCB with view onto the designed interface PCB is shown in Fig. 6.4.
The interface PCB mainly features a 24V/5V DC-DC converter and connectors for signal cables leading to the power module PCBs and to

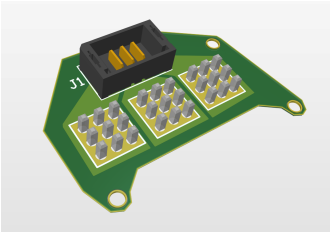


Figure 6.3: 3D model of one adapter PCB.

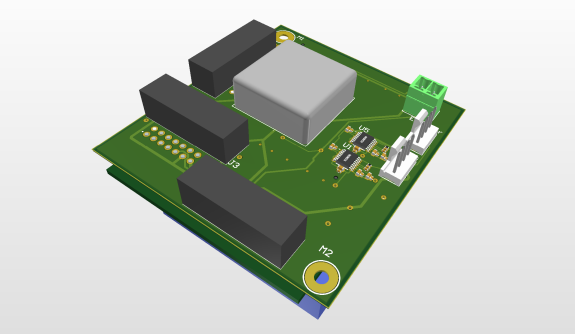


Figure 6.4: 3D model of the control PCB.

the encoder. Furthermore, the interface PCB contains a temperature measurement circuit for a monitoring of the electronics ambient temperature in the inverter end cap $T_{\mathrm{e,amb}}$ and the motor winding temperature T_{wdg}. The FPGA PCB features an FPGA which performs the actual control based on the measured signals and based on the reference operating point that is obtained via an EtherCAT interface.
The main components on the control PCB are summarised in Tab. 6.3.

6.3 Mechanical Design

Based on the specification of the virtual prototype given in section 6.1, a mechanical CAD model of the complete IMD system is implemented which also includes the 3D models of the inverter PCBs presented in the previous section. An exploded view of the implemented IMD CAD

Table 6.3: Main components on the control PCB. Maximum rated operating temperature $T_{\mathrm{op,max}} \geq 85\,^{\circ}\mathrm{C}$.

Type of component	Number	Name	Description/Ratings
ADC	2	LTC1402IGN#TRPBF	5 V, 12 bit
Isolated DC-DC	1	THN 10-2411WIR	24 V/5 V
Bus transceiver (enable)	2	SN74LVCH16T245DGGR	5 V
FPGA	1	Altera Cyclone V FPGA GX	-

model is shown in Fig. 6.5.
It must be noted that the specification of the virtual prototype includes an insulation layer thickness of zero ($l_{\mathrm{ins}} = 0$ in Tab. 4.10) and a heat sink fin length of zero ($c_{\mathrm{hs}} = 0$ in Tab. 6.1). Hence, the thermal insulation layer and the heat sink fins can be omitted in a system with the considered specification. This is likely due to the relatively low rated power of 1.5 kW. Nevertheless, these components are also shown in Fig. 6.5 to illustrate how a realistic mechanical design with all components of the considered IMD concept looks like.
Fig. 6.6 shows a view into the end cap of the IMD CAD model. This

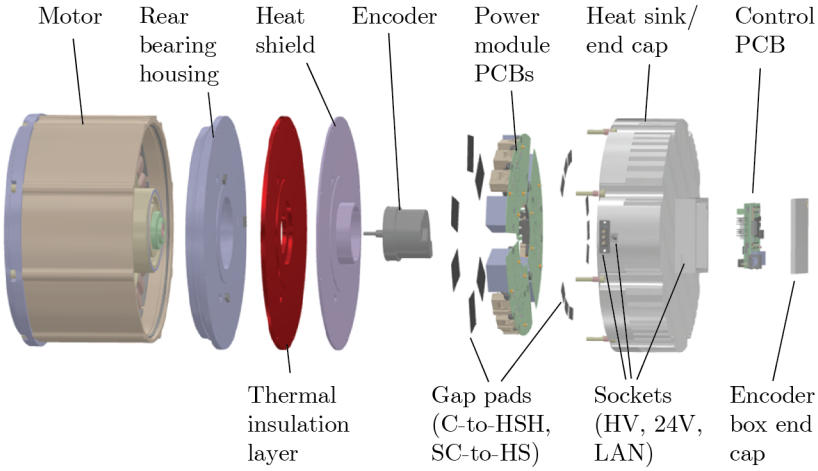


Figure 6.5: Exploded view of the mechanical CAD model of an IMD based on the specification given in section 6.1, extended by a thermal insulation layer and heat sink fins.

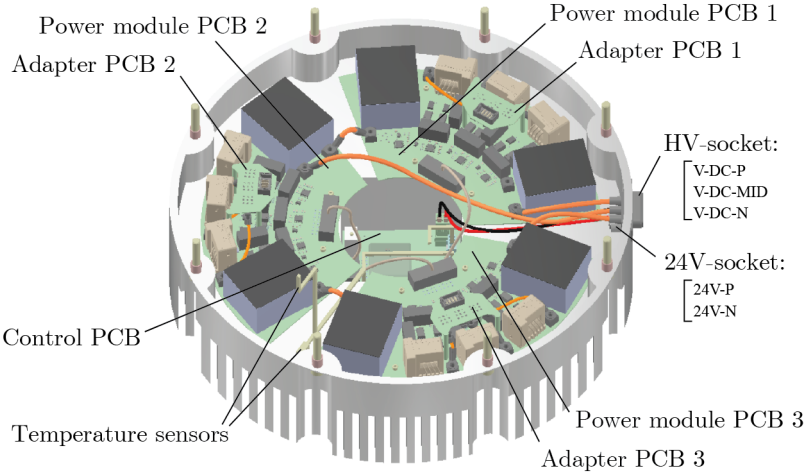


Figure 6.6: View into the end cap of the IMD CAD model from Fig.6.5.

includes all PCBs defined in the equivalent circuit diagram given in Fig. 6.1, i.e. the power module PCBs 1-3, the adapter PCBs 1-3, and the control PCB. In addition, Fig. 6.6 also shows the two temperature sensors for the electronics ambient temperature $T_{\mathrm{e,amb}}$ and for the motor winding temperature T_{wdg}.

7 Conclusion and Outlook

In this chapter, first a conclusion on this thesis is given in section 7.1. Finally, an outlook for future research is given in section 7.2.

7.1 Conclusion

In chapter 2, an overview of existing design concepts for IMDs resulting from a literature research is given, considering thermo-mechanical integration concepts, inverter topologies, PWM schemes, and motor windings. For each of these concept categories, the most relevant concepts are identified, classified, and evaluated with regard to their suitability for an IMD design based on the torque motor introduced in section 1.2. The following conclusions are drawn from this chapter:

- The literature research on thermo-mechanical integration concepts for IMDs has shown a variety of already existing concepts which are classified with regard to the inverter position, the cooling technology, the cooling integration, and the IMD modularity. The evaluation of these concepts results in axial encoder-sided integration with passive cooling and with a thermal insulation layer as the most suitable concept for the considered type of motor.

- An extensive overview of known VSI topologies is presented, in which the VSI topologies are classified as 2L/3L 3Φ inverters, multilevel 3Φ inverters, phase-modular $N_{\mathrm{ph}}\Phi$ inverters, buck-/boost-based 3Φ inverters, and impedance source 3Φ inverters. For the IMD modelling and design, five VSI topologies are selected which

include the standard/non-modular topologies 2L, 3L-NPC, and 3L-TT, and the modular topologies SPB and N_{m}P-2L.

- The presented classification of PWM schemes covers different variants of carrier-based PWM, SVM, and programmed PWM. For the IMD modelling and design, the modulation schemes 2L-SPWM, 2L-OCPWM, 3L-SPWM, and 3L-NPBPWM are selected.

- To include the motor design in the IMD modelling and design, different types of rotating-field stator windings are classified and evaluated based on different criteria such as the coil span, the type of conductor, the number of layers, and the type of winding distribution. Resulting from this evaluation, double-layer tooth-coil windings with round wire conductors are selected for the IMD modelling and design.

In chapter 3, models for the calculation of the target quantities power density, efficiency, cost, and reliability of IMDs are presented. The following conclusions are drawn from this chapter:

- A relatively extensive collection of models for the modelling of IMDs is presented. This includes inverter related models (PWM, DC link dimensioning, semiconductor conduction/switching losses, reliability), motor related models (phase voltages, torque, winding losses, iron losses), and models related to the IMD system level (temperature distribution, system volume, system costs).

- A PWM model is presented which is based on the duty cycle functions from chapter 2.2 of [39], and for which this thesis provides additional explanations on how these functions are derived and how they can be used to calculate the switched inverter output voltages.

- For the DC link dimensioning, analytical models for the capacitor requirements (voltage, capacitance, current capability) are presented. For the required capacitance, the model from section 2.4.1 of [39] is extended to account for voltage-current phase shifts $\phi \neq 0$.

- A semiconductor conduction loss model is presented which is based on the model from [86] and modified so that $R_{\mathrm{ds,on}}$ is scaled with the chip cost.

- A semiconductor switching loss model is presented which is a generalisation of the model from [87] to all considered inverter topologies (2L, 3L-NPC, 3L-TT, SPB, N_{m}P-2L).

- A model for the calculation of the inverter reliability is presented which incorporates all considered inverter topologies.

- A scalable motor model is presented which includes known models (for the motor voltages, the motor torque, and the electrical motor parameters) and a new criterion for the evaluation of slot-pole combinations with regard to the achievable motor-converter-modularity.

- The presented motor winding loss models include 1) a relatively simple model including the skin effect and 2) a more complex model that also incorporates the proximity effect based on an application of the general proximity loss model for round conductors from [99] to double-layer tooth-coil windings.

- With regard to the thermal modelling a lumped parameter based thermal model of the complete IMD and of the finned heat sink/end cap is presented. The latter is also validated in a numerical simulation for exemplary specifications (Tab. 3.42 & Tab. 4.18) with a thermal resistance deviation of $< 5\,\%$.

- Two IMD volume models are presented that are based on mechanical IMD models with different degrees of detail.

- A model for the IMD costs is presented. This includes the component cost model from [141] for the essential inverter components and an estimation of the motor costs based on essential motor parts.

In chapter 4, three design studies are presented, each of which includes a general design procedure for IMDs or for an IMD component and an application of the respective design procedure to exemplary system specifications of a 1.5 kW high-torque low-speed IMD. The following conclusions are drawn from these design studies:

- *Design study based on the general IMD design procedure IMD-Design-Proc-1 (Fig. 4.2)*

  - In this design study, the SPB-C combined with a 3-, 6-, 9-, or 12-phase tooth-coil wound non-salient PMSM is analysed and compared based on the general "2D-optimisation" procedure *IMD-Design-Proc-1* for the optimal design of IMDs in terms of power density and efficiency.
  - The results of the design procedure application show that the winding factors of the proposed 6-, 9-, and 12-phase (multiphase) motors are on average 3.7 % higher than the winding factors of 3-phase motors with 2, 3, or 4 phase-aligned winding systems. The higher winding factor can be used to increase the maximum efficiency by 0.70 % or the maximum power density by 3.8 %.
  - Furthermore, the possible motor-converter modularity is analyzed. As a result, 3-phase motors allow a higher degree of motor-converter modularity compared to multiphase motors.

- *Design study based on the general IMD design procedure IMD-Design-Proc-2 (Fig. 4.6)*
  - With *IMD-Design-Proc-2*, a general "3D-optimisation" procedure for the optimal design of IMDs in terms of power density, efficiency, and cost is presented. This procedure enables the comparison of modular converter topologies (2L3Mser/2L3Mpar) to standard/non-modular topologies (2L/3LNPC/3LTT) covering a large design space including different PWM variants, semiconductor technologies (Si/SiC/GaN), and winding schemes.
  - The results of the design procedure application are analysed in terms of 3D-pareto-fronts, showing that the cost-optimal system configuration is 2L-OC-Si-3ph. Compared to this, the suggested design has the configuration 2L3Mpar-OC-GaN-9ph and enables an efficiency increase of +2.26 % at 36 % higher cost. Assuming a utilization of 90 % and an energy price of 0.1 CHF/kWh, the higher costs are compensated by the lower energy consumption after approximately 2 years.
  - The results of the design procedure application are further analysed to compare the considered topologies, PWM schemes, and semiconductor technologies with regard to maximum efficiency at equal system cost and volume. As a result, modular topologies reach higher efficiencies than the

standard topologies due to the general advantage that modular topologies can be combined with multiphase windings. The optimal PWM scheme and the optimal semiconductor technology cannot be predicted in general, as they depend on the system specification, such as the torque ripple constraint.

- *Design study based on the general heat sink/end cap design procedure HS-Design-Proc (Fig. 4.11)*
  - With *HS-Design-Proc*, a procedure for the optimal heat sink design is presented which results in the passive cooling limit in terms of the $CSPI$. This heat sink design procedure can be used by system designers to determine whether passive cooling with a finned heat sink is sufficient for a realistic heat sink volume or whether a different cooling system with a higher $CSPI$ (e.g. using liquid cooling) is required.
  - The design procedure application results in a $CSPI$-range of $0.67..1.8\,\mathrm{W\,K^{-1}\,L^{-1}}$. This relatively low $CSPI$-range requires rather high diameter to power ratios. Such ratios are characteristic for high-torque, low-speed motors and loads which therefore should be the primary "target-group" for passively cooled IMDs.

In chapter 5, the control of IMDs consisting of an SPB-C and a 9-phase PMSM is investigated. The following conclusions are drawn from this chapter:

- A control concept for drive systems consisting of a symmetrical 9-phase PMSM connected to an SPB-C via a cable with the impedance (R_b, L_b) is presented. The concept is based on [11], adapted to PMSMs, and extended by introducing the cable impedance that represents a source impedance of the DC source.
- For taking this source impedance into account, the appropriate choice for the module DC link voltage reference is found to be $v_\Sigma/3$. This choice leads to a voltage controller only acting on the balancing of the DC link module voltages, independently of fluctuations of the total DC link voltage (v_Σ) during for example load steps.
- The total DC link voltage is kept stable via sufficiently large DC link capacitors. Controlling also the total DC link voltage

is theoretically possible with an additional voltage controller in the torque producing current subspace. However, such total DC link voltage control is not considered practically useful due to its high bandwidth requirement and due to an additionally resulting torque ripple.

- The stability analysis of the module DC link voltages leads to a stability condition on the high frequency gain of the DC link balancing controller. Taking the stability condition for the gain into account, the controllers of the proposed concept are tuned in the frequency domain based on the assumption/condition of sufficiently large frequency intervals between the bandwidths of the involved control loops.
- Using the resulting controller parameters, the complete control concept is validated in a simulation for exemplary system specifications (Tab. 5.1) with a 1.5 kW high-torque low-speed PMSM.

In chapter 6, a virtual prototype of an IMD based on an SPB-inverter and a 1.5 kW high-torque low-speed PMSM is presented. The following conclusions are drawn from this chapter:

- For the virtual prototype, a design of inverter PCBs and a mechanical CAD model of the overall IMD system are presented which are based on the results of the design study from section 4.2.
- The virtual prototype shows that the design procedure used in the design study (*IMD-Design-Proc-2*) leads to a realistic prototype design.

7.2 Outlook

The following topics could be considered in future research:

- *Motor winding insulation and* $\mathrm{d}v/\mathrm{d}t$*-filter*: The presented IMD design procedures do not take any reinforced motor insulation or $\mathrm{d}v/\mathrm{d}t$-filter into account, which has a negative impact on the lifetime of the insulation when fast switching WBG devices are used. Therefore, future research should include the development of design procedures for the optimal design of the motor insulation and/or $\mathrm{d}v/\mathrm{d}t$-filters.

- *Physical iron loss modelling*: In this thesis, an improved iron loss density model is presented which is based on measurements and hence still of empirical nature. A potential future research topic is to develop a physical iron loss model that can predict losses in silicon steel based on physical (instead of empirical) properties of the material. This probably requires a look into the material structure on a level of grains/molecules/atoms in order to identify the "material state variables" that are relevant for the iron loss density calculation. A related potential research topic in the field of mechanical engineering is to adapt/develop the production processes for silicon steel so that these material state variables can be set with the parameters of the production process. This would avoid the need of silicon steel characterisation based on iron loss measurements for a large number of operating points. Given that the iron losses depend on a relatively large number of operating point parameters (harmonics, minor hysteresis loops, DC-offset, field rotation, relaxation, etc.), a material characterisation for all operating points based on loss measurements is relatively "costly" in terms of money and time. If the material can instead be characterised based on few fundamental physical properties, the "cost" of iron loss modelling could be reduced.

- *Prototype*: A real prototype could be built based on the virtual prototype presented in this thesis. Such a prototype could for example be used to provide a measurement based validation of the presented control concept.

A

Transformation Matrices Required for the Presented Control Concept

In this section, the transformation matrices presented in [11] are summarised which are required for the control concept described in chapter 5. These transformation matrices are used to transform any voltage/current vector $\boldsymbol{x}_\gamma$ in a given vector space, referred to as γ, into the voltage/current vector $\boldsymbol{x}_\nu$ in a different vector space, referred to as ν. The general transformation is given by $\boldsymbol{x}_\nu = \boldsymbol{T}_{\gamma-\nu} \cdot \boldsymbol{x}_\gamma$. There, $\boldsymbol{T}_{\gamma-\nu}$ is the transformation matrix from vector space γ to vector space ν. The vector spaces γ and ν can be any of the vector spaces introduced in section 5.1.3, i.e. $\gamma, \nu = \{\text{abc}, \text{VSD}, \text{dqVSD}, \text{abc1}, \text{MS}, \text{dqMS}\}$.
The abc-to-VSD transformation matrix is given by

$$\boldsymbol{T}_{\mathbf{abc-VSD}} = \frac{2}{9} \begin{bmatrix} & \cos(\boldsymbol{\theta}_\mathbf{s}) & \\ & \sin(\boldsymbol{\theta}_\mathbf{s}) & \\ & \cos(2\boldsymbol{\theta}_\mathbf{s}) & \\ & \sin(2\boldsymbol{\theta}_\mathbf{s}) & \\ & \cos(4\boldsymbol{\theta}_\mathbf{s}) & \\ & \sin(4\boldsymbol{\theta}_\mathbf{s}) & \\ {}^3\!/_2\boldsymbol{I}_\mathbf{3} & {}^3\!/_2\boldsymbol{I}_\mathbf{3} & {}^3\!/_2\boldsymbol{I}_\mathbf{3} \end{bmatrix} \tag{A.1}$$

where $\boldsymbol{I}_\mathbf{3}$ is the identity matrix with 3 rows/columns and $\boldsymbol{\theta}_\mathbf{s}$ is the vector of the winding axes angles of a symmetrical nine-phase motor given by

$$\boldsymbol{\theta}_\mathbf{s} = \frac{2\pi}{9} \begin{bmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 \end{bmatrix}. \tag{A.2}$$

The VSD-to-dqVSD transformation matrix is given by

$$\boldsymbol{T}_{\mathbf{VSD-dqVSD}} = \begin{bmatrix} \boldsymbol{T}_{\mathbf{R}}(-\theta_{\mathrm{e}}) & \mathbf{0} & \cdots & \mathbf{0} \\ \mathbf{0} & \boldsymbol{T}_{\mathbf{R}}(+\theta_{\mathrm{e}}) & \mathbf{0} & \vdots \\ \vdots & \mathbf{0} & \boldsymbol{T}_{\mathbf{R}}(-\theta_{\mathrm{e}}) & \mathbf{0} \\ \mathbf{0} & \cdots & \mathbf{0} & \boldsymbol{I}_{\mathbf{3}} \end{bmatrix} \tag{A.3}$$

where $\boldsymbol{T}_{\mathbf{R}}(\theta_{\mathrm{e}})$ is the standard rotation matrix given by

$$\boldsymbol{T}_{\mathbf{R}}(\theta_{\mathrm{e}}) = \begin{bmatrix} \cos(\theta_{\mathrm{e}}) & -\sin(\theta_{\mathrm{e}}) \\ \sin(\theta_{\mathrm{e}}) & \cos(\theta_{\mathrm{e}}) \end{bmatrix}. \tag{A.4}$$

The abc-to-abc1 transformation matrix is given by

$$\boldsymbol{T}_{\mathbf{abc-abc1}} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{A.5}$$

which corresponds to a reordering of phases based on the grouping into three-phase winding systems.
The abc1-to-MS transformation matrix is given by

$$\boldsymbol{T}_{\mathbf{abc1-MS}} = \begin{bmatrix} \boldsymbol{C}(\alpha = 0) & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \boldsymbol{C}(\alpha = \frac{2\pi}{9}) & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \boldsymbol{C}(\alpha = \frac{4\pi}{9}) \end{bmatrix} \tag{A.6}$$

where $\boldsymbol{C}(\alpha)$ is a generalised form of the Clarke transformation given by

$$\boldsymbol{C}(\alpha) = \frac{2}{3} \begin{bmatrix} \cos(\alpha) & \cos(\alpha + \frac{2\pi}{3}) & \cos(\alpha + \frac{4\pi}{3}) \\ \sin(\alpha) & \sin(\alpha + \frac{2\pi}{3}) & \sin(\alpha + \frac{4\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}. \tag{A.7}$$

The MS-to-dqMS transformation matrix is given by

$$\boldsymbol{T}_{\mathbf{MS-dqMS}} = \begin{bmatrix} \boldsymbol{T}_{\mathbf{dq}}(\theta_{\mathrm{e}}) & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \boldsymbol{T}_{\mathbf{dq}}(\theta_{\mathrm{e}}) & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \boldsymbol{T}_{\mathbf{dq}}(\theta_{\mathrm{e}}) \end{bmatrix} \tag{A.8}$$

where $\boldsymbol{T}_{\mathbf{dq}}(\theta_{\mathrm{e}})$ is given by

$$\boldsymbol{T}_{\mathbf{dq}}(\theta_{\mathrm{e}}) = \begin{bmatrix} \cos(\theta_{\mathrm{e}}) & \sin(\theta_{\mathrm{e}}) & 0 \\ -\sin(\theta_{\mathrm{e}}) & \cos(\theta_{\mathrm{e}}) & 0 \\ 0 & 0 & 1 \end{bmatrix}. \tag{A.9}$$

B

Iron loss density model parameters and measurement results

In this section, the model parameters of the iron loss density model M2LSE5+BPG introduced in section 3.8.3 are given for the electrical steel sheet types from Tab. B.1. Furthermore, a comparison between the measured and the model-predicted iron loss density curves is shown. The presented model parameters result from a parameter fitting to the results of the measurement series Meas-STx which includes measurements with a sinusoidal excitation (MeasSin-STx) and measurements with a DC-biased excitation (MeasSinDC-STx).
Each of the following sections contains the following data related to one sheet type:

Table B.1: Grades of the electrical steel sheet types (ST) considered in this section.

x: ST-ID	Grade
3	M330-35A
4	M235-35A
5	M270-50A
6	M400-50AP
7	M530-50A
8	M800-50A
9	NO10
10	NO20-15

- Model parameters of the iron loss density model M2LSE5+BPG:
  - Table with the frequency-dependent loss coefficients $K_{\mathrm{h},0}(f)$, $K_{\mathrm{c},0}(f)$, $K_{\mathrm{e},0}(f)$, and $K_{\alpha,0}(f)$
  - Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients $K_{\mathrm{h,dc}}(H_{\mathrm{dc}})$, $K_{\mathrm{c,dc}}(H_{\mathrm{dc}})$, and $K_{\mathrm{e,dc}}(H_{\mathrm{dc}})$
  - BH-curve at low-frequency (50 Hz) required to obtain H_{dc} from B_{dc}
- Comparison of measured and model-predicted iron loss density curves, i.e. the fitting quality:
  - For sinusoidal excitation based on the results of the measurement series MeasSin-STx
  - For DC-biased excitation based on the results of the measurement series MeasSinDC-STx

B.1 Sheet type 3 (M330-35A)

Table B.2: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST3.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	1.5242e-2	4.8467e-5	7.6085e-4	3
IC_2	1500	9000	5.9665e-2	2.104e-5	4.9798e-4	1.9904
IC_3	10000	100000	2.0301e-1	1.1051e-5	7.4585e-5	1.835

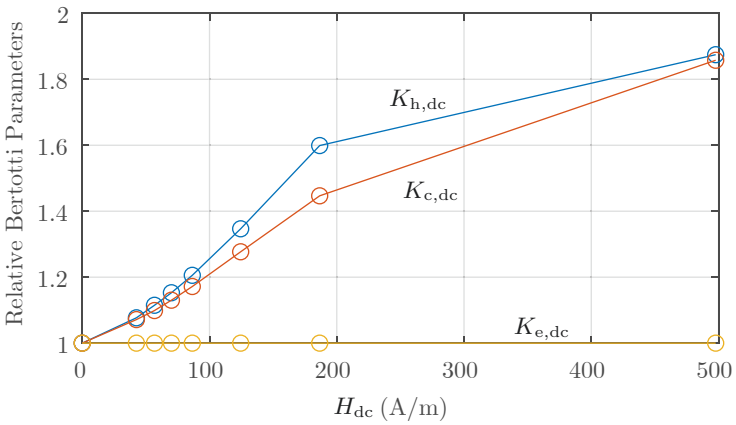


Figure B.1: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST3.

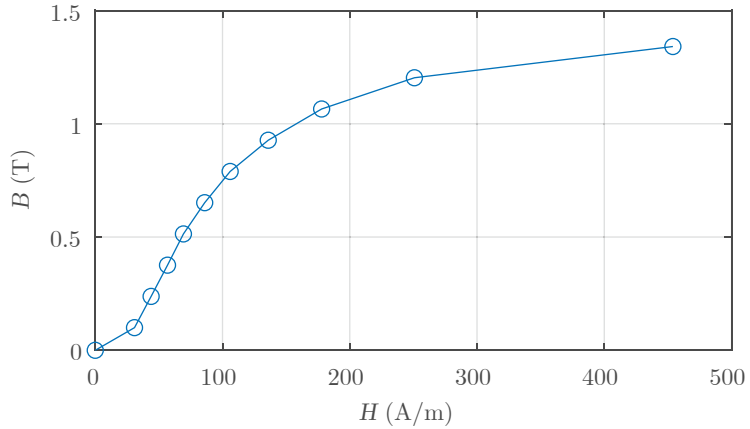


Figure B.2: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST3.

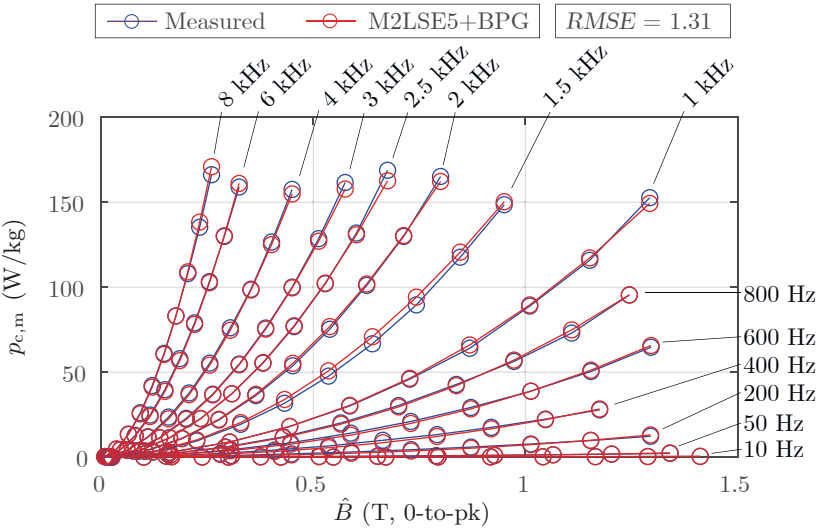


Figure B.3: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST3.

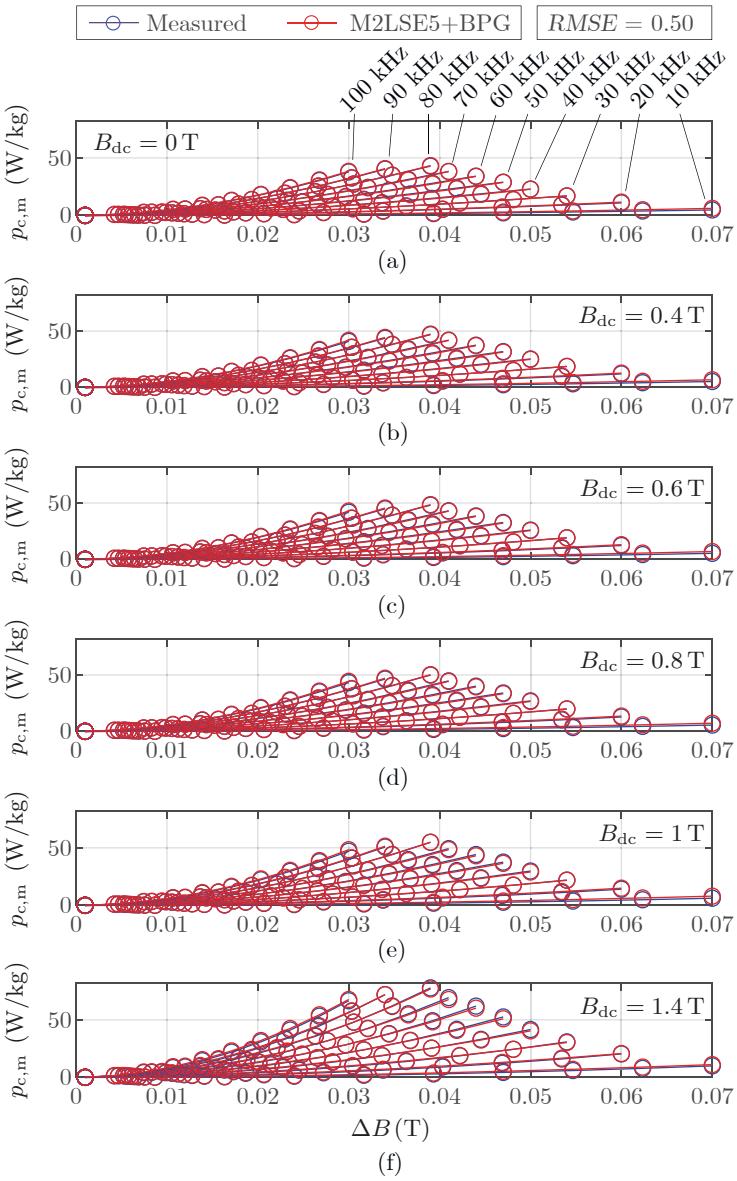


Figure B.4: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST3.

B.2 Sheet type 4 (M235-35A)

Table B.3: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST4.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	1.4078e-2	3.6914e-5	8.6025e-4	3
IC_2	1500	9000	5.7485e-2	2.0435e-5	3.0176e-4	1.969
IC_3	10000	100000	3.6616e-1	9.0315e-6	1.1289e-4	2.0527

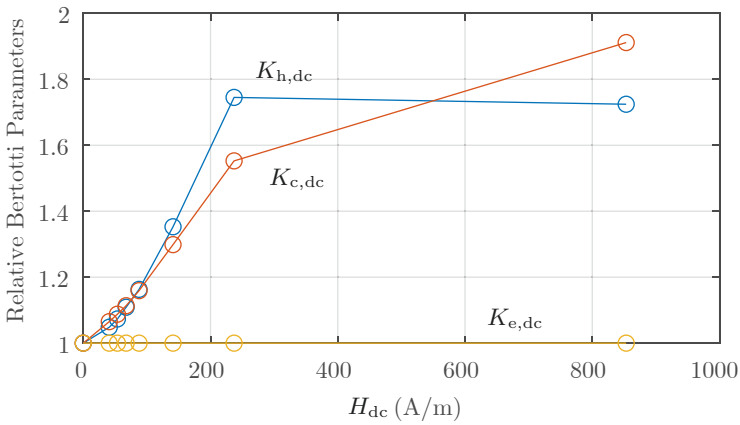


Figure B.5: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST4.

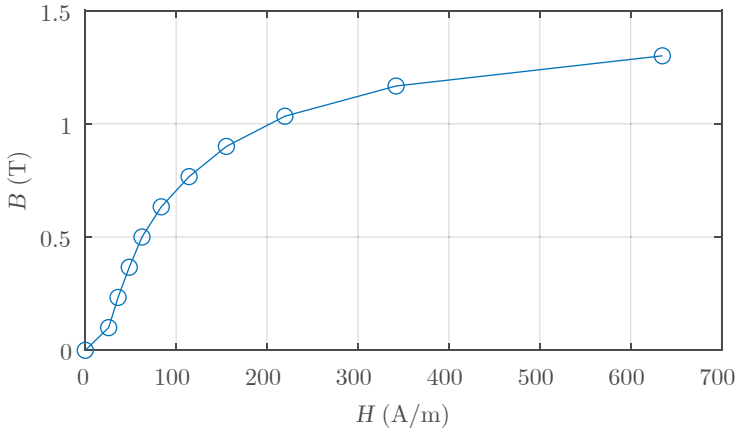


Figure B.6: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST4.

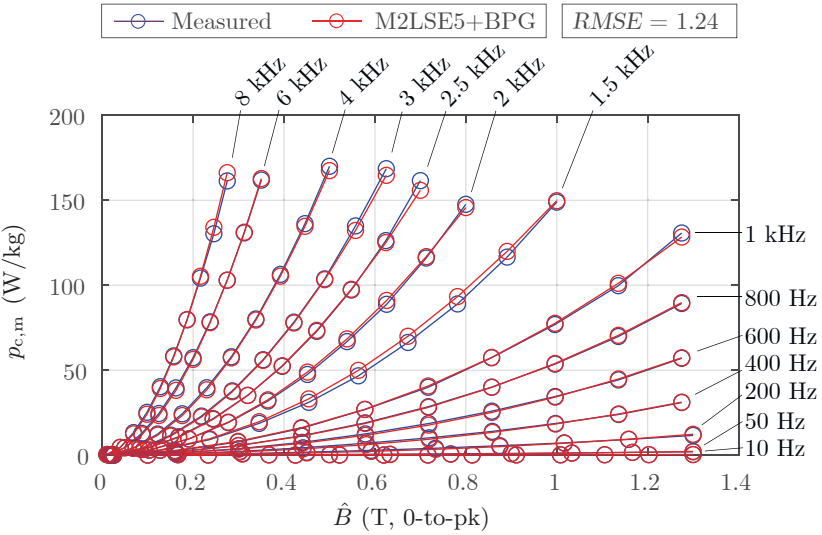


Figure B.7: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST4.

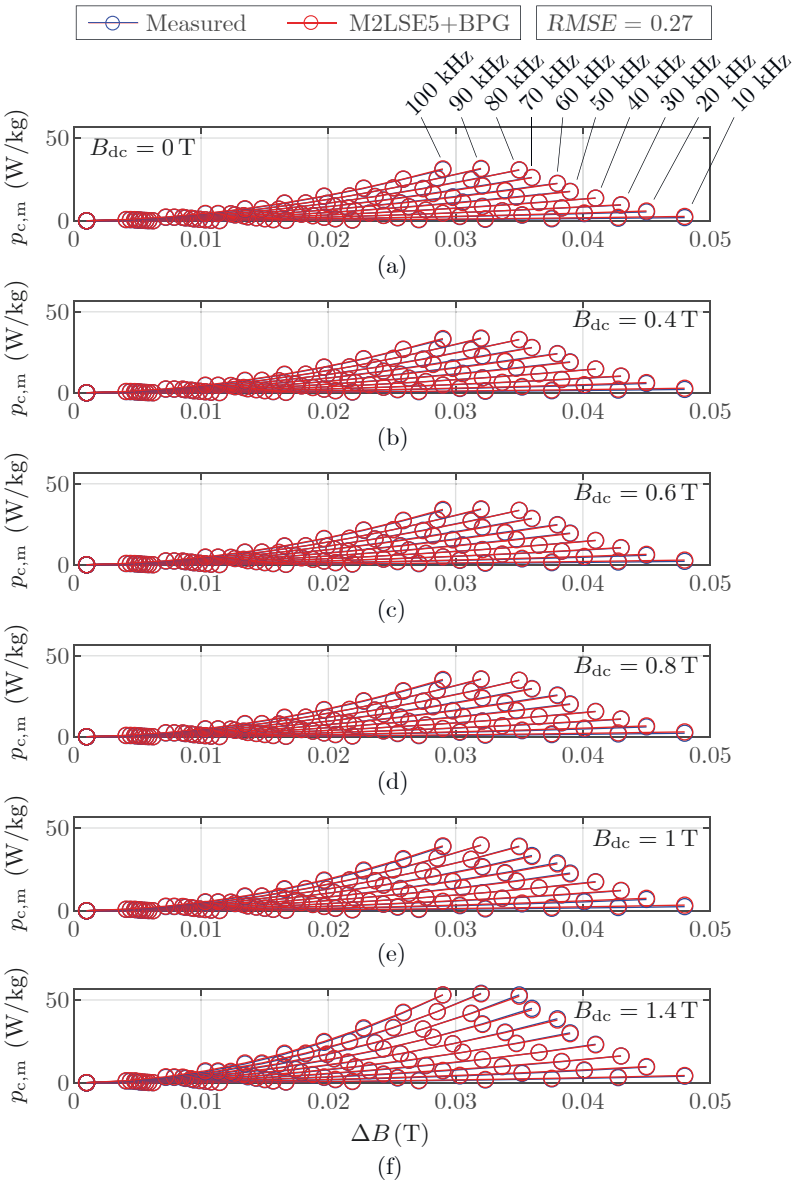


Figure B.8: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST4.

B.3 Sheet type 5 (M270-50A)

Table B.4: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST5.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	2.4109e-2	9.39e-5	1.7871e-4	3
IC_2	1500	9000	8.8541e-2	3.0177e-5	5.4104e-4	2.1309
IC_3	10000	100000	3.1258e-1	2.1775e-5	1.0651e-4	1.796

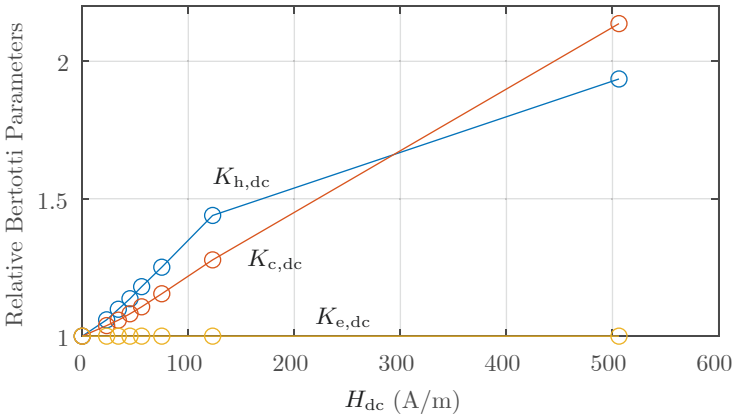


Figure B.9: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST5.

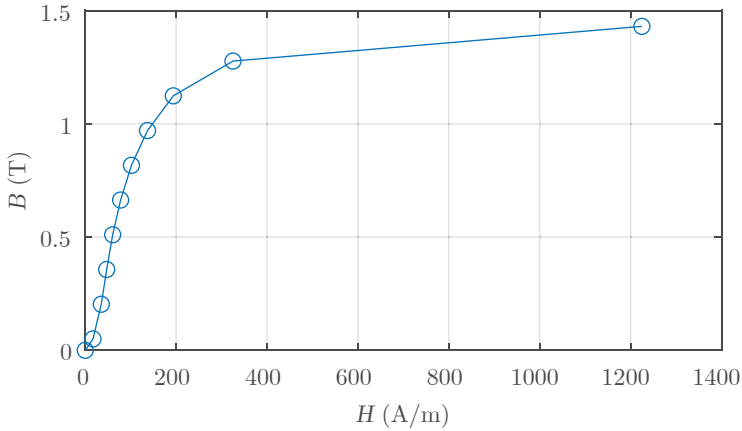


Figure B.10: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST5.

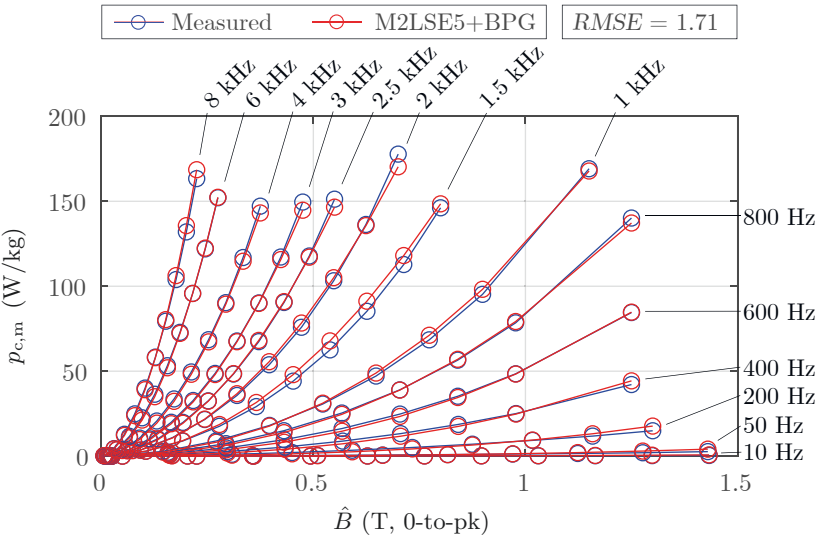


Figure B.11: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST5.

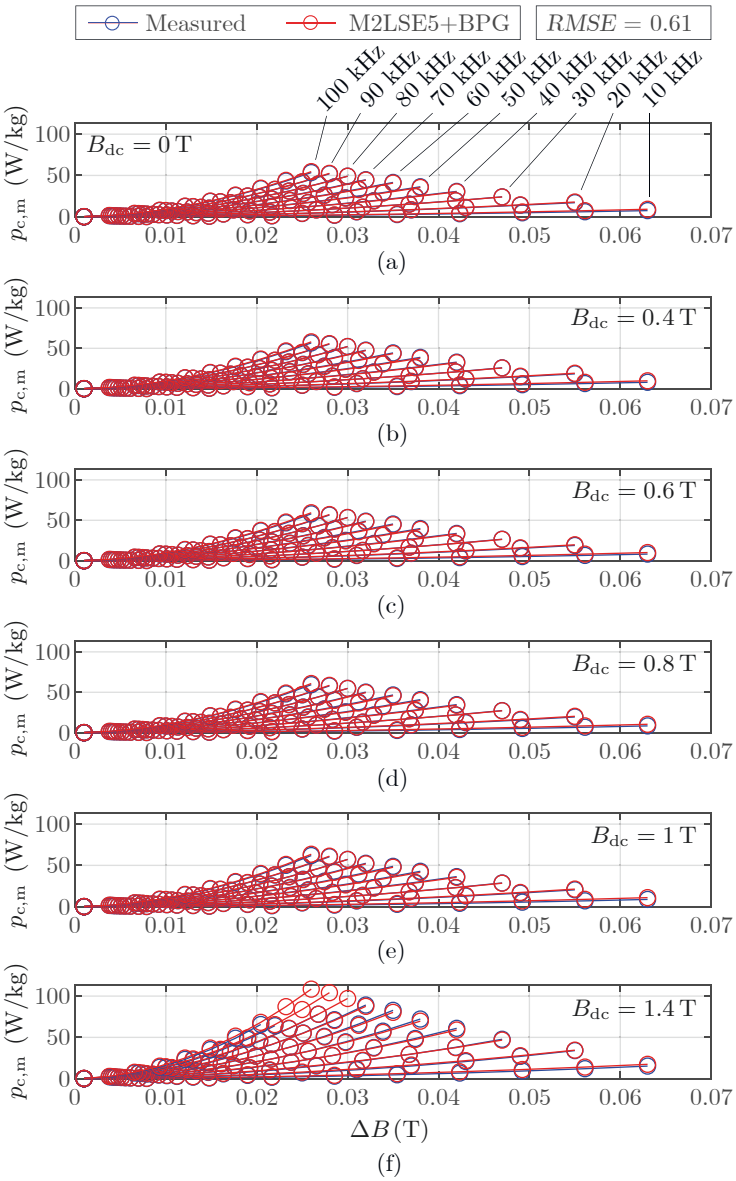


Figure B.12: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST5.

B.4 Sheet type 6 (M400-50AP)

Table B.5: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST6.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	3.7416e-2	1.3374e-4	2.4999e-4	3
IC_2	1500	9000	1.1796e-1	3.7479e-5	9.5249e-4	2.1146
IC_3	10000	100000	5.3748e-1	3.518e-5	1.4822e-4	1.8229

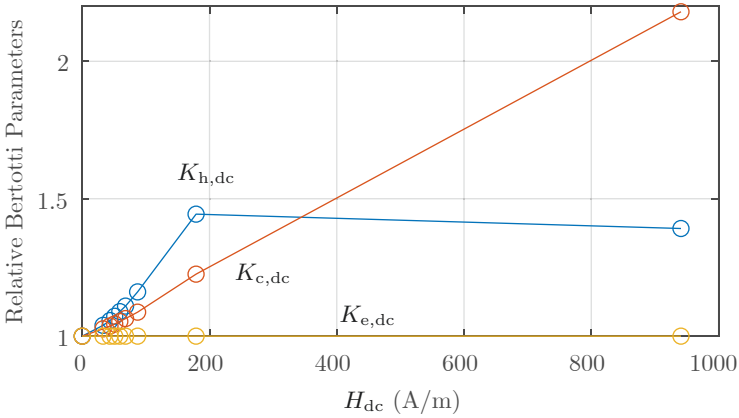


Figure B.13: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST6.

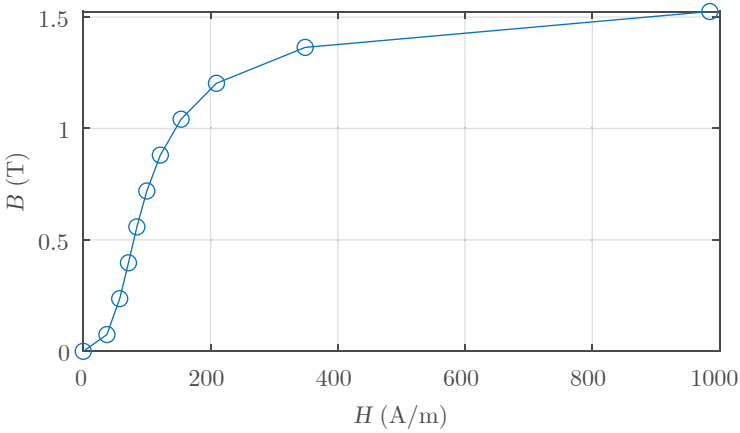


Figure B.14: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST6.

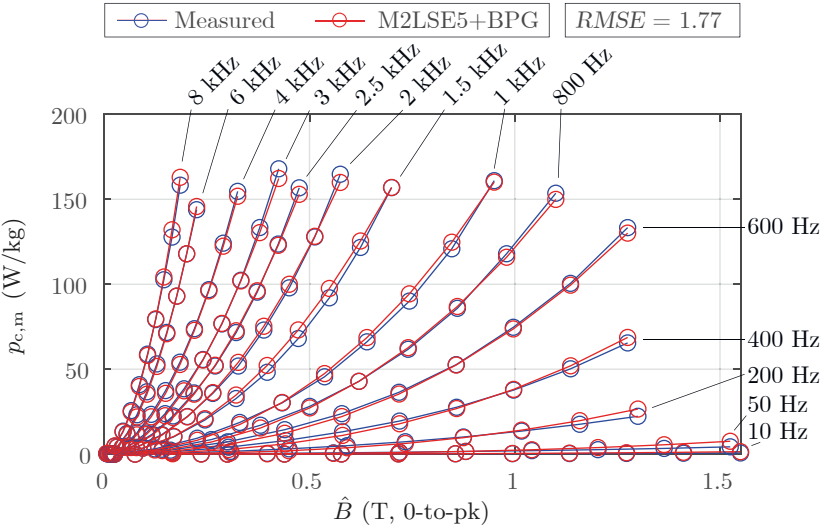


Figure B.15: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST6.

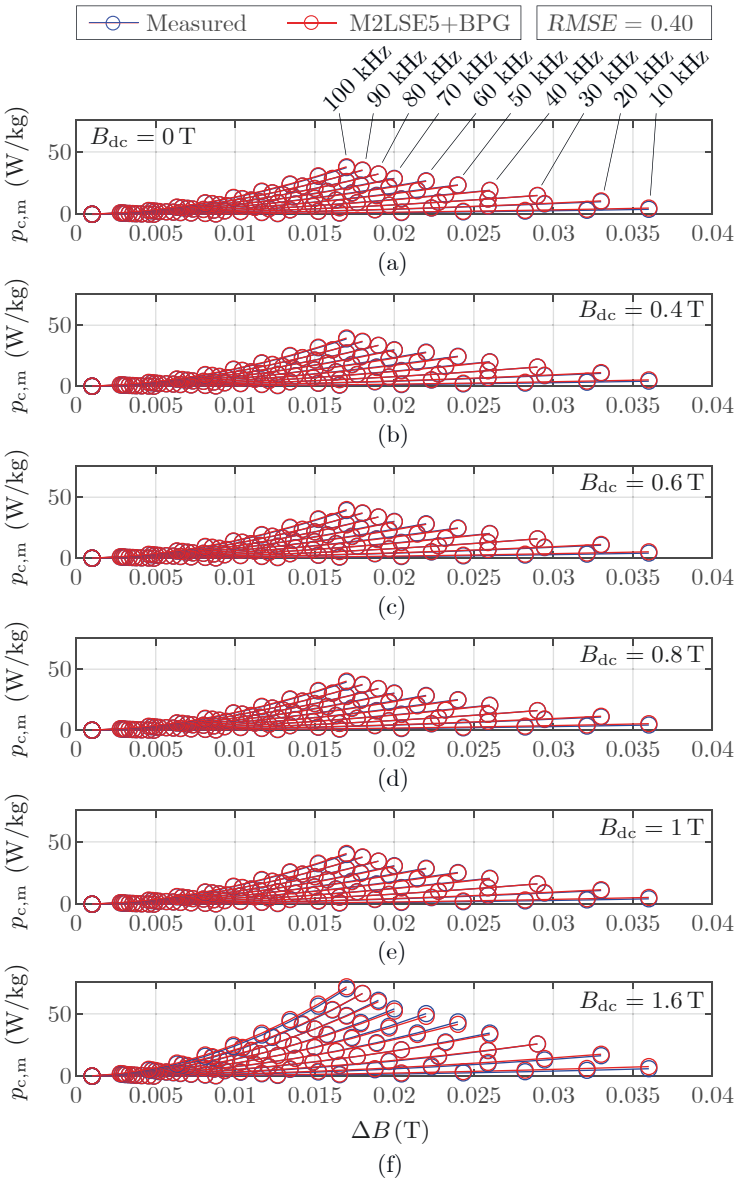


Figure B.16: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST6.

B.5 Sheet type 7 (M530-50A)

Table B.6: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST7.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	4.4671e-2	1.5298e-4	2.2204e-14	3
IC_2	1500	9000	1.3816e-1	3.7941e-5	9.0806e-4	2.1733
IC_3	10000	100000	2.5469e-1	1.7583e-5	1.8442e-4	1.8033

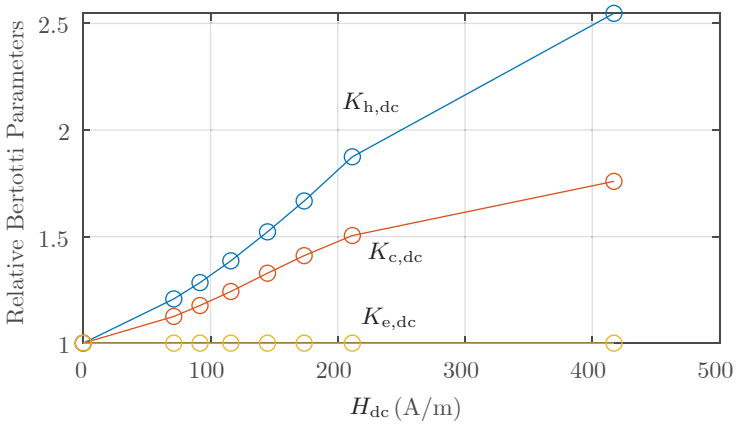


Figure B.17: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST7.

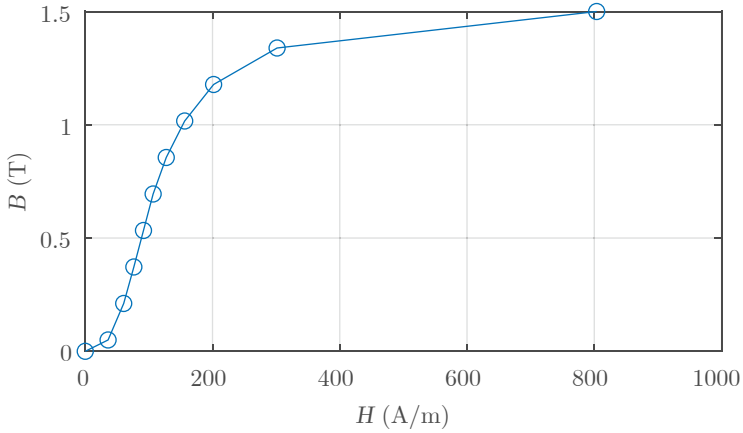


Figure B.18: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST7.

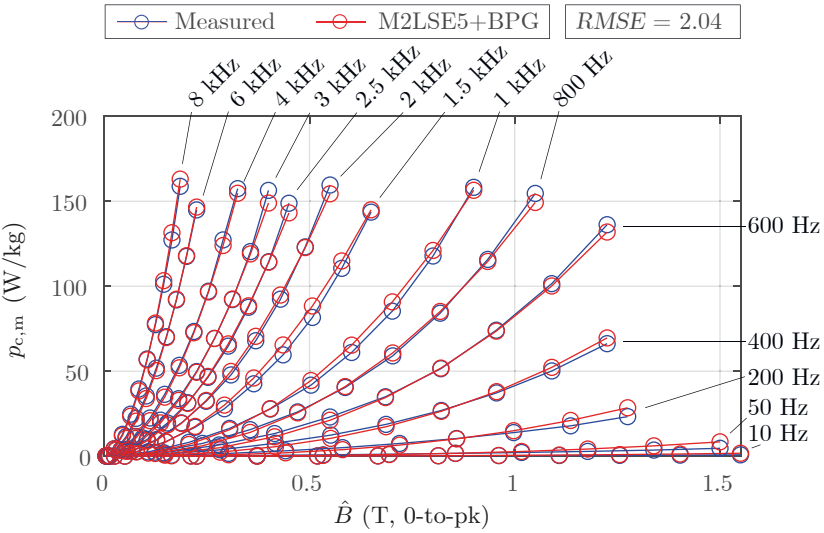


Figure B.19: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST7.

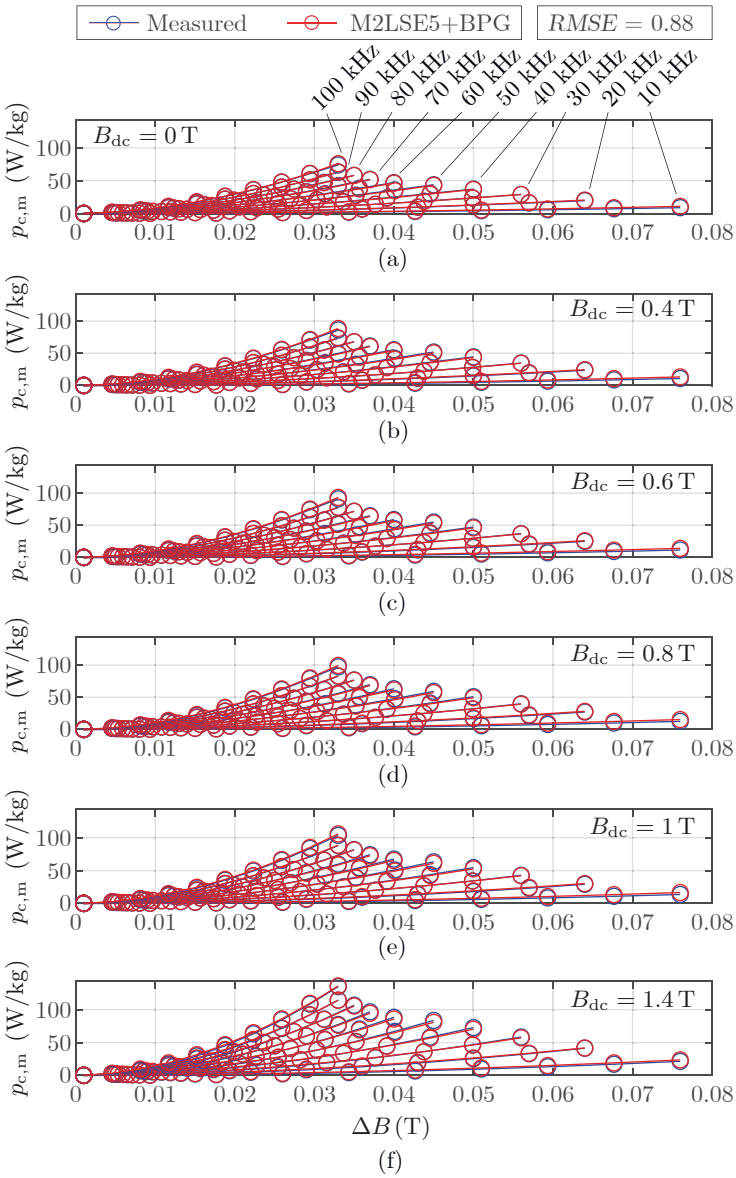


Figure B.20: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST7.

B.6 Sheet type 8 (M800-50A)

Table B.7: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST8.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	4.622e-2	1.5028e-4	3.2116e-5	3
IC_2	1500	9000	1.346e-1	4.2571e-5	8.3456e-4	2.1602
IC_3	10000	100000	2.5331e-1	3.4683e-5	3.7602e-9	1.6477

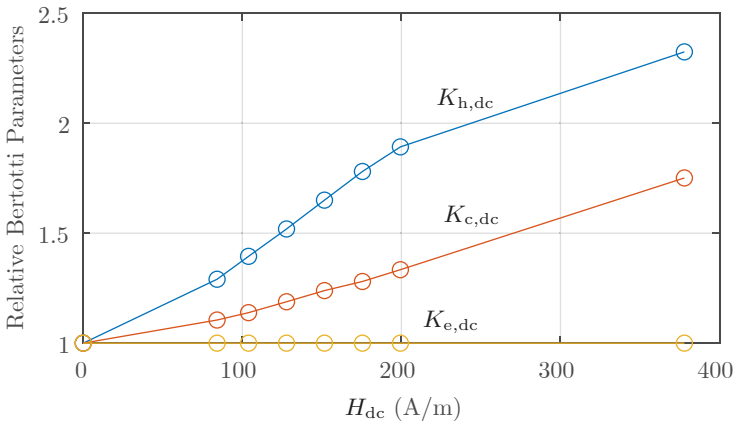


Figure B.21: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST8.

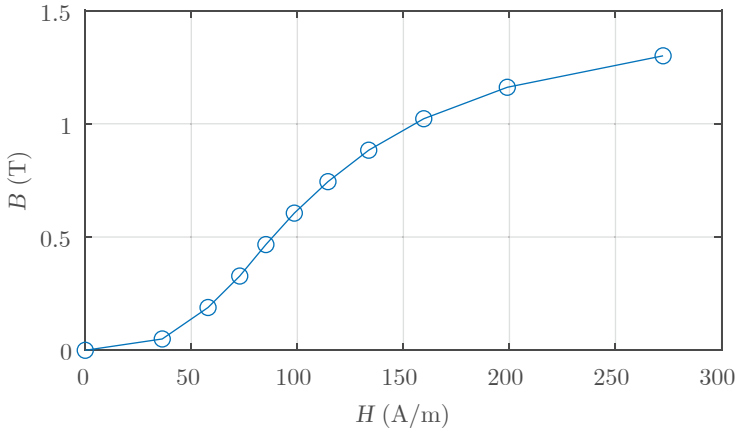


Figure B.22: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST8.

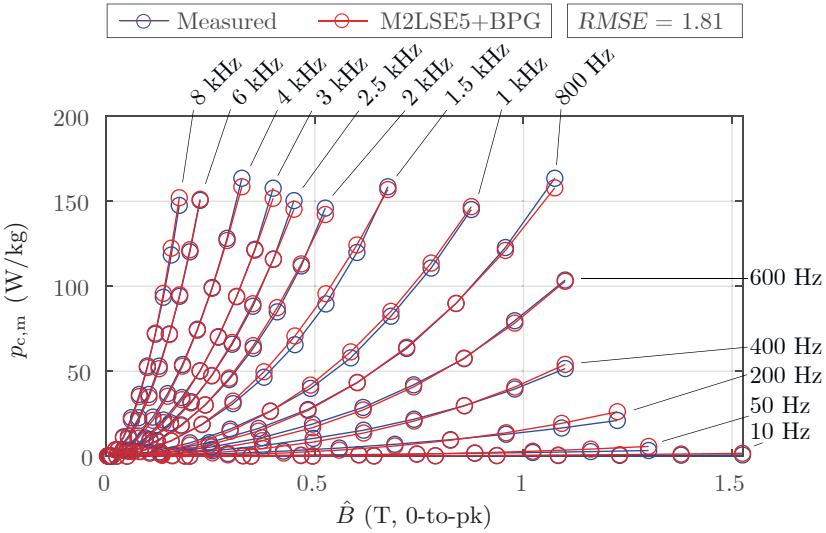


Figure B.23: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST8.

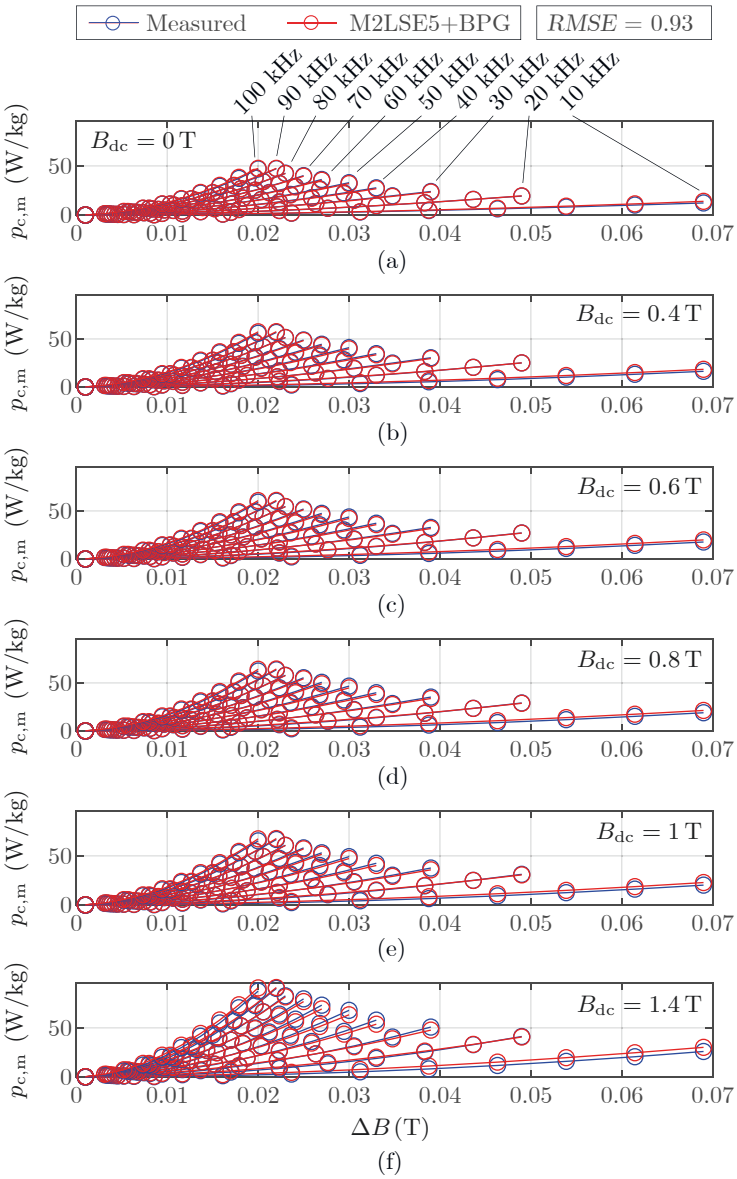


Figure B.24: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST8.

B.7 Sheet type 9 (NO10)

Table B.8: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST9.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	1.9779e-2	2.0182e-9	6.113e-4	2.5448
IC_2	1500	9000	2.5913e-2	4.9787e-6	2.7897e-4	2.0959
IC_3	10000	100000	5.2774e-2	1.0639e-6	1.4936e-5	2.23

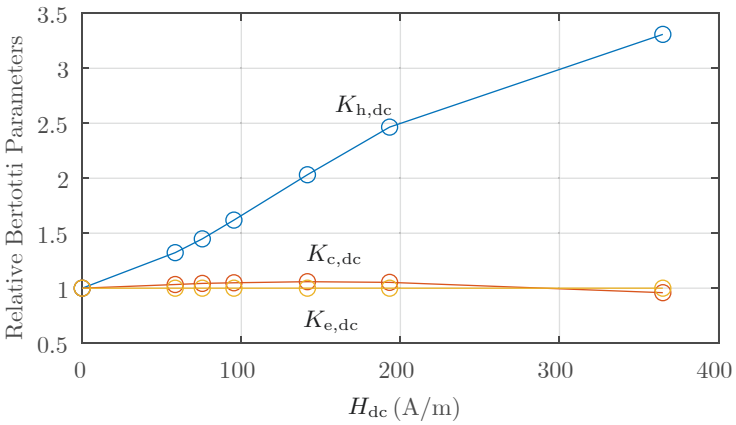


Figure B.25: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST9.

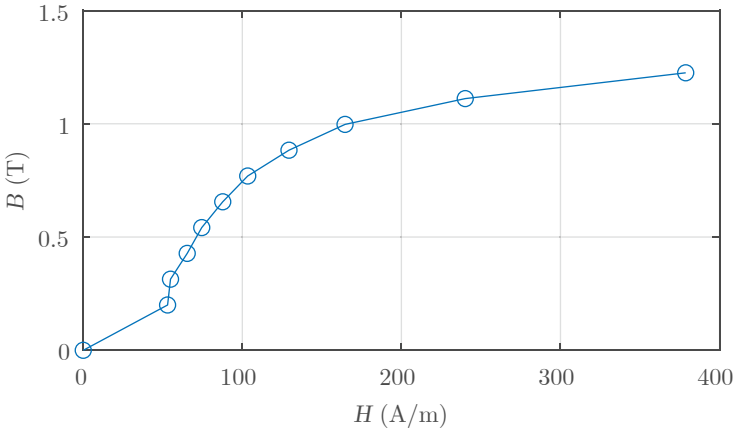


Figure B.26: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST9.

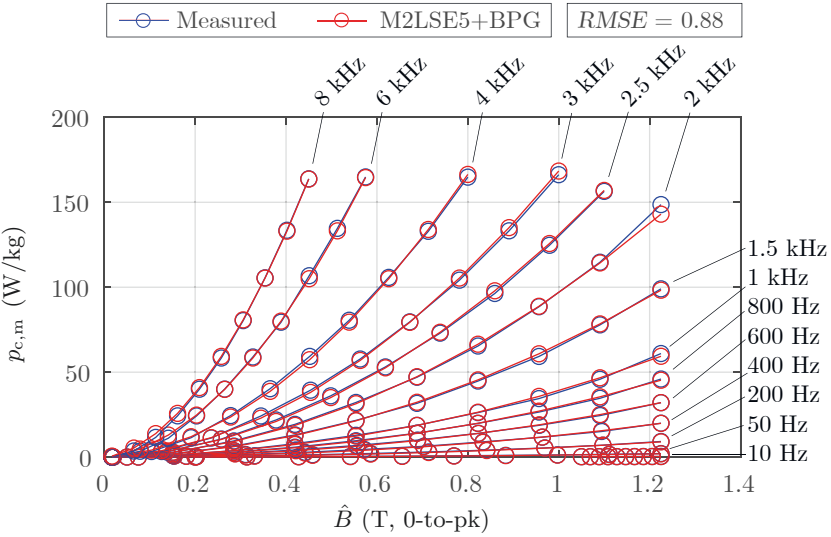


Figure B.27: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST9.

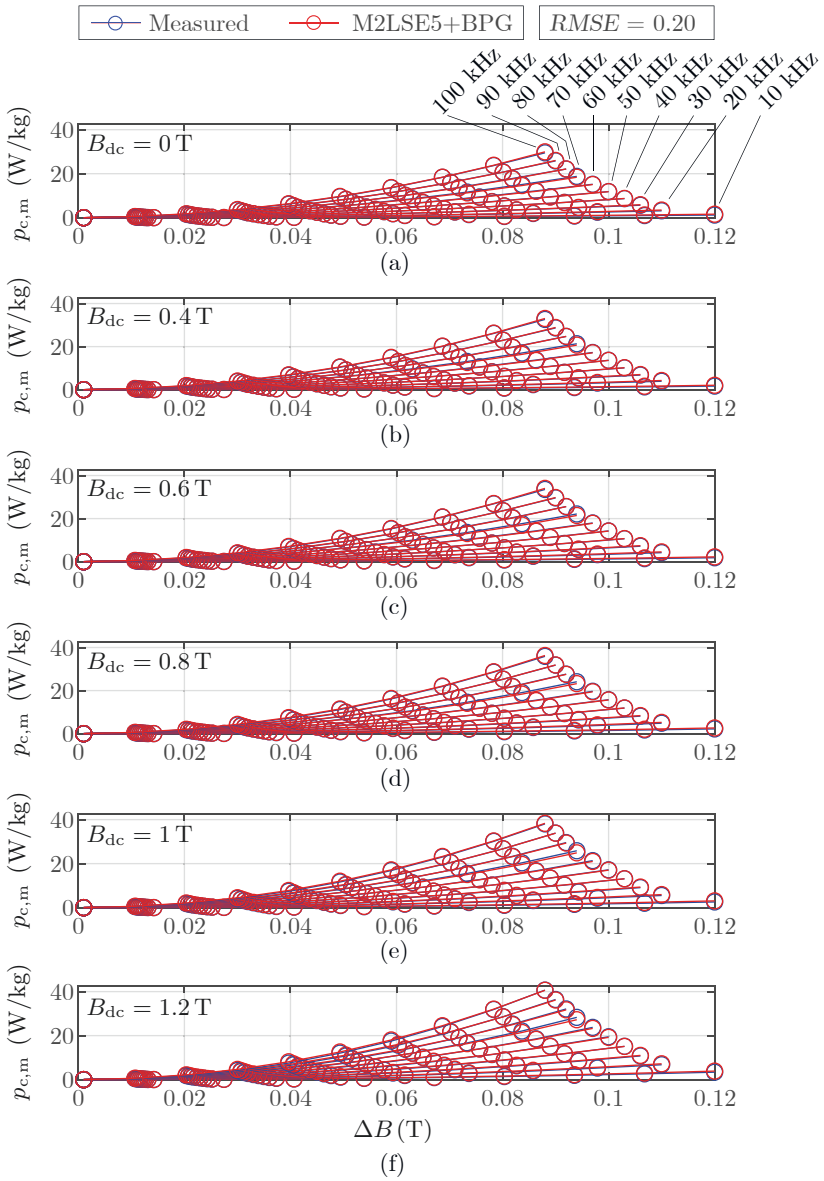


Figure B.28: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST9.

B.8 Sheet type 10 (NO20-15)

Table B.9: Frequency-dependent loss coefficients for iron loss density model M2LSE5+BPG, resulting from the measurement series Meas-ST10.

Interval	$f_{\mathrm{IC}_j,\mathrm{LB}}$ (Hz)	$f_{\mathrm{IC}_j,\mathrm{UB}}$ (Hz)	$K_{\mathrm{h},0,\mathrm{IC}_j}$	$K_{\mathrm{c},0,\mathrm{IC}_j}$	$K_{\mathrm{e},0,\mathrm{IC}_j}$	$K_{\alpha,0,\mathrm{IC}_j}$
IC_1	10	1000	1.7327e-2	1.1767e-5	7.0329e-4	2.3231
IC_2	1500	9000	3.4114e-2	1.1995e-5	3.0023e-4	1.9202
IC_3	10000	100000	2.0681e-1	3.9703e-6	6.7894e-5	2.1977

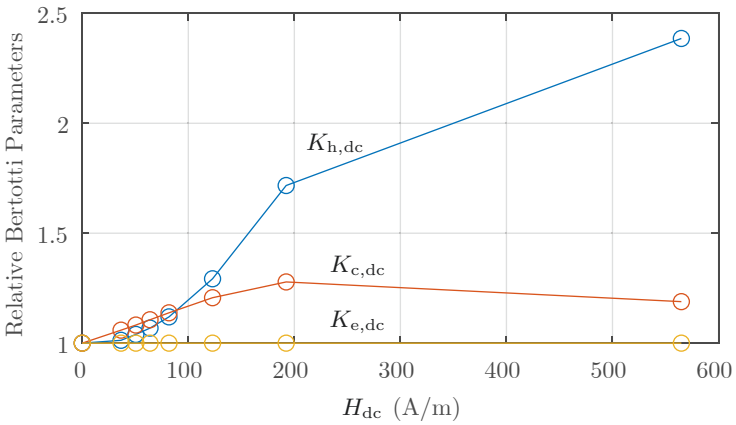


Figure B.29: Bertotti Premagnetisation Graph (BPG) showing the DC bias-dependent loss coefficients of iron loss density model M2LSE5+BPG, resulting from Meas-ST10.

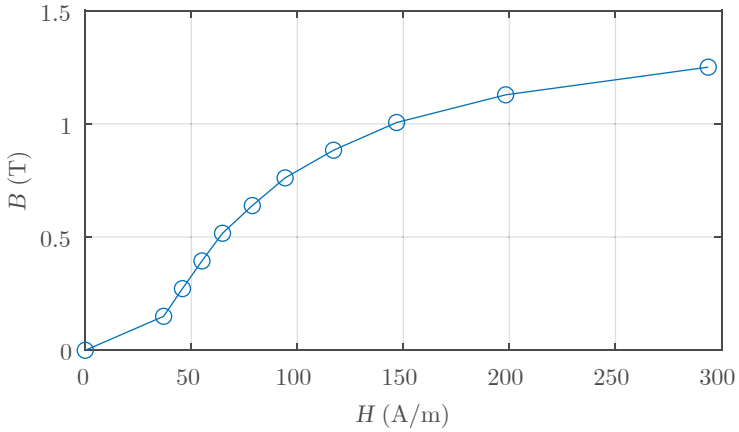


Figure B.30: BH-curve at 50 Hz required for iron loss density model M2LSE5+BPG to obtain H_{dc} from B_{dc}, resulting from Meas-ST10.

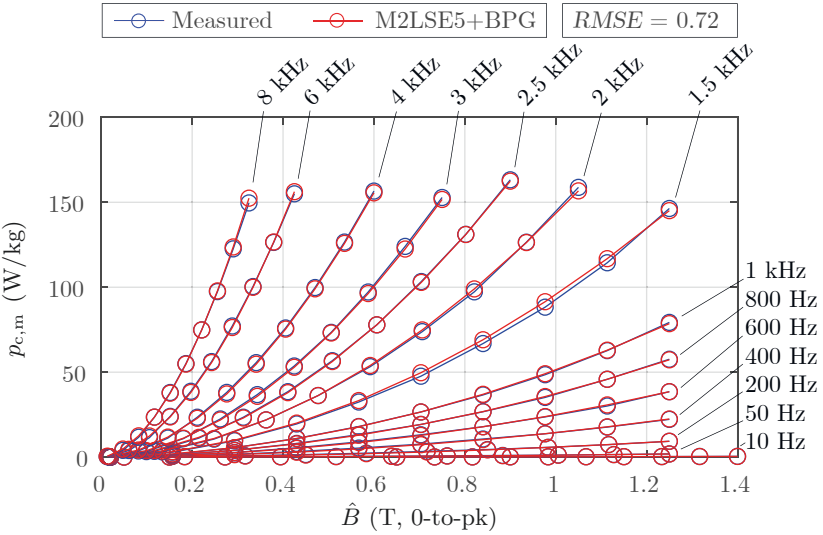


Figure B.31: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSin-ST10.

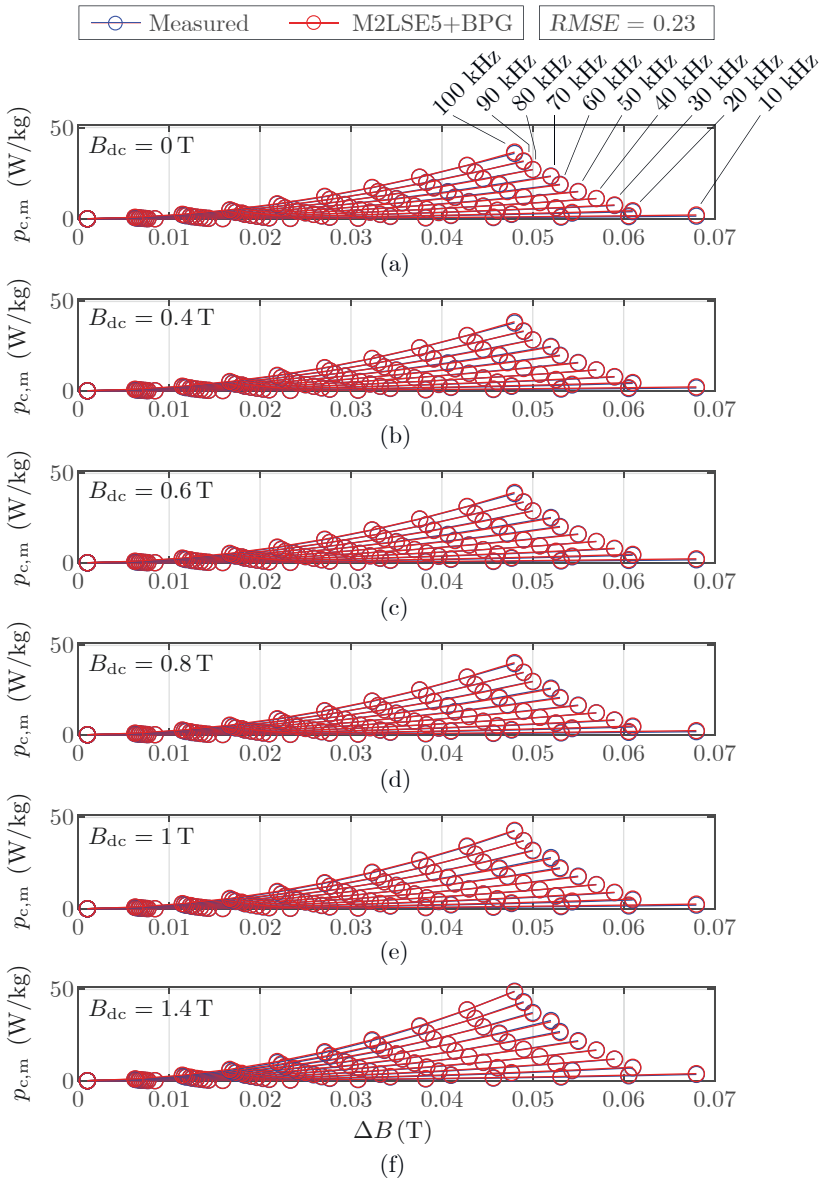


Figure B.32: Comparison of the predicted iron loss density curves, using the model M2LSE5+BPG, to the measured iron loss density curves from MeasSinDC-ST10.

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