An Impedance-Boosted Transformer-First Discrete-Time Analog Front-End Achieving 0.34 NEF and 389 MΩ Input Impedance

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Publication date:
2024-04

Permanent link:
https://doi.org/10.3929/ethz-b-000658454

Originally published in:
IEEE Journal of Solid-State Circuits 59(4), https://doi.org/10.1109/jssc.2024.3354243

An Impedance-Boosted Transformer-First Discrete-Time Analog Front-End Achieving 0.34 NEF and 389 MΩ Input Impedance

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***Abstract*—This paper presents a transformer-first analog front-end (AFE) for ultra-low-power sensor nodes. The proposed AFE employs a discrete-time transformer based on series-parallel converters as an input stage. The switched-capacitor transformer can provide a passive low-noise voltage gain, attenuating the input-referred noise (IRN) of the following continuous-time chain. However, it also degrades the AFE input impedance. As a remedy, this paper presents an input-resistance-boosting (IRB) loop that successfully increases the input resistance, sensing the output of a following continuous-time stage. At the same time, we also introduce an input-capacitance-canceling (ICC) loop to improve the input impedance at high frequencies. The proposed AFE achieves 389 $\mathrm{M\Omega}$ input impedance at 1 kHz, which represents a 39$\times$ improvement compared to prior work. Moreover, it attains superior noise efficiency, with an IRN of $1.36\ \mu\mathrm{V_{RMS}}$, while consuming 370 nW. This results in a noise efficiency factor (NEF) of 0.34 and a power efficiency factor (PEF) of 0.1, the lowest-reported values to the best of the authors' knowledge. The impedance-boosted chain consisting of the switched-capacitor transformer, first continuous-time amplifier, and the IRB loop achieves an NEF of 0.27 and a PEF of 0.06.**

***Index Terms*—Transformer-first analog front-end, Low-noise Amplifier, Noise efficiency factor, NEF, Power efficiency factor, PEF, Switched-capacitor transformer.**

I. Introduction

MINIATURIZED devices that integrate sensing, computing and communication capabilities enable a revolutionary leap in the way we perceive and interact with our physical environment [1]–[5]. Internet-of-everything wireless sensor nodes are envisioned to perform widespread monitoring of environmental quantities and bio-signals, providing an unprecedented level of information on our surroundings and health [6]–[17]. However, the ubiquitous deployment of tiny sensor nodes involves several challenges on their power consumption. Moreover, these miniaturized platforms usually suffer from stringent requirements on their input-referred noise (IRN) as they need to handle extremely weak signals, with amplitudes that usually fall in the μV range.

To overcome this challenge, miniaturized wireless sensor nodes frequently rely on a low-noise amplifier (LNA), which significantly boosts the input signal, minimizing additional noise contributions from the following stages. Because of its strict noise requirements, the LNA is usually the most power-hungry component in the system and should be optimized in terms of noise and power consumption.

The noise efficiency of an amplifier has been characterized using two metrics, known as noise efficiency factor (NEF) and power efficiency factor (PEF). Several structures have been investigated to minimize the NEF and PEF of continuous-time amplifiers (CTAs). Recent approaches mainly rely on a technique known as current reuse to increase the transconductance of the amplifier while maintaining the same current consumption [18]–[25]. Using this concept, an inverter-stacking amplifier, introduced in [26], [27] achieved the lowest-reported noise efficiency factor among CTAs. However, this technique poses several limitations to the supply headroom and the output dynamic range, resulting in limited PEF improvements. As a result, continuous-time amplifiers failed in achieving a PEF < 1, with minimal improvements in the last decade [28].

More recently, discrete-time amplifiers (DTAs) became interesting as a promising technique to significantly push the NEF and PEF boundaries of analog front-ends (AFEs) [28]–[32]. A discrete-time switched-capacitor (SC) architecture based on series-parallel converters was introduced in [28]. This structure, known as series-parallel amplifier (SPA), allows achieving 0.45 NEF and 0.2 PEF. The SPA works as a transformer, providing a passive voltage gain and consequently improving the IRN of the AFE chain.

However, the input resistance of the SPA introduced in [28] is limited by the bottom-plate capacitors which are charged and discharged at each sampling cycle, causing a non-zero average input current proportional to the input voltage. Moreover, the SPA also exhibits a significant input capacitance, requiring impedance boosting. A discrete-time AFE using a multiphase stepwise charging of the bottom-plate capacitance was proposed in [33]. However, the input impedance was limited to $10\,M\Omega$, which may still cause a degradation of the signal-to-noise ratio (SNR) for some environmental and bio-signal sensing applications operating with a signal source with a large output impedance. Also, the stepwise charging technique allows boosting the input resistance but does not address the input capacitance of the SC discrete-time transformer.

In this work, we propose an impedance-boosted analog front-end, using a series-parallel input stage and achieving 0.34 NEF and 0.1 PEF, the lowest-reported NEF and PEF to the best of the authors' knowledge. The proposed AFE features input-resistance-boosting (IRB) and input-capacitance-

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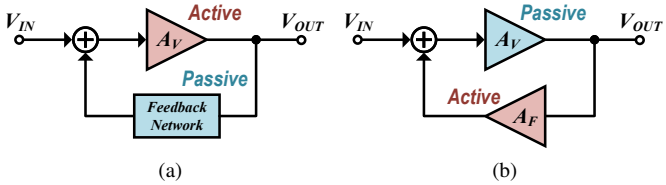


Fig. 1. Conventional block diagram of an active amplifier with negative feedback (a), and block diagram of the proposed passive feed-forward path using active feedback.

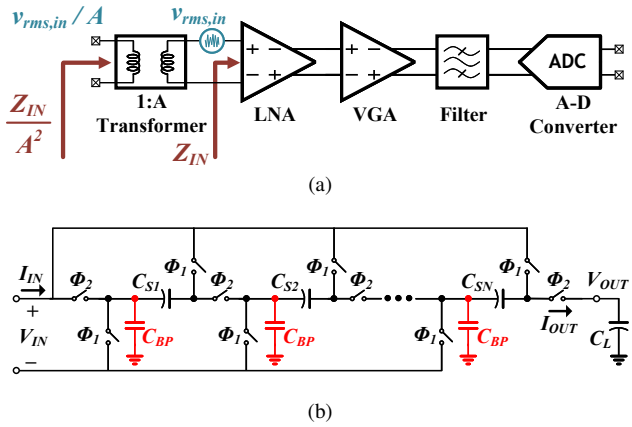


Fig. 2. Block diagram of a transformer-first sensor interface circuit (a), and schematic of a discrete-time switched-capacitor transformer based on a series-parallel converter.

canceling (ICC) loops, achieving 389 $M\Omega$ input impedance. Moreover, the discrete-time approach introduced in this paper inherits the advantages of the SPA introduced in [28], generating negligible flicker noise and becoming highly attractive for low-frequency applications.

This paper is an extended version of [34] and is organized as follows: Section II presents the working principle, benefits, and theoretical limits of the proposed transformer-first sensor interfaces; Section III introduces the implementation details, including the impedance boosting technique and calibration; Section IV presents the measurement results, and finally, Section V concludes the paper.

II. Transformer-first Analog Front-Ends

A. Benefits of Passive Low-Noise Amplification

Low-noise linear amplification is required in an extensive range of sensor read-out circuits which usually need to deal with extremely weak signals. The typical block diagram of conventional amplifiers consists of an active feed-forward path and a passive feedback network as shown in Fig. 1a. The feed-forward path is usually designed using active components that provide a high driving strength, but at the same time, introduce several imperfections, in terms of accuracy, noise, and linearity. Conventionally, the widely adopted solution to deal with the imperfections introduced by the active feed-forward path has been the negative feedback, using a passive feedback network. However, active components in the feed-forward path intrinsically introduce a limitation in the noise efficiency of an amplifier.

To understand the fundamental NEF limitation of CTAs, let us first introduce the well-known NEF definition for an amplifier with input-referred noise $v_{rms,in}$, total current draw I_{tot}, and bandwidth f_{BW} [35]:

$$NEF \triangleq v_{rms,in}\sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot f_{BW}}}, \tag{1}$$

where k, U_T and T denote the Boltzmann's constant, the thermal voltage, and the absolute temperature, respectively. For a single-pole amplifier, when thermal noise is dominant, the IRN can be expressed as a simple function of the noise power spectral density $S^2_{rms,in}$, and bandwidth:

$$v_{rms,in} = \sqrt{S^2_{rms,in} f_{BW} \pi/2}. \tag{2}$$

Substituting (2) in (1), we obtain

$$NEF = \sqrt{\frac{S^2_{rms,in} \cdot I_{tot}}{4kTU_T}}, \tag{3}$$

when thermal noise is dominant, and the amplifier has a single-pole low-pass behavior. As a result, the noise efficiency factor depends on the product of the noise power spectral density $S^2_{rms,in}$ and the current consumption I_{tot}, which is limited by the transconductance efficiency g_m/I_D of the active devices. As an example, for a single MOS transistor, if we denote the input-referred noise power spectral density as $S^2_{rms,in,MOS}$ and the drain current as I_D, the noise-current product can be expressed as a function of the g_m/I_D:

$$S^2_{rms,in,MOS} \cdot I_D = \frac{2q}{(g_m/I_D)^2}, \tag{4}$$

where q is the electron charge. Therefore, the minimum achievable NEF is closely related to the maximum g_m/I_D of the devices, which is physically limited.

To overcome the limitations of active components, in this work, we propose to employ a passive feed-forward path and apply active feedback. The basic block diagram is represented in Fig. 1b. Compared to active amplification schemes, passive gain can be inherently more linear and accurate while introducing lower noise and allowing us to completely avoid the NEF limitations described above. A passive gain stage provides a voltage gain (A) and attenuates the input current, operating as a transformer. This allows reducing the input-referred noise at the expense of a reduced input impedance.

The block diagram of a sensor-interface circuit using a passive input stage is shown in Fig. 2a. We refer to such a sensor-interface circuit as a transformer-first AFE. While the input-referred noise is improved by a factor of $1/A$, the input impedance Z_{IN} would be degraded by $1/A^2$. In addition, the passive gain stage introduces an additional impedance, further lowering Z_{IN}. To resolve this issue, this work introduces an active feedback (Fig. 1b) consisting of an input capacitance canceling (ICC) loop [36] and the proposed input resistance boosting (IRB) loop.

B. Discrete-Time Switched-Capacitor Transformer

Passive voltage gain offers a low-noise and highly linear amplification, avoiding the distortion, noise, and linearity issues of active circuits. The benefits of passive voltage gain have been successfully and widely demonstrated in high-frequency applications by adopting on-chip transformers or resonant LC tanks to improve noise and linearity [37]–[41]. However, these implementations result in a low input impedance and require high-quality-factor passive components, which are usually not available for low-frequency applications.

In this work, we propose a discrete-time transformer implemented with a switched-capacitor series-parallel converter. First introduced in [28] and named as a series-parallel amplifier (SPA), a switched-capacitor series-parallel network can provide a linear low-noise passive gain, achieving 0.45 NEF and 0.1 PEF. The basic building block is shown in Fig. 2b and operates in two phases. In the sampling phase, Φ_1 is high, and Φ_2 is low and the input signal is sampled on N capacitors in parallel. We refer to these capacitors as the sampling capacitors and assume they are equally sized, i.e. $C_{S1} = C_{S2} = ... = C_{SN} = C_S$. In the hold phase, Φ_2 is high, and Φ_1 is low, and the capacitors are serialized, achieving a voltage gain of $N+1$ if the bottom-plate capacitance C_{BP} is neglected. However, a fraction of the charge on the sampling capacitor is lost because of the charge-sharing operation due to the bottom-plate capacitors, resulting in an actual voltage gain $A < N+1$. The voltage gain A was derived in [28] and can be expressed as

$$A = 1 + \sum_{i=1}^{N} \frac{\chi_i}{\chi_N}, \tag{5}$$

and the χ_i are polynomial functions with degree $i-1$ defined as

$$\chi_{i+1} = \chi_i + \alpha \sum_{j=1}^{i} \chi_j, \tag{6}$$

where $\alpha = C_{BP}/C_S$ is the ratio of the bottom-plate capacitance to the sampling capacitance. The term χ_1 is constant and equal to 1 [28]. Note that in (5) , the ratio of χ_i to χ_N corresponds to the attenuation of the voltage on the i-th capacitor during the hold phase. As an example, for a $1:2$ converter, we have $\chi_1 = 1$ and $\chi_2 = 1+\alpha$. The voltage on the sampling capacitor C_{S1} at the end of the hold phase would therefore be $V_{CS1} = V_{IN}/(1+\alpha)$, as expected because of the charge conservation during the charge-sharing process between C_{S1} and C_{BP2}. Assuming $C_{BP} \ll C_S$, i.e. $\alpha \ll 1$, (5) can be simplified as

$$A \simeq 1 + \frac{2N + \alpha N(N^2-1)/3}{2 + N(N-1)\alpha}. \tag{7}$$

If the effect of the bottom-plate capacitors is negligible, i.e. if $\alpha = 0$, we get $A = N+1$ as expected.

C. Noise Efficiency Factor

We have seen that the NEF of a CTA is fundamentally limited by the g_m/I_D ratio and the NEF is typically higher than 1. In this regard, the SC transformer allows us to significantly improve the noise efficiency over conventional CTAs. First, let us discuss the input-referred noise of the discrete-time series-parallel transformer shown in Fig. 2b. During the sampling phase, while we are sampling the input signal V_{IN}, we also sample a kT/C_S noise on each capacitor. This noise appears at the output during the hold phase, determining a total output noise given by the sum of the uncorrelated noise contributions on each capacitor, i.e. $v^2_{rms,out} = N \cdot kT/C_S$. As sampling noise spreads its total power uniformly in the Nyquist bandwidth from 0 to $f_S/2$, the output noise power spectral density is $S^2_{rms,out} = N \cdot 2kT/(C_S f_S)$, according to the well-known folding mechanism due to the sampling operation on a capacitor [42]. Assuming a single-pole low-pass filter is implemented in the signal bandwidth f_{BW}, the total output noise can be expressed as

$$v_{rms,out,SPA} = \sqrt{N \frac{2kT}{C_S f_S} f_{BW} \frac{\pi}{2}}. \tag{8}$$

The IRN is simply obtained by dividing by the voltage gain A:

$$\begin{aligned} v_{rms,in,SPA} &= \frac{1}{A}\sqrt{N \frac{2kT}{C_S f_S} f_{BW} \frac{\pi}{2}} \\ &= \frac{N}{A}\sqrt{\frac{2kT}{C_{TOT} f_S} f_{BW} \frac{\pi}{2}}, \end{aligned} \tag{9}$$

where $C_{TOT} = NC_S$ is the total sampling capacitance. Note that the IRN depends on the sampling frequency and the sampling capacitance and can be reduced by either increasing f_S or C_S, at the expense of additional power consumption or area respectively. To derive the noise efficiency factor, we then need to discuss the current consumption of the SC transformer. The current consumption is mainly determined by the clock distribution network, level converters, and switch drivers. If V_{SW} and C_{SW} denote the voltage swing and total capacitance that needs to be charged and discharged at each sampling cycle, the total current consumed by tdiscrete-time series-parallel transformer can be calculated as

$$I_{SW,SPA} = C_{SW} f_S V_{SW}. \tag{10}$$

Finally, the noise efficiency factor can be derived by substituting (9) and (10) in (1):

$$\begin{aligned} NEF_{SPA} &= \frac{N}{A}\sqrt{\frac{2kT}{C_{TOT} f_S}}\sqrt{\frac{C_{SW} f_S V_{SW}}{4kTU_T}} \\ &= \frac{N}{A}\sqrt{\frac{C_{SW}}{C_{TOT}}\frac{V_{SW}}{2U_T}}. \end{aligned} \tag{11}$$

The expression derived for the NEF of the series-parallel transformer allows us to make some important observations and understand the advantages of the proposed passive amplification over conventional amplifiers.

- For continuous-time amplifiers, the trade-off between the input-referred noise and current consumption is physically limited as it depends on the g_m/I_D ratio. However, the NEF of the proposed passive discrete-time transformer depends on the ratio C_{SW}/C_S and scales with

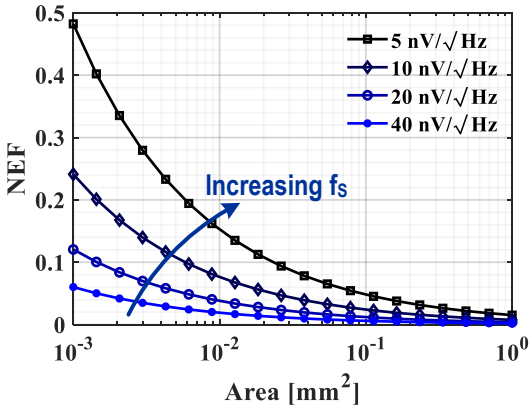


Fig. 3. NEF of the switched-capacitor transformer as a function of the area for a given IRN requirement.

process technology. In advanced technology nodes, C_{SW} can be further reduced, leading to an even smaller NEF.

- The proposed switched-capacitor solution exploits transistors as switches only, thus introducing negligible flicker noise. This becomes particularly attractive for low-frequency applications.
- The input-referred noise and current consumption can be easily adjusted by changing the sampling frequency depending on the application requirements.

Equation (9) shows that the IRN is a function of the product of the total sampling capacitance C_{TOT} and the sampling frequency f_S. Given a requirement on the desired input-referred noise, the resulting product of C_{TOT} and f_S can be determined from (9). The individual choice of C_S and f_S is then based on the requirements in terms of area, power consumption, input impedance, and NEF. Increasing the sampling capacitance and decreasing the sampling frequency while keeping the same product of C_{TOT} and f_S, results in a lower NEF, as the IRN is constant and the current consumption can be reduced due to the lower f_S. Fig. 3 shows the NEF as a function of the area for a given IRN requirement, assuming a capacitance density of 6 fF/μm^2. The NEF can be improved by increasing the sampling capacitance and decreasing the sampling frequency while their product is constant, at the expense of additional area occupation. Therefore, given an area requirement, the NEF can be minimized by fully utilizing the available area and maximizing C_{TOT}. Once the desired value of C_{TOT} is determined based on the area requirement, the sampling frequency can be calculated from C_{TOT} and the required IRN. The choice of the gain should also take into account the IRN contribution from the following stages and the NEF specification for the entire AFE. Increasing the gain of the SC transformer allows reducing the IRN of the following stages, but it also degrades the input impedance, which is discussed next.

D. Input Impedance

In this section, we discuss the input impedance Z_{IN} of the switched-capacitor transformer of Fig. 2b. First, while we are sampling the input voltage, we see an input capacitance $C_{TOT} = NC_S$, given by the parallel combination of the N sampling capacitors. However, the total input capacitance C_{IN} is actually higher than C_{TOT}, if the proposed switched-capacitor transformer operates with a load capacitance C_L. In order to understand the effect of C_L, let us consider a series-parallel transformer that drives a load resistance Z_L. Assuming the input power $P_{IN} = V_{IN}I_{IN}$ is equal to the output power $P_{OUT} = V_{OUT}I_{OUT}$, we can find $I_{OUT} = I_{IN}/A$. Then, the input impedance of the SC transformer due to the load impedance, Z_L, is

$$\frac{V_{IN}}{I_{IN}} = \frac{V_{OUT}/A}{A \cdot I_{OUT}} = \frac{1}{A^2}\frac{V_{OUT}}{I_{OUT}} = \frac{1}{A^2}Z_L. \tag{12}$$

Note that the proposed discrete-time series-parallel stage works as an impedance transformer, providing a voltage gain of $N+1$ and attenuating the input current by the same amount. As a consequence, Z_L is degraded by a factor of $(N+1)^2$ when referred to the input. If the load impedance is a capacitance C_L, which is typically the input capacitance of a following continuous-time stage, it is boosted by a factor of $(N+1)^2$ at the input terminals. The total input capacitance C_{IN} is calculated as the sum of these two contributions:

$$C_{IN} = NC_S + (N+1)^2 C_L. \tag{13}$$

In addition, the proposed switched-capacitor transformer exhibits an input resistance R_{IN} due to the bottom plate capacitors. Let us first consider the input resistance when $\alpha = 0$ and assume a scenario where a DC voltage $V_{IN,DC}$ is applied at the input of the discrete-time transformer. In this situation, the SPA produces an output of $V_{OUT,DC} = (N+1)\cdot V_{IN,DC}$. When the capacitors are configured in parallel for the sampling phase, the voltage on the sampling capacitors is already $V_{IN,DC}$ before connecting to the input. This is because no charge is lost during the amplification phase when the bottom-plate capacitance is 0. Consequently, the input current $I_{IN,DC}$ is 0, and the input resistance is infinite. However, the bottom-plate capacitors extract a fraction of the sampled charge from the sampling capacitors at each sampling cycle, degrading the input resistance. In the previous section, we showed that the bottom-plate capacitors reduce the gain from the ideal value of $N+1$ to A. Therefore, when the sampling capacitors are connected in parallel in the next sampling phase, each capacitance holds a voltage of $(A-1)V_{IN,DC}/N$, slightly lower than V_{IN}. This is because a fraction of the charge stored on the sampling capacitors has been taken to charge the bottom-plate capacitance while the capacitors are in series. The total charge lost in this process needs to be replenished from the input terminals at each sampling cycle. In this condition, the input DC current is given by:

$$I_{IN,DC} = \left(V_{IN,DC} - \frac{A-1}{N}V_{IN,DC}\right)NC_S f_S. \tag{14}$$

The DC input resistance can then be calculated as:

$$\begin{aligned} R_{IN} &= \frac{V_{IN,DC}}{I_{IN,DC}} = \frac{1}{NC_S f_S}\frac{1}{1-(A-1)/N} \\ &= \frac{1}{C_{BP} f_S}\frac{\alpha}{N+1-A}. \end{aligned} \tag{15}$$

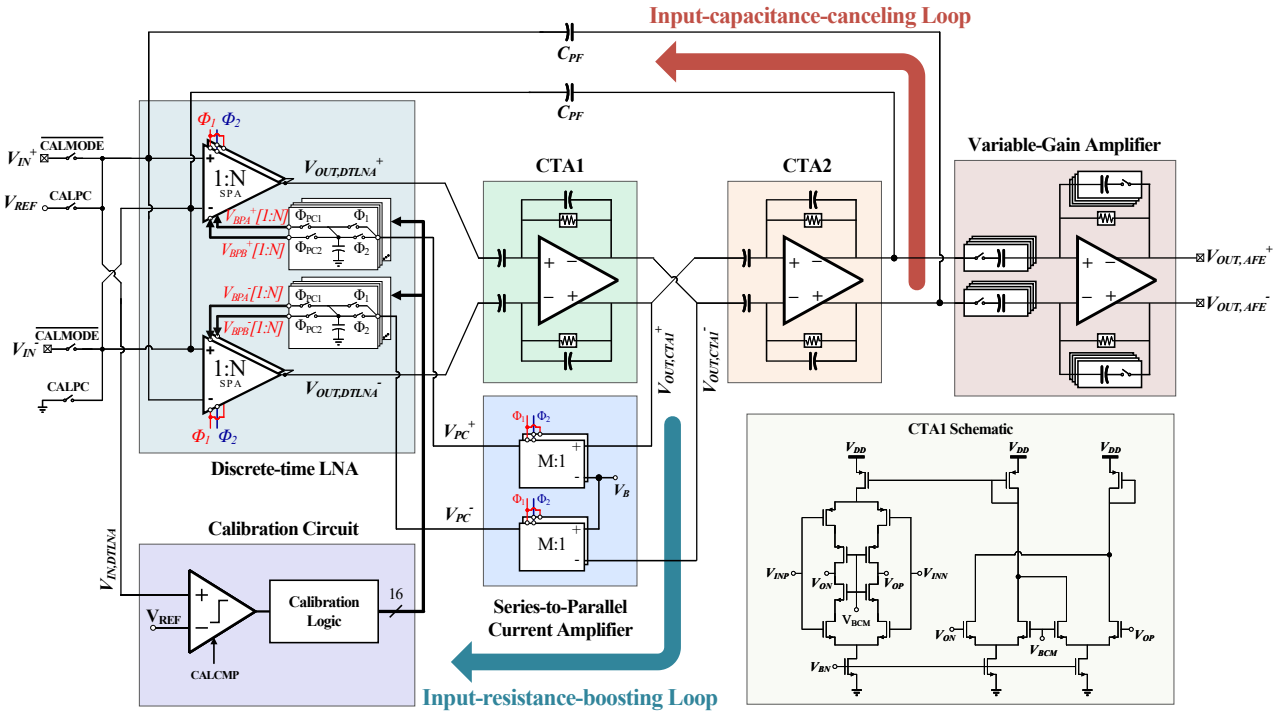


Fig. 4. Simplified schematic of the proposed analog front-end chain.

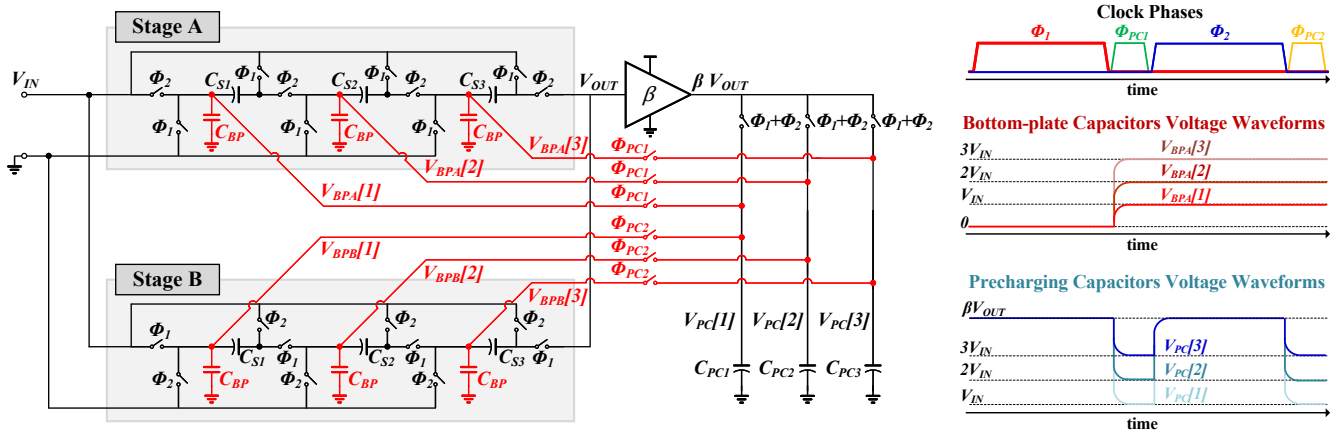


Fig. 5. Simplified schematic of a 1:N switched-capacitor discrete-time transformer with input-resistance boosting (a), and IRB waveforms (b).

The total input impedance Z_{IN} of the proposed transformer is the parallel combination of the input capacitance C_{IN} and input resistance R_{IN} derived in this section:

$$Z_{IN} = R_{IN}||1/(sC_{IN}). \tag{16}$$

III. Implementation Details and Analysis

A. Proposed Analog Front-End Architecture

The overall schematic of the proposed AFE is depicted in Fig. 4. The AFE employs a discrete-time low-noise amplifier (DTLNA) as an input stage. The DTLNA is based on switched-capacitor series-parallel transformers and introduces a passive voltage gain to attenuate the IRN of the following stages.

The DTLNA is followed by two continuous-time amplifiers, CTA1 and CTA2, and a variable-gain amplifier (VGA) receives the output of CTA2 to generate the AFE output. The continuous-time amplifiers are implemented using inverter-based differential input pairs to achieve a higher transconductance and, thus, a lower NEF.

The proposed AFE also features two input-impedance-boosting loops to increase the input resistance and lower the input capacitance of the DTLNA. The input-resistance-boosting loop works by precharging the bottom-plate capacitors using the CTA1 output and includes an M:1 series-to-parallel downconverter which serves as a current amplifier. The IRB loop and the purpose of the proposed M:1 downconverter

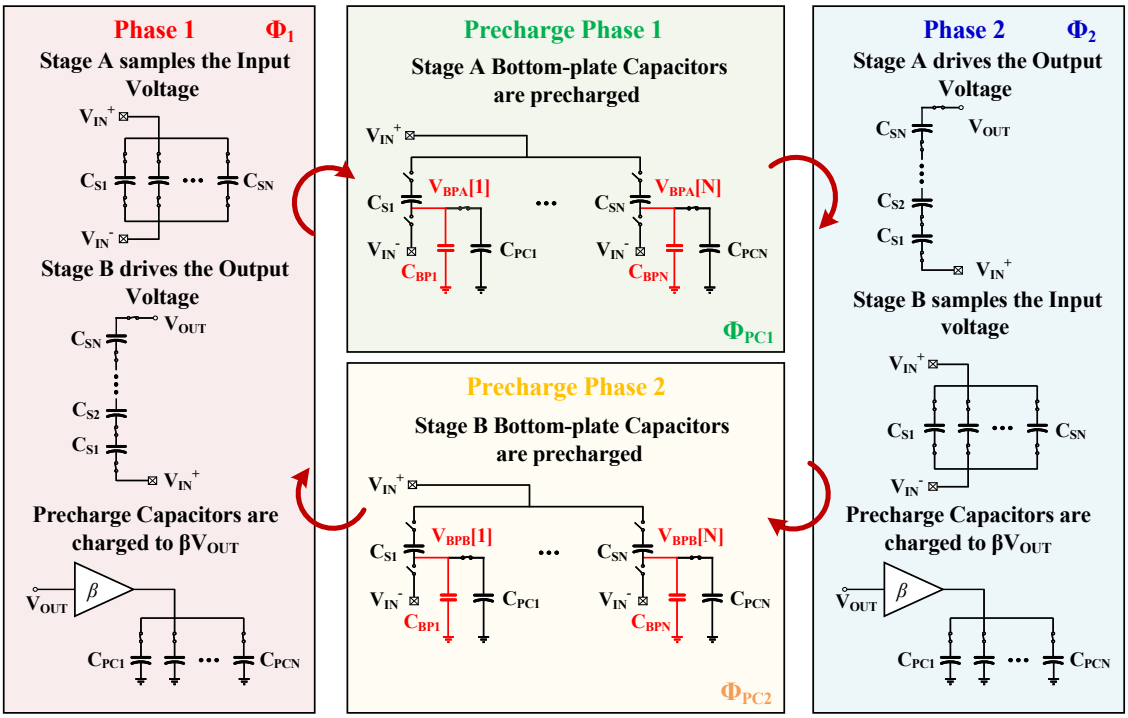


Fig. 6. Operating principle of the proposed input-resistance-boosting mechanism.

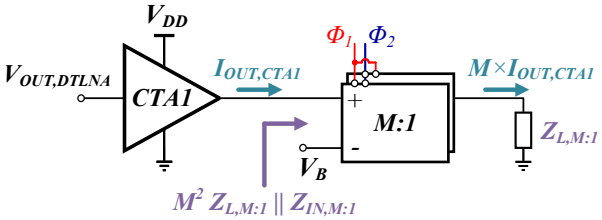


Fig. 7. Impedance transformation provided by the series-to-parallel M:1 downconverter to reduce the load seen by the continuous-time amplifier.

are discussed in Section III-C, while the ICC loop is explained in Section III-D. The proposed IRB method also requires a calibration circuit which is explained in Section III-E.

B. Discrete-Time Low-Noise Amplifier

As mentioned, the proposed DTLNA should provide a noise-efficient passive voltage gain. To serve this purpose, the DTLNA is based on SC transformers. It consists of two paths that receive both the positive and negative input voltage levels with opposite polarity and generate the fully differential output.

The positive path samples the input voltage $V_{IN} = V_{IN}^{+} - V_{IN}^{-}$ on $N = 9$ capacitors in parallel and generates an output voltage

$$\begin{aligned} V_{OUT,DTLNA}^{+} &= V_{IN}^{+} + N(V_{IN}^{+} - V_{IN}^{-}) \\ &= V_{CM} + \left(N + \frac{1}{2}\right)V_{DM}, \end{aligned} \tag{17}$$

where V_{CM} and V_{DM} denote the input common mode and differential mode respectively. Similarly, the negative path receives an input voltage of $V_{IN}^{-} - V_{IN}^{+}$ and generates an output voltage

$$\begin{aligned} V_{OUT,DTLNA}^{-} &= V_{IN}^{-} - N(V_{IN}^{+} - V_{IN}^{-}) \\ &= V_{CM} - \left(N + \frac{1}{2}\right)V_{DM}. \end{aligned} \tag{18}$$

Therefore, the output voltage of the DTLNA is

$$\begin{aligned} V_{OUT,DTLNA} &= V_{OUT,DTLNA}^{+} - V_{OUT,DTLNA}^{-} \\ &= (2N+1)(V_{IN}^{+} - V_{IN}^{-}) \\ &= (2N+1)V_{DM}. \end{aligned} \tag{19}$$

Note that, while the input common mode appears in the expressions of $V_{OUT,DTLNA}^{+}$ and $V_{OUT,DTLNA}^{-}$, there is no common mode to differential mode conversion in (19). Also, thanks to the fully differential operation, the voltage gain is nearly doubled, i.e. the DTLNA gain is $A_{DTLNA} = 2N + 1$, if the bottom-plate capacitors are neglected.

Each path consists of two time-interleaved SC transformers (stage A and stage B) based on the series-parallel topology depicted in Fig. 2b. Stage A and stage B operate in anti-phase to avoid floating the output. When Φ_1 is high, stage A is configured in parallel and samples the input voltage, while stage B is configured in series to drive the output. Vice versa, when Φ_2 is high, stage A drives the output and stage B samples the input voltage. Consequently, the load capacitance is always driven either by stage A or B and the noise introduced by the sampling operation on the load capacitance is negligible.

C. Input-Resistance-Boosting Loop

The main idea of the IRB loop is to precharge the bottom-plate capacitors before the hold phase, using the output of

the first CTA (CTA1). A schematic of the input-resistance-boosting loop is shown in Fig. 5a, together with its operating waveforms (Fig. 5b), for a simplified case with $N = 3$. The key operating principle is explained in Fig. 6. First, during phase 1, while stage A is sampling the input and stage B is driving the output, the precharge capacitors (C_{PC1}, C_{PC2}, C_{PC3}) are charged using the CTA1 output. The DTLNA cannot be directly used for this precharging operation as active circuits are needed to produce the additional charge. In this work, the CTA1 output voltage is attenuated by the M:1 downconverter to provide the charge. If the total gain introduced by the CTA1 and M:1 downconverter is denoted as $\beta = A_{CTA1}/M$, the precharge capacitors are initially charged to βV_{OUT} during phase 1, when Φ_1 is high.

Then, during a brief precharge phase when Φ_{PC1} is high, we perform a charge-sharing operation between the bottom-plate capacitors and the precharge capacitors. After the charge-sharing operation, the voltage $V_{BP,i}$ on the i-th bottom-plate capacitance ideally needs to be iV_{IN} but it depends on the size of the precharge capacitors. Therefore, a calibration of the precharge capacitance is needed for accurate precharging. At the end of phase 1, the i-th precharge capacitance, $C_{PC,i}$, stores a charge $Q_{PC,i} = \beta V_{OUT} C_{PC,i}$ and after the charge-sharing operation, the voltage on the bottom-plate capacitors is

$$V_{BP,i} = \frac{\beta V_{OUT} C_{PC,i}}{C_{PC,i} + C_{BP}}. \tag{20}$$

By equalizing $V_{BP,i}$ to iV_{IN}, the i-th precharge capacitance can be found as

$$C_{PC,i} = \frac{iC_{BP}}{(N+1)\beta - i}. \tag{21}$$

For the fully differential case (Fig. 4), the precharge capacitance is

$$C_{PC,i} = \frac{iC_{BP}}{\frac{A_{DTLNA}}{2}\beta - i}. \tag{22}$$

If the precharge capacitors are sized exactly according to (21), the bottom-plate capacitors are already charged to the intermediate voltages in the series configuration, and they will not subtract any charge from the sampling capacitors. As a result, the voltage gain A_{DTLNA} can be restored to the ideal value of $2N + 1$. At the same time, the proposed technique boosts the input resistance because, when stage A is switched back to the parallel configuration, the voltage on the sampling capacitors is equal to V_{IN} and they will not take any charges from the input terminals. During phase 2 (Φ_2 is high), we also charge the precharge capacitors again so that we can have another precharge phase for the bottom-plate capacitors of stage B. As in the previous case, when Φ_{PC2} is high, the bottom-plate capacitors in stage B are precharged to (20) by sharing charges with the precharge capacitors. The time-domain waveforms of $V_{BP,i}$, $V_{PC,i}$, and clock signals are shown in Fig. 5b.

Finally, note that the precharge capacitors should be quickly set to βV_{OUT} before each sampling cycle with sufficient accuracy. As the total precharge capacitance could be much higher than the bottom-plate capacitance C_{BP}, an M:1 voltage downconverter is introduced to amplify the precharging current. The M:1 downconverter samples the CTA1 output on a series of M capacitors and rearranges these capacitors in parallel to generate its output voltage.

The proposed M:1 downconverter offers several advantages with negligible area and power overhead:

- It reduces the power consumption of the CTA1 by increasing its load impedance. We have seen that for an SC transformer with a gain of A, a load impedance Z_L can be referred to the input as Z_L/A^2. Therefore, the series-to-parallel M:1 downconverter increases the load impedance seen by the CTA1 by a factor of M^2. The CTA1 load impedance can be expressed as $M^2 Z_{L,M:1}$, where $Z_{L,M:1}$ is the load impedance of the M:1 downconverter. Furthermore, the input capacitance of the M:1 downconverter is given by a series of M capacitors, resulting in a high input impedance of the M:1 downconverter itself $Z_{IN,M:1}$. The total input impedance of M:1 downconverter is illustrated in Fig. 7.
- The resolution of the impedance boosting is proportional to βC_{LSB}, where C_{LSB} is the minimum calibration resolution of the precharge capacitors. As the M:1 downconverter lowers β, it improves the maximum achievable input impedance of the DTLNA, thanks to a more precise calibration.

D. Input-Capacitance-Canceling Loop

While the proposed IRB loop allows boosting the input resistance, the input impedance may still be limited by C_{IN} at high frequencies. Therefore, we also introduce an input-capacitance-canceling (ICC) loop. The ICC loop employs positive feedback to create a negative capacitance at the input through Miller effect. The negative capacitance cancels C_{IN} and boosts the high-frequency input impedance [36], [43]. The ICC loop provides an input current, I_{PF}, to the AFE input terminals, which should ideally match the AFE input current, I_{AFE}, thus minimizing the current drawn from the input source, I_{IN}. If I_{PF} is equal to I_{AFE}, the input capacitance is perfectly canceled and I_{IN} becomes 0.

We can calculate the ideal positive feedback capacitance C_{PF} in the ICC loop by equalizing I_{PF} and I_{AFE}. In this case, the positive feedback current is given by

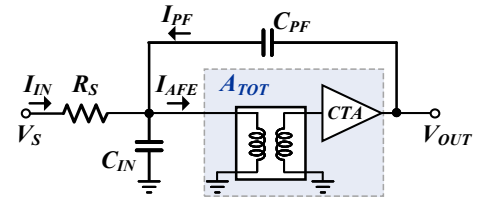
$$\begin{aligned} I_{PF} &= sC_{PF}V_{IN}(A_{DTLNA}A_{CTA1}A_{CTA2} - 1) \\ &= sC_{PF}V_{IN}(A_{TOT} - 1), \end{aligned} \tag{23}$$

where A_{CTA1} and A_{CTA2} represent the gain of the CTA1 and CTA2 respectively, and A_{TOT} is the total gain provided by the DTLNA, CTA1, and CTA2.

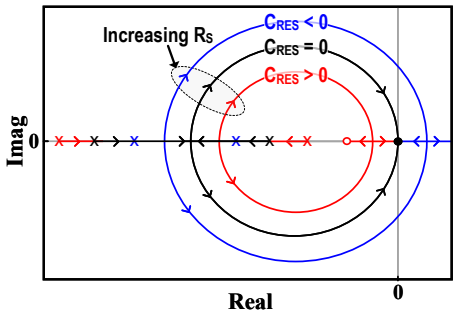
The AFE current caused by C_{IN} is $I_{AFE} = sC_{IN}V_{IN}$. Then, the ideal value of C_{PF} to cancel the input capacitance is

$$C_{PF} = \frac{C_{IN}}{A_{TOT} - 1}. \tag{24}$$

Variations of C_{PF} result in imperfect cancellation of C_{IN} and residual I_{AFE}. Still, the precision of the cancellation is defined by capacitance ratios, between C_{PF} and C_{IN} and



(a)



(b)

Fig. 8. Simplified circuit model for stability considerations (a), and a root locus of closed-loop poles as a function of R_S (b).

between the capacitors defining the closed-loop gain of the amplifier stages. Therefore, a sufficient capacitance cancellation is achieved without performing calibration or trimming.

The residual capacitance after cancellation can be calculated as

$$C_{RES} = C_{IN} - (A_{TOT} - 1)C_{PF}. \tag{25}$$

To make some observations regarding the stability of the positive feedback loop, let us consider the simplified circuit depicted in Fig. 8a, which represents a transformer-first AFE with positive feedback. The resistance R_S represents the source impedance while C_{IN} is the input capacitance. Let us assume that the transformer and the continuous-time amplifier provide a total low-frequency gain of A_{TOT} and have a dominant pole in $-1/\omega_P$.

The closed-loop transfer function of the system in Fig. 8a can be derived as

$$\frac{V_{OUT}}{V_S} = \frac{A_{TOT}}{1 + s(\frac{1}{\omega_P} + R_S C_{RES}) + s^2 \frac{R_S(C_{IN}+C_{PF})}{\omega_P}} \tag{26}$$

The system is unstable when the poles of (26) lie on the right-half plane, namely if

$$C_{PF} > \left(C_{IN} + \frac{1}{\omega_P R_S}\right) \frac{1}{A_{TOT} - 1} \tag{27}$$

Note that, the stability of the positive feedback loop depends on the source resistance. For instance, if $R_S = 0$ the system is stable for any value of C_{PF} and the amplifier generates $V_{OUT} = A_{TOT} V_S$. However, the system may become unstable for large values of the source resistance. If $R_S \to \infty$, (26) can be approximated as

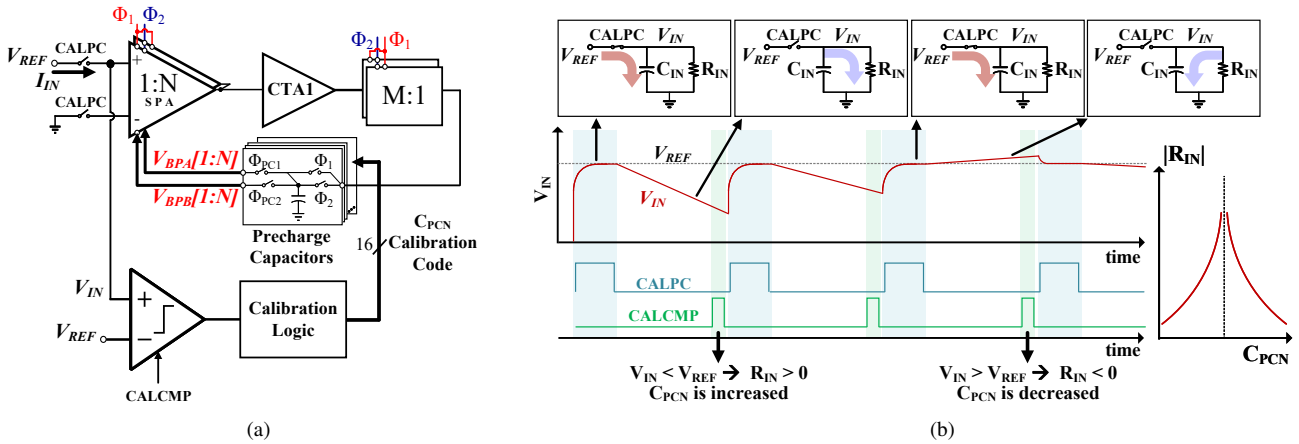
$$\frac{V_{OUT}}{V_S} \simeq \frac{A_{TOT}}{sR_S(C_{RES} + (C_{IN} + C_{PF})/\omega_P)} \tag{28}$$

The resulting transfer function has a pole in the origin and a pole in $-C_{RES}\omega_P/(C_{IN} + C_{PF})$. The latter can be in the right-half plane if the residual input capacitance is negative. Fig. 8b shows the root locus of the simplified circuit in Fig. 8a, obtained while increasing the source resistance R_S. Three different cases are considered, depending on the value of C_{PF}. If C_{PF} is lower than (24), the residual capacitance is positive and the system is stable for any value of the source resistance. If C_{PF} exactly satisfies (24), the residual capacitance is $C_{PF} = 0$, and the closed-loop transfer function has two poles in the origin when $R_S \to \infty$. Finally, for large values of the source resistance, the system can become unstable if C_{PF} is larger than (24). Our AFE operates with a positive residual input capacitance of approximately 200 fF and is stable for any value of the source resistance. Based on simulation results, our AFE tolerates a 34 MΩ source resistance while maintaining a critically damped response. If the source resistance is further increased, the AFE response becomes underdamped, with a pole quality factor of 1 when the source resistance is 62 MΩ. Additionally, the positive feedback loop can degrade the phase margin of the continuous-time amplifiers. Our CTAs can still maintain a phase margin higher than 70° while using the discussed ICL for impedance boosting.

E. Calibration

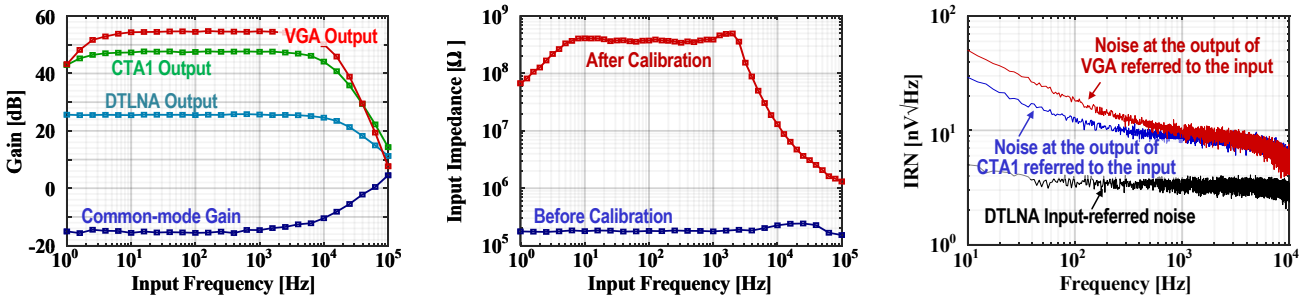
As explained in Section III-C, the input resistance can be increased using the proposed IRB loop. However, the input-resistance-boosting mechanism relies on the accuracy and precision of several parameters, including the matching between the precharge capacitors and bottom-plate capacitors, as well as the gain of the CTA1 and M:1 downconverter. When the precharge capacitors are set according to (21), the input resistance is boosted to infinity. If the precharge capacitors are smaller, the charge lost by the bottom-plate capacitors are not sufficiently restored, and R_{IN} becomes smaller. By contrast, if the precharge capacitors are larger, R_{IN} becomes negative and decreases in magnitude. Therefore, the precharge capacitors need to be accurately calibrated to maximize the input resistance. However, it should be noted that the calibration can be performed only on one of the precharge capacitors. This is because it is only important to match the total charge lost by the bottom-plate capacitors and the total charge restored by the precharge capacitors, rather than matching each individual charge lost by the i-th bottom-plate capacitor to the charge restored by the corresponding i-th precharge capacitor. As far as the total lost charge equals the total restored charge, the voltage on the sampling capacitors becomes V_{IN} when they are configured in parallel before sampling the input. In this work, we choose to calibrate the largest precharge capacitor, C_{PCN}, as this leads to the smallest resolution in controlling the restored charge. Thus, it helps achieving a high input resistance with a given finite resolution for calibrating the precharge capacitance.

A simplified schematic of the circuit in calibration mode is shown in Fig. 9a. The calibration works as follows. The input of the SC transformer is first set to a reference voltage V_{REF} (CALPC is high), charging the input capacitance of the AFE to V_{REF}. Then, the input voltage of the proposed AFE is floated for several sampling cycles. When the charge



(a) (b)

Fig. 9. Simplified schematic in calibration mode (a), and calibration waveforms (b).



(a) (b) (c)

Fig. 10. Measurement results on the transfer function (a), input impedance (b), and input-referred noise (c).

restored by the precharge capacitors is not sufficient, the charge on the input capacitance of the AFE is periodically subtracted by the bottom-plate capacitors, and the voltage on the input capacitance decreases from the initial value of V_{REF}. Indeed, the input capacitance of the AFE, previously precharged to V_{REF}, is discharged through its input resistance R_{IN}. After several sampling cycles, CALCMP goes high, and the input voltage is compared with the initial value of V_{REF}. If $V_{IN} < V_{REF}$, the input resistance is positive, and the calibration logic increases C_{PCN} by C_{LSB}. As a result, the voltage difference $V_{REF} - V_{IN}$ becomes smaller in the next calibration iteration with a larger C_{PCN}. The aforementioned process repeats until V_{IN} becomes larger than V_{REF} at the final comparison step, which means the input resistance becomes negative. At this point, the calibration stops with the previous value of the precharge capacitance, yielding the largest positive input resistance. The transient waveforms of the input voltage and clock signals are shown in Fig. 9b.

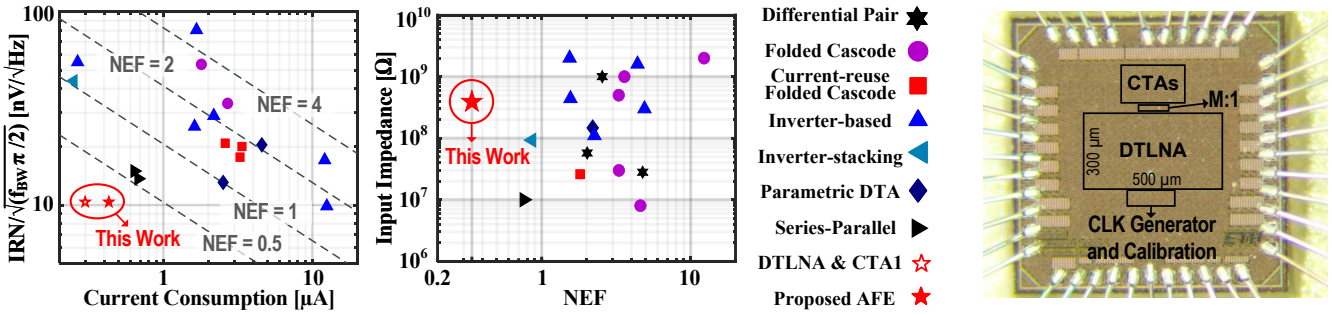
IV. Measurement Results

The proposed AFE was fabricated in a 22 nm FDSOI process and occupies an area of $0.21\ \text{mm}^2$. The area is dominated by the DTLNA which occupies $0.15\ \text{mm}^2$, while the CTAs and M:1 downconverter occupy $0.022\ \text{mm}^2$ and $0.0047\ \text{mm}^2$, respectively. The transfer functions of the proposed DTLNA and AFE are shown in Fig. 10a. The DTLNA achieves a total gain of 25.6 dB, which is sufficient to attenuate the IRN of the following CTAs. The CTA1 and CTA2 offer a gain of 22 dB and 7 dB, respectively. The overall AFE gain can be configured between 26 dB and 85 dB, by programming the VGA. The proposed AFE achieves a 70 dB common-mode rejection ratio and a 78 dB power supply rejection ratio.

Fig. 10b shows the magnitude of the input impedance Z_{IN} over frequency before and after the calibration. The calibration successfully boosts R_{IN} from $160\,\text{k}\Omega$ to approximately $400\,\text{M}\Omega$. The proposed AFE also maintains a high input impedance over a wide frequency range thanks to the ICC loop, resulting in $|Z_{IN}| = 389\,\text{M}\Omega$ at 1 kHz.

The input-referred noise spectrum is shown in Fig. 10c. The input-referred noise floor is $4\,\text{nV}/\sqrt{\text{Hz}}$, $8.6\,\text{nV}/\sqrt{\text{Hz}}$, and $9.1\,\text{nV}/\sqrt{\text{Hz}}$, measured for the DTLNA alone, the chain of our DTLNA and CTA1, and the overall AFE, respectively. Note that the DTLNA and CTA1 contribute nearly equally to the total IRN despite a large gain provided by the DTLNA. For conventional CTAs, the IRN is usually dominated by the first stage because the IRN contribution of the next stages is negligible. This is the optimum operating condition only when the NEF of the first and second stages are similar. However, in the proposed design, the NEF of the DTLNA is much smaller than that of the CTA1, so that the optimum condition is achieved when the noise of the DTLNA is similar to the noise of CTA1 after attenuating by the DTLNA gain.

As derived in [31], to minimize the NEF of the chain, it is important to optimize the ratio $\gamma = I_{DTLNA}/I_{CTA1}$



(a) (b)

Fig. 11. Performance comparison with prior works (a) and die micrograph (b).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This Work		Atzeni VLSI 2022 [33]	Jang VLSI 2018 [31]	Muller JSSC 2015 [44]	Shen JSSC 2018 [45]	Mondal JSSC 2020 [27]
	DTLNA, CTA1, M:1	AFE Chain					
Technology	22 nm		55 nm	180 nm	65 nm	180 nm	180 nm
CTA/DTA	DTA		DTA	DTA	CTA	CTA	CTA
Supply [V]	0.6 (DTLNA), 1 (CTAs)		0.9, 1.4	1.2	0.5	1	1.35
Area [mm^2]	0.21		0.41	0.073	0.025	-	0.24
Gain [dB]	47.6	26 - 85	23 - 80	30 - 60	30	25.6	36
Bandwidth [kHz]	10		10	8	0.5	10	0.24
Power [μ W]	0.24	0.37	0.74	5.5	2.3	0.25	0.187
Noise Floor [$nV/\sqrt{Hz}$]	8.6	9.1	15	24.5	58	-	158
IRN [μV_{RMS}]	1.30	1.36	2.46	2.3	1.3	6.7	3.07
NEF	**0.27**	**0.34**	**0.76**	**2.2**	**4.76**	**1.07**	**0.86**
PEF	**0.06**	**0.1**	**0.67**	**5.8**	**11.3**	**1.14**	**0.99**
Input Impedance [MΩ]	**389**		**10**	**147**	**28**	**-**	**93**
THD [dB] (V_{IN} [V_{PP}])	-54 (10 mV)		-	-40 (5 mV)	-	-	-56 (17 mV)
CMRR [dB]	70		82	77	88	84	95
PSRR [dB]	78		76	70	67	76	68

where I_{DTLNA} and I_{CTA1} are the current consumption of the DTLNA and CTA1, respectively. The optimum current ratio γ_{opt} depends on the noise efficiency factors of the DTLNA and CTA1 (NEF_{DTLNA} and NEF_{CTA1} respectively) and can be derived as [31]

$$\gamma_{opt} = (2N+1)\frac{NEF_{DTLNA}}{NEF_{CTA1}}. \tag{29}$$

This results in an optimum current ratio of nearly 1 for the DTLNA and CTA1, when $NEF_{DTLNA} \simeq 0.1$ and $NEF_{CTA1} \simeq 2$. At this optimum current division, the input-referred noise of the amplifier chain is calculated as follows:

$$\begin{aligned} v^2_{rms,opt} &= v^2_{rms,DTLNA} + \frac{v^2_{rms,CTA1}}{(2N+1)^2} \\ &= v^2_{rms,DTLNA} \cdot \left(1 + \frac{1}{\gamma^2_{opt}}\right) \end{aligned} \tag{30}$$

Consequently, we observe nearly the same contributions from the DTLNA and CTA1 to the overall IRN, as shown in (30) and Fig. 10c. The total integrated IRN is $1.36\,\mu V_{RMS}$ for the total AFE chain and $1.3\,\mu V_{RMS}$ for the chain of DTLNA and CTA1, while consuming 370 nW and 240 nW, respectively.

Fig. 11a and Table I compare the proposed design with prior works. The impedance-boosted chain consisting of the DTLNA and CTA1 achieves 0.27 NEF and 0.06 PEF, while the NEF and PEF of the total AFE are 0.34 and 0.1, respectively, the lowest-reported values to date. This corresponds to a $10\times$ power reduction compared to any continuous-time amplifier, while generating the same IRN. At the same time, compared to other amplifiers using SC transformers, the proposed design achieves a higher input impedance while reducing the area occupation.

V. CONCLUSION

We propose the transformer-first AFE as a promising technique for noise-efficient amplification. For low-frequency applications, passive gain can be implemented using discrete-time switched-capacitor converters operating as transformers. The proposed discrete-time transformer-first AFE achieves superior noise efficiency compared to conventional continuous-time analog front-ends, with an NEF of 0.34 and a PEF of 0.1. In addition, this work proposes an input-resistance-boosting loop that restores the charge loss caused by the bottom-plate capacitors. It also adopts an input-capacitance-canceling loop to improve the high-frequency impedance. The IRB and ICC loops successfully boost Z_{IN} to $389M\Omega$ at 1 kHz after calibration.

ACKNOWLEDGMENTS

This project was supported in part by the Swiss National Science Foundation Starting Grants 2022 (#211210) "Millimeter-scale Secure and Intelligent Computer Class for Internet of Everything."

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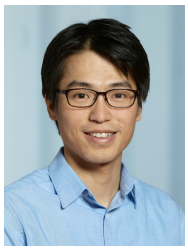

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