Influence of the rds,on temperature dependency of SiC MOSFETs on the optimal switching cell mechanical layout

Author(s):
Papadopoulos, Georgios; Biela, Jürgen

Publication date:
2023

Permanent link:
https://doi.org/10.3929/ethz-b-000635617

Originally published in:
https://doi.org/10.23919/epe23ecceeurope58414.2023.10264375

Influence of the $r_{ds,on}$ temperature dependency of SiC MOSFETs on the optimal switching cell mechanical layout

Georgios Papadopoulos and Jürgen Biela
Laboratory for High Power Electronic Systems, ETH Zürich
Zürich, Switzerland

Email: papadopoulos@hpe.ee.ethz.ch

***Index Terms*—Converter Design Optimisation, Switching Cell Building Block, Electrothermal model, Standardised Switching Cell, Standardised Half-Bridge arrangement, Thermal Performance.**

***Abstract*—The design of power electronic systems is typically performed based on optimisation procedures. In this paper, the influence of the temperature dependant on-state resistance on the optimal switching cell mechanical layout is investigated. A standardised half-bridge switching cell is modelled and optimised to discuss the importance of establishing general layout recommendations.**

I. Introduction

For the design of power electronic systems various optimisation procedures have been presented for identifying the optimal converter design [1–3]. Often multiple requirements like high power density, high efficiency, low failure rate, and low cost should be fulfilled by the design at the same time. Typically, many of these goals are competing, as for example, the demand for lower losses, which results in higher efficiency, is usually contradictory to designing converters with a higher power density. Therefore, multi-objective and multi-domain optimisation procedures are used in order to evaluate the converter system in various domains, as e.g. electric, electromagnetic, thermal, etc., and to derive the best possible overall design compromise for each application considering the given specifications and constraints [3].

To evaluate and to compare the performance of different converter designs and topologies, accurate and comprehensive models of the system and its components are necessary. These models, which can be based on analytical equations, numerical simulations, or a combination of both, result in a virtual prototype/digital twin of the system that enables the analysis of its behavior and performance from various angles [4]. By using virtual prototypes and simulation tools, it is possible to efficiently evaluate and compare the design and the performance of converters before building a prototype system.

Virtual prototypes of converter systems often include models for various components such as semiconductor devices [5, 6], gate drivers [7], capacitors [8, 9], magnetics [10], and also for the temperature distribution [11], which have been extensively investigated in the literature. Concerning multi-objective optimisation procedures for the mechanical design, the focus has mainly been on optimising the geometry of single components as magnetics [10], or capacitors [8], or of the cooling system for dissipating losses [12]. More recent studies propose also mechanical design optimisation of the switching module [13, 14] and its control scheme [15], or the unified switching cell (SC) block (i.e. power semiconductor devices, gate drivers, decoupling capacitors, and cooling system) as an individual building block [16].

In [13, 14] a multi-objective optimisation tool for the rapid design of power semiconductor modules is presented for optimising the module's layout in terms of performance and power density. This tool includes models of the electrical parasitics and the thermal coupling between the devices. In [16], the switching cell building block (SCBB) is defined and introduced as an aggregated "component" in the converter optimisation procedure. Based on this component, the procedure can be divided into three major building blocks as illustrated in fig. 1. Each building block (i.e. magnetics, capacitors, and switching cell) is described by its electrical model and mechanical dimensions. In case of the SCBB, it is described by an electrical schematic (e.g. half-bridge) and a switching cell mechanical layout (SCML), which has been standardised for a half-bridge in [16]. The standardised SCMLs and the individual component models have been combined in [16] to a detailed electro-thermal model of the SCBB. By using this electro-mechanical model in an optimisation procedure it has been shown

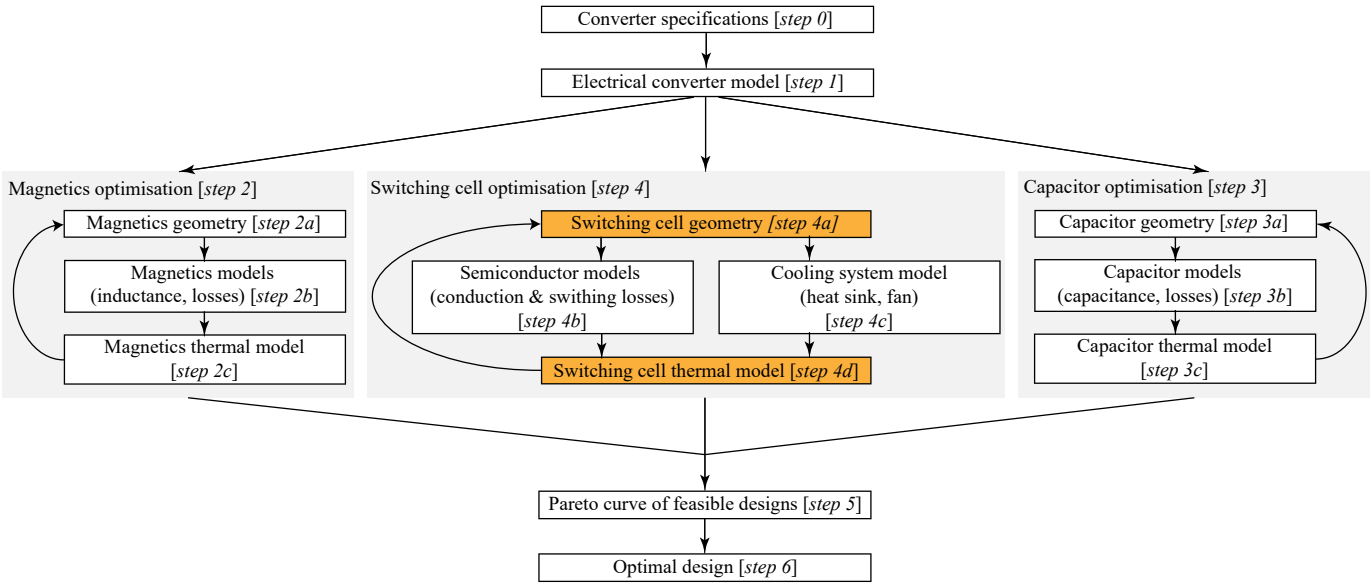

Fig. 1. Proposed converter optimisation procedure including model and optimisation of the converter switching cell.

that there is an optimal arrangement of the switching cell components that results in minimal losses.

So far, the focus of the switching cell mechanical layout has been on investigating the impact of the different parasitic elements (i.e. inductances and capacitances) on the switching behaviour [7, 13], which is also influenced by the semiconductor device's parasitic capacitors as shown in [17]. In this paper, the impact of the temperature dependent on-state resistance on the optimal arrangement of the switching cell components is investigated. This temperature dependency of the on-state resistance can be parametrised based on the device's slope of the on-state resistance with respect to the operating junction temperature $s = dr_{ds,on}/dT_j$. This parametrisation can be used to define a more general layout recommendation for standardised switching cell mechanical layouts.

For demonstrating the impact of the slope of the on-state resistance with respect to the operating junction temperature on the SC mechanical layout, a half-bridge buck converter for a battery interface application is examined as example. For simplicity, and to further narrow down the design space, the focus is on standard TO-247 packages, SOIC-8 integrated gate driver circuits, ceramic decoupling capacitors, 4-layer PCBs with $70\,\mu\mathrm{m}$ copper thickness, and heat sinks with a cooling fan (Table I). However, the basic concept could be also be applied to other components.

In section II, the selected standard geometrical layout of the half-bridge switching cell building block is defined along with its degrees of freedom. In section III, the models and the optimisation procedure of the switching cell building block are presented. In section IV, simulation results of the optimisation of a switching cell mechanical layout are presented, and afterwards in section V, these are validated by FEM simulations. Finally, in section VI, the benefits of expressing the optimal switching cell mechanical layout in terms of the semiconductor device's temperature dependent parameters are discussed, and in section VII, the importance of establishing general layout recommendations for standardised switching cells is highlighted.

II. Degrees of freedom of the standardised switching cell mechanical layout

In order to include the half-bridge switching cell as a building block into the converter optimisation procedure, it is necessary to model the electrical behaviour (i.e. fig. 3) and the mechanical layout (i.e. fig. 2) of the components. The heat sink used to dissipate the power losses from the switching cell, constitutes the bulkiest component of the switching cell. As a result, it is used as a sort of "base/anchor" element for standardising the switching cell mechanical layout (SCML).

The standardised SCML building block, as identified in [16] and shown in fig. 2, is used as an example in this study. The basic degrees of freedom (DOFs) in the design are identified and the models for optimising the building block are presented. The outer dimensions of the switching cell, i.e. its width w_{sc}, length l_{sc}, and height h_{sc}, as well as the distance between the semiconductor switches d_{semi}, are the degrees of freedom for optimising the geometrical arrangement. The height and width of the

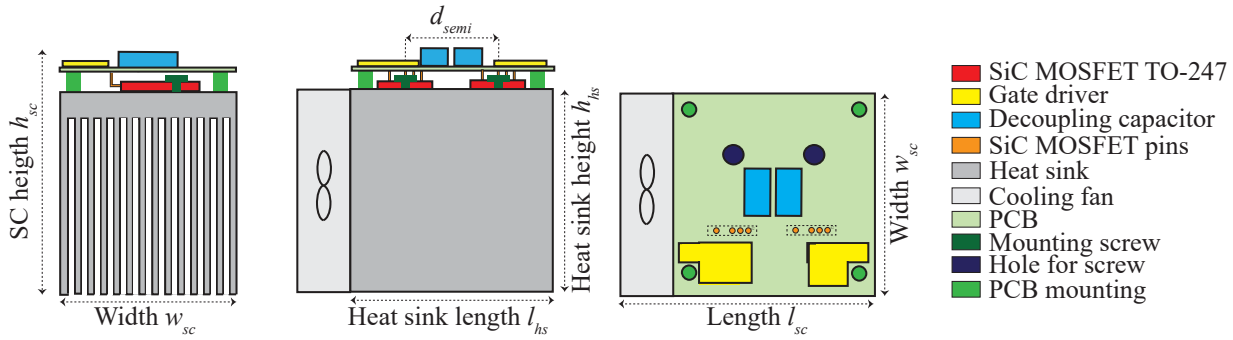

Fig. 2. Degrees of freedom (h_{sc}, w_{sc}, l_{sc}, h_{hs}, l_{hs}, d_{semi}) of the selected SCML.

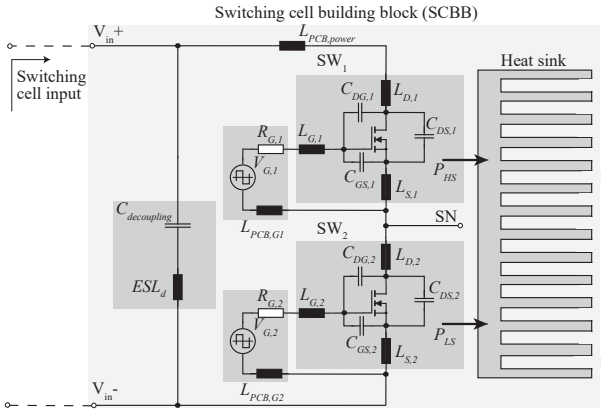

Fig. 3. Basic electrical schematic of a half-bridge switching cell building block (SCBB).

switching cell are mainly determined by the cooling fan's dimensions, but the length of the heat sink, which affects the heat sink's thermal resistance and the switches' operating temperature, needs to be optimised. The semiconductor switches are usually placed in or near the middle of the heat sink to maximise the heat spreading/ dissipation. The placement of the DC-link decoupling capacitors and the switches on the PCB affects the power loop parasitics and the switching losses. Typically, the decoupling capacitors are placed as close as possible to the switches. However, the minimum distance and the routing of the PCB traces/planes are limited by the required clearance distance (shown in fig. 5), which is given as input to the optimisation process based on the converter specifications (i.e. voltage level, pollution degree etc.).

III. Model of the Selected SCML

The flow chart of the proposed procedure for optimising the mechanical layout of the half-bridge switching cell is illustrated in fig. 4. The detailed steps for evaluating the SCMLs in terms of parasitics, losses, and cooling system design are explained in the following.

TABLE I
Considered components, packages, and dimensions for standardising SCMLs of half bridge converters.

Component	Package/type
Semiconductor switch	TO-247
Gate driver IC	SOIC-8
Decoupling capacitor	Ceramic 2225
SMD driver resistors/capacitors	1210
Mounting device	Screw
Forced cooling fan	Quadratic fan 40x40 mm
PCB layers	4
PCB copper thickness	70 μm

- **Step 1**: Select a SCML based on the system requirements and the qualitative evaluation presented in [16]. In the following, the SCML illustrated in fig. 2 is considered as example.
- **Step 2**: Derive the mechanical constraints for the optimisation variables based on the selected SCML. For example, in the selected SCML (fig. 2) the length of the heat sink l_{hs} must be greater than the sum of the width of the switches and the distance between their centres (d_{semi}) in order to ensure proper mounting on the heat sink.
- **Step 3**: Select a specific semiconductor device based on the converter specifications (voltage, current) and cost, e.g. from a database.
- **Step 4**: Select decoupling capacitors based on the analysis presented in [9, 16]. The minimum recommended capacitance value $\geq$ 50 times the output capacitance of the selected semiconductor switch at DC-link voltage. In the considered optimisation procedure, the maximum number of parallel capacitors fitting on the available PCB space is selected in step 4 in order to minimise the power loop parasitic inductance and at the same time fulfil the lower boundary for the decoupling capacitor: $C_{decouple} \geq 50 \cdot C_{OSS}$.
- **Step 5**: Select gate driver IC and gate resistors based on the specifications of the selected semiconductor device.

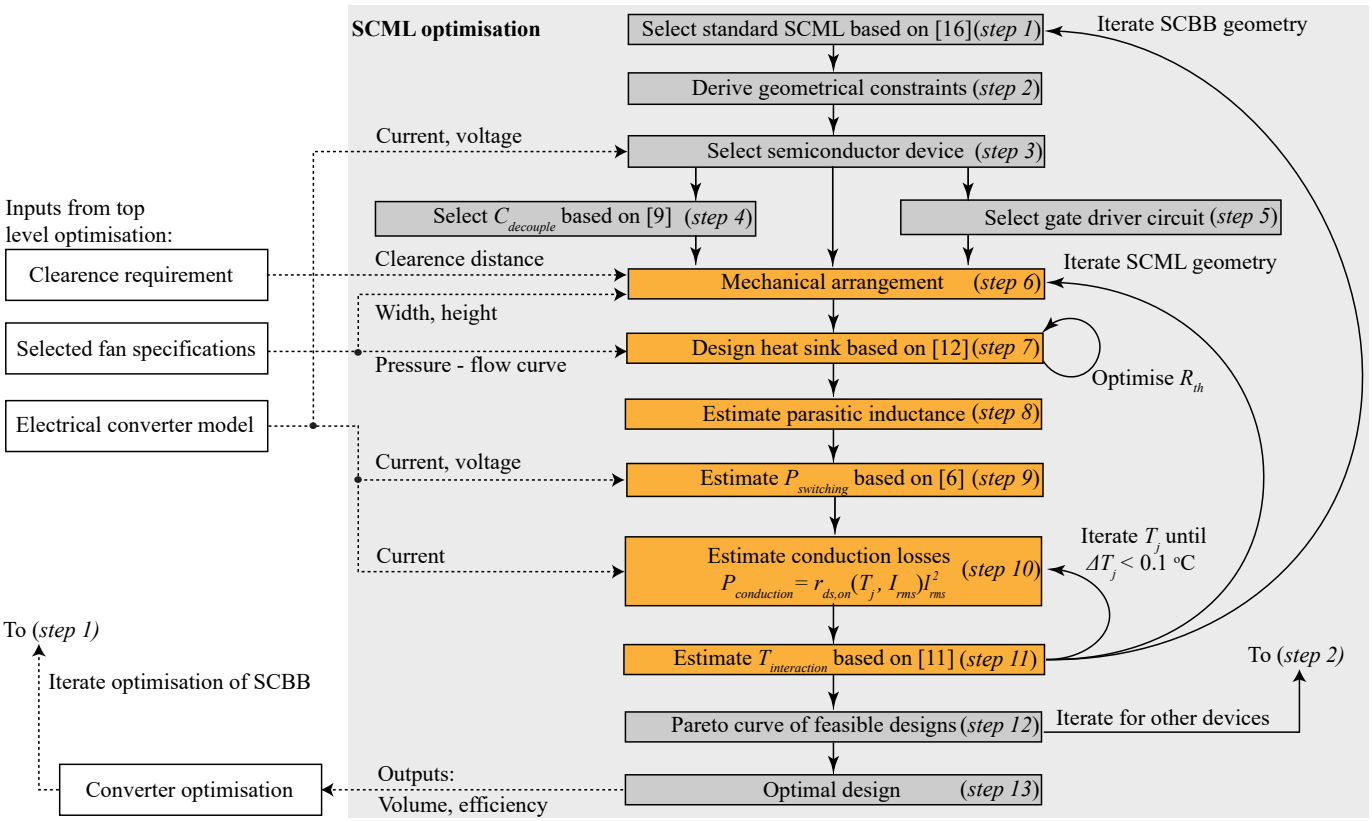

Fig. 4. Switching cell optimisation procedure based on an electro-thermal model with forced air cooling.

- **Step 6**: Mechanically "arrange" the components in the virtual prototype and the selected SCML based on the geometrical parameters illustrated in fig. 2. The width w_{sc} and the height h_{sc} of the switching cell are determined based on the dimensions of the selected cooling fan, which is given as input in the optimisation routine. The gate driver is mounted on the PCB as close as possible to the semiconductor switch to minimise the parasitic gate loop inductance. The PCB traces and planes illustrated in fig. 5 are routed according to the electrical schematics (fig. 3), the clearance distance and the number of PCB layers. The limit of the maximum current density for the PCB traces is set to $50\,\mathrm{A/mm^2}$ for the external layers and $20\,\mathrm{A/mm^2}$ for the internal layers. The length l_{sc} of the switching cell and the distance between the semiconductors d_{semi} are adjusted during the optimisation procedure to optimise the SCML.
- **Step 7**: For the heat sink's outer dimensions l_{hs}, w_{hs} and h_{hs}, which result in step 6, optimise locally the remaining heat sink geometrical parameters, i.e. base plate thickness d_{hs}, channel width s_{hs}, fin length c_{hs}, fin width t_{hs}, and the number of channels n_{fins} in order to minimise the thermal resistance of the heat sink $R_{th,hs}$ and the cooling fan power losses as described in [12, 16].

To account for the fact that the size of the heat source (semiconductor switch) is relatively small compared to the size of the heat sink's plate, an equivalent spreading resistance is considered as described in [18].

$$R_{th,sp} = \frac{\Psi_{max}}{\lambda_{al} r_1 \sqrt{\pi}} \tag{1}$$

There, r_1 is the equivalent radius of the heat source (semiconductor switch), λ_{al} the thermal conductivity of the aluminium heat sink, and Ψ_{max} is the dimensionless constriction resistance derived based on the Biot number and the dimensions of the heat-sources and the heat sink's plate as described in [18].

In the total thermal resistance of the system, the thermal resistance $R_{th,gr}$ of the thermal grease used to thermally couple the semiconductor switch to the heat sink at the mounting position is also considered.

$$R_{th,gr} = \frac{d_{gr}}{\lambda_{gr} l_{semi} w_{semi}} \tag{2}$$

There, d_{gr} is the assumed thickness of the thermal grease, λ_{gr} its thermal conductivity, l_{semi} and w_{semi}

the length and width of the switch's package respectively. Thus, the total thermal resistance of the system is calculated by adding the case to junction thermal resistance $R_{th,cj}$ given in the semiconductor's datasheet.

$$R_{th,system} = R_{th,hs} + R_{th,sp} + R_{th,gr} + R_{th,cj} \quad (3)$$

- **Step 8**: Estimate the PCB power and gate loop inductances based of the considered PCB layout given in fig. 5. For simplifying the calculation, the single trace/plane inductance formula: $L_{dc} = \mu_r \cdot \frac{d_t l_t}{w_t}$ is used as an approximation, where $\mu_r = 1$ is the assumed relative permeability of copper and d_t, l_t, as well as w_t are the thickness, the length and the width of the single trace/plane. To improve the accuracy of the estimated inductances, refined parasitic inductance models can be used. The gate loop is defined by the closed loop connecting the gate and the source of each semiconductor with the driver IC, the gate resistor, and the gate driver's supply capacitor. The power loop is the closed loop connecting the DC-link decoupling capacitors with the drain and the source pins of the semiconductors. The PCB power loop parasitic inductance is approximately given by:

$$L_{PCB,power} = L_{PCB,D} + L_{PCB,S} + L_{PCB,DS} + ESL_d/n_{decouple} \quad (4)$$

  The approximation of the parasitic inductances is based on the PCB layout given in fig. 5.
- **Step 9**: The switching losses of each semiconductor switch are estimated as described in the model presented in [6] independently of the junction temperature based on the semiconductors' typical capacitances, the selected gate driver (gate-source voltage and gate resistors), the parasitic inductances estimated on step 8 as well as the operational voltage and current. The voltage and current waveforms are given as inputs (e.g. in piecewise linear (PWL) format), to the optimisation routine from the electrical model of the converter.
- **Step 10**: Calculate the conduction losses with $P_{conduction} = r_{ds,on}(T_j, I_{rms}) \cdot I_{rms}^2$ based in the first step on an assumed operation junction temperature T_j and the RMS current of each switch, which is calculated based on the current waveform given as input based on the electrical model of the converter. The semiconductor's on-resistance $r_{ds,on}$ is derived as function of the operational temperature and the current from the respective conductance curves in the datasheet. The PCB traces/planes conduction losses are also calculated in this step, by summing the resistance of each simplified single section of the PCB layout presented in fig. 5 based on the copper resistivity ρ_{cu}:

$$r_{dc,pcb} = \rho_{cu} \cdot \frac{l_t}{d_t \cdot w_t} \cdot \Big(1 + \big(\theta_{cu} \cdot (T_j - T_{amb})\big)\Big) \quad (5)$$

- **Step 11**: The mutual heat coupling between the two switches is estimated based on the heat spreading model for the isotropic base plate as described in [11, 16].
  Assuming a linear thermal model, the junction temperature of each switch is derived based on:

$$T_{j,i} = (P_{conduction,i} + P_{switching,i}) R_{th,system} + T_{interaction,k\to i} + T_{amb} \quad (6)$$

  There, $T_{interaction,k\to i}$ is the superimposed temperature rise of the i-th semiconductor switch, caused by the conduction and switching losses of the k-th semiconductor switch, and the variable T_{amb} is the ambient temperature. The calculated junction temperature is iterated between step 10 and 11 until the relative error between the assumed junction temperature at step 10 and the calculated one is smaller than $0.1\,^{\circ}\mathrm{C}$.
- **Step 12**: Derivation of the pareto-front curves for the feasible geometries, where the junction temperature does not exceed the maximum allowed junction temperature: $T_{j,max} = 150\,^{\circ}\mathrm{C}$, minus a margin, which is chosen to be $10\,^{\circ}\mathrm{C}$ in the considered case. At this point additional optimisation iterations are performed for various slopes $s = dr_{ds,on}/dT_j$.
- In the final step, the best design is chosen based on the system volume and efficiency requirements. The output of the suggested routine can be linked to a converter system optimisation, where the SCBB is optimised based on the proposed models for several SCMLs, cooling fans or topologies.

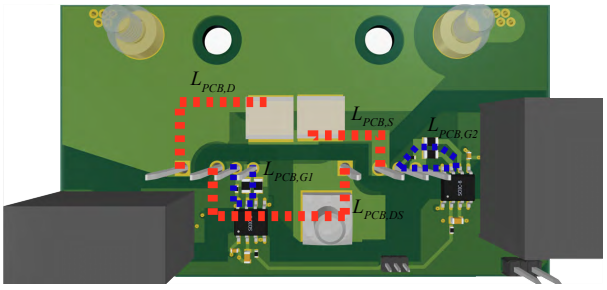

Fig. 5. Considered simplified sketch of the power and the gate loop on a 4-layer PCB for calculating the parasitic loop inductances (step 8 in fig. 4).

TABLE II
STANDARD BUCK CONVERTER SPECIFICATIONS WITH OUTPUT POWER $P_{out} = 540\,\text{V} \cdot 40\,\text{A} = 21.6\,\text{kW}$.

Parameter	Symbol	Value
Input voltage	V_{in}	800 V
Output voltage	V_{out}	540 V
Output current	I_{out}	40 A
Ripple voltage	ΔV_{pp}	$< 5\,\%$

IV. Optimisation results for the selected SCML

In order to demonstrate the application and performance of the presented modelling and optimisation of the SCML, a DC-DC converter for an electric vehicle charger with the specifications given in Table II is used as an example. The results of the optimisation for the selected components presented in Table III are illustrated in figs. 6 and 7. Fig. 6 depicts the pareto front power losses vs. volume and the selected design point for the SC. In fig. 7 it is illustrated, that there is an optimal distance between the two semiconductor switches for the selected standard SCML, where the power losses of both semiconductor switches are minimised. The power losses initially decrease with an increasing distance between the switches due to two main reasons. The first reason is the initial decrease of the switching losses due to the impact of the clearance distances, which results in thinner PCB traces/planes, and thus, higher parasitic inductances for short distances d_{semi}. The second reason is because of the mutual heat coupling between the two switches, which exponentially reduces with increasing distances.

At larger distances d_{semi}, the increasing distance between the semiconductors results again in higher power losses due to increasing power loop parasitic inductance, which results in higher switching losses. Consequently, there is an optimal distance for minimal losses.

This optimal distance is highly dependent on the dependency of the on-state resistance of the semiconductor switch with respect to its junction temperature. As shown in fig. 8, the optimal distance for minimal losses on a switching cell with predefined cooling fan and length is linearly dependant to the $dr_{ds,on}/dT_j$ slope s and thus, to the total power losses. The point highlighted by a green arrow in the graph represents the optimal

TABLE III
CHOSEN COMPONENTS FOR OPTIMISING THE SELECTED SCML GIVEN IN FIG. 2.

Component	Manufacturer	Product number
Switch	Infineon	IMZA120R020M1H
Gate driver IC	Infineon	1EDI60N12AF
Decoupling cap.	KEMET	C2225C104KFRACAUTO
Cooling fan	Sanyo Denki	9GA0412P6G001

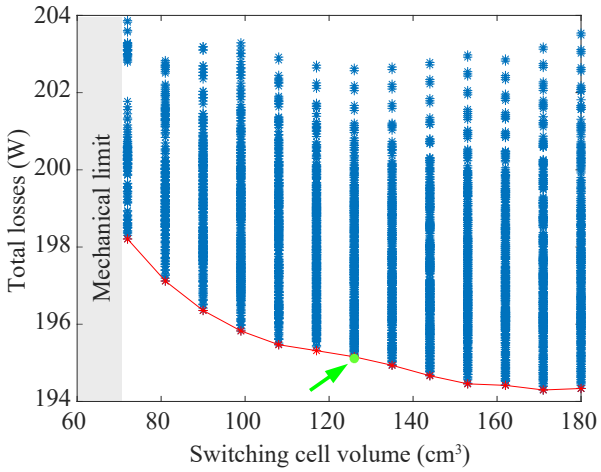

Fig. 6. Pareto front losses-volume of the half-bridge SC with a 40x40 mm cooling fan. The point highlighted in green is the selected SC for which the analysis in fig. 7 and fig. 8 is performed.

point with minimal losses illustrated in fig. 7 and the remaining/other points are derived for varying slopes s of the semiconductor's $r_{ds,on}$ with respect to its junction temperature. In case of a relatively low dependency of the on-state resistance on the junction temperature (i.e. a small slope s), the optimal distance is mainly affected by the constrains determined by the clearance distance and, thus, the optimal distance is relatively independent of the slope as could be seen in the three horizontal values highlighted in orange in fig. 8.

The correlation of the optimal distance to the slope s also depends on the length of the switching cell's heat sink l_{HS}. As shown in fig. 9, the two semiconductor switches of the half bridge SC need to be placed further apart to achieve the optimal SC design in terms of efficiency when longer heat sinks are used. With longer heat sinks the cooling system's performance is improved, which is resulting in lower total thermal resistance of the system.

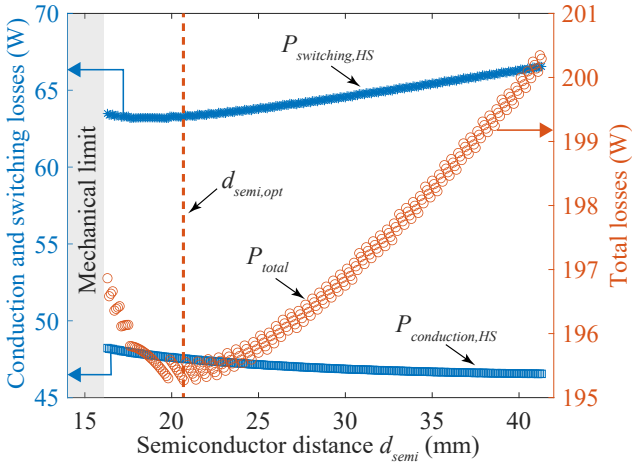

Fig. 7. Total as well as high-side switch losses in the half-bridge SC with a 40x40 mm cooling fan and a length of 70 mm.

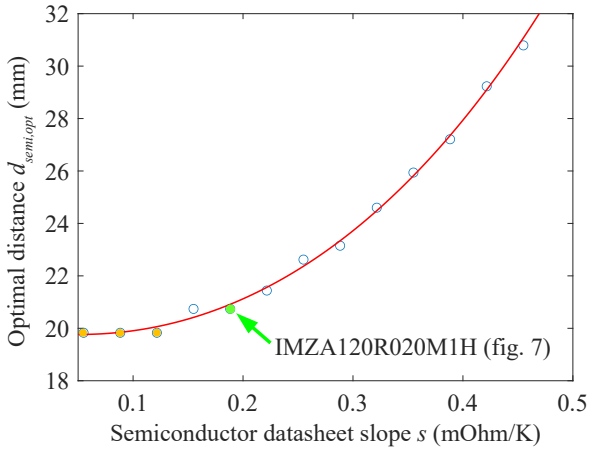

Fig. 8. Optimal distance d_{semi} between the two semiconductor devices derived for various slopes $s = dr_{ds,on}/dT_j$ in the half-bridge SC with a 40x40 mm cooling fan and a length of 70 mm.

Reducing the thermal resistance of the system decreases the impact of the thermal coupling between the switches. This is because the thermal link between the two devices is kept approximately constant, while the thermal resistance of each device to the ambient is reduced. Therefore, the thermal coupling between the switches becomes less significant at the SC level, resulting in reduced temperature interaction between the two devices for the same distance between them.

As a consequence of this reduced temperature interaction, the slope in fig. 7 for reducing the conduction losses becomes steeper as the distance between the semiconductors increases. On the other hand, the slope of the increasing switching losses with respect to the distance between the two devices remains the same since the switching losses are assumed to be independent of the junction temperature.

Therefore, the optimal distance between the semiconductor switches is achieved at higher distances, where the reduction in thermal coupling outweighs the increase in switching losses due to the increased distance. This means that the impact of the heat sink length on the optimal component placement becomes more significant when semiconductor switches with a higher slope s are chosen. With an increased temperature dependency of the on-state resistance necessitates a further reduction of the thermal coupling between the switches is necessary, what results in a higher optimal distance.

As shown in fig. 7, the total losses and the switching losses are following the same trend when d_{semi} is increased. Initially, they are both reduced, as already discussed. The switching losses decrease due to the impact of the clearance distance on the parasitic inductances and the total losses decrease due to the combination of the clearance distance and the thermal interaction between the two switches. Despite following a similar trend, the point that both switching and total losses are minimal is shifted up and right in the graph when devices with an increased s are used. This shift depends mainly on the increase of the $r_{ds,on}$ resistance of the MOSFET with temperature, and it can be expressed with a linear correlation between the optimal distance between the MOSFETs and the slope s of the on-state resistance with respect to the junction temperature, which is proportional to the switching cell's total losses.

V. Validation of Thermal Model by FEM

In this section, simulation results based on an electro-thermal FEM and CFD (computational fluid dynamics) simulation for the optimised SCML (marked as green point in fig. 6) are presented for validating the electro-mechanical model described in section III.

Initially, a universal geometrical model of a switching cell parametrised based on the selected cooling fan is implemented in FEM. This switching cell is simulated for various distances between the switches in order to validate the proposed analytical model. In the FEM model, the on-resistance of the selected semiconductor switch is implemented as a function of the operating current and temperature. Additionally, the switching losses are implemented as a function of the estimated parasitics based on the designed geometry of the SC. The performance of the cooling fan is determined based on the CFD analysis performed with the assumption of having laminar flow in the channels.

The temperature distribution of the optimised half-bridge SC with 40x40 mm cooling fan and length of 70 mm is illustrated in fig. 10. The validation of the ther-

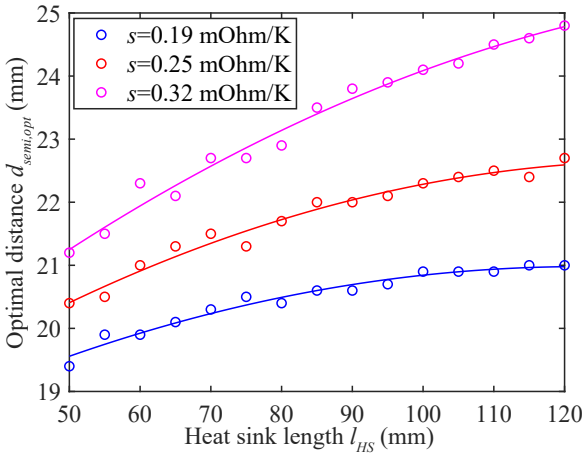

Fig. 9. Optimal distance d_{semi} between the two semiconductor devices derived for various slopes $s = dr_{ds,on}/dT_j$ and heat sink lengths l_{HS} in the half-bridge SC with a 40x40 mm cooling fan.

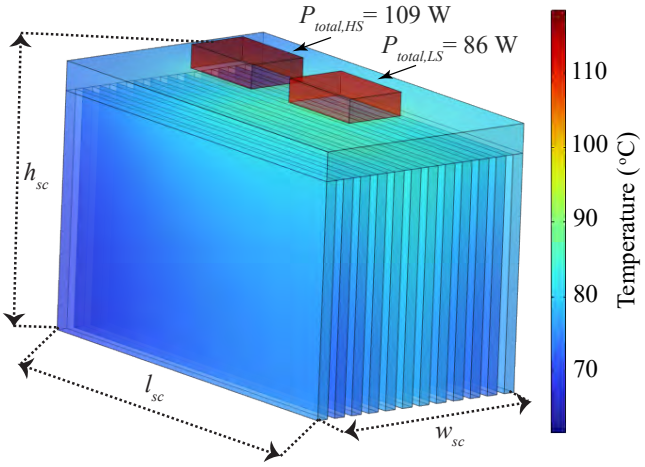

Fig. 10. Temperature distribution of the optimised half-bridge SC with 40x40 mm cooling fan and length of 70 mm.

mal model (thermal resistance and mutual heat coupling) is performed by comparing the operating temperatures of the semiconductor switches resulting from the analytical and the FEM model for several distances of the two devices.

The resulting operating temperature of a semiconductor switch of the half-bridge SC as a function of the SC's length and distance between the semiconductors is illustrated in fig. 11 as example. As illustrated in the figure, the results from the analytical model are very close to the results derived from FEM.

VI. Discussion

The SCML optimisation procedure presented in section III and thermally validated with FEM in section IV can be time-consuming, especially when multiple semiconductor devices and cooling fans are considered. To simplify this process, a look-up table of the optimal distance with respect to the semiconductor's slope s

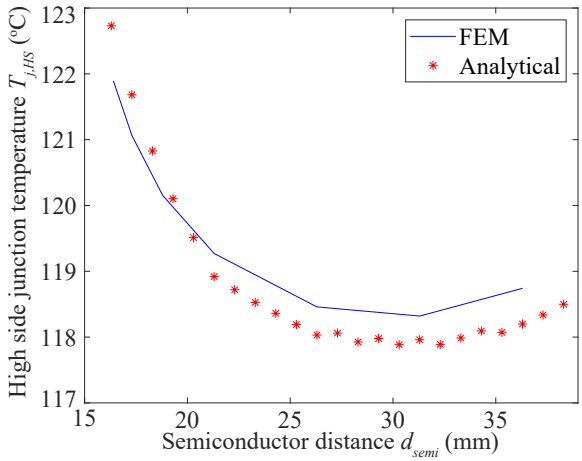

Fig. 11. Operating temperature of a switch of the half-bridge SCs with a length of 70 mm as a function of the semiconductor distance at an ambient temperature $T_{amb} = 20\,°C$.

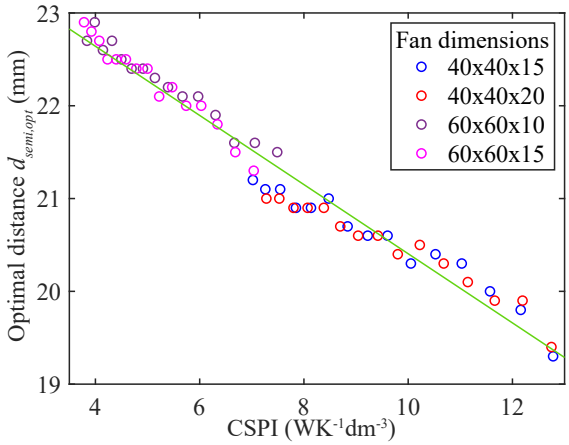

Fig. 12. Optimal distance d_{semi} between the two semiconductor devices derived for various Cooling System Performance Index (CSPI) in the half-bridge SC with 40x40 mm and 60x60 mm cooling fans presented in Table IV.

given in the datasheet can be created from the results of the optimisation procedure, which can be used to reduce the number of steps involved. By using the look-up table as a pre-conditioning of the optimisation parameters in the optimisation procedure presented in fig. 4, developers can significantly reduce the number of iterations required between step 6 and 11.

In cases where the same cooling fan is used, the optimal distance between two semiconductor devices can be determined based on the slope s of their on-state resistance with respect to junction temperature, as given in the datasheet. This eliminates the need to rerun the full optimisation procedure for the same SCML design. However, when using different cooling fans or when selecting another point on the Pareto front (fig. 6), the look-up table and optimal distance can still be used as a pre-conditioning of the optimisation parameters in the optimisation procedure.

A parameter which could be used to pre-condition the optimisation parameters and give an initial indication of the optimal switching cell mechanical layout is the Cooling System Performance Index (CSPI) as defined in [19], which represents the volumetric thermal conductivity of the cooling system. As it is shown in fig. 12, a lower value of CSPI which entails a better cooling

TABLE IV
Considered cooling fans for examining the impact of the cooling system on $d_{semi,opt}$.

Product number	Dimensions
9GA0412P7G001	40x40x15 mm
9GA0412P6G001	40x40x20 mm
9GA0612G9001	60x60x10 mm
9GA0612P7G01	60x60x15 mm

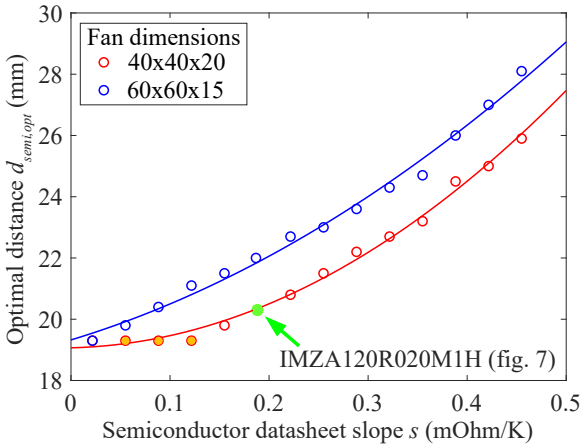

Fig. 13. Optimal distance d_{semi} between the two semiconductor devices derived for various slopes $s = dr_{ds,on}/dT_j$ in the half-bridge SC with 40x40 mm and 60x60 mm cooling fans presented in Table IV.

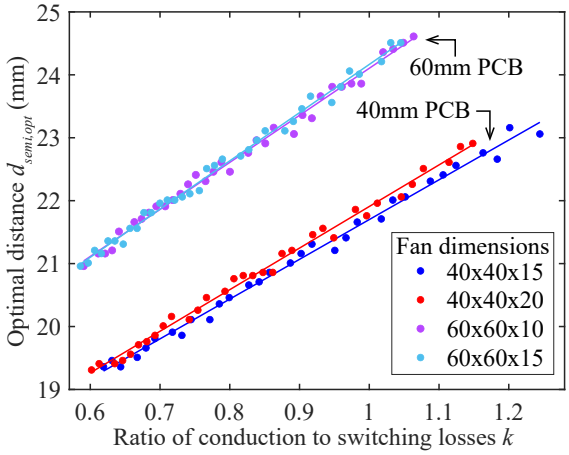

Fig. 14. Optimal distance d_{semi} between the two semiconductor devices derived for various conduction to switching losses ratios $k = P_{cond}/P_{sw}$ assuming nearly constant sum of the total losses in the half-bridge SC with 40x40 mm and 60x60 mm cooling fans presented in Table IV.

system performance would result in increased optimal distance between the two semiconductor switches. As it has already been discussed for fig. 9, an improved cooling system performance increases the importance of reducing the thermal coupling between the two semiconductor switches in order to achieve an optimised SCML. Therefore, the optimal distance between the two switches is inverse proportional to the CSPI.

Fig. 13 demonstrates that using a better cooling fan (60x60x15 mm), which corresponds to a lower CSPI, leads to an optimised SCML design where the semiconductor switches need to be placed further apart compared to the case of a weaker cooling fan (40x40x20 mm). In both cases, a linear correlation is observed between the optimal distance between the semiconductor switches and the slope s of their on-state resistance with respect to the junction temperature.

The main difference between the two graphs given in fig. 13 lies in the effect of the clearance distance constraints on the correlation between the slope and the optimal distance. In the case of a 40x40 mm cooling fan, the optimal distance remains independent of the slope for a low temperature dependency of the on-state resistance, as indicated by the three horizontal values highlighted in orange. However, with a 60x60 mm cooling fan, there is a linear correlation between the slope and the optimal distance for the entire range. A possible reason for this difference is that when using a 60x60mm cooling fan, the width of the SC's PCB is also 60mm. This allows for wider PCB power and gate loop paths, resulting in reduced parasitic inductances and, consequently, lower switching losses.

Fig. 14 illustrates that the optimal distance between the two semiconductor devices has a linear dependency on the ratio of conduction to switching losses $k = P_{\text{conduction}}/P_{\text{switching}}$. In order to evaluate the impact of the ratio k on the optimal design, k is varied in the presented points for each cooling fan while the sum of conduction and switching losses is kept approximately constant. In this ratio, the conduction losses are influenced by temperature and can be directly linked to the slope s of the on-state resistance with respect to the junction temperature given in the datasheet. On the other hand, the switching losses are linked to the parasitic inductances of the PCB and the parasitic capacitors of the semiconductor devices.

Therefore, in terms of optimising the SCML design, these findings provide further justification for the observed correlation between the optimal distance of the semiconductor devices and to the temperature dependency of the on-state resistance $r_{ds,on}$, as well as on the parasitic inductances and capacitances in both the PCB and the semiconductor devices. The importance of PCB parasitic inductances in optimising SCML can be observed from the shift of the curves when improving the cooling system by using a 60x60 mm fan. This shift is primarily due to the reduction of the parasitic inductances resulting from using wider tracks enabled by the 60 mm PCB, and secondarily due to the improved cooling system.

To simplify the design procedure, the identified correlations could be used to create a database with look-up tables for the optimal distances between semiconductor devices with respect to the slope s (given in the datasheet) to the considered cooling fans and to the switching cell volume. By running the complete switching cell optimisation procedure shown in fig. 4 once, using a specific set of cooling fans, the neces-

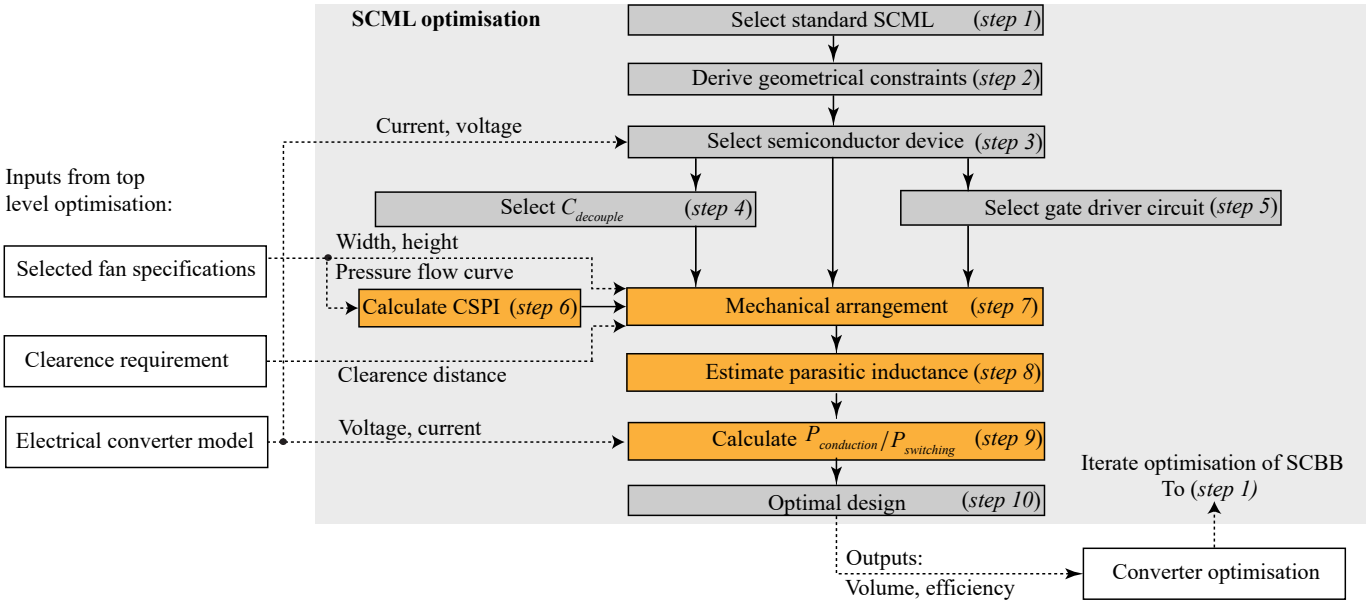

Fig. 15. Simplified switching cell optimisation procedure based on look-up tables database derived using the optimisation procedure presented in fig. 4.

sary database with look-up tables can be derived. This database can then be integrated into the switching cell optimisation procedure, as illustrated in fig. 15. The highlighted steps in orange in fig. 4 are replaced by the corresponding highlighted steps in orange in fig. 15.

As shown in fig. 15, this approach allows to determine the optimal layout of the switching cell using the datasheet value of the slope s for the selected semiconductor device, together with the cooling fan's width and the CSPI, as well as the slope of switching losses in relation to the parasitic inductances of the PCB, and the ratio of conduction to switching losses. Implementing this process significantly simplifies the optimisation procedure, particularly since the optimised SCBB can be directly derived from the datasheet values of the chosen semiconductor device and the employed cooling system. With the simplified procedure the switching cell and, eventually the converter system can be optimised more efficiently, as the computationally intensive analytical models are replaced with look-up tables in the top level converter optimisation. This leads to an improved performance and reduced development costs.

VII. Conclusion

In this paper, a standardised switching cell is modelled and introduced as an additional building block in the converter optimisation procedure. This standardised switching cell is composed of individual component models (power semiconductors, heat sink, parasitics, DC-link decoupling capacitors, gate drivers). It is described by an electrical schematic and a mechanical layout. The mechanical layout of the switching cell is standardised for including it in an electro-mechanical model, which is used to optimise the switching cell building block design.

An example of a buck converter design is used to demonstrate the benefits of modelling and optimising the switching cell mechanical layout and to prove that there is an optimal design of the switching cell with minimal losses, which can be parametrised independent of a specific switch. The results indicate that by optimising the mechanical layout of the switching cell, a reduction of $4-5\,^{\circ}\mathrm{C}$ of the junction temperature can be achieved leading to an improved efficiency and a longer lifetime for the converter system. In the examined example the total power losses of the switching cell has been reduced by $1\,\%$ compared to the common recommendation of placing them as close as possible through the optimal placement of the selected components.

The design of the switching cell is primarily influenced by the datasheet slope s of the semiconductor switch, which describes the increase in on-state resistance with temperature. This correlation, combined with the impact of the cooling system performance, emphasises the importance of establishing general layout recommendations for standardised layouts based on the selected components. These general layout recommendations can be formulated as look-up tables, which would speed up the process of designing optimised switching cells and, ultimately, converter systems.

References

[1] A. Stupar, T. McRae, N. Vukadinović, A. Prodić, and J. A. Taylor, "Multi-objective optimization of multi-level DC–DC converters using geometric programming," *IEEE Trans. on Power Electronics*, vol. 34, no. 12, 2019.

[2] R. Burkart and J. W. Kolar, "Component cost models for multi-objective optimizations of switched-mode power converters," in *IEEE Energy Conversion Congress and Exposition (ECCE USA)*, 2013.

[3] S. Waffler, M. Preindl, and J. W. Kolar, "Multi-objective optimization and comparative evaluation of Si soft-switched and SiC hard-switched automotive DC–DC converters," in *Industrial Electronics Annual Conference (IECON)*, 2009.

[4] J. Biela, J. W. Kolar, A. Stupar, U. Drofenik, and A. Müsing, "Towards virtual prototyping and comprehensive multi-objective optimisation in power electronics," in *International Exhibition & Conference for Power Electronics Intelligent Motion Power Quality (PCIM)*, 2010.

[5] D. Christen and J. Biela, "Analytical switching loss modeling based on datasheet parameters for SiC MOSFETs in a half-bridge," *IEEE Trans. on Power Electronics*, vol. 34, 2019.

[6] A. Hu and J. Biela, "An analytical switching loss model for a SiC MOSFET and schottky diode half-bridge based on nonlinear differential equations," in *European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, 2021.

[7] M. Nagel, S. Race, I. Kovacevic-Badstuebner, T. Ziemann, and U. Grossner, "Virtual PCB layout prototyping: Importance of modeling gate driver and parasitic capacitances," in *IEEE Design Methodologies Conference (DMC)*, 2022.

[8] D. Menzi, D. Bortis, G. Zulauf, M. Heller, and J. W. Kolar, "Novel iGSE-C loss modeling of X7R ceramic capacitors," *IEEE Trans. on Power Electronics*, vol. 35, 2020.

[9] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of DC-link decoupling capacitors," in *IEEE Energy Conversion Congress and Exposition (ECCE USA)*, 2013.

[10] M. Stojadinović and J. Biela, "Modelling and design of a medium frequency transformer for high power DC–DC converters," in *International Power Electronics Conference (IPEC - ECCE Asia)*, 2018.

[11] Y. Muzychka, J. Culham, and M. Yovanovich, "Thermal spreading resistance of eccentric heat sources on rectangular flux channels," *Journal of Electronic Packaging*, vol. 125, 2003.

[12] D. Christen, M. Stojadinovic, and J. Biela, "Energy efficient heat sink design: Natural versus forced convection cooling," *IEEE Trans. on Power Electronics*, vol. 32, 2017.

[13] I. Al Razi, Q. Le, T. M. Evans, H. A. Mantooth, and Y. Peng, "Powersynth 2: Physical design automation for high-density 3-d multichip power modules," *IEEE Trans. on Power Electronics*, vol. 38, 2023.

[14] Q. Le, M. M. Hossain, T. Evans, Y. Peng, and H. A. Mantooth, "Thermal runaway mitigation through electrothermal constraints mapping for mcpm layout optimization," in *IEEE Design Methodologies Conference (DMC)*, 2022.

[15] L. Zhou, M. Eull, and M. Preindl, "Optimization-based estimation and model predictive control for high performance, low cost software-defined power electronics," *IEEE Trans. on Power Electronics*, vol. 38, 2023.

[16] G. Papadopoulos and J. Biela, "Standardised switching cell building block for converter design optimisation with detailed electro-thermal model," in *European Conference on Power Electronics and Applications (EPE - ECCE Europe)*, 2022.

[17] A. Hu and J. Biela, "Verification and application of an analytical switching loss model for a SiC MOSFET and schottky diode half-bridge," in *International Power Electronics Conference (IPEC - ECCE Asia)*, 2022.

[18] S. Lee and K. P. Moran, "Constrtiction/spreading resistance model for electronics packaging," in *Thermal Engineering Joint Conference (ASME-JSME)*, 1995.

[19] U. Drofenik, G. Laimer, and J. Kolar, "Theoretical converter power density limits for forced convection cooling," in *International Exhibition & Conference for Power Electronics Intelligent Motion Power Quality (PCIM)*, 2005.