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ENERGY EFFICIENT ANALOG MIXED-SIGNAL FRONT ENDS FOR CNT-FET NO$_2$ AIR-QUALITY NANOSENSORS

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"Rien ne pousse à l'ombre des grands arbres"

Constantin Brâncuși

Abstract

Alongside climate change, air pollution is one of the most concerning public health topics of the 21st century. Statistics estimate that more than seven million people die from air pollution yearly, especially in low- and middle-income countries, where people suffer from the highest exposure. Inhalable micrometer particulate matter ($PM_{2.5}$ and PM_{10}), nitrogen dioxide (NO_2), ozone (O_3), sulfur dioxide (SO_2), and carbon monoxide (CO) are the most common pollutants, permanently monitored by World Health Organization (WHO). The six pollutants mentioned above are the main causes of a few million premature deaths annually and NO_2 is one of the most important pollutants in the eye of public health. WHO's new guidelines recommend an NO_2 average level that should not exceed $107\,ppb$ hourly, and $5\,ppb$ annually.

This thesis tackles the NO_2 monitoring problem by employing carbon nanotube field-effect transistors (CNT-FETs) as sensing elements, hence extending the ubiquitous Internet-of-Things (IoT) applications, i.e., novel air quality monitoring systems. The first prototype design proposes an embedded system that can interface up to four CNT-FETs and may expand the IoT domain for environmental and lifestyle applications. The platform performance is demonstrated using a CNT-FET nanosensor, exposed to NO_2 gas concentrations from $200\,ppb$ down to $1\,ppb$. The sensor signals are measured for NO_2 concentrations as low as $1\,ppb$, achieving a 3σ limit of detection (LOD) of $23\,ppb$ with an R^2 linear fit coefficient of 0.95. Although this prototype offers custom configuration, i.e., range, bandwidth, sampling rate, acquisition time intervals, SD card, and Bluetooth Low Energy (BLE) connection, its average power consumption of $64.5\,mW$ is relatively high.

Increasing the system's power efficiency and downscaling its physical dimensions towards a fully integrated circuit (IC) is highly desired. Consequently, this thesis further presents the concept, design, and realization of an integrated signal acquisition system as a second prototype. The research advances a front-end mixed-signal solution composed of an adjustable CNT-FET voltage bias with a $28\,mV$ step, which controls a regulated cascode for the current mode readout. This stage is followed by a transimpedance amplifier (TIA) with $109\,dBOhm$ gain, $0.75\,pA/\sqrt{Hz}$ noise, $4\,\mu A$ input range with

noise filtering included, and differential output. The latter is connected to a $9\,bit$ SAR ADC of $91.7\,fJ/conv$. The design is realized in $180\,nm$ CMOS technology and occupies a silicon area of $0.18\,mm^2$. When supplied at $1.8\,V$, the system consumes an average power of $4.04\,\mu W$ at an ADC sampling rate of $2.66\,kSps$ and $200\,ppb$ of NO_2 gas concentration. The CNT-FET nano-sensor connected to the proposed IC demonstrates NO_2 gas concentration measurements from $0\,ppb$ to $200\,ppb$ in humid air, i.e., $50\,\%$ R.H. Lab measurement results shows that the full acquisition system achieves a 3σ LOD of $18.5\,ppb$ with an R^2 of 0.8. The integration of the IC and the CNT-FET as a part of a wireless sensor node, consuming an estimated power of $378\,\mu W$, is currently under development. This research presents the development of the prototypes and the demonstration of battery-powered air quality monitoring systems. Still, no comprehensive study characterizing the gas sensor was carried out in this context.

Zusammenfassung

Nebst dem Klimawandel stellt die Luftverschmutzung eines der besorgniserregendsten Themen der öffentlichen Gesundheit des 21. Jahrhunderts dar. Statistiken schätzen, dass jährlich mehr als sieben Millionen Menschen aufgrund von Luftverschmutzung sterben; dies ist insbesondere der Fall in Ländern mit niedrigem und mittlerem Einkommen, in welchen die Menschen stärkerer Luftverschmutzung ausgesetzt sind. Zu den sechs häufigsten Schadstoffen, welche laufend von der Weltgesundheitsorganisation (WHO) überwacht werden und als Haupterreger für Gesundheitsrisiken und Todesfälle gelten, gehören der einatembare Feinstaub im Mikrometerbereich ($PM_{2.5}$ und PM_{10}), Stickstoffdioxid (NO_2), Ozon (O_3), Schwefeldioxid (SO_2) und Kohlenmonoxid (CO). Einer der besorgniserregendsten Schadstoffe, welcher in die Aufmerksamkeit der öffentlichen Gesundheit gerückt ist, ist NO_2. Zur Prävention der öffentlichen Gesundheit empfehlen die neuen Richtlinien der WHO Maximalrichtwerte für die oben genannten Schadstoffe. Basierend auf diesen Richtlinien lassen sich die folgenden Grenzwerte für den Schadstoff NO_2 entnehmen: der Durchschnitt pro Stunde sollte $107\,ppb$ nicht überschreiten, während der jährliche Durchschnittswert nicht höher als $5\,ppb$ sein sollte.

Problemstellung dieser Arbeit ist es, eine Lösung zur Überwachung der NO_2 Partikel in der Luft zu erarbeiten. Basis dieses IoT-basierten neuen Überwachungs-systems sind Carbon-Nanoröhrchen, welche als Sensorelemente eingesetzt werden. Der erste Systemprototyp, welcher im Rahmen dieser Arbeit entwickelt wurde, stellt ein Eingebettetes System dar, welches bis zu vier CNT-FETs als Sensorelemente ansteuern kann. Als komplett integriertes System erweitert es die IoT Domäne im Bereich der Umwelt- und Lifestyle-Anwendungen. Mit Hilfe der präsentierten Messplattform konnten NO_2 Konzentrationen von $200\,ppb$ bis hin zu $1\,ppb$ in ambienter Luft gemessen werden. Die Messungen bei NO_2 Konzentrationen von $1\,ppb$ erreichten ein 3σ Detektionslimit (Limit of Detection, LOD) von $23\,ppb$ mit einem linearen Anpassungskoeffizenten R^2 von 0.95. Das hier vorgestellte System zeichnet sich zudem durch die Konfigurierbarkeit verschiedener für den Energieverbrauch relevanter Parameter aus; darunter Reichweite, Bandbreite, Abtastrate, Intervalle zwischen Messungen, SD Karte, und die Verbindung zu anderen Bluetooth Low Energy Geräten. Dennoch bedarf es

Verbesserungen im Bereich der Leistungsaufnahme, zumal die Plattform eine durchschnittliche Leistungsaufnahme von $64.5\,mW$ aufweist.

Im zweiten Teil dieser Arbeit wird die Konzeption, das Design und die Realisierung eines integrierten Signalerfassungssystem aufgezeigt, welches eine physikalische Herunterskalierung des ersten Prototypen darstellt, und gleichzeitig eine höhere Energieeffizienz aufweist. Resultat der Forschungsarbeit ist eine Front-End-Mixed-Signal-Lösung mit einer einstellbaren CNT-FET-Spannung von $28\,mV$ Auflösung, welche eine geregelte Kaskode für das Auslesen des Stromes zwischen Quelle und Senke der Sensortransistoren kontrolliert. Die zweite Stufe besteht aus einem Transimpedanzverstärker (Transimpedance Amplifier, TIA) mit einer Verstärkung von $109\,dBOhm$ und einem Verstärkungsverlauf von $1\,dBOhm$, $0.75\,pA/\sqrt{Hz}$ Rauschen, einem Eingansbereich von $4\,\mu A$ mit integriertem Rauschfilter und differentiellem Ausgang. Dieser Ausgang ist mit einem $9\,bit$ SAR ADC von $91.7\,fJ/conv$ verbunden. Das Design wurde in $180\,nm$ CMOS Technologie realisiert und nimmt eine Silikonfläche von $0.18\,mm^2$ ein. Bei einer Spannungsversorung von $1.8\,V$ zeigt das System bei einer Abtastrate von $2.66\,kSps$ und einer Konzentration von $200\,ppb$ NO_2 eine durchschnittliche Leistungsaufnahme von $4.04\,\mu W$. In Verbindung mit einem CNT-FET Nanosensor konnten mit dem hier vorgestellten integrierten Schaltkreis NO_2 Gaskonzentration von $0\,ppb$ bis zu $200\,ppb$ in Luft von $50\,\%$ relativer Feuchtigkeit gemessen werden. Laborcharakterisierungen des Gesamtsystems zeigen, dass das gesamte Messsystem ein $3\,\sigma$ LOD von $18.5\,ppb$ mit einem R^2 von 0.8 erreicht. Während diese Arbeit die Entwicklung der oben dargestellten Protoypen und das Aufzeigen der Plausibilität einer Anwendung dieser Prototypen in batteriebetriebenen Geräten zur Überwachung der Luftqualität ins Zentrum stellt, wird in diesem Rahmen keine komplette Studie zur Charakterisierung des Gassensors durchgeführt. Die Implementation eines Sensornetzwerkknotens, dessen Leistungsaufnahme auf ca. $378\,\mu W$ geschätzt wird und auf dem entwickelten System basiert, stellt ein weiterer Punkt für die zukünftige Forschung dar.

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List of Abbreviations

AC   Alternative current

AD2   Analog discovery 2

ADC   Analog to digital converter

AFE   Analog front-end

AI   Artificial intelligence

API   Application programming interface

ASIC   Application specific integrated circuit

AWG   Arbitrarily waveform generator

BER   Bit error rate

BLE   Bluetooth low energy

BW   Bandwidth

CDC   Charge-to-digital converter

CLK   Clock

CMOS   Complementary metal oxide semiconductor

CNT   Carbon nanotube

CP   Conducting polymers

CPU	Central processing unit
$CQDs$	Colloidal quantum dots
CSV	Comma-separated file
CT	Continuous time
CTC	Clear timer on compare
DAC	Digital to analog converter
DAQ	Data acquisition
DC	Direct current
DNL	Differential nonlinearity
DR	Dynamic range
DT	Discrete time
DUT	Device under test
EDA	Electronic design automation
$ENOB$	Effective number of bits
ERF	Error function
FB	Feedback
FET	Field effect transistor
FFT	Fast Fourier Transform
FoM	Figure of merit
FS	Full scale

FSA Finite-state automata

FSM Finite-state machine

FVC Forced vital capacity

GBW Gain-bandwidth

GND Ground

$GPIOTE$ General purpose input output task event

GUI Graphical user interface

HD Harmonic distortion

IC Integrated circuit

IDE Integrated development environment

INL Integral nonlinearity

IoT Internet of things

ISR Interrupt service routines

IT Information technology

LCR Inductor-capacitor-resistor

LDO Low drop-out

LOD Limit of detection

LPF Low pass filter

LSB Least significant bit

$LSPR$ Localized surface plasmon resonant

$MEMS$ Microelectromechanical systems

MOS Metal oxide semiconductor

MOx Metal oxide senor

MSB Most significant bit

$MWCNT$ Multi-walled carbon nanotube

NDC Negative differential conductance

$NEMS$ Nanoelectromechanical systems

NRs Nanorods

PCB Printed circuit board

PGA Programmable gain amplifier

PM_{10} Particulate matter $10\mu m$

$PM_{2.5}$ Particulate matter $2.5\mu m$

POR Power on reset

PPI Programmable peripheral interconnect

PSD Power spectral density

PVT Process-voltage-temperature

QSS Quasi steady state

QTF Quartz tuning fork

$R.H.$ Relative humidity

RMS Root-mean-square

RSS	Root-sum-square
SAR	Successive approximation register
SAW	Surface acoustic wave
SB	Schottky-barrier
SD	Slope detection
SEM	Scanning electron microscopy
$SFDR$	Spurious free dynamic range
SH	Self Heating
SMD	Surface-mounted device
$SNDR$	Signal to noise and distortion ratio
SNR	Signal to noise ratio
SOA	Safety operational area
SoA	State of the art
SOI	Silicon on insulator
SP	Signal path
SPI	Serial peripheral interface
SSR	Sum squared regression
SST	Sum of squares
ST	Settling time
$SWCNT$	Single walled carbon nanotube

THD Total harmonic distortion

TIA Transimpedance amplifier

$UFPM$ Ultra-fine particulate matter

$ULDO$ Ultra low-dropout

UV Ultraviolet

$VLSI$ Very large scale integrated

VOC Volatile organic compound

WHO World health organization

WLP Wafer-level packaging

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1 Introduction

1.1 Impact of global air quality on human health

Over the last decades, ambient air pollution has become a topic of worldwide concern. The efforts of the World Health Organization (WHO) to reconcile the national ambient air quality around the globe by introducing guidelines and levels [14] are still unclear. Researchers have shown that long-term exposure to poor air quality represents a substantial human health threat [15].

The effects of long-term exposure to air pollution have been investigated in clinical studies, and different effects leading to decreased life expectancy have been revealed. For instance, [16] reports that an increase of $25\,\mu g/m^3$ of NO_2 level can be associated with a $4.1\,\%$ increase in pulse wave velocity and $37.6\,\%$ increase in augmentation index. Additional exposure to $5\,\mu g/m^3$ of SO_2 further increases the pulse wave velocity by $5.3\,\%$ for young adults.

Evidence between exposure to $PM_{2.5}$, PM_{10} and O_3 and reduced lung function in children has been investigated in [17]. A detrimental effect on the development of lung function under exposure to $17.92\,g/m^3$ of $PM_{2.5}$ and $24.9\,ppb$ of O_3 was associated with an annual lung volume growth deficit of $75\,mL$ for boys and $61\,mL$ for girls, affecting the flow in forced vital capacity (FVC). A research study investigated the change in lung cancer incidence or mortality associated with NO_2 and NO_x respectively from traffic sources [18]. The study shows an overall metaestimate of $4\,\%$ to $7\,\%$ risk increase in lung cancer incidence per $12\,\mu g/m^3 NO_2$ exposure.

According to various studies, there is a link between air pollution and diseases such as diabetes. For example, the study presented in [19] indicates that exposure to air pollutants can be associated with several effects, i.e., impaired glucose metabolism, insulin resistance, and type 2 diabetes mellitus. Another example of the dangers that emerge from air pollution is shown in [20], which reported a potential drop in weight at birth of $11.4\,g/1\,ppm$

of CO, and up to $20.1\,g/20\,ppb$ of NO_2 exposure. The same study shows pooled odds ratios for low birth weights ranging from $1.05\,g/10\,\mu g/m^3$ of $PM_{2.5}$ up to $1.1\,g/20\,\mu g/m^3$ of PM_{10} based on exposure during the entire pregnancy. Moreover, associations between cognitive development for children and traffic-related air pollution have been a topic of the investigation reported in [21]. The study suggests that all pollutants are suspected to be neurotoxicants, especially for children. Dementia is also discussed as an adverse effect of air pollution. In [22], it has been hypothesised that when NO_2 or NO_x is inhaled, it can induce an increased production and deposition of Amyloid peptides [23][24][25]. Furthermore, the frontal cortical and subcortical areas can be affected by inhaling $PM_{2.5}$ or by Ultra-Fine Particulate Matter (UFPM), $\leq 1\,\mu m$, passing through the olfactory bulb [23][25][26]. Effectively, it can be already appreciated that severe health threats are caused by air pollution.

The first federal research legislation involving air pollution issues was established in 1955 by the US Public Health Service as the Air Pollution Control Act [27]. As part of these proceedings, the federal government conducted extensive ambient monitoring studies and stationary source inspections for the first time. Concurrently to those studies, most countries around the globe implemented a public health service and authorized research into techniques for monitoring and controlling air pollution.

1.1.1 Recommended limit values for air pollutants

In one-third of the world's countries, air quality standards are scarce, and the laws are underdeveloped. Compared to WHO's guidelines, these countries seem to lack legally-mandated air quality laws; therefore, the quality of life remains under question. In other countries, such laws exist but are misaligned with WHO's guidelines. A comparison between different countries and WHO 's guideline values of the main six pollutants is presented in Table 1.1. The following paragraph presents these countries and their law system regarding air quality:

- **EU/UK:** In 1980, the air quality guideline limit was introduced by the 80/779/EEC directive. In the UK, the LAQM technical guidelines support local authorities in carrying out their duties under the Environment Act 1995, and the Environment order 2002 (Northern Ireland) [38]. For the EU, the ambient air quality limit values were updated in 2008 by directive 2008/50/EC for protecting human health [39].

- **US:** The Clean Air Act (CAA) recommends air quality responsibilities and relationships for federal, state, tribal, and local agencies. The

| | Country List | | | | | | | |
Pollutant and Exposure time	EU[28]/UK[29]	USA[30]	Japan[31]	Australia[32]	China[33]	India[34]	South Africa[35]	International WHO[36]
$PM_{2.5}$ $[\mu g/m^3]$								
1h	-	-	-	-	-	-	-	-
24h	-	65	35[37]	25	$50^a/150^b/250^c$	$60^{a,b}$	-	5
annual	-	15	15[37]	8	$40^a/150^b/250^c$	$40^{a,b}$	-	15
PM_{10} $[\mu g/m^3]$								
1h	-	-	200	-	-	-	-	-
24h	50	150	100	50	$50^a/150^b/250^c$	$100^{a,b}$	120	15
annual	40	50	-	-	$40^a/150^b/250^c$	$60^{a,b}$	50	45
O_3 $[\mu g/m^3]$								
1h	180/240	240	-	-	-	-	-	-
8h	120 for 25 days/year	160	-	-	-	120	-	100
24h	120 for 25 days/year	-	-	-	-	-	-	-
Peak season	-	-	-	-	-	-	-	60
SO_2 $[\mu g/m^3]$								
1h	350	-	262	200	$150^a/500^b/700^c$	-	350	-
3h	-	1310	-	-	-	-	-	-
24h	125	365	104	80	$50^a/150^b/250^c$	$80^{a,b}$	120	40
annual	20	79	-	20	$20^a/60^b/100^c$	$50^a/20^b$	50	-
NO_2 $[\mu g/m^3]$								
1h	20	-	2 -	120	$120^a/120^b/240^c$	-	200	-
24h	-	-	75-113	-	$80^a/80^b/120^c$	80^a	-	10
annual	40	100	-	30	$40^a/40^b/80^c$	$40^a/30^b$	40	25
CO $[\mu g/m^3]$								
1h	-	40000	-	-	$10000^{a,b,c}$	$4000^{a,b}$	30000	-
8h	10000	10000	22900	9000	-	$2000^{a,b}$	10000	10
24h	-	-	11500	-	$4000^{a,b,c}$	-	-	4

a: residential areas; b: commercial areas; c: industrial areas

Table 1.1: Comparative analysis of pollutants

local governments have developed a state implementation plan (SIP) containing rules and guidelines to reduce the pollution level to comply with the specified standard [40].

- **Japan:** The Offensive Odor Control Law (OOCL) was enacted in 1972 to regulate offensive odors emitted from business activities [41]. The corresponding administration specifies the regulation area, establishes the regulation standards, and hears opinions related to public announcements for cooperation.

- **Australia:** Australia defines national applicable air quality standard regulations for seven pollutant types managed by the National Environmental Protection Council (NEPC). The current standard was updated by the National Environment Protection for Ambient Air Quality (Air NEPM) [32].

- **China:** Since 2000, the daily Air Pollution Index (API) and air quality levels have been available in big cities. Those are regulated by the Law of the People's Republic of China on the Prevention and Control of Atmospheric Pollution. The standards are (GB3095-1996), National Ambient Air Quality (NAAQ), (GB13223-2003), and the Emission Standards of Air Pollutants for Thermal Power Plants [42].

- **India:** In 1981, the Prevention and Control of Pollution (PCP) Act was introduced. National Environment Engineering Research Institute spatially monitors air quality data (NEERI) [43].

- **South Africa:** The National Environmental Management (NEM) introduced Air Quality Act (AQA) in 2005 as the updated approach to air pollution control, including the devolution of responsibility to local government and effects-based management and air quality management (AQM) as the control strategy. This act implements air quality standards with the aim of decentralization [44].

1.1.2 WHO air quality guidelines

A complete inventory can be found in [45] concluding that only 21% of the countries meet the guideline values [46] for $PM_{2.5}$ and 46% for PM_{10}. For SO_2, only 7% of countries met the $24\,h$ standards and 16% met the $1\,h$ standards. NO_2 standards for the $24\,h$ average are met by 73% of the reported countries.

Although this indicates an increased coverage area of the world map regard-

ing air quality regulations, there are gaps related to inadequate monitoring. The spatial variation in specific air pollutants within cities is less extensive. In particular, one study [47] shows one order of magnitude concentration variations within a few hundred meters of area for NO_2 and UFP. To address this problem, land-use regression models to capture within-city variability for UFP have been explored in [48] [49], and recently scaled up to the global context for NO_2 [50]. The major problem here is the lack of spatiotemporal monitoring data capabilities. For simplicity, the WHO values [28] are converted to $[ppb]$ units[1] where possible such that the literature reported sensing performance can be related to the WHO values as in Table 1.2.

Table 1.2: Air quality guidelines for the six classical pollutants.

Pollutant	unit	exposure time	actual limit	targeted limit
$PM_{2.5}$	$[\mu g/m^3]$	annual	35	5
		24 hour	75	15
PM_{10}	$[\mu g/m^3]$	annual	70	15
		24 hour	150	45
O_3	$[ppb]$	peak season	51	31
		8 hour	82	51
NO_2	$[ppb]$	annual	21	5
		24 hour	64	13
		1 hour	-	107
SO_2	$[ppb]$	24 hour	48	15
CO	$[ppm]$	24 hour	6	4
		max. daily 8-h mean	-	9

The following subchapters introduce a paradigm shift towards sensors and circuitry that can fulfill the need for large-scale portable gas sensing applications.

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[1]at atmospheric pressure : $[\mu g/m^3] = ([ppb] \cdot 12.187 \cdot m\,[g/mol])/(273.15 + temp.°C)$, where m is the molecular weight of the gaseous pollutant.

1.2 SoA on smart gas sensing technology

Compared to complementary metal-oxide-semiconductor (CMOS) technology aggressive scaling or even microelectromechanical systems (MEMS) technology progress, the gas sensors are still bulky and power-hungry, yet becoming indispensable for the future. The following section is intended to overview the broad potential sensing materials like silicon, polymers or nanoparticles, and carbon nanomaterials. The aim is to pursue a brief review of miniaturized gas sensors as a research prerequisite.

1.2.1 Solid-state gas sensing elements

1.2.1.1 Metal Oxide (MOx) sensors

In the recent research literature, the capabilities of different metal oxides (MOx), such as ZnO, In_2O_3, ITO, and SnO_2, have been investigated for detecting hydrogen, VOCs, CO, and NO_2 in the environment [51]. When heated at increased temperatures, between $250\,°C$ and $550\,°C$, and by enhanced diffusion at the grain boundaries in the bulk of the material, the MOx materials can adsorb oxygen at the surface, which is forming a depletion layer in the thin film. An overall decrease or increase in the film resistance results, depending on whether the material is n-type or p-type. The sensor response is the resistance difference, i.e., the resistance of the sensor material in the air compared to the resistance in the presence of reducing or oxidizing gas. Lately, this technology has been exploited to introduce miniaturized solid-state gas sensors with integrated hotplates. However, design challenges such as sensing material choice, power consumption, and large integration scale must be addressed. Numerous gas sensor material requirements make it nearly impossible to find an optimal one. A research work, presented in [52], investigates different choices of metal oxides for a gas sensor design determined by factors such as: gas sensor type, the device for which the sensor is being designed, and construction for sensor fabrication.

The development of a single metal, front-side silicon bulk micromachining fabrication MOx technology is proposed in [53]. The paper reports a power consumption of $8.9\,mW$ at $400\,°C$, which is obtained by featuring a self-insulated layout between the heater and sensing layer. The sensor has been functionalized and characterized by different gases under different working conditions. The reported response time is $50\,seconds$ for detecting C_6H_6 (VOC) down to $5\,ppb$. In [54], the miniaturization and the wafer-level packaging (WLP) of micromachined MOx gas sensors are tackled. Several custom

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fabrication steps allow the direct WLP of the sensors on silicon by integrating the MOx films underneath the dielectric membrane in the cavity micromachined in the silicon wafer. This ensures protection in the application while still allowing the target gases to reach the sensing layer. The research reports measurement results for NO_2 concentrations down to $300\,ppb$ and CO concentrations down $10\,ppm$ at a 50% relative humidity (R.H.), with a sensing area reduced to $100 \times 100\,\mu m^2$ and power consumption below $20\,mW$ at $300\,^{\circ}C$.

The research presented in [55] proposes an n-type ZnO metal-oxide sensing structure. The sensor reacts with an oxidizing gas, i.e., NO_2, in which the sensor's conductance is decreased. The R.H. within this experiment was controlled at $50\,\%$. Four levels of NO_2 exposure ranging between 0.5 and $5\,ppm$ of NO_2 and between 50 and $500\,ppm$ of acetone were used to determine the sensor response. The gas time exposure was $30\,minutes$, and recovery appeared in $90\ minutes$ for synthetic air. Sensing and recovery work at a power consumption of $45\,mW$. A more recent work [56] has reported a conventional MOx material (p-type and n-type SnO_2) that exhibits high linearity in the 0-10 ppm range of VOCs. The readout method uses the impedance imaginary part at the high-frequency shoulder of the dielectric relaxation peak spectra. Due to impedance spectroscopy, the coefficient of determination, R^2, confirms outstanding linearity $>> 0.99$. The sensor and readout electronics power consumption is around $100\,mW$.

Different options for choosing suitable sensing material depending on the specific application are investigated in [57]. The work presents a systematic routine for determining the sensing material by knowing the exploration conditions and the sensing performance requirements, i.e., nature of the detecting gas, required sensitivity, and response rate. As a result, the paper shows that SnO_2-based sensors exhibit improved sensitivity and stability to reducing gasses (i.e., H_2, CO, NH_3, CH_4, and NO) during operation in reducing atmospheres. In contrast, sensors based on In_2O_3 show better response on oxidizing gases (i.e., NO_2, O_2 and CO_2), with less sensitivity to humidity, and shorter recovery time. Moreover, titanium-substituted chromium oxide, $Cr_{2-x}Ti_xO_{3+z}$ (CTO) exhibits high chemical stability and good conductivity response, ensuring a measurable resistance range. Compared to SnO_2-based devices, CTO-based sensors are more humidity insensitive. As a drawback, CTO-based sensors are not sensitive to certain gases such as methane.

1.2.1.2 Metal Oxide Semiconductor (MOS) sensors

MOS-type gas sensors use sensing transistors in which the gate is composed of a thin layer, e.g., platinum. As a sensor signal response, the changes in the threshold voltage can be explored [58]. In this case, the gas analyte atoms can diffuse in this layer and becomes polarized under the influence of an externally applied electric field. The dipole layer decreases the platinum work function, which reduces the MOS sensor's threshold voltage.

The work reported in [59] presents thermally isolated semiconductors for gas sensing applications. The sensor consists of four MOS-FET arrays. Three MOSFETs are used as gas sensors since their gates are covered in thin catalytic metals. The fourth is a reference with a standard gate covered in nitride. All devices are integrated on a micro-hotplate and fabricated using bulk micromachining of silicon. This low thermal mass device allows for field and thermal effects combinations and a pulsed temperature mode of operation. The same research group reports in [60] further experiment results depending on the sensor, the nature of the surrounding gaseous atmosphere, and the type of materials used as catalytic sensing film. After the gas exposure, a pulsed temperature scheme is proposed to reduce the recovery time for specific applications, such as hydrogen detection. The small area of the micromachined device allows pulsing the temperature of MOS-FET gas sensors with a time constant of less than $100\,ms$ at a low-power consumption of $90\,mW$. Moreover, cycling the temperature allows for the discrimination between different gas mixtures and gaseous mixtures of hydrogen and ammonia in the air. The research indicates that a specific combination of sample and temperature profiles could expand the information contained in the sensor response.

A different work reported in [61] proposes gas-sensitive metal/MOS FET based on silicon carbide (SiC). It uses an Ir/WO_3-gated sensing layer to study the benzene (C_6H_6) response down to the $10\,ppb$ concentration range in dry air. Several measurements have observed repeatability at a constant temperature from 180 to $300\,^\circ C$.

1.2.1.3 Nanoparticles-based sensor

Structural features of nanoscale materials often enhance the chemiresistive sensor's performance with increased design complexity. Despite their complexity, different research studies coupled the nanoparticles to multivariable transducers for achieving sensor response selectivity among gas analytes [62]. In 1998, Wohltjen and Snow [63] gave the first example of a chemires-

istor device comprising a film of octanethiol-encapsulated $2\,nm$ gold nano-particles deposited on an interdigitated micro-electrode. A research group has demonstrated a sensing mechanism involving similar dielectric constants for vapors in [64]. Their method uses peptide-capped gold nanoparticles on individual multivariable sensors. A detection model for toxic vapors, i.e., acetonitrile, dichloromethane, and methyl salicylate, have been proposed for data interpretation and discrimination. As a part of the inductor-capacitor-resistor (LCR) resonator, the peptide-capped gold nanoparticles indicate highly chemical vapor selectivity. The sensor signal response represents their resonance impedance spectra achieved with the help of a multivari-ate spectral analysis. As a result of this research, dichloromethane could be discriminated from methyl salicylate using a single sensor.

More recent research [65] investigates metal oxide quantum dot films as chemiresistive gas sensors. The scope of the research is low-temperature gas sensors based on thin oxide colloidal quantum dots (CQDs). For this pur-pose, the CQDs were designed with a reduced interdot spacing to promote carrier transport, resulting in a thin film with controllable carrier density. The work shows CQD sensor response upon H_2S gas exposure at different temperatures reporting optimum sensing at $70\,°C$. This value is substan-tially lower than the temperature required by MOx sensors, as presented in section 1.2.1.1. Such a result can reduce the sensor's power consumption up to one order of magnitude. CQD sensor repeatability within $25\,\%$ of the signal response variation with a response time of 37 $seconds$ and 127 $seconds$ of the recovery time, when exposed to $50\,ppb$ of SnO_2. The reported CQD selectivity is one order of magnitude higher when exposed to H_2S compared to SO_2, NO_2 and NH_3. In [66], NO_2 gas sensors based on zinc oxide nanorods (ZnO NRs) decorated with gold nanoparticles (Au NPs) working under visible-light illumination with different wavelengths at room temper-ature are presented. The contribution of localized surface plasmon resonant (LSPR) by Au NPs attached to the ZnO NRs is demonstrated. According to their results, the presence of LSPR extends the functionality of ZnO NRs to-wards longer wavelengths (green light) and increases the response at shorter wavelengths (blue light) by providing new inter-band gap energetic states. However, the light illumination introduces a power consumption overhead and physical dimensions to the final sensor.

Instead, the effects of nanowire self-heating on gas sensing and change of transport properties can be used for ultra-low power consumption gas nano-sensors. This result has been reported in [67] as the Joule heating effect of the quasi-1D nanostructures in the absence of an external heater. The research from [68] investigates the self-heating effect in sensor films fabric-ated by randomly oriented nanofibers. The reported method overcomes the need for complex fabrication of hot-plates or external haters and substan-

tially reduces the sensor complexity and fabrication costs. This paper explores the linear temperature-voltage dependence and implements a 2-point fast calibration method to enhance the sensor measurement reproducibility. Nevertheless, power consumption in the range of tens of mW due to the high operating temperature of $225\,^{\circ}C$ offers no clear advantage compared to the micro-heaters approach. The paper reports, however, practical sensor response toward NH_3, NO_2 gases, and humidity.

1.2.1.4 Carbon nanomaterials-based sensor

The electrical properties of carbon nanotubes are sensitive to adsorbed gases, as early reported by Kong et al. [69] and Collins et al. [70], who showed that NO_2 and NH_3 could cause a significant voltage shift in carbon nanotube field-effect transistors (CNT-FETs). In recent years, carbon nanomaterials [71] [72] [73] [74], i.e., graphene, nanofibres, carbon nanotubes (CNTs), and single-walled CNTs (SWCNTs) have raised special interest for detecting different gas analytes due to their unique electronic properties. Carbon nanomaterials have several valuable sensing properties, e.g., excellent electrical and thermal conductivity, good chemical stability, and high mechanical strength.

However, when used as a gas sensor, an unambiguous determination of the intrinsic VTH is typically interfered with by significant hysteresis in CNT-FET gate characteristics. This group showed NO_2 detection through Al_2O_3 contact passivated CNT-FETs [75]. Subsequently, pulsed gate sweep techniques have been used for small resolvable threshold voltage (VTH) shifts upon sub- ppm NO_2 exposure [76]. Afterwards, the dry-transferred suspended CNT-FET device architecture was introduced. It eliminates process residues and achieves complete suppression of hysteresis with an approximate 9-fold improvement in the noise performance [77].

Usually, gas desorption from CNTs requires high external heating temperature levels, substantially degrading the sensor structure. A research paper [78] proposes an internally driven desorption technique rather than an externally applied source of electrons, yet similar to electron-stimulated desorption. It is based on the Poole-Frenkel conduction threshold, which exhibits full liquid desorbing in approximately $1\,minute$ at a temperature of $24\,^{\circ}C$. However, this method involves currents in the range of mA, which drastically increases the overall sensor power consumption. In contrast, suspended CNT-FET nanosensors employ a self-heated desorption method, which is low-power for gas sensor architectures [79]. Sensing NO_2 at ambient temperature is possible, and recovery from gas exposure at an extremely low power of $2.9\,\mu W$

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by exploiting the self-heating effect has been demonstrated [80]. The recovery time of $10\,minutes$ is two orders of magnitude faster than the non-heated recovery at ambient temperature.

The surface of the CNT-FET is intrinsically hydrophobic, similar to many $2D$ materials, e.g., graphene, MoS_2, and the effect of humidity on the suspended CNT-FET nanosensor have been investigated in [81]. Thanks to its suspended structure, no cross-sensitivity to water up to $60\,\%\,R.H.$ is observed, and the device remains sensitive to NO_2 with no apparent response degradation. This overcomes a critical bottleneck for the practical application of carbon nanotube gas sensors.

Moreover, several process parameters have been improved, i.e., (ALD) of platinum and alumina passivated [82] which provides a current response increase of more than one order of magnitude and SNR improvement as high as 200. The contact resistance at the CNT-metal interface has been reduced significantly by removing the top layer of the electrode surface with Ar-ion etching directly before nanotube placement [83]. This technological improvement reduces the median ON-resistance of transistors by orders of magnitude from $1.56\,M\Omega$ to $143\,k\Omega$.

Furthermore, sensor readout bias schemes and data post-processing algorithms have been explored as transient and steady-state regimes for the CNT-FET nanosensors in the presence of low-frequency noise [4]. It is demonstrated that initial-slope sensing lowers response time relative to steady-state sensing, leading to better linearity and dynamic range due to the flattening out of the Langmuir isotherm.

1.2.2 Hybrid sensing technologies

1.2.2.1 Carbon nanotube and metal oxide

In [84] active layers for detecting NO_2 are investigated. The study proposes the deposition of oxygen-functionalized MWCNTs to three different types of metal oxides, i.e., SnO_2, WO_3 or TiO_2. This results in metal oxide/MW-CNT hybrid films that present increased sensitivity towards NO_2 in the 100-$500\,ppb$ range when operated at room temperature. Response time and total recovery, down to baseline resistance, are reported within $10\,minutes$. In [85] a nanocrystalline hexagonal tungsten oxide sensing structure is presented. For the device fabrication, five hundred parts of WO_3 and one part of gold-decorated multi-walled CNTs (MWCNTs) have been added to the matrix with an average hexagonal size of 30-50 nm. Experimental results

at room temperature showed 2.5% a resistance change within $15\,minutes$ exposure $400\,ppb\ NO_2$ gas concentration difference.

1.2.2.2 Conductive polymer composite

Polymers exhibit electrical conductivities in sensor applications [86] that depend on the concentration of dopant ions in the material. The paper [87] discusses the usability of conducting polymers (CP) as selective layers in chemical sensors. The emphasis is put on actual semiconductors with a defined and discrete energy band structure and neglects the "hopping" or "redox" polymers calling them "poor conductors". The paper presents the change of CP conductance upon exposure to an analyte due to their porosity, making them easily penetrable by gases. It demonstrates that by adjusting the initial value of the work function, it is possible to tune the selectivity of the CP affinity to different gases (i.e., methanol, chloroform, dichloromethane, isopropanol, and hexane). This feature is an essential advantage of CPs that enables a variety of sensing layers with the price of ambient factors dependency. CP-based sensor arrays are compatible with solid-state technologies, i.e., CMOS, enabling commercialization at high volume with potential in the sensor market.

The selectivity and sensitivity of a fully integrated CMOS capacitive chemical sensor based on polymeric-sensitive layers are tackled in [88]. The system has been exposed to 1000-5000 ppm ethanol and 600-3000 ppm toluene for sensor performance analysis. Sensitivity and selectivity are investigated based on polymer thickness influence. Experimentally measured sensitivities are well in line with the calculated values. An array-based VOC sensor using carbon black organic molecules, i.e., propylgallate, lauric acid, and dioctyl phthalate, is presented in [89]. Linear signal response on 500 ppm n-hexane and ethanol is reported. Sensor discrimination between analytes is observed by exploring the high density of randomly oriented functional groups. Six months of stable measurement data between training and test phases are mentioned.

1.2.3 Other sensing technologies

1.2.3.1 Resonant sensors

A tunable resonator sensor attaches a photocrosslinking polymer wire to a microfabricated quartz tuning fork (QTF) has been reported in [90]. As a

function of the ethanol vapor concentration, the sensor's resonance frequency represents its signal response. The photocrosslinking of the PVCN wire improved the sensitivity of the QTF sensor and provided an easy way to create a sensor with a variable resonance frequency. It has been reported that photocrosslinking improves the sensor's sensitivity and Q factor. However, the dynamic range of the resonator was relatively narrow regardless of the degree of photocrosslinking. The proposed method directly enhances the sensor's sensitivity and designs a tunable resonance frequency with a time response of $10\,minutes$. However, the sensor reset requires other gas, i.e., dry N_2. Moreover, complex electronics are required for signal post-processing and resonance detection. In [91], Si cantilevers are reported to detect VOCs. Detection limits of $24\,ppm$ for ethanol and $26\,ppm$ for toluene were reported with zeolite-type coatings. The respective detection limits are given by the theoretical mass resolution values of the transducers and the signal-to-noise ratio.

Other research reported in [92] investigates the sensing performance of fiber and quartz crystal microbalance sensors coated with SWCNTs. The research explores sensor adsorption dynamics that can be adjusted via the overlayer SWCNT thickness. As a result, trade-off parameters like sensitivity, response, and recovery time can be tuned. Room temperature measurement results are reported for xylene and toluene VOCs vapors concentration below a few hundred ppb, response time below $20\,minutes$, and recovery time below $15\,minutes$.

1.2.3.2 Acoustic wave sensors

A surface acoustic wave (SAW) presented in [93] has been polymer-coated with a PB/PS(polystyrene, polybutadiene) film, and its viscoelastic properties of it have been investigated. The sensor has been exposed to N_2 analyte concentrations from 0% to 80%, and attenuation vs. velocity variations were measured with the polymer-coated SAW device. Based on a superposition of mass loading and plasticization by absorbed gas, responses of stiffness constant can be extracted indirectly with the help of a Maxwell model.

Another work reported in [94] investigates graphene oxide as a sensing layer for ZnO/glass SAW (surface acoustic wave) humidity sensor. Here, humidity vapors act as a sensor mass load rather than material impedance change. Sensor response time is below one second for 0.5 %-85 % R.H., recovery time in tens of seconds with a robust sensor drift, and stability evaluated over $60\,days$.

In [95], an alternative approach to MEMS/nanoelectromechanical systems (NEMS) sensors for material analysis and direct gas sensing is proposed. The piezotransistor transduced external excitation with a maximum noise-limited resolution of $12.43\,fm/\sqrt{Hz}$ and a superior responsivity of $170\,nV/fm$, which is similar to optical transduction limits. The piezotransistor consumes ultra-low-power of $1.36\,nW$ and demonstrates an ultra-high gauge factor of 8.700. These distinct properties, which allowed for detecting nanogram quantities of gas analytes via photoacoustic spectroscopy, can be easily applied to various novel sensing paradigms.

1.2.3.3 Catalytic sensors

For the first time, the influence of semiconductor electronic properties related to the catalytic reaction was investigated in 1957 [96]. Recently, a plasmonic sensing method based on arrays of nanofabricated gold disks has been reported [97]. The sensor readout method is based on peak shifts in the catalytic reaction. Three catalytic reactions, CO and H_2 oxidation on Pt, and NO_x conversion to N_2 on Pt/BaO were reported. A plasmon peak shift during $30\,minutes$ on NO_2 exposure from 0 to $1000\,ppm$ is demonstrated in the research. More recently, [98] reports a planar catalytic sensor fabricated on a free wedge-shaped alumina membrane with a microheater. Upon methane exposure in dry and humid air, the sensor signal is evaluated as a transient response process resulting from an excitation voltage. The sensor is operated in pulses twice per minute and consumes an average power of $1.2\,mW$.

1.2.4 SoA preliminary conclusions

Solid-state gas sensors have been in development for decades, with sensing elements such as catalytic metals, metal oxides, and polymers being the earliest examples. The most widely used transduction principles, i.e., resistance, capacitance, complex impedance, and work function, have been implemented in MOx, MOS, catalytic, resonant, and CNT-FET sensors. Gas sensors are engaging for a variety of IoT application scenarios. However, despite improvements in gas sensors based on existing sensing materials, such as MOS, [58] [61], and MOx [55] sensors, their power consumption remains high, i.e., tens to hundreds of milliwatts. Modern gas sensing scenarios, e.g., environmental monitoring, and demand sensing capabilities at a fraction of this power budget. However, just a few sensing materials initially demonstrated in the research have found their acceptance in practical applications in the last decades. Only recently, carbon nanotubes [79], nanowires [67], or

graphene [94] have become more attractive and are about to find wide practical acceptance. One reason could be the sensor's signal acquisition using lab equipment. In this case, miniaturized, i.e., integrated front-end circuitry, can overcome this limitation and enable high-volume, low-cost applications of such sensing materials.

With the presented SoA information as a prerequisite, this thesis will focus on the CNT-FET, IC system co-integration in the context of NO_2 pollution monitoring systems.

1.3 MOS-FET and CNT-FET devices

The Metal Oxide Semiconductor (MOS) Field Effect Transistor (FET) [99] represents by far one of the most influential innovations of the 20th century [100]. The MOS-FET became one of the widest manufactured devices in history. Since its invention as a stand-alone transistor by Mohamed M.Atalla and Dawon Kahng at Bell Labs in 1959, the MOS-FET has touched our daily lives. Currently, millions of Complementary (CMOS)-FETs can easily be integrated into a single chip, creating Very Large Scale Integrated (VLSI) circuits [101] executing complex functionalities. In this thesis, CMOS transistors are used in both modes as a switch or an amplifier, forming the main building blocks of the proposed application-specific integrated circuit (ASIC).

Further, the Carbon Nanotube (CNT) device is considered to be one of the most symbolic icons of nanotechnology [102]. When relating its structure to the graphene structure (two-dimensional hexagonal network of carbon atoms), the CNT is a rolled-up graphene sheet into a tube. Among the various CNT structures, the CNT Field Effect Transistor (CNT-FET) architecture received the most attention due to its advantages of having high performance, miniaturization, and mass production capability. Since its discovery in 1993 by Sumio Iijima reported in Nature journal [103], the CNTs have been fabricated only in academic or research laboratories. Only recently, in 2019, the first microprocessor made out of complementary CNTs was introduced [104]. Since then, the fabrication of CNT-FETs in commercial silicon manufacturing facilities and high-volume semiconductor foundry [105] is still under development. In this thesis, the CNT-FET is used as a sensing material for gas analyte detection rather than as a VLSI building element where classical MOS-FETs are used instead. The aim here is to combine these two technologies and create a sensing system in the context of IoT [106].

1.3.1 MOS-FET as circuit building device

Later in this thesis, a review and analysis of different design techniques for low-power integrated circuits (IC) design are performed. The aim is to choose the most suitable design methods for low-power analog IC design in a standard CMOS process. The proposed ASIC uses high transconductance, i.e., MOS transistors biased in weak or moderate inversion operation regimes, to reduce the input-referred voltage noise. At the same time, strong inversion is preferred for low-noise features when designing current mirrors. Tripple well technology features are explored for bulk-driven MOS transistors and dynamic threshold MOS transistors. The main advantage of such circuit design techniques is that the transistors' performance parameters can be changed without modifying the standard CMOS processes. Basic circuit building blocks like differential amplifiers, comparators, transmpedance amplifiers, or current mirrors are designed using these approaches. More about key features of integrated systems for modern portable applications are presented in [107].

1.3.2 Carbon Nanotube FET

To exploit the CNT electronic properties, the following sections briefly introduce the CNT-FET device in terms of its architecture, band structure, and transport mechanisms. The following common terminology introduced below:

- **Fermi level**, denoted as E_F, represents the energy level of an electron in a solid at a given temperature for which there is a 50 % probability of being occupied by the electron.

- **Electron affinity**, denoted as χ, is the negative of the energy required to introduce an additional initially free electron into a crystal.

- **Valence band**, denoted as E_V, represents the range of permissible energy values that are the highest energies an electron can have and still be associated with a particular atom of a solid material.

- **Conduction band**, denoted as E_C, represents the range of permissible energy values which an electron in a solid material can have that allows the electron to dissociate from a particular atom and become a free charge carrier in the material.

- **Bandgap**, $E_g = E_C - E_V$, represents the difference in energy between

the valence band and the conduction band of the solid material. This energy difference represents a range of energy states forbidden to electrons in the material.

- **Work Function**, denoted as Φ_m in metals, corresponds to the minimum amount of energy needed to remove an electron from the metal.

1.3.2.1 Classification of CNT

1. Single-walled or Multi-walled CNT: a single graphene sheet is rolled into a tube form, forming a single tube. MWNT has several walls and can have several concentric tubes or a single graphene sheet that rolls itself into a multiwall. Figure 1.1 shows the classification of CNT based on its wall structure.
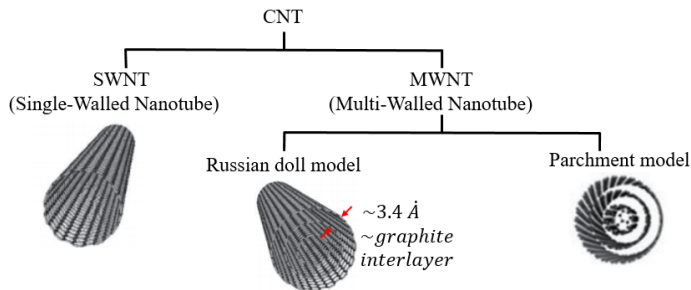
Figure 1.1: CNT classification based on its wall structure. Classification reproduced with figures adapted form [1].

2. Chirality: depending on which direction the graphene sheet is rolled into a nanotube, different types of chirality can be achieved. The arrangements can be categorized as in Figure 1.2, in terms of chiral vector $\vec{C_h} = m\vec{a_1} + n\vec{a_2}$, where n, m are translation chiral indexes; $\vec{a_1}$, $\vec{a_2}$ are the base vectors, and Θ is the chiral angle.

   For integer values of m,n, the following structures can be distingushed:

   - $n = m$: armchair CNTs

   - $m = 0$: zig-zag CNTs

   - $m \neq 0 \neq n$: zig-zag chiral CNTs

After the CNT is rolled-up, the magnitude of the chiral vector gives the CNT radius $r_{CNT} = \left| \vec{C}(n,m) \right| / 2\pi$. By a given radius, the corresponding circumerence d_{CNT} gives the bandgap of the CNT as:

$$E_g = \frac{2a_{cc}\gamma_0}{d_{CNT}},\tag{1.1}$$

where $a_{cc} = 1.42$ is the carbon-carbon bond length [108], and γ_0 is the hopping integral experimentally found to be $3.1\,eV$ [109].

The CNT electrical conductivity is given by its chiral indices as follows:

- $mod\,[n - m, 3] = 0$: metallic CNT

- $mod\,[n - m, 3] \neq 0$: semiconducting CNT
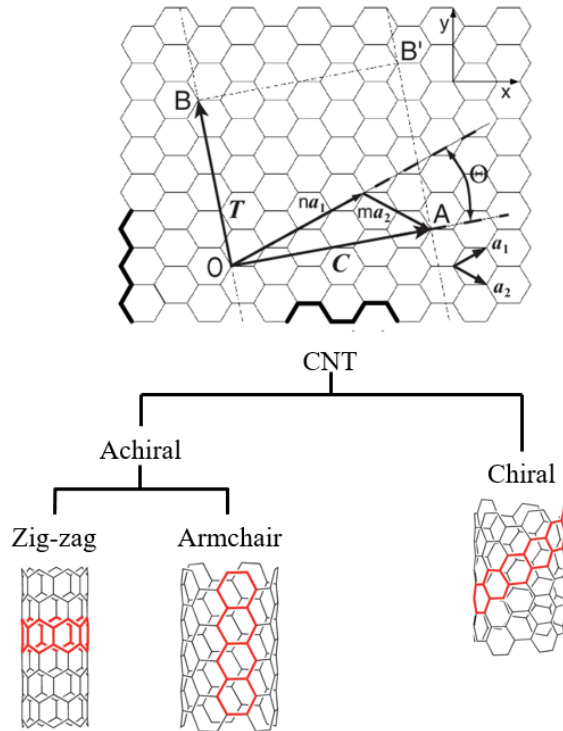
Figure 1.2: CNT classification based on chirality, the information reproduced form [2].

This thesis focuses on semiconducting p-type single-walled CNT and explores their electronic properties in the context of a chemical sensor. The following paragraph is briefly introducing the architecture of the p-type CNT-FET nanosensor and its band structure. For a comprehensive analysis, one can refer to the former Ph.D. thesis of this group [6].

1.3.3 CNT-FET device architecture

The CNT-FET device architecture needs to be introduced to understand its electronic properties. Starting from CNT synthesis and ending with their integration in gas sensors, the number of fabrication possibilities is vast [110]. Among other architectures, a suspended CNT structure is used in this thesis, advantageous for chemical applications due to the increased adsorption area, reduced hysteresis, and increased SNR [111]. A simplified schematic of the CNT architecture can be visualized in Figure 1.3. The detailed substrate fabrication process, including the CNT growth and transfer procedure, can be found in [6], improved in [83] and briefly summarised in chapter 4 of this thesis.
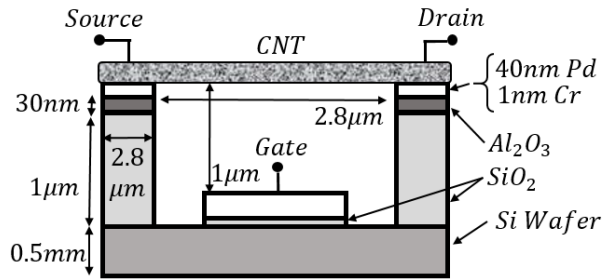
Figure 1.3: Suspended CNT-FET illustration on substrate including the three terminals: Source (S), Drain(D) Gate(G). Open Access figure reproduced from [3] published under the terms of Creative Commons CC BY license.

The dry-transfer technique fabricating these ultra-clean CNT-FET nanosensors facilitates a residue-free approach, avoiding charge traps at the oxide/CNT interface. This has helped suppress electrical hysteresis commonly observed during the electrical field-effect characterization of on-substrate/non-suspended CNT-FET nanosensors [111]. Furthermore, the suspended CNT-FET structure's particular architecture explores the sensor's lack of cross-sensitivity to humidity. The CNT-FET surface is intrinsically hydrophobic, similar to many 2D materials, e.g., graphene. Under such hydrophobic conditions, water molecules' adsorption is typically facilitated via defects and surface contaminants. Such contaminants can be introduced during standard photolithographic fabrication processes when the nanomaterial is in contact with photosensitive polymers and solvents. In such scenarios, the contaminants and residues facilitate secondary charge transfer, which may interfere with the sensor response to the analyte. The role of such

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adsorbed water layer on graphene FETs (transferred via polymer-assisted method) and non-suspended CNTs has been well studied [112][24].

1.3.3.1 Band structure

Band structure theory can be used to understand charge transport in CNT-FET, whose structure has been illustrated in Figure 1.3. In Figure 1.4 several band diagrams of the CNT-FET are shown for the following scenarios:

a) The CNT-FET is formed when the semiconducting CNT is brought in contact with the metal electrodes by forming Schottky-barriers (SBs) for carriers. For the used architecture, presented in Figure 1.3, palladium (Pd) electrodes are used. As a consequence, $(\chi + E_g/2) < \Phi_m < (\chi + E_g)$ and in this case $\Phi_{SB,h} < \Phi_{SB,e}$, which gives a $p-type$ characteristic.

b) Considering the S and D as being grounded, V_{GS}, can bend the E_C and E_V bands in the direction of this externally applied potential. For large and negative, V_{GS}, the SBs at the contacts become thinner, increasing the probability of carrier tunneling from the contacts into the CNT-FET. For the p-type semiconductor, the transmission probability into the channel is given by the width of the Schottky-barrier, W_{SB}.

c) A drain current, I_D, starts to flow when an additional external bias V_{DS}, is applied to the CNT-FET.

The metal type for the electrode influences the behavior of the CNT/electrode junction. Sensing capabilities for electrode/CNT devices with Pd instead of Au have been reported [113]. The good Pd/CNT contact has been associated with stronger interactions between the Pd surface and CNTs which aligns well with theoretical studies [114][115] [116]. The I_D current can generally change if one of its parameters is altered. For the CNT-FETs used in this research, the modulation of Schottky-barrier (in height or width) by the applied bias or when a CNT-FET is made with different metal electrodes has been studied in [6]. Moreover, the current depends on the CNT device conductivity, which can alter the doping level at the surface of the electrode/CNT contact. These sensing mechanisms are summarised in the next paragraph.
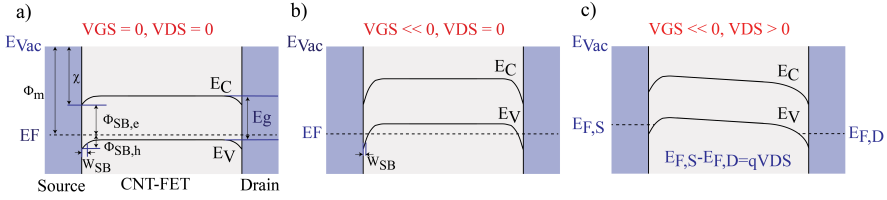
Figure 1.4: Energy band diagrams along the channel of a CNT-FET under different V_{GS} and V_{DS} bias conditions.

1.3.3.2 CNT-FET as gas sensing device

The sensing capabilities of CNT-FET devices in the presence of gas molecules are introduced and briefly discussed in the following paragraphs. Although the complete sensing mechanism is still debated in the literature, investigation of I_D-V_{GS} (transfer) characteristic changes upon gas exposure gives some insights into the potential sensing mechanism. As a starting point, a typical p-type CNT-FET characteristic is illustrated in Figure 1.5.a in gray, and the following potential sensing mechanisms can be denoted:

(i) **Schottky barrier modulation:** the presence of gas molecules at the junction of the metal electrode and CNT can modulate the Schottky barriers [117] [118] [119]. Contacts with and without passivation have been investigated to assess this sensing mechanism independently. In [120] a CNT-FET based sensor for NO_2 and NH_3 sensor have been passivated with poly methyl methacrylate (PMMA). In contrast to [118], changes in the transfer characteristics for channel and electrode/CNT devices have been reported. This result suggests that the effects on electrode/CNT junction and the length of the CNT contribute to the sensing mechanism. The same passivation with PMMA has been used in [121] for a CNT device exposed to NO_2 analyte. It has been concluded that the sensing response is mainly due to the electrode/CNT interface. On the CNT-FET I_D-V_{GS} characteristic this corresponds to an increase in the I_D current combined with a slight shift in threshold voltage, as sketched in Figure 1.5.a.

(ii) **Modulation of channel conductivity:** in [122] is suggested that the direct charge transfer between the gas molecules and CNT-FET channel [69] [123] is possible. Under ambient conditions, the CNT-FET is considered p-doped due to O_2 physisorption. Consequently, the CNT-FET conductance can be modulated by changing the number of majority charge carriers. Hence, further exposure to the p-dopant

analyte would lead to a decrease in the resistance, the reverse effect for n-type dopants [70] [124]. In [118] it has been found that complete coverage of a pristine CNT with SiO_2 drastically attenuated the response to NH_3 exposure. Subsequently, contact passivation only of electrode/CNT areas resulted in a sensor with comparable responsiveness and faster reversibility. Moreover, in [123] [122], the finding is that the NO_2 sensing mechanism occurs over the length of the CNT and not at the electrode/CNT contact regions. However, the same scientific reports associate NH_3 with less carrier density within the tube or, in the case of CO, almost no effect. Furthermore, in this research group, Mattmann *et al.* [75] state that charges transferred from the CNT to the NO_2 molecules are responsible for the hole doping since the metal electrodes were passivated and hence have no contribution to the sensing mechanism. As an effect, the electrostatic gating induces shifts in the transfer characteristics. On the CNT-FET I_D-V_{GS} characteristic, this corresponds to a shift in threshold voltage sketched in Figure 1.5.b when the transport is considered quasi-ballistic (short channel). For this research, the CNT-FET I_D-V_{GS} characteristic exhibits a combination of Figure 1.5.a and Figure 1.5.b characteristics corresponding to an increased I_D current and a threshold voltage shift as sketched in Figure 1.5.c. This is due to the relatively long channel ($L_{CNT} > 1 \, \mu m$ as illustrated in Figure 1.3), employing a diffusive regime with charge scattering and unpassivated contacts [6]. Experiments with the fabricated CNT-FET [4] are presented in Figure 1.5.d, when exposed to different NO_2 gas concentrations. This result supports a sensing mechanism that combines Schottky barrier modulation and channel doping. For simplicity, the role of contamination and defects [125] [126] [127], which might serve as energetically favorable adsorption sites for gas molecules, has been neglected here but cannot be underestimated [6].
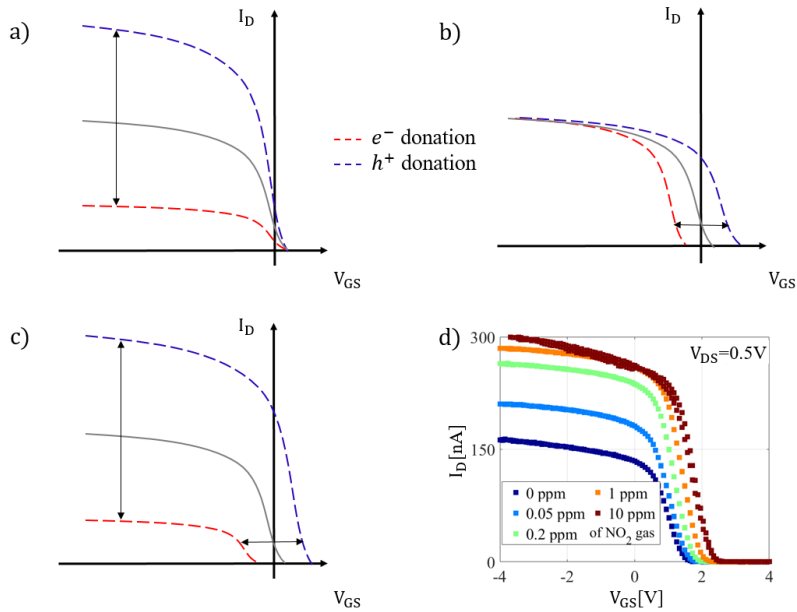
Figure 1.5: Transfer characteristics of the CNT-FET device exploring its sensing effect by highlighting: a) variations of I_D current at high negative V_{GS} values; b) threshold voltage shift around zero V_{GS} values; c) I_D variations and threshold voltage shift combined; d) typical transfer characteristic of the CNT-FET when is exposed to different NO_2 concentrations. Note: measurement result adapted from [4], conducted by Peter F. Satterthwaite.

1.4 Gas sensors: development and market trends

Today, large scale air quality monitoring systems are built from common measurement instruments based on gas chromatography [128] and mass spectrometry[129], ion mobility spectrometry [130] or direct spectrometry [131]. These instruments are relatively big, weighty, and expensive: $35\,cm$ (l) x $26\,cm$(w) x $15\,cm$ (h) and $5\,kg$ without a battery pack is the newest reported in literature [128]. In addition, this kind of equipment is most likely immobile; it requires specialized personnel for the installation and rigorous maintenance service with increased costs. They are indispensable instruments for high-precision measurements and high-selectivity detection. However, the relatively high number of yearly deaths as a result of exposure to ambient air pollution and exposure to smoke [132] created an increased de-

mand for novel, low-cost sensors capable of monitoring the levels of air pollution. The following subchapters complete the introduction with a paradigm shift towards sensors and circuitry that can fulfill the need for large-scale portable gas sensing applications.

1.4.1 Smart gas-sensing systems for environmental monitoring

The current trend of the 21st century is to redirect most existing technological solutions toward digitalization for a data-driven society. As a reaction, the IT-dominant world has increased its focus on developing Internet-of-Things (IoT) devices due to their versatility in applications, size, and long-lasting battery lifetime. IoT is a technology that aims to interconnect various devices, i.e., smartphones, smartwatches, wearables, sensor platforms, healthcare, and building automatization by combining power-efficient and small-sized electronics with sensors and actuators. Currently, the most popular embedded sensors are being used for monitoring temperature [133][134], relative humidity[135][136], light [137], proximity [138][139], and air quality [140][141].

This section continues with the CNT-based sensors research prototypes, start-up solutions including readout electronics with sensor signal post-processing, and existing commercial solutions. It concludes with examples of highly integrated circuits capable of amplification, filtering, or digital signal processing used for interfacing nanomaterials when used as sensing elements.

1.4.2 NO_2 CNT sensors - research prototypes

CNT-based materials have the potential of low-powered, cost-effective environmental sensors. This section focuses on monitoring the WHO recommended levels of NO_2 with the help of CNT- based sensors and how to integrate them into CNT sensing systems applications. In particular, for NO_2, WHO guideline currently recommends a limit of 21 ppb (annual mean) as already presented in subchapter 1.1.1. A study [142] reported full recovery of printed flexible-film CNTs on acid-free paper. The reported limit of detection (LOD) for their sensors was 125 ppb of NO_2 in ambient air. The claimed full recovery feature relies on the weak charge transfer between the gas analyte and the CNTs rather than covalent bonds. Covalently grafted poly(m-aminobenzenesulfonic acid) (PABS) deposited onto SWCNTs was

reported in [143] achieving a minimum detectable signal of $20\,ppb$ for NO_2. In [144] deposited thin films of MWCNTs onto platinum Pt electrodes were presented to be sensitive for $10\,ppb$ of NO_2 in dry air conditions. However, the sensors were operated at $165\,°C$ temperature for optimal sensitivity and recovery time. In [145] SWCNTs coated with polyethyleneimine (PEI) gas sensors are shown, achieving selectivity for NO_2 or NH_3. The PEI coat changed the SWCNTs from p-type to n-type semiconductor and resulted in a sensitivity of as low as $100\,ppt$ for NO_2 while being insensitive to NH_3. A more recent research [146] reports a CNT-FET sensor based on a few non-functionalized SWCNTs individually connected devices, which achieves a LOD of $86\,ppb$ NO_2 when operated at room temperatures. The device response is attributed to an exponential dependence of the SB height in the presence of NO_2 molecules.

1.4.3 Commercial solutions

The high demand for environmental sensing, indoor air quality monitoring devices, and other consumer devices, i.e., smart farming, has determined top companies to expand their product portfolio, aiming at the sensor market sector. The prominent players substantially increased their production in response to the increased demand in the gas sensor market. Table 1.3 summarizes relevant low-cost IoT sensors suitable for large-scale integration, i.e., surface-mounted device (SMD) solutions with a bulk acquisition price below $100\,USD$. An extended comparison of the summarised sensing technologies in terms of their feature size, power consumption, and acquisition price is presented in Figure 1.6.

1.4.4 Start-up companies based on CNT sensors

Up to date, a start-up called SmartNanotubes Technologies [147] reached the vision of digital smell recognition and self-proclaimed "first multi-channel gas detector chip for the mass market." The start-up developed a gas sensor platform based on the principle of an electronic nose. Their sensor array is chemiresistor-type nanomaterial dimensions of $22\,\times\,8\,mm$ consuming a power of $1\,\mu W$ for a limit of detection (LOD) $\leq 80\,ppb$ towards NH_3, PH_3, H_2S and VOCs with an operation temperature temperature range from $0°C$ to $+40°C$. Their demonstrator, "Smell-inspector," reads four sensor arrays of 16 channels each and sends them out every two seconds. The board demonstrator dimensions are $157\times\,40\,mm$ $67\,\times\,50\,mm$, and it consumes $280\,mW$. Their price for a prototype is about $300\,USD$. This start-up prototype solution is here compared with the presented commercial products

Table 1.3: SMD commercial air quality sensors for the air quality monitoring

Brand	Detection analyte	Technology	Image	Part nr.
Amphenol	CO_2	Non Dispersive IR		T6713
AMS	Total VOCs, eCO_2	MOx		CCS811
Aosong	Temp. and R.H.	Cap. MEMS		AHT10
Bosch	Pressure, temp., R.H., VOCs eCO_2	MOx		BME680
Figaro	Methane, Iso-butane, CO, H_2, Ethanol	Silicon+heater MOS + MEMS		$TGS8100$
Infineon	Real CO_2 level	Photoacoustic		$XENSIV^{TM}$
KEMET	CO_2/ CH_4/ NO	IR (sensor only)		$USEQGSxx$
Renesas	Total VOCs; CO_2 equiv.	Chem. MOx		$ZMOD4410$
Sensirion	VOCs, NOx	MOx		$SGP41$
ScioSense	VOCs, H_2, NO_2	MOx		$ENS160$
SGX S.tech	NO_2, H_2	MOS		$MiCS2714$
TI	Temp., R.H.	Cap. poly. dielectric		$HDC2010$

in Figure 1.6. By reducing the power budget, feature size, and costs, such smart sensor platforms can be integrated into wearable devices for monitoring air quality. Nevertheless, reducing sensor size often changes the sensing mechanism, requiring significant signal post-processing followed by practical validation.

1.4.5 CMOS low-power interfaces for CNT sensors

As Figure 1.6 suggests, an integrated version for the nanotubes-based sensor signal post-processing electronics is desirable due to its total physical dimension and high power consumption overhead. The same can be observed

for the signal acquisition electronics used in [56] research sensor, which has been implemented with commercial off-the-shelf components, i.e., AD5933 and ADuCM355 ICs requiring a power consumption of $50\,mW$ each.

Due to low-cost production, miniaturization, and integration capabilities embody a high commercialization potential, CMOS co-integration is widely used in sensing applications. The system can accommodate the sensing element with readout electronics and sensor signal processing, e.g., amplification, filtering, or digital signal processing. Few such examples of highly integrated circuits are given as being capable of interfacing nanomaterials when used as sensing elements.

Recently, CMOS integrated chemical sensors presented real candidates for IoT sensing applications. For example, [148] presents a design of a CMOS biosensor platform that can read 96 sensing elements simultaneously. The system shows resistance measurements from $50\,k\Omega$ up to $1\,G\Omega$ with an overall accuracy of $4\,\%$. The system noise performance is $0.84\,nA_{rms}$ at $1\,MHz$ bandwidth detecting solutions with $0.025\,pH$ units and $4\,\mu M$ NaCl resolution. A NO_2 CNT-based hybrid integrated measurement system has been presented in [149]. The research shows an energy-efficient integrated circuit (IC) sensor interfaced comprising of front-end circuits, i.e., a digital to analog converter (DAC) and a 10-bit analog to digital converter (ADC), that includes a calibration technique using off-chip reference resistors and achieves $1.34\,\%$ measurement accuracy. The sensor interface chip is designed in a $180\,nm$ CMOS technology node and consumes $32\,\mu W$ of power at a $1.83\,kS/s$ conversion rate. Furthermore, [150] reports a CNT-based biosensor system-on-a-chip (SoC) that has been used as a neurotransmitter detector. The SoC accommodates 64 CNT-based sensors that are sensitive to glutamate; hence, their conductance can be modulated by neurotransmitters.

1.5 Chapter summary

This chapter discusses the imminent threat of air pollutants, the lack of monitoring, and a vast combination of requirements for the new sensor technology. The recent innovations and sensor technology developments, including advances in micro-and nano-fabrication, have been summarised as state-of-the-art technology. By reducing the feature size and costs, nanotube-based sensors can be integrated into smart devices like home appliances, sensor nodes, or smartwatches to monitor air pollution. However, practical aspects like sensor sensitivity, signal acquisition, sensor stability, and limit of detection require significant signal conditioning circuitry, post-processing, and experimental validation. Subsequently, the design opportunities for novel

circuitry, research prototypes, and start-up companies have been enumerated.

As a conceptual overview, a sensing system can be imagined that identifies, monitors, and harmonizes worldwide air quality. The following list defines preliminary application design specifications:

- **Form factor**: for broad spatial coverage, the system must be small in size and lightweight to become portable.

- **Selectivity**: the sensing element needs to be sensitive towards the analyte of interest while being insensitive to other, perhaps similar, analytes. This includes insensitivity toward ambient temperature and humidity changes.

- **Resolution**: the system must be capable of outputting a reliable digital output signal that can be correlated to the analyte of the interest input value and has a limit of detection way below the maximum recommended value.

- **Range:** both the sensor saturation and the electrical circuitry have to cover the entire plausible gas analysis concentration range that might arise from the minimum time exposure interval.

- **Response time:** the volatility of the gas concentration in the air requires a system response time of seconds or minutes. This constrains the bandwidth of the electronics and the sensing and resets time intervals.

- **Operation temperature:** the temperature range for industrial applications, which varies between -20 $^\circ C$ and +80 $^\circ C$ fulfills both indoor and outdoor application requirements. Circuit temperature compensation and sensor calibration for different temperatures are necessary.

- **Battery operated:** battery life is the primary concern in all portable systems. The system's power consumption, effectively the sum of the sensor and signal acquisition circuit's power consumption, determines the battery lifetime. In addition, the required courses need low absolute power consumption while maintaining high power efficiency and performing sensor signal post-processing, meaning that the readout algorithms must be optimized in terms of computational complexity.

- **Production costs and scalability:** these two parameters are the critical characteristics of large-scale sensor nodes that can be commer-

cialized at low market costs. CMOS semiconductor technology offers the right ingredients for analog and digital integrated circuits. Regarding sensing capabilities, CMOS-compatible nanomaterials can be used as a transducer and co-integrated in an SoC hybrid solution.

- **Communication data security:** for large sensor nodes from remote areas to urban agglomeration, a wireless interconnection or pairing with other mobile devices is necessary. This enables centralized spatial coverage and facilitates comprehensive data analysis.

The system mentioned above sums up the current research's primary motivation, aiming to build and scale-up air quality monitoring systems. As a result, these advances may boost the current gas sensor IoT market with new technologies, which are forecasted to reach revenues of $3.8\,billion\,USD$ in 2030 [151].

1.6 Thesis organization

By developing an easy and cost-effective way to monitor pollutants, the preliminary step in implementing clean air policies, which are vital for achieving sustainable air quality levels, is being made. The following chapters of the thesis present two prototypes of interfacing gas sensors with their associated front-end readout circuits: off-the-shelf discrete components and monolithic design approaches.

- **Off-the-shelf discrete components:** this method employs separately dedicated ICs for the sensor readout circuits. The versatility of many components available on the market is an advantage of this approach. The other main advantage is that there is no restriction on debugging the circuits directly on the PCB, resulting in a fast redesign cycle. Hence, the circuit and the sensor performance can be adjusted toward system optimization. However, the physical dimensions of the components and long PCB interconnects limit the system's performance by increasing its form size and weight. In addition, the discrete components approach requires more power consumption due to component overhead. In contrast, a single-chip implementation offers a dedicated solution and can become even cheaper considering extensive volumes.

- **Monolithic approach:** the dedicated sensor readout circuits are all on the same silicon chip, forming an application-specific integrated circuit (ASIC). This solution has several advantages, including low power

consumption and a tiny form factor. Moreover, the sensor element can be co-integrated into the silicon chip. However, a fault in one block will fail the entire chip, even if the rest of the blocks are working correctly. The ASIC design approach can be cost-effectively only in high unit volumes, making it commercially attractive.

This thesis evaluates the two proposed systems individually and as stand-alone systems connected to the CNT nanosensors. The thesis concludes with NO_2 gas exposure experiments performed in lab conditions and compares the system performance.
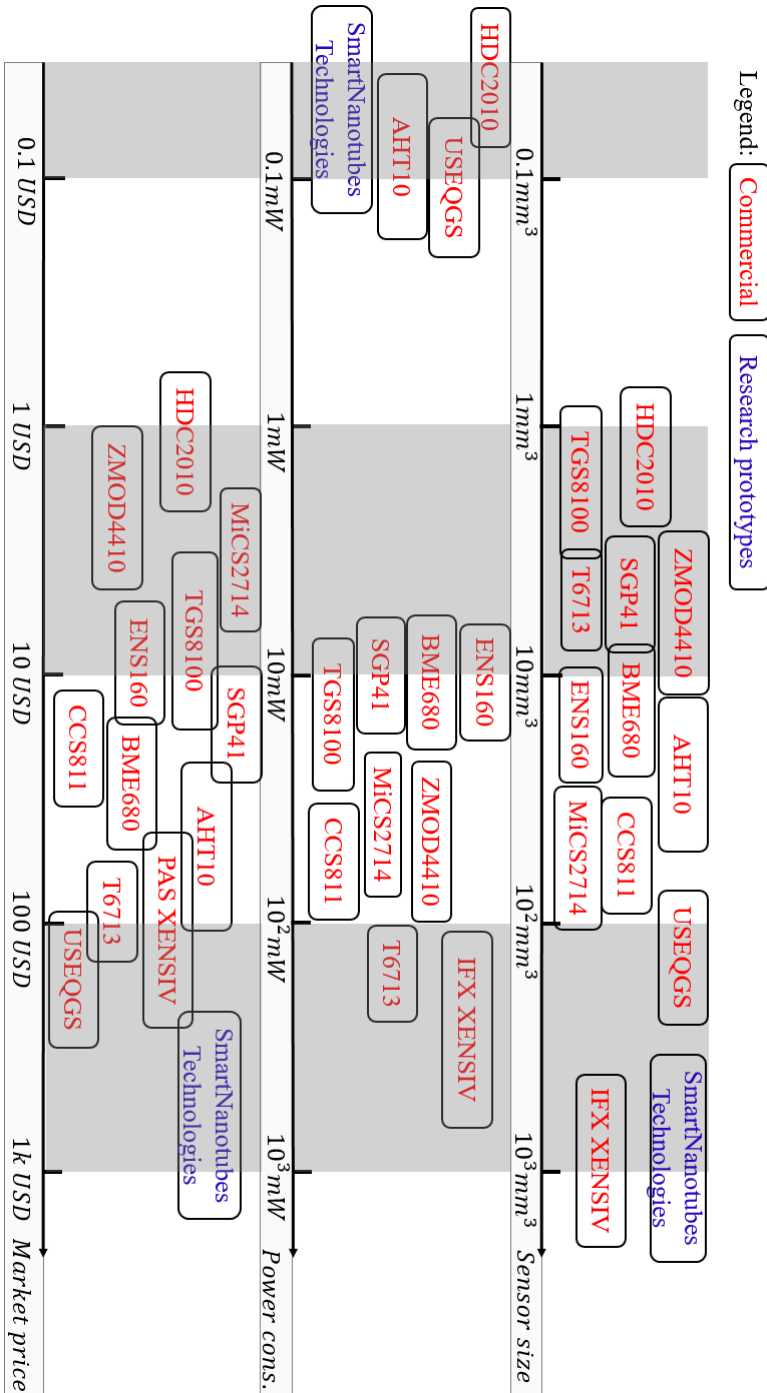
Figure 1.6: Comparison of gas sensing technologies (both commercial and research prototypes): size, power consumption and market price.

2 Embedded Sensing Platform

This chapter presents the concept, realization, and performance evaluation of a portable, customizable embedded platform for suspended CNT-FETs published in [3]. The ability of the semiconducting CNT-FET device to change its electrical characteristics [79] [111] when exposed to NO_2 makes it a promising candidate for sensing applications. Thanks to its low-power operation at room temperature and nanoscale physical dimensions, CNT-FET-based NO_2 sensors are well-suited for integration into IoT air-quality monitoring applications [106]. However, the CNT-FET gas sensor suffers from few main shortcomings despite its great potential: while the device allows sensing signals down as low as tens of *ppb* [83], the device-to-device variations [6], aging effects [152], hysteresis [153], humidity cross-sensitivity [111], and relatively noisy output signal [111] [4] can make the readout design electronics a challenge [154][3]. The platform's hardware can adapt to the nanosensor requirements and can measure a wide current range. In addition, this prototype is fully autonomous and reconfigurable, employing a user-defined instruction set. The chapter ends by summarizing the performance of the embedded system and the CNT-FET nanosensor compared to other research gas sensing solutions.

2.1 Conceptual design

A battery-operated, fully autonomous, customizable, embedded sensing platform for resistive CNT-FET nanosensors is desired. The concept starts with a solution that can cope with the sensor's main drawbacks. The highest level of flexibility compensates for the device-to-device variations with programmable source-drain bias, gate bias, and bias time intervals via digital-to-analog converters (DACs) [155]. Multi-channel drain currents with programmable ranges are designed to digitize sensor signals with the help of a current-to-digital converter (CDC) [5]. The embedded system is programmable with the help of a microcontroller that steers the building blocks mentioned above via the serial peripheral interface (SPI) or I^{2}C and RS232/RS485 interfaces. It offers Bluetooth low energy (BLE) [156] wireless connection, an SD card

[157] and operation modes for high energy efficiency. The block schematic of this system is presented in Figure 2.1.
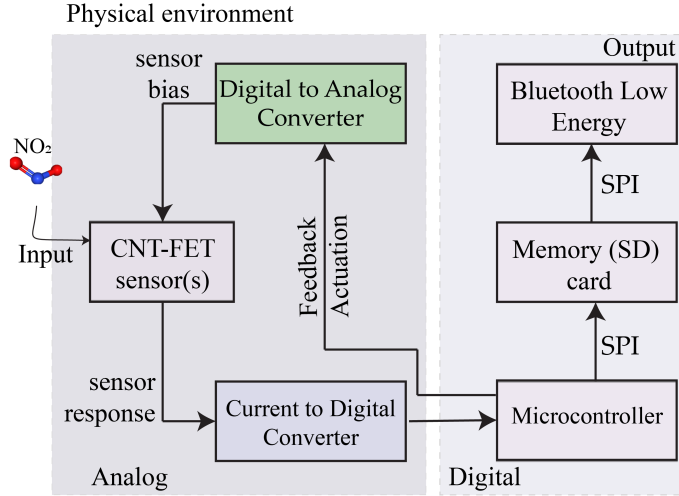
Figure 2.1: Block schematic of the embedded platform divided into two parts: the analog section including nanosensor within a control loop with DAC actuation and sensor response fed to a CDC. The digital section comprises the microcontroller, SD card, and BLE peripherals connected using an SPI protocol. Open Access figure reproduced from [3] published under the terms of Creative Commons CC BY license.

In a sensing application, the CNT-FET device, introduced in chapter 1.3.3, can be used as a voltage-biased FET device [158][159]. When used as a nanosensor, a first prerequisite for the CNT-FET is finding the optimal bias conditions such that the response time is minimized [4], the gas analysis sensitivity maximized [111], and the recovery time minimized without a substantial sensor degradation [79]. Moreover, the CNT-FET sensor is still developing in terms of device architecture [6] and the fabrication processes [83]. The set of preliminary specifications is highlighted below:

- Four variable current input range up to $7\,\mu A$

- Variable resolution of the ADC higher than $12\,bit$.

- Variable sampling rate up to few $kSps$

- Four independent CNT-FET drain bias voltages programmable in the range $0\,V$ to $+5\,V$

- One common CNT-FET gate bias voltage programmable in the range -10 V to +5 V

- Local data storage

- Wireless connection, i.e., BLE

- Low power consumption: $\leq 100\,mW$

2.2 CNT-FET(s) drain bias

Due to high device-to-device variations and potential degradation effects of CNT-FET sensors, as presented in [152], an adjustable/re-programmable system is desirable. This is realized through the possibility of individually accommodating an adaptive bias voltage for each CNT-FET. The bias voltage of each sensor is software-defined and converted by two dual 12-bit DAC MCP4922 [155] with a $1.25\,mV$ resolution on each drain channel. This simple software-based solution allows easy adjustment of parameters via SPI, such as sensitivity or current baseline [4], which can be dynamically tuned over time between devices, and extended towards automatic calibration procedures. Additionally, the CNT-FETs can be biased with drain V_{DS} potentials up to $V_{bat.}=5\,V$. As a result of the higher currents passing through the device, the effect of Joule heating promotes faster desorption of the gas molecules from the sensor surface, thus shortening the transition between sensor operation and reset state [79] or allowing for dynamic signal evaluation using pulsed heating of the tube [4]. The $V_{bias1...5}$ outputs dedicated for CNT-FET bias are presented in block schematic (top part) as in Figure 2.2.

2.3 CNT-FET(s) gate bias

In the case of a p-type CNT-FET device (characteristic shown in Figure 1.5.d), the V_{GS} bias voltage must be negative and higher than $V_{bat.}$ (the battery voltage potential referred to ground). This negative voltage is locally inverted and boosted on the embedded platform when using a single battery as supply voltage, i.e., $V_{bat.}$. This functionality is implemented using two charge-pumps MAX660 [160], connected in cascade, which is designed to double and invert the $V_{bat.}$ potential. The block schematic is presented in the bottom part of Figure 2.2. An additional op-amp configured as shown in Figure 2.2 generates V_{bias5} and enables the CNT-FET V_{GS} programmability. This can be implemented for pulsed gate sweeps, reducing hysteresis in the

sensing application [153]. Using the superposition principle applied on the linear op-amp, the V_{bias5} potential can be programmed in the following bias interval expressed as:

$$V_{bias5} = V_{bat.} \cdot \left(3 \cdot \frac{SPI_{code}}{2^{DAC_{res.}}} - 2 \right) \in [-2V_{bat.}, V_{bat.}] \qquad (2.1)$$

where $V_{bat.} = 5\,V$ is the battery voltage supply, $DAC_{res.}$ represents the DAC resolution, and SPI_{code} input code, respectively. As a result, the CNT-FET V_{GS} bias potential can be programmed in the $[-10,\ 5]\,V$ range with $3.65\,mV$ resolution by the help of V_{bias5}.
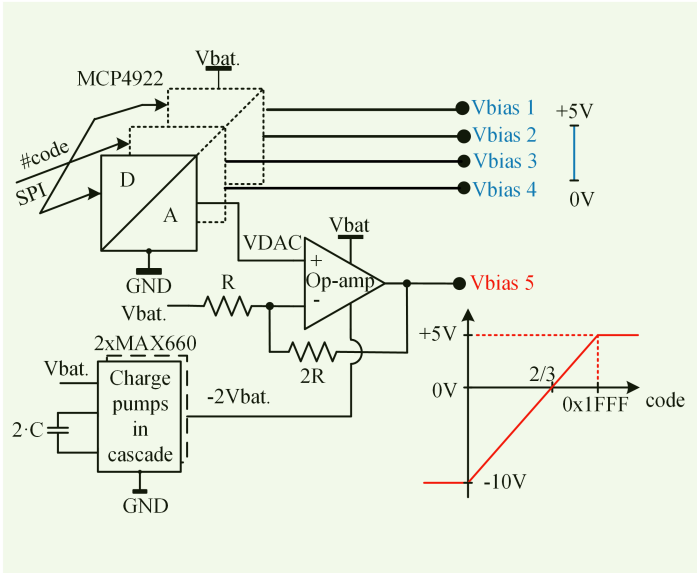
Figure 2.2: Block schematic for the CNT-FET(s) bias. Four individually programmable channels, $V_{bias1...4}$, in the range of $[0,\ 5]\,V$. One common programmable gate channel, V_{bias5}, in the range range of $[-10,\ 5]\,V$.

Figure 2.3 shows an example of the bias block functionality for both the unipolar and bipolar outputs. This was realized by following a repetitive bias scheme output, including the timing of one second bias period wherein the duty cycle is $0.7\,seconds$ ON and $0.3\,seconds$ OFF.
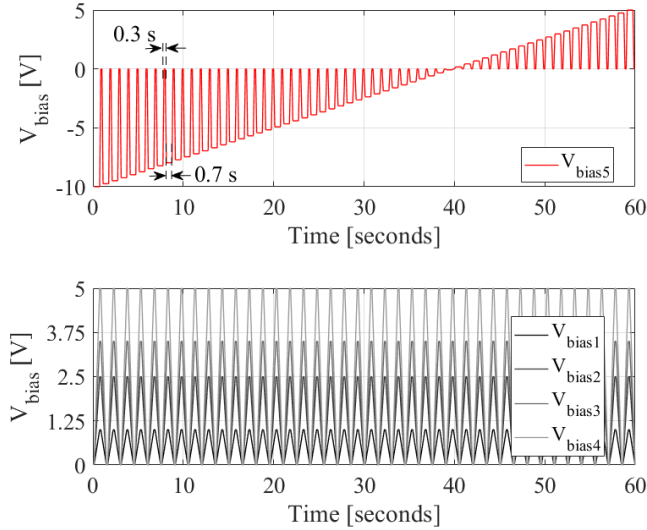
Figure 2.3: Example of the programmed bias block for the unipolar V_{bias1} to V_{bias4} (bottom) and the bipolar V_{bias5} (top). Open Access figure adapted from [3] published under the terms of Creative Commons CC BY license.

2.4 CNT-FET(s) sensor signal acquisition

Current sensor readout is a widely used technique for acquiring fA to μA signals from nanosensors, e.g., nanopores for DNA sequencing [161], organic-FET for single-molecule detection [162], and CNT-FET for gas sensing [80]. The embedded platform design uses this technique, implementing current integrators operating as current-to-voltage converters for resistive sensors, i.e., voltage-biased CNT-FET(s) devices. In practice, current integrators can be built as continuous-time (CT) or discrete-time (DT) implementations. Both architectures have their advantages and disadvantages, which can be shortly summarized in the following paragraph.

The CT implementation encounters the trade-off between input-referred noise set by feedback resistor, low-frequency integration capability, and op-amp saturation. Moreover, in the context of a field sensing application, the out-of-band interference signals injected in the virtual ground force the op-amp to source/sink the same amount of current independent of the signal frequency. On the other side, the DT method suffers from noise modulation due to periodic reset, limited dynamic range imposed by the trade-off

between input signal level and in-band noise, and clock jitter requirements. A comprehensive review of those two approaches with their pros and cons, including noise analysis and performance comparison, can be found in [163].

The DT architecture is chosen here since it usually offers more degrees of freedom, i.e., full-scale range and sampling frequency configuration through a digital interface. This CT design decision is chosen for the ASIC, i.e., the TIA block as the dedicated version for the CNT-FET nanosensor application, and is presented in chapter 3.4.1.

2.4.1 Current-to-digital converter (CDC)

This block represents the core of the embedded platform, defining its performance; hence it deserves special attention. As an architecture, the DT has been chosen over the CT topology since it offers the highest flexibility, i.e., it can be dynamically tuned through software. Consequently, the quad-channel DDC114 [5] current-to-digital converter from Texas Instruments has been selected as being an optimum solution for the application. This IC implements a "true-integration" function with the help of tandem working switched-capacitor integrators [164] over a variable period. Moreover, when sensing below nA currents, the tandem working DT solution suppresses the modulated noise introduced by the periodic reset compared to the single DT integrator [165]. The periodic reset appears as a noise voltage multiplied by a square wave and duty-cycled with a ratio of integration period divided by sampling period [163] for a single op-amp DT integrator. As an effect, the white noise changes from a stochastic to a cyclostationary process with time-varying statistical functions [165], which decreases the DT integrator's SNR when reset frequency increases [166]. To mitigate this effect, DDC114 uses a switching scheme between two op-amps with feedback capacitances of the same value, also known as "ping-pong" implementation. The Figure 2.4 shows the simplified schematic of DDC114 reproduced from [5] together with the timing diagram that controls the switches of the front-end when implementing the time-interleaved integrators in "Convert" and "Integrate" configurations. The other two phases, i.e., "Reset" and "Wait" configurations, are not shown in Figure 2.4 for simplicity. In practice, for this scheme to work, the mismatch between the two integrators, such as feedback capacitors and offset of op-amps, requires a careful design and compensation of process variations. Another solution that simplifies the matching requirements is implementing the "ping-pong" operation between two capacitors with only one op-amp, as proposed in [166]. However, despite its simplicity and reduced power consumption, the "true-integration" feature would not be possible anymore, which might cause a loss of input data.
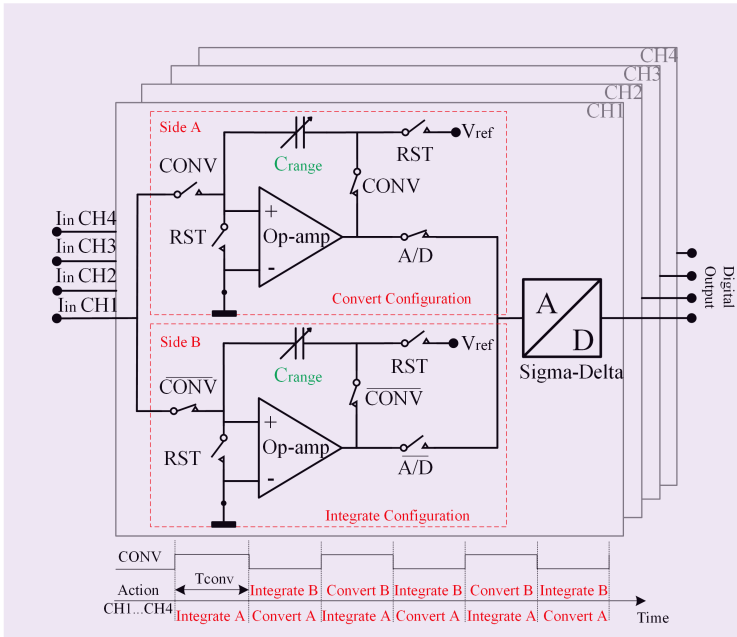
Figure 2.4: Detailed schematic structure and timing of the front-end true integrators, including analog to digital (AD) converter inside the DDC114. Block schematic adapted and simplified form [5].

In the context of CNT-FET nanosensors, several DDC114 key attributes, i.e., variable sampling rate, conversion with a selectable resolution (RES.), a full scale (FS) range, and noise FS, are presented in the following paragraphs.

2.4.2 DDC114 CDC operation principle

The DDC114 front-end integrators can be programmed by the T_{conv} and C_{range} variable parameters, namely the conversion time and integrating capacitance. The bottom part of Figure 2.4 shows the T_{conv} signal diagram which controls the $CONV$ and $\overline{CONV}$ switches, common for all eighth DT integrators. The timing is a critical design parameter for a correct operation and obtaining a high-precision digital representation of the CNT-FETs currents. For this purpose, an external timer integrated into the microcontroller (ATmega 2560 [13]) has been used. The pre-scaled 16 MHz system clock increments this timer, running in a clear timer on compare (CTC) match mode [13]. With this implementation, the OCR0A drives the conversion period T_{conv}, which thus can be programmed in the interval of [2000...0.64] ms. A complete conversion of all four-channels takes only $2 \cdot T_{conv}$ (one

integration period) for the DDC114 [5]. Hence this would give a variable sampling rate from $[0.001...3.125] \, kSps$, which can be set with the granularity of f_{OCR0A} [13] interruption timer. The C_{range} operation parameter chooses the integration capacitors by selecting a combination of three dedicated bits, which connects one out of eight possible values formed by the capacitor bank, namely: $[3, 12.5, 25, 50] \, pF$.

Additionally, the ATmega 2560 analog comparator on $AIN1$ input is used to synchronize with the system clock the $DVALID$ signal (not shown in Figure 2.4 for simplicity) sent arbitrary by the DDC114 [5]. This completes the front-end DT integrators, which are configurable, as summarized next.

2.4.2.1 Full-scale range

When choosing the integration period T_{conv} and C_{range} parameters, the full-scale (FS) can be programmed between $[1.5 \, nA - 7.2 \, \mu A]$ which is well in line with the typical CNT-FETs drain current [79]. The output data format can be selected by the desired resolution (res) of [16; 20] bits which corresponds to an $I_{in}[LSB]$ of $[1.4; 23] \, fA$ and $[6.8; 109] \, pA$, respectively. As a result, the four channels' digital output $[CH_1 : CH_4]$ can be expressed as:

$$Out_{FS} = \left[\frac{I_{in(1:4)}[nA] \cdot T_{conv}[\mu s]}{C_{range}[pF] \cdot V_{REF}[mV]} \cdot \left(2^{res[bit]} - 1 \right) \right] + 2^{(res[bit]-8)}, \quad (2.2)$$

where $V_{REF}{=}4096 \, mV$ is the DDC114's external voltage reference [167], and the factor $2^{(res-8)}$ depicts the readout value at zero current input. This value corresponds to approx. 4% of the FS range [5] and represents an offset intentionally introduced as a safety margin that prevents negative input currents due to PCB parasitics or leakage currents. Level contours illustrating the FS current input range as a function of the two independent parameters T_{conv} and C_{range} are presented in Figure 2.5.a.

2.4.2.2 Signal-path bandwidth

The bandwidth (BW) of the DT front-end integrators of the DDC114 can be calculated as for CT integrators where the selected feedback capacitor C_{range} stores charge for the programmed integration time T_{conv}. Here, the frequency response of the Sigma-Delta ADC that follows the front-end integrators, as presented in Figure 2.4, does not influence the BW of the DT integrators since it operates at a constant higher sampling frequency. As a result, the

a)   b)
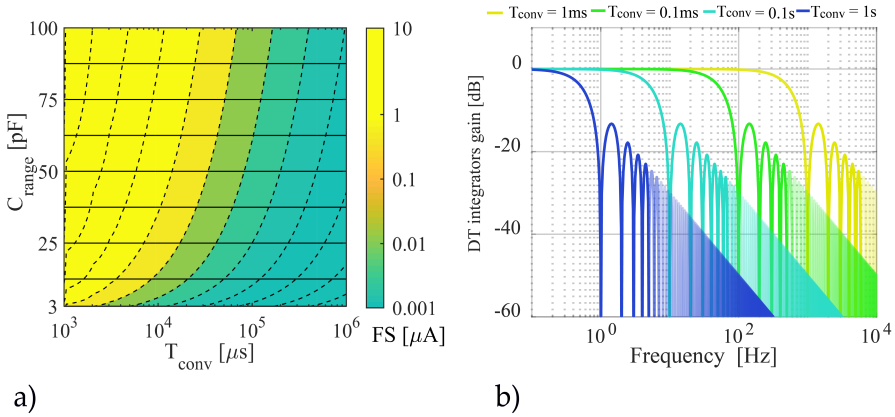
Figure 2.5: Front-end FS range of the DT integrators obtained by: a) configuring the two parameters T_{conv} and C_{range} parameters individually; b) the resulting BW of DT integrators after configuring a T_{conv} time interval. Open Access figure adapted from [3] published under the terms of   Creative Commons CC BY license.

system's bandwidth can be estimated by evaluating its transfer function (see Appendix A.1), which is expressed as:

$$DDC114_{int\ gain} = \frac{1}{C_{range}} \cdot \frac{sin\left(\pi \cdot T_{conv} \cdot freq\right)}{\pi \cdot freq} \ [V/A] \qquad (2.3)$$

For the fine-tuning of the frequency response at a given FS, one can set a T_{conv} and C_{range} as shown in Figure 2.5.b.

2.4.2.3 Thermal noise

The output noise in the digital representation of the DDC114 has different origins. From a system-level perspective, the noise of the CNT-FET itself and the noise of electrical circuits, i.e., PCB tracks, DT integrators, and AD converter quantization noise, is important. The first step towards system design in the presence of noise is to evaluate the noise sources individually and how they propagate towards the output through the signal path. Since DDC114 is a specialized IC without a detailed internal schematic available, its noise can be evaluated by monitoring the digital output result while being configured on the highest FS range, i.e., $I_{LSB} = 109\,pA$, with the current inputs left opened. The resulted output referred offset, and RMS noise is

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presented in Figure 2.6 and represents the internal noise produced by the DDC114 without the CNT-FETs connected yet.
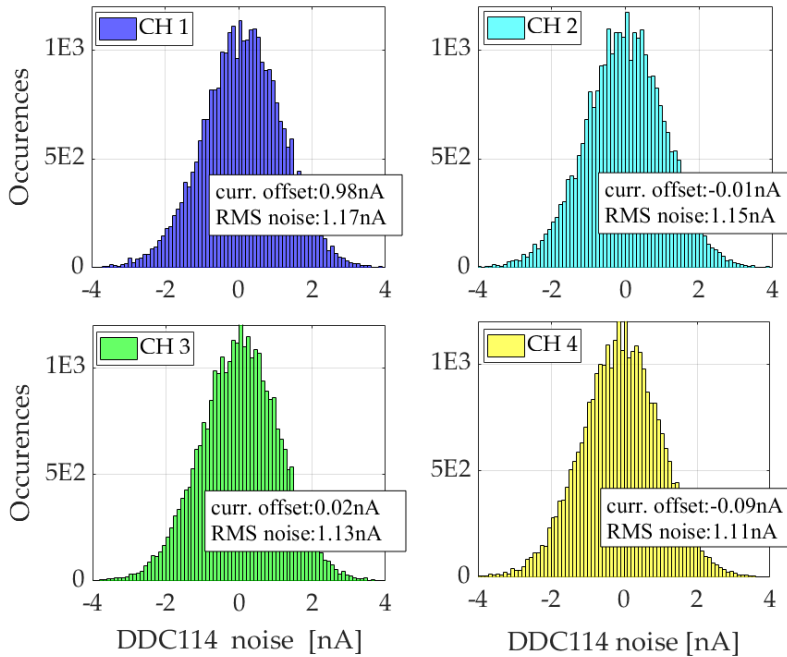
Figure 2.6: Equivalent output referred current noise of the DDC114 when all four channels are left open (and shielded). For this measurement the T_{conv} and C_{range} parameters were configured for highest FS range (worst case noise).

In the context of a CNT-FET NO_2 sensing application, the sensor's noise needs to be lower or comparable with the noise introduced by electronics. This experimental determination has been performed with the help of lab equipment [6] with superior performance, i.e., $4.3\,fA/\sqrt{Hz}$ input noise, used to acquire CNT-FET currents while being exposed to the analyte of interest at several concentrations within the desired range of measurements. The resulted currents after one hour of exposure for each NO_2 gas concentration of $[0, 20, 140, 500]\,ppb$, and at two distinct bias points $V_{DS} = [0.2; 0.5]$ V are presented in Figure 2.7. The noise RMS level of the CNT-FET is bias dependent and NO_2 analyte dependent, as highlighted. In the best-case scenario, at $10\,nA$ drain current, when exposed to $20\,ppb$ NO_2, the CNT-

FET RMS noise level is comparable with the DDC114 in worst-case scenario, as presented in Figure 2.6.

The noise contribution of the CNT-FET resistive nanosensor, which is NO_2 gas-dependent, must be included as a contribution of the DDC114 output referred noise. The CNT-FET noise contribution can be modeled using the current source equivalent circuit because of the DDC114 current inputs. The CNT-FET equivalent resistor connected to the DDC114's input appears to produce a significant amount of thermal noise at first sight. However, the additional output referred noise decreases as the CNT-FET resistance values increase in this configuration. When considering thermal noise, the voltage noise's spectrum density is proportional to the resistance value. Complementary, the spectral density of current noise is inversely related to the magnitude of resistance when using the Thevenin equivalent (a current source in parallel with the noiseless CNT-FET) [168]. In other words, the lower the NO_2 gas concentration, the higher the CNT-FET resistance, and the lower the DDC114 output referred noise. By considering this a linear system, the mean-squared output noise can be calculated as a function of the DDC114 transfer function expressed in Eq. 2.3 and the CNT-FET input noise as:

$$\overline{Out_{R_{CNTFET}}noise}^2 = \int_0^\infty \underbrace{\left| \frac{sin\left(\pi \cdot T_{conv} \cdot freq\right)}{\pi \cdot freq} \right|^2 df}_{DDC114\ transfer\ function} \cdot \underbrace{\frac{4kT}{R_{CNTFET}}}_{CNTFET_{noise}} \cdot \frac{1}{C_{range}^2}$$

$$(2.4)$$

The expression of the internal noise Power Spectral Density (PSD) can be expressed (complete derrivation in Appendix A.2) in terms of FS as:

$$Out_{R_{CNTFET}}noise = \frac{\sqrt{\frac{4kT}{R_{CNT}(NO_2)} \cdot \frac{T_{conv}}{2}}}{C_{range}V_{REF}} \cdot I_{FS}, \qquad (2.5)$$

where I_{FS} represents the FS current that can be resolved by DDC114 for a given FS configuration as shown in Figure 2.5. The current noise calculated in Eq. 2.5 is inversely proportional to the value of R_{CNT} as this equation shows. This translates into a small current noise contribution at low gas concentrations where the CNT-FET resistance is relatively high [83]. Since the two noise sources are statistically independent, they can be added in

power. Hence the total noise of the embedded signal path can be expressed as:

$$SPout_{noise} = \sqrt{DDC114_{noise}^2 + Out_{R_{CNTFET}}noise^2} \qquad (2.6)$$
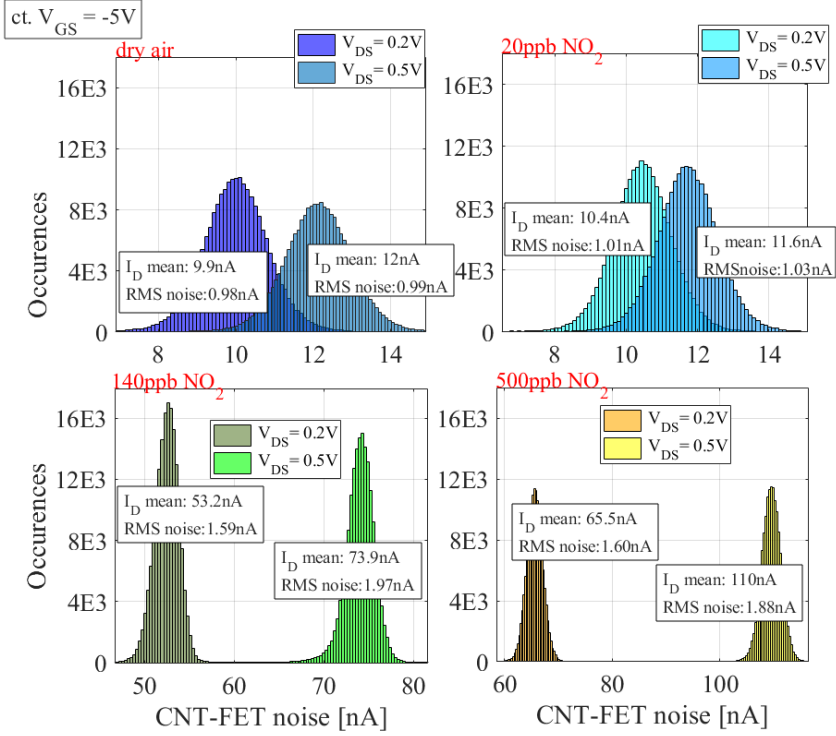
Figure 2.7: CNT-FET current mean and RMS noise values when exposed to $[0, 20, 140, 500]$ ppb NO_2 at $V_{DS} = [0.2; 0.5]$ V and constant $V_{GS} = -5V$. Data are acquired by high precision lab equipment: CT integrator Femto DLPCA-100 with gain of 10^6 Ω, acquisition board NI_{6289} used for V_{DS} bias generator and AD conversion. The complete measurement setup is described in [6].

Figure 2.8 shows the results of signal-path (SP) output noise vs. NO_2 gas concentration according to Eq. 2.6. The same figure evaluates also the CNT-FET bias influence on the resistance R_{CNT}.
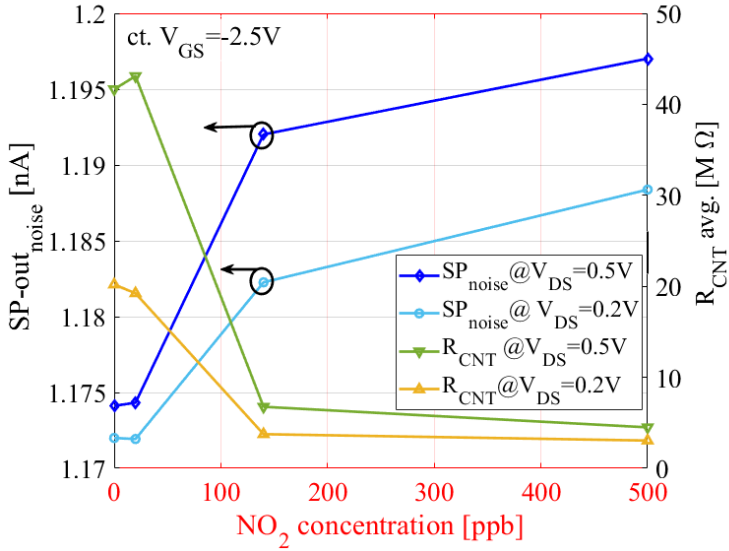
Figure 2.8: Embedded platform's signal path output noise vs. R_{CNT} as a function of NO_2 gas analyte.

2.5   Embedded programming

To automate the CNT-FETs NO_2 gas sensing routine, an event-triggered finite state machine (FSM) runs on the embedded platform's microcontroller. The FSM's working principle has its origin in the well-known Turing machine [169], the theoretical computing machine invented by Alan Turing [170]. Today, it still deserves attention since FSMs are some of the most software-implemented structures, e.g., for behavioral modeling of artificial intelligence (AI) algorithms.

2.5.0.1 FSM theory

A finite-state machine (FSM), also known as a finite-state automaton (FSA), is a computational model that maps an input sequence to an output sequence. This model can be characterized by a mathematical structure in which the previous state(s) (as well as the machine's inputs) determine the next state. The FSM can be summarized using a seven-tuple [171] as follows:

$$FSM = \langle X, Y, Q, \delta, \lambda, Q_0, Q_n \rangle , \tag{2.7}$$

45

where:

- $X_{1\cdots n}$: a limited set of input symbols (input alphabet)

- $Y_{1\cdots n}$: a limited set of output symbols (output alphabet)

- $Q_{0\cdots n}$: a limited set of internal states (computation mechanism)

- δ_{ij}: transition computation ($X_i \times \underbrace{Q_j \times Q_{j-1} \times Q_{j-2} \times \cdots Q_{j-n}}_{FSM\ memory\ depth} \to$
  Q_{j+1})

- λ_{ij}: output computation ($X_i \times \cdots \to Y_{i\cdots}$)

Depending on λ_{ij} expression, two types of FSM architecture can be distinguished:

1. Mealy FSM: output determined by current state and current input ($\lambda_{ij} = X_i \times Q_j \to Y_{ij}$)

2. Moore FSM: output determined by current state only ($\lambda_j = Q_j \to Y_j$)

It can be seen that in the Mealy FSM, a change in the input causes an immediate change in the output. This might become problematic for digital implementation, presented as follows, since it creates asynchronous feedback loops. Moreover, memory depth of one is more common in practice.

2.5.1 Hardware described v.s. the software described FSMs

The FSM can change its internal states based on inputs, becoming a fully autonomous measuring system. The modern FSM implementation is usually designed as an automata pattern in the VHDL hardware description language. More recently, integrated development environments (IDEs) offer helpful tools for enabling low-power FSM development on the microcontroller. Interrupt service routines (ISRs) are highly desirable when combining multiple peripherals in a microcontroller environment. This facilitates the design of an event-driven sensing system. In Figure 2.9 the three main parts of an interrupted-based Moore FSM are shown:

a) System setup: executed only once at power-on reset for configuration

b) ISR: placed before the *Void loop ()* and executed on demand

c) FSM core: executed in an endless loop
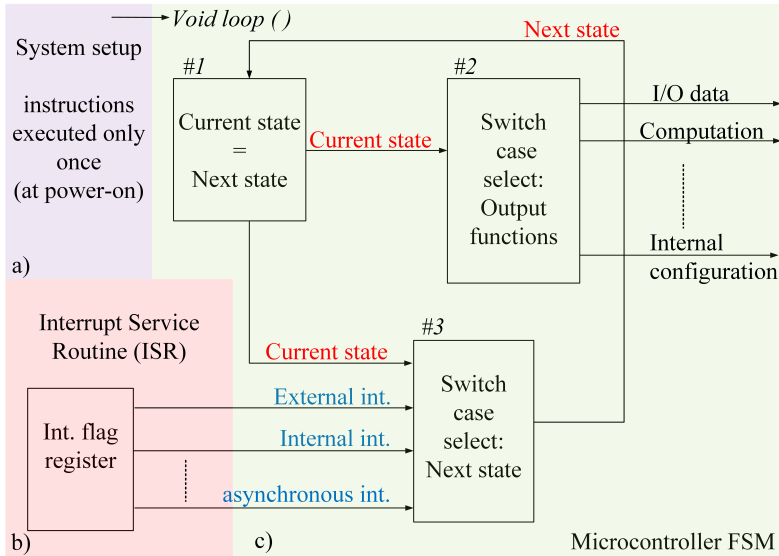
Figure 2.9: Block schematic of a generic FSM structure implemented on the microcontroller: a) system setup configuration; b) ISR handling register; c) FSM core implementation.

The FSM core is executed in the *Void loop ()* and shows that the machine's functionality can be divided into three functions executed in the following order:

1. Actualizes the Current state as being the Next state calculated lastly

2. Output functions take the Current state as input values and produce a value as output

3. State-transition functions take input values and current state as inputs and compute the next state as output

2.5.2 Interruption-based v.s. input-pulling execution

There is a fundamental difference between interrupt and polling code execution. In polling code, the central processing unit (CPU) checks the status

of the peripherals in a loop and finds if they require a routine execution. In contrast, an external or internal interruption routine notifies the CPU by an interruption flag [13] for executing an instruction sequence a priory described within the code. The two distinct implementations are presented in Figure 2.10, for comparison.
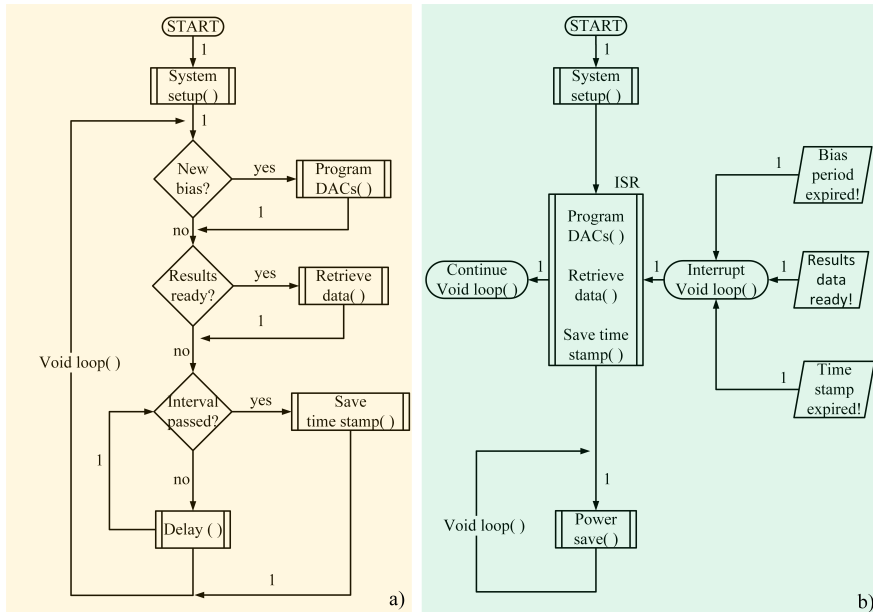
Figure 2.10: Execution flow chart for the two distinct programming modes: a) polling mode where four loops are nested in the fifth big loop; b) for comparison the implementation with only one loop and waits for interruptions.

From a practical perspective, the event-driven interruption on a microcontroller allows dividing the FSM execution code as well-determined routines, often called "structural programming." In this case, triggering FSM state transitions with interruption flag registers set by external peripherals is feasible when all states, inputs, and outputs are defined. Hence, writing the FSM execution code becomes straightforward once the entire system's functionality has been described. Moreover, testing the code is now effortless: run through every possible state-input pair and check that the outputs and state transitions behave as intended.

As seen from Figure 2.10, the interruption-based code is an alternative to the several nested loops and inputs polling when programming the FSM structure. This implemented interruption-based enables even more advantages, e.g., modifying, adding, removing, or reordering FSM states by avoiding the

super loop full of "spaghetti code." The embedded platform can fully explore these features as they are described next.

2.5.3 Implementation of FSM for measuring NO$_2$ gas concentration

Event-triggered FSM is presented in Figure 2.11 inside the circles, the FSM's internal states are shown. The arrows represent the transition between individual states, and the logic condition is highlighted unless it is "1", which means by default. The power consumption of each state is highlighted by the corresponding color of *Low*, *Medium*, and *High* power levels.

The structure of the event-triggered FSM can be better understood by dividing it systematically into three distinguished FSM parts:

1. **Inputs:** any event that requires the system to generate an output or change its behavior is an input. The embedded platform has three input scenarios: power-on reset, SPI peripheral (SD card, DACs, DDC114), and internal timers [13]. The individual inputs are highlighted above the arrows interconnecting states in Figure 2.11.

2. **State transitions:** the arrows in the state diagram of Figure 2.11 represent state transitions and highlight the FSM's internal state change. A state transition appears whenever an input produces an output that changes the state of the FSM. An input can only trigger a state transition at a time. The state transitions also define how the embedded platform performs a complete sensing routine. For example, no arrow connects the *Sensor Bias* with *Save results on SD card* directly. Therefore, every bias change is followed by the CNT's current acquisition (*Read Sensor Currents* and *SPI Transaction*).

3. **Outputs:** the functions that have to be executed by the FSM in response to an input. In Figure 2.11, the outputs are illustrated as circles between the transition arrows. The FSM generates a unique output following an input event, i.e., state transitions. An additional state called *Power Save* is executed so long as the microcontroller receives no interruption. The internal microcontroller peripherals and unused peripherals are turned off to save power consumption in this state. For this specific measurement routine, the embedded platform has seven outputs: *Sensor Bias*, *Read Sensor Currents*, *SPI data Transaction*, *Save results on SD card*, *Log activity on BLE*, and *Power Save IDLE*. Note that the double circle represents the final state when the FSM is finished and ready to restart.
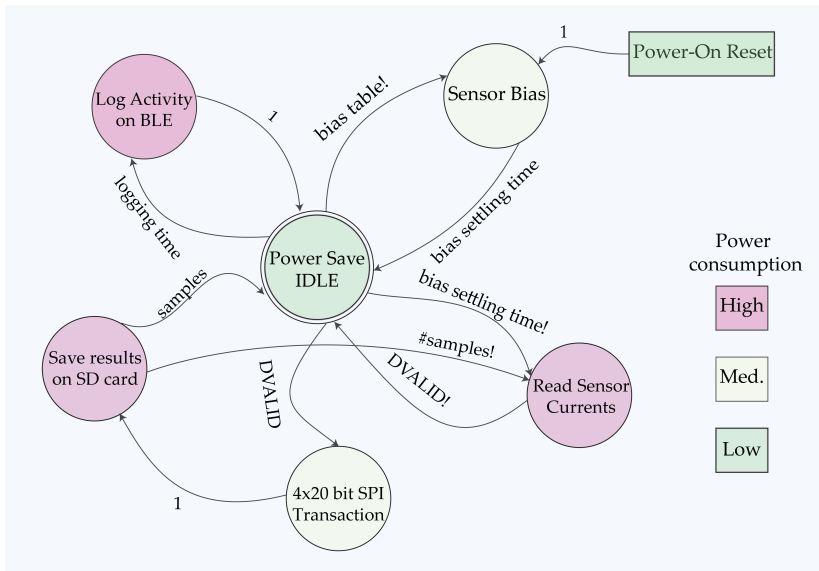
Figure 2.11: Illustration of the FSM states and state transitions and their corresponding power consumption. Open Access figure adapted from [3] published under the terms of Creative Commons CC BY license.

The discrete actions of each state composing output functions (circles) of the FSM are presented in Table 2.1.

2.5.4 SD card data file system

As presented before, this architecture is fully reconfigurable with the help of its inputs. For example, the state transitions of the FSM can be configured by a standard comma-separated (CSV) file stored on the SD card. The *Stimuli.CSV* file contains a customizable potential bias scheme that operates the CNT-FET(s) for a predefined time interval. The resulting current measurements are stored in a separate *Results.CSV* file on the SD card. Note that two consecutive measurement sessions will not overwrite the data but store the existing results with a new timestamp. Figure 2.12 overview of the configuration file system. The SD file system and block and data path are shown starting from the input *Stimuli.CSV* file and feeding the microcontroller's configuration registers. The internal timer interruptions steering the FSM execution can be dynamically configured on the flight. Moreover, external interruptions for the CDC and the desired bias voltages for the DACs are configured. Consequently, this timing and voltage amplitude is applied to the CNT-FET(s) terminals and the CDC and digitizes the analog currents saved on the SD card as *Results.CSV* file.

Sensor Bias	Read Sensor Currents	4x20bit SPI Transaction	Save on SD card	Log activity on BLE	Power Save IDLE
-dis. interrupts	-dis. interrupts	-dis. interrupts	-enable SD CS	-create string	-set SMCR
-reset DDC114	-stop TCNT5	-dis. TCCR3B CONV	-save times tamp	-start a serial port	-wait for OCF2A
-enable SD CS	-en DDC114	- create data buffer	-save bias values	-send to the BLE	
-read bias timing	-TCCR3B for $T_{conv.}$	-begin SPI transaction	-save current values		
-conf. OCR1A	-TCCR3B start	-end SPI transaction	-disable SD CS		
-conf. OCF2A	-ACSR for DVALID	-split CH1-CH4 res/			
-read bias values	-ACIE analog comp	-convert bit to μ A			
-disable SD CS	-ACIE rising edge	-reset DDC114			
-endable DACs CS	-ACIE int. BG	-en. interrupts			
-set Bias1 value	-en. interrupts				
-set Bias2 value					
-set Bias3 value					
-set Bias4 value					
-set Bias5 value					
-configure TCNT5					
-start TCNT5					
-DACs settling					
-en. interrupts					

Table 2.1: Description of each state output function (circles) of the FSM. The full name of the involved registers (written in capital letters), together with their functional description can be found in [13].
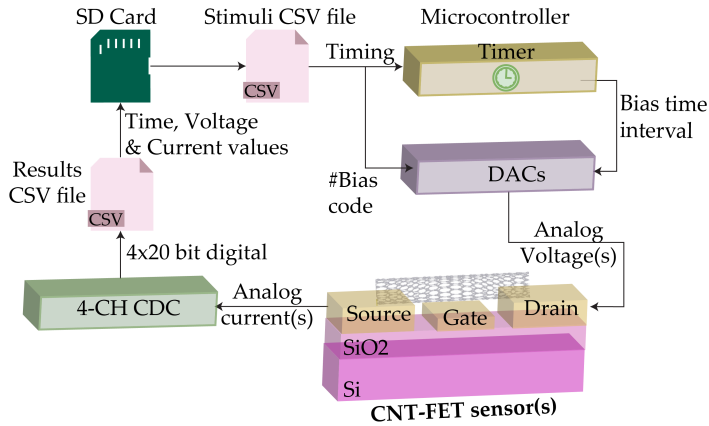
Figure 2.12: SD file system and block configuration illustrating the *Stimuli.CSV*. The file feeds the microcontroller and configures internal timers interruption for FSM execution, external interruptions for the CDC, and the desired bias voltages for the DACs. The CNT-FET(s) sensor measurement cycle ends with the digitized currents added on the SD card under *Results.CSV*. Open Access figure adapted from [3] published under the terms of Creative Commons CC BY license.

2.6 Physical design

The embedded platform's physical design, debugging, and characterization was conducted within a semester project in the department by Pascal Schläpfer [172]. The project aimed to structure the prototype previously realized on break-out boards into a compact embedded platform as shown in Figure 2.13. The design includes the test chamber footprint for lab measurements. In this development phase, it has been appreciated that the platform can be realized on a standard two-layer PCB. The SMD components and interconnections were placed on the top layer, and the ground plane was located on the bottom. For the physical design development, several practical considerations were taken into account:

- **Signal-path integrity:** since the measurement currents are in the nA to μA range, the CDC subsystem layout requires special attention. The DDC114 is placed close to the test chamber, where the CNT-FETs are exposed to the gas analyte. The voltage reference [167] is placed as close as possible to it. In addition, no tracks are routed below the measurement signal tracks before they are fed into the DDC114 analog

inputs. The four channels are shielded with a copper ground plane around them, as is recommended in the datasheet [5]. In Figure 2.13, the CDC is not visible since it is located under the BLE module.

- **Power supply:** the power supply and ground routing require a careful design for complete signal integrity. This has been realized considering the five golden rules when designing a PCB. First, this implies having clean ground, i.e., not disturbed by spikes (sudden sharp changes in potential) induced by any neighbor component. Second, decoupling capacitors are essential since digital circuitry operating on fast clock signals can create battery voltage drops or spikes in the analog domain. Third, low noise and low drop-out (LDO) regulators are placed for the different analog and digital supply domains. The analog and digital grounds are separated as a star connection routing starting from the battery connector. Fifth, no power tracks and only the necessary signal tracks are routed on the bottom layer, perpendicularly on the top layer (where possible).

- **Physical dimensions:** The sensor platform is not as compact as the current technology would allow it to be. The footprint of the test chamber gives a substantial part of the dimensions overhead for the final platform dimensions. The test chamber is the mechanical component that seals the CNT-FET(s) socket, and the embedded platform can be directly connected to the lab measurement setup. It enables measurements within the well-controlled gas flow and humidity profiles. This is aligned with an edge of the PCB, which makes it compatible with the gas setup fixture [6]. Figure 2.13 illustrates its positioning and size relative to the other electronic components of the embedded platform. The PCB is held as small as possible while using the elements at hand. As can be seen in Figure 2.13, the test chamber occupies about 50 % of PCB area.

2.7 Power consumption

Table 2.2 illustrates the distributed power consumption (reported in the datasheets of the components) among all main building elements of the embedded platform when running actively. For comparison, the IDLE (stand-by and leakage) power consumption distribution over different components are presented too, in the second part of Table 2.2. It can be observed that tremendous average power reduction can be achieved by powering up only the individual components that need to operate at the time.
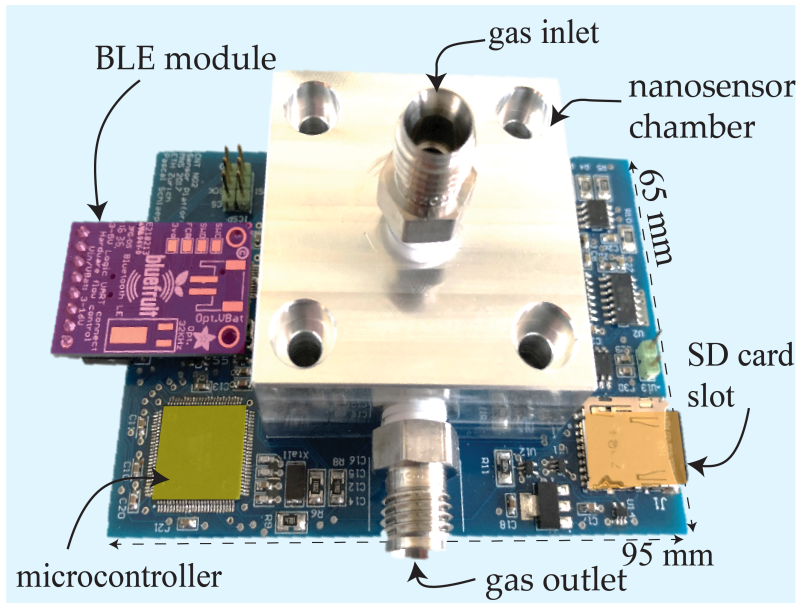
Figure 2.13: Image of the embedded platform with highlights of primary building blocks, including a test chamber in the middle with the gas inlet on the top and gas outlet on the side. The BLE module is on a separate break-out board attached to the platform. Open Access figure adapted from [3] published under the terms of Creative Commons CC BY license.

Consequently, an IDLE state of the FSM is highly desired, as introduced in section 2.5. It switches off unnecessary peripherals and puts the microcontroller into *Power Save* mode as already illustrated in Figure 2.11. When operating in this mode, a timer is still active and responsible for waking up according to the programmed bias timing loaded priory from *Stimuli. CSV* in Table 2.1. The measured power consumption of the platform is presented in Figure 2.14 when five current response samples were acquired in a row every five seconds, with an IDLE state in between. This sampling rate is typical for an environmental monitoring station at $1\,Sps$.

As illustrated in Figure 2.14, the power consumption in active mode, where the sequence of the FSM states *Sensor Bias*, *Read Sensor Currents*, *SPI Transaction*, *Save on SD card*, or *Log Activity BLE* is performed, results to a peak power of $225\,mW$. This value is lower than the theoretical one predicted in Table 2.2. When the microcontroller is on stand-by, and BT stays paired, the power consumption drops to $60\,mW$ in the IDLE state. This is, however, substantially higher than predicted, as in Table 2.2. In this case, the DDC114 power consumption overhead has been identified as responsible
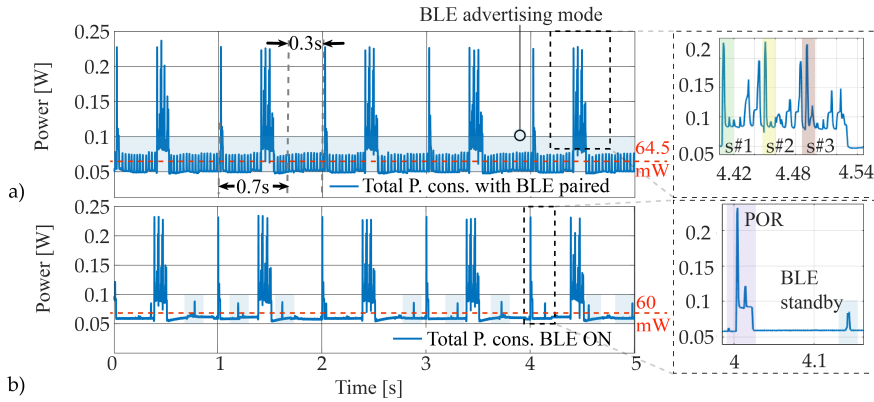
Figure 2.14: Power consumption of the embedded platform: a) while acquiring three *Sps* annotated as *s*1, *s*2, and *s*3 wherein the BLE power consumption is visible in the continuous peaks when operating in advertising mode compared with b) wherein fewer power peaks are observed when BLE is ON but not paired. The POR (power-on reset) power consumption is also visible when the IDLE state is left at each new bias period of one second with the corresponding duty cycle. Open Access figure adapted from [3] published under the terms of   Creative Commons CC BY license.

for the power consumption difference. In this design phase, the embedded platform achieves an average power consumption of $64.5\,mW$ when operated with the given measurement protocol. This value is suitable for a $5\,V$ power bank battery that can ensure up to nine days of continuous operation for the measurement protocol in this configuration. The overall power consumption in active mode can be further decreased when the state transitions are reduced, whereas the power in the IDLE state can be reduced close to the leakage level when more devices are disabled. Compared to the start-up SmartNanotubes Technologies presented in chapter 1 the power consumption of the embedded platform is still $4.5\,times$ lower. However, both solutions can improve their energy efficiency using a duty-cycle, which can be further developed through software.

2.8 Further development

2.8.1 Power consumption optimisation

The power consumption overhead in the IDLE state primarily originates from the operation of DDC114 [5]. Although the DDC114 has been driven in reset mode in this state, it still draws a DC power consumption of about $55\,mW$ (measured as a sum of VDDA and VDDD pins towards the ground). This has been validated by measurements at different sampling rates as presented in Figure 2.15a. When no sampling is programmed ($T_{conv} = 0$), the measured power consumption corresponds with the one measured in Figure 2.14. The measured values are for all four channels of the DDC114 at different sampling rates matched with the values reported in Figure 2.15a. The minor difference compared to Figure 2.15a is given by the V_{ref} analog reference [167], which is required for the DDC114 to operate. This power consumption overhead can be reduced by adding two switches for VDDA and VDDD, which can be turned OFF by the FSM whenever the CDC block is not used.
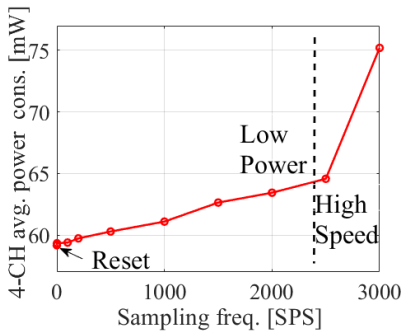
(a) Measured power consumption of DDC114 as a function of its the sampling rate.

(b) Peak power consumption reported in the DDC114 datasheet [5].

Figure 2.15: Open Access figure adapted from supplement of [3] published under the terms of Creative Commons CC BY license.

2.8.2 Relative humidity and temperature sensors

Basil Müller [173] conducted these two add-on features within a semester project in the department. The resulting design is presented in Figure 2.16.

2.8.2.1 Humidity sensor

A relative humidity (R.H.) sensor has been added to the embedded platform for cross-sensitivity to humidity experiments. The chosen sensor is an SMD component, i.e., the HIH-4030-001 [174] placed inside the test chamber to get more accurate R.H. measurements. The sensor output analog voltage has been connected to (the ADC9) channel of the microcontroller [13]. This enables the measurements amortization of the extended FSM.

2.8.2.2 Temperature sensor

In addition, a temperature sensor was placed inside the test chamber, next to the humidity sensor. An SMD Pt1000 [175] was chosen as a good fit for the test chamber. The sensor is connected as a voltage divider with a fixed resistor. The output voltage of the divider was then connected to the ADC7 [13]. The $10\,bit$ ADC at a reference of $5\,V$ can obtain a sufficient resolution of $1.07\,^{\circ}C$ for an interval of -$30\,^{\circ}C$ to $70\,^{\circ}C$.

Figure 2.16: CAD model of the platform's physical design highlighting the additional sensors and their interconnections.

(a) AlphaSense NO2-A43F connected to the gas setup [6] via its dedicated analog front-end (AFE). Design and realization of plexiglass fixture by Matthias Dupuch.
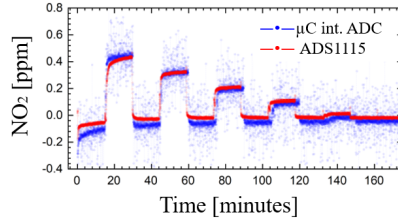
(b) Overlapping measurement profiles of signals acquired with and without the ADS1115 16 *bit* ADC.

Figure 2.17: AlphaSense $NO_2 - A43F$, AFE and NO_2 measurement results with ADS1115 16 *bit* ADC.

2.8.3 NO$_2$ reference sensor

The measurement lab setup presented in [6] currently works as an open-loop system. The analyte concentration of NO_2 is calculated theoretically with the help of mass flow controllers. However, better control of the NO_2 analyte concentration is desired. Co-integration of AlphaSense $NO_2 - A43F$ [176], low-cost, electrochemical [177] reference gas sensor, at the outlet of the platform's test chamber in Figure 2.13, is proposed [178]. This solution can be connected to the embedded platform via its dedicated analog front-end (AFE) [179] presented in Figure 2.17a. The measurement gas setup can become a closed loop with this add-on and the embedded platform. The mass flow controllers can be connected to the RS-232 built-in serial [13] interface, and the pneumatic valves [6] via the RS-485 industrial interface. However, the AlphaSense $NO_2 - A43F$ has a zero-level drift of 0 to 20 *ppb* equivalent per year [176]. In this case, the AlphaSense low-cost sensor can be replaced, or the setup needs to be recalibrated in this configuration.

The sensor development, the gas setup adaptation, its operation, tests, and analysis were conducted in a semester project by Dejan Bozin, mainly supervised by Dr. Kishan Thodkar [180]. One of the conclusions of their project was that the microcontroller ADC offered a limited resolution [181]. Measurements showed that low levels could not have been accurately resolved ($\sigma = 65.4$ *ppb* @ 0.5 *ppm*). Instead, ADS1115 16 *bit* ADC [182], with an integrated programmable gain amplifier (PGA) and I^2C protocol, has been used. The PGA offers up to $\times 8$ gain, amplifying the signal close to the ADC full-scale for the experiments using concentrations up to 500 *ppb* NO_2. In this case, an resolution of 0.0038 *ppb* was achieved. This high precision ADC reduced the standard deviation ($\sigma = 5.3$ *ppb* @ 100 *ppb*). The comparison between the two results is presented in Figure 2.17b.

2.9 Chapter summary

This chapter presented the concept, realization, and performance evaluation of a portable, customizable embedded platform for nanosensor applications. The platform's hardware can adapt to the demands of the nanosensor requirements and is capable of measuring a wide current range. In addition, the solution is fully autonomous and reconfigurable, employing a user-defined instruction set. The FSM's embedded functions allow for setting various platform parameters, namely: the CDC integration time and capacitor bank, defining the FS and BW, DAC bias level/period (including a bipolar potential beyond the supply voltage), and time intervals for SD card storage and BLE data transmission. The peak power consumption of about $225\,mW$ corresponds to the CDC acquisition and SD card data storage. Moreover, an additional power-saving FSM-state deactivates the $\mu C's$ internal blocks and thus reduces the average power consumption to $64.5\,mW$. The power bank, a $5\,V$; $2800\,mAh$ rechargeable battery, can ensure up to nine days of continuous operation for the measurement protocol in this configuration. However, the given values of the average power consumption are determined not considering computing power for further signal evaluation. The presented embedded system has been published in [3] and confirms the preliminary results from [154] by exploring both sensing solutions with repetitive experiments and portable-embedded platforms at a fraction of total power consumption in comparison to lab equipment.

In comparison, a commercial reference platform, e.g., Aeroqual, which uses an SM-50 O_3 measurement unit for outdoor environments, operate at a high minimum power consumption of $2.5\,W$, excluding wireless communication [183]. The Telaire 6713 [184] from Amphenol Advanced Sensors suffers from a similar shortcoming [183]. While the sensor itself is suitable for wearables due to its form factor of $30{\times}15.6\,mm$, its average power consumption of $135\,mW$ without sensor electronics is relatively high for a long-term battery-operated system. A recently published full system solution is the W-Air module presented in [185] at a sampling rate similar to the one presented in this work. The system draws an average power of $150\,mW$, twice the value compared to the average value presented in Figure 2.14. Compared with the start-up solution presented in [147], the proposed embedded system has an average power consumption of 1.75 lower for the equivalent sampling rate and the number of channels. A summary of the embedded system's performance compared to selected gas sensing solutions is presented in Table 2.3. The embedded platform is further connected to the CNT-FET nanosensor and exposed to NO_2 analyte, and results are further presented in chapter 5.

Although the proposed platform is highly suitable for various sensing applications within the context of IoT, the size of the platform and its power

consumption can be further miniaturized and reduced, respectively. The need for an integrated circuit specialized for the CNT-FET nanosensor has emerged for this purpose. The following chapter presents this integrated circuit, i.e., ASIC, and addresses dedicated analog mixed-signal blocks for interfacing the CNT-FET for air-quality monitoring systems.

IDLE power consumption 8.16mW

SD card [157]: 63.2% ∴ 38%
DDC114 [5]: 17.2% ∴ 0%
nRF51 BLE [156]: 13.6% ∴ 61%
ATmega 2560 [13]: 4.17% ∴ 0.1%
MCP4922 [155]: 1.36 ∴ 0.61%
MAX660 [155]: 0.39% ∴ 0%
REF-DDC [167]: 0.39% ∴ 0%

Active power consumption: 316.17 mW
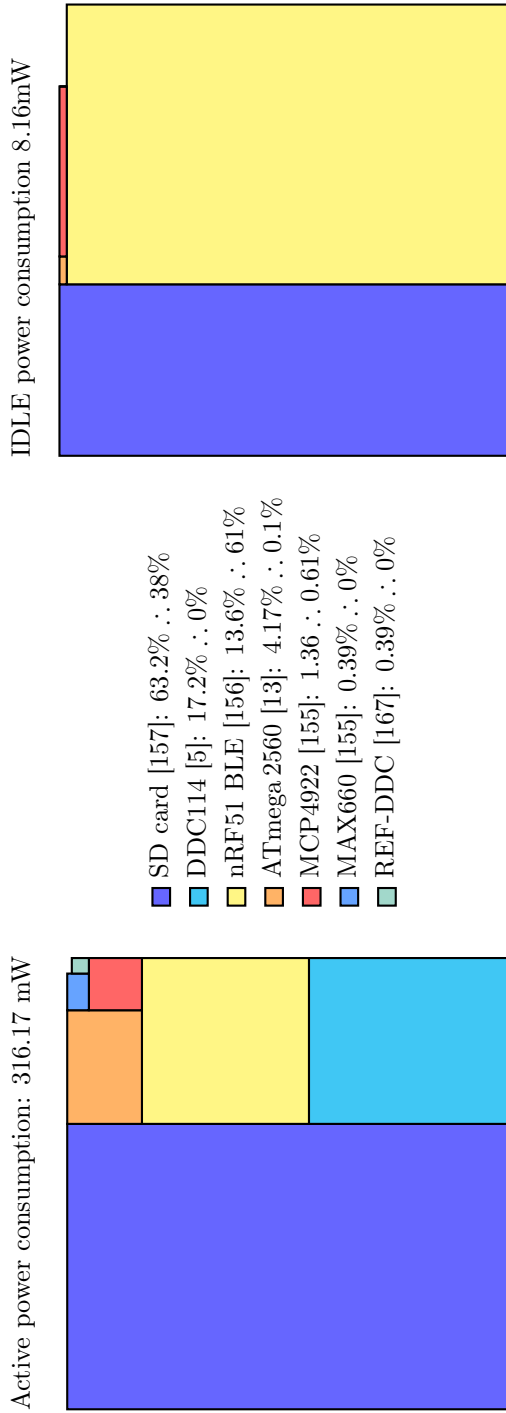
Table 2.2: Theoretical relative power consumption of main components of the embedded platform referred to Active and IDLE (stand-by) states.

Spec./Ref.:	This Work	[183]	[184]	[185]	[186]	[147]
Supply [V]:	5	11	5	3.6	5	3
Connectivity:	BLE/serial	I2C/serial	I2C/UART	BLE	BLE	BLE/USB
Detector interface:	CNT-FET	electrochem.	IR	MOx	electrochem.	CNT
Channels:	4	1	1	2	2	64
Area $[cm^2]$:	9.5×6.5	6×7.5	0.3×1.5	-	-	16.6×6.4
Power $[mW]$:	60 avg. @ 3 Sps	2500-6000	2000	avg. 125	avg. 180	280 @ 0.5 Sps start-up
Purpose:	research	commercial	commercial	research	research	research

Table 2.3: Embedded Platform Performance Summary and Comparison

3 Dynamic Signal Acquisition ASIC

Due to low-cost production, miniaturization, and integration capabilities embodying a high commercialization potential, co-integration of CMOS with other technologies [187][188] is commonly used nowadays. The system can accommodate sensing elements with readout electronics and sensor signal processing, e.g., amplification, filtering, or digital signal processing. Few such examples of highly integrated circuits are given as capable of interfacing nanomaterials when used as sensing elements [189][190][191]. Moreover, as presented in chapter 1.2.1.2 MOS integrated chemical sensors are real candidates for IoT sensing applications [61][56].

This chapter presents the concept, circuit design, and physical design of a front-end integrated circuit (IC) for the CNT-FET nanosensor. It starts with a bias block for the CNT-FET followed by a signal path composed of a transimpedance amplifier (TIA) and successive approximation register (SAR) analog to digital converter (ADC). The circuit analysis, dimension, sizing, and the physical design matching techniques for transistors, capacitors, and resistors are performed by the help of an electronic design automation (EDA) tool, i.e., Cadence. The chapter continues with a comprehensive characterization of the applcation specific IC (ASIC), presenting measurement results for individual blocks. Consequently, system acquisition errors, noise, and power consumption are measured and put into perspective with the CNT-FET nanosensor. Part of this chapter, i.e., the TIA, has been published in [192], and the entire system is currently under revision. At the end of the chapter, the performance of this design is summarized and compared to the SoA of signal acquisition ICs for gas sensors.

3.1 General design considerations

In this research, the primary motivation is to develop a readout integrated circuit independent of the evolution of the CNT-FET fabrication process. Consequently, both the fabrication process and circuit design can be par-

allelized, which leads to performance improvement of the overall sensing system. Hence, this thesis implements a hybrid solution, which employs separate dies for the CNT-FET nanosensor and the CMOS integrated circuit. Since the CNT-FET fabrication process is in development [83], the same CMOS ASIC can be reused for new devices arriving from the cleanroom. However, external interconnections have to be driven by the ASIC, which represents capacitive loads with parasitics. This hybrid architecture introduces a power consumption penalty and causes signal integrity degradation by additional noise. Moreover, the hybrid solution is more expensive than a single-chip implementation, making sense only in early development phases or when commercialized in low volumes. When considering high volumes, the monolithic approach is more suitable. The drawback here is that a fault in the CNT-FET nanosensor will fail the entire chip, even though the CMOS part is working correctly.

3.2 Proposed IC front-end architecture

One way to interface a resistive nanosensor is to inject a current as a stimulus (current-biased) and measure the resulting voltage using a readout circuit. Due to the wide dynamic range of the resistance, it is difficult to directly perform the resistance to voltage conversion using a fixed bias current while ensuring sufficient linearity under a reasonable voltage headroom. Furthermore, in the case of the CNT-FET nanosensor used as NO_2 gas transducer, the resistance to voltage conversion has additional implications. First, the sensor parameters such as sensor baseline and LOD are highly voltage bias dependent. Hence, the resulting output voltage changes the CNT-FET nanosensor sensitivity with the gas concentration when injecting a current, making it impractical for precise sensing applications. Second, a bias current leads to the build-up of a voltage, which might exceed the allowed electric fields at the CNT-FET terminals for a particular NO_2 gas concentration [6]. Such a fixed current conversion architecture was proposed in [149], wherein the CNT-FET nanosensor is considered analyte dependent only. The latter simplification leads to additional complexity when finding the transfer characteristic of the sensor. Complementary to [149], this thesis proposes the alternative approach: applying a known voltage (voltage-biased) and measuring the resulting current, which carries the information related to NO_2 concentration.

The overall circuit block diagram can be seen in Figure 3.1, and presents: a) the CNT-FET nanosensor on a different substrate, b) analog and digital input/output signals, c) a 6 *bit* DAC, d) a regulated voltage bias, e) an adjustable current mirror, f) a transimpedance amplifier with a single-ended

to differential signal conversion, and g) a 9-bit SAR ADC. As shown in Figure 3.1, the CNT-FET nanosensor is biased by the VDS_{CNT} voltage and the VGS_{CNT} voltage. The resulted ID_{CNT} current, taken as sensor signal response, is further processed by the analog-mixed signal circuits. The proposed sensing circuit uses a static voltage bias, here denoted as VDS_{CNT}, which determines the CNT-FET nanosensor characteristics. In Figure 3.1.a, it can be seen that the architecture interfaces the CNT-FET nanosensor with a single pin, which is useful when interfacing nanosensor arrays with time multiplexing. For the current implemented system the VGS_{CNT} potential is externally. The ASIC concept includes, however, an integrated charge-pump block which will be further presented in section 3.6.1 of this chapter.
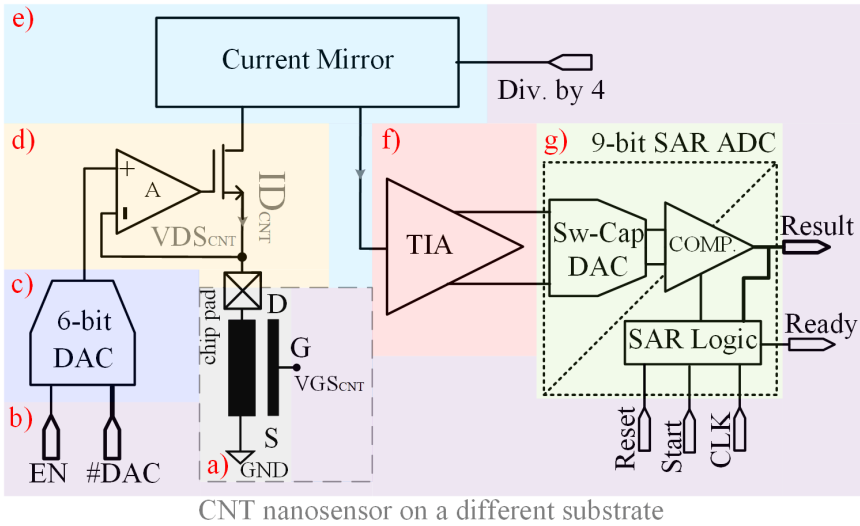
Figure 3.1: Block schematic of the proposed architecture composed by: a) CNT-FET nanosensor; b) input/output signals; c) 6 bit DAC; d) a regulated voltage bias; e) current mirror; f) transimpedance amplifier; g) 9 bit SAR ADC.

3.3 Drain bias for CNT-FET nanosensor

The proposed bias block is presented in Figure 3.2 and uses a static voltage bias, denoted as VDS_{CNT}, which determines the CNT-FET nanosensor characteristics. This voltage has to be adjustable to define the baseline, slope, noise, and limit of detection for the CNT-FET nanosensor as presented in [4]. Moreover, to ensure sufficient self-heating effect to the CNT-FET nanosensor to reset [79], elevated drain voltages VDS_{CNT}, i.e., above $1.3\,V$, are

required. Hence, a relatively high $1.8\,V$ supply was adopted despite its power penalty.
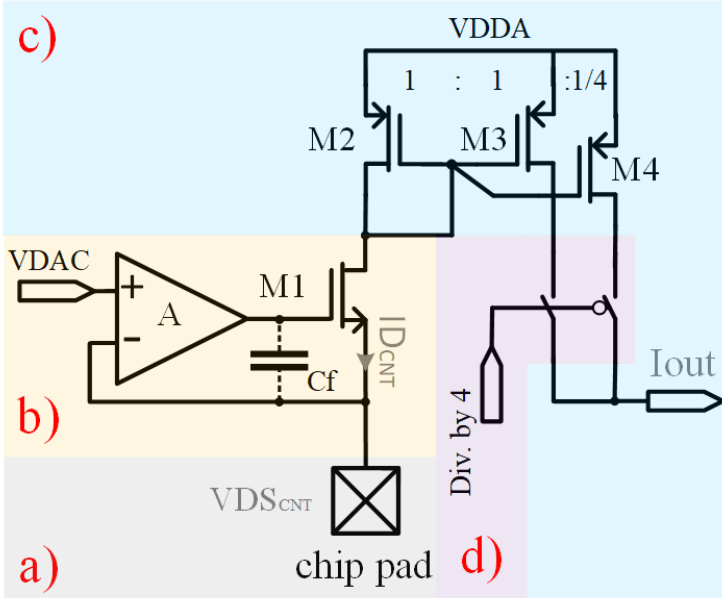
Figure 3.2: Current mirror of the proposed architecture composed by: a) chip pad; b) voltage regulator; c) current mirror; d) div. by 4 control signal.

3.3.1 Voltage regulator and current mirror

In this particular application, the regulated voltage, VDS_{CNT}, needs to be kept constant despite a wide variation of the sensor resistance. The block, shown in Figure 3.2.b, set the sensor's VDS_{CNT} bias voltage connected from the chip pad towards GND. The resulting current ID_{CNT} is processed by the current mirror (Figure 3.2.c) implemented with M2-M3 with an optional division by four via M4 (Figure 3.2.c), which might be used for elevated VDS_{CNT}-levels, i.e. when the CNT-FET self-heating current needs to be monitored [79].

A voltage regulator with a low input impedance of $1/(gm_1 \cdot A)$ is proposed, where gm_1 is the M1 transistor's small-signal transconductance (derivation can be found in Eq. A.3.1). A relatively narrow bandwidth design for the voltage regulator is desired due to the significant time constants of the mo-

lecule kinetics of gas molecules [193], which are responsible for the CNT-FET nanosensor's slow time response. Cadence simulation shows that a bias current of $50\,nA$ is sufficient for achieving $230\,Hz$ bandwidth and a gain of about $A = 50\,dB$ with a simple one-stage OTA. In addition, a capacitor C_f can be externally added to maintain circuit stability. Moreover, a limited GBW is desired for open-air field CNT-FET nanosensor applications, where EMI could be injected into the stand-alone chip pad and further propagates as an undesirable high-frequency component of I_{OUT} [194]. The ASIC external pin, where the CNT-FET is connected, can be affected by induced EMI perturbations on higher frequencies but still in the TIA bandwidth. The transfer function of an AC coupled V_{emi} perturbation is calculated in [194] and presents a gain peak towards high frequencies due to the complex poles in the denominator. The unfavorable effect of this structure can be mitigated by lowering the OP-amp gain-bandwidth product (GBW) [194]. Furthermore, the feedback amplifier serves as a voltage buffer for the resistive DAC, presented next.

3.3.2 Matrix resistive DAC

The system is designed such that the VDS_{CNT} can be programmable by a $6\,bit$ DAC. The DAC LSB step is designed to be $28\,mV$, found in [3] to be sufficient when choosing the CNT-FET bias point. Due to the slow time response of the CNT-FET nanosensor, this voltage has to be stable for a predefined period in the range of minutes [79]. Because of the time constants, it is advantageous to use a resistive DAC compared to a capacitive one due to the dominating leakage currents of the latter. The matrix DAC [195] is presented in Figure 3.3 and implemented here as a voltage divider and composed by:

    a) **Logic decoder**: a 2-dimensional row-column decoding architecture is used here to reduce the parasitic capacitance, C_{par}, by reducing the number of switches required to change the DAC resistance linearly [196]. In addition, CMOS switches to access the output of the resistive divider have been designed.

    b) **Resistive divider**: a 64 unit poly-resistors R of $0.5\,\mu m \times 221\,\mu m$ each, giving a total value of $64 \cdot R = 32.1\,M\Omega$, was chosen for implementing the voltage divider [197]. This relatively high total value is desired for reduced power consumption yet still provides sufficient linearity despite its small finger aspect ratio and sub-second settling time despite high RC_{par} time constants.

As shown in Figure 3.3.a, a power gating switch, EN, is added to the duty

cycle of the DAC to save power consumption of both the IC and the CNT-FET nanosensor. As a result, the system's high energy efficiency can be maintained at sampling rates below $1\,Sps$.
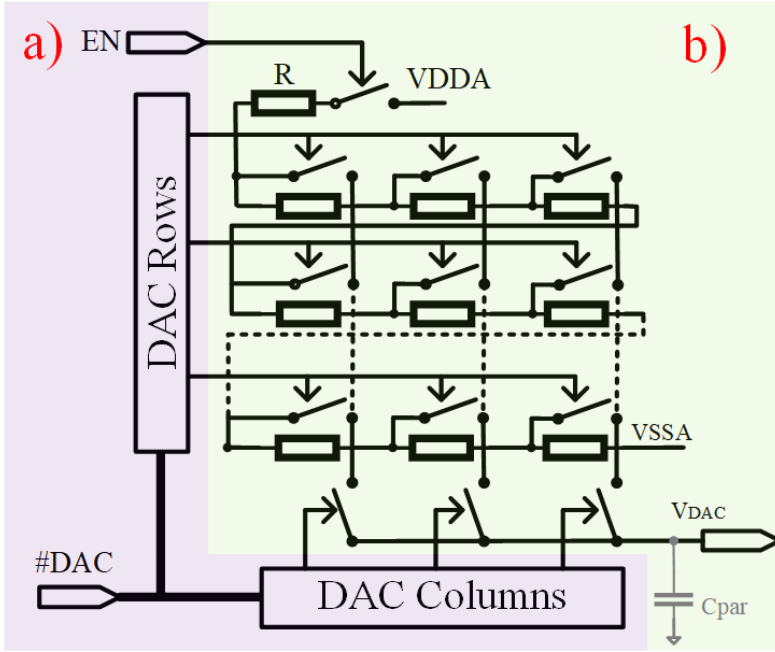
Figure 3.3: Block schematic of the resistive DAC composed by: a) logic decoder; b) resistive divider and analog switches.

Since this resistive DAC is used for programming the CNT-FET nanosensor bias, it operates as a low-frequency signal source. In such applications, the two most essential characteristics are:

- **Power consumption** of the designed DAC is 101 nW and the feedback op-amp consumes $90\,nW$.

- **Linearity** is the ability of a DAC to drive the output voltage, V_{DAC}, in the same direction that the digital input stirs. With the op-amp biased in weak inversion, the VDS_{CNT} output achieves this at the end of the conversion time event.

Measuement result of the standalone 6 bit resistive DAC's static performance is presented in Figure 3.4.

a)

b)
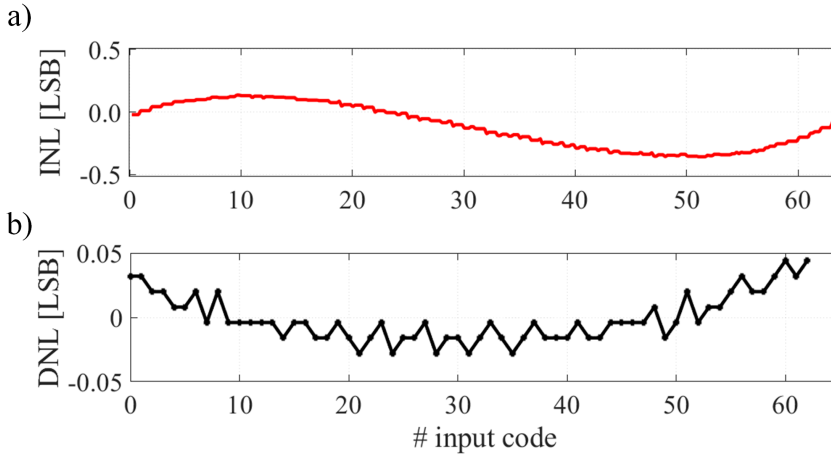
Figure 3.4: Resisitive DAC measured static performance: a) integral nonlinearity (INL); b) differential nonlinearity (DNL). DUT: ASIC V3 presented in Appendix A.6.

The integral nonlinearity (INL) is the largest difference between the real and ideal finite resolution characteristics measured in $LSBs$ [198]. The DNL Differential Nonlinearity (DNL) measures the separation between adjacent levels measured at each vertical jump in LSB [198]. It can be seen in Figure 3.4 that the VDS_{CNT} output reaches a value within $\pm 0.5\,LSB$ for both INL and DNL static performance parameters.

3.4 CNT-FET nanosensor signal-path

3.4.1 Transimpedance amplifier

The concept of a transimpedance amplifier (TIA) is as old as the feedback theory and its 16 possible configurations introduced in the late 60s [199]. The TIA is one of these configurations that utilize negative feedback to create a low input impedance suitable for processing currents, therefore acting as a current-to-voltage converter with the help of a gain resistor [199]. Since 1967, when Miller patented two TIAs for converting a photodiode's current to a differential output voltage [200], the TIA has received broad attention even today in different domains, i.e., RF receivers [201] [202], optical receivers [203][204][205], photonics [206], and biological [207][208] sensing. Such a

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broad spectrum of applications makes the TIA "a circuit for all seasons" [209].

This chapter proposes a single-stage bidirectional input TIA, presented in Figure 3.5, with current dynamic bias and differential output. Implemented as a nested structure with reduced voltage headroom, the TIA allows high reuse of passive and active devices while enabling dedicated positive and negative feedback loops for the common mode and differential paths. In addition, it implements a bi-quadratic cell that behaves as a low-pass filter. The following paragraphs present the TIA small-signal and large-signal operation, frequency behavior, noise, distortion performance, and design imperfections, i.e., offset, mismatch, and PVT variations.
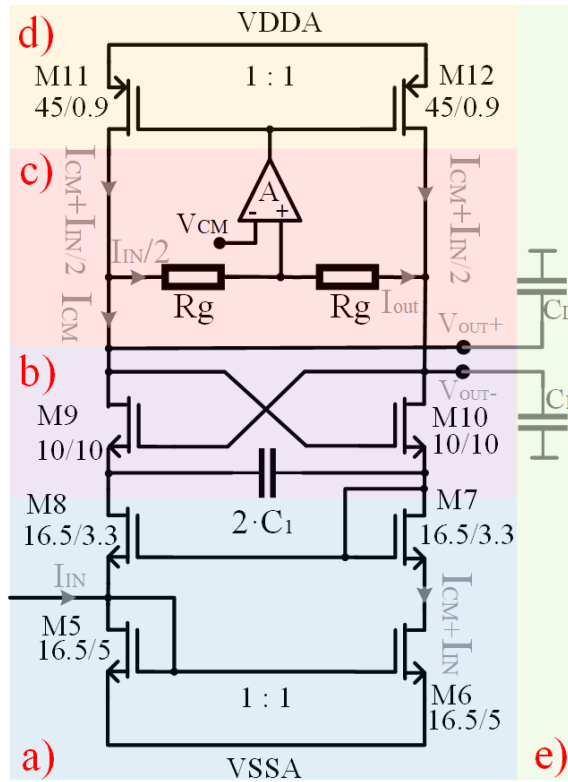
Figure 3.5: Schematic of the TIA composed by: a) cascode current mirror; b) cross-coupling structure and frequency compensation capacitor; c) gain stage and common feedback; d) adaptive bias implemented by voltage-controlled current sources; e) capacitive load.

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3.4.1.1 Operation principle

The operation principle of the TIA can be explained intuitively by identifying its branch currents and their relationship at the input and output nodes, as Figure 3.6 presents in three cases for a) $I_{IN} > 0$, b) $I_{IN} < 0$, and c) $I_{IN} = 0$. A variable input current, $I_{IN}(t)$, changes the current values through the TIA branches as simulation results presented in Figure 3.7. It can be observed that the currents follow their interdependence from Figure 3.6. Moreover, when $I_{IN} >> 0$ or $I_{IN} << 0$, the currents are substantially higher than the static value, noted as I_{CM} in Figure 3.6.c, constructing a dynamic operation point of the transistors. This operation is not typical for a classical amplifier [198], where the static currents are fixed with respect to the signal value.
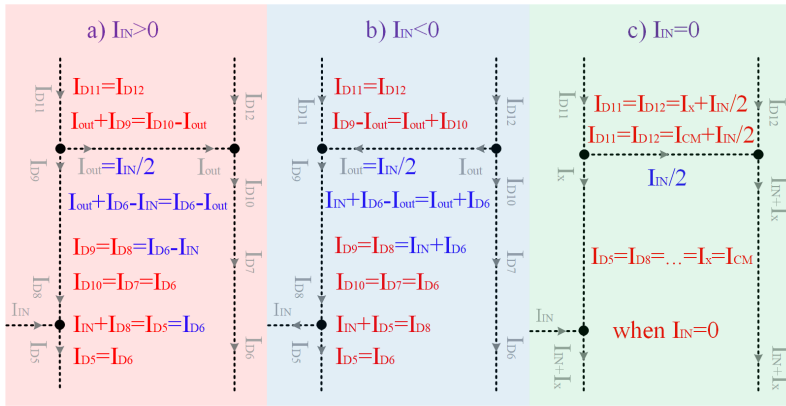
Figure 3.6: TIA currents relationship at input and output nodes for: a) $I_{IN} > 0$, b) $I_{IN} < 0$, and c) $I_{IN} = 0$.
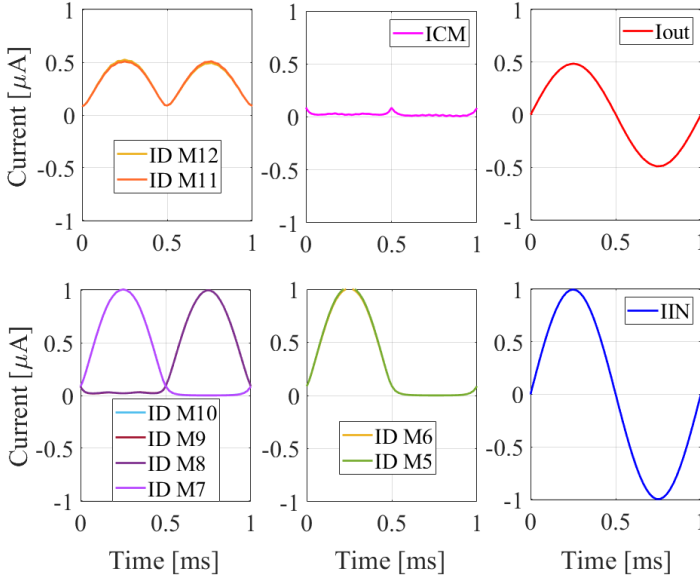
Figure 3.7: TIA simulation of a dynamic input current, $I_{IN}(t)$, and the resulted currents of the TIA internal structure.

Since I_{IN} changes its sign and amplitude value, the transistor's working regime changes too through all operation regions, i.e., cut-off, triode, saturation, sub-threshold [210] as simulation results shown in Figure 3.8. Although the input current significantly influences the operating point of TIA, the TIA_{gain} holds its value as long as the current passing the $2 \cdot Rg$ resistor equals $I_{IN}/2$, i.e., when M5-M6 work as a current mirror, M11-M12 as controlled current sources, and the TIA load is balanced. It can be remarked that the TIA gain value is independent of the operating point of its transistors, which is uncommon for the most active circuits. In this case, the small-signal approximation of the MOS drain current, $id = gm \cdot vgs$, holds for a minimal change interval of the $I_D(V_{GS})$ function, i.e., a linear, quadratic, or exponential dependency. Consequently, for the following paragraphs, the transistor's transconductance will be denoted as Gm to highlight its dependency given by its operation region determined by the I_{IN} value.

3.4.1.2 Small-signal towards the large-signal operation

The single-stage TIA with only two current branches, a single input, and differential output is presented in Figure 3.5 including its capacitive load.
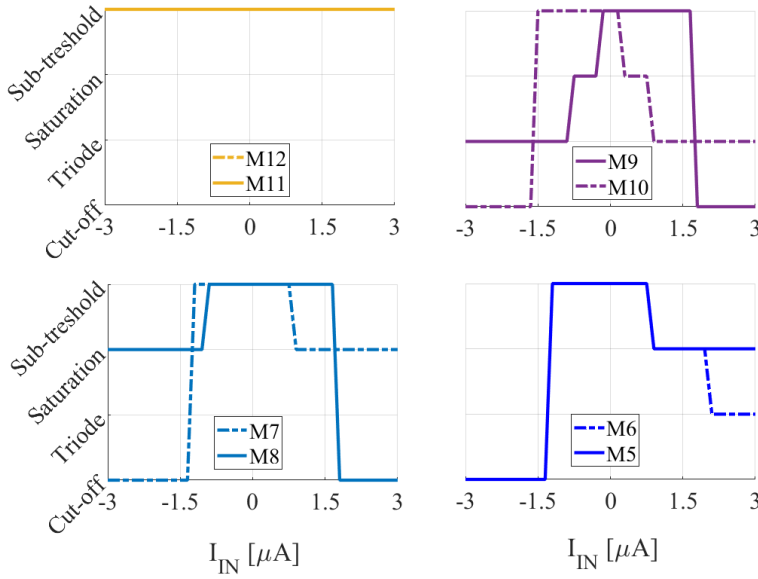
Figure 3.8: TIA transistor's simulated discrete operation regions as a function of I_{IN} input current sign and value.

The next paragraphs describe the TIA building components and their functionality starting from small I_{IN} level, to moderate and large signal lelvel.

a) **Input current mirror** is formed by nMOS transistors M5-M6 as shown in Figure 3.5.a. This structure implements two functions:

– **An impedance adaptation**, as being the first stage of the TIA, it provides low input impedance $Z_{IN} \approx 1/Gm_5$ [210]. In addition, the drains of M7-M8 provide high output impedance $Z_{M7;M8} \approx 1/Gds_{7;8}$ [210], for the upper stage, i.e., the cross-coupling structure.

– **A current imbalance on the branches** when a current $I_{IN} \neq 0$ is present at the TIA input, it is summed up with I_{CM} by the diode-connected M5 and copied over to I_{D6}. Whereas, when $I_{IN} = 0$, the M5-M6 forces current, I_{CM}, equal on both TIA branches.

b) **Cross-coupling structure** which is presented as "a circuit for all seasons" in [211] [212] [213]. Shown in Figure 3.5.b it represents the core of the TIA, and implements three functions:

- **High output differential impedance** [214][215] which comes in parallel with the resistors, R_g, and set the TIA transimpedance gain. Its value, $Z_{outDiff} \approx 1/Gds_9 + 1/Gds_{10}$, which comes in parallel with the resistors R_g that sets the TIA transimpedance gain.

- **Bi-quad filter core** [216][217] is realized by the cross-coupling structure and capacitor $2 \cdot C_1$, which can suppress the intrinsic noise by an in-band zero introduced in the noise transfer function of the TIA. This feature is further presented in section 3.4.1.3.

c) **Resistors and feedback op-amp** is presented in Figure 3.5.c, and implements two functions:

  - **The transimpedance gain** as a consequence of $I_{IN} \neq 0$ the branch currents, I_{D7}; I_{D8}, variate in the range of $[I_{CM},\ I_{CM} +I_{IN}]$ and $[\ I_{CM} +I_{IN},\ I_{CM}]$ respectively. The difference of $I_{IN}/2$ flows through the two resistors, R_g, defining the transimpedance of the $TIA_{gain} = (V_{OUT+} - V_{OUT-})/I_{IN} = R_g$. For this design the value of $2 \cdot R_g = 973\,k\Omega$ has been chosen, value which is limited by the output voltage swing.

  - **Common-mode output level** by the identical resistors are used to consciously sample the output nodes' midpoint level, which is regulated to the common-mode output voltage as further detailed.

d) **Voltage controlled current sources**, composed by p-MOS transistors M11-M12 as presented in Figure 3.5.d, are driven by a single-stage op-amp implementing two functions:

  - **Common-mode (CM) feedback loop** is formed by the resistors R_g, M11-M12 transistors, and the op-amp, A. The loop regulates the common-mode output voltage to V_{CM}, which is set by an external reference.

  - **CM output impedance** implemented by the help of the same feedback loop is low, i.e., $Z_{outCM} \approx 1/\left[A \cdot (Gds_9 + Gds_{10})\right]$.

3.4.1.3 Frequency behaviour

For low input current levels, $I_{IN} = \pm 200\,nA$, the transconductances of M9 and M10 have been designed to be symmetric, i.e., $Gm_9 \approx Gm_{10}$ and $(Gm_9 + Gm_{10})/2 = Gm \approx 1/R_g$ as presented in Figure 3.9. The signal propagation path from the single-ended input to the differential output must be determined to evaluate the TIA frequency behavior. Due to many feedback loops inside the TIA structure, this signal transfer function is not trivial to derive and cannot be calculated easily by hand. For low I_{IN} current levels, the TIA can be split in half and is presented in Figure 3.10 thanks to its symmetric structure. The pair M9-M10 from Figure 3.5.b has been replaced by a sign inverter, -1, at the gate of M10. For analyzing this structure further, a linear signal-flow graph [218] as illustrated in Figure 3.10.f is used. This shows the high number of feedback loops and highlights the complexity of the TIA structure even when split in half.
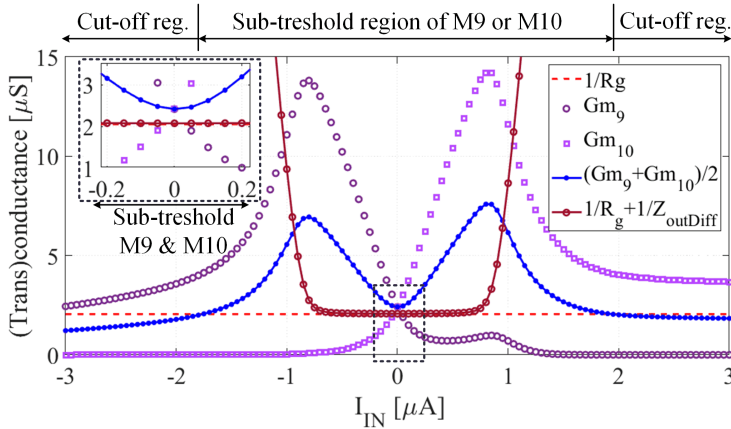
Figure 3.9: Simulation plots of the Gm_9, Gm_{10} transconductances as a function of input current. Matching of Gm with $1/R_g$ at low input levels.

Here the branches represent the signal through the circuit, and the arrows represent the driving strength impedance of each node. In addition, the noise sources and their propagation paths toward output are added and further analyzed. Using Mason's gain rule formula [218][219], the transfer functions are calculated in MATLAB with the help of the function $Mason.m$ available on [220]. Consequently, the transimpedance gain can be calculated as:

$$H_{TIA}(s) = \frac{R_g}{s^2 C_1 C_L R_g / Gm + s(C_L R_g - C_1 R_g + C_1/Gm) + 1}, \qquad (3.1)$$

where C_1 is the single-ended capacitance at the source of M9, M10 and C_L represents the TIA output load to the ground, i.e., the sampling capacitors of the SAR ADC modeled as in Figure 3.10.e. The relatively small output transconductance of the transistor, Gds, is also neglected here for simplifying the mathematical expressions. Equation 3.1 shows a second-order low-pass characteristic with an in-band transimpedance of R_g. The frequency of the two poles can be calculated as follows:

$$\omega_{p1;p2} = \frac{\frac{C_L}{C_1}R_gGm + 1 - R_gGm}{-2C_LR_g} \cdot$$

$$\cdot \left(1 \pm \sqrt{1 - \frac{4\frac{C_L}{C_1}R_gGm}{\left[\frac{C_L}{C_1}R_gGm + 1 - R_gGm\right]^2}}\right) \quad (3.2)$$
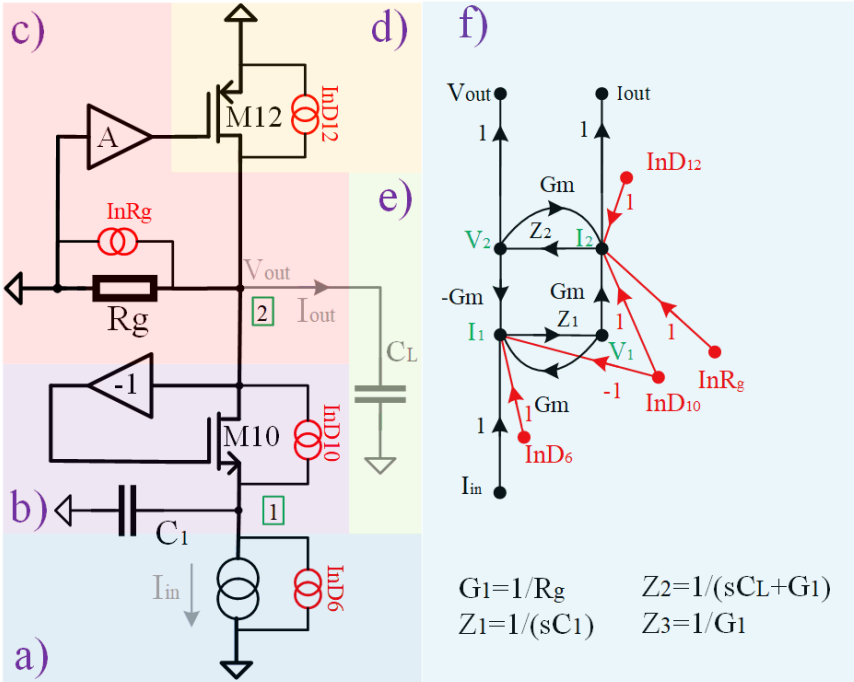
Figure 3.10: Schematic of the half-TIA composed by: a) input current mirror noise; b) noise of the half cross-coupling structure; c) gain resistor noise; d) adaptive bias current sources noise; e) capacitive load modelling the next stage. f) SFG including noise sources.

The parasitic poles and zeros given by transistors C_{gs} can be neglected at this point. It is possible to do so since the large value of C_L, and C_1 set the dominant poles. The Gm value in the transfer function suggests an obvious input signal dependency of the two poles $\omega_{p1}; \omega_{p2}$. While one of the two M9-M10 transistors operates in weak-inversion (i.e. subthreshold region presented in Figure3.8), then the value of $Gm \cong I_D/(nU_T)$ is a direct function of I_{IN}. Here the term n is the subthreshold factor, and U_T represents the thermal voltage. At low current input levels, when, $Gm \approx 1/R_g$, and with the TIA capacitive load matched, i.e., $C_L = C_1$ (shown in Figure 3.5.d-e), the two filter poles from Eq. 3.2 becomes complex conjugates with the value of $\omega_{p1}; \omega_{p2} = -1/(2R_gC_L)\cdot(1 \pm j\sqrt{3})$. This way, second-order filtering with maximized bandwidth can be achieved where it is essential, i.e., at low input signal levels. Bode plots presented in Figure 3.11.a show the TIA transfer function behavior at low input signal levels. It can be observed a second-order in-band transfer function that remains almost unchanged, with a slightly increased cut-off frequency. In early filter synthesis attempts, [221], minimizing the number of active devices was a typical constraint challenge. This architecture creates a bi-quadratic filter with the fewest active and passive components possible, thanks to multiple feedback loops, which create conjugated poles.

The TIA frequency response is presented in Figure 3.11.b for high current levels. It can be observed that the frequency of two poles, $\omega_{p1}; \omega_{p2}$, has changed now since the approximation $Gm \approx 1/Rg$ doesn't hold anymore. However, the TIA gain value remains unchanged within $1\,dB\,\Omega$ flatness for I_{IN} currents of $\pm1.8\,\mu A$.

3.4.1.4 Noise

The use of the cross-coupled structure implements noise reduction for the internal TIA transistors at low input current levels, i.e., where M9 and M10 transistors work simultaneously in weak inversion (denoted as the subthreshold discrete region in Figure 3.8), at high gm/I_D values. This method has been introduced in [222] called "pipe filter" and is also valid for the internal noise sources of the TIA. Conceptually a high impedance presented to a current source can create an in-band degeneration of the transistor's transconductance that forces the noise to recirculate, creating noise suppression. This effect, in turn, reduces the thermal noise and increases the linearity [192]. Noise simulations results with and without the cross-coupled structure are presented in Figure 3.12.

Each transistor and the R_g resistors inject a different amount of noise into various points of the TIA structure, which propagates through different paths

a)

b)
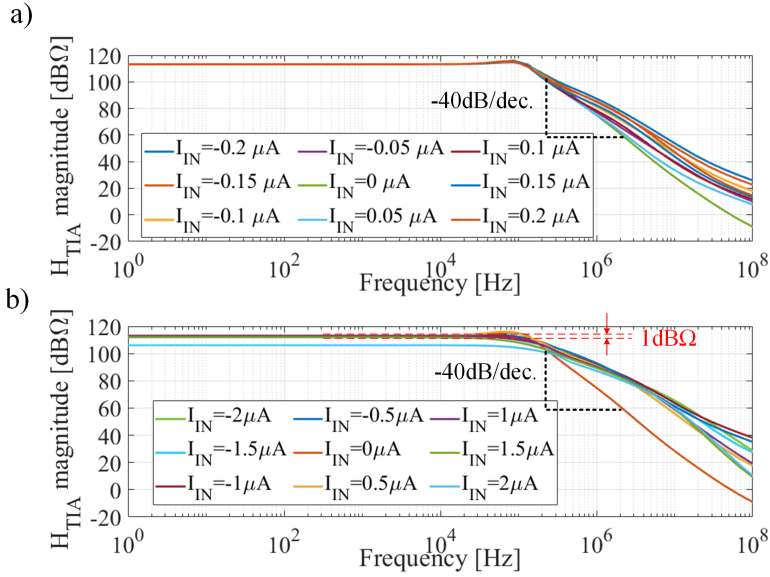
Figure 3.11: Bode plots of TIA transfer function for: a) small I_{IN} current levels span where $Gm \approx 1/R_g$, and b) large I_{IN} current levels where $Gm \neq 1/R_g$ and $C_1 = C_L = 2\,pF$ for both cases.
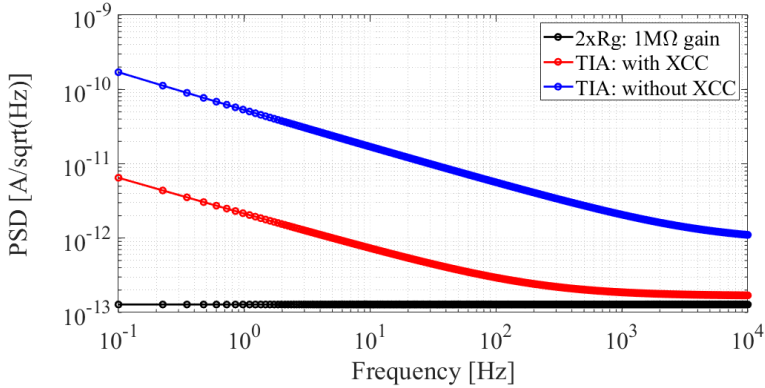
Figure 3.12: PSD simulation results of the TIA with and without the cross-coupled structure (XCC), structure when input left open: $I_{IN} = I_{offset}$.

toward its outputs. This makes a theoretical noise analysis of the TIA very difficult. Moreover, the CMFB regulation loop of the TIA creates CM noise besides the channel noise of M11 and M12. In the case of a perfect symmetric load, the CM noise will not be seen at the TIA output. Hence, for DM

analysis, the CM noise can be neglected. Using the SFG from Figure 3.10.f (expression derived in Eq. A.3.2.3), and assuming only white noise sources, the channel noise of M12 together with the noise of R_g remains, as in:

$$N_{InM12,InRg} = \frac{R_g\left(1 + sC_1/Gm\right)}{s^2 C_1 C_L R_g/Gm + s(C_L R_g - C_1 R_g + C_1/Gm) + 1} \quad (3.3)$$

Further, the channel noise of M10 can be calculated, as in:

$$N_{InM10} = \frac{sR_g C_1/Gm}{s^2 C_1 C_L R_g/Gm + s(C_L R_g - C_1 R_g + C_1/Gm) + 1} \quad (3.4)$$

This noise transfer function of Eq. 3.3 is flat in the pass-band whereas Eq. 3.4 shows band-pass characteristics. The noise associated with M5-M6 is injected at the input and thus is processed by the transfer function of Eq. 3.1. Bode plots presented in Figure 3.13 shows the TIA transfer function behaviour for I_{IN} currents of $\pm 0.2\,\mu A$.
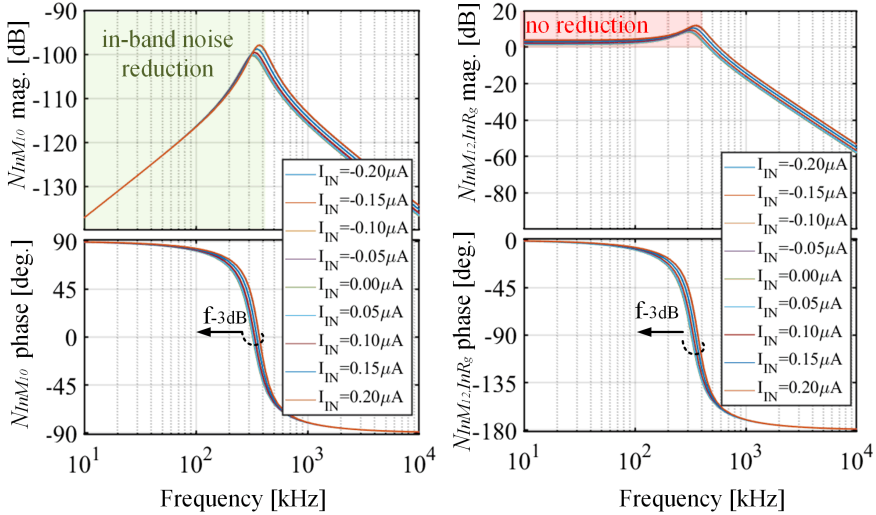
Figure 3.13: Normalised Bode plots for transistor and resistor thermal noise injection when $C_1 = C_L = 2pF$.

The signal and noise characteristics of the TIA have been measured and qualitatively compared with the theoretical calculations as shown in Figure 3.14. The measured BW of $10\,kHz$ is obtained when its output was connected to $10\,M\Omega\,\|26\,pF$ load, representing the input impedance of the oscilloscope. Due to this external load, the frequency of the two poles expressed in Eq. 3.2 are located at $\omega_1 = 8\,kHz$ and $\omega_2 = 60\,kHz$ in Figure 3.14. In the context of the CNT-FET nanosensor application, external capacitors can be added for

setting the TIA bandwidth of interest when connecting it to the next stage, i.e., the ADC, to prevent aliasing effects [223].

Figure 3.14 shows the shape of the output noise spectrum. At low frequencies, the main noise contributors are the channel noise of M6-M7, processed as the input signal. Towards high frequencies, the noise of M10 starts to increase first, reaching a maximum close to the amplifier's second pole, and then decreases because of the capacitor, C_L, which filters not only the signal but also the noise injected by M10. This behavior of the filter is explained by the presence of a zero in origin as the transfer function in Eq. 3.4 suggests. This produces a passband characteristic for the noise of M10 rather than a low-pass characteristic as for the signal and CM noise sources.
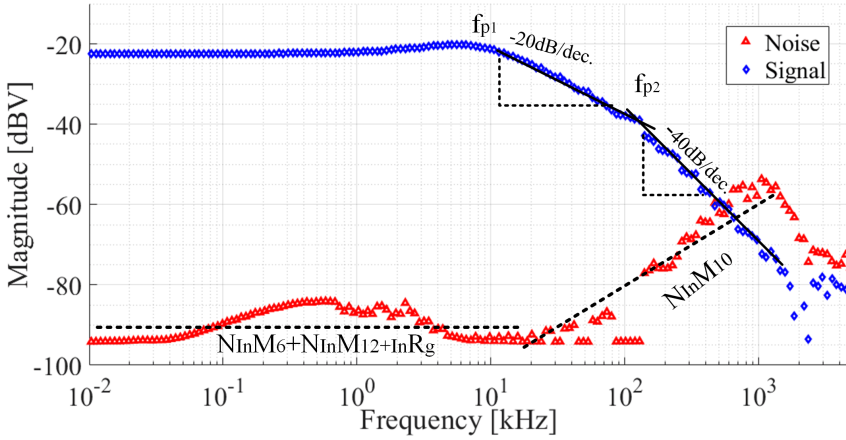
Figure 3.14: The signal and noise characteristics of the TIA when $C_L = 26\,pF$, and $C_1 = 2\,pF$. DUT: ASIC V3 presented in Appendix A.6.

3.4.1.5 Distortions

Any frequency component added by an active circuit at its output distinctive form its input, can be called a distortion of the signal. From the schematic of the TIA presented in Figure 3.5, the single-ended output voltage of the amplifier can be expressed as:

$$V_{CM} + \frac{VOUT_+}{2} = VGS_{10} + VGS_8 + VGS_5, \tag{3.5}$$

where $VGS_X \overset{w.i.}{=} (nkT/q)ln\left[(ID_X L_X)/I_m W_X\right] + VTH$ when M10, M8 and M5 operate in weak inversion (see Figure3.8). Hence the Eq. 3.5 can be

rewritten as:

$$V_{CM} + \frac{VOUT_{diff}}{2} = 2a \cdot ln\left(1 + \frac{I_{IN}}{I_{CM}}\right) + 2a \cdot ln\left(I_{CM}\right) + a \cdot ln(b) + c, \quad (3.6)$$

where, $a = (nkT)/q$, $b = ln\left[(L_{10}L_8L_5)/(I_mW_{10}W_8W_5)\right]$, and $c = 3VTH$. By the help of Volterra series [224], the distortions of the TIA (derivation in Appendix A.3.2.4) can be expressed in therms of second harmonic distortion (HD_2), and third harmonic distortion (HD_3) as:

$$HD_2 = \frac{1}{4} \cdot \frac{I_{in}}{\left(2 + \frac{I_{in}/2}{I_{CM}}\right)} \quad (3.7)$$

and

$$HD_3 = \frac{1}{12} \cdot \frac{I_{in}^2}{\left(2 + \frac{I_{in}/2}{I_{CM}}\right)^2} \quad (3.8)$$

The TIA's distortions were explored by determining its spurious-free dynamic range (SFDR). The SFDR performance metric represents the RMS signal component amplitude ratio to the RMS value of the worst spurious signal in the spectrum. In the case of the TIA, the worst spur is a harmonic of the input signal. Measurement results at different I_{in} input current levels are presented in Figure 3.15. The harmonic HD_2 and HD_3 together with total harmonic distortion THD have been evaluated over the band of the TIA at a constant input current value, and the results have been presented in Figure 3.16.

3.4.1.6 SNR and PSD

With the input not driven, the TIA noise power spectral density (PSD) at low frequencies can be calculated by evaluating the thermal noise of the resistor R_g and the noise contribution of the MOS transistors M6, M10, and M12 (full expression derived in Appendix A.27). The resulting PSD for one branch is then multiplied by a factor of two due to its symmetric structure:

$$S_{Nin^2} = 2\frac{\left\{\left[Gm^2 + \omega^2C_1^2\right] \cdot 4q\left[\frac{U_T}{Rg} + \frac{\gamma_{nD}}{m}\left(2I_{CM} + 3/2I_{IN}\right)\right]\right\}}{\left(Gm + \omega^2C_1C_LRg\right)^2 + \omega^2\left[GmRg\left(C_1 - C_L\right) + C_1\right]^2} \propto I_{IN} \quad (3.9)$$

In which q is the electron charge, $\gamma_{nD-W.I.} = n/2$ is the noise parameter, and the $m = 1.2$ is the subthreshold gate coupling coefficient which results
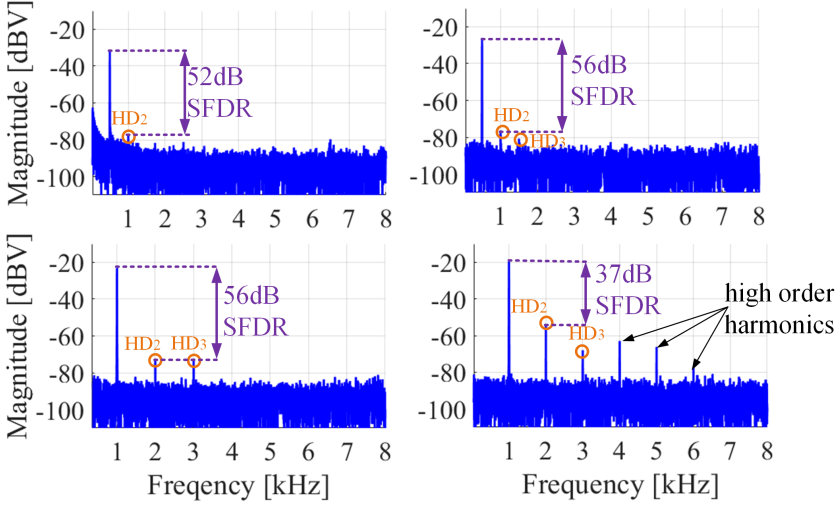
Figure 3.15: Measurement results of the TIA SFDR at different I_{IN} values. Measurement conditions: $C_1 = 2\,pF$, and $C_L = 26\,pF$. DUT: ASIC V3 presented in Appendix A.6.
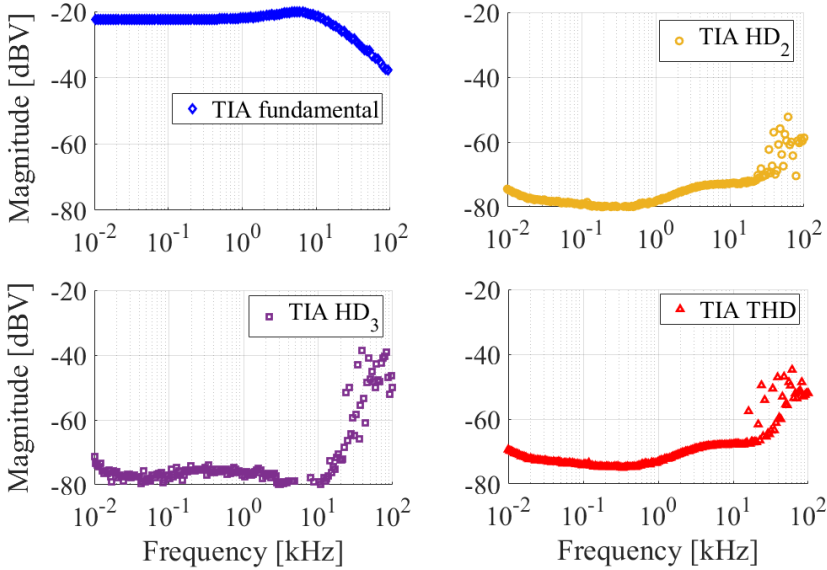
Figure 3.16: TIA measurement results of the fundamental, HD_2, HD_3, and THD values. Measurement conditions $C_1 = 2\,pF$, $C_L = 26\,pF$. DUT: ASIC V3 presented in Appendix A.6.

from the operation in weak inversion [107]. With a simulated bias current of $I_{CM} = 90\,nA$ and $2 \cdot R_g = 974\,k\Omega$, the PSD close to DC frequencies is $S_{Nin^2} \cong 0.7pA/\sqrt{Hz}$, at room temperature. The SNR in the pass-band of the filter can be calculated as follows:

$$SNR = \frac{\left(I_{IN}/\sqrt{2}\right)^2 Gm^2}{2\left\{[Gm^2 + \omega^2 C_1^2] \cdot 4q\left[\frac{U_T}{Rg} + \frac{\gamma_{nD}}{m}\left(2I_{CM} + 3/2I_{IN}\right)\right]\right\}} \quad (3.10)$$

For simplicity, the frequency dependence can be ignored in Eq. 3.10, and the in-band spot SNR with $1\,Hz$ be further calculated as:

$$SNR = \frac{\left(I_{IN}/\sqrt{2}\right)^2}{4q\left[\frac{U_T}{Rg} + \frac{\gamma_{nD}}{m}\left(I_{CM} + 3/2I_{IN}\right)\right] \cdot BW} \quad (3.11)$$

Thus, the SNR increases with I_{IN}^2 at small current values, for in-band signals, when $I_{IN} \ll \frac{2}{3}\left(U_T/R_g + 2I_{CM} \cdot \gamma_{nD}/m\right)$, whereas for values above it increases with I_{IN}. A similar TIA design approach with dynamic bias can be found in [225], where the SNR scales with I_{IN} for limited bandwidth.

Measurements have been performed with the input not driven, and a finite output load, and the TIA achieves a low-frequency noise as low as $0.75\,pA/\sqrt{Hz}$ as Figure 3.17 shows. Compared to the measurement results, the ultra low-frequency noise power ($< 1\,Hz$) becomes higher due to the common-mode noise introduced by VCM external bias source and the $VDDA_{TIA}$ supply.
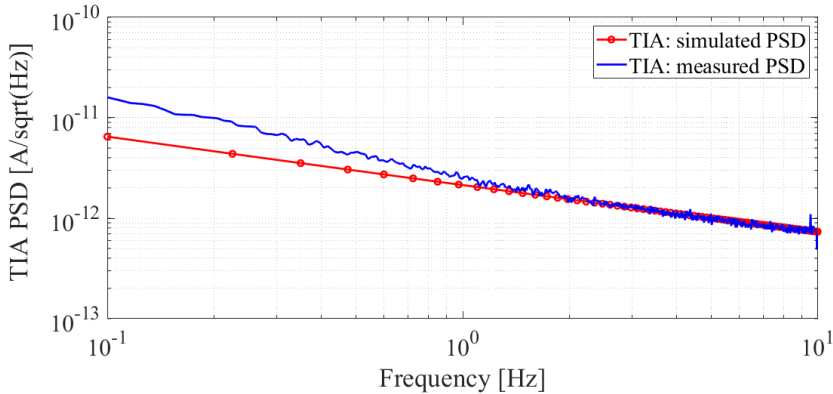
Figure 3.17: Measurement results of the TIA PSD when its input is not driven, i.e., when $I_{IN} = I_{Offset}$. DUT: ASIC V3 presented in Appendix A.6.

3.4.1.7 Mismatch and offset

Mismatch originates in threshold voltage variation due to oxide thickness variation and dopant fluctuations [226]. The relative mismatch of the transistor's oxide thickness and the gate length and width variation is neglected in this thesis. In general, a circuit designer can only use the device dimensions, i.e., area, width, length, the device layout, and the device bias point to control the matching [227][226].

For the proposed TIA, the primary mismatch components are illustrated in Figure 3.18. The current sources M11-M12 and current mirror M5-M6 are experiencing the same overdrive voltage by design. At the low I_{IN} level, the systematic error of the current mirror M5-M6 was minimized by adding M7-M8 as a cascode. One can rewrite (derivation can be found in Appendix Eq. A.3.2.5) the transimpedance gain equation, i.e., $TIA_{gain} = (V_{OUT+} - V_{OUT-})/I_{IN} = R_g$ by including the drain current mismatch of M5≢M6 and M11≢M12 due to their threshold voltage, VTH, random variations as:

$$\frac{V_{OUT+} - V_{OUT-}}{I_{IN}} = \frac{R_g\left[(I_{D11} - I_{D12}) + (I_{D5} - I_{D6}) + I_{IN}\right]}{I_{IN}} \quad (3.12)$$

The current $(I_{D11} - I_{D12}) + (I_{D5} - I_{D6})$ build a differential output voltage that can be expressed as input offset current, $I_{INoffset}$, in terms of VTH variations, as:

$$I_{INoffset} = I_{CM} \cdot \frac{\Delta VTH_{M11;M12} + \Delta VTH_{M5;M6}}{nU_T - (\Delta VTH_{M11;M12}/2 + \Delta VTH_{M5;M6})}, \quad (3.13)$$

in which ΔVTH terms are VTH variation of M5-M6 and M11- M12 transistor pairs. Considering I_{CM} as being constant, the standard deviation of the input-referred offset, $\sigma(I_{INoffset})$, due to random threshold variations can be expressed, as:

$$\sigma(I_{INoffset}) \cong \sqrt{\left[\frac{I_{CM}}{nU_T}\right]^2 \cdot \left(\frac{AV_{Tp}^2}{W_{11,12} \cdot L_{11,12}} + \frac{AV_{Tn}^2}{W_{5,6} \cdot L_{5,6}}\right)}, \quad (3.14)$$

in which $AV_{Tn} = 5\,mV\,\mu m$ and $AV_{Tp} = 5.49\,mV\,\mu m$ are the Pelgrom proportionality constants of pMOS and nMOS transistors for $180\,nm$ technology node [228]. By plugging in Eq. 3.14 the area of the transistors from Figure 3.5 the standard deviation of input-referred offset is $\sigma(I_{INoffset}) = 3.68\,nA$ at room temperature and a bias of $90\,nA$.

Measurement results distributed over seven TIA packaged samples are presented in Figure 3.19.a and show an average gain of $109.85\,dB\Omega$ within

$0.7\,dB\Omega$ flatness over all samples. The input offset has been measured as next and compared to the theoretical value-from Eq. 3.14. Figure 3.19.b shows the $I_{INoffset}$ spread value of the same TIA in seven samples (Note: without a large number of samples, a statistical analysis would end in a fallacy [229] with errors in order of magnitudes). The factor 4.7 difference between the calculated and the measured value is mainly given by the assumption of no geometrical variations of the transistors and a zero offset CM op-amp A. Moreover, contributions from variable leakage of the ESD diodes, die package, QFN48 socket imperfections, or Keithley2400 [230] current integration error must also be considered here.
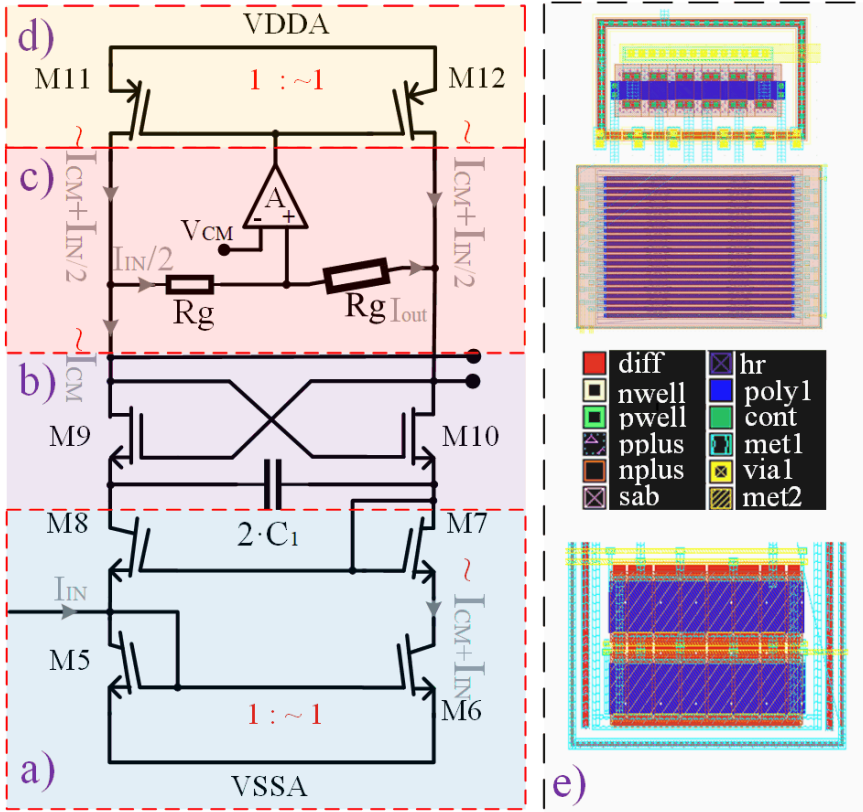
Figure 3.18: Schematic of the TIA mismatch components: a) input current mirror mismatch; c) gain resistor mismatch; d) adaptive bias current sources mismatch; e) CMOS layout design of the respective components.

One solution for improving the offset is to increase the area of transistors.

However, this comes at intense power consumption, which might not justify CNT-FET nanosensor applications with their relatively more significant device-to-device variation [6] [83]. It is highly desirable to mitigate device mismatch's effect for general purpose analog signal processing to achieve the desired accuracy performance. As presented at the beginning of this paragraph, the device mismatch is caused by randomness in fabrication processes and hence is usually corrected after device fabrication [226]. As an alternative, one broadly used method, i.e., auto-zero calibration or chopping/spinning techniques [231] can do offset corrections on the flight without technology modifications. This method comes at the price of interrupting the signal processing and regularly making the circuitry offline. Furthermore, the limitation of these correction techniques is given by the matching accuracy between its switches [231]. Furthermore, the switching timing depends now on an external precise quartz oscillator which draws additional power. Despite the introduced functional disadvantages, these methods have improved system accuracy significantly for decades. Other approaches propose a post-fabrication selection of optimal devices from a large set of redundant fabricated devices [232]. However, this is not always the most cost-effective option.
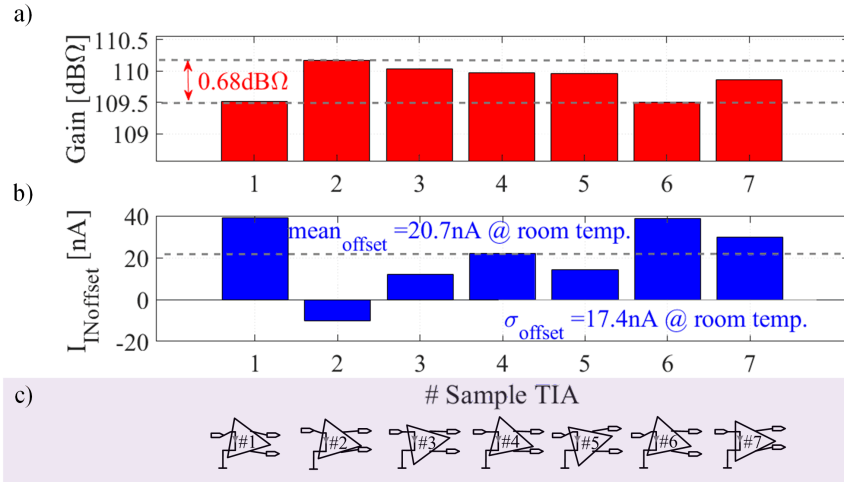
Figure 3.19: Measurement results of seven TIA samples: a) transimpedance gain and gain flatness; b) input referred offset; c) illustration of the seven samples. Measurements were performed at room temperature with a Keithley 2400 source-meter lab instrument. DUT: ASIC V3 presented in Appendix A.6.

3.4.1.8 PVT variations

The I_{CM} bias current is generated with the help of the op-amp connected in a negative feedback loop at the gates of M11 and M12, which operates as two voltage-controlled current sources. The analytical value of I_{CM} current about I_{IN} is not trivial to calculate. However, its dependency can be expressed as:

$$
\begin{cases}
V_{CM} + \frac{V_{out}}{2} \overset{\mathrm{I_{IN}<0}}{=} \underset{I_{CM}}{V_{GS10}} + \underset{I_{CM}+I_{IN}/2}{V_{GS8}} + \underset{I_{CM}}{V_{GS5}} \\[2em]
V_{CM} \overset{\mathrm{I_{IN}=0}}{=} \underset{I_{CM}}{V_{GS10}} + \underset{I_{CM}+I_{IN}/2}{V_{GS8}} + \underset{I_{CM}}{V_{GS5}} \\[2em]
V_{CM} - \frac{V_{out}}{2} \overset{\mathrm{I_{IN}>0}}{=} \underset{I_{CM}+I_{IN}/2}{V_{GS10}} + \underset{I_{CM}}{V_{GS8}} + \underset{I_{CM}+I_{IN}/2}{V_{GS5}}
\end{cases}
\tag{3.15}
$$

As can be seen from Eq. 3.15, the I_{CM} value changes with the I_{IN} current (also visible in Figure 3.7) substantially changing the transistor's conductance. Nonetheless, its effective value does not influence the gain of the TIA, which is Gm independent. Compared to a classical open-loop gain amplifier, this TIA has a DC gain defined by the value of Rg resistors rather than a gm value, which is considered constant.

The variations of transistors M11-M12 dominate the mismatch of this TIA, M5-M6 analyzed in 3.4.1.7 and the Rg resistors variations [198]. Process-voltage-temperature (PVT) simulations are presented in Figure 3.20 showing a $1\,dB\Omega$ gain flatness for $I_{IN} = \pm 1\,\mu A$ at operation temperatures from -20°C to 80°C and 1.8V ±0.1V VDDA supply voltage.

Figure 3.20: Simulation results of the TIA PVT: nMOS, pMOS transistor process variation, nominal Rg resistor value, and $1.8\,V \pm 0.1\,V$ VDDA.

When including the Rg gain variations, one can trim its effective value with the help of a digital block which can add or subtract resistive finger elements via CMOS switches.

3.4.1.9 Power consumption

The static power consumption is $180\,nW$ when supplied at $1.8\,V$. It scales dynamically with the input current level, $|I_{IN}|$, thanks to the class AB operation. The power consumption has been measured with the help of a shunt resistor, $7.7\,k\Omega \pm 1\%$ at substantial $|I_{IN}|$ values such that its voltage drop could be monitored. The absolute differential voltage versus $|I_{IN}|$ current span is presented in Figure 3.21.a. The resulted power consumption has been measured in Figure 3.21.b for currents $|I_{IN}| > 0.2\mu A$ where the resulted voltage drop can be measured. For $|I_{IN}| > 1.2\mu A$ current values, the

voltage drop, $VDDA - I_{cons} \cdot R_{shunt}$, becomes significantly such that the TIA can't operate properly. Different power consumption can be observed when sinking current from the TIA, i.e., $I_{IN} < 0$, due to the TIA branches, which have slightly different currents.

a)

b)
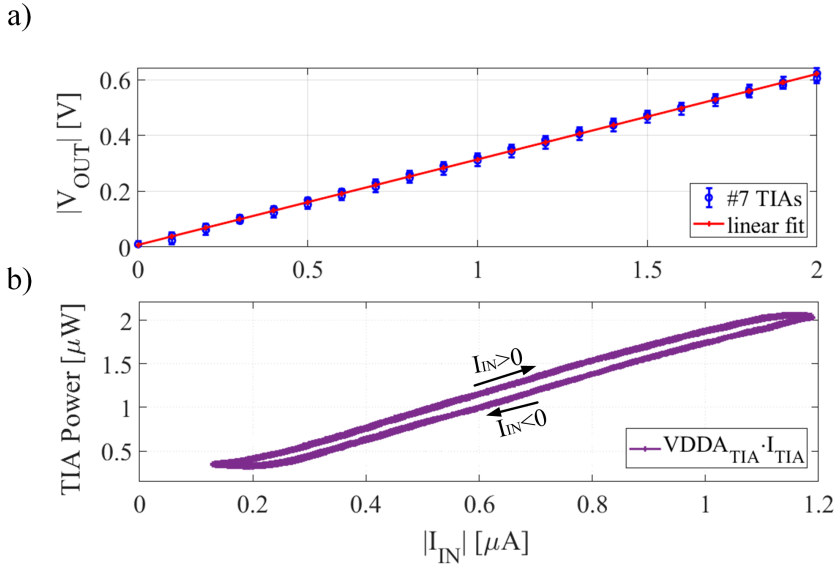
Figure 3.21: Measurement of the TIA: a) transfer characteristic without shunt resistor; b) dynamic power consumption measured with $7.7\,k\Omega$ shunt resistor which includes CM op-amp bias. DUT: ASIC V3 presented in Appendix A.6.

3.4.1.10 Figure of merit

The concept of a figure of merit (FoM) was firstly used around 1865 as a metric and represents a numerical quantity based on one or more system or device characteristics that describe a measure of efficiency or effectiveness [233]. For this design, a particular expression of FoM [234] is used to evaluate the overall performance of the designed TIA as:

$$FoM = \sqrt{\frac{P[W]}{kT \cdot BW[Hz]}} \cdot \frac{K[\%]}{DR[ratio]}, \tag{3.16}$$

where P represents power consumption, BW is the bandwidth, DR is the spurious-free dynamic range, and K is the linearity in %. In this case, the

smaller the FoM, the better the design performance. Compared to the very popular expression, $NEF = Vin_{rms}\sqrt{(2 \cdot I_{TIA})/(\pi V_T \cdot 4kT \cdot BW)}$, the FoM from Eq.3.16 was introduced in [235], which is often used for low noise amplifiers, transimpedance amplifiers, and sensor front-end. However, this FoM is not appropriate for this particular design since the current consumption, I_{TIA}, is dynamic and depends on I_{IN} due to which the power consumption scales linearly. The I_{IN} level performs trade-offs, i.e., SNR, PSD, and SFDR. Moreover, FoM [235] is not appropriate because it considers only thermal noise, whereas FoM [234] also includes linearity in addition to noise and current consumption. A comprehensive comparison with different designs is presented in Table 3.1.

Table 3.1: Comparative analysis of different TIA implementations recently published in the literature.

Ref. Spec.	[154] This work	[236] BioCAS'16	[237] ISSCC'18	[238] JSSC09	[239] IEEE-Trans'06	[240] IEEE-Bio'12
Technology [μm]	**CMOS 0.18**	CMOS 0.35	CMOS 0.13	CMOS 0.5	BiCMOS 1.2	CMOS 0.18
Channels	**1**	1	12	4	16	1
Bidirectional input	**yes**	yes	no	yes	yes	no
Architecture	**CT**	CT	DT	CT	CT	DT
Bandwidth [kHz]	**10**	4.8	5	5	12	0.1
Sensitivity [pA]	**2 @ 1Hz**	55	3.4	7.4	46	22
Linearity [%]	**4**	1[a]	2	0.005	1	0.2
SFDR [dBc]	**56**	67	50.3	56	40(DR)	55
Area [mm^2]	**0.02**	0.11	0.004	5.1	4.5	0.18
Power/ch. [μW]	**0.28**	9.5	0.05	72	776	90
FoM [234]	**0.16**	38	0.33	0.35	7	29

[a]estimated value

3.4.2 Successive approximation register ADC

Successive-approximation register (SAR) architecture is one possible choice when implementing a moderate-speed Nyquist analog-to-digital converter (ADC) [223]. Although the SAR ADC with charge redistribution architecture appeared in the late 70s [241], in the last two decades, it was revived thanks to CMOS process technology scalings and recent architectural innovations. The capacitive nature of the CMOS technology and the small size and cost of CMOS switches make this specific architecture an attractive choice. Several designs are presented in the literature, where analog and digital circuits are operated at reduced supply levels, tremendously improving the power efficiency, and conversion speed [242] [243] [244] [245] [246]. A collection of ADC architectures compared by their energy per conversion and accuracy is updated annually as a survey presented in [7]. Compared to other architectures of medium accuracy, the SAR ADC is proven to be exceptionally power-efficient. Its SNDR range of 40 to $70\,dB$ is sufficient to fulfill the design criteria for the CNT-FET NO_2 nanosensor, where low-frequency analog signals need to be converted into a digital representation.

In the current literature, a few designs achieving either high speed, high precision, or low power consumption are worth mentioning. The fastest SAR ADCs reach sampling rates of up to $90\,GSps$ when using a time-interleaving technique [247] of 64 SAR ADC channels, each running at $1.4\,GSps$. This design was produced on a CMOS $32\,nm$ silicon on insulator (SOI) technology, demonstrating the possibilities of technology scaling for SAR ADCs. The SNDR accuracy is $101\,dB$, and the power consumption is $15.7\,\mu W$ from a $1.2\,V$ supply with up to $5\,MSps$ for a SAR ADC is reported in [248]. This performance has been achieved by using an oversampling technique [223]. The DAC mismatch errors and comparator noise are frequency-shaped and pushed out of the band with this approach, resulting in a clear in-band spectrum. A remarkable low power consumption of $1\,nW$ can be found in [246] in the form of a $10\,b$, $1\,kSps$ SAR ADC. This extremely low power consumption is achieved using sub one V supply, attofarad (aF) DAC capacitors, an energy-efficient comparator design, and asynchronous logic. However, at such low power levels, the significance of the leakage current becomes apparent. While today the SAR ADC architectures remain a popular choice, one can observe the trend of moving towards combinations of SAR ADCs and various other ADC architectures, so-called hybrid designs (SAR-assisted ADCs). These hybrids attempt to match the power efficiency of SAR ADCs with concepts from various topologies, such as pipelining [249], sub ranging [250], noise-shaping [251], and sigma-delta modulators[252]) to overcome the shortcomings of the SAR ADCs.

The high-speed ADC at $MSps$ sampling rates is not necessary for the CNT-

FET nanosensor application due to its relatively slow response time [4]. Instead, a moderate resolution is desired, i.e., $<10\,bit$, with few $kSps$ and very low power consumption. This thesis explores the classical (without calibration) SAR ADC, which can achieve good power efficiency and accuracy mainly given by the DAC capacitor minimum value and matching offered CMOS technology node.

3.4.2.1 SAR ADC theory of operation

The generic architecture of a SAR ADC is shown in Figure 3.22, which conceptually shows a sampler, a DAC, and an ADC comprising a feedback loop by a summation point, where the result of the last two is evaluated successively.
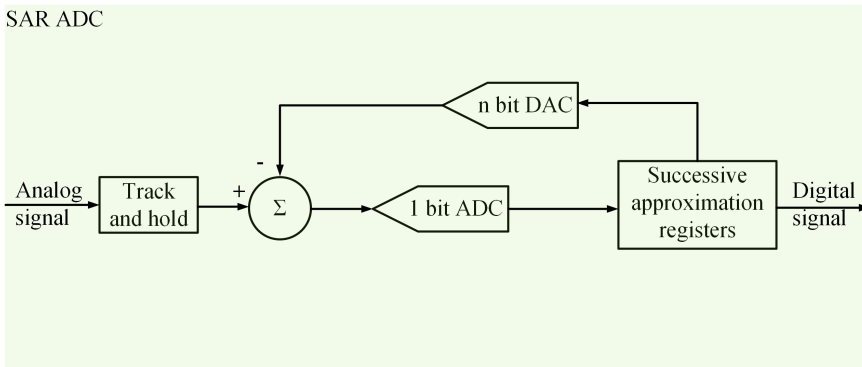
Figure 3.22: Generic block diagram of a SAR ADC.

This working principle can be compared with an old-fashioned balance scale: on one side of the scale, an unknown quantity is placed, whereas, on the other side, a known weight, i.e., 1/2 of the full-scale, is set. The scale compares these two values and shows if the unknown is "lighter" or "heavier" than 1/2 of full-scale. This initial weight is the most significant bit (MSB) in a SAR ADC. The 1/2-scale weight is kept on the scale if the unknown quantity is larger; if it is smaller, it is removed. This process is repeated with lighter weights in a binary succession, e.g., 1/4, 1/8, 1/16, 1/32, ...$1/2^n$ of the full scale. For the electronic SAR ADC, this can be translated as follows:

- Each visual comparison with a new scale weight represents the ith conversion step of the SAR ADC

93

- 2^n represents the number of available weights, or the resolution, respectively

- Each scale weight represents a binary bit b_i of the SAR ADC

The flow chart implementing the SAR algorithm is presented in Figure 3.23.
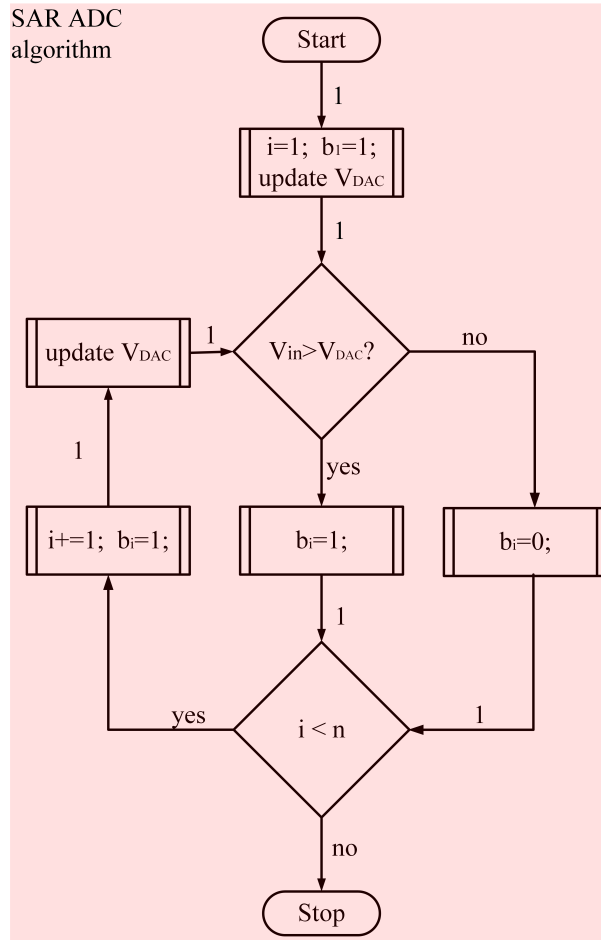
Figure 3.23: SAR algorithm resolving a n *bit* ADC conversion visualised as a flow chart.

In the here presented ASIC design, the SAR ADC, which is visualized in a generalized form in Figure 3.22, has been implemented in $180\,nm$ CMOS, as

illustrated in Figure 3.24 as one particular architecture that offers excellent power efficiency [243].
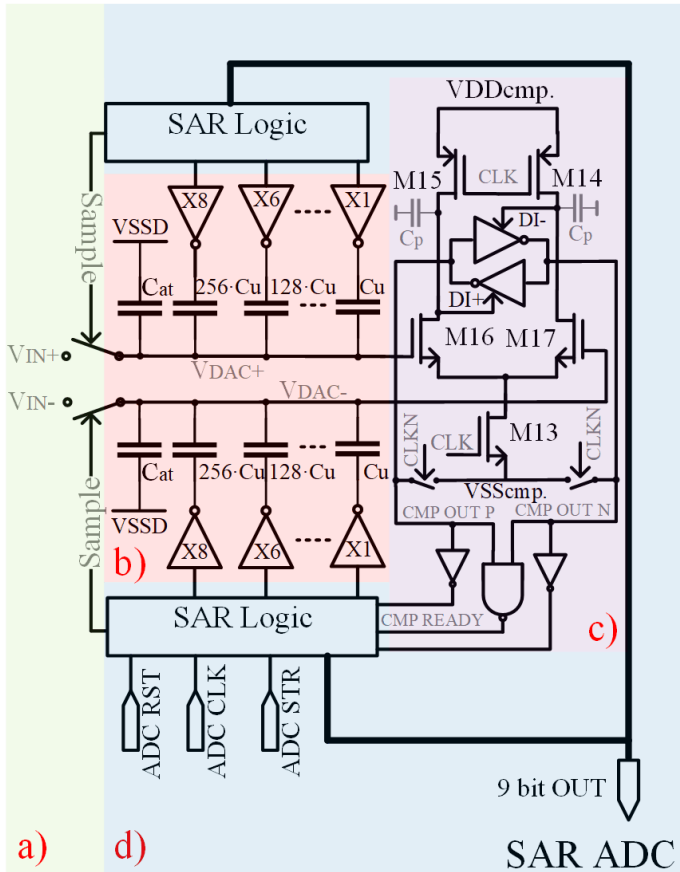
Figure 3.24: Schematic of the differential SAR ADC composed by: a) differential sampling switches; b) differential capacitive DAC including bottom plate logic drivers; c) regenerative latch dynamic comparator and static logic gates; d) digital data registers implementing the SAR algorithm including input control signals and 9 *bit* output result.

At its input, $\pm V_{IN}$, the differential TIA voltage, is sampled on the top plates, denoted by $\pm V_{DAC}$, of a differential capacitor array as presented in Figure 3.24.a. The build-up charge is then isolated from the input on the DAC top plates as presented in Figure 3.24.b. The top plates of the DAC are connected to the dynamic latch comparator's nMOS gates, illustrated in Figure 3.24.c, yet preserving the charge. Subsequently, the comparator can evaluate upon the $V_{DAC+} - V_{DAC-}$ voltage difference, and the digital result

closes a loop via the SAR memory registers presented in Figure 3.24.d, back to DAC capacitor array's bottom plates. The same capacitor array is utilized for sampling the input signal, constructing the DAC, and creating the nested summation point in this configuration as shown in Figure 3.22, while preserving excellent power efficiency. The following paragraphs describe each block in detail, including its shortcomings and trade-offs.

3.4.2.2 Track and hold

During an A to D conversion, the analog signal must remain unchanged. For this requirement, a so-called track and hold circuit is implemented. This block stores the analog input signal onto an element, i.e., a capacitor, and keeps it stable such that the SAR ADC can quantize it. In Figure 3.24.a, the differential track and hold is composed of two switches, sampling the input on the DAC capacitors rather than an explicit additional capacitor. As shown in Figure 3.24.b, the top plates of the DAC capacitors track the input differential signal $(V_{IN+} - V_{IN-})$ as long as the *Sample* signal is on a logic high level. As soon as *Sample* transitions to a logic low, the input is sampled and stored on the DAC capacitors. A simple solution for the implementation of the sampling switches is given by connecting an n-channel (nMOS) and a p-channel MOS (pMOS) device connected in parallel as presented in Figure 3.25a. This circuitry can be implemented in $180\,nm$ CMOS, as illustrated in Figure 3.25b, where $VDD >> VTH_p + VTH_n$. In this design, the common voltage level, $V_{CM} = 900\,mV$, denotes the middle range leading to a switch with a rail-to-rail conductivity. Alternatively, one may use clock bootstrapping [253] at the sampling transistor gate. This generates a gate input-dependent control voltage of $V_{IN} + V_{DD}$. However, in this particular $1.8\,V$ design, the bootstrapping block would only consume additional power without being superior in terms of linearity compared to when used in conjunction with sub $1\,V$ designs [254].

Several non-idealities were considered when designing the track and hold circuit block. These can be classified according to the status of the circuit:

- **Tracking phase:** When the *Sample* signal is *high*.

    - **ON-resistance**: At first glance, the R_{on}, in series with the capacitive load, C_L, forms a low-pass filter (LPF) that defines the SAR ADC bandwidth. Moreover, $Ron_N \approx L/[W \cdot (V_{Sample} - V_{IN} - VTH_n)]$ [198] is signal-dependent, an effect that introduces frequency-dependent distortion [255]. However, in this particular design, the CNT-FET sensor signal frequency is well below the cut-off LPF, above which distortion

(a) Sample and hold CMOS switch highlighting its finite on resistance and the capacitive load.

(b) Track and hold transistor pair in UMC $180\,nm$ CMOS layout. The capacitive load is not shown.
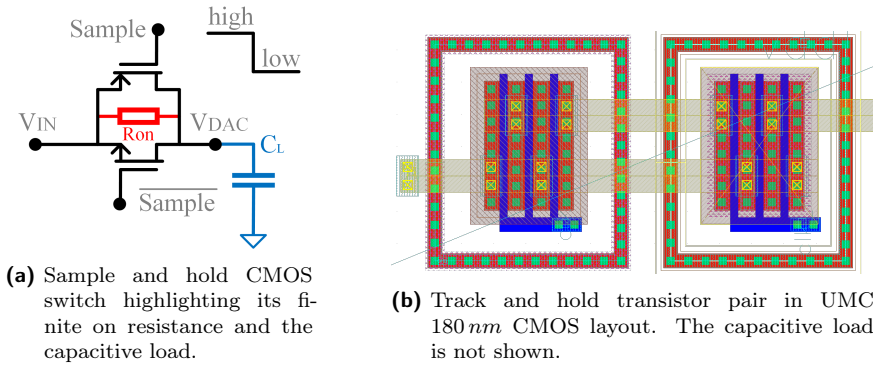
Figure 3.25: SAR ADC track and hold block implemented as CMOS switch: schematic and $180\,nm$ UMC CMOS layout.

becomes significant. To overcome these shortcomings without increasing the *Sample* signal amplitude, the R_{on} has been decreased by increasing the $W_{n;p}/L_{n;p} = 50$ ratio. Another option would have been the use of low V_{TH} transistors at the price of an increased leakage or a bootstrap circuit [256].

- **Sampling instance:** When the *Sample* signal switches from *high* to *low*.

  - **Charge injection:** When the sampler switches to *low*, the electrical charge Q_{ch} in the channel needs to be evacuated in the time instance. This effect is called charge injection and creates a voltage spike $V_{spike} = Q_{ch}/(2C_L)$ causing offset, gain errors, and frequency-independent distortion. However, these parasitic effects caused by this spike are partially compensated by the differential nature of the SAR ADC. A common solution is the use of dummies that compensate for charge injection. In this design, the total transistor area, $W \cdot L$, has been reduced to $L = 240\,nm$, thus compensating for the charge injection impact. Here the trade-off between R_{on} and charge injection when sizing the sample and hold transistors becomes apparent.

  - **Sampling noise:** Superimposed on the input signal, the thermal noise originating from the CMOS switches is also sampled on C_L, having a total noise power of kT/C_L. Moreover, in this SAR ADC design, the noise is doubled. The only design solution here is to size C_L adequately. However, the relatively high supply voltage of $1.8\,V$ in this particular design leads to a sufficiently high SNR.

– **Jitter and time skew:** The instance of a time when the sample is acquired can be derived from the nominal timing by Δt_{Sample}. For a periodic input signal, this generates an error at the output of the sampler $\Delta V_{DAC} = (\delta V_{in}/\delta t) \cdot \Delta t_{Sample}$. The error becomes critical for ADCs with high-frequency input signals, which is not the case in the CNT-FET sensing application presented here. This parasitic, on the other hand, is noteworthy for introducing the general terminology of jitter (Δt_{Sample} is random) and skew (Δt_{Sample} is fixed).

– **Signal aliasing:** Signal aliasing is another a topic of concern when designing the track and hold circuitry. Aliasing refers to signal reflection around the sampling frequency in the frequency domain. Aliasing is an undesirable result that necessitates using low-pass anti-aliasing filters in front of the ADC to remove high-frequency noise components that would otherwise alias into the pass-band [223]. The TIA can realize such a filter as presented in section 3.4.1.

- **Hold phase:** When the Sample signal is *off*. During this stage, the SAR ADC's input should be entirely isolated from the rest of the circuit (ideally disconnected).

– **Leakage:** Any resistive path, which connects its input with the output of the sampler, results in a leakage of the sampled voltage. When the sample transistors are not driven properly, a channel from the drain to the source or the substrate is created. If the sampled voltage leaks via such paths during the conversion step, the output will be incorrect. For the reduction of this leakage, individual well substrate contacts have been used, as shown in Figure 3.25b. Minimizing the W/L ratio can make a compromise between the leakage and R_{on}. Another solution, which can reduce the leakage, is using low threshold voltage transistors.

– **Capacitive coupling:** The C_{DS}, drain to source capacitances (not shown in Figure 3.25a for simplicity) of the CMOS transistors directly couples the V_{IN} with V_{DAC}. This effect, in turn, leads to faults in the ADC conversion process. Because the application only requires relatively low sampling frequencies in the kHz range, R_{on} does not need to be exceedingly low, so the C_{DS} can be maintained low by reducing the transistor area.

3.4.2.3 Capacitive DAC

This DAC is implemented as a switched capacitor array, a structure that explores the advantage of having no active power consumption. Unlike alternative solutions, such as a resistive array, only displacement currents flow on the capacitor's plates. Its complete schematic has been shown in Figure 3.24, and design considerations, including imperfections, are described next.

- **Design characteristics**

  - **Switching scheme:** The monolithic switching scheme, implementing binary search by the means of charge redistribution, was used in this design. Despite different switching techniques presented in the literature, which can reduce the DAC power consumption substantially, such as split capacitor switching [257], merged capacitor switching [242], average charge switching [245], or detect and skip switching [250] schemes, the monolithic scheme was chosen for its simplicity. It has no logic gates or internal references, which increases linearity, reduces noise, and lowers the overall power consumption making it a good choice for moderate resolution ADCs [246].

  - **Full-scale range:** The DAC array is presented in Figure 3.24, where capacitors are driven in a binary manner by standard library logic inverters at their bottom plates implemented. To reduce energy consumption, the value of the LSB unit capacitor, C_u, is set to $2\,fF$.
    This represents the unit size of an $1.28{\times}1.28\,\mu$m MIM capacitor (on metal top layers 5-6), being the minimum value offered by UMC $180\,nm$ technology's PDK. Since the architecture was chosen to be fully differential, the input voltage range can reach $2{\times}VDD_{dig}$ and hence two capacitors, $Cat = 750\,fF$ each, have to be added to obtain the desired peak-to-peak full-scale input range of the ADC. Therefore, the VFS_{pp} differential can be expressed as:

$$VFS_{pp} = 2 \cdot \frac{VDDdig.\left(2^9 - 1\right)C_u}{\left(2^9 - 1\right)C_u + C_{at}} = 1.45 V_{pp} \qquad (3.17)$$

  - **Speed:** The SAR algorithm resolves the bits by switching the logic inverters connected to the bottom plates of the SAR DAC. Each switching instance of the DAC causes an exponential settle

of the next level given the $R_{on} \times C_{DAC}$ time constant, which limits the speed of the ADC. Given the binary-weighted capacitors, the on-resistance has been decreased by using inverters with weighted switching strength ($\times 8$, $\times 6$, $\times 1$ from the standard library) to keep the switching speed constant.

- **Nonidealities**

  - **Noise:** The thermal noise is originating from the CMOS switches is injected into the DAC top plate capacitors array at the sampling instance. Due to the differential structure, the noise total noise power doubles as $2kT/C_{DAC}$. The thermal noise of the differential sampling capacitors can be expressed in terms of effective differential noise power as:

$$ P_{noise} C_{DAC} = 2 \cdot \frac{kT \left(2^9 - 1\right) C_u}{C_{at} \left[\left(2^9 - 1\right) C_u + C_{at}\right]} = \left(49 \mu V_{RMS}\right)^2, \quad (3.18) $$

    which is well below the ADC quantization noise of 0.81 mV_{RMS}. The on-resistance of the logic inverters adds additional noise to the bottom plate of the capacitor array. Scaled inverters, denoted as $\times 8$, $\times 6$, $\times 1$ in Figure 3.24.b, have been used to overcome this effect. However, a considerable amount of noise is injected via VDD_{dig} since the SAR ADC structure has no dedicated V_{ref}. Without the requirement of an internal reference, the ADC design becomes less complex. However, it shifts the problem to the power supply (also the ADC reference in this case), making a low noise LDO a hard requirement.

  - **Mismatch:** Capacitor mismatch is the main restriction in the DAC design, limiting the linearity achieved with a SAR ADC. Severe mismatches of the DAC capacitors can be visible in the static linearity characteristic of the ADC [254]. Once the binary-scaled ratio has a mismatch, random or systematic variation, the DAC's comparison and intermediate voltage steps during the SAR algorithm alter the binary search. The selection of the DAC and capacitance C_s is a trade-off, i.e., a larger value than parasitics becomes much easier to scale and match. In contrast, a smaller value achieves lower power consumption, smaller chip area, and faster conversion rates. Considering the mismatch impact on the SAR ADC performance, the layout of the individual capacitors and the layout of the overall array deserve special attention. The library default MIM capacitors impose significant contacts and routing overhead for the unit capacitor elements. Instead, a custom-made,

manually tuned capacitor unit has been implemented, shown in Figure 3.26. This design uses symmetric common-centroid placement and dummies for the complete array. The effective capacitance of the structures was validated and re-tuned with a post layout RC extraction tool. However, further improvements to this SAR ADC are possible. For example, a correction procedure can add a small capacitor in parallel with the DAC array for mismatch compensation [258]. This minimizes the mismatch while keeping power consumption low at a reasonable noise performance [258]. Another option would be to use oversampling, which partially shifts the mismatch out of the band via classic chopping and dithering [259], or a dedicated mismatch-error shaping technique [248].
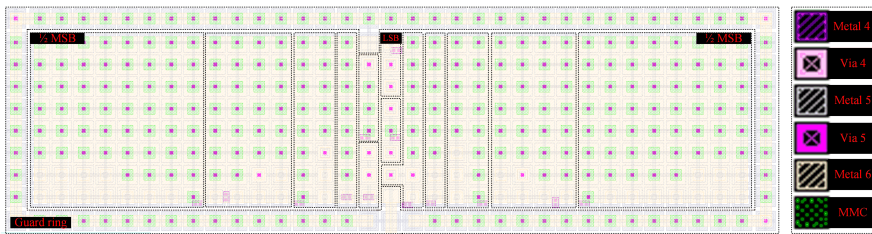
Figure 3.26: Layout of the half differential capacitive DAC array composed by: guard ring, binary scaled capacitors $256 \times C_u$ to C_u; In this particular layout C_{at} is not shown.

3.4.2.4 Dynamic regenerative comparator

The $1\,bit$ ADC, shown in Figure 3.22, represents an analog comparator with digital output. Its transistor level implementation is shown in Figure 3.24.c representing a dynamic architecture known in the literature as the Elzakker comparator. For the first time, it has been proposed in [260], and it consumes 2.5 times less energy for the same input-equivalent noise than one of [261] at an input CM level of $VDD_{cmp}/2$. Its main advantage is that it works on the rising CLK edge, resets on the falling CLK edge, and only consumes power on CLK transitions.

- **Theory of operation**

    In the first conversion cycle, the comparator determines whether its positive input signal $V_{DAC+} = V_{IN+}$ is greater or smaller than its negative input signal $V_{DAC-} = V_{IN-}$ and sends the result, $COMP_{OUT}$, back to the SAR registers. At the DAC side, the MSB is switched,

causing charge redistribution and new voltage levels V_{DAC+} and V_{DAC-} at the input of the comparator. This structure has two parts:

- **Analog preamplifier:** The preamplifier provides high gain and isolation for the capacitive DAC while the charge is redistributed. On CLK low, the pMOS transistors $M14$, $M15$ in the preamplifier precharge the parasitic output capacitances of the nodes DI_+ and DI_- to VDD_{cmp}. When CLK transitions to high, the preamplifier's tail transistor, M15, starts to conduct, letting the current flow through the differential pair. This current discharges the Cp capacitors so that the DI_+ and DI_- voltage levels drop rapidly. The input signal difference coming from the DAC is applied at the gate of M16-M17, which results in drain current differences causing one of DI_+ or DI_- to discharge faster, employing dynamic preamplification.

- **Regenerative latch:** The regenerative latch takes a digital decision based on positive feedback. In the phase of CLK low, the regenerative latch outputs, $COMP_{OUT_N}$ and $COMP_{OUT_P}$, are set to ground (V_{SSD}), and the preamplifier is disconnected. When the CLK changes to high, the DI_+ and DI_- voltage difference is fed to the regenerative latch, and the digital result ($COMP_{OUT_N}$; $COMP_{OUT_P}$) is passed to the SAR block. Once the CLK transitions to low again, the comparator resets, and the next cycle starts.

- **Nonidealities**

  - **Speed:** The comparator's delay represents the time difference between rising edge CLK and the valid digital output data $COMP_{OUT}$. This delay is inversely proportional to the differential input voltage present at M16-M17 and directly proportional to the Cp value: the smaller the voltage or higher the Cp, the longer the delay, reaching the comparator's metastability at the limit. This metastability effect leads to erroneous bits values during the successive approximation algorithm execution.

  - **Noise:** The here presented comparator comprises a pure analog block (the preamplifier) and a purely digital one (the regenerative latch), thus composing a hybrid structure. Because of the latched comparator, the noise analysis is more complex than classical analog comparators. The noise can be modeled as an input-referred noise source at the preamplifier side. In contrast, the output noise should be modeled at the output as a bit error rate (BER) [254].

The BER is generally used for digital communication systems to express that the transmission has a probability of sending a "1" and receiving a "0" due to the random noise of the transmission channel. Those two measures can be linked by the error function (ERF) function [254], which can be expressed as:

$$P_{"1"} = \frac{1}{2}\left[1 + ERF\left(\frac{V_{DAC}}{\sqrt{2Pn_{cmp}}}\right)\right],\qquad(3.19)$$

where $P_{"1"} = 1 - P_{"0"}$. When $V_{DAC} \approx 0$, the theoretical probability becomes $1/2$, thereby, the output result is affected by the noise. When V_{DAC} is different than 0, the Pn_{cap} (inversely proportional to C_p value [261]) dictates the probability $P_{"1"}$.

– **Mismatch:** The layout of the M16-M17 differential stage plays a crucial role while dictating the Cp value. An imbalance of the two branches due to inequal parasitics can lead to substantial comparator offset. The layout of differential pair M16-M17 has been realized with an odd number, i.e., five fingers interdigitated in a serpentine-like structure to overcome this effect. Moreover, two dummies have been added with half-length at the boundaries of the serpentine together with a substrate ring. The routing of critical signals, DI- and DI+ has been realized as fully symmetric. Perpendicular routing on adjacent metal layers is used to suppress signal coupling, i.e., CLK signal with analog signals. The complete layout of the comparator, including the regenerative latch and logic gates, is presented in Figure 3.27. A matched $Cp = 4.9\,fF$ value has been obtained at post-simulation of this structure.
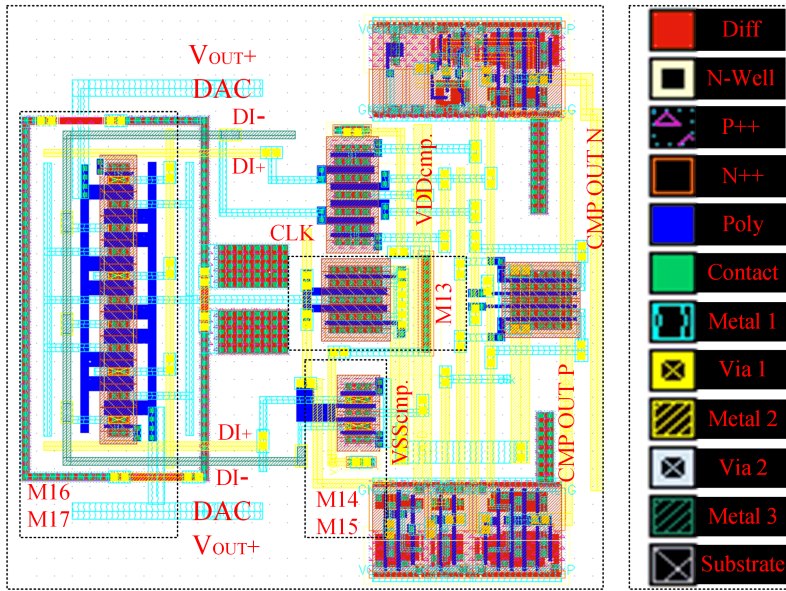
Figure 3.27: Layout of the dynamic comparator's preamplifier and the regenerative latch including logic gates in $180\,nm$ UMC CMOS technology node. Analog preamplifier's transistors together with critical signals routing are highlighted.

- **Power consumption**

  The power consumption of the dynamic comparator is proportional to the value of Cp. In this design, the smallest possible value has been used, i.e., the parasitics of the differential stage interconnections. There is no capacitor cell, as shown in Figure 3.27. There is, however, a direct trade-off between power usage and noise output. The comparator operates only during the discharging phase (rising CLK edge). An apparent power efficiency improvement here would be to operate the comparator on both edges as previously proposed in [262] rather than using the discharging phase only. This approach was not implemented due to the logic gate overhead and additional transistor pair.

3.4.2.5 Digital control signals

A library standard set of flip-flops implements the data register, containing the digital code that controls the DAC. The register set comprises a shift register (flip-flops) array and two arrays of result registers. The first set im-

plements a shift register array starting with the sampling phase and stirring the successive approximation i^{th} step as presented in Figure A.1 of the Appendix A.3.3. At the end of the SAR, this register will have the final digital output code of the ADC. Digital cells from the standard library have been used in this first design. The power efficiency can be further improved with custom logic circuitry as suggested in [243].

3.4.2.6 Static performance

The absolute static accuracy of an ADC can be described by its major imperfections, i.e., offset, gain, and nonlinearities [223]. Traditional static specifications, such as integral nonlinearity (INL) and differential nonlinearity (DNL), are typical metrics for determining an ADC's static performance: the nonlinearities are the most critical imperfections since the other ones, i.e., gain and offset, can be calibrated. In distinction, there is no procedure capable of correcting linearity errors post-design. These can be summarised as:

- **Integral nonlinearity: INL**

  At any point in the ADC transfer function, the INL (relative accuracy) represents the highest deviation of the output code from its code centers.

- **Differential nonlinearity: DNL**

  The maximum variation of an actual output code step from the ideal step value of $1\,LSB$ is represented by the DNL (absolute accuracy). The ADC's transfer function is non-monotonic if the differential nonlinearity is more than $1\,LSB$.

For the ADC INL and DNL characterization, the "servo-loop" test method has been used [223]. The AD9717 [263] DAC integrated in the Analog Discovery 2 (AD2) characterization setup. The accuracy of $14\,bits$ of the arbitrary waveform generator (AWG) is significantly higher than the designed ADC device under test (DUT). In Figure 3.28a, the "servo-loop" concept is illustrated. The $14\,bits$ $105\,MSps$ AD9648 [263] in the AD2 oscilloscope was used as reference ADC. In addition, the pattern generator and the logic analyzer were used to control the ADC (DUT) and acquire the data. Further AD2 schematics and the SDK manual can be found in [263] [264]. The USB interfaces the hardware in a Python script. Moreover, averaging techniques can mitigate the impacts of ADC input-referred noise when using this measuring method.

The designed ADC was characterized at a supply voltage of $1.8\,V$. The measured integral/differential nonlinearities are shown in Figure 3.28b with a peak value of $[-1.2; 1.3]\,LSB$ for INL and $[-0.25; 0.35]\,LSB$ for DNL, respectively.

The main origins of the nonlinearities of this design are:

1. Mismatch of binary-driven capacitors

2. Scaling of digital inverters (non-binary in this PDK)

3. Routing asymmetries

Large INL and DNL errors raise the noise and distortion level of the ADC, making it inappropriate for the application. The distortions metric is examined further as the ADC's dynamic performance.
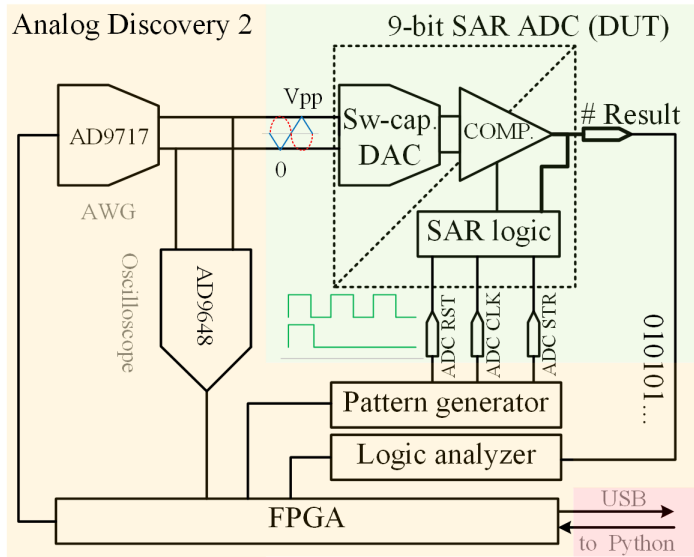
(a) Block schematic of the servo-loop and ADC as a device under test (DUT) realized with AD2 hardware controlled in Python via USB interface. Signal trigger and synchronization for the measurement are ensured by the FSMs implemented in AD2 FPGA as described in the AD2 manual [264].
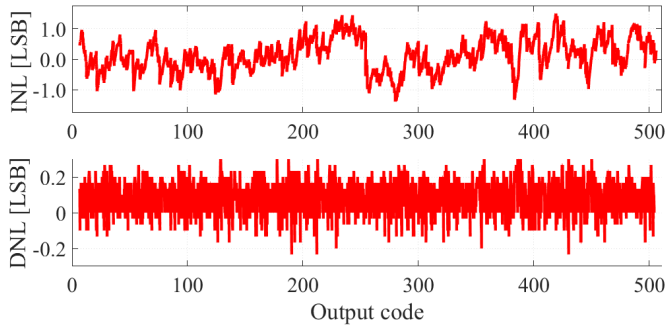
(b) Measurement results of the designed ADC INL and DNL static linearity performance. DUT: ASIC V3 presented in Appendix A.6.

Figure 3.28: INL and DNL linearity of the designed ADC: practical measurement setup and the obtained performance.

3.4.2.7 Dynamic performance

In addition to the introduced static performance, the ADC becomes fully characterized by measuring its dynamic (AC) performance. For the quanti-

fication of the ADC AC performance, six popular metrics [223] is used, i.e., signal-to-noise ratio (SNR), total harmonic distortion (THD), total harmonic distortion plus noise (THD + N), spurious-free dynamic range (SFDR), signal-to-noise-and-distortion ratio (SINAD), and the effective number of bits (ENOB). Comprehensive definitions and the mathematical relationship between SINAD, SNR, and THD can be found in [223]. For example, the ratio of the RMS signal amplitude to the mean value of the root-sum-square (RSS) of all other spectral components, including harmonics but excluding DC components, is known as SINAD [223].

The SINAD is a good indicator of an ADC's overall dynamic performance because it incorporates all components that contribute to noise and distortion [265]. Using the relationship for the theoretical SNR of an ideal n-bit ADC as follows, this metric can be transformed to the effective-number-of-bits (ENOB): $SNR = n \times 6.02 + 1.76\,dB$ [223]. The equation can be solved for n by substituting the value of SINAD for SNR, resulting in the ENOB being expressed as:

$$ENOB = \frac{SINAD - 1.76\,dB}{6.02} \qquad (3.20)$$

In this design, measuring the ENOB using "sinewave curve fitting" has been used [223]. The dynamic testing of this ADC has been performed using the same hardware setup as in Figure 3.28a. Instead of the ramp test signal (marked in blue), a sinusoidal input signal (marked in red) has been used with the following characteristics:

- The input sinusoidal signal is ADC full-scale [265].

- The input sinusoidal signal frequency is different from the subharmonics of the sampling signal [223].

- The five complete cycles of the input sinusoidal signal or more [266] are stored in the data record for Python data export.

The recorded data is then imported into Python for further postprocessing. There are numerous algorithms for calculating an ADC's distortion and noise [223].
The one used here is based on FFT and is presented in Appendix A.3.4. The measured ADC resulted spectrum for the ENOB derivation is presented in Figure 3.29 when using single-tone excitation at $0.1\,dBFS$, which includes subharmonics components due to the hard distortions of the single tone with an amplitude slightly beyond FS.
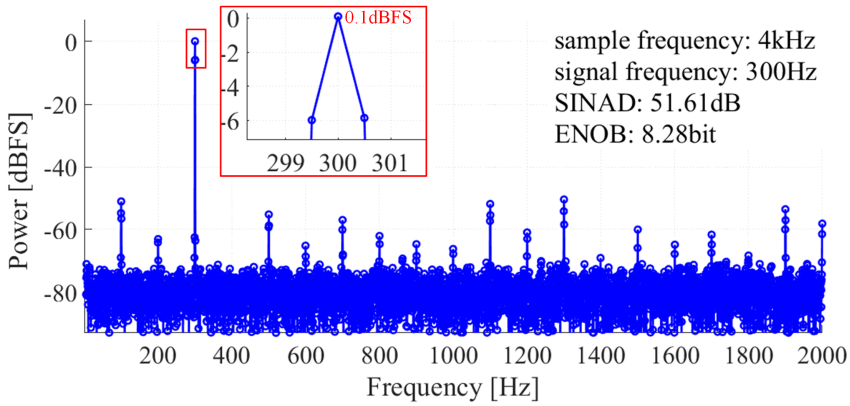
Figure 3.29: $9\,bit$ SAR ADC FFT: $f_{in} = 0.3\,kHz$, $f_s = 4\,kSps$, Hanning window-ing, N=23230 points, single tone spectrum including sub-harmonics. DUT: ASIC V3 presented in Appendix A.6.

3.4.2.8 Power consumption

The ADC consumes only dynamic power thanks to the capacitive array and the dynamic latched comparator. The power consumption for its analog and digital part has been measured separately, and the result is presented in Figure 3.30.
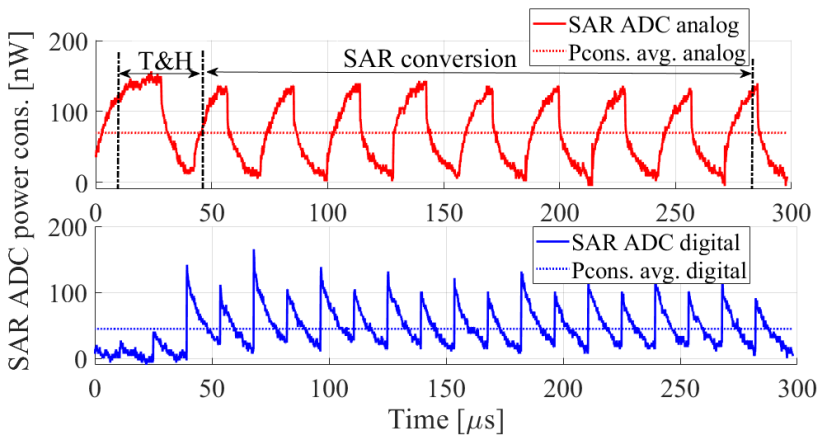
Figure 3.30: SAR ADC power analog and digital consumption measurement with the input left open. DUT: ASIC V3 presented in Appendix A.6.

The total average power consumption is $114.5\,nW$ at $1.8\,V$ supply, which can be translated into an energy efficiency [267] of $P_{total}/(fs \cdot 2^{ENOB}) = 91.7\,pJ/conversion$. In the context of a CNT-FET used as NO_2 nanosensor, the response is low frequency or almost DC [154]. Consequently, the SAR ADC can sample faster and employ averaging to enhance the converter's effective resolution. This improves the effective resolution (ENOB) by $3\,dB$ or $1/2$ bit per doubling of the sampling rate [223]. Another advantage of a fully dynamic ADC is that it has no static power consumption and thus achieves high energy efficiency at very low sampling rates.

3.4.2.9 FoM

For the characterization of the ADC, there exist several performance metrics [223]. A simple and practical FoM is constructed by a primary subset of these metrics, i.e., resolution, conversion rate, and power dissipation. This metric subset describes the trade-off resolution, power dissipation, and conversion rate trade-offs. For this particular SAR ADC, which achieves a $SINAD > 50\,dB$, the Schreier-based FoM was used [268], and can be expressed as:

$$FoM_S = SINAD + 10 \cdot log_{10}\left(\frac{f_s/2}{P_{total}}\right) \qquad (3.21)$$

When applying this formula to the SAR ADC, the $f_s/2$ equal to the Nyquist frequency yields a FoM of $154.03\,dB$. This result is comparable to the state of the art [7] as shown in Figure 3.31.
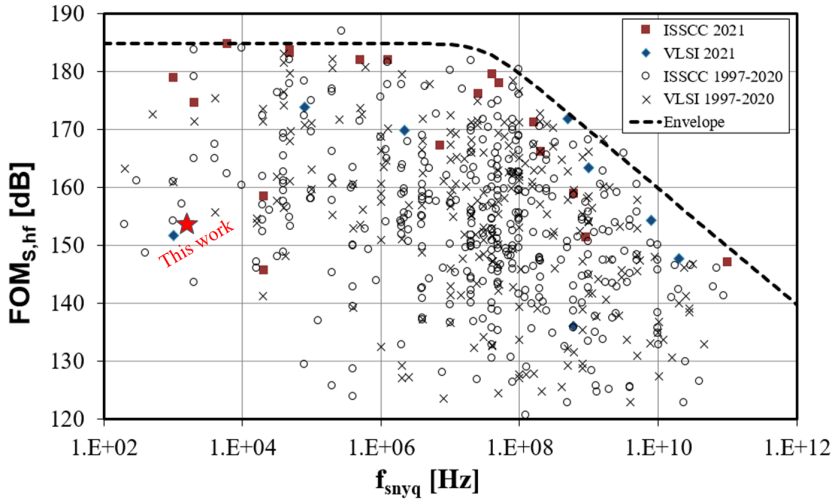
Figure 3.31: SAR ADC Schreier FoM versus frequency from collection ADC survey 2021 of Boris Murmann [7].

This achieved performance is relatively modest yet still comparable with SOA. The main reason for the resulted FoM is the power consumption overhead given partially by the high $C_u = 2\,fF\,LSB$ unit capacitor compared to the SoA $C_u = 0.25\,fF$ [246]. Moreover, the measured power consumption includes the pad-ring logic drivers, which are not having a detailed schematic in this PDK for power consumption simulations. However, the ADC shows enough performance for the final application with the CNT-FET nanosensor.

3.5 System evaluation

After the designed blocks have been individually evaluated, the entire acquisition IC must also be characterized. This section addresses the system level where the measurement error and power consumption are of interest.

3.5.1 Relative measurement error

Instead of a CNT-FET device, a set of variable resistors have been connected at the input pin of the ASIC shown in Figure 3.1. The test setup uses integer multiples of $1\,M\Omega$, $1\,\%$ series resistors for coarse value and a $8\,bit$ resistor

[269] for fine programmable value. In this way, a $10\,M\Omega$ software emulator has been created, which can synthesize the entire span of CNT-FET resistor values recently reported by this group in [82] [83]. When programming the VDS_{CNT} with the $6\,bit$ DAC, DC currents ranging from $20\,nA$ to $10\,\mu A$ have been generated. The resulted current has been compared with its theoretical value, and the relative measurement error is shown in Figure 3.32.
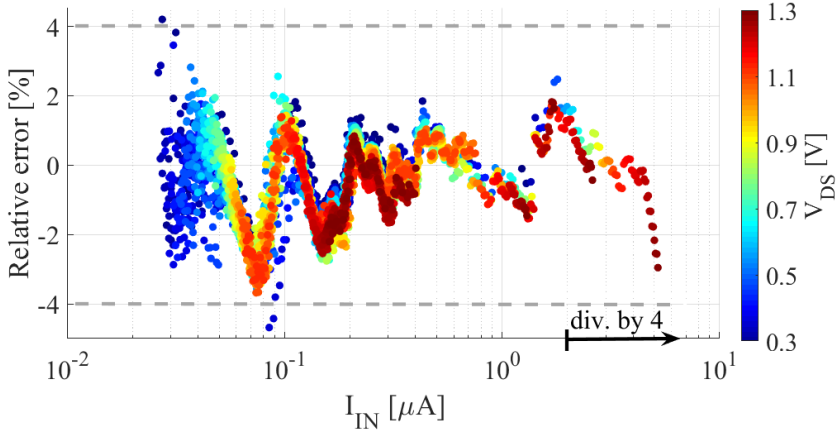
Figure 3.32: ASIC current measurement relative error for VDS_{CNT} bias voltages up to $1.3\,V$ and I_{IN} varied over two decades with div. by 4. DUT: ASIC V3 presented in Appendix A.6.

One can observe that a I_{IN} current can be obtained from different combinations of resistor values and bias voltages, giving a range of errors. When the I_{IN} value exceeds $2\,\mu A$, the "div. by 4" needs to be activated to avoid TIA saturation. The worst-case relative error of the system stays within $\pm 4\,\%$, which is reasonable for an ASIC without any calibration procedure.

3.5.2 Power consumption

The system's power consumption is mainly dynamic and depends on the I_{IN} current signal at the chip pad. However, the DAC, voltage regulator, and the TIA, draws DC current in the absence of I_{IN} as presented in the first part of Table 3.2 illustrated as a square pie. The second square pie next to it illustrates how the dynamic power consumption of the ASIC scales with the value of I_{IN}. Nevertheless the ADC power consumption scales mainly with its sampling frequency.

3.6 Further development

In this section, a design for a switched polarity (step-up and step-down) charge pump has been implemented together with a variable frequency regulator. However, the latter was not correctly working in silicon. The concept, schematics, and measurement results are presented next, together with suggestions for a further redesign.

3.6.1 Gate bias sub-block

As already presented in chapter 2.3, the V_{GS} CNT-FET potential (illustrated as being not connected in Figure 3.1) must be negative or positive and higher than VDDA [6]. This has been realized on the embedded platform with two charge-pumps MAX660 [160], connected in cascade, with an op-amp as an output buffer. In this section, an integrated Dickson-like charge pump that implements the same functionality is presented.

John F. Dickson was the first to introduce an integrated voltage multiplier for nonvolatile memory circuits [270] in 1976, which has its origins in the Cockroft-Walton multiplier realized with discrete components back in 1932 [271]. The Dickson-charge pump was self-oscillating and produced substantially higher voltages, i.e., $40\,V$ from a standard power supply of $5\,V$. Such structure works today in low voltage CMOS circuits implemented as successive capacitors and switches network. Usually, this type of multiplier does not provide substantial current at its output. Hence it is not suited as a DC-DC converter [272] with restive loads but rather for capacitive loads, i.e., the gate of the CNT-FET nanosensor. However, a more recently improved version [273], called the folding Dickson converter, has been declared one of the best choices for a DC-DC step-up converter with reduced dynamic loss and regular structure operation.

Small changes can be made to the original Dickson charge pump, i.e., replacing the diodes with actively driven switches, canceling the threshold voltage, VTH, of the CMOS switches, and eliminating the body effect of the transistors. These features combined together, broth this structure back on the stage in state-of-the-art designs [274] [275] [276], which can achieve efficiencies above $70\,\%$.

Most current applications require a step-down or a boost-up single polarity converter. In the case of the CNT-FET nanosensor, however, both positive and negative high voltage is required for biasing its gate. This is due to the

device-to-device variation, which influences the VTH and continuous process development of the p-type CNT-FET device [83]. Compared to the discrete component implementation presented in chapter 2.3, the proposed ASIC is has a $VDDA = 1.8\,V$ only. This limitation would be required two charge pumps implemented on the chip, one to boost the $1.8\,V$ positive and one to invert and boost to a negative voltage value.

A single charge pump with changeable polarity can be used to reduce chip size and power consumption. Moreover, this would typically need another op-amp to feed the desired voltage to a common terminal, i.e., VGS_{CNT}. In addition, a regulation loop that can digitally program the amplitude and polarity of the VGS_{CNT} is desired. The schematic of the CNT-FET nanosensor gate bias block is presented in Figure 3.33. The four non-overlapping phases generator is constructed from the digital input CLK signal and used for the charge-pump core. Moreover, apart from the CNT-FET gate capacitance modeled as a C_L in Figure 3.33, the pumping frequency is controlled by a programmable regulation loop via a feedback capacitor. The regulation loop has been realized by reusing the SAR ADC's already designed subblocks, i.e., the capacitive DAC and the latched comparator. Here, the C_{FB} is used to invert back the FB voltage (when negative) and bring it within the common-mode range of the comparator. Additionally, the D registers have been used for implementing a variable CLK frequency divider by an integer factor of 2, 4, or 8.

3.6.1.1 Four non-noverlapping phases

This subblock is designed to generate and feed four different phases to the charge-pump core from an input single phase digital signal. Its structure and output signals are presented in Figure 3.34. Since the four phases have to drive heavy capacitive loads of the charge-pump core, their output is designed with tapered inverters and buffers scaled as $\times 4, \times X8, \times 12$ as highlighted in Figure 3.34.a. In addition, two feedback paths, denoted as $FB1$ and $FB2$ are used to implement the timing scheme presented in Figure 3.34.b as $T1$, $T2$, $T3$, $T4$. This is critical since the charge transfer in the charge-pump core varies from stage to stage, hence the time constants are different. This implementation allows the non-overlapping timing scheme to work independently of the load.
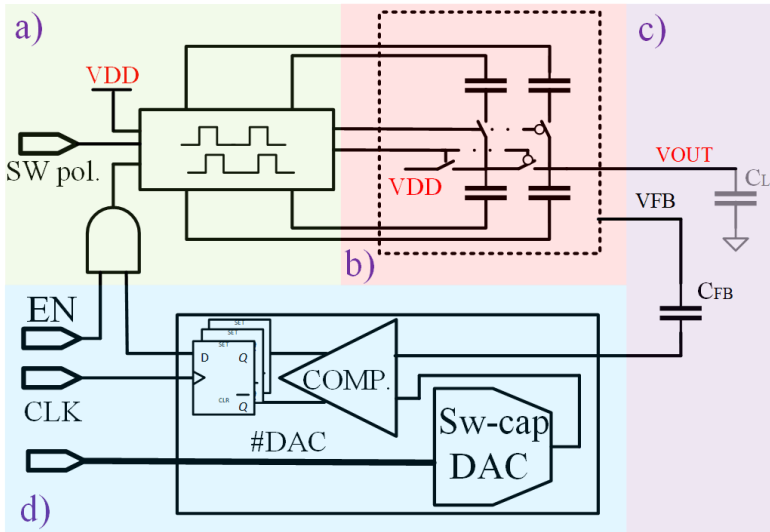
Figure 3.33: Charge-pump block schematic formed by: a) four non-noverlapping phases generator; b) charge-pump core; c) capacitive load and feedback; d) regulation loop.

3.6.1.2 Charge-pump core

This charge-pump core has been implemented by following the concept and simulation results of [8]. The simulated structure has been realised in a very similar CMOS technology node of $0.13\,\mu m$ with triple well feature. The charge-pump core is presented in Figure 3.35.

This structure can step up the VDD voltage when switches $S1$ and $S2$ are ON. Oppositely, when switches $S3$, $S4$, and $S5$ are turned ON, the VSS is connected after the last stage, and the charge is pumped on via the top side of this structure towards $VOUT$. The four non-overlapping phases are used to sample charge on the bottom plate of the CP capacitors and transfer it from one stage to another via the $'charge\ transfer'$ stages. In this implementation, four n-type stages and one p-type stage are used for a $\pm 5\,V\ VOUT$ from $1.8\,V\ VDD$. The p-stage is used when the core is pumping negative, and its substrate should not conduct [8]. As it can be seen from Figure 3.35, the charge transfer blocks are switches driven by phases instead of simple diodes [270] or diode-connected transistors [277] [278]. One design challenge here is the isolation between charge transfer individual blocks and the reverse polarization of the parasitic substrate diodes. Consequently, the transistor-level of such charge transfer block will be presented next.

a)

b)
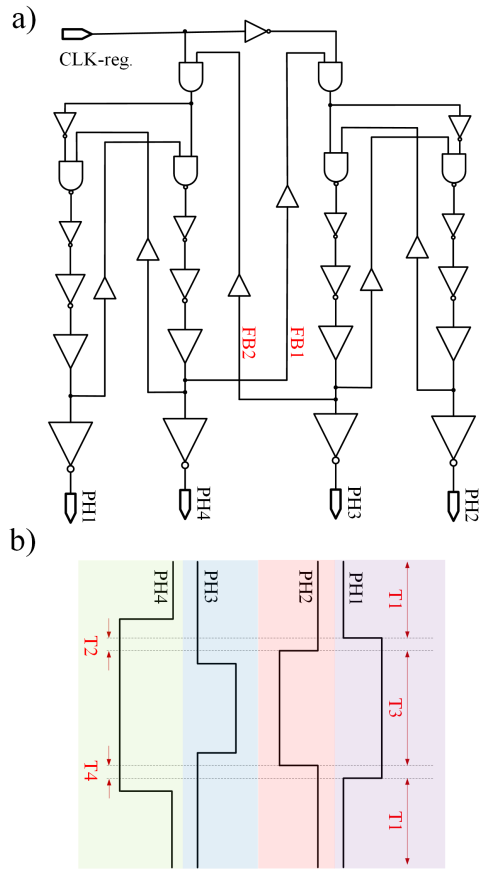
Figure 3.34: Gate level schematic of the phases generator composed by: a) four non-noverlapping phases with tapered buffers, b) illustration of the generated phases.
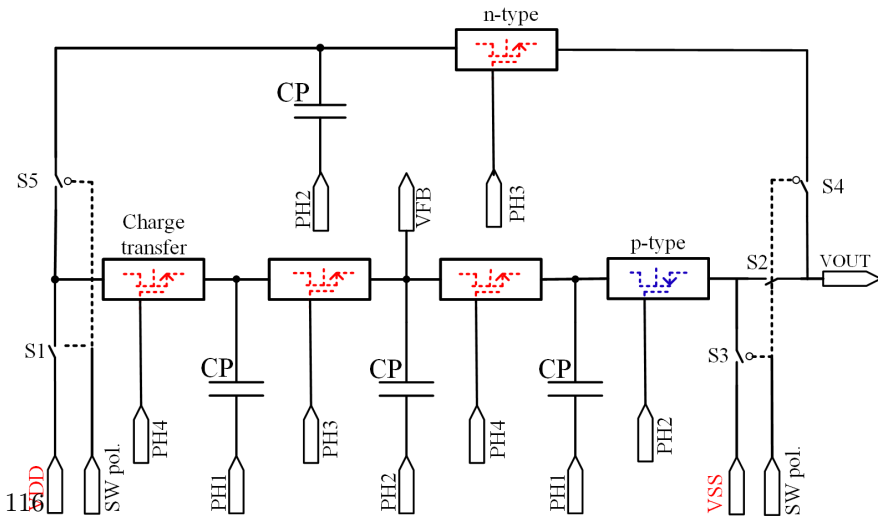
Figure 3.35: Charge-pump block schematic formed illustrating the charge transfer stages together with the pump capacitances and polarity switches [8].

3.6.1.3 Charge transfer stage

The chip's body bias becomes critical for monolithic charge pumps, especially when working with negative voltage respective to the ground. It is essential to keep all substrate diodes of the pMOS and nMOS transistors back biased such that the current flows through the transistor channel and can be controlled via its gate. The schematic of the charge transfer nMOS transistor denoted as M1, including substrate diodes and the additional transistors for body control, is presented in Figure 3.36.a.

The small capacitor C_g is used as a bootstrapping structure [279] for M1. With the help of M2 and Mtw transistors, the body control scheme is controlled such that it can back bias the substrate diodes marked with dashed lines. Since the technology has a p-type substrate connected to GND, a triple well (t-well), and nMOS transistors can ensure no substrate current flow. The p-type body and deep n-well are connected when the charge pump is positive. The PN junction between substrate and n-well is reverse biased in this situation. On the other hand, the n-well is connected to GND when the charge pump is negative. This makes the PN junction between the p-type body and p-well reverse biased. This configuration proposed in [8] prevents the substrate current. The layout of the n-type charge transfer stage is presented in Figure 3.36.b.

For the p-stage in the proposed charge pump, when the charge pump is negative, the n-type body potential is close to GND, and the body control scheme should be a break. Since the p-stage is the input stage in negative operation and suffers from the body effect, this causes little impact on the performance [8]. Despite the relatively high voltage, the Cadence simulation showed no safe operational area (SOA) warning messages for the capacitor and CMOS switches. In this way, the design is validated and not affected since the maximum voltage across stages is only equal to the input drive voltage, regardless of the number of stages.

3.6.2 Measurement results

The gate bias block of the CNT-FET nanosensor has been characterized, and the measurement results are presented in Figure 3.37. The unregulated, $1\,pF$ load output voltage has been measured first and presented in Figure 3.37.a. In the positive configuration, the $VOUT$ reaches $5\,V$. However, it achieves about $-3\,V$ only when configured to pump negatively. The output load has been progressively increased to $10\,pF$, and a voltage drop difference has been observed at the same CLK frequency of $300\,kHz$.
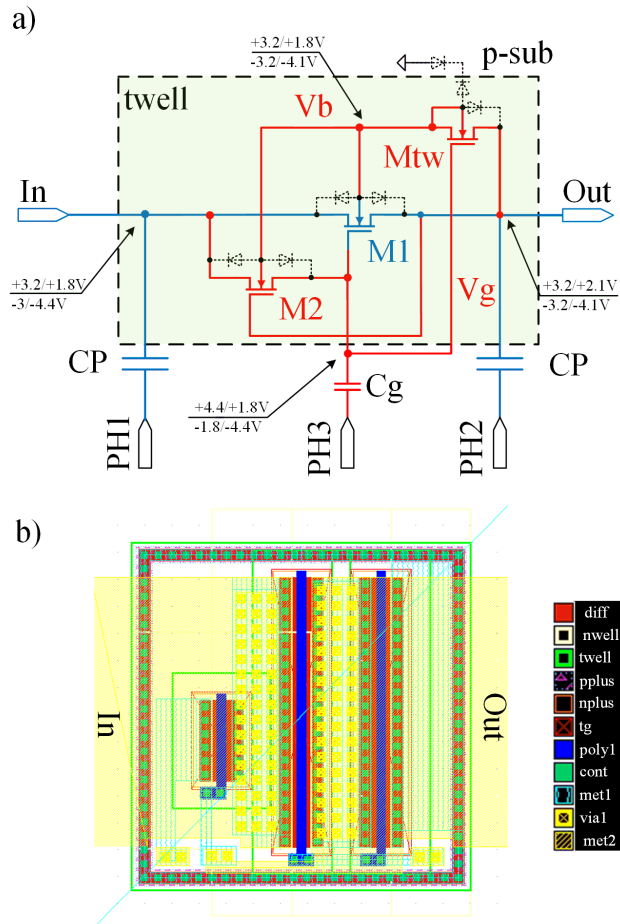
Figure 3.36: Example of one charge transfer stage [8]: a) illustrating substrate
diodes together with the nodes simulated amplitude; b) the layout
of the transistors including contacted t-well structure designed in
UMC 180 nm.

Another measurement was conducted when the regulation loop was active.
The results show an incremental step as marked in Figure 3.37.a. However,
this does not work as designed. The last measurement result has been ac-
quired with the charge-pump overloaded as presented in Figure3.37.b.

For further investigations, the ASIC V2 presented in Appendix A.5 can be
used. This version has been dedicated for the charge-pump characterisation.
It offers access to individual sub-blocks via test pads, giving more design
insights than the presented measurements via the chip pad-ring. Further, a
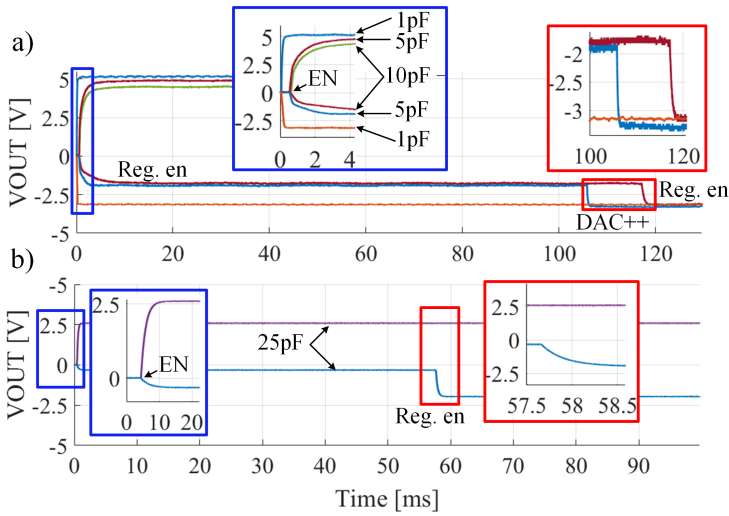
Figure 3.37: Measurement results with different C_L values and with the feedback loop active, and inactive respectively. DUT: ASIC V1 presented in Appendix A.4.

charge vector analysis [280] needs to be performed to inspect both configurations of the proposed charge pump. Then a redesign of the more robust version can be implemented in silicon.

3.7 Chapter summary

A dedicated power-efficient ASIC that acquires output signals from resistive nanosensors, i.e., a CNT-FET, has been designed, fabricated in CMOS technology, and characterized in the lab. For the IC research prototype, three distinguished tape-outs of the ASIC have been implemented (V1 for the final application, V2 dedicated for the charge-pump characterization, and V3 for individual block characterization). Each version has a combination of the presented blocks summarised in Appendix A.4, A.5 and A.6 respectively. The measurement results show that the proposed design offers input range, bandwidth, ADC speed, and precision well in line with alternative solutions for resistive nanosensors. These features are necessary for fully integrating CNT-FETs on CMOS substrate and market acceptance in the IoT domain.

Various gas measurement systems based on MEMS, NEMS, micro hotplate, and CNTs have been reported in the literature [281] [282] [283] [149]. Such transducers are often integrated with CMOS signal conditioning in an SoC

approach. MEMS [281], and NEMS [282] resonant beam transducers are dedicated to mass sensing applications and can detect different VOCs based on gas chromatography (GC), mass spectrometry, and biochemical analysis. As presented in chapter 1, MOx gas sensors present another solution for monitoring CO and NO_2. Resistance of the MOx sensor changes on exposure to a gas analyte and is typically operated at high temperatures $200\,°$-$400\,°C$ [283]. At such high operation temperatures, a monolithic solution is realized as a micro hotplate, including signal conditioning, fabricated in a standard CMOS process with additional post-micromachining steps. With an inherited high power consumption, ranging from $\approx 10\,mW$ [284] up to $\approx 100\,mW$ (single hot plate) [283] due to thermal dissipation, such solutions are not well suited for battery-powered remote sensing applications.

Compared to the other integrated systems, this design offers dynamic power consumption, directly proportional to the CNT-FET bias and input signal, i.e., NO_2 gas analyte. Table 3.3 summarizes the performance of this design and a comparison to the SoA signal acquisition ICs for gas sensors. The ASIC is further connected to the CNT-FET nanosensor and exposed to NO_2 analyte and results are presented in chapter 5.
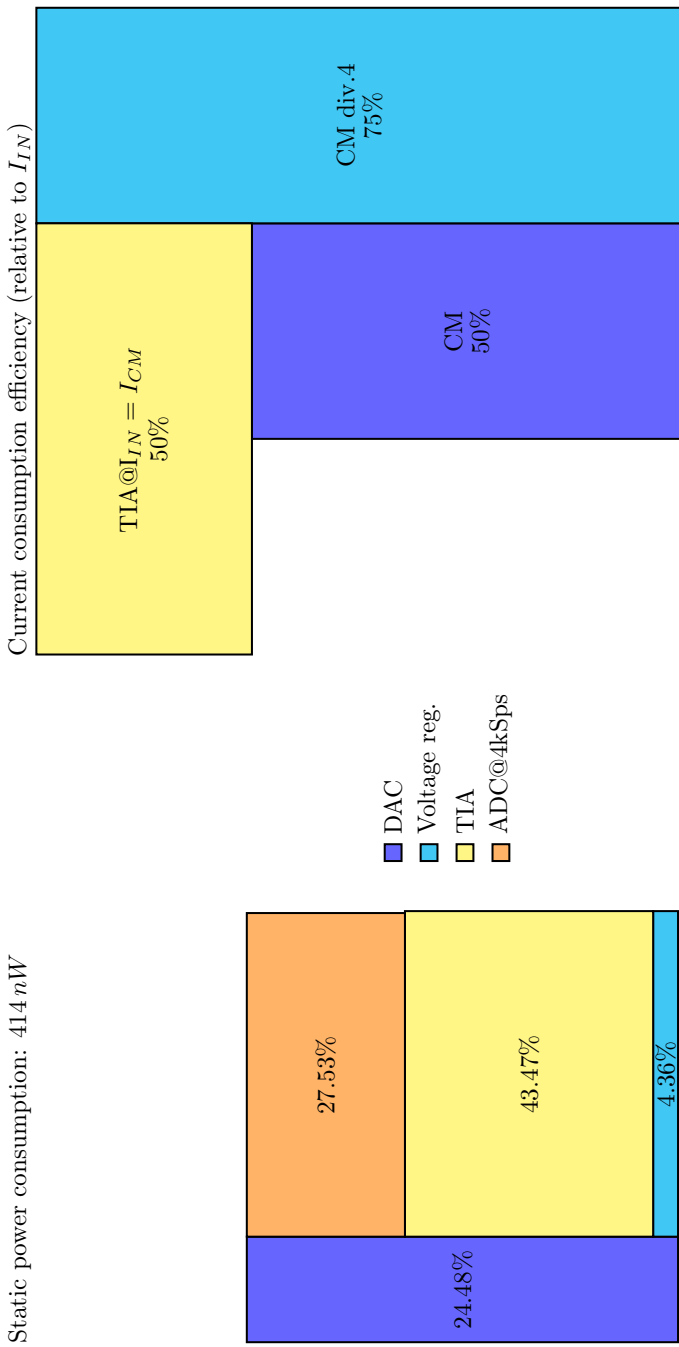
Table 3.2: Static power consumption distribution of the ASIC building blocks together with the dynamic power consumption scaling factor as a function of I_{IN}.

Table 3.3: ASIC Performance Summary and Comparison

Spec./Ref.:	This Work	ISSCC 16 [281]	ISSCC 16 [282]	IEEE SJ06 [283]	JSSC 09 [149]
Supply [V]:	1.8	3	0.5	5	1.2
Power [μW]:	4.04 avg.[a]	930	68000	10^5 (single)	32
Tech. [nm]:	180	350	28	800	180
Detector type:	resistive (CNT)	capacitive (MEMS)	capacitive (NEMS)	reisstive (micro-hotplate)	resistive (CNT)
Detector interface:	6 bit adaptive	10 bit adaptive	10 bit adaptive	N/A	8 bit adaptive
Amplifier:	CT	chopped	lock-in	CT	N/A
ADC:	SAR 9 bit	SAR 10 bit	SAR 10 bit	SAR 10 bit	SAR 10 bit
Channels:	1	1	3	1	1
Sampling freq. [$kSps$]:	2.66	10	2000	N/A	1.83

[a] for sensor power dissipation of 2.43 μW avg.

4 System Measurement Results

This chapter presents extensive CNT-FET nanosensor experimental results acquired with the two different interfacing systems, i.e., the embedded platform and the ASIC. It starts with the CNT-FET device architecture description introducing the transfer steps. The chapter continues with the DC characteristics ID_{CNT}-VGS_{CNT} [83] of particular samples and NO_2 experimental part. This part explores variation parameters, i.e., exposure time, gas concentration, relative humidity, and bias profile of the CNT-FET nanosensor connected to the embedded platform. The results from experiments related to the VDS_{CNT} and VGS_{CNT} CNT-FET nanosensor parameters are used as preliminary data for samples connected to the ASIC toward an optimum sensing performance.

4.1 CNT-FET nanosensor fabrication

The CNT-FET nanosensors samples used in the following experiments were fabricated by Dr. Kishan Thodkar and labeled with KTDS indicative followed by their device number. For fabrication, the devices use the same architecture, and process flow described comprehensively in [83]. The as-grown CNTs are then mechanically transferred to the substrate, comprising of mesa-like source (S) and drain (D) electrodes allowing to assemble the CNTs suspended from the substrate and the gate (G) as already presented in Figure 1.3. The CNT and the substrate form a suspended CNT-FET structure with a channel length of $2.8\,\mu m$ and a gate distance of $1\,\mu m$. A top view of the substrate accommodating up to four devices together with a zoom-in scanning electron microscopy (SEM) image of a typical CNT-FET device is shown in Figure 4.1. The source and drain contacts are metalized before CNT-FET transfer using Cr $(1\,nm)$ and Pd $(40\,nm)$ thermal evaporation. The drain current ID_{CNT} is controlled by the gate located under the suspended structure, as shown in Figure 1.3.
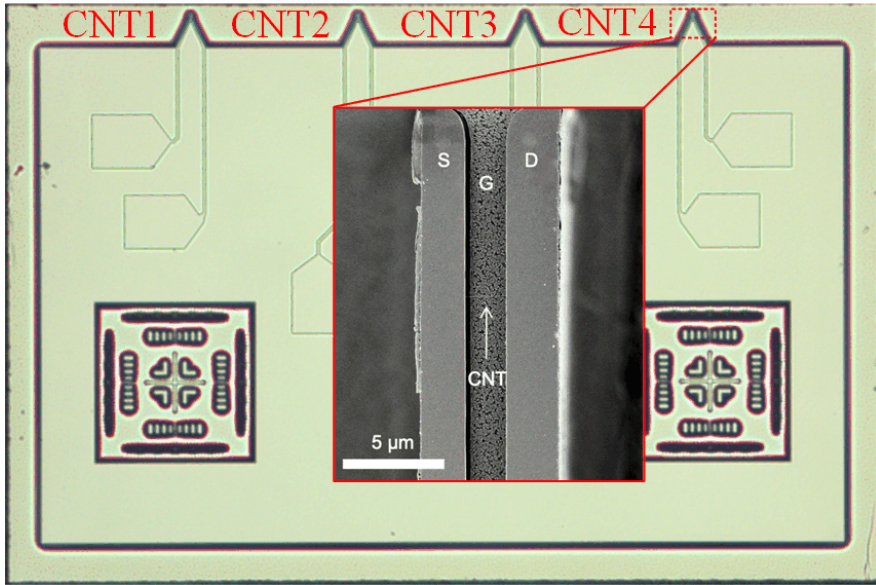
Figure 4.1: Optical image of the substrate, accommodating four devices with a zoom-in scanning electron microscopy (SEM) image highlighting a CNT-FET. Images curtesy of Seoho Jung.

4.2 CNT-FET nanosensor gas kinetics

The mechanism of gas adsorption on the surface of a CNT-FET is an ongoing subject of contention, as presented in the introduction 1.3.3.2. The experimental section of the thesis is confined to a restrictive interpretation of the measurement results due to the lack of a CNT-FET nanosensor compact model. The following paragraphs will provide an outline of nanosensor dynamics as well as a theoretical model that can be employed in this thesis for data analysis and interpretation.

The gas adsorption on the CNT-FET's surface is directly related to the nanosensor kinetics. This is based on Langmuir isotherm [285], which has been adopted by the research group [4]. On many solid-state chemical sensors, the Langmuir adsorption model characterizes the adsorption/desorption behavior of analytes [286][287][288][289], including CNT-FET nanosensor [152][111]. However, for this model to hold, the subsequent assumptions need to be assessed:

- Only monolayer adsorption can be considered such that Langmuir isotherm theory is applicable.

- The nanosensor response needs to be proportional to the surface coverage. This assumption is verified if the characteristics follow the Langmuir theory.

- The binding energy of the analyte and the sticking coefficient does not depend on the surface coverage.

- The change in metal work function, Φ_m, is proportional to the surface coverage. It is assumed to be true despite other sensing mechanisms presented in the introduction chapter 1.3.3.2.

- Possible effects of adsorption on the substrate are negligible. This assumption might contradict other research findings presented in the introduction chapter 1.3.3.2.

- The temperature is constant during the sensing phase. This constraint can be met for measurements in lab conditions only. Otherwise, an external temperature sensor might be used for temperature compensation.

Starting from the Langmuir adsorption isotherm [285], the coverage of an analyte on the CNT-FET nanosensor surface can be described as:

$$\frac{d\theta}{dt} = r_{ads} - r_{des} = K_{ads} \cdot p \cdot (1 - \theta) - K_{des} \cdot \theta, \tag{4.1}$$

where θ describes the number of covered adsorption sites on the surface of the CNT-FET at partial gas pressure p. The $r_{ads} = K_{ads} \cdot p \cdot (1 - \theta)$ represents the rate of analyte adsorption, and $r_{des} = K_{des} \cdot \theta$ the rate of desorption. K_{ads} and K_{des} are the adsorption or desorption constants, respectively. The adsorption constant depends on the sticking coefficient, the molecular cross-section, and the temperature. In contrast, the desorption constant is a function of the attempt frequency (also known as the pre-exponential factor of the Arrhenius equation [290] describing the frequency of the collisions) and the binding energy of the analyte on the surface. Using the boundary condition, $\theta_{(t=0)} = 0$, the solution of Eq. 4.1 can be calculated [4] as:

$$\theta(t) = \theta_\infty \left(1 - e^{\frac{-p K_{ads} t}{\theta_\infty}} \right), \tag{4.2}$$

where θ_∞ denotes the Langmuir isotherm expressed as:

$$\theta_\infty = \frac{K \cdot p}{K \cdot p + 1}, \tag{4.3}$$

where $K = K_{ads}/K_{des}$. This boundary condition is only valid if the CNT-FET nanosensor is reset, where all gas molecules have desorbed. In other

words, before the nanosensor can be used again for sense, it must recover in an environment free of analytes for at least the estimated relaxation time. A set of practical CNT-FET bias experiments have been conducted, and their results are presented in the following paragraphs to explore the sensing, i.e., adsorption and recovery desorption effects.

4.3 Lab gas characterization setup

The experiments were performed in a controlled gas atmosphere in which the CNT-FET nanosensor is exposed to a stable predefined gas concentration. Using the old setup [6], it is possible to apply NO_2 and SO_2 concentrations between $1\,ppb$ and $10\,ppm$ and to vary the relative air humidity between 0 and $90\,\%$. The complete documentation on how to program this gas setup can be found in [291]. More recently, the setup has been updated with a relative humidity (R.H.) [174] and temperature (T) sensor [292] as presented in Figure 4.2.

For the given setup, a high level of reuse is desired. Hence, all parts of the existing setup can be kept in place, except the National Instruments DAQ card (NI PCI-6289) and the low noise current-to-voltage amplifier (Femto DHPCA 100). The embedded sensing platform presented in chapter 2 or the ASIC presented in chapter 3 has been connected to the existing output gas line with the help of a test chamber. In this case, the data of the gas setup [291] and the new acquisition systems under test can be correlated by their timestamps, which are extracted and used when plotting experimental data.

4.4 Embedded platform NO$_2$ measurement results

The FSM has been programmed to acquire consecutive samples with a temporal delay of $1/3$ seconds in between for the current set of experiments. Denoted as τ in [4], this sampling period has been chosen due to strong signal correlation, given by the $1/f$ noise, and mitigating the white noise with the LPF effect. For the same CNT-FET devices, the influence of the observation window and the sampling frequency has been investigated in a previous work which can be found in [4].
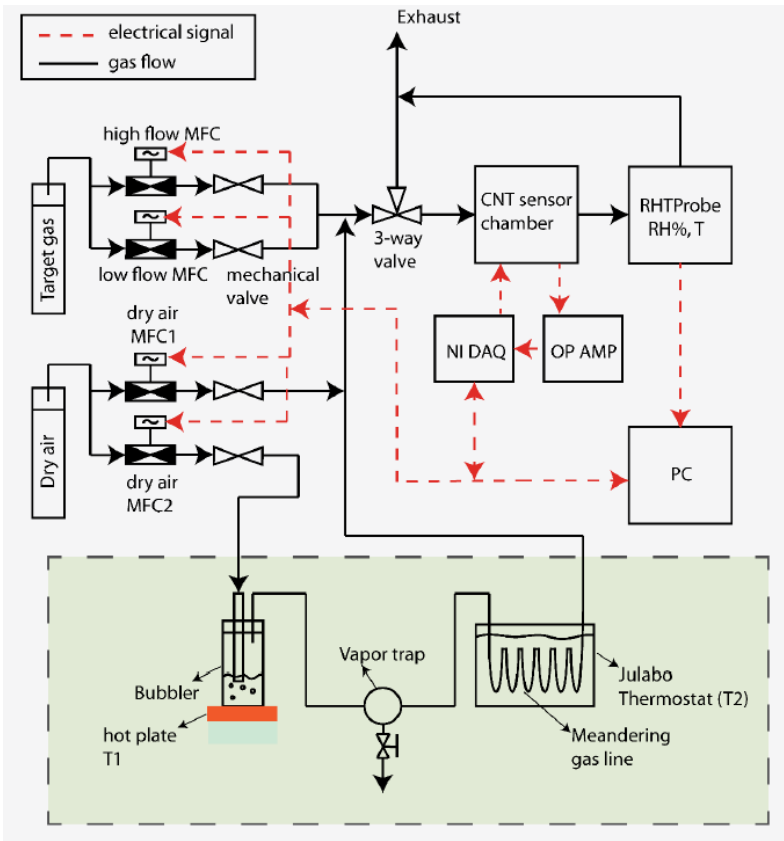
Figure 4.2: Overview of the CNT-FET gas sensor characterization setup. Note: the black lines denote the gas flow scheme the red dotted lines indicate the electrical connections. The grey area in the image was redrawn from S. Eberle's Ph.D. thesis 2019 [6]. The green region is the updated addition along with the R.H., and T probe installation [9]. Illustration courtesy of Dr. Kishan Thodkar.

4.4.1 KTDS15 CNT-FET nanosensor characterization

A pre-characterization of the CNT-FET nanosensors needs to be performed before running experiments with exposure to NO_2 gas analyte. In Figure 4.3.a the transfer characteristic of KTDS15 device, mounted in the test chamber under atmospheric conditions, is presented at different VDS_{CNT} bias levels. The CNT-FET nanosensor shows no pronounced hysteresis, which is expected for suspended CNT-FET device architecture [79]. The output characteristics of the CNT-FET nanosensor is presented in Figure 4.3.b, wherein the current values are acquired at different VGS_{CNT} bias levels.

The current curves show two different operational regions of the CNT-FET nanosensor:

1. A linear region where the CNT-FET device current is linearly proportional to the applied bias and can be used for sensing.

2. The CNT-FET device self-heating [79] region, which can be observed for elevated bias levels and is used for sensor reset.
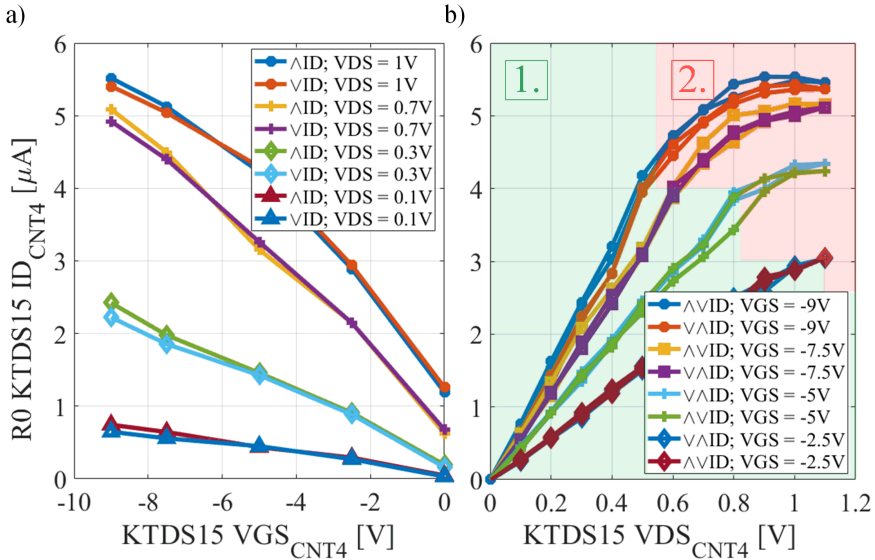
Figure 4.3: KTDS15 CNT4 device: a) transfer characteristics VDS_{CNT} bias showing no substantial hysteresis; b) output characteristics of the same device at different VGS_{CNT} bias. Here, R0 represents the number of the experiment and CNT4 refers to channel 4 of the substrate carrier.

Self-heating (SH) is an undesired Joule effect in the case of MOS-FETs and has to be minimized [293][294] to keep the device within the SOA area when higher currents are passing through. In contrast, this self-heating effect promotes faster desorption of the gas molecules from the CNT-FET nanosensor surface, thus shortening the transition between sensor operation and reset state [80] [295]. However, the heating effects of elevated voltage levels have to be utilized with care for each CNT-FET nanosensor individually due to their device-to-device conductance variation [83]. The energy dissipated in the CNT-FET nanosensor can lead to disruptive effects when used over an extended period. Amongst them, the main limitations of this application feature are:

- Chemical oxidation in presence of O_2

- Device and contact degradation

- Irreversible damage of the device

The experimental determination for the KTDS15 device optimum bias level is presented in the next paragraph.

4.4.2 Experimental determination of bias voltages for KTDS 15 device sensing and reset

A first step, after DC pre-characterization, is to determine the optimum VDS_{CNT} for NO_2 gas sensing routine. This experiment was performed by successively exposing the CNT-FET nanosensor to a constant, mid-range, NO_2 concentration of $100\,ppb$, followed by a reset phase in dry air. The result of this experiment is presented in Figure 4.4.a.
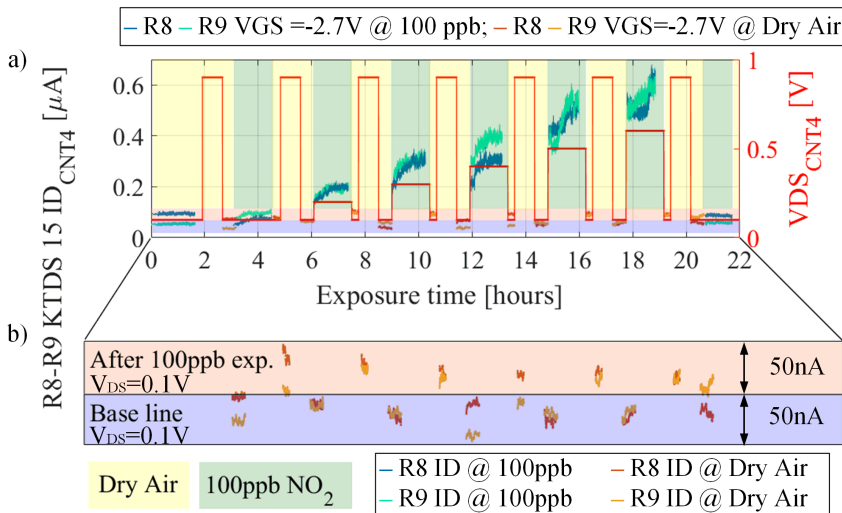
Figure 4.4: R8-R9 KTDS15 CNT4 device: a) signal response at $100\,ppb\ NO_2$ constant VGS_{CNT}, and different VDS_{CNT}; b) magnification of the baseline current after reset phase (not shown), and after $100\,ppb\ NO_2$ analyte exposure.

As a result, the current signal value and its corresponding slope increase with VDS_{CNT} values up to $450\,mV$. An increasing current is noticeable for the bias values with $VDS_{CNT} > 450\,mV$, but the corresponding initial

slope decreases. The latter might be due to the self-heating effect induced by the rising VDS_{CNT}, which initiates the desorption of NO_2 molecules from the CNT-FET nanosensor surface. In the last self-heating experiments [4], a temperature of $\approx 70\,°C$ was observed to trigger NO_2 desorption. However, an on-chip heater was utilized during the experiment, whereas in the experiment presented in Figure 4.4.a, the local temperature of the CNT-FET was modulated by increasing the VDS_{CNT} of the nanosensor. These findings provide an insight into the influence of temperature on the CNT-FET nanosensor response and thermal binding kinetics, K_{ads} and K_{des}, of the NO_2 gas analyte. Moreover, one can observe an increased noise level of the current signal for $VDS_{CNT} > 450\,mV$, an effect that decreases the nanosensor's SNR [4]. Note: the sensing results were acquired for pulsed VGS_{CNT} bias as suggested in [6] (in this thesis with $1\,second$ period, and $70\,\%$ duty cycle as introduced in Figure 2.3), and extracted at $VGS_{CNT} = -2.7\,V$. For consistency, this experiment has been conducted twice, and as a consequence, $VDS_{CNT} < 450\,mV$ are used further for the steepest slope, lower noise, and robust results when operating the CNT-FET nanosensor in sensing mode.

A second experimental step would be to evaluate the efficiency of the CNT-FET nanosensor reset phase. For this purpose, a zoom-in of the baseline and "after exposure" bands are shown in Figure 4.4.b. The measurement baseline is defined as being the nanosensor current level after a reset phase performed with the help of elevated bias voltage, $VGS_{CNT} = -7.5\,V$ and $VDS_{CNT} = 900\,mV$, which leads to the self-heating as shown in Figure 4.3. The effectiveness of the CNT-FET reset can be quantified by evaluating the spread of the current around the baseline after a self-healing phase. After repetitive exposure to $100\,ppb$ NO_2 gas concentration, the pink band highlights the gas molecules' contribution as a current offset. A proper reset phase would lower the current level (at the same bias conditions) and bring it back to the baseline, i.e., the blue band in Figure 4.4.b. For example, a high power dissipated in the CNT-FET during the reset phase would lead to a baseline current undershoot. A low power reset would not change the current offset of the concentration exposure. As a result, a CNT-FET nanosensor bias of $VGS_{CNT} = -7.5\,V$ and $VDS_{CNT} = 900\,mV$ is appropriate in the reset phase for a baseline current level dispersion of about $50\,nA$.

Moreover, it can be observed that the current level remains within $50\,nA$ relative value after $100\,ppb$ NO_2 exposure regardless of VDS_{CNT} amplitude applied during exposure. This suggests that the number of adsorption states is constant with VDS_{CNT}, and only the slope (speed) can be influenced by its value. This experiment has been repeated twice for consistency of the mentioned observation. However, the sensor reset time of $45\,minutes$ has been kept constant in this experiment. The reset energy used in this sensor can be further optimized and is presented in the following experiment.

4.4.3 Experimental determination of reset time for KTDS 15 device

The reset phase duration and bias levels are correctly tuned to when the same baseline current level is reached after NO_2 gas exposure. After fixing the bias levels for self-heating, of $VGS_{CNT} = -7.5\,V$ and $VDS_{CNT} = 900\,mV$, an additional experiment has been conducted to determine the optimum reset phase duration as presented in Figure 4.5.
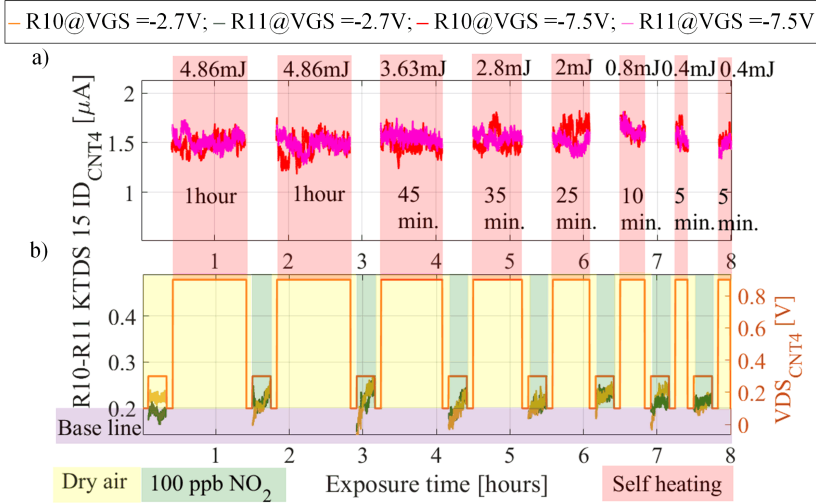
Figure 4.5: R10-R11 KTDS15 CNT4 device experimental results for a) signal response at $100\,ppb\ NO_2$ constant VGS_{CNT}, and VDS_{CNT}; b) self heating current levels for variable reset period and the corresponding dissipated energy.

The nanosensor has been successfully exposed to $100\,ppb\ NO_2$ at a constant period and bias level during the sensing phase. In contrast, during the reset phase, the period has varied from $1\,hour$ down to $5\,minutes$ at a constant CNT-FET power dissipation of about $1.35\,\mu W$ as presented in Figure 4.5.a Consequently, after each reset phase, the resulting current level is evaluated concerning the nanosensor's baseline. As shown in Figure 4.5.b, a long reset phase, i.e. one hour, would lead to a baseline current undershoot. In contrast, the short reset phase, i.e., five minutes, would lead to incomplete desorption after exposure to the gas concentration. This experiment has been repeated twice. Energy dissipation of $3.63\,mJ$ down to $0.8\,mJ$ would be sufficient for resetting the nanosensor after a midrange gas concentration, i.e., $100\,ppb\ NO_2$ exposure. A conservative reset period of $45\,minutes$ dissipating $3.63\,mJ$ of energy has been chosen in the following experiments.

4.4.4 Experimental results with NO$_2$ exposure of KTDS15 device

The experimental evaluation of the KTDS15 device with the help of its baseline led to a bias of $VGS_{CNT} = -2.7\,V$ and $VDS_{CNT} = 0.1\,V$ in sensing, and a sensor recovery window of $45\,minutes$ at an elevated bias of $VGS_{CNT} = -7.5\,V$ and $VDS_{CNT} = 0.9\,V$ in reset state.

In the next experiment, the KTDS15 nanosensor was exposed to NO_2 gas concentrations of $[0, 200, 150, 100, 50, 10, 1, 0, 0]\,ppb$ under constant dry air-flow. The gas concentration steps are chosen to start from high to low NO_2 values preceded by dry air exposure for two main reasons: first, to define a baseline of the CNT-FET nanosensor drain current in the absence of NO_2 gas, and second, to highlight the effectiveness of CNT-FET nanosensor reset by evaluating this baseline. The results of this experiment are presented in Figure 4.6 and show a sensitive, current response of the CNT-FET nanosensor to NO_2 exposure. For the CNT-FET nanosensor reset, a SH operation was performed after each concentration of NO_2 exposure.
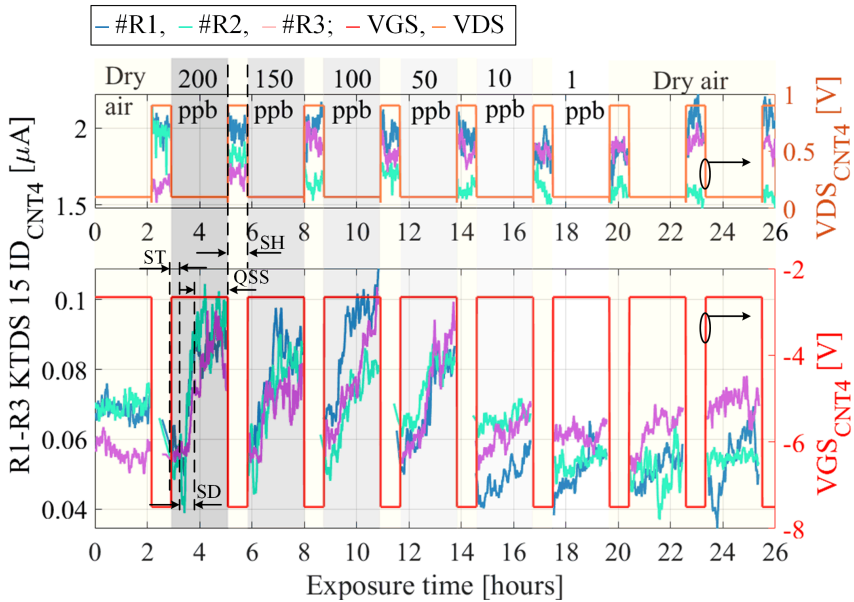
Figure 4.6: KTDS15 CNT4: three superimposed data sets with averaged CNT-FET current measurement (y-axis split in top part used for nanosensor reset current values and the bottom for representing sense current samples) of the same experimental design, i.e., exposure to a decreasing NO_2 gas concentration from 200 to $0\,ppb$.

As observable in the top part of the Figure 4.6, the CNT-FET nanosensor SH effect enables an accelerated gas desorption mechanism. The nanosensor current is saturated in this bias region, which induces the SH onset, resulting in a negative-differential conductance behavior [79] as shown in Figure 4.3. The bottom part of the Figure 4.6 shows the CNT-FET drain current values when exposed to NO_2. The experimental sequence was repeated thrice at the same bias levels and NO_2 gas concentrations for consistency. Significant repeatability and the effective sensor reset between the measurements data sets [1, 2, 3] are observable in Figure 4.6.

As mentioned, FSM has been programmed for this measurement set to acquire consecutive samples with a temporal delay of $\tau = 1/3\,seconds$. This sampling value has been chosen due to the strong signal correlation of the 1/f noise and mitigating the white noise with the LPF effect. For the same CNT-FET devices, the influence of the observation window and the sampling frequency has been investigated in a previous work which can be found in [4]. Depending on the application requirements, the sampling rate of the embedded platform can be increased up to $3.125\,kSps$, which offers sufficient BW for gas sensing applications involving complex data post-processing.

4.4.5 Relative humidity cross-sensitivity

The humidity cross-sensitivity experimental result of the KTDS15 nanosensor has been investigated as the last experiment. This CNT-FET has been fabricated by using the dry transfer technique [83]. And in the absence of residues or defects, water molecules' adsorption on the CNT-FET nanosensor's hydrophobic surface is highly reduced. This technique minimizes the cross-sensitivity of the nanosensor's response to humidity, as demonstrated in [111]. The experimental results with the KTDS15 CNT-FET nanosensor are presented in Figure 4.7.

In Figure 4.7 the influence of relative humidity pulses has been evaluated in comparison to dry air conditions. Reduced cross-sensitivity to humidity is observable for gas flow conditions with 0 and $100\,ppb$ NO_2 gas concentration. One can observe similar current response in the $NO_2 - D.A.$ region compared to the $NO_2 - R.H.$ region. The same observation can be made for the CNT-FET current levels in the absence of the NO_2 analyte for $D.A.$ and $R.H.$ respectively. As presented in chapter 1.2.1.4 the dry-transfer technique utilized to fabricate the suspended CNT-FET nanosensors have demonstrated insensitivity to relative humidity [81]. The dry-transfer technique used to fabricate these ultra-clean CNT nanosensors facilitate a residue-free approach avoiding charge traps at the oxide/CNT interface. This has immensely helped in suppressing electrical hysteresis commonly observed during the electrical
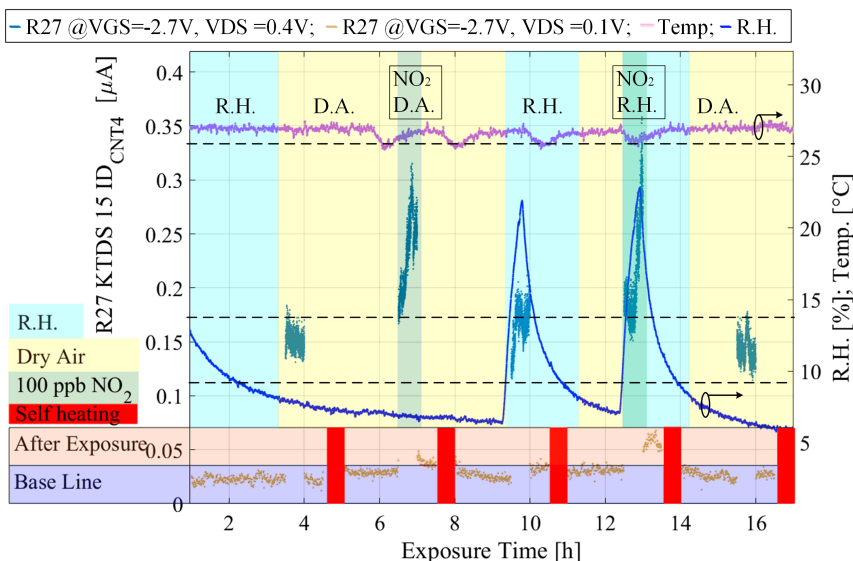
Figure 4.7: R27 KTDS15 CNT4 device: CNT-FET nanosensor signal response
at 0 and 100 ppb NO_2 gas concentration in the absence and presence
of humidity.

field-effect characterization of on-substrate/non-suspended CNT-FET nano-
sensors [111]. After investigating and presenting humidity cross-sensitivity,
the KTDS15 device stopped working during the subsequent experiment, i.e.,
R28. It likely happened due to degradation [152] or an ESD event. Consid-
ering the high number of experiments, i.e., 29 conducted over 36 days, this
should have been expected.

4.5 ASIC NO₂ measurement results

4.5.1 KTDS19 CNT-FET nanosensor characterization

Instead, a similar devices, KTDS 19-22-23, have been used for further NO_2
experiments using the ASIC as a signal acquisition front-end. The same pro-
cedure has been applied and pre-characterisation measurements results with
the ASIC as a front-end are presented in Figure 4.8.a for the CNT-FET trans-
fer characteristic and Figure 4.8.b for output characteristic respectively.

As a next step, the experimental determination of the optimum bias levels,

a)

b)
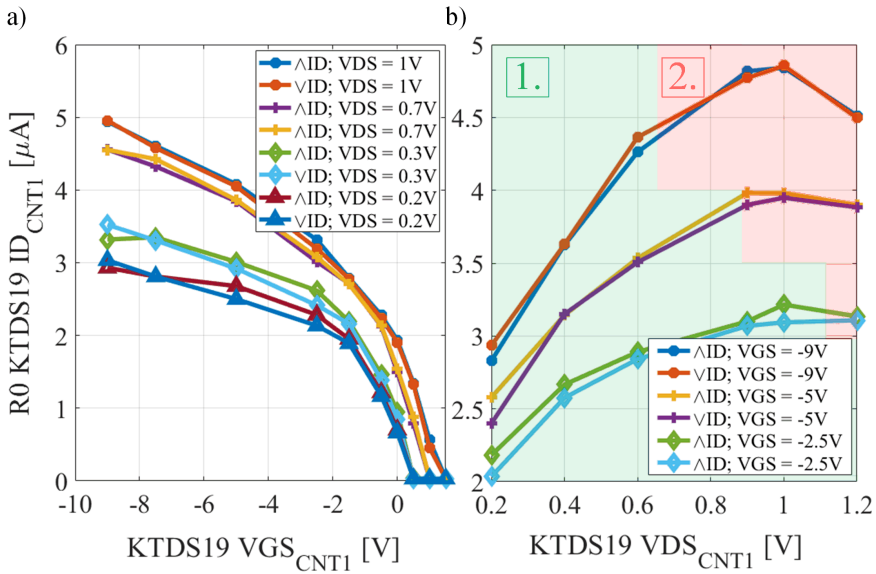
Figure 4.8: KTDS19 CNT1 device: a) transfer characteristics VDS_{CNT} bias showing no substantial hysteresis; b) Output characteristics of the same device at different VGS_{CNT} bias. Note: R0 represents the experiment number and CNT4 refers to channel 4 of the substrate carrier.

i.e., VGS_{CNT} and VDS_{CNT}, has been found by following the same procedure as in 4.4.2 and 4.4.3.

4.5.2 Experimental results with NO_2 exposure of KTDS 22-23 device

Finally, a CNT-FET nanosensor was connected to the IC and exposed to NO_2 gas concentrations of [0, 10, 20, 50, 100, 200] under constant 50% R.H. airflow. The same measurement procedure has been used in 4.4.4. The experiments in Figure 4.9 present reproducible current slopes of the CNT-FET nanosensor to NO_2 exposure, demonstrated by two repetitive measurements (R1 and R2) of the same device. The bottom part of Figure 4.9 shows that the CNT-FET drain current values are biased at a $VGS_{CNT} = -0.3\,V$ and $VDS_{CNT} = 0.2\,V$ and exposed to NO_2 gas analyte. The top part of Figure 4.9 shows the sensor reset window at an elevated bias voltage, $VGS_{CNT} = -7.5\,V$ and $VDS_{CNT} = 0.65\,V$, after each exposure sequence. For this particular device, the bias region, in which the CNT-FET nano-

sensor current is saturated, induces the SH onset resulting in a negative-differential conductance (NDC) behavior. The SH operation was performed under constant 50% R.H. airflow after each NO_2 concentration exposure for the CNT-FET nanosensor to reset.
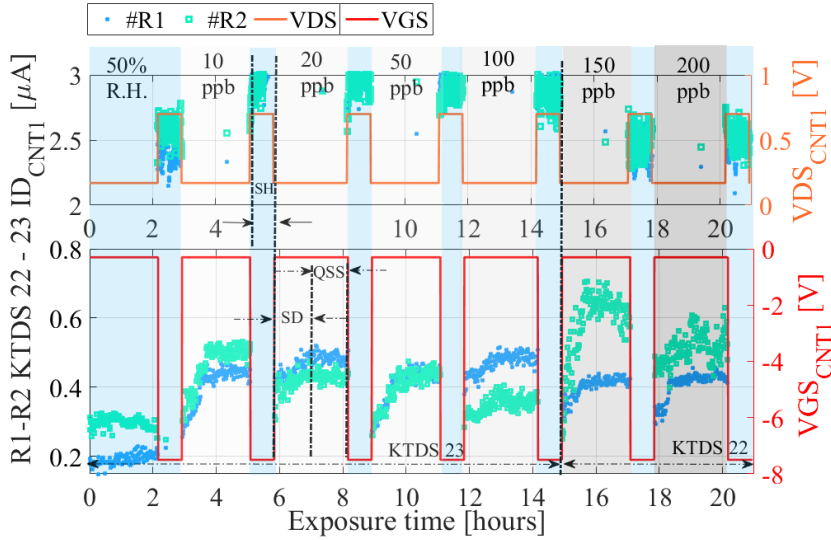
Figure 4.9: KTDS 22-23 CNT1: two superimposed data sets with CNT-FET nanosensor current measurement of the same experimental design, i.e., exposure to a decreasing NO_2 gas concentration from 200 to 0 *ppb*.

4.6 Power consumption

As presented in chapter 3.4.2.8, the power consumption of the ASIC measurement system is dynamic and depends on the CNT-FET nanosensor device characteristics, NO_2 analyte concentration, the applied bias level, and ADC sampling frequency. Based on measurements presented in Figure 4.9 (using an external VGS_{CNT}) the CNT-FET nanosensor draws $3.24\,\mu W$ of power when operating in the self-heating regime and $1.62\,\mu W$ when operating in sensing mode at $0\,ppb$ NO_2. This gives the CNT-FET nanosensor an average power consumption of $2.43\,\mu W$. The total power consumption for the entire sensing system operated as in Figure 4.10.a. is $4.04\,\mu W$ as shown Figure 4.10.b., when supplied at $1.8\,V$ and an ADC sampling rate of $2.66\,kSps$ the CNT-FET sensor biased at $VDS_{CNT} = 0.2\,V$ at $200\,ppb$ NO_2.

Compared with the power consumption of the DDC114 presented in Fig-
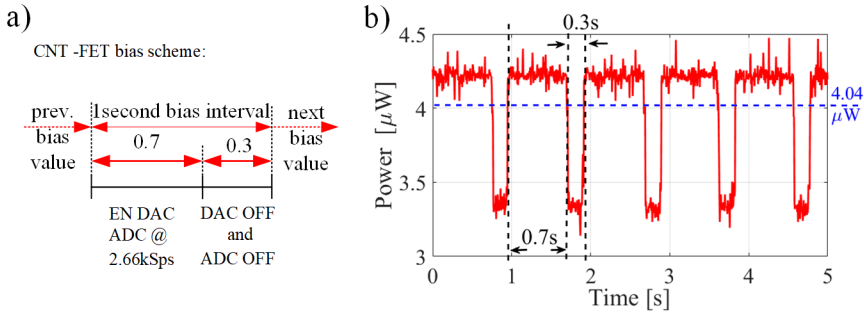
Figure 4.10: a) Custom bias timing scheme for CNT-FET nanosensor and b) the corresponding power consumption of the sensing system.

ure 2.15b, at a similar sampling rate, i.e., $2.5\,kSps$, the ASIC power consumption is three thousand times lower, which also includes the drain bias block for the CNT-FET nanosensor.

4.7 Chapter summary

An application of the embedded platform, presented in chapter 2, has been demonstrated by integrating an ultra-sensitive CNT-FET nanosensor. A reproducible CNT-FET nanosensor response to NO_2 exposure (R1, R2, R3) was demonstrated down to $1\,ppb$, including a Self-Heating (SH) reset after each concentration of NO_2 exposure. The user-defined software-based solution allows for simple custom, bias periods, and levels, thus offering flexibility and further trade-offs between functionality and energy efficiency. The humidity cross-sensitivity experimental result of the CNT-FET nanosensor has also been investigated.

Further, the proposed ASIC described in chapter 3 successfully interfaces with the CNT-FET nanosensor and achieves similar sensing performances. The experiments present reproducible current slopes of the CNT-FET nanosensor to NO_2 exposure, demonstrated by two repeated measurements (R1 and R2) of two different devices, i.e., KTDS 22 and KTDS 23. The ASIC is more compact than the embedded system and consumes less power. Moreover, its power consumption is dynamic and directly proportional to the NO_2 concentration in combination with the CNT-FET nanosensor. Those features make it suitable for environmental monitoring and health protection applications.

Based on the experiments of this chapter, the next chapter presents the sensor signal evaluation for the embedded platform and ASIC from the perspective of other research publications, start-up prototypes, and commercial solutions.

5 CNT-FET Nanosensor Signal Evaluation

In this chapter, the experimental data are post-processed with the help of readout algorithms implemented in Matlab, and the CNT-FET sensing performance is assessed. The chapter introduces two different sensing regimes, for which the corresponding advantages and drawbacks are highlighted [3]. The chapter continues with two different strategies for sensor signal evaluation involving readout algorithms, i.e., slope detection and quasi-steady-state regime [4]. As a performance FoM, the limit of detection (LOD) is introduced to evaluate and compare the CNT-FET sensing performance when connected to sensor interfacing systems, i.e., the embedded sensing platform and the dynamic signal acquisition ASIC. For the standalone CNT-FET LOD performance, one could refer to [6] [296] research results of the group. The last part of this chapter presents the system's performance in the context of air quality monitoring applications and compares it with other research, start-up prototypes, and commercial implementations currently available.

5.1 CNT-FET sensing regimes

Following the sensor kinetics established in chapter 4.2, the current response to a specific gas concentration can be divided into a transient and a quasi-steady-state part [4]. The following section uses these sensing regimes to extract NO_2 gas concentration from the measured current levels. A typical response of a CNT-FET nanosensor when exposed to NO_2, is shown in Figure 4.6. After its transient state, the current is expected to converge to a constant value, the so-called steady-state current. In reality, the current is never completely steady; indeed, it tends to drift away as the flicker noise series progresses with time [4]. For consistency, experimental results of NO_2 gas response for KTDS15, KTDS22, and KTDS23 CNT-FET nanosensors are used for data analysis.

5.1.1 CNT-FET NO$_2$ quasi-steady-state response

One can observe a transient state, followed by a region where the current is expected to converge to a constant value, i.e., steady-state current in Figure 4.6. The main drawback of sensing in the quasi-steady-state regime is the long waiting until this state is reached, where θ_∞ denotes the Langmuir isotherm expressed as:

$$\theta_\infty = \frac{K \cdot p}{K \cdot p + 1},\tag{5.1}$$

This equation demonstrates the non-linearity of the steady-state sensitivity due to the saturation behavior of the Langmuir isotherm.

5.1.2 CNT-FET NO$_2$ transient response

For Figure 4.6, under the same initial conditions, the initial-slope signal can be simply written,

$$\frac{d\theta(t)}{dt}\Big|_{t=0} = K_{ads} \cdot p,\tag{5.2}$$

wherein θ represents the CNT-FET nanosensor surface coverage, p is the analyte concentration or partial pressure and K_{ads} is the adsorption coefficient. This expression highlights a first-order proportionality factor between the initial slope and the analyte gas concentration of the Langmuir model, which becomes highly nonlinear towards the quasi-steady state. In other words, it can be stated that initial-slope sensing has several advantages that can be explored when performing sensing with the CNT-FET:

1. First-order linear fit

2. Faster response time (no need for device stabilization)

3. Measurement of higher concentrations beyond the dynamic range

From this point of view, transient sensing may seem favorable. Preliminary work analyzing the characteristics of transient sensor response was carried out in [4]. In the next paragraph, both methods' advantages and drawbacks when sensing are explored.

5.2 Experimental determination of LOD and R^2

The Langmuir model will be assumed to be sufficient to demonstrate the performance of the experimental data since no novel gas response models were developed in the scope of this thesis. For this purpose, two parameters, i.e., the limit of detection (LOD) and R^2 are introduced in the following paragraphs.

5.2.1 Limit of detection (LOD)

The limit of detection (LOD) has been defined, and it indicates the lowest concentration of an element that can be consistently identified with a specific analytical procedure [297]. Some other organizations, i.e., ISO [298] have tried to standardize the LOD definition. This subject is still a matter of scientific debate. However, in simple terms, the LOD is the lowest concentration value resulting from the measurement of a sample containing the analyte, i.e., NO_2 that can be discriminated from a measurement of a sample not containing the component, i.e., dry air [299]. The LOD used in this thesis to evaluate the performance of the CNT-FET nanosensor can be expressed as:

$$LOD = 3\sigma \cdot \frac{noise_{RMS}}{slope},$$

(5.3)

where the *slope* is for low gas concentrations, i.e., 0 to 50 *ppb*. The major challenge here is obtaining reliable and repeatable results with a limited number of CNT-FET nanosensors for applying statistics. For the low number of samples, few complex methods to do statistics are recommended [229]. However, those are beyond the scope of this thesis and would require extensive knowledge of statistics. Moreover, they need adaptation and standardization for the current research.

5.2.2 Coefficient of determination: R^2

For the considered Langmuir model, the linearity of the initial slope signals has to be validated by the practical experiments presented in chapter 4. For this purpose, the coefficient of determination, R^2, [300] is introduced. The coefficient of determination is a statistic that indicates how well the initial slope fits the model. R^2 is a statistical measure of how well the regression

line approximates the observed data in the context of linear regression [301], and it can be represented as:

$$R^2 = 1 - \frac{sum\ squared\ regression\ (SSR)}{total\ sum\ of\ squares\ (SST)} = 1 - \frac{\sum_{i=1}^{n}\left(y_i - \hat{y}_i\right)^2}{\sum_{i=1}^{n}\left(y_i - \bar{y}_i\right)^2}, \quad (5.4)$$

where $\hat{y}$ are the regression line predicted values of y and $\bar{y}$ represents the mean of all the y values, i.e. $\frac{\sum_{1}^{n} y}{n}$. In the case of the transient response, it shows how linear is the slope of the CNT-FET nanosensor output current when exposed to the NO_2. Moreover, it should be stated how the linear response degrades towards the highly non-linear quasi-steady-state region after long transients and at high analyte concentrations, respectively.

5.3 Sensor signal evaluation acquired with the embedded platform

The experiments presented in Figure 4.6 are used for observing the CNT-FET nanosensor current evolution over time, and three different regions within a NO_2 exposure pulse can be highlighted:

- Settling time (ST) of 20 $minutes$

- Transient or slope detection (SD) region from five to 20 $minutes$

- Quasy steady state (QSS) during the last 5 $minutes$

5.3.1 Transient slope detection SD signal response

According to this model, the initial slope of the current signal dependency upon gas concentration can be expressed as in Eq. 5.2. This shows the advantage of the initial slope signal, which is linearly proportional to the gas concentration under evaluation. An ST of 20 $minutes$ was considered after the NO_2 gas flow was started, as depicted in Figure 4.6. After the ST, the nanosensor's initial slope, SD response is investigated at various time windows ranging from five up to 20 $minutes$. In Figure 5.1, the initial slope of the CNT-FET nanosensor current response during the first 12 $minutes$ of NO_2 exposure in the SD region is presented. Good sensor linearity can be observed within this time window, evaluated by the R^2 coefficient. The

error bar length highlights the total electronic noise, i.e., the noise of the CNT-FET nanosensor and the embedded platform. The spread between the error bars at a given gas concentration represents the CNT-FET nanosensor response variation between experiment repetitions R1 to R3.
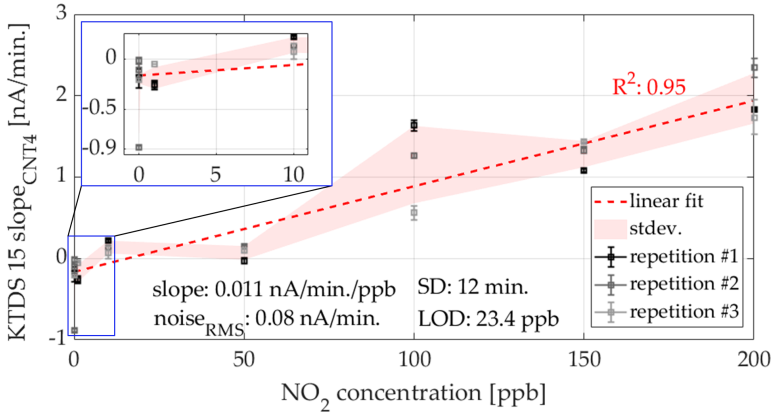
Figure 5.1: The current slope of the first $12\,minutes$ transient CNT-FET nanosensor response. Inset: Magnified transient response (blue-dotted square) of the nanosensor from 0 to $10\,ppb$. Open Access figure adapted from the supplement of [3] published under the terms of Creative Commons CC BY license.

Using the linear fit shown in Figure 5.1 as the device calibration curve and including the resulting error bars as being the noise of the three acquired samples, the LOD can be determined as proposed in 5.2.1. Here, the $noise_{RMS}$ is calculated as the RMS value of the slope's standard deviation across individual current signal response samples at $[10, 1, 0]\,ppb\,NO_2$ concentration. The shaded area, i.e. $stdev.$, of Figure 5.1 illustrates the standard deviation around the average current value for all measurement data sets $[1, 2, 3]$ at each gas concentration. Using the data and their respective fits, as shown in Figure 5.1, the LOD limit values are calculated as:

$$LOD_{SD} = 3 \cdot \frac{noise_{RMS}}{slope} \approx 23\,ppb \qquad (5.5)$$

Each data point represents an average and the standard deviation of 32 samples acquired at fixed bias conditions of $VDS_{CNT} = 0.1\,V$, and $VGS_{CNT} = -2.7\,V$. Further extractions of the LOD and R^2 vs. the time window size and CNT-FET bias are detailed in 5.3.3.

5.3.2 Quasi-steady-state QSS signal response

In comparison, the result presented in Figure 5.2 shows the data from Figure 4.6 denoted as QSS, wherein the average steady-state current response during the last $5\,minutes$ of the two hours NO_2 exposure is evaluated as CNT-FET nanosensor sensing response.
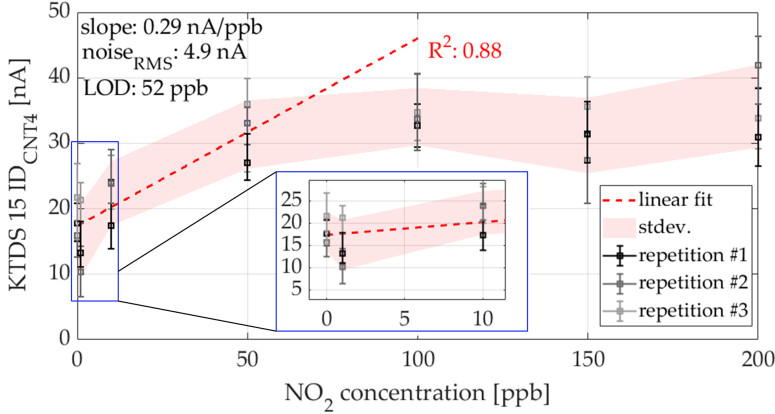
Figure 5.2: The CNT-FET nanosensor's last five-minute quasi-steady-state (QSS) response when exposed to NO_2 gas concentrations Inset: Magnified QSS (blue square) of the nanosensor from 0 to $10\,ppb$. Open Access figure adapted from supplement of [3] published under the terms of Creative Commons CC BY license.

Using the same procedure as in section 5.3.1 with data from Figure 5.2, the LOD for QSS signal response can be derived as:

$$LOD_{QSS} = 3 \cdot \frac{noise_{RMS}}{slope} \approx 52\,ppb \qquad (5.6)$$

Here the classical approach of SS or QSS, wherein the Langmuir isotherm flattening is observable in Figure 5.2 is inferior in terms of LOD and R^2 compared to SD, especially at higher gas concentrations due to the increased surface coverage [4].

5.3.3 CNT-FET LOD and R^2 bias dependency

The reported response time of SD $= 12\,minutes$ corresponds to LOD=$23\,ppb$ $(3\,\sigma)$ when averaging $3\,Sps$ and achieves the highest linearity evaluated with the help of the R^2 linear fit parameter, as presented in Figure 5.3.a. The LOD can be improved to $18.2\,ppb$ for the same SD by lowering the sampling rate with slightly less linearity. The SD time can be decreased further down to $6\,minutes$ with a LOD of $84\,ppb$ (3σ) and substantially less linearity. The importance of the averaged of samples is visible at a higher VGS_{CNT} bias, as presented in Figure 5.3.b, where the CNT-FET nanosensor current exhibits more noise but steeper slope, achieving $25\,ppb$ (3σ) for SD $= 7\,minutes$ by sacrificing the CNT-FET sensor linearity to a corresponding R^2 of 0.84.
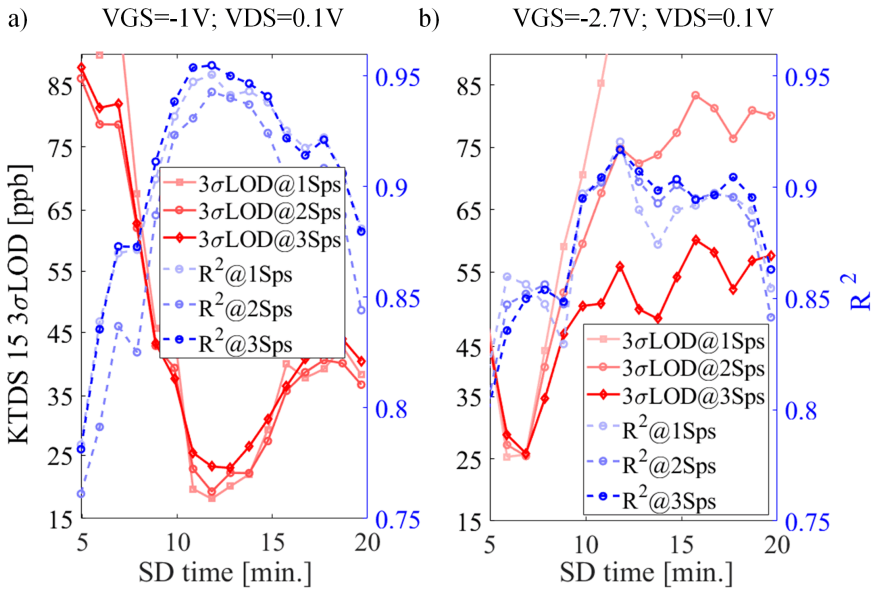
Figure 5.3: LOD and R^2 coefficient as a Slope Detection (SD) time window function for: a) $VGS_{CNT} = -1\,V$ and b) $VGS_{CNT} = -2.7\,V$ with a common $VDS_{CNT} = 0.1\,V$, when 1 to $3\,Sps$ are acquired and averaged. Figure a) is adapted from open access supplement of [3] published under the terms of   Creative Commons CC BY license.

It can be concluded that the KTDS15 CNT-FET can resolve concentrations of NO_2 below $23\,ppb$ when operated in pulsed SH and SD by the embedded platform. It has been highlighted that the initial slope sensing based on SD can dramatically decrease the response time, offering better linearity and dynamic range.

5.4 Sensor signal evaluation with the ASIC

Based on the raw data from Figure 4.9, the initial slope of the CNT-FET nanosensor current response during $18\,minutes$ of NO_2 exposure at the beginning of the SD region (here ST has been shorten to $5\,minutes$) is shown in Figure 5.4. Good linearity of the initial slope can be observed within this time window where the $LOD = 18.6\,ppb\;(3\,\sigma)$ is calculated as in Eq. 5.3. Here, the $noise_{RMS}$ is calculated as the RMS value of the slope's standard deviation across individual current signal response samples (R1; R2) at 50% R.H. airflow.
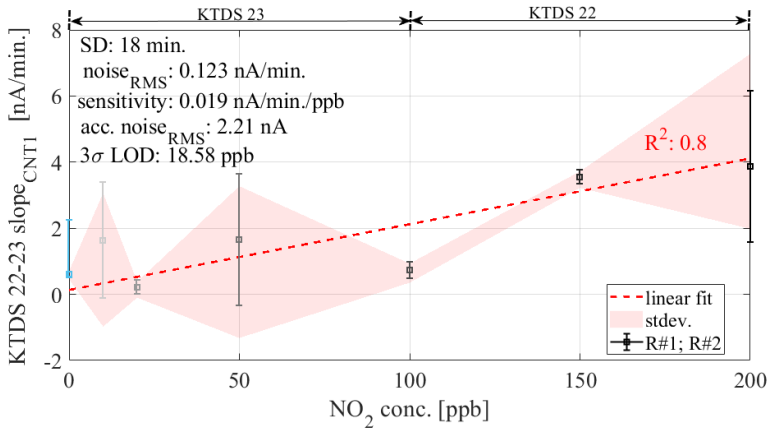
Figure 5.4: The current slope, SD, of $18\,minutes$ transient CNT-FET nanosensor response. Note: The error bar length highlights the total electronic noise (i.e. noise of the CNT-FET nanosensor and the CMOS IC) including the NO_2 target concentration inaccuracy over exposure time and distinct measurements (R1 and R2) of KTDS22 and KTDS23 CNT-FET nanosensors.

5.4.1 CNT-FET LOD and R² bias dependency

The response time of $18\,minutes$ can be decreased further down to $12\,minutes$, as presented in Figure 5.5.b with a LOD of $30\,ppb\;(3\,\sigma)$ for a different bias level of $VGS_{CNT} = -0.1\,V$; $VDS_{CNT} = 0.2\,V$ achieving a slightly decreased linearity to a corresponding R^2 of 0.75. The importance of the VGS_{CNT} bias point is presented in Figure 5.5 where the LOD and R^2 tradeoff as a function of SD time and sampling rate are presented.
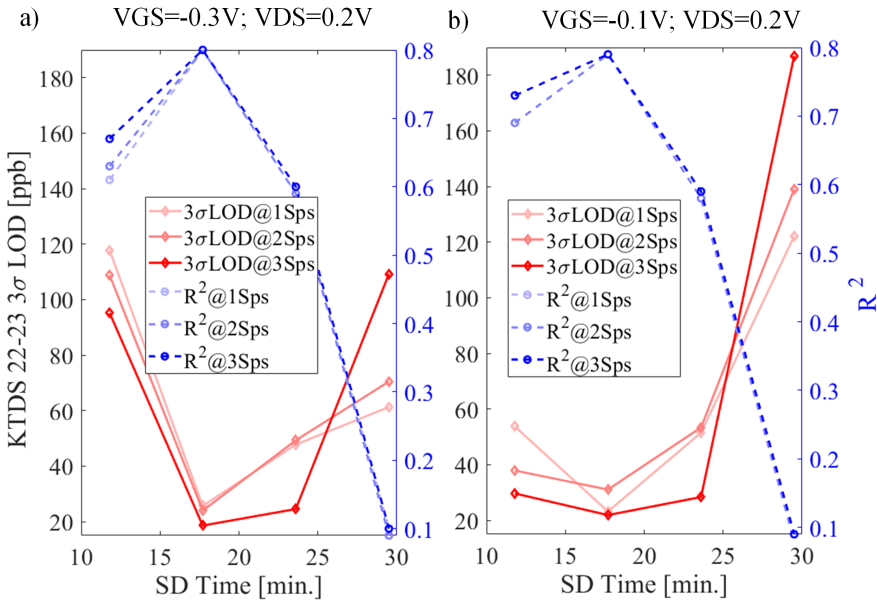
Figure 5.5: LOD and R^2 coefficient as a Slope Detection (SD) time window function for: a) $VGS_{CNT} = -0.3\,V$ and b) $VGS_{CNT} = -0.1\,V$ with a common $VDS_{CNT} = 0.2\,V$, when 1 to $3\,Sps$ are acquired and averaged.

5.5 Chapter Summary

5.5.1 CNT-FET nanosensor and the embedded sensing platform

Sensor signals are measured for NO_2 concentrations of $1\,ppb$, the $3\,\sigma$ limit of detection (LOD) of $23\,ppb$ is determined in slope detection (SD) mode, including the sensor signal variations in repeated measurements. This result is in the range of the WHO actual limit values presented in Table 1.2. Moreover, the different designs presented in Table 2.3 and compared from a system-level perspective are further compared in Table 5.1 form sensing design perspective: the commercial reference platform, e.g., Aeroqual, which uses an SM-50 O_3 measurement unit [183] for outdoor environments, provides highly accurate ozone measurements within $[0...150]\,ppb$. The Telaire 6713 from Amphenol Advanced Sensors, a sensor measuring indoor CO_2 concentrations within $[400...5000]\,ppb$ with high accuracy, suffers from a similar shortcoming [184]. A recently published full research system solution is the W-Air module presented in [185] employs two MOX for O_3 and CO_2 sensors from the shelf,

Embedded System Performance Comparison				
Ref./Spec.	**Detector type**	**Compound identification**	**3σ LOD [ppb]**	**Methodology**
This Work	CNT	NO_2	23	slope detection
Commercial [183]	electrochem.	O_3	1 (LDL)	linear response
Commercial [184]	IR	CO_2	$\pm30000 \pm3\%$ (acc.)	ABC calibrated
Proc.ACM 18 [185]	MOX	O_3; CO_2	O_3:4;CO_2:64	NN calibrated
IEEE SAS 15 [186]	electrochem.	NO_2; CO	NO_2 :23;CO :2000	linear response

Table 5.1: Comparison of sensing solutions integrated in an embedded system.

trying to eliminate the interference of VOC emissions. Another research prototype [186] demonstrates $[0...13]\,ppm\,CO$ $[0...10]\,ppm\,SO_2$ $[0...27]\,ppm$ NO_2 analytes.

5.5.2 CNT-FET nanosensor and the dynamic signal acquisition ASIC

The designed ASIC can interface with the CNT-FET nanosensor and demonstrates NO_2 gas concentration measurements from $0\,ppb$ to $200\,ppb$ in the humid air. Lab characterization of the entire system shows that the complete acquisition system achieves a 3σ LOD of $18.5\,ppb$ with an R^2 linear fit coefficient of 0.8. The system's dynamic power consumption depends on the CNT nanosensor device characteristics, NO_2 analyte concentration, and the applied bias level. Another example of a CNT-based system is presented in [149], achieving a power consumption of $32\,\mu W$ with a measured minimum gas concentration of $50\,ppm$ of NO_2, which is not suitable for the needs of air-quality monitoring systems. Compared to the other integrated systems, this design offers the lowest power consumption and, in combination with the CNT-FET nanosensor, is capable of measuring NO_2 concentrations below $50\,ppb$, which makes it suitable for use in environmental monitoring and health protection applications. Table 5.2 summarizes the performance of the designed system in perspective with the SoA signal acquisition ICs for gas sensors.

5.6 Preliminary design conclusions

The embedded platform offers a wide current range, and high versatility makes it suitable for signal acquisition from resistive nanosensors such as silicon nanowires, carbon nanotubes, graphene other 2D materials. Compared to other implementations, the embedded platform demonstrates a state-of-

ASICs System Performance Comparison				
Ref./Spec.	Detector type	Compound identification	$3\,\sigma$ LOD [ppb]	Methodology
This Work	CNT	NO_2	18.6	slope detection
ISSCC 16 [281]	MEMS	C_9H_{12}	15	chromatography
ISSCC 16 [282]	NEMS	C_3H_{10}	30	chromatography
IEEE SJ 06 [283]	micro-hotplate	CO	200	linear response
JSSC 09 [149]	CNT	NO_2	50000	rel. resistance

Table 5.2: Comparison of sensing solutions (co)integrated into CMOS techno-
logy.

the-art (SoA) 3σ LOD of a CNT-FET nanosensor, exposed to NO_2 gas
concentrations from $200\,ppb$ down to $1\,ppb$.

The ASIC design demonstrates NO_2 gas concentration measurements from
$0\,ppb$ to $200\,ppb$ in the humid air when connected to the CNT-FET nano-
sensor. Lab characterization shows that the complete acquisition system
achieves a 3σ LOD of $18.5\,ppb$. Compared to the other integrated systems,
this design can measure a thousand times lower NO_2 concentrations.

As introduced in chapter 1, both proposed systems are suitable for environ-
mental monitoring and health protection applications.

6 Sensor Node Demonstrator with the CNT-FET and ASIC

This chapter introduces the concept of a compact sensor node for the CNT-FET, which uses the designed ASIC as a signal acquisition block and includes an Android application to visualize the sensor data on a smartphone. The chapter starts with the embedded software description, which has been realized as an improved iteration of the FSM introduced in chapter 2.5. Compared to the embedded platform presented in chapter 2, the software runs directly on the nRF 52 [156] SoC, interfacing the ASIC via a daughterboard with the help of an Adafruit Featherboard [10]. After the hardware interface is described, the software part of the sensor node concept introduces a lookup table with reference NO_2 results of the pre-characterized CNT-FET nanosensor, which can be used for mapping the ID_{CNT} initial slope to a corresponding NO_2 analyte concentration. The sensor node is designed to reduce its power consumption by switching off dynamically SoC blocks when not used and implementing an interruption-based sensing routine as introduced in chapter 2.5.2. Finally, a graphical user interface (GUI) for the data transmission over BLE is developed based on the Arduino Bluefruit application programming interface (API). This application stores BLE data sent by the nRF 52 [156] and displays it to the user, in *ppb* equivalent or as raw currents on a graph. The Android App was programmed with Android Studio and is compatible with all devices running on Android 4.1 or higher. However, the displayed values are test data since, due to date, this sensor node couldn't have been characterized with actual CNT-FET nanosensors in a real-case scenario.

6.1 Conceptual design

This sensor node concept comes as a final application demonstrator, an improvement of the embedded platform presented in chapter 2. The sensor node application demonstrator is designed to operate in-field, connected wireless to the sensor node such that as many physical locations as possible can be covered. A key parameter of this design is power consumption, followed

by its physical dimensions. The power consumption determines the sensor node operation time for a given energy density of the power source, i.e., a coin lithium cell battery. The ASIC enables this presented in chapter 3, which exhibit dynamic power consumption, and the SoC nRF 52 features different power profiles. Finally, the sensing platform's production cost can be minimized from a mass production perspective.

In Figure 6.1.a-c, the sensor's node main building blocks are described in the context of a daughterboard attached to Adarfruit nRF 52 Feather (shown in Figure 6.1d.) and forms a compact, mobile, low-cost, low-power, fully autonomous sensing system. The hardware components reduction is enabled mainly by the developed ASIC (Figure 6.1.c) specialized for the CNT-FET nanosensor.

The embedded software design effort has been substantially reduced thanks to the FSM functions 2.5.3, which are now reused to run on the nRF 52 CPU core. Moreover, the features of nRF 52 SoC are explored for ASIC steering signal generation, local data postprocessing, and RF transmission via the BLE protocol. A visualization of the "NOXE" smartphone application is presented in Figure 6.1.e.

6.2 Daughterboard

The daughterboard presented in Figure 6.2 accommodates a PLCC socket with up to four CNT-FET nanosensors. Since the designed ASIC can process one single channel at a time, an analog multiplexer [302] is connected in between. The daughterboard is then connected to the Adafruit [10], which features the nRF 52 SoC, and a USB programming interface.

This development board has been used due to the substantial effort of Adafruit in integrating the low-level SoC libraries in an Arduino IDE. This embedded system environment offers a high abstraction level appropriate for the nRF 52 SoC when designing complex applications, i.e., NO_2 gas sensor node. The different embedded tasks are executed by the SoC as being the core of the system and can be summarised as follows:

1. Generates control signals for the ADC variable sampling rate

2. Setting the precise VDS_{CNT} bias level via the ASIC DAC

3. Acquire digital data from the ASIC and post-process them locally
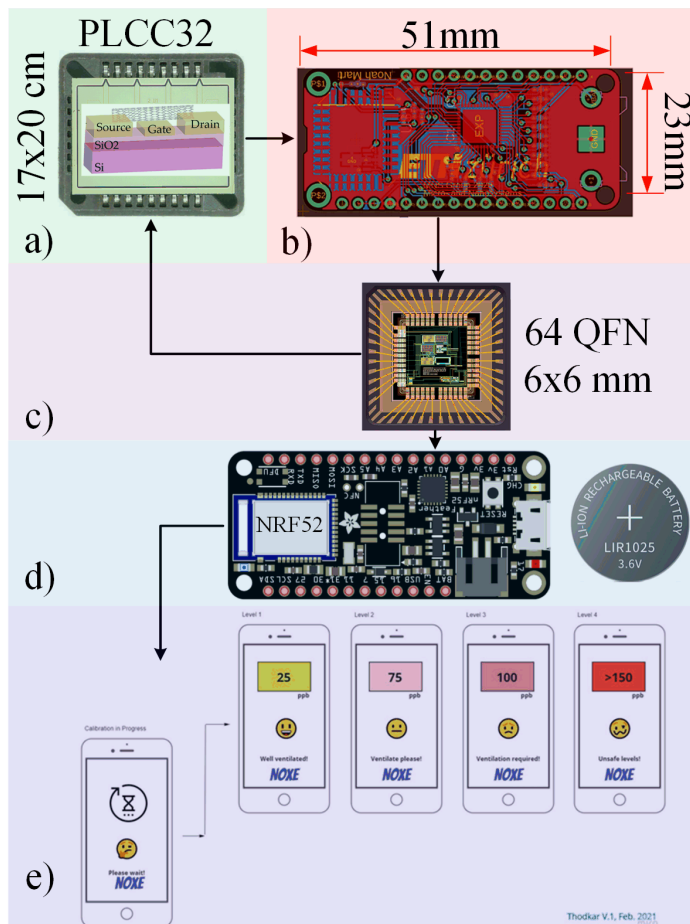
Figure 6.1: Block schematic of the application demonstrator composed by: a) CNT-FET nanosensor placed in PLCC 32 socket; b) daughterboard which accommodates the CNT-FET and the ASIC together with bias circuitry; c) the ASIC V1 in a QFN 64 pin package, d) Adafruit Feather nRF 52 and a Li-Ion 3.6 V battery; e) an illustration of the smartphone App (illustration courtesy of Dr. Kishan Thodkar.)

4. Steer the measurement routine with the help of a low-energy FSM

5. Send data via SoC-integrated BLE
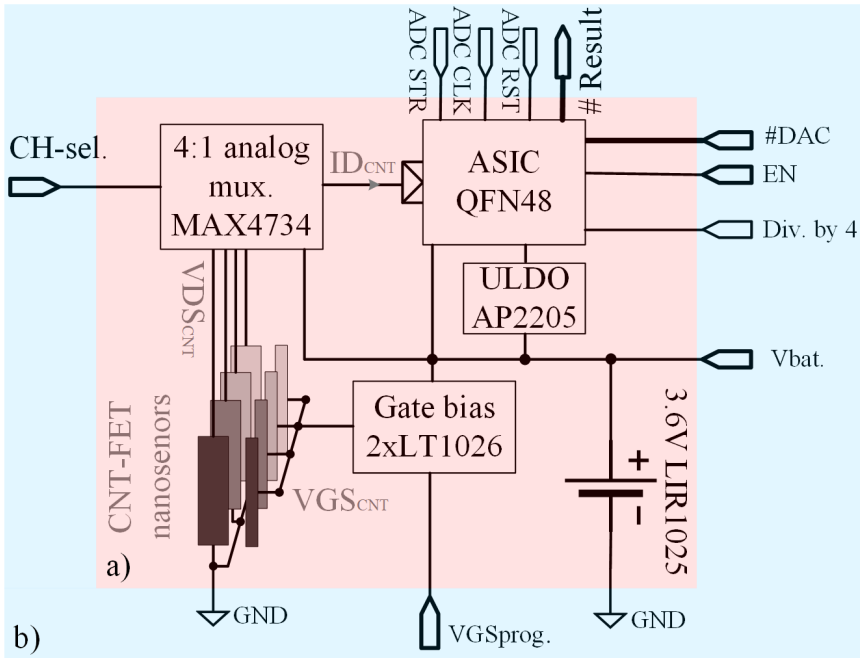
Figure 6.2: Block schematic of the CNT-FET based sensor node composed of: a) daughterboard accommodating four nanosensors, the ASIC, an analog multiplexer, a stand-alone Gate bias, a 3.6 V rechargeable battery with a 1.8 V ULDO; b) pinout peripherals towards the Adafruit Feather board [10].

6.3 Adafruit Feather nRF 52

The Adafruit Feather nRF 52 was chosen as the development board, exploring its hardware resources, i.e., BLE or external timer interrupts [156]. The embedded code runs natively on the nRF 52 CPU, which is fast, efficient, and smaller than the ATmega 2560 [181]. Moreover, the powerful ARM Cortex M4F processor with one MB flash and $256\,KB$ SRAM offers a native USB port rather than ISP [181] interface, and the bootloader can be mass-storage-based. This is supported by circuit Python hardware; UART pins can communicate to other peripherals. This solution offering low power potential is a single-chip solution that supports central and peripheral modes [156]. An overview of the embedded software running on the SoC for the NO_2 sensing node application is presented in Figure 6.3 highlighting the particular set of stack functions. A detailed description of the stack functions can be found in [11].
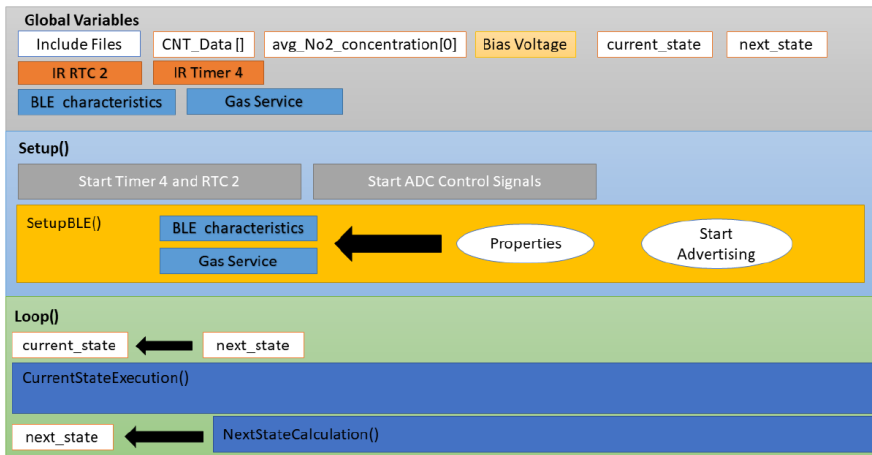
Figure 6.3: Embedded software structure of the sensor node running on the nRF 52 [11].

6.4 LIR1025 battery and USB power

Compared with the embedded platform presented in chapter 2, the power source here can be further decreased thanks to the ASIC dynamic power consumption and the new sensor node concept. Hence, instead of a 5V power bank, a different battery was selected based on its size and nominal voltage. Even though the nRF 52 board has a built-in battery jack (2-pin JST-PH) [10], a coin cell, LIR 1025 3.6 V, $6\,mAh$ rechargeable battery has been used. The coin cell battery has the advantage of a much smaller size [303] and can be mounted between the Adafruit Feather and the daughterboard. The USB port works as the programming interface and power supply, including $100\,mA$ battery charging current [10]. Moreover, it happens in a 'hot-swap' fashion such that the battery operates as a backup when the USB power is disconnected. The power consumption is variable for Adafruit Feather, tunable by the configuration programming of the nRF 52 chip. An interactive tool for calculating the nRF 52 power consumption profile can be found in [12]. The results of a simulation are presented in Figure 6.4.

6.5 Voltage LDO

The ASIC digital input/output pins are supplied by the VCC and VSS power domain of 3.3 V as presented in A.4.2 A.5.2 A.6.2. However, the designed
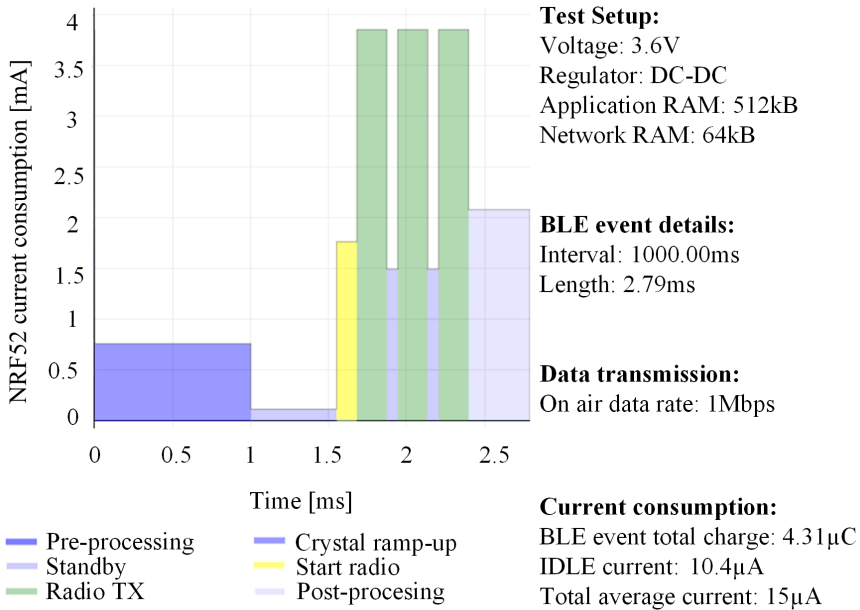
Figure 6.4: Power profiler for nRF 52 simulation for $1\,Sps$ at $0\,dBm$ transmission power. Figure resulted from interactive Online Power Profiler for Bluetooth LE.

ASIC core extensively presented in chapter 3 has two different power supply domains:

1. VDDA: $1.8\,V$

2. VDDdig.: $1.8\,V$

A local regulated supply voltage of $1.8\,V$ is required for the ASIC core to be powered. An ultra low-dropout voltage (ULDO) regulator is needed to step down the battery from $3.6\,V$ to $1.8\,V$ by using an AP2205-18Y-13 [304]. The main reason for using this part is its ultra-low quiescent current of $10\,nA$ [304]. Two ceramic capacitors were added at ULDO input and output of $1.1\,\mu F$ and $2.0\,\mu F$.

6.6 Charge-pumps

As presented in 1.3.3.2, the CNT-FET nanosensor requires a VGS_{CNT} variable potential referred to as GND. Since the ASIC integrated charge pump (presented in chapter 3.6.1) had no working regulator, an external one has been used instead. The appropriate device used here is the LT1026 voltage converter [305], which can operate in the range of input values from $0\,V$ to $6.6\,V$ and convert this to a $\pm 12\,V$ output voltage. To do so, two identical LT1026 have been connected in a cascade. The first one doubles the battery voltage of $3.6\,V$, whereas the second charge pump is to double the obtained $\approx 6\,V$ to $\approx 12\,V$ or to double and invert the voltage obtaining $\approx$-$12\,V$. These configurations are presented in [305] and implemented as in Figure 6.2.

6.7 ADC control signals

As presented in chapter 3.24, three control signals for steering the ASIC ADC operation are needed. The signals can be generated by the nRF 52 SoC and passed the daughterboard. They come as a correlated toggling sequence that aims to control the ADC sampling rate precisely. The ADC signal consists of the following:

1. ADC STR signal activates the sample switches after one clock cycle.

2. ADC CLK signal comes as ten front edges, i.e., one for tracking the signal and the rest of nine for successive approximation conversion while holding the sampled value.

3. ADC RST after conversion, the ADC returns to its initial state with the help of the reset signal.

The variable sample rate embedded function was created by Noah Marti as a part of his Bachelor's Thesis [306]. The final implementation includes timers, the Programmable Peripheral Interconnect (PPI), and the General Purpose Input/Output Task and Event (GPIOTE) module. The ADC sampling rate control signals are generated events at desired time instances linked to tasks in the GPIOTE module with the help of the PPI. Compared to the method using interrupts, this method has the advantage that the nRF 52 CPU is not used during runtime, and there is no processing that could influence the time between event generation and task execution. The time step between event generation and task execution is one clock cycle. This does not affect

the runtime, as the signal is periodicâthe signal pattern is illustrated in Figure 6.5.

For using the nRF 52 hardware resources efficiently, only two timers are used for the signal, so other timers can be used for the FSM implementation. Hence TIMER2 and TIMER3 [156] generates the trigger events marked with A-F; in Figure 6.5 where τ is a user-set variable.

$$\tau = \frac{T_{sample-ADC}}{32} \tag{6.1}$$

1. A: set ADC RST to HIGH; after $4\,\tau$

2. B: set ADC STR to HIGH; after $5\,\tau$

3. C: set ADC CLK to HIGH; after $10\,\tau$

4. D: set ADC STR to LOW, allow the second timer to link its events to tasks; after $11\,\tau$

5. E: forbid the second timer to link its events to tasks after $30\,\tau$ (stop ADC CLK toggle).

6. F: set ADC RST to LOW, clear the timer after $32\,\tau$

Hence, an integer multiple of $32 \cdot \tau$ can be programmed, achieving $T_{sample-ADC}$ up to tens of $kSps$ for the CNT-FET signal acquisition. A detailed signal description can be found in [306].

Figure 6.5: ADC control signals: a) ADC reset operating on inverse logic, b) ADC start conversion operating on inverse logic, and c) ADC clock highlighting the track phase and the successive conversion steps. Figure adapted form [11].

6.8 Slope detection algorithm

Compared to the embedded platform's data structure presented in chapter 2.5.4, where the data is stored on an SD card and post-processed in Matlab, the proposed sensor node implements a slope detection (SD) algorithm locally on the SoC. As introduced in chapter 5, this readout algorithm measures the gas concentration with the transient response of the CNT-FET nanosensor and outperforms the quasi-steady state QSS readout. From the application perspective, this substantially reduces energy consumption by avoiding long QSS time exposure and can be used in air pollution monitoring as introduced in 1.4.2. Furthermore, from the computation complexity perspective, the SD is sufficient to use simple methods like linear-least-squares that can be executed in $\mathcal{O}(4N)$ [307]. However, only pre-characterized CNT-FET nanosensors from the lab can be used due to device reproducibility. Thanks to good repeatability, the pre-characterized CNT-FETs can be installed on the sensor node and exposed to the field. For example, the KTDS15 has been extensively characterized in the lab, and its slopes for different NO_2 analyte concentrations are presented in Figure 6.6. The information obtained from the initial slopes can be used for visualization and as a requirement for the back-calculation of analyte concentration. As introduced in 5.1.2, these initial slopes can be expressed as:

$$S_0' = \frac{\sum_{i=1}^{N} 6S\left(i\Delta t\right)\left[2i - (N+1)\right]}{\Delta t N\left(N^2 - 1\right)} = K_{ads} \cdot p, \qquad (6.2)$$

where N represents the number of data samples from Figure 6.6 within Δt sense, and p is the partial pressure of the gas analyte (different NO_2 concentrations in Figure 6.6). As the partial pressure is proportional to the actual gas concentration, it can be stated that the initial slope is linearly dependent on the analyte concentration. The proposed observation window for the implementation in this thesis is 5 to 15 $minutes$, values which come good in line with [4] findings. This formula was implemented in the gas-sensor-readout program by Jan Portmann [308]. While Liliane Paradise [307] explored various other methods such as neural networks to get a filtered response, slope detection together with a subsequent lookup table comparison (and linear interpolation between the lookup table entries) has been chosen as being the most effective among them, in terms of implementation simplicity and not very computationally demanding. The simplicity of each of the proposed algorithms follows to enable easy integration into the gas sensing platform. The slope detection algorithm is presented in Appendix A.7 as a pseudo-code. The complete implementation as a macro function in C++ can be found in [308].
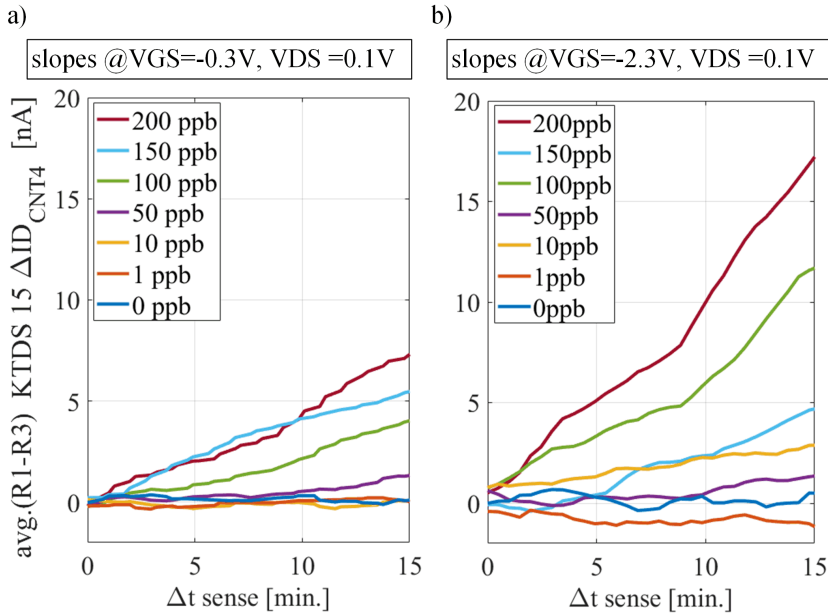
Figure 6.6: KTDS15 CNT-FET nanosensor precharacterised slopes: a) $VGS_{CNT} = -0.3\,V$ and b) $VGS_{CNT} = -2.3\,V$ with a constant $VDS_{CNT} = 0.1\,V$ for NO_2 gas concentrations.

6.9 Physical design

The final hardware design step for the sensor node is the daughterboard's layout and assembly, which accommodates the CNT-FETs socket with the ASIC, and connects to the Adafruit Feather, which comes plug and play [10]. This has been realized as a student project of Pablo Bennloch [309] which presents the PCB design, manufactured and successfully assembled with all soldered components and stacked to the Adafruit board. The physical design of the daughterboard is presented in Figure 6.7.a. The final physical layout of the complete sensor node, including its dimension, is shown in Figure 6.7.b.

6.10 Android App design

As a final software development step, the GUI of the sensor node has been designed for an Android device. This application demonstrator aims to ac-
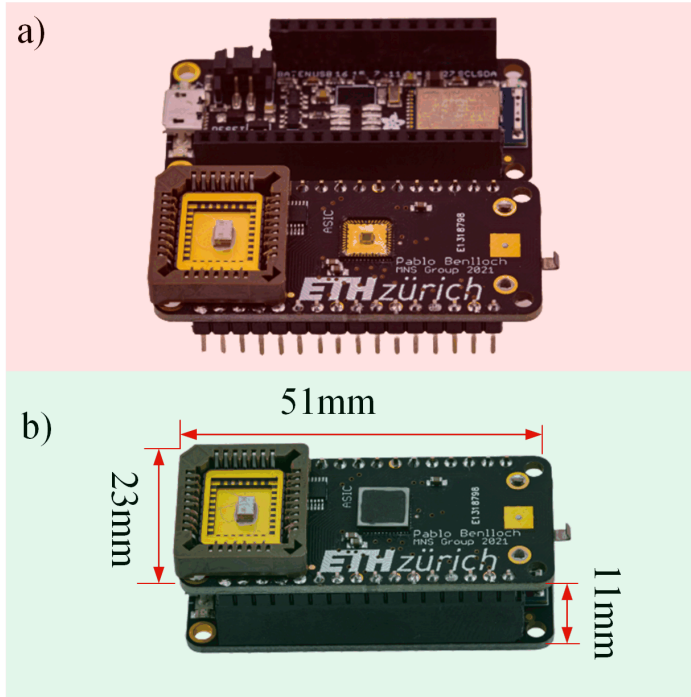
Figure 6.7: Physical design of: a) the daughterboard [12] PCB next to the Adafruit Feather devboard; b) physical dimensions of the final sensor node.

commodate a place-holder for the received sensor node data and display them on the screen. Postprocessing sensor values that ensure data quality are implemented in the sensor-readout code of the nRF 52. An overview of the sensor node App functionality is given below:

1. Read sensor node data i.e., raw current, timestamp, NO_2 concentration.

2. Display CNT-FET nanosensor raw drain current measurement over time in a continuously updating graph.

3. Display data of interest to the user as a label, i.e., low, medium, high.

4. Warn the user, displaying a dynamic warning dependent on the gas concentration.

5. Read the sensor node's battery level and report the level.

The layout of the sensor node App is presented in Figure 6.8 and shows the information mentioned above intuitively.
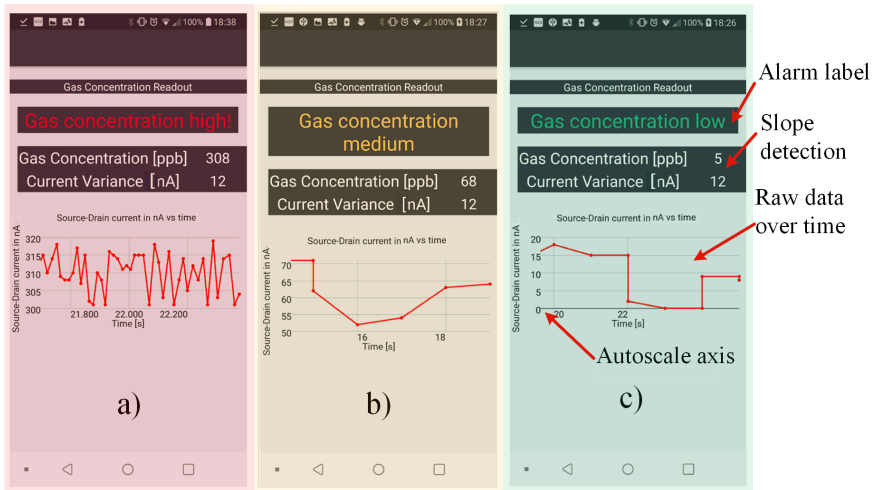
Figure 6.8: GUI demonstrator of the Android application for test data of a) high; b) medium; c) low NO_2 gas concentration readout. Figure adapted from [11].

The proposed Android application developed as a Bachelor's Thesis by Lucas Gimeno[11] fulfills the basic requirements for the CNT-FET nanosensor to be interfaced with the ASIC, and the acquired signal is sent to a mobile device via nRF 52 BLE SoC.

6.11 Power consumption

Table 6.1 illustrates the distributed power consumption among all main building elements (including the CNT-FET nanosensor and the ASIC) of the sensor node when running actively. For comparison, the embedded platform power consumption distribution presented in the chapter is shown in the second part of Table 6.1. It can be observed that the sensor node achieves massive power consumption reduction for similar sensing performance. However, substantial power consumption is drawn by the G-Bias implemented with the two LT1026 and the voltage regulator AP2205. This suggests the necessity of a second ASIC design iteration which includes a charge pump, voltage regulator, and band-gap reference.

6.12 Chapter summary

A compact wireless NO_2 sensor node based on CNT-FET nanosensors has been presented yet is still developing. For the time being, the nRF 52 embedded software can generate control signals for the IC and acquires measurement results that can be used for the slope detection algorithm. Moreover, data results are conveniently transmitted via BLE to Android-compatible smartphone apps. However, the daughter board of the sensor node would need a complete characterization before running NO_2 gas measurements with real CNT-FET nanosensors.

Sensor node power consumption: 378.17 μW

- ■ nRF52 SoC [b]
- ■ ULDO AP2205 [c]
- ■ MUX4734 [304]
- ■ G-Bias [d]
- ■ ASIC & CNT [e]

Embedded platform power consumption 83.2 mW [a]

- ■ CDC [5]
- ■ BLE [156]
- ■ μC [13]
- ■ D-Bias [155]
- ■ G-Bias [155]
- ■ V-REF [167]
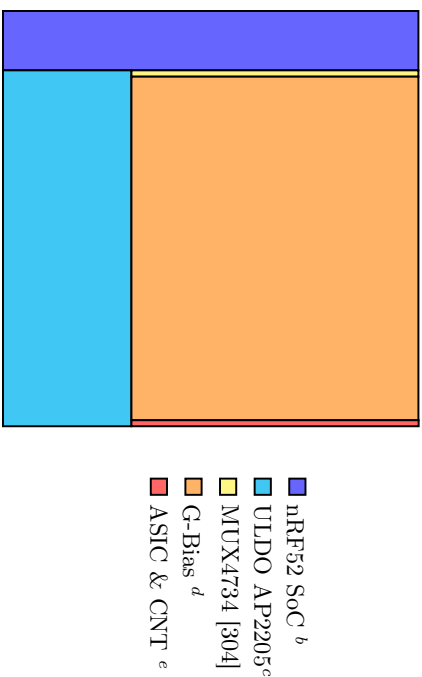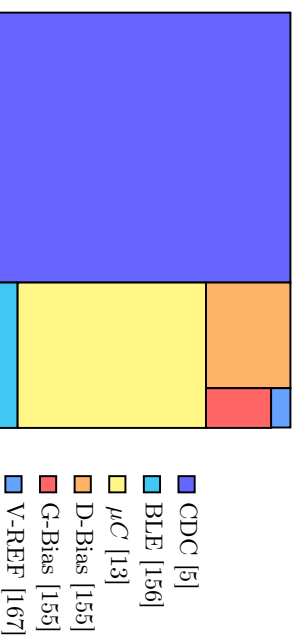
Table 6.1: Estimated power consumption of the sensor node compared to the embedded platform.

[a] SD card has been removed; only blocks with similar functionally are compared.
[b] $1\,Sps$ at $0\,dBm$ transmission power estimated by Online Power Profiler for Bluetooth LE.
[c] estimated value from the data-sheet [304]
[d] estimated value from the data-sheet [305]
[e] when supplied at $1.8\,V$ and an ADC sampling rate of $2.66\,kSps$ the a CNT-FET sensor biased at $VDS_{CNT} = 0.2\,V$ at $200\,ppb\ NO_2$

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7 Conclusions and Future Work

7.1 Embedded sensing platform

The first part of this research presents the concept, realization, and performance evaluation of a portable and customizable embedded platform for the CNT-FET nanosensor. The platform's hardware can adapt to the nanosensor requirements and measure a wide current range. In addition, this solution is fully autonomous and highly configurable, employing a user-defined instruction set. Thanks to the FSM's embedded functions, various platform parameters allow for setting, namely:

1. The CDC integration time and capacitor bank

2. Defining the FS and BW

3. DAC bias level/period (including a bipolar potential beyond the supply voltage)

4. Time intervals for SD card storage and BLE data transmission

5. Power-saving FSM-state deactivates the CPU internal blocks and thus reduces the average power consumption

A reproducible CNT-FET nanosensor response to NO_2 exposure was demonstrated down to $1\,ppb$ of NO_2 in dry air with a $3\,\sigma$ LOD as low as $23\,ppb$ (1σ: $7\,ppb$) in lab conditions. This first implementation of a compact embedded sensor platform demonstrates the remarkable capability of the CNT-FET nanosensor readout. It fulfills WHO's respective annual exposure limits for one of the main six pollutants, i.e., NO_2. The embedded solution, which the user can configure, allows for simple addition, replacement, and reordering of FSM states, thus offering flexibility and enabling further trade-offs between functionality and energy efficiency. The energy efficiency of the proposed platform can be further optimized by reducing, reordering, or customizing the software-defined FSM states and state transition timings. However, the

physical dimensions of the platform and its DC power consumption are relatively high because of the use of off-the-shelf components.

Consequently, a specialized ASIC has been developed to optimize power consumption and achieve miniaturization. As a final result, a CNT-FET-based sensor node has been realized. The critical component of this sensor node is the ASIC which integrates the front-end sensor signal acquisition and is concluded in the following paragraph.

7.2 Dynamic signal acquisition ASIC

The concept, design, physical layout, and characterization of a dedicated CMOS current signal acquisition IC that interfaces with a CNT-FET nanosensor have been presented in this thesis. One attractive block of this design is the single-stage single-ended input to differential output TIA. This structure compares favorably to the classical TIAs, which require constant high-bias currents for achieving low noise. The noise level vs. power consumption is low thanks to the class AB circuit operation, which uses the input current as part of the bias, a feature that is uncommon for an ordinary TIA. Additionally, the common-mode regulation reduces the in-band noise of the gain resistors at the output by suppressing the common-mode component. The ASIC has been connected to the CNT-FET nanosensor, and a reproducible nanosensor current response was acquired on exposure to the NO_2 gas analyte in the humid air. Several key design parameters for air quality applications were achieved. First, the acquisition achieves a LOD of $18.5\,ppb\ NO_2$, in line with the current WHO guideline values. The LOD system performance parameter is determined by the total noise of CMOS IC circuits and CNT-FET nanosensor, together with measurement errors like repeatability and time drift effects. Second, the proposed voltage-bias architecture can accommodate a broad range of NO_2 current values by keeping a constant programmable bias voltage, which defines the system's overall performance. In addition, this feature can be used for CNT-FET device-to-device variation adjustment and sensor degradation compensation. The system's total power consumption scales inherently with the sensor input current, i.e., analyte gas concentration. The design is realized in $180\,nm$ CMOS technology and occupies a silicon area of $0.18\,mm^2$. Accordingly, when connected to the proposed IC, the CNT-FET nanosensor demonstrates NO_2 gas concentration measurements from $0\,ppb$ to $200\,ppb$ in the humid air. Lab characterization of the entire system shows that the complete acquisition system achieves a 3σ LOD of $18.6\,ppb$ with an R^2 linear fit coefficient of determination of 0.8. At the same time, the IC offers input range, bandwidth, ADC speed, and precision in line with alternative solutions for resistive sensors. These fea-

tures are necessary for further integrating CNT-FETs on CMOS substrate toward market feasibility in the IoT domain.

7.3 Sensor node demonstrator employing the CNT-FET and ASIC

The sensor node and the smartphone App introduce the CNT-FET nanosensor in the IoT domain towards air quality monitoring in urban areas at a fraction of size and cost. The application demonstrator reduces the number of hardware components thanks to the ASIC circuit dedicated to the CNT-FET nanosensor. Moreover, the sensor node can post-process the acquired nanosensor data by implementing transient slope detection. This can be achieved with lab pre-characterized nanosensor data stored in a lookup table, in which the current slopes can be translated to an actual NO_2 gas concentration. Future work could validate this concept with measurements performed in a real-case scenario using the CNT-FET nanosensor.

A Appendix

A.1 DDC114

The bandwidth of the DDC114 can be determined when evaluating its transfer function.

$$V_{out} = \frac{1}{C_{range}} \int_0^{T_{conv}} \underbrace{I_{IN}}_{ct. \ for \ t=T_{conv}} dt = \frac{I_{IN}}{C_{range}} \cdot T_{conv} \tag{A.1}$$

$$\frac{V_{out}}{I_{IN}} = \frac{T_{conv}}{C_{range}} \tag{A.2}$$

The frequency dependency can be determined by taking the Fourier transform of the system's impulse response. The DT integrator's impulse response is a pulse of width T_{conv}.

$$H(f) = \frac{V_{out}}{I_{IN}} = \frac{T_{conv}}{C_{range}} * \underbrace{\left[u\left(t + \frac{T_{conv}}{2}\right) - u\left(t - \frac{T_{conv}}{2}\right) \right]}_{rectngular \ window} \tag{A.3}$$

$$H(freq) = \frac{V_{out}}{I_{IN}} = \frac{T_{conv}}{C_{range}} \cdot sinc(\pi \cdot T_{conv} \cdot freq) \tag{A.4}$$

A.2 DDC114

$$\overline{Out_{R_{CNTFET}}noise}^2 = \int_0^\infty \underbrace{\left| \frac{sin\left(\pi \cdot T_{conv} \cdot freq\right)}{\pi \cdot freq} \right|^2 df}_{DDC114 \ transfer \ function} \cdot \underbrace{\frac{4kT}{R_{CNTFET}}}_{CNTFET_{noise}} \cdot \frac{1}{C_{range}^2} \tag{A.5}$$

$$\overline{Out_{R_{CNTFET}}noise} = \sqrt{\underbrace{\int_0^\infty \left| \frac{sin\left(\pi \cdot T_{conv} \cdot freq\right)}{\pi \cdot freq} \right|^2 df}_{1/2 \cdot T_{conv}} \cdot \underbrace{\frac{4kT}{R_{CNTFET}}}_{CNTFET_{noise}} \cdot \frac{1}{C_{range}^2}}$$

$$\text{(A.6)}$$

$$\overline{Out_{R_{CNTFET}}noise} = \frac{1}{C_{range}} \cdot \sqrt{\frac{2kT}{R_{CNTFET}} \cdot T_{conv}} \qquad \text{(A.7)}$$

To express the noise in current reffered to the DDC114 full-scale (FS) range the Eqn. A.7 can be devided by the integrator's full-scale voltage, $V_{FS} = V_{REF}$, and multiplied to the I_{FS} as:

$$Out_{R_{CNTFET}}noise = \frac{\sqrt{\frac{4kT}{R_{CNT}(NO_2)} \cdot \frac{T_{conv}}{2}}}{C_{range}V_{REF}} \cdot I_{FS} \qquad \text{(A.8)}$$

A.3 Signal Path

A.3.1 Input Impedance

The resulting impedance $Z_{in(0)}$ at the pad is calculated as in:

$$Z_{in}\left(0\right) = \frac{V_{test}}{I_{test}}, \qquad \text{(A.9)}$$

where

$$I_{test} = gm_1 \cdot (A+1) \cdot (-V_{test}) - gds_1 \cdot \left(\frac{I_{test}}{gm_2} + V_{test} \right) \qquad \text{(A.10)}$$

hence

$$\frac{V_{test}}{I_{test}} = -\frac{1 + \frac{gds_1}{gm_2}}{gm_1 \cdot (A+1) + gds_1} = -\frac{\frac{1}{gds_1} + \frac{1}{gm_2}}{A \cdot \left(\frac{gm_1}{gds_1} \right) + 1} \cong \frac{-1}{gm_1 \cdot A} \qquad \text{(A.11)}$$

A.3.2 TIA

A.3.2.1 Signal Transfer Function

The TIA signal transfer function is given by the SFGs. as:

$$H_{Iin}(s) = \frac{V_{out}(s)}{I_{Iin}(s)} = \frac{R_g}{s^2 C_1 C_L R_g \cdot \frac{1}{Gm} + s\left(C_L R_g - C_1 R_g + C_1 \cdot \frac{1}{Gm}\right) + 1} \tag{A.12}$$

The frequency of the two poles can be derived as follows:

$$\omega_{p1}; \omega_{p2} = -\frac{\frac{C_L}{C_1} \cdot R_g Gm + 1 - R_g Gm}{2 \cdot C_L R_g} \cdot \left[1 \pm \sqrt{1 - \frac{4\frac{C_L}{C_1} R_g Gm}{\left(\frac{C_L}{C_1} \cdot R_g Gm + 1 - R_g Gm\right)^2}}\right] \tag{A.13}$$

A.3.2.2 Poles and zeros

Approximation of the two poles:

$$\begin{aligned} \omega_{p1} &= \frac{Gm}{\sqrt{C_1 C_L}} \\ \omega_{p2} &= \frac{Gm}{C_L} \end{aligned} \tag{A.14}$$

$$H_{nM10} = \frac{1 + \frac{sC_1}{Gm}}{s^2 \frac{C_1 C_2}{Gm^2} + s\frac{C_L}{Gm} + 1} \tag{A.15}$$

the zero of the this transfer function can be written in therms of ω_{p1} as:

$$\omega_z = j\omega_{p1}\sqrt{\frac{C_L}{C_1}} \tag{A.16}$$

this transfer function can be re-written in therms of ω_{p1} and ω_{p1} as:

$$H_{nM10} = \frac{1 - j\frac{\omega}{\omega_{p1}}\sqrt{\frac{C_1}{C_L}}}{1 + j\frac{\omega}{\omega_{p2}} - \frac{\omega^2}{\omega_{p1}^2}} \tag{A.17}$$

A.3.2.3 SNR

The SNR is defined as $\frac{SignalPower}{NoisePower}$ at the same point of the circuit. For this design, the SNR will be evaluated at the output of the TIA. Suppose an input signal $I_{IN}(t) = I_{in}\,sin\,(\omega t)$ will have a power of :

$$P_{I_{IN}} = \left(\frac{I_{in}}{\sqrt{2}}\right)^2 = \frac{I_{in}^2}{2} \tag{A.18}$$

The signal input power is propagated towards output by the transfer function $H(j\omega)$. Hence the signal power at the output can be expressed as:

$$P_{V_{out}} = \frac{I_{in}^2}{2} \cdot |H(j\omega)|^2 \tag{A.19}$$

The noise sources, however, are injecting noise in different points of the circuit, which propagates differently towards the output of the TIA. The total noise power can be written as:

$$P_{noise} = \overline{I_{nD6}^2} \cdot |H(j\omega)|^2 + \left(\overline{I_{nD12}^2} + \overline{I_{nRg}^2}\right) \cdot |N_{nD12}; R_g(j\omega)|^2 + \overline{I_{nD10}^2} \cdot |N_{n10}(j\omega)|^2 \tag{A.20}$$

The current noise of the individual transistor drains can be expressed as follows:

$$I_{D6} = I_{CM} + I_{in} \overset{w.i.}{\Rightarrow} \overline{I_{nD6}^2} = \frac{4q\gamma_{nD}}{m} \cdot (I_{CM} + I_{in}) \tag{A.21}$$

$$I_{D12} = I_{CM} + \frac{I_{in}}{2} \overset{w.i.}{\Rightarrow} \overline{I_{nD12}^2} = \frac{4q\gamma_{nD}}{m} \cdot \left(I_{CM} + \frac{I_{in}}{2}\right) \tag{A.22}$$

The current noise of the individual transistor drains can be expressed as follows:

$$I_{D10} = I_{CM} + I_{in} \overset{w.i.}{\Rightarrow} \overline{I_{nD10}^2} = \frac{4q\gamma_{nD}}{m} \cdot (I_{CM} + I_{in}) \tag{A.23}$$

The noise transfer functions can be written as:

$$|H(j\omega)|^2 = \frac{1}{\left|j^2\omega^2 \cdot \frac{C_1 C_L}{Gm^2} + j\omega \cdot \frac{C_L}{Gm} + 1\right|^2} \tag{A.24}$$

$$|N_{n10}(j\omega)|^2 = \frac{\omega^2 \frac{C_1^2}{Gm^2}}{\left|-\omega^2 \cdot \frac{C_1 C_L}{Gm^2} + j\omega \cdot \frac{C_L}{Gm} + 1\right|^2} \tag{A.25}$$

$$|N_{n12}; R_g(j\omega)|^2 = \frac{1 + \omega^2 \frac{C_1^2}{Gm^2}}{\left|-\omega^2 \cdot \frac{C_1 C_L}{Gm^2} + j\omega \cdot \frac{C_L}{Gm} + 1\right|^2} \tag{A.26}$$

The SNR can be then expressed:

$$SNR = \frac{\frac{I_{in}^2}{2} \cdot |H(j\omega)|^2}{\overline{I_{nD6}^2} \cdot |H(j\omega)|^2 + \left(\overline{I_{nD12}^2} + \overline{I_{nRg}^2}\right) \cdot |N_{nD12}; R_g(j\omega)|^2 + \overline{I_{nD10}^2} \cdot |N_{n10}(j\omega)|^2} \tag{A.27}$$

by substituting the individual expressions of the signal and noise transfer functions, the SNR can be further simplified and expressed as:

$$SNR = \frac{\frac{I_{in}^2}{2}}{4q \left(1 + \omega^2 \frac{C_1^2}{Gm^2}\right) \cdot \left[\frac{V_T}{R_g} + \frac{\gamma_{nD}}{m}\left(2I_{CM} + \frac{3}{2}I_{in}\right)\right]} \tag{A.28}$$

wherein $Gm \overset{w.i.}{\rightarrow} = \frac{I_D}{nV_T} = \frac{I_{in} + I_{CM}}{nV_T}$ and hence, the SNR can be further expressed as:

$$SNR = \frac{P_{signal_{out}}}{P_{noise_{out}}} = \frac{\frac{I_{in}^2}{2} \cdot (I_{in} + I_{CM})^2}{4q \left[(I_{in} + I_{CM})^2 + \omega^2 C_1 (nV_T)^2\right] \cdot \left[\frac{V_T}{R_g} \cdot \frac{\gamma_{nD}}{m} \cdot \left(2I_{CM} + \frac{3}{2}I_{in}\right)\right]} \tag{A.29}$$

for $I_{in} \gg I_{CM}$ the SNR is direct proportional to I_{in} and decreases over frequency with ω^2.

A.3.2.4 Harmonic distortions

A TIA input sinusoidal current, i.e., $I_{IN} = I_{in} \cdot sin(\omega t)$ has a maximum $I_{in-peak} = I_{in} \cdot 1$, and generates a peak output voltage $V_{out-peak} = V_{CM} + V_{out-diff}/2$. This output differential voltage can be rewritten as:

$$V_{out-peak} = 2a \cdot ln(I_{CM} + I_{in}) + a(I_{CM}) + a \cdot ln(b) + c \qquad \text{(A.30)}$$

Discussion: The Taylor series expansion takes place around the operating point of the circuit. Since this TIA design has a variable operating point, i.e., $ID_{11} = ID_{12} = I_{CM} + I_{IN}/2$, the expansion will take place around $io = I_{CM} + I_{in}/2$

$$\underbrace{V_{out-peak} = 2a \cdot ln\left(I_{CM}\left(1 + \frac{I_{in}}{I_{CM}} + a\right)\right)}_{= f(I_{in})} + a \cdot ln(I_{CM}) + a \cdot ln(b) + c \quad \text{(A.31)}$$

$$f(I_{in}) = 2a \cdot ln\left(1 + \frac{I_{in}}{I_{CM}}\right) + 2a \cdot ln(I_{CM}) + a \cdot ln(b) + c \qquad \text{(A.32)}$$

$$f(I_{in})/_{I_{in}=i_o} \simeq f(io) + \frac{f'_{(io)}}{1!} \cdot (I_{in} - io) + \frac{f''_{(io)}}{2!} \cdot (I_{in} - io)^2 + \frac{f'''_{(io)}}{3!} \cdot (I_{in} - io)^3 + \dots$$
$$\text{(A.33)}$$

$$f(I_{in})/_{I_{in}=i_o} \simeq 2a \cdot ln(I_{CM} + i_o) + a \cdot lm(I_{CM}) + a \cdot ln(b) + c + \dots \quad \text{(A.34)}$$

$$\dots + \underbrace{\frac{a}{1 + \frac{i_o}{I_{CM}}}}_{K1} \cdot (I_{in} - i_o) - \underbrace{\frac{a}{\left(1 + \frac{io}{I_{CM}}\right)^2}}_{K2} \cdot (I_{in} - i_o)^2 + \underbrace{\frac{2a}{\left(1 + \frac{io}{I_{CM}}\right)^3}}_{K3} \cdot \frac{(I_{in} - i_o)^3}{3}$$
$$\text{(A.35)}$$

$$HD_2 = \frac{1}{2}\left|\frac{K_2}{K_1}\right| \cdot I_{in} = \frac{1}{2} \cdot \frac{a}{\left(1 + \frac{I_{CM} + I_{in}/2}{I_{CM}}\right)^2} \cdot \frac{\left(1 + \frac{I_{CM} + I_{in}/2}{I_{CM}}\right)}{2a} \cdot I_{in} = \frac{1}{4} \cdot \frac{1}{2 + \frac{I_{in}/2}{I_{CM}}} \cdot I_{in}$$
$$\text{(A.36)}$$

$$HD_3 = \frac{1}{4}\left|\frac{K_3}{K_1}\right|\cdot I_{in}^2 = \frac{1}{4}\cdot\frac{2}{3}\cdot\frac{a}{\left(1+\frac{I_{CM}+I_{in}/2}{I_{CM}}\right)^3}\cdot\frac{\left(1+\frac{I_{CM}+I_{in}/2}{I_{CM}}\right)}{2a}\cdot I_{in}^2 \quad (A.37)$$

$$HD_2 = \frac{1}{4}\cdot\frac{I_{in}}{\left(2+\frac{I_{in}/2}{I_{CM}}\right)} \quad (A.38)$$

$$HD_3 = \frac{1}{12}\cdot\frac{I_{in}^2}{\left(2+\frac{I_{in}/2}{I_{CM}}\right)^2} \quad (A.39)$$

A.3.2.5 VTH Mismatch

$$Currents\begin{cases} I_{in} = I_{D5} - I_{D9} \\ I_1 = I_{D11} - I_{D9} \\ I_2 = I_{D12} - I_{D10} \\ I_{D9} = I_{D5} - I_{in} \\ I_1 = I_{D11} - (I_{D5} - I_{in}) \\ I_{D10} = I_{D6} = I_{D5} \\ I_2 = I_{D12} - I_{D6} \end{cases} \quad (A.40)$$

$$Voltages\begin{cases} V_{out1} = I_1 R_g + V_{CM} \\ V_{out2} = I_2 R_g + V_{CM} \end{cases} \quad (A.41)$$

The transimpedance gain $G = \frac{V_{out1}-V_{out2}}{I_{in}}$ can be written as

$$G = \frac{R_g\left[(I_{D6} - I_{D5}) + (I_{D11} - I_{D12}) + I_{in}\right]}{I_{in}} \quad (A.42)$$

in nominal conditions when $I_{D6} = I_{D5}$ and $I_{D11} - I_{D12}$ the transimpedance gain is given by the R_g. However, a current mismatch in the current mirrors formed by nMOS mirror $M5 - M6$ and/or pMOS mirror $M11 - M12$

generates an offset current which translates in an output offset voltage. The offset current can be expressed as

$$I_{offset-in} = \underbrace{(I_{D11} - I_{D12})}_{I_{\Delta 112}} + \underbrace{(I_{D5} - I_{D6})}_{I_{\Delta 56}} \tag{A.43}$$

where $I_{\Delta 112}$ and $I_{\Delta 56}$.

$$\begin{cases} I_{\Delta 112} \cong gm_{121} + \Delta_{VT112} + \frac{\Delta\beta_{112}}{\beta} \\ I_{\Delta 56} \cong gm_{56} + \Delta_{VT56} + \frac{\Delta\beta_{56}}{\beta} \end{cases} \tag{A.44}$$

$$I_{offset} = \frac{1}{nVT} \cdot \left[\left(I_{CM} + \frac{I_{offset}}{2} \right) \cdot \Delta_{VTH112} + (I_{CM} + I_{offset}) \cdot \Delta_{VTH56} \right] \tag{A.45}$$

$$I_{offset} = \frac{I_{CM} (\Delta_{VTH112} + \Delta_{VTH56})}{nVT - \left(\frac{\Delta_{VTH112}}{2} + \Delta_{VTH56} \right)} \rightarrow \sigma_{I_{offset}} \tag{A.46}$$

$$\sigma_{I_{offset}} \approx \sqrt{\left[\frac{I_{CM}}{nVT} \right]^2 \cdot \left(\frac{A^2_{VT_{PMOS}}}{W_p L_p} + \frac{A^2_{VT_{NMOS}}}{W_n L_n} \right)} \tag{A.47}$$

$$\sigma^2_{I_{offset}} \approx \left[\frac{I_{CM} \left(nVT - \frac{\Delta_{VT56}}{2} \right)}{\left(nVT - \frac{\Delta_{VT112}}{2} - \Delta_{VT56} \right)^2} \right]^2_{when \Delta_{VT56} = \Delta_{VT112} = 0} \cdot \frac{A^2_{VT112}}{2W_{P11-P12} \cdot L_{P11-P12}} \tag{A.48}$$

$$+ \left[\frac{I_{CM} \left(nVT - \frac{\Delta_{VTH112}}{2} \right)}{\left(nVT - \frac{\Delta_{VTH112}}{2} - \Delta_{VTH56} \right)^2} \right]^2_{when \Delta_{VTH56} = \Delta_{VTH112} = 0} \cdot \frac{A^2_{VTH56}}{2W_{P5-P6} \cdot L_{P5-P6}} \tag{A.49}$$

$$I_{offset} = I_{CM} \cdot \frac{\Delta_{VTH112} + \Delta_{VTH56}}{nVT - \left(\frac{\Delta_{VTH112}}{2} + \Delta_{VTH56} \right)} \tag{A.50}$$

this is a function of two variables, hence by applying Papoulis formula [310], one can calculate

$$f_{(x_1,\, x_2)} = a \cdot \frac{x_1 + x_2}{b - \left(\frac{x_1}{2} + x_2\right)}$$

$$\sigma^2_{f_{(x_1\, x_2)}} = \left[\frac{\delta f_{(x_1\, x_2)}}{\delta x_1}\right]^2 \cdot \sigma^2\left(x_1\right) + \left[\frac{\delta f_{(x_1\, x_2)}}{\delta x_2}\right]^2 \cdot \sigma^2\left(x_2\right) \qquad \text{(A.51)}$$

$$\frac{\delta f_{(x_1,\, x_2)}}{\delta x_1} = \frac{\delta Ioffset}{\delta \Delta_{VTH112}} = \frac{I_{CM}\left(nVT - \frac{\Delta_{VTH56}}{2}\right)}{\left(nVT - \frac{\Delta_{VTH112}}{2} - \Delta_{VTH56}\right)^2} \qquad \text{(A.52)}$$

$$\frac{\delta f_{(x_1,\, x_2)}}{\delta x_2} = \frac{\delta Ioffset}{\delta \Delta_{VTH56}} = \frac{I_{CM}\left(nVT + \frac{\Delta_{VTH112}}{2}\right)}{\left(nVT - \frac{\Delta_{VTH112}}{2} - \Delta_{VTH56}\right)^2} \qquad \text{(A.53)}$$

$$\sigma^2_{Ioffset} = \left[\frac{I_{CM}\left(nVT + \frac{\Delta_{VTH56}}{2}\right)}{\left(nVT - \frac{\Delta_{VTH112}}{2} - \Delta_{VTH56}\right)^2}\right]^2 \cdot \frac{A^2_{VTHp}}{2W_p L_p} \qquad \text{(A.54)}$$

$$+ \left[\frac{I_{CM}\left(nVT + \frac{\Delta_{VTH112}}{2}\right)}{\left(nVT - \frac{\Delta_{VTH112}}{2} - \Delta_{VTH56}\right)^2}\right]^2 \cdot \frac{A^2_{VTHn}}{2W_n L_n} \qquad \text{(A.55)}$$

A.3.3 Schematic of the flip-flop data registers of the SAR ADC
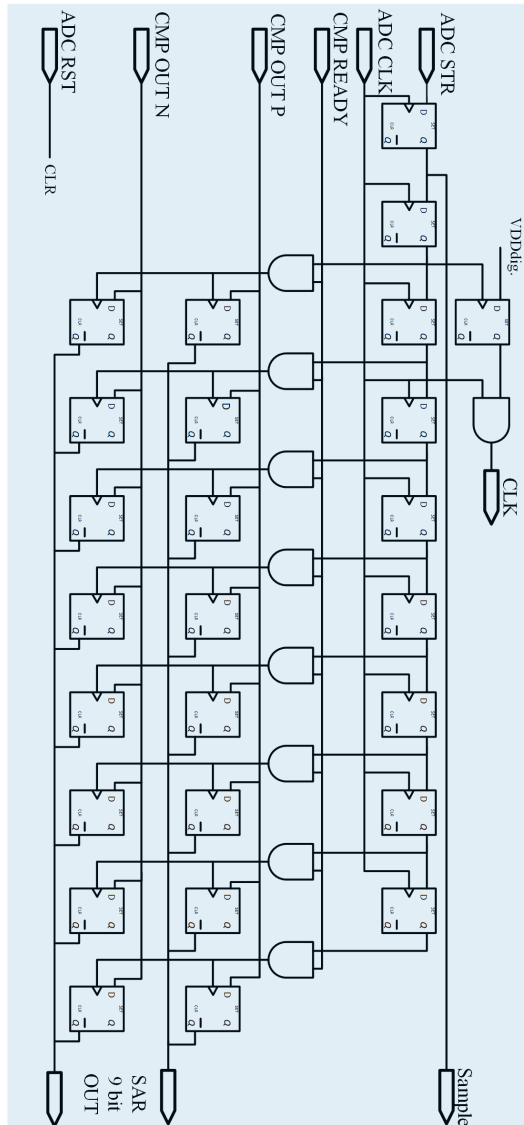
Figure A.1: Schematic of the flip-flop data registers of the SAR ADC. The input and output signals are highlighted explicitly. ADC_{RST} uses connection by name to register CLR.

A.3.4 FFT spectral analysis technique for calculating ENOB of the designed SAR ADC

Algorithm 1 FFT spectral analysis technique for calculating ENOB of the designed SAR ADC.

---

import M acquired ADC bitstream vector
import record time information

$plot(time, V_{ADC})$ ▷ plot the reconstructed interpolated points of sinusoid
$FFT_{ADC} \leftarrow FFT(V_{ADC})$
$N \leftarrow lenght(FFT_{ADC})/2 + 1$ ▷ nr of points is half of FFT points
$fs \leftarrow t_n - t_{n-1}$ ▷ calculate fs from time info.
$X \leftarrow (0; \ fs/2; \ N)$ ▷ construct frequency axis
$han \leftarrow hanning(length(V_{ADC}))$ ▷ avoid spectral leakage with windowing function
$Y \leftarrow FFT(han * V_{ADC})$ ▷ convolute V_{ADC} with the Hanning window
$Y_{dBFS} \leftarrow 20log(abs(Y)/sqrt(2))$ ▷ convert the resulted spectra in dB full-scale
$plot(X, Y_{dBFS})$ ▷ plot the resulted spectra for visual inspection
$idx\_fun \leftarrow idx.max(Y_{dBFS})$ ▷ assuming the fundamental has the highest amplitude
$FFT_{span} \leftarrow 100$ ▷ create a span of 100Hz around each harmonic
for $idx = 2 \cdot idx_{fun}; idx <= N; idx_{fun}+ = idx_{fun}$ **do**   ▷ spanning over signal harmonics
    $har_{lvl} = max(Y_{dBFS}[idx - FFT_{span} : idx + FFT_{span}])$ ▷ save harmonic level
    $har_{idx} = idx$ ▷ save harmonic index
    $sig_{idx} = [idx - 2 \cdot FFT_{span} : idx + 2 \cdot FFT_{span}]$ ▷ save signal index around har_{idx}
end for
$n\_floor_{idx} = Y_{dBFS} - har_{idx} - sig_{idx}$ ▷ take remaining idx as noisefloor
for $idx = 1; idx <= length(har_{idx}); idx = 1$ **do**
    $PDist+ = 10^{har_{lvl}[idx]/10}$ ▷ calculate distortion power
end for
$PNoise \leftarrow 10^{avg(n\_floor)/10} * N/2$ ▷ calculate noise power
$PSignal \leftarrow 10^{Y_{dBFS}(idx\_fun)/10}$ ▷ calculate signal power
$SINAD \leftarrow 10log_{10}(PSignal/(PDist + PNoise)$ ▷ calculate SINAD
$ENOB \leftarrow (SINAD - 1.76)/6.02$ ▷ derive ENOB
additionally it can be calculated:
$THD \leftarrow PDist/PSig$ ▷ total harmonic distortion
$THDN \leftarrow (PDist + PNoise)/PSig$ ▷ total harmonic distortion & noise

A.4 ASIC V1 Tape-out

The first version integrates all the designed blocks, including the regulated charge pump. This is also the most optimistic design for a "first time right" result. The V1 tape-out silicon die photo is presented in Figure A.2. The pin-out description is presented in Table A.4.2.

A.4.1 ASIC V1 silicon die photo
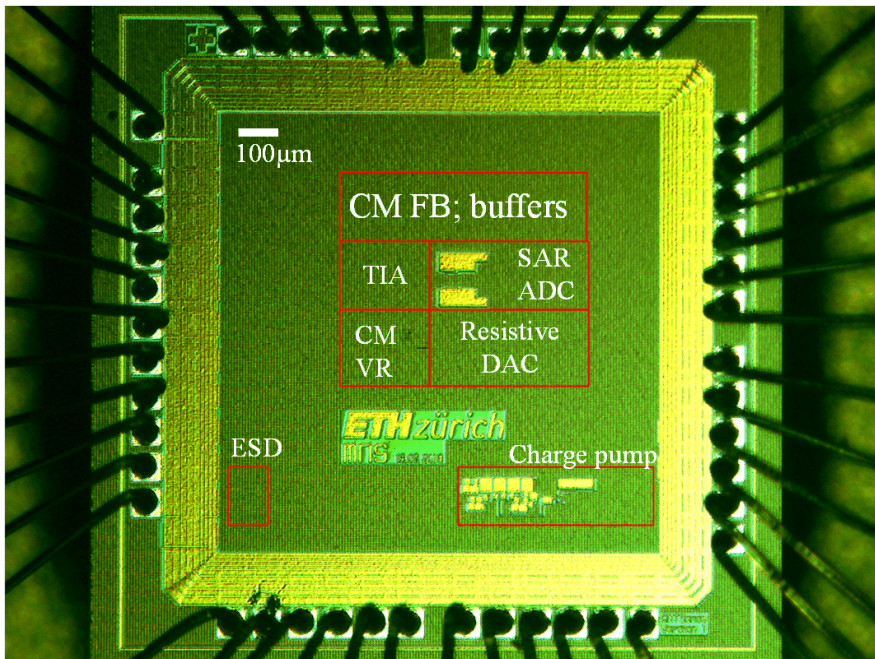
Figure A.2: ASIC V1 designed in UMC $0.18\,\mu m$ CMOS technology.

A.4.2 ASIC V1 pin-out

CNTSense TOP V1			
PIN	**Nr.**	**Function**	**Description**
GND RING	1	Digital Power	GND connection of the Padring; to be connected on the PCB GND
VDDA	2	Analog Power	Analog power supply, 1.8V Nominal
Ip_buf_n	3	Analog Input	Bias current for voltage buffer, 100nA Nominal, n_current mirror
In_buf_p	4	Analog Input	Bias current for voltage buffer, 100nA Nominal, p_current_mirror
In_cmfb	5	Analog Input	Bias current for CMfb stage, 100nA Nominal
V_CM_ref	6	Analog Input	Bias voltage for CMfb ref, 900mV Nominal, or VDDA/2
I_CNT_in	7	Analog Input	Analog Input CNT current
I_bias_p	8	Analog Input	Bias current for DAC buffer, 100nA Nominal, p_current mirror
VDDD	9	Digital	Digital power supply, 1.8V Nominal
VDDA/VSSA	10	Analog/Digital	Analog and Digital Power GND. C decoupling as close as possible to this pin on the PCB
VNEG	11	Analog Output	VG output form the Charge Pump. Padring diode and connection removed, Bipolar ESD diode added, not form UMC standard library
NC	12	-	not connected
VDDRING	13	Digital Power	VDDD for the digital pins
SW_Pol	14	Digital Input	This pin switches the polarity of the VNEG output form charge pump
Reg_EN_n	15	Digital Input	Active on "0", enabling the CP regulation Loop
Start_reg	16	Digital Input	Active on rising edge
G_Set_7..0	17...24	Digital Input	Bit 7 (MSB) ... 0 (LSB)CP output voltage set
GND RING	25	Digital Power	GND connection of the Padring; to be connected on the PCB GND
CLK_CP	26	Digital Input	Charge Pump clock signal input
GND	27	Digital Power	GND connection of the Pad Ring Digital Driver IO Buffers
VCC	28	Digital Power	VDD connection of the Pad Ring Digital Driver IO Buffers; to be decoupled on the PCB as close as possible
D_DAC_EN	29	Digital Input	This pin enables the D_bias DAC output voltage
Div_4	30	Digital Input	When enabled, the I_CNT_in current is divided by a factor of 4
D_Set_0	31..36	Digital Input	Bit 0..5 D_Bias output voltage set
VDDRING	37	Digital Power	VDDD for the digital pins
ADC_clk	38	Digital Input	ADC_clk
ADC_rst	39	Digital Input	ADC_reset_sample_caps
ADC_start	40	Digital Input	ADC_start_conversion
B_out_7...0	41...48	Digital Output	ADC_output result

A.5 ASIC V2 tape-out

The second version is dedicated to the charge-pump blocks. It provides extra probe pads without ESD protection for testing the subblocks of the structure. The V2 tape-out silicon die photo is presented in Figure A.3. The pin-out description is presented in Table A.5.2.

A.5.1 ASIC V2 silicon die photo
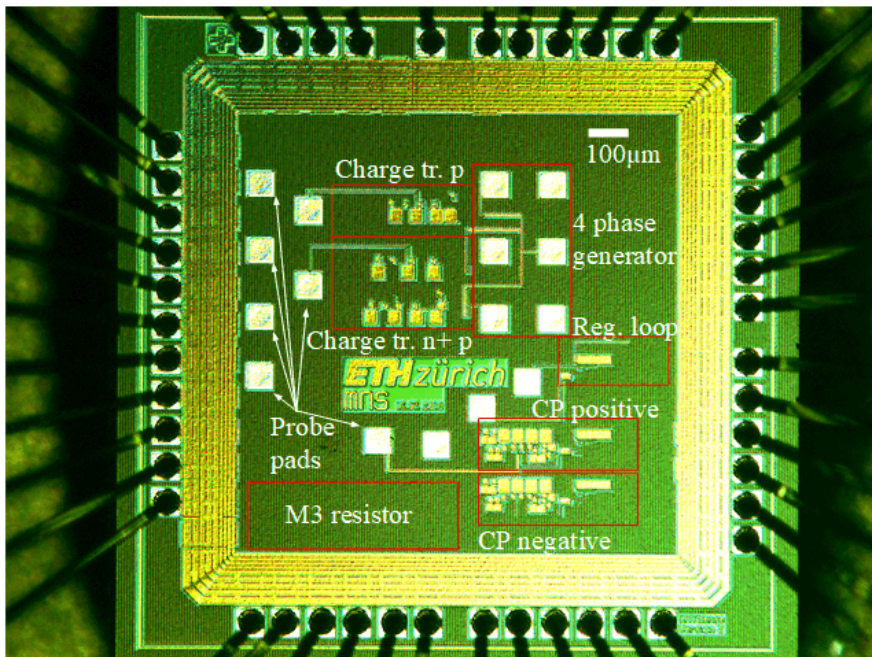
Figure A.3: ASIC V2 designed in UMC $0.18\,\mu m$ CMOS technology.

A.5.2 ASIC V2 pin-out

CNTSense TOP V2			
PIN	**Nr.**	**Function**	**Description**
SW_POL	1	Digital Input	This pin is connected to a test pad together with an analog input pad.
VDDA	2	Analog Power	Analog power supply, 1.8V Nominal
NC	3	-	not connected
V_out_CP_P	4	Analog Output	This pin is connected to a test pad. The bonding pad is ESD protected
NC	5	-	not connected
VSSA ESD	6	Analog Power	Ground pin for the ESD test diode
I_ESD pad leak	7	Analog input	input of custom ESD structure
ESD_bip_test	8	Analog Input	It connects the bipolar ESD test structure. The current should be monitored
VDDD	9	Digital Power	Digital power supply, 1.8V nominal
VSSD/VSSA	10	Star connection of the	
V_NEG	11	Analog Output	This is connected through a M3 resistor to the CP output
NC	12		
VDD_{RING}	13	Digital Power	Padring power supply, 3.3V nominal
SW_pol	14	Digital Input	This pin switches the polarity of the V_NEG output form charge pump
Reg_en_n	15	Digital Input	Active on '0', enabling the CP regulation Loop
Start_reg	16	Digital Input	Active on rising edge
G_Set_8...1	17-24	Digital Input	Bit 7 (MSB) ... 0 (LSB)CP output voltage set
GND RING	25	Digital Power	Padring GND.
CLK_CP	26	Digital Input	Charge Pump clock signal input-both common for both CP(with and without a bonded pad to the package)
GND	27	Digital Power	Digital circuit GND
VCC	28	Digital Power	Digital supply 1.8V Nominal
FB_Set_8...1	29...36	Digital Input	Bit 7 (MSB) ... 0 (LSB)CP output voltage set for the standalone FB loop
VDD Ring	37	Digital Power	Pad ring supply, 3.3V Nominal
FB_start	38	Digital Input	Charge pump regulation loop
FB_CLK	39	Digital output	Regulation loop CLK
FB_f_pump	40	Digital output	Charge pump regulated frequency
FB_PH	41	Digital output	Charge pump nonoverlaping phases
VCC	42	Digital Power	Digital supply 1.8V Nominal
GND	43	Digital Power	Digital circuit GND
NC	44	-	Not connected
CLK_CP_P_N	45	Digital input	CLK for positive and negative CP sub-blocks
EN_CP_N	46	Digital input	Enable charge pump negative sub-block
EN_CP_P	47	Digital input	Enable charge pump positive sub-block
EN_CP_PN	48	Digital input	Enable charge pump both subblocks

A.6 ASIC V3 tape-out

The third version integrates the signal path only, providing enough chip pads for analog and digital signals such that the characterization of individual blocks is possible. The V3 tape-out silicon die photo is presented in Figure A.4. The pin-out description is presented in Table A.6.2

A.6.1 ASIC V3 silicon die photo
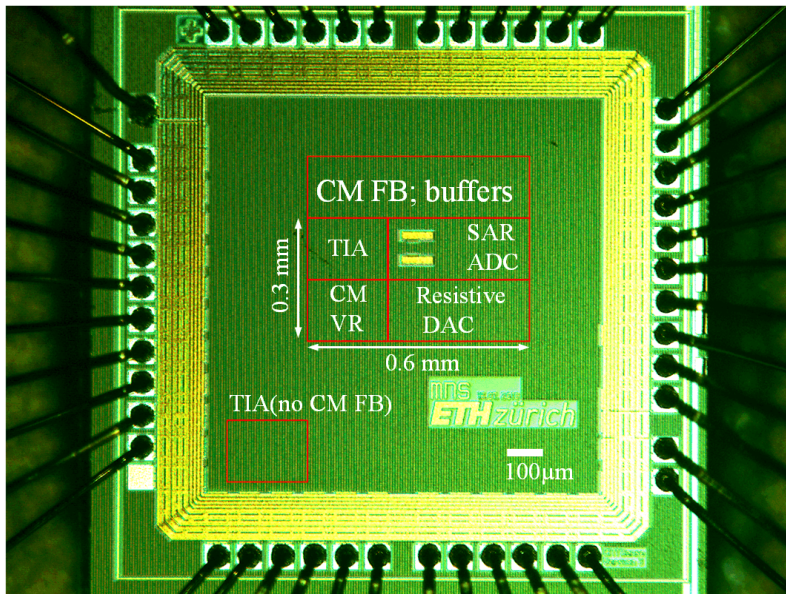
Figure A.4: ASIC V3 designed in UMC $0.18\,\mu m$ CMOS technology.

A.6.2 ASIC V3 pin-out

CNTSense TOP V3			
PIN	**Nr.**	**Function**	**Description**
VCC	1	Digital Power	3.3 V Padring supply, connect as close as possible a decoupling cap
VDDA	2	Analog Power	1.8V Nominal, connect a decoupling cap as close as possible to this pin
I_bn_cmfb	3	Analog Input	Bias current 100nA nominal for CM feedback
I_bn_buff_p	4	Analog Input	Bias current 100nA nominal for voltage buffer P
I_bp_buf_n	5	Analog Input	Bias current 100nA nominal for voltage buffer N
V_CM_REF	6	Analog Input	Common mode reference voltage 900mV nominal, or VDDA/2
I_in_1	7	Analog Input	TIA bidirectional current input
I_bias_p	8	Analog Input	Bias current 100nA for DAC buffer output
I_CNT_in	9	Analog Input	Input current for input cascode
VSSD/VDDA	10	Analog Power	Analog & Core ground
V_out_p_NCMFB	11	Analog Output	TIA output P, connect to this pin to a CMFB resistor/2 with the VDDA/2 with an OP-amp in the loop
V_out_n_NCMFB	12	Analog Output	TIA output N, connect this pin to a CMFB resistor/2 with VDDA/2 with an OP-amp in the loop
I_in_NOCMFB	13	Analog Input	TIA (no CMFB regulation loop) input current
V_CM_in	14	Analog Input	Output of the CMFB OPAMP connected to this pin
V_out_TIA_p	15	Analog Output	TIA output P including CMFB loop
V_out_TIA_n	16	Analog Output	TIA output N including CMFB loop
V_CNT_bias	17	Analog Input	Input buffered voltage for CNT bias
I_out	18	Analog Output	Output current of the Regulated cascode with the current mirror
Comp	19	Analog Input	Connect a compensation cap for the regulated cascode OTA
V_out_buf_n	20	Analog Output	Negative output of the voltage buffer
V_out_buf_n	21	Analog Output	Positive output of the voltage buffer
V_in_buf_p	22	Analog Input	Positive input of the voltage buffer
V_out_buf_p	23	Analog Input	Positive input of the voltage buffer
V_s_ADC_p	24	Analog Input	Differential ADC sampler input_p
V_s_ADC_n	25	Analog Input	Differential ADC sampler input_n
V_DAC	26	Analog Output	Output Voltage 6 Bit resistive DAC, unbuffered
GND	27	Digital Power	GND Ring
GND	28	Digital Power	GND Digital
VCC	29	Digital Power	3.3V PAD ring CLK VDD
Div_4	30	Digital Input	When enabled, the I_CNT_in current is divided by a factor of 4
D_Bias_Set<1..6>	31	Digital Input	Bit 0 D_Bias output voltage set
ADC_clk	37	Digital Input	ADC clock
ADC_rst	38	Digital Input	ADC reset sample caps
ADC_start	39	Digital Input	ADC start conversion
B_out_ADC<8...0>	40-48	Digital Output	ADC_output result

A.7 Algorithm for computation of NO_2 gas concentration with slope detection

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Algorithm 2 Computation of NO_2 gas concentration with slope detection.

import N_total acquired CNT_{FET} nanosensor data in a vector

shorten the vector to the relevant datapoints $N\_total \leftarrow N$ ▷ (optional)

for $idx = 1;\ \ idx <= size(N);\ \ idx+ = 1$ **do**   ▷ implement Eq. 6.2
     $initial\_slope+ = 6 \cdot N(idx) \cdot [2 \cdot idx - (N+1)]$
     idx+=1
end for

$initial\_slope/ = \Delta t \cdot N \cdot (N^2 - 1)$ ▷ implement Eq. 6.2

$initialize\ lookuptable \leftarrow 1$ ▷ initialize the lookuptable

$values \leftarrow lookuptable.csv$ ▷ precharacterisation data from Figure 6.6

$values \leftarrow initial_{slope}[pA/s],\ corresponding\ gas\_conc[ppb]$ ▷ corresponding NO_2

$sort(lookuptable.begin(),\ lookuptable.end())$ ▷ sort increasing $initial_s lope NO_2$

$check\ initial_{slope} > initial_{slope}\ 0ppb$ ▷ check boundaries

$check\ initial_{slope} < initial_{slope}\ 200ppb$ ▷ check boundaries

$critical\ value = lookuptable.begin()$ ▷ set lower boundary

for $idx = lookuptable.begin();\ \ idx! = lookuptable.end();\ \ idx+ = 1$ **do**   ▷ find lower boundary
     if $lower\_boundary > initial_{slope}$ **then**
         $i \leftarrow i - 1$
     else
         $critical\_value = lookuptable(idx)$
     end if
end for

$y_1 = critical\_value$
$y_2 = critical\_value + 1$
$x = initial_{slope}$
$x1 = critical\_value$
$x1 = critical\_value + 1$
$NO_2\ gas\ concentration = y1 + (y2 - y1)/(x2 - x1) \cdot (x - x1)$ ▷ linear int.

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Student Projects Supervised

1. Michael Noack, "Field setup for NO_2 monitoring system", HiWi Project, ETH Zurich 2017.
   Supervisors: S. Nedelcu, S. Eberle, C. Hierold.

2. Laurent Braun, "Low energy Wireless Link and User Interface for NO_2 Gas Sensor Platform", Bachelor's Thesis, ETH Zurich 2017. Supervisors: S. Nedelcu, S. Eberle, C. Hierold.

3. Soléne Bastien, "Read out Circuit for MEMS Vibration Trigger". Semerster Thesis, ETH Zurich 2017. Supervisors: V. Maiwald, S. Nedelcu, F. Sutton, C. Hierold.

4. Carl Philipp Biagosch, "Portable Platform for Carbon Nanotube Gas Sensor". Bachelor's Thesis, ETH Zurich 2017. Supervisors: S. Nedelcu, C. Hierold.

5. Peter Satterthwaite, "Transient Response Analysis for Improved Carbon Nanotube Based NO_2 Sensing". Semester Project, ETH Zurich 2017. Supervisors: S. Eberle, S. Nedelcu, C. Hierold.

6. Pascal Schläpfer, "PCB Design for a Portable Carbon Nanotube Gas Sensor Platform". Semester Project, ETH Zurich 2017. Supervisors: S. Nedelcu, C. Hierold.

7. Stephan Burkhalter, "Wireless ultra-low power front-end for CNT gas sensor". Semester Project, ETH Zurich 2017. Supervisors: S. Nedelcu, C. Hierold.

8. Rafael Monasterios Gallardo, "Wireless ultra low power front-end for CNT gas sensor". Semester Project, ETH Zurich 2019. Supervisors: S. Nedelcu, C. Hierold.

9. Kanata Tanaka, "SAR Auto-Range Embedded Function for variable Gain SWCNT-Current Integrator", ETH Zurich 2019. Supervisors: S. Nedelcu, C. Hierold.

10. Anthony Barison, "Integrated Analogue Verification and Performance Benchmark in the context of an SAR 9-Bit ADC". Master's Thesis, ETH Zurich 2019. Supervisors: S. Nedelcu, C. Hierold.

11. Liliane Paradise, "Design and Integration of Readout Algorithms for Embedded Carbon Nanotube Gas Sensor Platform". Master's Thesis, ETH Zurich 2019. Supervisors: M. Vollmann, S. Nedelcu, C. Hierold.

12. Marc Milewski, "Gas Sensing Platform". Bachelor's Thesis, ETH Zurich 2019. Supervisors: M. Vollmann, S. Nedelcu, C. Hierold.

13. Jan Portmann, "nRF52 Embedded Programming for Wireless NO_2 gas-sensor". Bachelor's Thesis, ETH Zurich 2020. Supervisors: S. Nedelcu, C. Hierold.

14. Noah Marti, "nRF52 Embedded Programming for Bluetooth NO_2 gas-sensor". Bachelor's Thesis, ETH Zurich 2020. Supervisors: S. Nedelcu, C. Hierold.

15. Lucas Javier Gimeno, "nRF52 Embedded Programming for a CNT Gas Sensor Platform Including a Smartphone App". Bachelor's Thesis, ETH Zurich 2021. Supervisors: S. Nedelcu, C. Hierold.

16. Pablo Benlloch Garcia, "PCB Redesign for a Portable Carbon Nanotube Gas Sensor Platform". Semester Project, ETH Zurich 2021. Supervisors: S. Nedelcu, C. Hierold.

17. Basil Müller, "PCB design and assembly for a CNT gas sensor wireless platform". Semester Project, ETH Zurich 2021. Supervisors: S. Nedelcu, C. Hierold.

18. Dejan Bozin, "Characterization of trace gas analysis for gas sensor measurements". Semester Project, ETH Zurich 2021. Supervisors: S. Nedelcu, Kishan Thodkar, C. Hierold.

Publications

A.1 Conferences

1. S. Nedelcu, T. Burger, and C. Hierold, "A 160nW, 56dB SFDR, 109dBOhm, Bidirectional 4uA Max. Input - Differential Output Amplifier with Nested Noise Reduction," in 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, vol. 2020-October, pp. 1-5.

2. S. Nedelcu, S. Eberle, C. Roman, and C. Hierold, "An Embedded, Low-Power, Wireless NO2 Gas-Sensing Platform Based on a Single-Walled Carbon Nanotube Transducer," in 4th International Conference nanoFIS 2020 - Functional Integrated nanoSystems, 2020, vol. 56, no. 1, p. 6.

A.2 Journals

1. S. Nedelcu, K. Thodkar, and C. Hierold, "A customizable, low-power, wireless, embedded sensing platform for resistive nanoscale sensors," Microsystems Nanoeng., vol. 8, no. 1, p. 10, Dec. 2022.

2. P. F. Satterthwaite, S. Eberle, S. Nedelcu, C. Roman, and C. Hierold, "Transient and steady-state readout of nanowire gas sensors in the presence of low-frequency noise," Sensors Actuators B Chem., vol. 297, p. 126674, Oct. 2019.

A.3 Poster presentations

1. S. Nedelcu, S. Eberle, Cosmin Roman and C. Hierold, "Embedded, Low Energy, NO2 Gas Sensing Wireless Platform Based on

Single - Walled Carbon Nanotube Transducer" Swiss NanoConvention, Lausanne, Switzerland, 2019.

2. S. Eberle, S. Nedelcu and C. Hierold, "Estimating the throughput of an automated, high-speed assembly system for carbon nanostructure based sensor" at the Micro and Nanoengineering Conference, Copenhague, 2018.

A.4 Talks

1. A 160nW, 56dB SFDR, 109dBOhm, Bidirectional 4uA Max. Input - Differential Output Amplifier with Nested Noise Reduction; ISCAS, Seville-Virtual, Spain, 12-14 October 2020.

2. Embedded, Low Power, NO_2 Gas Sensing Platform Based on Single-Walled Carbon Nanotube Transducer 4th International Conference; Functional Integrated nano Systems Graz-Virtual, Austria, 2 - 4 November 2020.