DISS. ETH Nr. 27820

DynACuSo: A High Power Dynamic Arbitrary Current Source with a Modular Design

A dissertation submitted to attain the degree of
DOCTOR OF SCIENCES of ETH ZURICH
(Dr. Sc. ETH Zurich)

presented by
GEORGIOS TSOLARIDIS

born 21/01/1991,
citizen of Greece

accepted on the recommendation of
Prof. Dr. Juergen Biela, examiner
Prof. Dr. Davide Aguglia, co-examiner

2021

ETH Zurich
Laboratory for High Power Electronics
Physikstrasse 3 | ETL F11
8093 Zurich | Switzerland

www.hpe.ee.ethz.ch

Στους υπέροχους γονείς μου,
Παναγιώτη και Ιωάννα

... και στον αγαπημένο μου αδερφό,
Γιάννη

Acknowledgement

Over a span of approximately 5 years, there is a number of people who contributed on a technical, but equally importantly on a personal level, to the completion of this work. From the early morning technical derivations in our light-deprived office, to the moments of late evening laughter in the summer bars around Zurich, and from the Friday morning lethargic meetings, to the memorable weekend excursions and gatherings. Looking back, I can see myself growing on a professional and personal level along with many of my close friends and colleagues, and I would like to take this opportunity to express my gratitude to the people that contributed.

First and foremost, nothing would ever get going without Prof. Dr. Juergen Biela. I would like to thank him for giving me the opportunity to be part of his group, his always helpful technical guidance and advice, his professionalism, but also his commitment in continuously improving HPE over the years. I would also like to thank Prof. Dr. Davide Aguglia for his co-supervision of my PhD defense. I kindly also thank Prof. Dr. Christian Franck who, together with his team, helped me on numerous occasions.

At this point, I would like to express my gratitude to two of the unsung heroes of this work, Pascal Zähner for his contribution in the design of the M3TC module and Pascal Seiler for his contributions in Chapter 5. This work would look a lot different without those two, and I hope their journey at HPE was as enjoyable for them as it was for me. I also had the privilege to be entrusted with the supervision of numerous other dedicated individuals, each of them putting their fair share of work. This experience has been extremely enjoyable and enriching for me. Therefore I would also like to take the opportunity to thank each of them, namely: Tanuj Sen, Konstantinos Anagnostopoulos, Joel Arnold, David Graber, Michael Hersche, Yannick Ruffiner, Michael Pritz, Philippe Alff, Bigna Marleina Härdi, Isabelle Schlatter, Nikolaus Patzelt, Nicolas Känzig and Jonathan Orsinger.

Among the numerous members of the lab I would like to specially thank my friend Simon Fuchs, who was from the first up until my last day at HPE willing to help over a cup of coffee or an extended lunch break. Countless times he was called, and countless times he delivered.

I would also like to express my absolute gratitude to my friend and office mate Dr. Daniel Christen, the one who answered my many questions in the first years, and served as my unofficial mentor at HPE. A big thank you goes also without saying to the sometimes annoying, sometimes helpful, but always purely inappropriate, Dr. Milos Stojadinovic, one of my closest friends and colleagues. I would also like to specially thank the Greek section of our lab, Spyridon Stathis, Georgios Papadopoulos, and Ioannis Stavropoulos. Our times together have been memorable and served as the best medicine especially during the times of the pandemic. Special recognition on a personal and professional level goes also to my favorite office mate Oliver Keel, one of the most energetic and talented individuals I have met. I believe the bonds we formed will remain strong over the course of time.

The atmosphere at HPE made, literally everyday enjoyable. Over the years this was the work of each individual and is a condition for the success of our lab. A big thank you goes to all the people that contributed to this atmosphere and with whom I had the privilege of working, namely: Dr. Jonas Wyss, Dr. Michael Jaritz, Dr. Johannes Burkard, Dr. Sebastian Blume, Dr. Andre Hillers, Dr. Dominik Gerber, Dr. Peng Shuai, Stefan Rietmann, Sadik Cinik, Hasan Inanc Sari, Evangelos Kalkounis, Tobias Rogg, Dr. Andreas Jehle, Richard Schlesinger, Adrian Widmer, Raffael Risch, Anliang Hu, Min Jeong, Thomas Ewald, Simon Beck, Qingchao Meng, Bastian Korthauer, Theophane Dimier, Thilo Bringezu and Dr. Mario Kazazi. A special thank you goes also to Jacqueline Perez, our unbelievably reliable and efficient secretary, and to Emir Arnautovic for his work on my hardware setup.

On a more personal level, I would also like to thank my very good friend Daniel Gsponer for creating an ideal environment for the necessary disconnection from work. On a similar note a big thank you goes to Vasco Farto and Sebastian Frison for their support, understanding and companionship.

Finally, a special thank you goes to my beloved Stavroula Despoudi, whose love and care has been an enormous inspiration and motivation for me over the years. Last but not least, I express my utmost gratitude to the three individuals, whose unconditional love has been the only thing constant over the many many years of my studies: Panagiotis Tsolaridis, Ioanna Poutoglidou and Giannis Tsolaridis.

Thank you for everything. Σας ευχαριστώ για όλα.
Giorgos, Zurich, October 2021

Abstract

Along with the giant research accelerators, like the ones that often appear in the news, thousands of smaller accelerators operate every day around the world, producing particle beams in hospitals and clinics, manufacturing plants and industrial laboratories, covering a wide spectrum of applications. Behind the often gigantic electromagnets there are tens of thousands of power electronic converters under operation. In addition to that, thousands of power electronic converters operate in international research centers, acting as a test-benches for various research projects. Among others, these test-bench systems are contributing to the future of the electric grid, which is a fundamental step towards a more sustainable future, by testing and validating high power components and systems that are employed in HVDC networks.

All the aforementioned systems have a common denominator: the delivery of a well-specified arbitrary current waveform to the device under test, by making use of sophisticated high-end power electronics converters. The specifications for those applications are ever-increasing and additional engineering effort is devoted to improve their performance. The limits of those systems are however not fully explored and the overall performance that can be achieved in terms of dynamic, precision and efficiency is not evident a priori.

This research project proposes and analyses a highly dynamic arbitrary current source concept with low output current ripple and a modular design. A suitable topology that has the potential to fulfill a list of strict specifications is initially envisioned, and its operational principle is explained. The topology is based on a multi-phase interleaved buck-type converter connected in series to a step voltage generator, with the ability to generate up to 1.5kA peak current and 10kV bipolar output voltage.

In the process of this work, it is recognized that conventional modelling assumptions for multi-phase interleaved buck-type converters are not suitable for a dynamic current source application with arbitrary loads, and therefore more advanced models need to be used. A specifications driven methodology is then devised to select the needed parame-

ters that are theoretically capable of simultaneously achieving dynamic, steady state and robustness specifications that arise from a range of different applications. Furthermore, a detailed investigation of suitable magnetic materials gives important insights into the volumetric density and efficiency of power inductors in high current pulsed power applications. Additionally to harness the full potential of the topology and the utilized hardware, a systematic comparative evaluation of different control concepts for multi-phase interleaved buck converters is performed. In the process of controller design an adaptive hybrid controller is proposed and identified as the most suitable one for systems operating with step transients.

To be able to characterize the performance of the source in terms of its output ripple, and in parallel minimize the load current ripple by active filter cancellation, innovation is pursued in this work and a current probe with high sensitivity, wide bandwidth and low settling time, based on the current transformer concept with an adaptive burden resistance is proposed. The probe is able to sense AC current ripple in the mA-range that is superimposed on high DC current in the-kA range, only µs after the step transient. It is then shown that the proposed probe can be used together with a linear amplifier, as an active filter to achieve superior ripple cancellation and enable the operation of the system with a load ripple in the ppm range.

A hardware prototype has been developed at the *Laboratory for High Power Electronic Systems (HPE)* at *ETH Zurich*, in order to validate the models, demonstrate the overall achievable performance and act as a test-bench for future research endeavors. The prototype system delivers 1kA continuous current, 1.5kA peak current, and up to 1.1kV output voltage. More importantly the prototype system achieved current gradients that exceeded 15A/µs and current ripple of some tens of mA when driving resistive/inductive loads, while also showing robustness and high controllability when driving currents with steep current gradients through a DC-arc.

Kurzfassung

Neben den in der Forschung verwendeten Teilchenbeschleunigern, die in den Medien häufiger Beachtung finden, sind auch hinter den Kulissen täglich tausende kleinerer Teilchenbeschleuniger im Einsatz, die in Krankenhäusern und Kliniken, Produktionsstätten und in Industrielaboren Teilchenstrahlen erzeugen und damit ein breites Anwendungsspektrum abdecken. Hinter den oft gigantischen Elektromagneten arbeiten üblicherweise zehntausende von leistungselektronischen Wandlern. Darüber hinaus werden in (den oft sehr fortschrittlichen) internationalen Forschungszentren tausende von leistungselektronischen Umrichtern betrieben, die als Prüfstandsysteme für verschiedene Projekte dienen. Nicht zuletzt tragen diese Prüfstandsysteme durch das Testen und Validieren von in HGÜ Netzen verwendeten Hochleistungskomponenten dazu bei, dass ein grundlegender Schritt in Richtung einer nachhaltigeren Zukunft gemacht werden kann.

Alle genannten Systeme haben einen gemeinsamen Nenner: Es muss dem zu testenden Gerät, durch den Einsatz einer hochentwickelten Leistungselektronik, eine exakt spezifizierte, beliebige Stromwellenform zur Verfügung gestellt werden können. Die Spezifikationen für diese Anwendungen werden ständig erweitert, und es wird zusätzlicher Aufwand betrieben, um ihre Leistungsfähigkeit weiter zu steigern. Die Grenzen dieser Systeme sind jedoch noch nicht vollständig ausgelotet und die erzielbare Gesamtleistung in Bezug auf Dynamik, Präzision und Effizienz sind nicht von vornherein ersichtlich.

Dieses Projekt analysiert und entwickelt in diesem Zusammenhang ein hochdynamisches Stromquellenkonzept mit geringer Welligkeit des Ausgangsstroms und flexiblem Design. Eine passende Topologie, die das Potenzial hat, eine Liste strikter Spezifikationen zu erfüllen wird zunächst ins Auge gefasst und das Funktionsprinzip erklärt. Das Topologie basiert auf einem mehrphasigen Abwärtswandler in Reihe geschaltet mit einem Stufenspannungsgenerator, mit der Möglichkeit zur Erzeugung von Ausgangsspitzenströmen bis zu 1.5kA und bipolarer Ausgangsspannung bis zu 10kV.

Im weiteren Verlauf dieser Arbeit wird ersichtlich, dass die konven-

tionellen Modellierungsansätze und Annahmen für mehrphasige verschachtelte Abwärtswandler nicht geeignet sind um eine dynamische Stromquelle für willkürliche Lasten zu beschreiben, daher findet eine detaillierte Neumodellierung statt. Darauf basierend wird eine durch die Spezifikationen vorgegebene Methodik ausgewählt, um die benötigten Parameter zur Beschreibung der dynamischen und stationären Zustands-, und Robustheitsvorgaben zu finden, die sich aus einer Reihe unterschiedlicher Anwendungen ergeben. Darüber hinaus wurden durch eine Reihe detaillierter Untersuchungen geeigneter magnetischer Materialien wichtige Einblicke in die volumetrische Dichte und Effizienz in gepulsten Hochstromsystemen gewonnen. Um das volle Potenzial der Topologie und der eingesetzten Hardware auszuschöpfen, wird eine Bewertung verschiedener Steuerungskonzepte für mehrphasige verschachtelte Abwärtswandler durchgeführt. Ein adaptiver Hybridregler für Systeme, die mit Sprungtransienten arbeiten, wird vorgeschlagen und als am besten geeignet identifiziert.

Um die Leistungsfähigkeit der Quelle hinsichtlich ihrer Ausgangswelligkeit charakterisieren zu können und gleichzeitig die Laststromwelligkeit durch aktive Filterunterdrückung zu minimieren, wird in dieser Arbeit eine Stromsonde mit hoher Empfindlichkeit, großer Bandbreite und geringer Einschwingzeit, basierend auf dem Stromwandlerkonzept mit adaptivem Abschlusswiderstand, vorgeschlagen. Der Tastkopf kann Wechselstromwelligkeit im mA-Bereich erfassen, die einem hohen Gleichstrom im kA überlagert ist, nur Mikrosekunden nach dem Sprung. Es wird gezeigt, dass die vorgeschlagene Sonde zusammen mit einem linearen Verstärker als aktiver Filter verwendet werden kann, um eine stark verbesserte Welligkeitsunterdrückung zu erreichen und den theoretischen Betrieb des Systems mit einer Lastwelligkeit im ppm-Bereich sicherzustellen.

Im Labor für *Hochleistungselektronik (HPE)* der *ETH Zürich* wurde ein Hardware-Prototyp entwickelt, um die Modelle zu validieren, die insgesamt erreichbare Leistung zu demonstrieren und um als Prüfstand für zukünftige Forschungsvorhaben zu dienen. Das Prototypsystem liefert 1kA Dauerstrom, 1.5kA Spitzenstrom und bis zu 1,1kV Ausgangsspannung. Noch wichtiger ist, dass das Prototypensystem Stromanstiegsflanken von über 15A/µs und eine Stromwelligkeit von einigen zehn mA beim Ansteuern von ohmsch-induktiven Lasten erreicht, und gleichzeitig eine hohe Robustheit und Steuerbarkeit beim Betrieb hoher dynamischer Ströme durch einen DC-Lichtbogen zeigt.

Abbreviations

AAF	...	Active Adaptive Filter
ADC	...	Analog to Digital Converter
CAD	...	Computer Aided Design
CC	...	Cross Connected
FB	...	Full Bridge
FEM	...	Finite Element Method
FPGA	...	Field Programmable Gate Array
FSA	...	Full Spectrum Approximation
HB	...	Half Bridge
HiL	...	Hardware-in-the-Loop
HVAC	...	High Voltage Alternating Current
HVDC	...	High Voltage Direct Current
HVDC-CB	...	High Voltage Direct Current Circuit Breaker
IC	...	Integrated Circuit
IGBT	...	Insulated Gate Bipolar Transistor
IO	...	Input Output
LQR	...	Linear Quadratic Regulator
M3TC	...	Marx-type Modular Multilevel Converter
MMC	...	Modular Multilevel Converter
MOSFET	...	Metal Oxide Field Effect Transistor
MPC	...	Model Predictive Controller
MT-HVDC	...	Multi Terminal High Voltage Direct Current
MV	...	Medium Voltage
MVDC	...	Medium Voltage Direct Current
P-HiL	...	Power Hardware-in-the-Loop
PAF	...	Passive Adaptive Filter
PCB	...	Printed Circuit Board
ppm	...	parts per million
PWM	...	Pulse Width Modulation
RMS	...	Root Mean Square
SFC	...	State Feedback Controller
SiC	...	Silicon Carbide
VSC	...	Voltage Source Converter

Table of Contents

1 Introduction

Motivation

Dynamically controllable, precise, and low ripple power supplies with peak output power levels up to several megawatts are a key enabling component for various modern, high-end applications. In this work, three main application areas of such sources are considered and presented along with their challenges and key requirements:

- HVDC Switchgear Characterization
- Power Hardware-in-the-Loop Simulations (P-HiL)
- Particle Accelerators and Plasma Sources

These applications often require a precise, high amplitude DC current with an ultra-low current ripple, and they often employ custom power supply units to deliver a high quality current waveform. The specifications of these systems are ever-increasing, hence systems that push the boundaries of the existing state-of-the-art are needed to improve the performance of crucial equipment in the fields of power generation, medical diagnosis and treatment, and theoretical physics. Fulfilling the requirements of a broad range of such applications with a single modular system constitutes the main motivation of this work.

HVDC Switchgear Characterization

HVDC technology has brought the dawn of a new era for the energy transmission system. Despite the fact that HVDC links have been installed since several decades, the recent advances in power electronic

converter systems have revived the interest in this technology. Driven by a growing global environmental awareness and an ever-growing decentralized power production, often in remote places, the traditional HVAC grid, with the centralized fossil fuel driven power generation, is gradually being replaced by the more modern HVDC grid, as more and more HVDC links are installed around the globe. It is therefore commonly agreed among electric grid operators that the HVDC grid is expected to dominate the future of electric transmission mainly due to its ability to interconnect systems with different frequencies, actively control the power flow, and transmit large amounts of power more efficiently over long distances [1].

Traditional HVDC links are used for connecting two (usually asynchronous) AC systems. Nevertheless, to exploit the full potential of this technology, multiple AC systems need to be interconnected. This approach is referred to in the literature as multi-terminal HVDC grid (MT-HVDC). MT-HVDC offers several advantages such as reduced operational costs, reduced losses and increased controllabillity of the power exchange over a number of different interconnected grids, and higher redundancy [2]. Due to large technological leaps in the area of Voltage Source Converter (VSC) technology, the realization of large scale MT-HVDC networks is nowadays a realistic scenario that is worth exploring [3].

However, VSC-based MT-HVDC networks are particularly vulnerable to faults occurring at the DC-side. More specifically, in case of a short circuit at the DC-side, the VSC acts as an uncontrolled rectifier and the current is only limited by the AC-side impedance [4]. Due to the small DC-side inductance, the rate of rise of the DC current is extremely high. Therefore breaking times that are orders of magnitude shorter are required for HVDC systems, compared to their HVAC counterparts. Multiple ways to interconnect AC systems with HVDC links have been investigated in literature, but the most attractive one, in terms of efficiency, flexibility, redundancy, and cost is to interconnect the lines on the DC-side, forming a true MT-HVDC network. To do so, while retaining the possibility to disconnect parts of the system without having to disconnect the whole network, requires extensive use of HVDC circuit breakers (CB) [5].

Evidently, the HVDC-CB, is a key enabling technology for the acceptance of the MT-HVDC network and its future deployment [6]. In fact, the non-availability of commercial HVDC-CB is one of the ma-

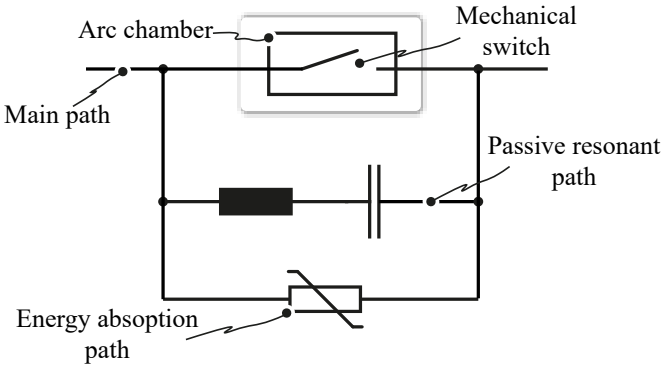

Figure 1.1: Simplified schematic of a passive-resonant HVDC-CB.

jor reasons that slows down the deployment of MT-HVDC [7]. When it comes to HVDC-CB, there are fundamental differences compared to the HVAC-CB, mainly due to the absence of a naturally occurring zero-crossing of the current. As a result, the HVDC-CB has to dissipate large amounts of energy and interrupt short circuit currents extremely fast. Despite the increased research attention over the past years, the development of the HVDC breaker is still in a rather premature level and the most suitable topology is still under investigation. The topology of the widely researched passive-resonant breaker is shown in Figure 1.1. A comprehensive review of the existing and future research activities related to the HVDC-CB can be found in [6, 8–10].

As previously mentioned, the absence of a naturally occurring zero-crossing makes the interruption of the current particularly challenging, since high current gradients need to be generated, in order to create artificial zero-crossings. Moreover, due to the absence of a high line inductance in the DC-side of the grid, the current can rise significantly in short times pushing the requirements for a fast breaker even further. A missing piece in the understanding of the breaker's operation is the understanding of the behavior of the arc that is formed in the arc chamber shown in Figure 1.1, when the mechanical switch opens.

It becomes clear that modelling the DC-arc is a crucial step towards the optimization of existing HVDC-CB topologies and the development of improved mechanical interrupters. Multiple approaches to the mod-

elling of the arc's behavior have been followed in literature over the years, but the complexity of its behavior makes the procedure rather challenging. So far, models with different levels of detail have been applied [11, 12]. The most successful simulation models are making use of transient arc-networks which are based on black box models, which require however the accurate extraction of the parameters of the arc, mainly its cooling power and its thermal inertia [13]. The intrinsic problem with the determination of these parameters arises from the fact that the cooling power of the arc is better determined by stationary currents, while the thermal inertia from currents with a steep gradients [14] .

In most of the previous methods, sinusoidal currents were used for the determination of the arc parameters because they are relatively easy to generate [15–18]. The drawback is however, that there is an obvious coupling between the current amplitude and the current gradient which does not allow the independent determination of the cooling power, and its thermal inertia. Exponential current waveforms and damped oscillation waveforms have also been applied in similar research activities, with the same disadvantages. The *High Voltage Laboratory (HVL)* at *ETH Zurich* has achieved significant progress in the field of understanding switching arcs by applying a fundamentally novel test philosophy for the extraction of its parameters [19].

The optimal waveform for the decoupling of the two crucial parameters was found to be the combination of repetitive constant current waveforms that aim for the extraction of the arc's cooling power (stationary parameter) followed by high current gradients that determine the thermal inertia (transient parameter) of the arc. In this way a simple step response analysis can be performed, and more trustworthy results can be obtained. More specifically in [20], the staircase-like current waveform with highly dynamic steps is identified as an optimal reference waveform. However, the need for high current dynamic and precision impose challenges on the design of the current injection circuitry. Nevertheless, the accuracy of the parameter determination is enhanced, since instead of fitting complex models to voltage measurements with non-ideal currents, complex test currents are applied, and a simpler evaluation of the voltage measurements of the arc is used for the parameter extraction.

A first endeavor for generating such complex waveforms was attempted by the *High Voltage Laboratory (HVL)* at *ETH Zurich* and its

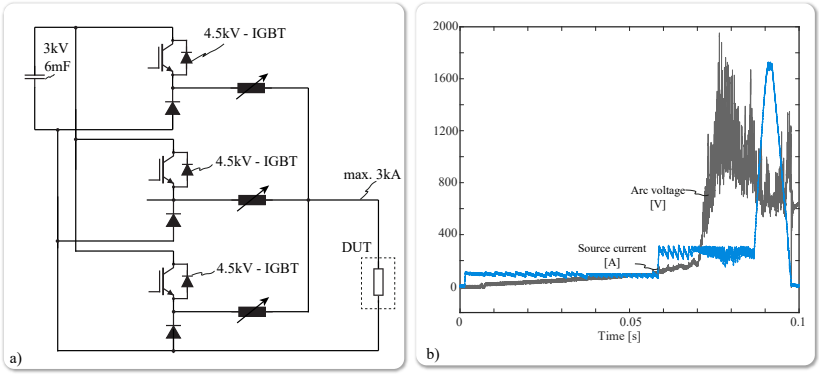

Figure 1.2: a) Schematic of the pulsed current source. b) Measurements of the arc voltage and arc current obtained with the pulsed current source at the *High Voltage Laboratory (HVL)* of *ETH Zurich* [21].

topology is shown in Figure 1.2a. Three buck modules equipped with variable inductors are connected in parallel to the device under test (DUT). Variable inductors are used to set the desired gradient of the current accordingly. Also slow switching high voltage IGBTs are used to control its amplitude. Measurements obtained with the developed prototype are shown in Figure 1.2b, where the voltage of the arc and its current are shown. The most significant results of the investigations can be found in [21] and [22], where DC-arcs are characterized under different conditions. Despite its success, the current source is limited in terms of its bandwidth, while the slow switching IGBTs do not permit the operation with a relatively low steady state ripple, as can be also noted in Figure 1.2b. Furthermore, the voltage of the source cannot be reversed, and as a result, fast step-down current gradients cannot be generated. These characteristics severely limit the scope of research.

As a response to those needs, a unidirectional arbitrary current source (UnACuSo) was developed at the *Laboratory for High Power Electronic Systems (HPE)* at *ETH Zurich* [24]. Each stack module of the UnACuSo can deliver 1.4kA of peak current for a maximum pulse length of 20ms and a maximum output voltage of 10kV. The source is based on a novel topology that consists of a multi-phase interleaved converter connected in series to a Marx-type voltage source converter, to increase the output voltage [25]. The topology of a single stack of the

developed source is shown in Figure 1.3a and a picture of the assembled hardware prototype in Figure 1.3b. The source delivers arbitrary current waveforms, with a maximum current gradient of approximately 2A/µs, combined with low load current ripple and relatively high precision. However, the relatively simple control limits its bandwidth. Furthermore, the prototype system cannot control highly dynamic loads (e.g. DC-arcs) due to the low inductance per converter module, the relatively high delays caused by the slow switching IGBTs, and the overall limited control bandwidth of the system [23]. Therefore, the UnACuSo is not suitable for the application in switchgear characterization.

In response to that, the dynamic arbitrary current source (DynACuso) has been developed in this work. The DynACuSo is based on the topology of the UnACuSo and involves several improvements in the

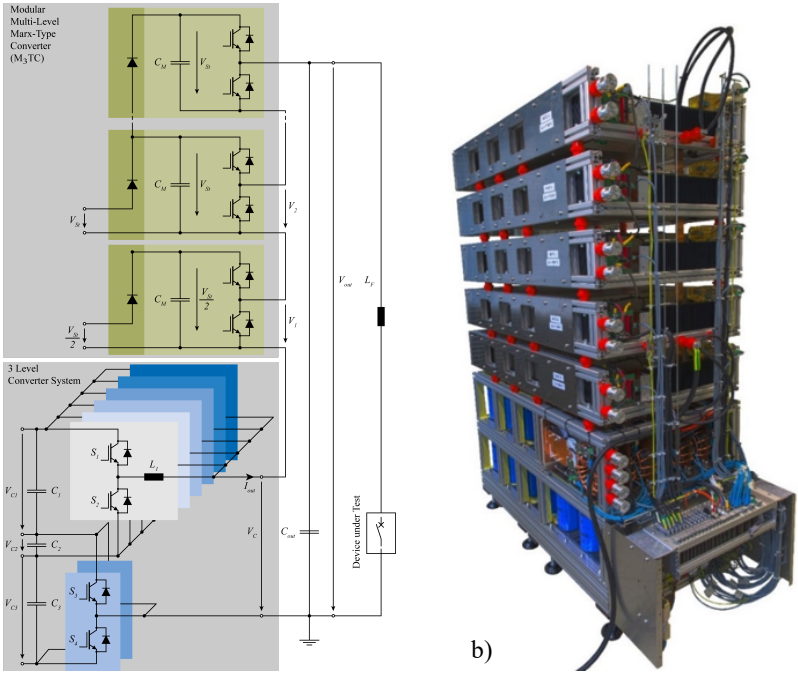

Figure 1.3: a) Schematic of the UnACuSo designed in the *Laboratory for High Power Electronic Systems* at *ETH Zurich*. b) Picture of the hardware prototype of the UnACuSo [23].

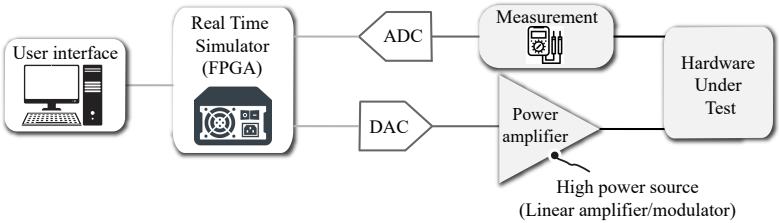

Figure 1.4: Schematic representation of a typical Power Hardware-in-the-Loop (P-HiL) Testing system.

hardware, upgraded semiconductors, improved control methods and increased controllabillity/bandwidth, specifically targeted for the application in switchgear characterization and the control of highly fluctuating loads.

Power Hardware-in-the-Loop Simulations

Hardware-in-the-Loop (HiL) simulation systems have gained popularity over the past years, since they combine the benefit of simulating parts of a system that are known and can be well-modeled with high accuracy, with experimental measurements of parts of the system that are not well-understood, and thus need to be tested. HiL testing is nowadays used in various application areas such as automotive and power systems to facilitate the development procedure [26].

Conventional HiL systems utilize relatively low power analog and digital IOs. However, for testing power devices and high power systems, the existence of a high power hardware interface [1] is necessary and therefore conventional HiL systems are insufficient. For these purposes, Power Hardware-in-the-Loop systems (P-HiL) have been developed, as they provide several advantages [27]:

- Cost-effective testing procedures since it requires minimal physical construction.
- Rapid model prototyping.
- Ability to test under critical conditions, while de-risking the testing procedure by testing in a controlled environment.

[1] hundreds of amperes/volts are often required.

On the downside, P-HiL systems usually require high power and high bandwidth amplification combined with a high reference tracking precision. The schematic of a typical P-HiL system is shown in Figure 1.4. The system comprises a user interface and a real time simulator with digital and analog IOs, that simulate the known parts of the system and a power interface. The power interface comprises the measurement system, the power amplifier, and the device under test.

Several different P-HiL systems with different levels of complexity have been reported in literature. For testing HVAC circuit breakers, the relatively simple Weil-Dobke circuit has been widely used to generate high sinusoidal currents in the kilo-amperes range [16]. A more advanced concept, based on a high power modular multilevel converter (MMC) system, used for investigating general faults on medium voltage DC (MVDC) grids is presented in [28, 29]. In [30], a P-HiL system is established, consisting of power inverters for testing low-voltage islanded micro-grids for distributed power generation. In [31], a differential boost converter system is used as switched-mode power amplifier for P-HiL simulation purposes. For increased bandwidth at a lower power level, linear amplifiers have also been utilized in P-HiL systems, as in [32].

In general, a high-end P-HiL system should feature high output current and/or voltage, superior bandwidth performance, good reference tracking capabilities and low output distortion (low output ripple). Regarding the application of P-HiL to the HVDC field, one can think of various different configurations depending on the research questions that need to be addressed. It should also be highlighted that the relevance of the method in the field of HVDC is further enhanced due to the high costs related to the physical construction of such systems, as well as the relative lack of field data at least at this point in time.

In Figure 1.5, two exemplary cases are shown for applications and testing purposes in the field of HVDC. In Figure 1.5a, a test-bed for mechanical interrupters is shown. In this case the passive circuits around the breaker (shown in Figure 1.1) can be accurately modeled in a real time simulator, where their parameters can be varied without the huge implementation effort and money investment that would be needed, if these were to be real hardware devices. On the other hand, as previously discussed, the behavior of the mechanical interrupter with its arc chamber depends on various conditions and it is rather unknown. Therefore, a power amplifier can provide the current to the mechanical breaker and the arc voltage that is measured on the terminals of the

hardware under test (HUT) can be fed-back to the real time simulator. In such a way, the development of optimized arc chambers can be facilitated.

Another example is shown in Figure 1.5b where a test-bed for stress tests is set up, for power components in an MT-HVDC grid. The MT-HVDC can be simulated in the real time simulator and one of its terminals, or a certain part of the terminals (e.g. power device or power module) can be tested without the need for extensive physical construction. Various faults can be tested and the influence of the configuration can be studied on the real hardware. Moreover, the expected fault magnitudes and over-voltages could give insights on the proper sizing of the converter components, in a risk-free testing environment.

The key enabling technology for both of the aforementioned examples, is a high power, high bandwidth current source with low ripple and high tracking accuracy. The DynACuSo that is developed as part

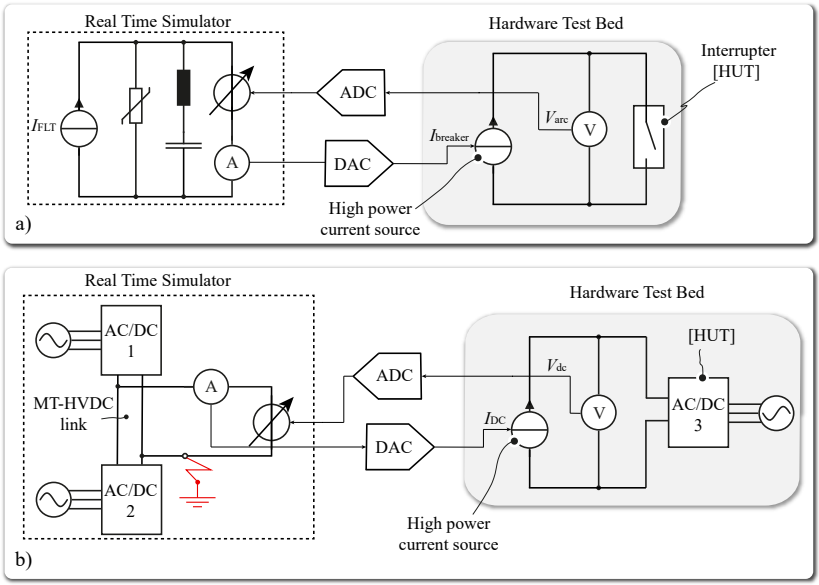

Figure 1.5: Exemplary applications of P-HiL systems for HVDC research/testing purposes. a) Test-bed for mechanical interrupters. b) Test-bed for power converters or their components (e.g. individual modules of a modular system) under critical fault conditions.

of this work can fulfill the needed specifications, and can therefore serve as the power amplifier interface for such applications to greatly facilitate the development procedure of mechanical interrupters and other high power components for HVDC applications.

Particle Accelerators and Plasma Sources

Specialized high-end power supplies are widely accepted as a necessary piece for particle accelerators. Around 30.000 accelerators are nowadays in operation around the world, with 2/3 of them used for industrial purposes and the rest for medical applications [33]. Accelerators have been around since the early 1920s, with the invention of the Cockcroft-Walton generator, and since then their contribution to science, technology and the understanding of the fundamental laws that govern the universe has been immeasurable [34].

For the acceleration of the particles, magnetic fields are needed in order to drive the particle beam and shape it according to the needs of the application [35]. These magnetic fields are usually generated by an electromagnet and a current supply is often used to drive the current of the electromagnet. The characteristics of the magnetic field, in terms of its amplitude, accuracy, and stability depend greatly on the characteristics of the current that is used to produce it. Different applications use different magnets and require different current specifications. In general, high amplitude magnetic fields with low ripple, high reproducability, and often high dynamic are required for many modern applications [36]. For example, beam deviation equipment used in accelerators with septum magnets require high amplitude current pulses with a stable flattop and fast current gradients [37].

Furthermore, several medical applications as for example cancer treatment systems [38], magnetic resonance imaging (MRI) systems [39], and proton radiation therapy systems [40] also require driving electromagnets with high current amplitudes [2], high precision, and low ripple. These systems, in order to achieve superior output ripple performance have been traditionally using linear amplifiers, but are gradually substituted by switching amplifiers due to the superior efficiency ratings, the reduced thermal management systems, and resulting operational costs [41]. In addition to the energy savings that drive the technological changes, achieving a higher dynamic performance while

[2] ranging from a couple hundreds of amperes to kilo-amperes

maintaining low output distortion could potentially have a significant impact on the overall system level performance. In order to achieve a high dynamic, when the load is an electromagnet, a high voltage pulse needs to be applied to the magnet to achieve a high di/dt, followed by a relatively low steady state output voltage, mainly to compensate the parasitic resistance of the magnet and the converter system losses.

In addition to the above, recent advances in fusion energy research have created an increased demand for high-end dynamic power supplies. In these systems, initially the arc is ignited by applying a short but high peak voltage pulse across the ignition electrode. After that a high and stable in amplitude arc current needs to be kept constant at a lower voltage amplitude [42, 43].

1.1 Requirements and Specifications

The current and voltage waveforms required by the aforementioned applications are graphically depicted in Figure 1.6. Table 1.1 lists the requirements of the different applications.

Based on these findings, a set of specifications for a multipurpose dynamic and modular current source has been determined, as shown in

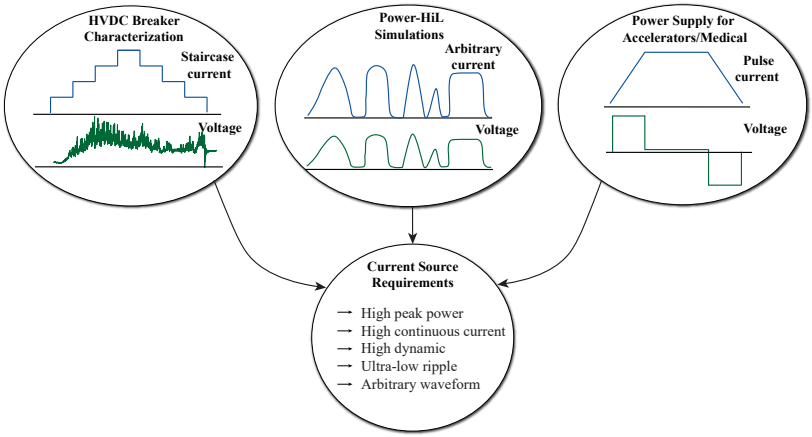

Figure 1.6: Qualitative requirements and application areas that result in the need for a multipurpose high power dynamic current source.

Table 1.1: Requirements for different applications and target specifications of DynACuSo.

	Applications		
Parameter	**Accelerators**	**P-HiL**	**HVDC**
Peak output current	up to 30kA	up to 2kA	up to 30kA
Peak voltage	up to 10kV	up to 2kV	up to 10kV
Voltage polarity	Bipolar	Bipolar	Bipolar
Load type	L	R/L	Dynamic
Current waveform	Pulse	Arbitrary	Arbitrary
Operating mode	Pulse/Cont.	Cont.	Pulse
Current rise/fall	★★★	★★★	★★★★★
Flattop ripple/accuracy	★★★★★	★★★	★★

Table 1.2. The topology of the investigated dynamic arbitrary current source (referred to in the text as DynACuSo from now on) is similar to the one designed in [23–25], where a current-shaping converter, which controls the output current of the system, is used in series with a step voltage generator (M3TC) in order to generate the required high output voltage. DynACuSo can deliver a maximum of ±10kV at the output, and has a peak current capability of 1.5kA, and its continuous current rating is 1.0kA. It should also be noted, that due to the modular design of the step voltage generator, the output voltage per stack module can be scaled with steps of 1.1kV, depending on the needs of the application. Adding DynACuSo modules in parallel can increase the current rating in steps of 1.5kA, up to the envisioned full scale source of 30kA.

Additionally, DynACuSo delivers fast current gradients to a wide range of loads, as shown in Table 1.2. The steepness of the current rise and fall depends on the maximum output voltage (number of M3TC stages installed) and eventually the total load inductance. Nevertheless, for the given load inductance range (5µH..100µH), the maximum voltage of 10kV can exceed the target gradient of >10A/µs, thanks to a combination of hardware/software design[3].

Furthermore, DynACuSo aims to push the boundaries of existing systems and explore their limitations regarding the flattop ripple cur-

[3] a detailed evaluation of the achievable dynamic of the DynACuSo with one and two installed M3TC stages can be found on Section 6.6.

Table 1.2: Target specifications of DynACuSo.

	DynACuSo	
Parameter	**Stack Module**	**Full-Scale**
Output peak current	1.5kA	30kA
Output cont. current	1.0kA	20kA
Voltage polarity	Bipolar	Bipolar
Peak voltage	±10kV	±10kV
Pulse length	10ms	10ms
Current waveform	Arbitrary	Arbitrary
Current rise/fall	>10A/µs	up to 200A/µs
Flattop ripple	500ppm	-
Load inductance		5µH .. 100µH
Load resistance		0.05Ω .. 1Ω
Load type		R/L/Dynamic(arc)

rent, which also depends on the load. For a 1kA current a 500ppm maximum load current ripple is targeted[4].

1.2 Project Outline

In the following, the objectives and research contributions of the project are briefly discussed, the structure of this dissertation is given, and the publications directly derived by the corresponding research conducted in the *Laboratory for High Power Electronic Systems (HPE)* at *ETH Zurich* are listed.

1.2.1 Project Objectives

The main goal of the project is the design, development, and experimental verification of a high power, dynamic, arbitrary current source with a modular design, that pushes the boundaries of State-of-the-Art systems, and fulfills a list of strict specifications which arise from multiple different application areas. The developed DynACuSo is the second

[4] a detailed evaluation of the achievable output ripple of the DynACuSo can be found on Sections 3.8.2 & 6.6.

generation current source, fully designed and developed at the *Laboratory for High Power Electronic Systems (HPE)*, following the Unipolar Arbitrary Current Source (UnACuSo) [23]. The subsidiary objectives of the project are listed below.

- Identification of a list of requirements for a multipurpose high-end current source.
- Identification of a suitable modular topology, and a subsequent system parameter selection routine, in order to fulfill the list of requirements.
- Optimization aiming to achieve the highest possible system level performance.
- Highly dynamic control of arbitrary loads, and demonstration of the ability to drive dynamic loads (i.e. arcs) through experimental measurements.
- Identification of optimal control schemes for non-isolated multiphase interleaved buck converters.
- Demonstration and verification of the system's capability through extensive experimental work.

1.2.2 Contributions

The scientific contributions of the project at hand are briefly summarized hereby.

- *Specification driven parameter selection routine to fulfill dynamic and ripple requirements*: A holistic approach is proposed in order to identify the parameters of the converter system and the ones of the output filter stage. The aim is to fulfill simultaneously the dynamic, ripple, and controllabillity/robustness goals.
- *Optimization of high power inductors in pulsed power applications with high continuous current rating*: An optimization routine for inductors is initially proposed, and the specifications of the inductors of the DynACuSo are used as a test case. The performance of different magnetic materials is evaluated in detail with

Pareto optimizations in terms of the resulting core material volume and efficiency. The results reveal the most suitable material for the needs of the application. Furthermore particular emphasis is laid on the thermal management concept, where potted and non-potted designs are compared in detail, revealing volume and loss tendencies for high power inductors. The results of this work lead to the extraction of general conclusions and insights regarding magnetic materials, thermal management, and the effect of the continuous current rating for pulsed power applications.

- *Design, development, and experimental validation of an adaptive hybrid control scheme for multi-phase interleaved buck converter systems*: This work proposes an adaptive hybrid controller that combines the time optimal response of the hysteretic controller during step transients with the good steady state properties of the PI controller with phase shift control during steady state. As a result, pulses with high dynamic, flattop precision, and low ripple at steady state can be achieved regardless of the parameters of the connected load. It is shown that the proposed scheme is an excellent choice for step transients.

- *Systematic optimization and comparative evaluation of different control structures for multi-phase interleaved buck converters*: In this work a generic systematic Pareto-optimization routine based on defined performance evaluation indicators and cost functions is proposed for the controller design. The investigation assumes the current shaping converter of DynACuSo as a test bench and investigates, optimizes, and compares five control schemes, revealing their advantages and disadvantages. Experimental work is also used to verify the results of the analysis.

- *Design and development of a current transformer with adaptive burden resistance for high sensitivity ripple current measurements in pulsed power systems*: A current transformer concept with adaptive frequency response is designed based on a proposed procedure, in order to measure the ripple of the current that is superimposed on a high DC current during flattop. The developed prototype current probe achieves a resolution of 0.125A/V, a settling time of approximately 16µs (after a step transient), and a wide bandwidth 2.5kHz-27MHz. Experimental measurements

verify the analytical calculations and the applicability of the solution for pulsed power applications is demonstrated.

- *Design and development of an active adaptive output filter for pulsed applications with ultra-low ripple specifications*: In order to achieve the strict ripple requirements of various applications, the developed AC current probe is used to feedback the load current ripple to an active output filter that further attenuates the load ripple of the system, with the use of a linear amplifier. The prototype filter demonstrates experimentally active attenuation up to 500kHz, and outperforms a passive solution at the expense of increased complexity and implementation effort.

- *Development of a functional prototype hardware demonstrator*: The DynACuSo has been designed, developed and experimentally tested under various conditions. The prototype system is used to validate the design considerations, models and methodologies used as part of the research activities of this work. The prototype achieves 1.5kA peak current, 1kA continuous current and up to 1.1kV output voltage.

- *Robust control and complex current waveform generation through DC-arcs*: In this work the ability of the developed DynACuSo to produce stair-case like current waveforms, with very short current rise/fall times through a DC-arc is demonstrated experimentally. The result opens new research opportunities for further DC-arc investigation and modelling efforts.

1.2.3 Further Contributions

During the course of the project, another scientific project has been undertaken, and is not described in this work but is mentioned in this section for completeness:

- *Multi-channel, high speed data link for isolated measurement data transmission.* An optical communication link, able to transmit two measurement data signals along with their respective clock, with a transmission speed up to 200MHz have been designed and developed. The communication link is based on a novel light intensity modulation scheme and various implementations have

been proposed based on the needed bandwidth and the implementation cost. The results of this work package have been presented in [44–46].

1.2.4 Thesis Outline

The next chapters of this work are outlined as follows.

- **Chapter 2** introduces the modular topology of the DynACuSo that can be used according to the needs of the application, and describes its operation principle. It shortly introduces the main parts of the system, and briefly describes qualitatively the influence of different parameters on the overall performance of the system.

- **Chapter 3** deals with modelling, design, and optimization of non-isolated multi-phase interleaved buck converters. The converter system is analytically modeled at transient and steady state and a systematic method is developed for the choice of the converter and output stage parameters, in order to fulfill simultaneously the high dynamic and low ripple requirements. A passive adaptive output filter stage that is suitable for pulsed-applications with high dynamic and low ripple is demonstrated and its benefits compared to standard solutions are highlighted. Furthermore, extensive research is conducted on high current inductors for pulsed and continuous operation. More specifically, the effect of the core material type on the core volume and efficiency of the power inductor is discussed, along with the effect of potting the inductor core in epoxy resin, for better thermal management. The effect of the continuous current rating to pulsed current rating ratio on the overall volume and losses of the system is also investigated for different materials. The analytical inductor models are finally verified by experimental measurements with the developed hardware prototype. Finally, the multi-phase interleaved prototype system is shown and its operation under different conditions is verified.

- **Chapter 4** optimizes and compares systematically five different control schemes for multi-phase interleaved buck converter systems, considering the current shaping converter of the DynACuSo

as a test-bench. Among these prominent control schemes an adaptive hybrid controller is proposed. The controller combines the time optimal response of a hysteretic controller, with the good steady state properties of a PI controller, to deliver excellent performance in step transients. Furthermore, generic performance evaluation indicators are defined along with a general optimization routine, and a cost function to determine the optimum point in a systematic way. The developed methodology can be extended for the optimization of any controller regardless of the converter system. The different controllers are then compared with simulations and experiments, providing useful insights on their advantages and disadvantages.

- **Chapter 5** initially discusses an AC current measurement probe tailored for pulsed currents with a very low ripple superimposed on high DC currents. A design procedure for such probes is shown and the different trade-offs are revealed. A current measurement probe is then proposed to achieve high sensitivity combined with a wide bandwidth and a low settling time. The developed current probe is then used as a reference generator to a high bandwidth active filter which can be used instead of a passive output filter. The active filter is analytically modeled and experimentally verified. The comparison with a passive filter reveals its superiority at the expense of increased implementation effort. The combination of the developed current probe and the active filter and their autonomous operation for pulsed shaped currents is demonstrated experimentally, with the high power prototype system.

- **Chapter 6** presents in detail the developed hardware prototype, including the step voltage generator (responsible for the generation of the high output voltage), the input capacitor bank (main storage element of the current-shaping converter system), and the interface converter system (responsible for providing the flexibility to operate the system both in pulsed as well as in continuous operation mode). The topology, the modes of operation, the design considerations and the control and communication design for the prototype systems are explained, and relevant experimental results are shown. Finally, the integration of the control of the step voltage generator into the overall control of the system is shown and experimental measurements with the complete prototype sys-

tem showcase the abilities of DynACuSo. More importantly, the ability of DynACuSo to generate staircase-like current waveforms with short rise/fall times and control the currents with robustness through DC-arcs is demonstrated with relevant experimental measurements.

- **Chapter 7** finally summarizes the main outcomes of the research project and lists possible suggestions for future improvements.

1.2.5 List of Publications

The findings of this research, including several of the text sections, tables and figures have been published in various scientific conferences and journals, which are listed chronologically in this section.

1. G. Tsolaridis and J. Biela, "Modular, Highly Dynamic and Ultra-Low Ripple, Arbitrary Current Source for Kicker Magnets and Plasma Research", *Pulsed Power Conference (PPC)*, Brighton, UK, 2017 [47].

2. G. Tsolaridis and J. Biela, "Hybrid Control Concept for Highly Dynamic Buck Converter Systems", *19th European Conference on Power Electronics and Applications (EPE, ECCE Europe)*, Warsaw, Poland, 2017 [48].

3. G. Tsolaridis and J. Biela, "Interleaved hybrid control concept for multi-phase DC-DC converters", *IEEE Energy Conversion Congress & Expo (ECCE)*, Cincinnati, Ohio, USA, 2017 [49].

4. G. Tsolaridis and J. Biela, "Flexible, Highly Dynamic, and Precise 30-kA Arbitrary Current Source", *IEEE Transactions on Plasma Science*, vol 46, Oct. 2018 [50].

5. G. Tsolaridis, S. Fuchs, A. Jehle M. Pritz, P. Alff and J. Biela, "High Speed, Multi-Channel, Isolated Data Transmission with a Single Fiber Based on Intensity Modulation", *20th European Conference on Power Electronics and Applications (EPE, ECCE Europe)*, Riga, Latvia, 2018 [44].

6. G. Tsolaridis, N. Patzelt and J. Biela, "Output Filter with Adaptive Damping for Interleaved Converters with Ultra-Low Ripple

and High Dynamic", *21st European Conference on Power Electronics and Applications (EPE, ECCE Europe)*, Genova, Italy, 2019 [51].

7. M. Pritz, Fuchs, A. Jehle, G. Tsolaridis,and J. Biela, "Low-Cost Multi-Channel Data Transmission over a Single Plastic Optic Fiber for Isolated Sensing Applications", *21st European Conference on Power Electronics and Applications (EPE, ECCE Europe)*, Genova, Italy, 2019 [45].

8. Fuchs, M. Pritz, G. Tsolaridis, A. Jehle and J. Biela, "Single Plastic Optical Fiber, Multiple Channel Data Link for Sensing Applications With PCB Implemented Transmitter and Receiver", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Dec. 2019 [46].

9. G. Tsolaridis, P. Seiler and J. Biela, "High Sensitivity Current Transformer with low Settling Time, for Magnified AC Current Measurements in Pulsed Current Applications", *22nd European Conference on Power Electronics and Applications (EPE, ECCE Europe)*, Lyon, France, 2020 [52].

10. G. Tsolaridis, M. Jeong and J. Biela, "Systematic Evaluation of Current Control Concepts for Interleaved Buck Converters", *IEEE Access*, 2021.

11. G. Tsolaridis, and J. Biela, "A High Power and Fast Arbitrary Current Source suitable for Power Hardware-in-the-Loop Simulations", *Pulsed Power Conference*, Conf. Proceedings, Denver, 2021.

1.2.6 Patents

During the course of the project, a scientific project has been undertaken, resulting in the following patent submission.

- J. Biela, S. Fuchs, A. Jehle and G. Tsolaridis, "Verfahren und Schaltung zum Erzeugen resprektive zum Empfangen eines Uebertragungssignals zur Signal Übertragung mit mehreren Kanälen über einen optischen Leiter", CH715149A2, Jan. 2021.

Interim Summary

High-power dynamic current sources which are able to generate controllable current waveforms are nowadays a key enabling technology for a wide range of different applications. They can be used to supply accelerator magnets and plasma sources for future fusion energy research, and serve as a test-bed for P-HiL simulation setups and characterization of future generation HVDC breakers. These systems usually require a high dynamic combined with low output current ripple and a relatively high accuracy while driving resistive, inductive or even dynamic loads, such as arcs. Due to their strict specifications, these converter systems are usually custom designed, tailored to the target application.

Based on the performed literature review, a list of specifications for a modular, dynamic high-end current source has been established, in order to fit the requirements of a wide range of applications. Each stack module of the DynACuSo can provide up to 1.5kA of arbitrary current waveform (in pulsed mode) and up to 10kV of bipolar output voltage. The source can operate continuously with up to 1kA current. More importantly, it can provide more than 10A/µs current rise/fall gradient for a wide range of inductive and resistive loads, and an output current ripple of less than 500ppm at 1kA is targeted. Additionally, the source can be used to drive fluctuating, dynamic loads with robustness and the necessary high bandwidth.

2
System Overview

Motivation

High power pulse power supplies, with a set of special specifications, like the ones described in Chapter 1 are usually tailored to the needs of a specific application, in which they are intended to be used. The customized nature of those systems increases the complexity during the design process, involving the definition of the system's topology and subsystems, along with the identification of the possible design trade-offs, when it comes to the top-level performance of the system. The need for a customized topology is even more pronounced when flexibility is required for systems with a broad range of potential applications, that aspire to fulfill sets of specifications that arise from different application areas. For these systems, special topologies need to be envisioned and a degree of modularity needs to be established in order to allow them to fit into different applications, with the minimum number of modifications to their hardware/software.

The majority of modern high power systems utilize switching power supplies, due to their high efficiency rating and ever increasing performance, compared to linear amplifiers. An investigation of different topologies that could fit into an application like the DynACuSo has been performed in [23]. A more systematic comparison of different concepts and topologies is considered to be outside of the scope of this work. Nevertheless, the concept of the DynACuSo is presented in detail in this chapter, together with its operational principle under various operating conditions and loads. A modular topology is envisioned and its subsystems are defined. Furthermore, design trade-offs are discussed,

and the effect of the different parameters on the system level performance is presented and qualitatively analyzed, setting the foundation for the research activities that follow in the upcoming chapters of this work.

2.1 DynACuSo Concept

The topology of a single module of the DynACuSo, is shown in Figure 2.1. It is designed in a modular way, according to the specifications listed in Table 1.2. and can deliver a maximum bipolar voltage of ±10kV and a peak current of up to 1.5kA to a resistive, inductive or dynamic load, while fulfilling its dynamic and ripple performance specifications.

The source module consists of the following building blocks:

- **Interface converter system**: A simple converter that provides the system with the flexibility to operate in pulsed and continuous mode.
- **Input capacitor bank**: A split DC-link that acts as the main storage element for delivering the high peak power pulse for several milliseconds.
- **Current shaping converter**: A dynamic multi-phase interleaved buck-type converter, responsible for controlling the current, and shaping arbitrary current waveforms.
- **Output filter**: Different topologies and concepts are investigated throughout this work regarding the system's output stage. Despite its negligible size compared to the rest of the system, it has a significant role in the overall system performance, and affects both the dynamic, as well as the ripple.
- **Step voltage generator**: A solid-state Marx-type Modular Multilevel Converter (M3TC), consisting of H-bridge modules, responsible for generating a step-like output voltage, by inserting or by-passing its pre-charged capacitors.

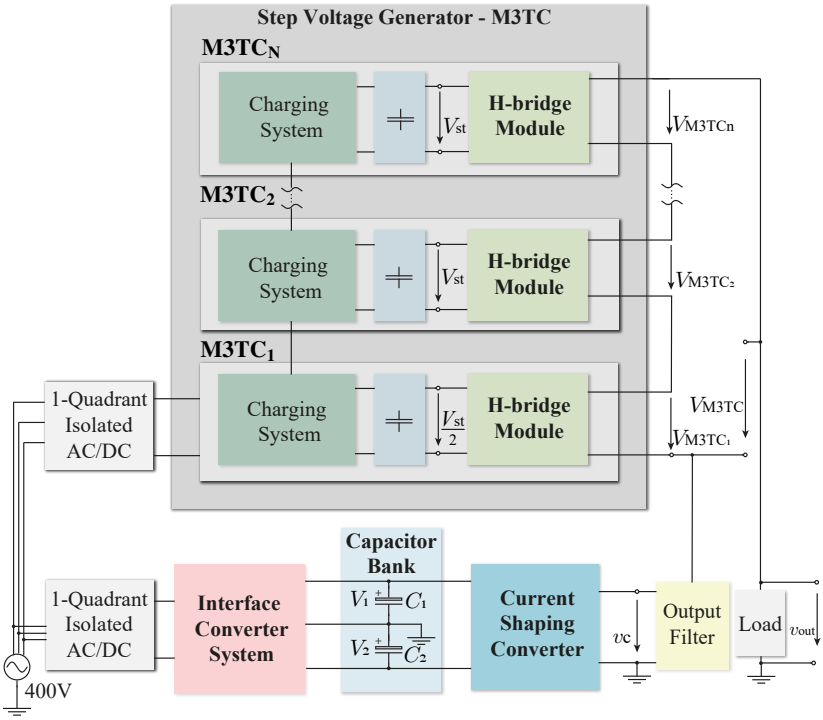

Figure 2.1: Representation of DynACuSo's topology and its main building blocks.

2.1.1 Principle of Operation

This section describes the basic operation principle of the source module in a simplified manner, for resistive, inductive and dynamic loads. Initially, Figure 2.2 shows the equivalent electrical circuit of DynACuSo. The current shaping converter (interleaved buck converter with split DC-link) is modeled here as a step voltage source (u_{con}), that can generate a voltage between V_1 and $-V_2$. It is connected in series to an inductor L_{eq}, which represents the equivalent inductance of the parallel connected modules of the interleaved converter, as will be revealed later on. The step voltage generator is modeled as a voltage source (V_{M3TC}) that generates discrete voltage levels with an amplitude of $0.5 \cdot V_{\mathrm{st}}$, which is the pre-charged level of $\mathrm{M3TC}_1$, noted in Figure

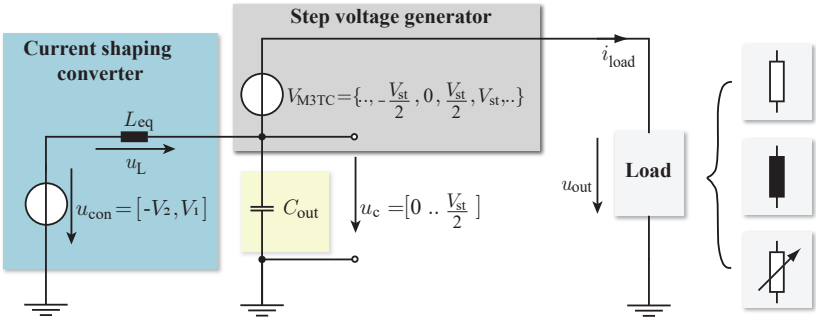

Figure 2.2: Simplified equivalent circuit of DynACuSo, with different loads connected at its output.

2.1. The output filter stage is at this stage simplified to a capacitor C_{out}. The three considered cases for the load are also shown, with the dynamic load being shown as a variable resistor.

The basic operating principle of the source module is illustrated in **Figure 2.3a**, where a rising current i_{load} is generated through a purely resistive load.

- At t_0: As the output current i_{load} increases, the converter output voltage v_{c} starts to increase too.
- At t_1: Voltage v_{c} reaches $0.5V_{\text{st}}$, which is the pre-charged value of M3TC_1. At that point, M3TC_1 is turned on and V_{M3TC} becomes $0.5V_{\text{st}}$, while v_{c} immediately collapses to 0V [1].
- At t_2: Voltage v_{c} reaches again $0.5V_{\text{st}}$ and M3TC_1 is turned off while M3TC_2, which is pre-charged to V_{st}, is turned on. Then, V_{M3TC} becomes equal to V_{st} and v_{c} collapses again to 0V.
- At t_3: Voltage v_{c} reaches $0.5V_{\text{st}}$, M3TC_1 is turned on again, and V_{M3TC} becomes $1.5V_{\text{st}}$.

The operation of DynACuSo when controlling a constant current through a dynamic load, that can be modeled, for simplicity, as a variable resistor is shown in **Figure 2.3b**.

[1] assuming that the capacitance C_{out} is small

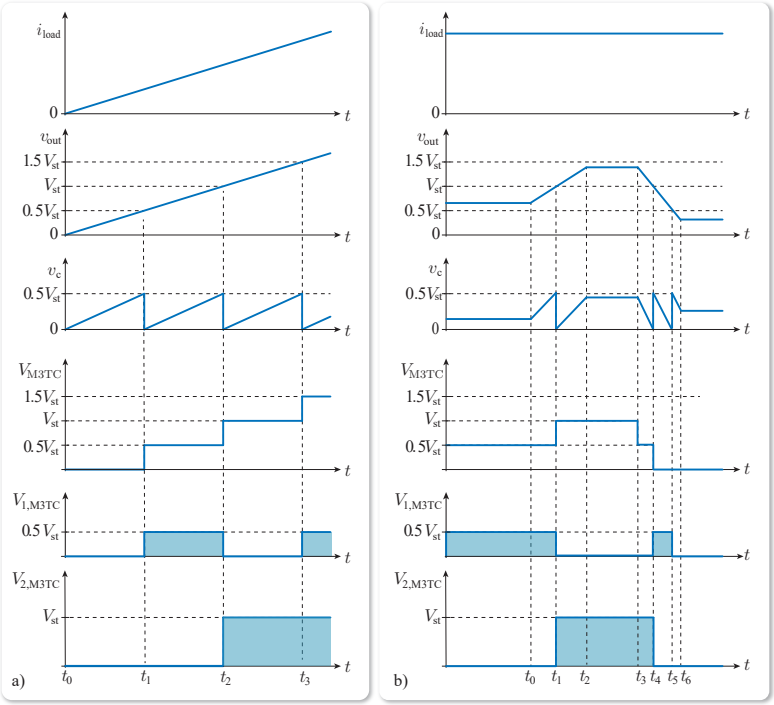

Figure 2.3: Operation principle of the DynACuSo. a) Rising load current through a purely resistive load. b) Constant current through a dynamic load.

- At t_0: The system is already at steady state, and since the output voltage v_{out} is higher than $0.5V_{st}$, M3TC$_1$ is inserted and V_{M3TC} is $0.5V_{st}$. A load disturbance occurs (e.g. load resistance is increasing) and in order to keep the current constant, the interleaved system is increasing output voltage v_c.
- At t_1: Voltage v_c reaches $0.5V_{st}$. As in the previous example, M3TC$_1$ is removed, and M3TC$_2$ is inserted. As a result V_{M3TC} becomes equal to V_{st}, while v_c collapses to 0V.
- At t_2: A new steady state is reached, and v_c remains constant.
- At t_3: A new load disturbance occurs, and the output voltage v_{out} decreases. In a similar way, the interleaved converter keeps the

current constant by decreasing v_c.

- At t_4: Voltage v_c reaches 0V. Then M3TC$_2$ is removed andM3TC$_1$ is inserted, making V_{M3TC} equal to $0.5V_{st}$. At that point v_c rapidly increases to $0.5V_{st}$.
- At t_5: Voltage v_c is reaching 0V again and M3TC$_1$ is removed too, while v_c increases rapidly again to $0.5V_{st}$.
- At t_6: A new steady state is reached, and v_c remains constant.

When the load is mainly inductive, the operation of the source module is slightly different. **Figure 2.4** shows a simplified example, of a pulse-shaped current through a mainly inductive load.

- At t_0: the load current is rising and the output voltage is given by (2.1), where L_{load} is the inductance of the load, while the parasitic resistance of the load (R_{load}) is neglected for clarity. Since v_{out} in this example is higher than V_{st} but lower than $1.5V_{st}$, only M3TC$_2$ is inserted during the rise of the output current. Based on the equivalent circuit of Figure 2.2, (2.1)-(2.2) are derived and the required v_c can be calculated.

$$v_{out} = L_{load} \cdot \frac{di}{dt} \qquad (2.1) \qquad\qquad v_c = v_{out} - V_{M3TC} \qquad (2.2)$$

- At t_1: the transient is over and therefore, the output voltage decreases rapidly to $V_{out,ss}$, which is usually low and stems from the losses of the inductive load. Since $V_{out,ss}$ can be fully covered by the current shaping converter, V_{M3TC} becomes 0V, thus bypassing all M3TC stages, and resulting to $V_{out,ss} = V_{c,ss}$.
- At t_2: The output current i_{load} is decreased with a constant gradient. In this example, $V_{out,f}$ lies between -V_{st} and -$1.5V_{st}$ and in order to keep the current shaping converter inside its operating region [0..$0.5V_{st}$], both M3TC$_1$ and M3TC$_2$ are inserted and V_{M3TC} becomes -$1.5V_{st}$. Based on (2.2) the required v_c can be calculated.

In addition to the above, as shown in **Figure 2.5**, the step voltage generator can facilitate the transients and increase the performance of the DynACuSo. The example assumes a purely resistive load, but the same principle can be applied to inductive loads.

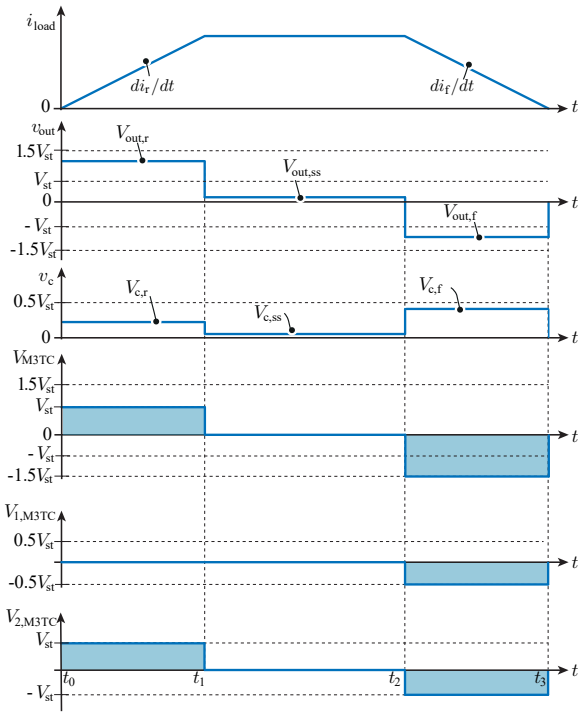

Figure 2.4: Operation principle of the DynACuSo feeding a pulsed-shaped current through an inductive load.

- At t_0: A step-up transient is initiated. Instead of waiting until v_c reaches $0.5V_{st}$, the system can immediately insert $M3TC_1$. In this way, V_{M3TC} becomes $0.5V_{st}$, as soon as the transient starts, and v_c collapses immediately to $-0.5V_{st}$. Then the maximum voltage that the system can apply across the inductors L_{eq} becomes $V_1+0.5V_{st}$, where V_1 is the voltage level of the upper capacitor of the split DC-link. Therefore, a higher current gradient can be generated.

- At t_1: Voltage v_c reaches 0V and in order to keep accelerating the transient, V_{M3TC} becomes V_{st}, by bypassing $M3TC_1$ and inserting $M3TC_2$. Due to this action, v_c collapses again to $-0.5V_{st}$ and the voltage across L_{eq} returns to its maximum value $V_1 + 0.5V_{st}$.

- At t_2: The transient is over and the system needs to enter its

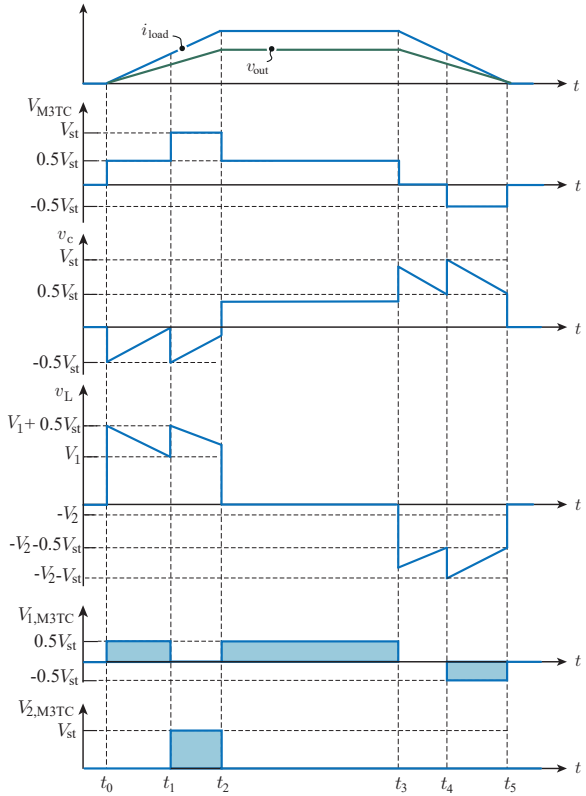

Figure 2.5: Operation principle of the DynACuSo with a resistive load and an improved control strategy fo increased dynamic performance during step transients.

steady state. To do so, the current shaping converter needs to return inside its operating region to be able to control the flattop of the pulse. Therefore in this example, V_{M3TC} returns to $0.5V_{\mathrm{st}}$ and v_{c} increases. The average voltage across the inductors V_{L} becomes 0V during flattop.

- At t_3: A step-down transient is initiated. In order to increase the dynamic performance, $\mathrm{M3TC}_1$ is bypassed immediately, V_{M3TC} becomes 0V and v_{c} increases by $0.5V_{\mathrm{st}}$. In this way, the maximum negative voltage that can be applied across L_{eq} becomes $-V_2 - v_{\mathrm{c}}$,

where V_2 is the voltage level of the lower capacitor of the split DC-link, shown in Figure 2.1.

- At t_4: Voltage v_c has reached $0.5v_c$, and in order to keep the high dynamic, V_{M3TC} becomes -$0.5V_{st}$, by inserting $M3TC_1$ in the negative direction. As a result, v_c becomes V_{st} and the voltage across L_{eq} becomes $-V_2 - V_{st}$.
- At t_5: The transient is over as i_{load} reaches 0A. $M3TC_1$ is then bypassed and V_{M3TC} returns to 0V.

It should be clarified, that the aforementioned description depicts a rather simplified operation of the system, without taking into account its non-idealities, and therefore depicts a rather simplified operation. In the real system, several adaptations need to be applied, in order to account for non-idealities such as measurement noise and delays, limited control bandwidth and semiconductor turn on/off times. The non-idealities have a negative influence on the system's ideal performance as they can only partially be compensated. Nevertheless, the operation principle of the actual system remains as described in the present Chapter, while the effect of the aforementioned non-idealities are discussed in more detail in Chapters 4 and 6.

2.1.2 Subsystems and Modularity

The detailed topology of DynACuSo is given in Figure 2.6, where the building blocks of Figure 2.1 are replaced by their respective electrical circuits. The topology is similar to the one described in [23].

A 6-phase interleaved 2-level buck converter with split DC-link is used as a current shaping converter, in anticipation of the results of Chapter 3. The split DC-link is used in order to enable the controllability of the current waveform when the converter voltage v_c is around 0V, and slightly enhances the dynamic performance of the system during step down transients. In this way, the buck type converter can generate $\{V_1, -V_2\}$ with respect to the ground. The interleaved concept increases the current rating of the converter system, as well as its modularity, and helps minimizing the output current ripple, which is discussed in detail in Chapter 3.

In order to reduce the ripple and increase the controllability of the current (i.e. increased bandwidth), a high switching frequency is desirable and therefore SiC devices are used for the interleaved converter

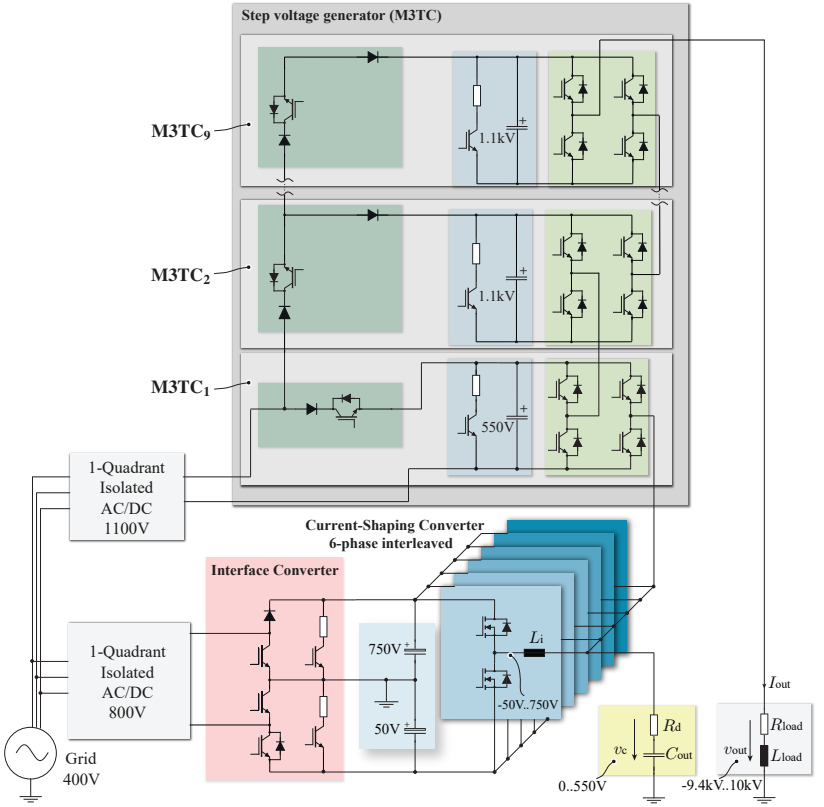

Figure 2.6: Detailed electrical schematic of the DynACuSo, along with the main chosen voltage levels.

modules. SiC devices are commercially available and industrially employed mainly with blocking voltages of 1.2kV and a wide range of current ratings. Based on the availability of SiC devices, the total DC-link voltage is chosen to be 800V. The maximum input voltage levels of 750V and 50V are chosen in order to allow sufficient control margin, when the voltage v_c is around its operating limits $v_c = [0, 550\text{V}]$.

For the step voltage generator, up to nine bipolar M3TC stages are connected in series, consisting in principle a solid-state Marx-type generator. Since the M3TC is only responsible for the generation of the

Table 2.1: Voltage levels/ratings used in the DynACuSo.

Description	Symbol	Voltage
Upper input capacitor	V_1	750V
Lower input capacitor	V_2	50V
Converter output voltage	v_c	0..550V
M3TC stage voltage	V_{st}	1.1kV
Max. output voltage	v_{out}	-9.4kV..10.1kV
Converter MOSFET rating		1.2kV
M3TC stage 1 IGBT rating		1.2kV
M3TC stage 2-9 IGBT rating		1.7kV

staircase output voltage, its dynamics are relatively slow, and a high switching frequency is not necessary. Nevertheless, reacting to sudden changes in the load (e.g. DC-arcs) requires semiconductor devices with short switching times. In this case, conventional silicon IGBTs are chosen. The stage voltage V_{st} is chosen to be 1.1kV based on the commercial available silicon IGBT modules. The total output voltage of the M3TC can be designed to be between ± 0.55 kV (if only one stage is used), with a step of ± 1.1kV, up to ± 9.35kV (if 9 stages are installed), in order to fit the needs of different applications. The capacitors of the M3TC stages are charged in parallel between pulses, by a low-power capacitor charger[2].

The electrical schematic of the interface converter is also depicted in Figure 2.6. The simple topology enables the charging of both capacitors of the split DC-link with the use of a single-quadrant standard 800V isolated AC/DC power supply.

It should be highlighted that choosing a lower voltage level for V_{st} would enable the use of faster devices for the step voltage generator (i.e. lower blocking voltage rating), and allow the M3TC to react faster to dynamic changes of the load, such as the ones described in Figure 1.2. However, that would limit the use of the SiC devices of the current shaping converter to a lower fraction of their maximum capabilities, and would require more M3TC stages to cover the 10kV range, which usually relates to increased implementation effort and increased costs. On the

[2]details regarding the charging concept of the step voltage generator are given in see Section 6.2.

Table 2.2: Effect of increasing the value of the main design parameters on the performance of DynACuSo.

	Current Gradient	**Current Ripple**	**Bandwidth & Control**	**Power Losses**	**Cost & Effort**
n	↑	↓	↑	↓	↑
L_i	↓	↓	↑	-	-
f_s	-	↓	↑	↑	-
V_1	↑	↑	↑	↑	↑
V_2	↑	↑	↑	↑	↑
C_out	↓	↓	↑	-	-
R_d	↑	↑	↑	-	-
N	↑	-	-	↑	↑
V_st	↑	-	-	↑	↑

other hand, choosing a higher voltage level for V_st, would require to extend the operating range of the current shaping converter. This could be done either by changing the devices of the current shaping converter to a 1.7kV blocking voltage class, or by using a multilevel topology. Nevertheless, the modularity of the system would be compromised, and slower devices with higher blocking voltage ratings would be required for the M3TC, severely limiting its performance with dynamic loads. The voltage levels/ratings used in the DynACuSo are summarized in Table 2.1.

2.1.3 Design Parameters and Performance

As previously discussed, the choice of the voltage level is mainly driven by the availability of semiconductor devices, and the required modularity of the system. However the choice of the rest of the main design parameters is not obvious and requires a holistic consideration of the trade-offs that arise. Table 2.2 lists the main design parameters and gives a qualitative indication of the impact that an increase in their values would have in the performance of the system, provided that all other parameters remain constant. In this table, n refers to the number of interleaved modules of the current shaping converter, f_s to their

switching frequency, N refers to the number of installed M3TC stages, and the rest of the symbols are as noted in Figure 2.6. A green arrow corresponds to a positive change, in contrast to a red arrow which corresponds to a negative change[3].

At first, increasing the number of phases n, while keeping the module inductance L_i constant, would increase the maximum current gradient that can be generated since the equivalent inductance L_eq (Figure 2.2) would be lower. Moreover, the current ripple reduces, due to the additional ripple cancellation offered by the interleaving concept, and the bandwidth of the system increases,since the effective switching frequency increases linearly with n. Regarding the power losses, the semiconductor area is increased and therefore the conduction losses of the semiconductors are reduced (assuming that the same semiconductor devices are used), and although the switching losses are increased, in general the power losses are expected to decrease. A more comprehensive investigation of the effect of n on the efficiency of DC-DC converters can be found in [53]. On the other hand, increasing n is associated with higher cost and higher implementation effort.

An increase in the module inductance value L_i results in an overall decreased current gradient but also decreased current ripple. The controllability in this case is higher, because the natural robustness of the current shaping converter against sudden load changes is increased. Regarding the power losses and the cost/effort, these values are difficult to be assessed without further investigation, and depend on many other design parameters of the inductor itself. It can be said however, that a higher inductance value would require a larger inductor volume and therefore more core material, which is a driving factor for the implementation cost.

Increasing the module's switching frequency f_s results in a decreasing ripple and increased bandwidth, although the maximum current gradient is unaffected. Nevertheless, higher switching frequency is associated with higher semiconductor losses. Additionally, increasing the input voltage levels V_1 and V_2 results in a higher current gradient, since a higher voltage can be applied across the equivalent inductance L_eq, but also the current ripple is increased. Moreover, an increase in the DC-link extends the operating range of the current shaping converter, and therefore increases its controllability, but is also associated with

[3]e.g. a bandwidth increase is a positive change indicated with a green arrow, but a power losses increase is a negative change indicated with a red arrow.

higher semiconductor switching losses. A higher cost is noted for this case in Table 2.2 mainly due to the need to upgrade the semiconductor devices and the input capacitor to non-industry standard ratings.

Figure 2.6 simply depicts the output filter as a capacitor C_{out} in series to a resistor R_{d}. The resistor could either be the parasitic resistance of the capacitance, or a damping resistance[4] in order to improve the loop properties, as demonstrated in more detail in Chapter 3. Clearly these two parameters are contradicting each other in terms of current gradient and ripple attenuation. Increasing C_{out} would result in a decreased load current gradient, but also an increased current ripple attenuation. On the other hand, increasing R_{d} practically reduces the effective capacitance of the filter and counteracts the previous changes.

Regarding the design parameters of the step-voltage generator, only the number of stages N and the voltage of the stage V_{st} are considered in Table 2.2. Clearly, a higher number of installed M3TC stages, and a higher voltage per stage increase the current gradient, especially with inductive loads that require a high voltage. Both however are associated with higher costs and add significant losses to the system. Likewise, an increase in V_{st} would require an increased semiconductor blocking voltage rating, which would lead to higher conduction losses and usually higher costs.

2.1.4 Operation Modes and Charging Concept

a. Pulsed operation mode

During the pulsed mode of operation, DynACuSo generates a high peak output power for a relatively long time duration (i.e. pulse lengths in the millisecond range). In order to avoid interruptions in the local grid, the source module is initially charged before the pulse by external power supplies (shown in Figure 2.6). The 800V supply and the interface converter are used to charge the input capacitor bank of the split DC-link, one at a time, and the detailed operation is described in Section 6.4.

Between each pulse, DynACuSo needs to return to its initial condition. To do so, the upper capacitor of the DC-link C_1 needs to be recharged, while the lower capacitor C_2 needs to be discharged, since for a unidirectional positive load current i_{load}, C_1 is discharging while C_2 is charging during the pulse. In the topology of Figure 2.6, the

[4] or even a linear operational amplifier as discussed in Chapter 5.

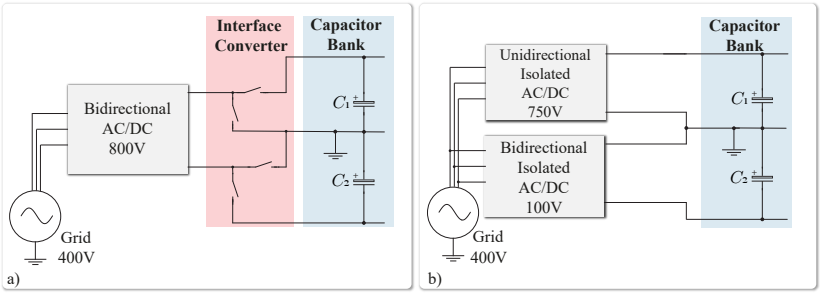

Figure 2.7: Alternative charging concepts for the input capacitor bank in pulsed operation mode. a) Charging with a single bidirectional supply and an interface converter system. b) Charging with two separate supplies.

800V supply is used to recharge C_1, while the discharge resistors of the interface converter are used to discharge capacitor C_2. The M3TC capacitors are re-charged by the 1.1kV supply, independently from the input capacitor bank.

Alternative solutions for the charging concept of the input capacitor bank are shown in Figure 2.7. Figure 2.7a makes use of a single bidirectional supply and a slightly different interface converter that is here illustrated using generic switches. In this way, the energy of the lower capacitor C_2 would not be lost between pulses. Figure 2.7b makes use of two separate supplies, one for C_1, which needs to be a standard 750V unidirectional supply and one for C_2 which needs to be a bidirectional 100V supply, to charge and discharge it accordingly. The interface converter in this case is not needed and a simple discharge circuit for C_1 would need to be added, while C_2 could simply discharge through the bidirectional supply, returning its energy to the grid.

b. Continuous operation mode

During the continuous mode of operation, the input capacitor bank is supplied by the external power supply, which needs to provide the necessary power to the load, as well as to compensate the losses of the system. Note that if the pulsed mode of operation is not needed, the input capacitor bank does not need to store a high amount of energy, but just to buffer the energy and deliver it to the load during the transients. Therefore, if pulsed operation mode is not necessary, the capacitor bank

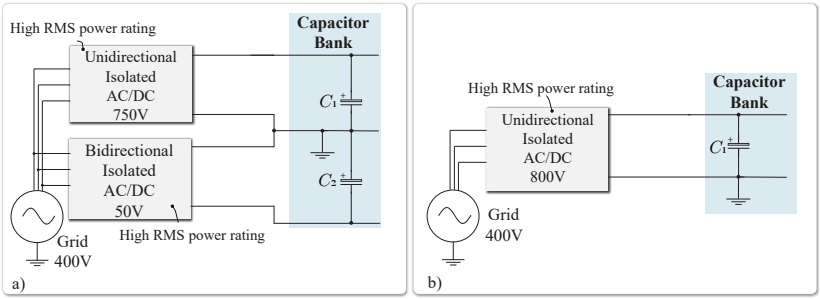

Figure 2.8: Alternative supply concept for the source module in continuous mode of operation. a) Two high power supplies needed to provide the power to the split DC-link. b) Single supply without split DC-link.

can be greatly reduced in capacitance value (and size).

Nevertheless, the topology of Figure 2.6 can operate in continuous mode only when the lower capacitor of the input bank C_2 is discharged and bypassed, through the switches of the interface converter. The capacitors of the M3TC are only used during the transients in this case, since at steady state the output voltage needs to be low, as the operation example of Figure 2.4, when supplying purely inductive loads. In this case, the capacitors of the M3TC do not need to be re-charged during operation and need only to provide the high output voltage at step-up and step-down.

Figure 2.8a shows the alternative topology, in order to operate the source module with split DC-link in continuous operation mode. Note that the bi-directional source that supplies the input capacitor C_2 in this case, needs to have a high RMS power rating and a peak current rating of 1kA, which increases dramatically its cost. On the contrary, Figure 2.8b shows the input stage when controllability of the current around $v_{\text{out}} = 0\text{V}$ is not needed. In this case, the split DC-link would not be needed and the system is simplified, since the interface converter becomes also obsolete.

2.2 Full-Scale Source

In the introductory chapter multiple applications, that have significantly higher current ratings compared to the 1.5kA peak current rat-

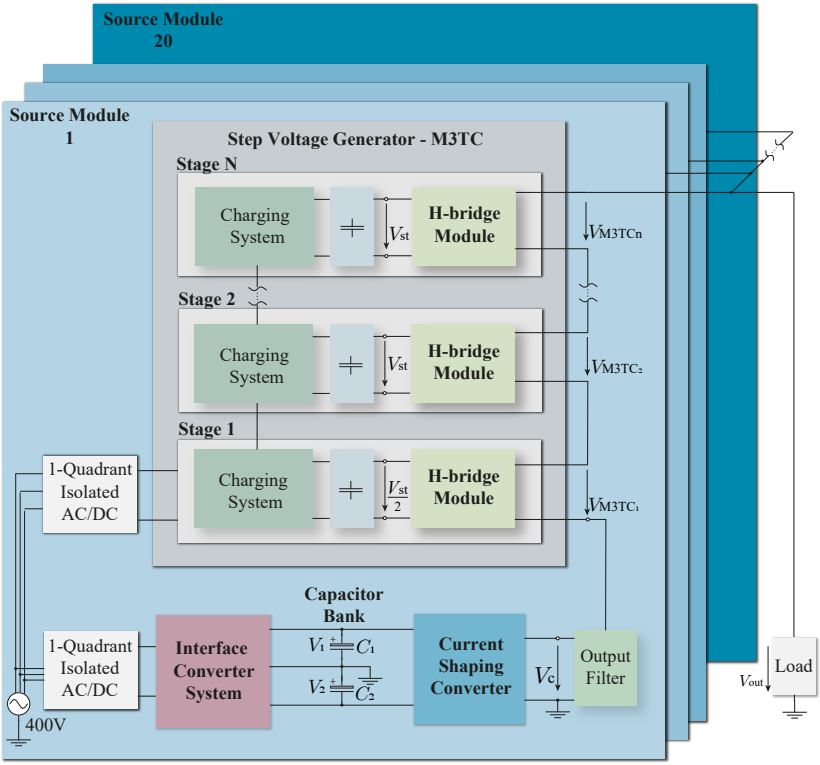

Figure 2.9: Schematic of the full scale source, consisting of 20 parallel DynACuSo modules.

ing of DynACuSo were presented. In order to serve these applications, multiple DynACuSo modules can be connected in parallel, as shown in Figure 2.9, where up to 20 DynACuSo modules are used. In this way, the output current rating can be scaled with steps of 1.5kA. Possible specifications for the full-scale source are listed in Table 1.2.

Apart from the output current rating, connecting multiple source modules in parallel increases the performance in terms of dynamic too, as long as the output voltage is sufficient to drive the current through the load. For resistive loads, the maximum achievable gradient scales linearly with the number of DynACuSo modules connected in parallel, as also noted in Table 1.2. For inductive loads, the achievable cur-

rent gradient depends mainly on the number of M3TC stages that are installed (maximum V_{M3TC}) and the inductance value of the load.

Additionally, the currents of the different DynACuSo modules can be interleaved, using the same phase-shifting control concept that is used for the currents of the individual modules of the current shaping converter[5]. In this way, the output current ripple can be greatly reduced, without the need for increasing the output filter. Interleaving the currents of multiple parallel connected source modules requires a fast communication scheme for data exchange and clock synchronization. In [54] a communication protocol was developed, able to synchronize multiple slave-master modules with a maximum delay of ±4ns, which is sufficient for the synchronization needs of the discussed full scale source. In practice, the source modules can be interleaved simply by sharing the same clock which is generated by the master (e.g. first) DynACuSo module. The control of each module is independent of the rest and only the PWM clock, the sampling clock and the current references need to be exchanged between the slaves and the master.

Interim Summary

This chapter presented the fundamental concepts of DynACuSo, its topology, its main building blocks and its operation principle in different operating scenarios. It was shown that every DynACuSo module is essentially an independent current source that can provide up to 1.5kA of peak output current in pulsed mode and 1kA continuously. DynACuSo uses also a modular topology and its maximum output voltage can be scaled with steps of 1.1kV, thanks to the use of a MMC topology as a step voltage generator.

Furthermore, the exemplary operation principle was shown, in case of supplying resistive, inductive and dynamic loads. Additionally, it was shown that the dynamic performance of DynACuSo can be significantly increased by utilizing the installed voltage of the M3TC stages during the transient. However, in order for the system to be able to take advantage of this control strategy, the current shaping converter needs to be able to operate momentarily outside of its nominal operating region (i.e. [0, 550V]), which needs to be taken into consideration during the converter design. Moreover, the detailed electrical schematic of

[5] the phase-shifting controller is described in Section 4.1.5

the topology was given, and its main voltage levels were determined, having in mind the standard semiconductor voltage ratings. A short discussion, in a qualitative manner, regarding the design parameters of the system revealed some of the major trade-offs that arise between the performance, efficiency and cost of the system. The discussion revealed that a holistic approach is needed for the design of DynACuSo in order for it to comply simultaneously with all the needed specifications.

3

Modelling & Optimization of High Power Interleaved Buck Converters

Motivation

Multi-phase interleaved DC-DC converters constitute an attractive topology for systems with a high current rating, as they enable the processing of a high power by splitting the current in multiple phases. At the same time buck, boost or buck-boost topologies can be utilized retaining the simplicity of the design, modulation and control. Furthermore, the interleaving concept enables low current/voltage ripple and high effective switching frequency leading eventually to reduced volume for passive components for input and output filters that need to abide by EMI regulations. This reduction of the passive components, not only helps in the reduction of the volume and cost of the system, but it also contributes to a higher dynamic performance, which makes the concept especially suitable for demanding applications. Such systems have been widely used in a variety of modern applications, such as electric fast chargers [53], e-mobility [55], accelerator power supplies [56], photovoltaic systems [57] as well as various power management systems for consumer electronics [58–60].

For the current shaping converter of DynACuSo, a multi-phase interleaved buck-type converter topology has been selected. Due to the wide adoption of such topologies, conventional modelling and ripple minimization techniques through interleaving are well understood and investigated in relevant literature. However, the current shaping converter of DynACuSo displays certain particularities that essentially ren-

der some of the common modelling assumptions invalid. For example a capacitor is commonly connected at the output of interleaved converters, to ensure a low output voltage ripple. The output voltage is considered constant in those cases and the load current ripple is neglected. The capacitor helps also in decoupling the phases of the system, and enables every phase to be studied autonomously. In the case of DynACuSo, on the one hand the voltage ripple is not specified and the load current ripple cannot be neglected as it is a crucial specification of the system's performance, and on the other hand, the output capacitance needs to be kept low in order to allow a highly dynamic performance. Furthermore, the load current ripple is proportional to the total converter current ripple, and since it is a crucial specification of the system, the assumption of symmetry between the phases of the system is not sufficient for an accurate determination of the resulting ripple performance, since even minor mismatches between inductance values can have a significant impact on the total converter current ripple. Accurate analytical modelling of the converter system for arbitrary resistive/inductive loads is therefore absolutely necessary, despite its relative complexity.

Additionally, in contrast to conventional systems where the output stage is simply a capacitor and whose value is chosen based on the needed voltage ripple, in the case of DynACuSo the trade-off between dynamic performance, quality factor and ripple attenuation needs to be considered, as the system is intended to be used with various loads. In fact the output stage of the current shaping converter despite its low volume plays a defining role on both the overall dynamic performance of the system, as well as on the load current ripple and the overall waveform quality of the load current (i.e. low overshoot and low disturbances). A closer look at various different options is therefore necessary and a suitable output stage that achieves a good trade-off between dynamic and steady state performance needs to be investigated.

Furthermore, the multi-objective nature of the envisioned system, that aims to fulfill a wide range of applications, imposes the need for a holistic, specification driven, design-space methodology, in order to properly select the system parameters and ensure that the specifications can be theoretically met. An optimization routine is then also needed in order to harness the hardware capabilities of the topology and ensure its feasibility, while maintaining high efficiency and reasonable implementation volume/cost. In the process of converter design

and feasibility, the design of the high power module inductor stands out, and a thorough investigation of different core materials, thermal management concepts and the effect of the continuous current rating, needs to take place. The power inductor investigations of this work provide general conclusions, which can be applied for similar systems. Finally, since the current shaping converter is essentially the backbone of DynACuSo, the developed prototype is discussed and extensive experimental measurements are necessary for its verification.

More specifically in this chapter, the governing equations of the current shaping converter are initially given and the converter system is modeled analytically. Later on in Section 3.3, the chosen output stage is described. After determining the topology, a parameter selection procedure is established and the design trade-offs are revealed. Section 3.4 describes the necessary loss and thermal models that are later used during the design and optimization of the prototype system. Section 3.6 describes the optimization procedure of the module inductor and gives in-depth insights of the effect of different materials and thermal management concepts for power inductors. Concluding the module design, Section 3.7 describes the prototype converter module and shows experimental results that validate its performance. Finally, Section 3.8 shortly presents the developed prototype current shaping converter, and shows results that verify its performance.

3.1 System Overview

The current-shaping converter is the backbone of DynACuSo, as it is responsible for controlling the output current, and delivering arbitrary current waveforms to the load. For the generation of the needed high dynamic and low current ripple and in order to comply with the specifications mentioned in Chapter 1, a suitable converter topology with properly chosen design parameters is needed.

The high nominal current per stack module in the continuous mode of operation (up to 1kA) requires a converter topology with a large semiconductor chip area and therefore multiple semiconductor modules need to be connected in parallel. Additionally, galvanic isolation is included in the external AC/DC supply that is connected to the input capacitor bank as noted in Figure 2.1, so a non-isolated topology can be selected for the current-shaping converter. As a result, similar to UnACuSo [23] a non-isolated multi-phase interleaved converter has been

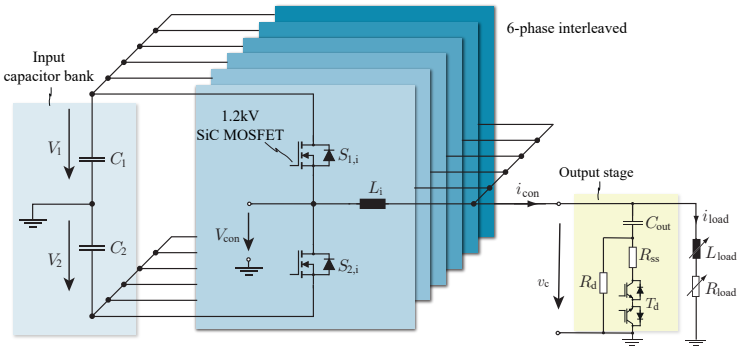

Figure 3.1: Electrical schematic of the current shaping converter, the input capacitor bank and the output stage of DynACuSo.

chosen for DynACuSo, shown in Figure 3.1. In anticipation of the results of this chapter, Figure 3.1 shows the eventually chosen 6-phase interleaved 2-level buck type converter.

3.1.1 Module Topology

In [23], a detailed comparison between 2-level and 3-level topologies has been performed for the UnACuSo. The comparative evaluation clearly points towards using 3-level topologies, due to their significantly lower losses, although a more reliable design could be achieved with a 2-level topology. After all, an improved 3-level topology shown in Figure 3.2 was chosen for UnACuSo. The topology uses 6 interleaved high frequency modules that control the current and 2 low frequency modules that are responsible for conducting the current, depending on the output voltage range. More specifically, when the output voltage is lower than V_{C1}, switch S_3 is turned-on and switch S_4 is turned-off. Instead when the output voltage is higher than V_{C1}, switch S_3 is turned-off and switch S_4 is turned-on.

A major difference to the UnACuSo during the design procedure of the new system, is the commercial availability of 1.2kV SiC MOSFET devices, which compared to the conventional silicon IGBTs used in the UnACuSo, give a significant performance edge on the system level. More specifically, the newest devices are significantly faster and

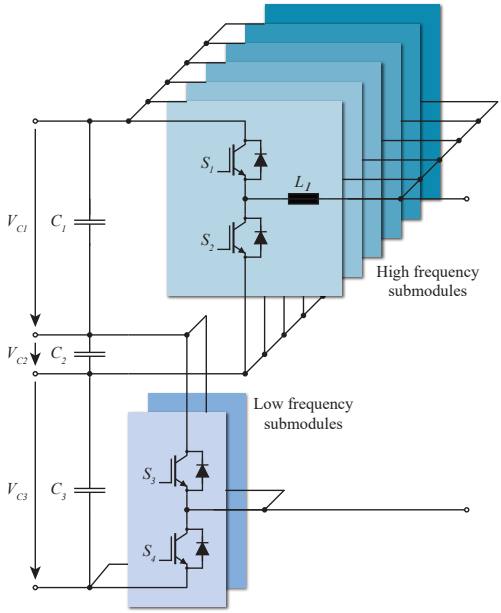

Figure 3.2: Electrical schematic of the multi-phase interleaved converter used in UnACuSo [23].

feature lower switching losses and similar conduction losses, despite the fact that they have a higher blocking voltage rating.

In general it should be remarked that 3-level topologies are associated with lower ripple for the same total input voltage, compared to 2-level topologies, since the devices switch only half of the DC-link voltage. However, when using SiC devices, this benefit can be compensated by the increased switching frequency that can be employed for the SiC devices. Furthermore, the increased switching frequency results in a higher control bandwidth, which is essential in order to improve the overall performance and robustness of the system.

Nevertheless, using the topology of Figure 3.2 with SiC devices replacing the Si IGBTs of the high frequency sub-modules would be an attractive option, since it would result in lower switching losses and a significantly lower ripple for the same switching frequency, and the same input voltage. However, in the case of abrupt voltage fluctuations in the converter output (e.g. DC-arc load), the converter's operating

region would have to be changed by turning on/off the low frequency sub-modules. These sub-modules are slow and the ability of the source to react to such large signal transients would be limited, despite the use of the superior devices. On the other hand, using SiC devices for the low frequency sub-modules too, would result in an unnecessarily high implementation cost.

Based on the above considerations, the 2-level topology with split DC-link shown in Figure 3.1 is pre-selected for this work and no further comparison is included in this work.

3.2 Converter Modelling

This section presents the transient and steady state models of the current shaping converter and gives its governing equations. Those models are used in Section 3.5 to determine the feasible design space for the choice of the parameters of the system, as well as in Sections 3.8.2 and 6.6 for the evaluation of the overall performance of the system.

3.2.1 Steady State

This part derives analytical models to calculate the converter current i_{con} and the load current i_{load}, for any number of interleaved phases regardless of the output stage and the connected load.

In general, conventional interleaved DC-DC converters without special dynamic performance requirements often use a relatively large capacitance value at the output to reduce the voltage ripple, while the load is often approximated by a constant resistor. Therefore, two common approximations are typically made in literature regarding the calculation of the output ripple:

- The load conducts only the DC part of the converter current while the AC part is completely filtered by the output capacitor [61].
- The peak-to-peak converter current ripple is completely contained at the fundamental switching harmonic (worst case approximation) [62–64].

In the case of highly dynamic converters, the output capacitance value needs to be small and for high quality waveforms a damping resistance is also usually inserted. Therefore, a significant part of the high

frequency current could be conducted by the load [65]. Furthermore, in power supplies for magnets, the load is mainly inductive with a very small resistive part, compromising the validity of the first approximation as the load impedance remains low for a wide range of frequencies.

The load current ripple in current source converters is a crucial design specification and an accurate filter design needs to take into consideration the effect of the output stage. Moreover, the fundamental harmonic approximation can result in a significant error leading to an over-dimensioned output capacitance that could potentially compromise the dynamics of the system.

Nevertheless, based on the common approximations simple analytic expressions can be derived for the estimation of the converter current ripple as well as the load current ripple [53]. At first in Figure 3.3 the operational principle of a buck module with an asymmetrically split DC-link is shown and the main waveforms for an ideal operation are given. The duty cycle D in steady state as well as the peak-to-peak individual module current ripple $\Delta i_{\mathrm{L,pp}}$, for the buck module shown in Figure 3.3a can be determined by (3.1)-(3.2). It is observed that due to the split DC link, the converter can generate a bipolar voltage u_{con}, which enables controlling the current when the output voltage is around 0V and increases the dynamic performance for step down transients.

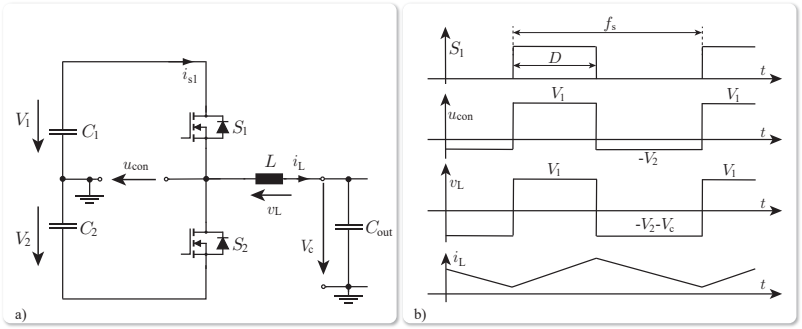

Figure 3.3: Simplified operational principle of a buck converter module with an asymmetrically split DC-link. a) Schematic and parameter definitions. b) Main waveforms at steady state.

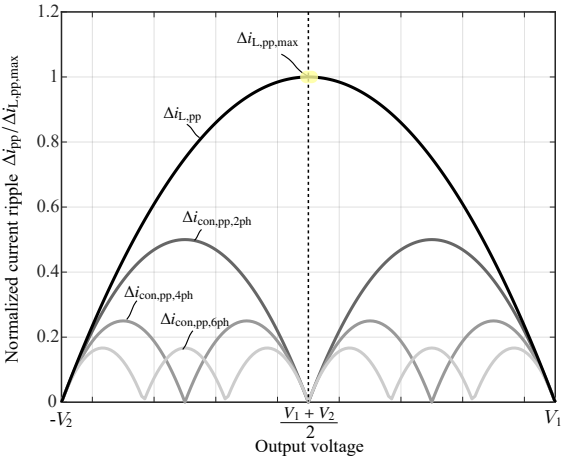

Figure 3.4: Normalized converter module current ripple $\Delta i_{\mathrm{L,pp}}$ and converter current ripple $\Delta i_{\mathrm{con,pp}}$ for different number of phases, as a function of the output voltage V_{c}.

$$D = \frac{V_2 + V_{\mathrm{c}}}{V_1 + V_2} \tag{3.1}$$

$$\Delta i_{\mathrm{L,pp}} = \frac{V_1 + V_2}{L \cdot f_{\mathrm{s}}} \cdot D \cdot (1 - D) \tag{3.2}$$

In the above, V_{c} is the average value of the instantaneous output voltage v_{c}, and f_{s} is the switching frequency. As previously mentioned, the output converter current ripple can be dramatically reduced, by applying a $\frac{2\pi}{n}$ phase shift between the modules. In the simplified case, the converter output current ripple $\Delta i_{\mathrm{con,pp}}$ is not dependent on the output network (output stage and load) and can be calculated by (3.3)-(3.4) [53].

$$D_{\mathrm{i}} = D - \frac{1}{n} \lfloor n \cdot D \rfloor \tag{3.3}$$

$$\Delta i_{\mathrm{con,pp}} = \frac{V_1 + V_2}{L \cdot f_{\mathrm{s}}} \cdot D_{\mathrm{i}} \cdot (1 - n \cdot D_{\mathrm{i}}) \tag{3.4}$$

Figure 3.4 shows a theoretical calculation of the peak to peak module current ripple $\Delta i_{\mathrm{L,pp}}$ and converter current ripple $\Delta i_{\mathrm{con,pp}}$ for different number of symmetrical phases, as a function of the output voltage V_{c}.

The ripple is normalized with the maximum peak-peak module current ripple $\Delta i_{\mathrm{L,pp,max}}$ noted on the figure.

If the n phases are optimally interleaved, then the effective switching frequency of the converter current ripple $\Delta i_{\mathrm{con,pp}}$, is n-times higher than the switching frequency of the individual modules. The simplest way to derive the load current ripple then is based on the second assumption made at the beginning of this Section. The triangular converter current ripple can be modeled as sinusoidal current with an amplitude equal to the peak value of the triangular ripple $\Delta i_{\mathrm{con,pp}}$ at the frequency $\omega_{\mathrm{ripple}} = 2\pi \cdot n \cdot f_{\mathrm{s}}$. The amplitude of the load current ripple can then be calculated as in (3.5), where Z_{f} is the impedance of the filter branch in parallel to the load.

$$\Delta i_{\mathrm{load,pp}}(\omega_{\mathrm{ripple}}) = \Delta i_{\mathrm{con,pp}} \cdot \frac{|\underline{Z}_{\mathrm{f}}(\omega_{\mathrm{ripple}})|}{|\underline{Z}_{\mathrm{f}}(\omega_{\mathrm{ripple}}) + \underline{Z}_{\mathrm{load}}(\omega_{\mathrm{ripple}})|} \tag{3.5}$$

A more accurate way to calculate the ripple is by using Fast Fourier Transformation (FFT), in order to calculate the complete harmonic spectrum of the converter current i_{con}, instead of assuming that the total converter ripple is contained at its fundamental harmonic. This method is referred to in the text from now on as Full Spectrum Approximation (FSA).

Based on the above, i_{con} is a current with a ripple of $\Delta i_{\mathrm{con,pp}}$, a frequency of $f_{\mathrm{eff}} = n \cdot f_{\mathrm{s}}$ and a duty ratio of D_{i}. If a sufficient number of harmonics is used, its waveform can be accurately deduced and the magnitude $|i_{\mathrm{con}}|$ and phase $\angle i_{\mathrm{con}}$ can be derived with an FFT. Each harmonic of i_{con} is then filtered according to the response of the output stage (filter and load), at that particular frequency. In this way, not only the ripple amplitude $\Delta i_{\mathrm{load,pp}}$ but also the complete i_{load} waveform can be derived.

Equations (3.6), (3.7) give the magnitude and phase of i_{load} respectively in every harmonic frequency, with k being an integer number, ranging from $1..N_{\mathrm{h}}$ and $\underline{Z}_{\mathrm{o}} = \frac{\underline{Z}_{\mathrm{f}}}{\underline{Z}_{\mathrm{f}} + \underline{Z}_{\mathrm{load}}}$. The load current is then simply the sum of all harmonic components $1..N_{\mathrm{h}}$, given in (3.8).

$$|\underline{i}_{\mathrm{load}}(k \cdot f_{\mathrm{eff}})| = |\underline{i}_{\mathrm{con}}(k \cdot f_{\mathrm{eff}})| \cdot |\underline{Z}_{\mathrm{o}}(k \cdot f_{\mathrm{eff}})| \tag{3.6}$$

$$\angle \underline{i}_{\mathrm{load}}(k \cdot f_{\mathrm{eff}}) = \angle \underline{i}_{\mathrm{con}}(k \cdot f_{\mathrm{eff}}) + \angle \underline{Z}_{\mathrm{o}}(k \cdot f_{\mathrm{eff}}) \tag{3.7}$$

$$\underline{i}_{\text{load}} = \sum_{k=1}^{N_{\text{h}}} |\underline{i}_{\text{load}}(k \cdot f_{\text{eff}})| \cdot e^{j \cdot \angle \underline{i}_{\text{load}}(k \cdot f_{\text{eff}})} \tag{3.8}$$

FSA is in the vast majority of cases sufficiently accurate, but nonetheless relies on two main assumptions:

- v_{c} is approximately constant and its ripple does not influence $\Delta i_{\text{con,pp}}$.
- The module inductances L_{i} are identical in value.

The first assumption is usually valid, in conventional converter designs, where the output voltage has a relatively low ripple by design. However for highly dynamic converters the voltage ripple might become significant, due to the described need for a smaller effective capacitance in the filter branch. This is especially the case for damped and over-damped systems. In general the smaller effective capacitance (e.g. in Figure 3.5 higher R_{d} and smaller C_{out}) would ensure an over-damped loop with higher cut-off frequency and therefore higher dynamic performance, as will be shown in Section 3.3. Additionally, the second assumption is very difficult to achieve in practice as slight mismatches in the inductance value often occur due to manufacturing tolerances. These mismatches are especially pronounced in higher power bulkier chokes, where setting tight mechanical constraints is particularly challenging and expensive.

It becomes evident, that for an accurate estimation of the load current ripple, regardless of the output stage or the module inductance mismatches, the complete n-phase interleaved system needs to be analytically solved. The unknown states of the system are the module currents $\underline{i}_{\text{L,i}}$ and the output voltage $\underline{v}_{\text{c}}$, that are functions of the frequency (i.e. phasors) and can be represented as complex numbers as in (3.9)-(3.10), where k is used as a notation for the harmonic number (integer multiple of the fundamental switching frequency ω).

The inputs of the system of equations are the converter voltages $\underline{V}_{\text{con,i}}$ which are rectangular waveforms that are phase shifted[1] by an angle $2 \cdot \pi / n$. These inputs are known for any given operating point and can also be expressed as complex numbers, as in (3.11). The output impedance (filter & load) is also considered known, and could be expressed as in (3.12).

[1] the phase-shift controller is explained in Chapter 4 ensures the proper phase shifting between the phases

$$\underline{i}^k_{\mathrm{L,i}} = i^k_{\mathrm{L,r,i}} + j \cdot i^k_{\mathrm{L,j,i}} \qquad (3.9) \qquad \underline{v}^k_{\mathrm{c}} = v^k_{\mathrm{c,r}} + j \cdot v^k_{\mathrm{c,j}} \qquad (3.10)$$

$$\underline{V}^k_{\mathrm{con,i}} = b^k_{\mathrm{r,i}} + j \cdot b^k_{\mathrm{j,i}} \qquad (3.11) \qquad \underline{Z}^k_{\mathrm{o}} = Z^k_{\mathrm{o,r}} + j \cdot Z^k_{\mathrm{o,j}} \qquad (3.12)$$

To facilitate the implementation of the system of equations in a programming environment, the equations are given here already split in real and imaginary part and modeled as a linear $2 \cdot (n+1) \times 2 \cdot (n+1)$ system that can be formulated in matrix form as $\mathbf{A} \cdot \mathbf{X} = \mathbf{B}$. The system is linear and analytic solutions can be derived. In (3.16)-(3.19) the analytic expressions of the module currents $\underline{i}_{\mathrm{L,i}}$ and output voltage $\underline{v}_{\mathrm{c}}$ are shown for the case of equal module inductances $L_{\mathrm{i}} = L$. The generic case for unequal inductances L_{i} can also be derived but the representation of the result in a closed generic formula is rather impractical.

$$\mathbf{A} = \begin{bmatrix} k \cdot \omega \cdot L_1 & 0 & \dots & 0 & 0 & 0 & 1 \\ 0 & -k \cdot \omega \cdot L_1 & \dots & 0 & 0 & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & k \cdot \omega \cdot L_{\mathrm{n}} & 0 & 0 & 1 \\ 0 & 0 & \dots & 0 & -k \cdot \omega \cdot L_{\mathrm{n}} & 1 & 0 \\ -Z^k_{\mathrm{o,r}} & Z^k_{\mathrm{o,j}} & \dots & -Z^k_{\mathrm{o,r}} & Z^k_{\mathrm{o,j}} & 1 & 0 \\ -Z^k_{\mathrm{o,j}} & -Z^k_{\mathrm{o,r}} & \dots & -Z^k_{\mathrm{o,j}} & -Z^k_{\mathrm{o,r}} & 0 & 1 \end{bmatrix} \qquad (3.13)$$

$$\mathbf{X} = \begin{bmatrix} i^k_{\mathrm{L,r,1}} \\ i^k_{\mathrm{L,j,1}} \\ \dots \\ i^k_{\mathrm{L,r,n}} \\ i^k_{\mathrm{L,j,n}} \\ v^k_{\mathrm{c,r}} \\ v^k_{\mathrm{c,j}} \end{bmatrix} \qquad (3.14) \qquad \mathbf{B} = \begin{bmatrix} b^k_{\mathrm{j,1}} \\ b^k_{\mathrm{r,1}} \\ \dots \\ b^k_{\mathrm{j,n}} \\ b^k_{\mathrm{r,n}} \\ 0 \\ 0 \end{bmatrix} \qquad (3.15)$$

$$i^k_{\mathrm{L,r,i}} = \frac{\begin{array}{r} L^2\cdot k^2\cdot\omega^2\cdot b^k_{\mathrm{j,i}} + L\cdot k\cdot\omega\cdot\left(-Z^k_{\mathrm{o,r}}\cdot\sum_1^n b^k_{\mathrm{r,i}} - Z^k_{\mathrm{o,j}}\cdot\sum_1^n b^k_{\mathrm{j,i}}\right) \\ +\, n\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\left(\sum_1^n b^k_{\mathrm{j,i}} - n\cdot b^k_{\mathrm{j,i}}\right) \end{array}}{L\cdot k\cdot\omega\cdot\left(L^2\cdot k^2\cdot\omega^2 - n^2\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\right)} \tag{3.16}$$

$$i^k_{\mathrm{L,j,i}} = \frac{\begin{array}{r} -L^2\cdot k^2\cdot\omega^2\cdot b^k_{\mathrm{r,i}} + L\cdot k\cdot\omega\cdot\left(Z^k_{\mathrm{o,r}}\cdot\sum_1^n b^k_{\mathrm{j,i}} - Z^k_{\mathrm{o,j}}\cdot\sum_1^n b^k_{\mathrm{r,i}}\right) \\ +\, n\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\left(-\sum_1^n b^k_{\mathrm{r,i}} + n\cdot b^k_{\mathrm{r,i}}\right) \end{array}}{L\cdot k\cdot\omega\cdot\left(L^2\cdot k^2\cdot\omega^2 - n^2\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\right)} \tag{3.17}$$

$$v^k_{\mathrm{c,r}} = \frac{\begin{array}{r} L\cdot k\cdot\omega\cdot\left(Z^k_{\mathrm{o,r}}\cdot\sum_1^n b^k_{\mathrm{j,i}} - Z^k_{\mathrm{o,j}}\cdot\sum_1^n b^k_{\mathrm{r,i}}\right) \\ -\, n\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\cdot\sum_1^n b^k_{\mathrm{r,i}} \end{array}}{-L^2\cdot k^2\cdot\omega^2 + n^2\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]} \tag{3.18}$$

$$v^k_{\mathrm{c,j}} = \frac{\begin{array}{r} L\cdot k\cdot\omega\cdot\left(Z^k_{\mathrm{o,r}}\cdot\sum_1^n b^k_{\mathrm{r,i}} + Z^k_{\mathrm{o,j}}\cdot\sum_1^n b^k_{\mathrm{j,i}}\right) \\ -\, n\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\cdot\sum_1^n b^k_{\mathrm{j,i}} \end{array}}{-L^2\cdot k^2\cdot\omega^2 + m^2\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]} \tag{3.19}$$

The analytical expressions of the total converter current $\underline{i}^k_{\mathrm{con}}$ are derived based on equations (3.16) and (3.17), by summing up the real and imaginary parts of the n individual module currents $\underline{i}^k_{\mathrm{L,i}}$.

$$i^k_{\mathrm{con,r}} = \frac{L^2\cdot k^2\cdot\omega^2\cdot\sum_1^n b^k_{\mathrm{j,i}} + n\cdot k\cdot\omega\left(-Z^k_{\mathrm{o,r}}\cdot\sum_1^n b^k_{\mathrm{r,i}} - Z^k_{\mathrm{o,j}}\cdot\sum_1^n b^k_{\mathrm{j,i}}\right)}{k\cdot\omega\cdot\left(L^2\cdot k^2\cdot\omega^2 - n^2\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\right)} \tag{3.20}$$

$$i^k_{\mathrm{con,j}} = \frac{-L^2\cdot k^2\cdot\omega^2\cdot\sum_1^n b^k_{\mathrm{r,i}} + n\cdot k\cdot\omega\left(Z^k_{\mathrm{o,r}}\cdot\sum_1^n b^k_{\mathrm{j,i}} - Z^k_{\mathrm{o,j}}\cdot\sum_1^n b^k_{\mathrm{r,i}}\right)}{k\cdot\omega\cdot\left(L^2\cdot k^2\cdot\omega^2 - n^2\cdot\left[(Z^k_{\mathrm{o,r}})^2 + (Z^k_{\mathrm{o,j}})^2\right]\right)} \tag{3.21}$$

Based on the above model, the solution for the module current $\underline{i}_{\mathrm{L,i}}$, the converter current $\underline{i}_{\mathrm{con}}$ and the load current $\underline{i}_{\mathrm{load}}$ can be derived for an arbitrary output stage. For non-symmetrical inductance values, the system of (3.13)-(3.15) can be solved analytically to derive similar expressions, leading to an accurate calculation of the load current ripple

$\Delta i_{\mathrm{load,pp}}$

3.2.2 Transient State

The models in this section derive the maximum theoretically possible current gradient of the load current, when the system is subjected to step transients of different amplitude. To simplify the analysis a time-optimal controller is assumed and the effect of the controller is not taken into consideration. A detailed investigation of control algorithms to achieve this time-optimal behavior is performed in Chapter 4.

The simplified equivalent of the system during transient operation can be seen in Figure 3.5a. The multi-phase interleaved system is simplified to an ideal voltage source connected in series to the equivalent impedance of the parallel modules. This approach assumes that the system is controlled by a time-optimal controller, that makes the most out of the capabilities of the topology and turns on the high-side switches (i.e. $S_{1,\mathrm{i}}$ in Figure 3.1) when a step up transients occurs, or respectively turns on the low-side switches (i.e. $S_{2,\mathrm{i}}$ in Figure 3.1), when a step down transient occurs.

Note that in Figure 3.5a if the step voltage generator is neglected, the circuit is linear and an analytical solution can be derived. In a first step the circuit of Figure 3.5a can be analytically solved and the time-optimal gradient di_{con}/dt of the converter current i_{con} can be derived.

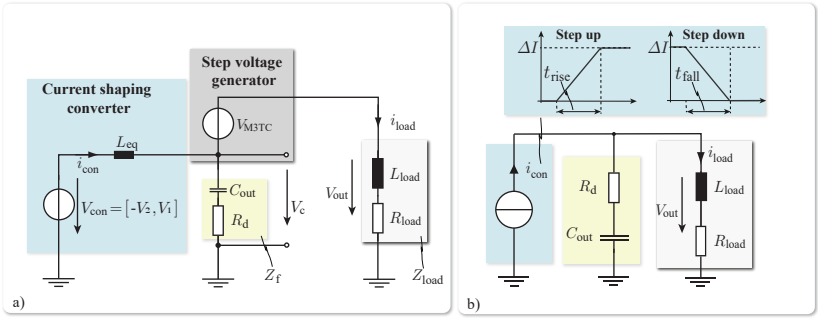

Figure 3.5: a) Simplified equivalent circuit of DynACuSo used for the derivation of the converter current, assuming a time-optimal ideal controller. b) Equivalent transient model of DynACuSo used for the derivation of the load current.

In a second step, in order to evaluate the performance of the system, including the output stage during transients, the current shaping converter is modeled as an ideal current source that can deliver a maximum current gradient $k = di_{\text{con}}/dt$, which was calculated in the previous step, without any overshoot , as shown in Figure 3.5b. The interleaved converter is then substituted by an independent current source implemented as a ramp input, from 0 to I_{ref} in the case of a step up transient and from I_{ref} to 0 in the case of a step down. Consequently, the converter current rise time is given as: $t_{\text{rise}} = \frac{\Delta I}{k}$.

In the Laplace domain, the converter current is expressed as in (3.22) and the load current is derived by (3.23).

$$\underline{i}_{\text{con}}(s) = \frac{k}{s^2} \cdot \left(1 - e^{-s \cdot \frac{\Delta I}{k}}\right) = \frac{\Delta I}{t_{\text{rise}}} \cdot \frac{1}{s^2} \cdot \left(1 - e^{-s \cdot t_{\text{rise}}}\right) \quad (3.22)$$

$$\underline{i}_{\text{load}}(s) = \frac{Z_{\text{f}}(s)}{Z_{\text{f}}(s) + Z_{\text{load}}(s)} \cdot i_{\text{con}}(s) \quad (3.23)$$

On the contrary, if the step voltage generator is included, then the circuit of Figure 3.5a becomes non-linear and the system can only be solved numerically with a time-domain simulation. To facilitate the simulation, the voltage of the step voltage generator can be expressed as in (3.24), (3.25), for a step up and a step down transient respectively. Equations (3.24), (3.25) are derived based on the operation principle of the flexible dynamic source described in Figure 2.5 for increased dynamic performance. In (3.24), (3.25) the symbols $\lfloor$ and $\rfloor$ represents the floor function.

$$V_{\text{M3TC,rise}} = \left(\left\lfloor \frac{V_{\text{out}}}{0.5V_{\text{st}}} \right\rfloor + 1\right) \cdot 0.5V_{\text{st}} \quad (3.24)$$

$$V_{\text{M3TC,fall}} = \left(\left\lfloor \frac{V_{\text{out}}}{0.5V_{\text{st}}} \right\rfloor - 1\right) \cdot 0.5V_{\text{st}} \quad (3.25)$$

3.3 Output Stage

Despite the significant ripple attenuation that the interleaving concept provides according to Figure 3.4, additional attenuation of the high frequency current ripple is usually necessary for systems with strict ripple specifications, such as the ones listed in Table 1.2. The design of the output stage is of crucial importance since it not only influences

the load current ripple at the pulse flattop but also affects the dynamic performance of the load current as well as the quality of the load current waveform. Therefore the topology and the parameters of the output stage need to be carefully considered during the design of the system.

In conventional converters a simple filter branch consisting of a single film capacitor (preferably with low R_{esr}) can be added in parallel to the load to prevent the high frequency ripple components of the current from flowing into the load, as shown in Figure 3.6a. More specifically, a high capacitance value results in lower cut-off frequency and therefore higher ripple attenuation for a given load and frequency. On the other hand this solution compromises the dynamic of the load current, by increasing its rise time compared to the rise time of the converter current. It becomes evident, that the output capacitance is then a trade-off between the load current dynamics and the load current ripple. Consequently it can be said that the value of the output capacitance is not only constrained to a minimum but also to a maximum value.

Furthermore, simply the inclusion of a low output capacitance is often not enough since the formation of the L_{load}-C_{out} with a low resistance R_{load}[2] could lead to resonances, at frequencies that would be triggered during the converter's transient [66]. Note that this is especially pronounced in highly dynamic systems, and particularly for the case of DynACuSo due to the high dynamics of the voltage v_{c} at the output of the interleaved converter every time one of the M3TC stages switches (refer to Figure 2.1). More specifically, the high dv/dt across the filter capacitor C_{out}, would cause a relatively high discharge/charge current to naturally flow into the load, after every transition of an M3TC stage.

Consequently in order to damp the aforementioned resonances and achieve higher quality waveforms during transients (e.g. lower load current overshoot), the output filter branch could consist of an output filter combined with a damping filter (C||RC filter), as highlighted in Figure 3.6b [67], [68]. This choice usually results in a bulkier solution, mainly due to the increased size of the damping capacitor C_{d}, that also compromises the dynamic of the load current. The limitations of the conventional C||RC filter have been highlighted for the current shaping converter of the DynACuSo in [51].

Another option, is shown in Figure 3.6c where a simple RC branch is included in parallel to the load [69]. In general this filter leads to a

[2] this is often the case when driving magnets.

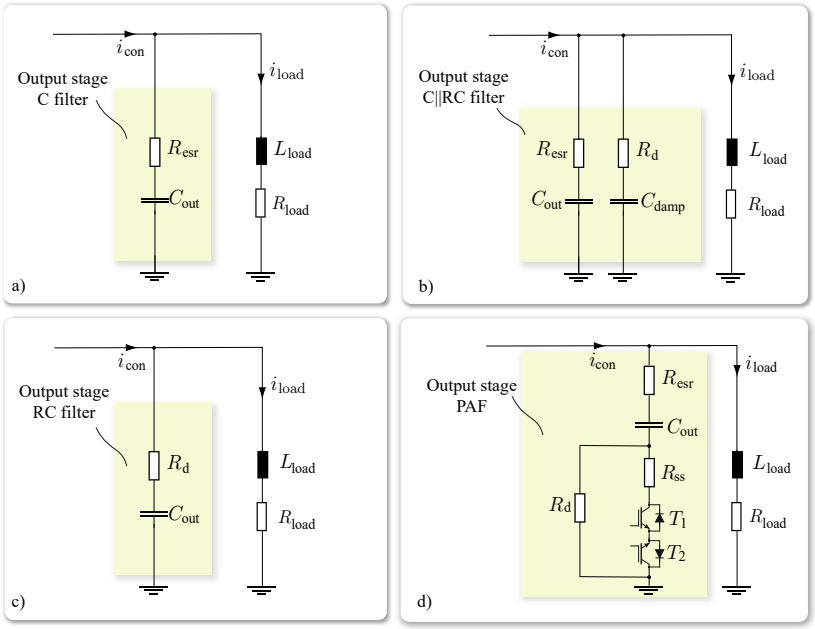

Figure 3.6: Output stage circuit alternatives. a) Capacitive branch. b) C||RC filter. c) RC filter. d) Proposed passive adaptive filter impedance, referred to in the text from now on as PAF.

decreased ripple attenuation compared to the C||RC filter, due to the absence of a fully capacitive branch. On the other hand, the transient properties of the output stage are drastically improved. More specifically, the higher the value of R_d, the lower the ripple attenuation and the higher the transient performance of the load current.

Finally damping by means of control would be possible if the load current was measured. However for the designed source, this would require a rather costly current sensor, that should be able to measure currents up to the kA range and a relatively high bandwidth (i.e. several hundreds of kHz). This option is not considered in this work. Additionally, RL damping filters have been studied in literature too [62], [69]. Due to the increased nominal current rating of the source, these options are also excluded from the present study.

In order to overcome the limitations of the discussed solutions this

section presents an output stage with passive adaptive impedance, which is referred in the text from now on as Passive Adaptive Filter (PAF). The topology of the PAF is shown in Figure 3.6c) and one of the main advantages of the solution is that it is suitable for a wide range of loads. The PAF uses two semiconductor switches[3] to change its impedance during the transient state and effectively provide damping for the duration of the transient. When steady state (e.g. pulse flattop) is reached, the impedance of the output stage changes again to favor ripple attenuation.

3.3.1 Operation Principle

The operation principle of the proposed PAF is explained graphically in Figure 3.7. In steady state (Figure 3.7d), switches $T_1\&T_2$ are turned on and the equivalent resistance of the PAF becomes $R_{\mathrm{eq}} = R_{\mathrm{ss}}||R_{\mathrm{d}}$, which is approximately equal to R_{ss} in case $R_{\mathrm{d}} \gg R_{\mathrm{ss}}$. When a transient is detected by the controller, switches $T_1\&T_2$ are turned off and for the duration of the transient the equivalent resistance of the branch becomes $R_{\mathrm{eq}} = R_{\mathrm{d}}$, as depicted in Figure 3.7c. In this way, the active

[3]IGBTs with anti parallel diodes are shown in Figure 3.6, but MOSFETs would also be applicable.

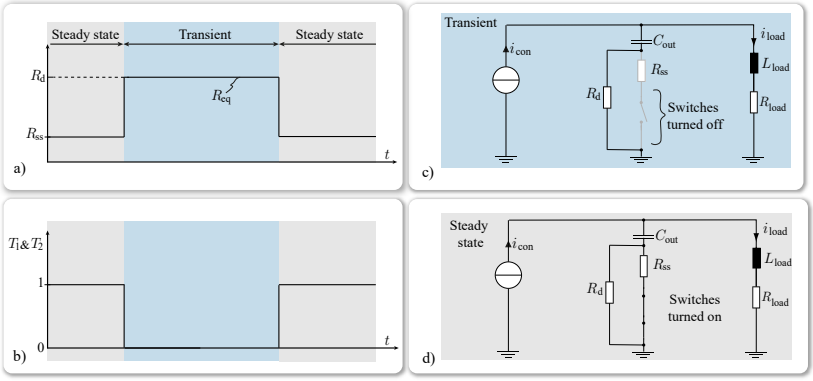

Figure 3.7: Operating principle of the proposed output filter. a) Equivalent branch resistance value R_{eq}. b) Gate control of the bi-directional switch $T_1\&T_2$. c) Equivalent circuit of the proposed output filter during transient. d) Equivalent circuit of the proposed output filter during steady state.

branch becomes a simple RC filter with a large damping resistance value and excellent dynamic properties. After the transient, the switches are turned on again and the system returns to steady state. The detection of the transitions from transient state to steady state and vice-versa are explained in Section 4.1.5 and [49].

3.3.2 Design Considerations

At first, the capacitance value C_{out} and the resistance value R_{ss} are chosen based on the intended steady state performance of the filter for a wide range of inductive loads. At steady state it is assumed that $R_{\text{d}} \gg R_{\text{ss}}$ and therefore $R_{\text{ss}} || R_{\text{d}} \approx R_{\text{ss}}$. To determine the load current ripple i_{load}, equations (3.16)-(3.21) can be used to firstly calculate v_{c} and then i_{load} can be calculated based on the filter/load combination ($\underline{Z}_{\text{o}}$).

An additional design constraint arises from the need to have a sufficiently damped system even at steady state, since imperfect interleaving or control related sub-harmonic oscillations of the converter current i_{con} may drive the output voltage v_{c} and therefore the load current i_{load} to instability, or at the very least compromise the overall accuracy of the system. The simplified system with R_{ss} inserted can be described in the Laplace domain by (3.26). The quality factor is given by (3.27).

$$\underline{Z}_{\text{ss}}(s) = \frac{\underline{i}_{\text{load}}}{\underline{i}_{\text{con}}} = \frac{R_{\text{ss}} \cdot C_{\text{out}} \cdot s + 1}{C_{\text{out}} \cdot L_{\text{load}} \cdot s^2 + (R_{\text{ss}} + R_{\text{load}}) \cdot C_{\text{out}} \cdot s + 1} \tag{3.26}$$

$$Q = \frac{1}{R_{\text{ss}} + R_{\text{load}}} \cdot \sqrt{\frac{L_{\text{load}}}{C_{\text{out}}}} \tag{3.27}$$

A quality factor $Q \leq \frac{\sqrt{2}}{2}$ (optimally damped) at steady state is considered in this work, to avoid amplification of sub-harmonic components of the current. Based on this, the minimum steady state resistance can be derived from (3.28), assuming that $R_{\text{ss}} \gg R_{\text{load}}$. It is quite clear that the largest R_{ss} value arises for the largest considered load inductance L_{load}.

$$R_{\text{ss}} \geq 2 \cdot \sqrt{\frac{L_{\text{load}}}{2 \cdot C_{\text{out}}}} \tag{3.28}$$

During transients, the damping resistor R_{d} dominates the response

of the load current according to (3.29). The high value of R_d, ensures a sufficiently low quality factor and therefore a sufficiently damped response.

$$\underline{Z}_\mathrm{tr}(s) = \frac{i_\mathrm{load}}{i_\mathrm{con}} = \frac{R_\mathrm{d} \cdot C_\mathrm{out} \cdot s + 1}{C_\mathrm{out} \cdot L_\mathrm{load} \cdot s^2 + (R_\mathrm{d} + R_\mathrm{load}) \cdot C_\mathrm{out} \cdot s + 1} \tag{3.29}$$

$$Q = \frac{1}{R_\mathrm{d} + R_\mathrm{load}} \cdot \sqrt{\frac{L_\mathrm{load}}{C_\mathrm{out}}} \tag{3.30}$$

Similar to the steady state case, it is clear that the largest R_d value arises for the largest considered load inductance L_load. However in this case, the higher damping resistance does not compromise any aspect of the performance of the system. A $Q \leq 0.1$ is considered in this work during transient [51].

As an example, Figure 3.8 compares the frequency response of the proposed PAF with the frequency response of a C||RC filter with the same quality factor. It can be observed that the C||RC filter offers a higher ripple attenuation for all frequencies but at the same time results in a low cut-off frequency that eventually leads to a slower transient performance. On the contrary, by adapting the impedance of the output filter, a high cut-off frequency (i.e. dark blue curve) can be combined with a good steady state attenuation (i.e. light blue curve), in order

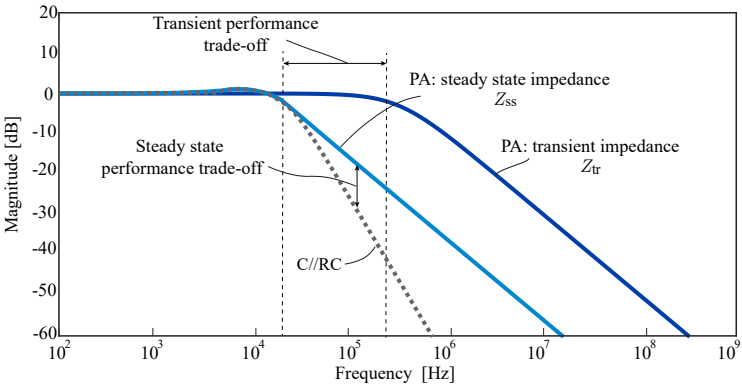

Figure 3.8: Examples of the frequency response of the proposed PAF, and the response of a C||RC filter with the same quality factor Q.

to achieve a better trade-off between transient and steady state performance. Finally, it should be highlighted that the C||RC filter results in a relatively bulky C_{d} capacitor. The size of this capacitor depends on the output load inductance L_{load} but nonetheless it can be concluded that it is significantly larger than the C_{out} needed for the proposed filter [51].

3.4 Component Modelling

In this section the loss and thermal models of the semiconductor devices and the inductor, as well as the thermal model for the cold plate are shortly presented. These models are used in order to design the converter system and assess its thermal feasibility, volume and efficiency. It should be clarified that low volume and high efficiency are not primary goals of the system. However, they are strictly associated with its cost, its mechanical integration and ultimately its practical feasibility.

3.4.1 MOSFET Modelling

At first, the Semikron SKM350MB120SCH17 device is pre-selected based on a preliminary comparative evaluation of its datasheet values with modules with similar ratings and its availability [70]. The selected part number is a 1.2kV 2nd generation SiC power module featuring an additional external SiC Schottky diode in parallel to the MOSFET. The operating limit of the device in terms of junction temperature is 175°C and the limit for the case temperature is 125°C.

For the conduction losses, the device is typically modeled with a temperature dependent on-state resistance $r_{\mathrm{ds,on}}(T_{\mathrm{j}})$. The conduction losses are then given as in (3.31), where the RMS current can be calculated as in (3.32), assuming a switching period T_{p}.

$$P_{\mathrm{c}} = I_{\mathrm{RMS}}^2 \cdot r_{\mathrm{ds,on}}(T_{\mathrm{j}}) \tag{3.31}$$

$$I_{\mathrm{RMS}} = \sqrt{\frac{1}{T_p}\int_0^{T_p} i_{\mathrm{S}}(t)dt} \tag{3.32}$$

Evidently, the distribution of the conduction losses between the upper switch S_1 and the lower switch S_2, depend on the operating point

of the module and its duty cycle. Higher duty cycles result in higher RMS currents for S_1 and vice-versa.

For the calculation of the switching losses, look-up tables can simply be used based on the manufacturer's datasheet. However since in the datasheet the switching conditions often do not match the application switching conditions (e.g. in terms of DC voltage and gate resistance), linear scaling can be assumed when the relevant information is missing, as in (3.33) where V_{dc} is the DC link voltage used in this work ($V_1 + V_2$) and V_{data} is the DC link voltage used to measure the losses in the manufacturers datasheet. The switching losses are then simply the product of the switching energy and the switching frequency.

$$P_{\mathrm{sw}} = \frac{V_{\mathrm{dc}}}{V_{\mathrm{data}}} \cdot f_{\mathrm{s}} \cdot (E_{\mathrm{on}} + E_{\mathrm{off}} + E_{\mathrm{rr}}) \tag{3.33}$$

Since the converter is operating in continuous conduction mode (CCM) and the output current does not reverse direction, the upper switch S_1 is assumed to be dissipating the total switching losses, including the total reverse recovery losses of the additional Schottky diode, as worst case consideration, as in (3.34).

$$P_{L,S_1} = P_{\mathrm{sw}} + P_{c,S_1} \tag{3.34}$$

$$P_{L,S_2} = P_{c,S_2} \tag{3.35}$$

Since the current rating of DynACuSo[4] is different in continuous mode of operation compared to pulsed mode, the temperature of the semiconductor devices needs to be examined in both operation modes. In general, in pulsed power systems apart from the maximum junction temperature that should not exceed the absolute maximum operating temperature of the device $T_{\mathrm{j,max}}$, care must be taken regarding the maximum temperature difference ΔT_{j} due to the temperature cycles [71]. A high temperature difference ΔT_{j} between pulses can cause faster device aging, reduce its reliability and lifetime [72], [73].

Figure 3.9a shows the steady state thermal model that can be used for the extraction of the maximum expected junction temperature in continuous operation mode, which can be calculated from (3.36). The steady state thermal resistances are usually be given in the manufacturer's datasheet, while the thermal resistance of the cold plate $R_{\mathrm{th,CP}}$ is discussed in Section 3.4.3.

[4] in fact this is true for most of the pulsed power systems

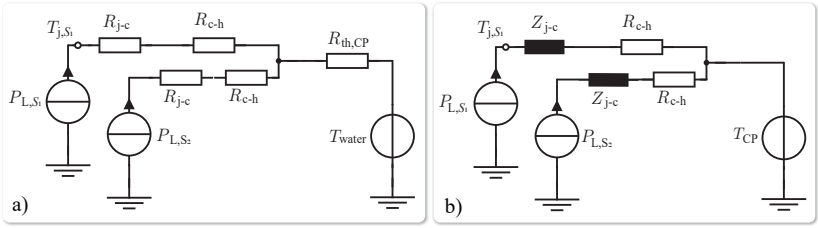

Figure 3.9: Thermal model of the semiconductor devices. a) Steady state model in continuous mode of operation. b) Transient thermal model in pulsed mode of operation.

$$T_{j,S_1} = T_{\text{water}} + (P_{L,S_1} + P_{L,S_2}) \cdot R_{\text{th,CP}} + P_{L,S_1} \cdot (R_{\text{j-c}} + R_{\text{c-h}}) \quad (3.36)$$

Figure 6.12b shows the transient thermal model that can be used for the extraction of the maximum junction temperature swing ΔT_{j}, during the pulsed mode of operation. In this case, the module's case temperature can be considered constant, due to the large thermal capacitance of the cold plate. In the model, the transient thermal resistance of the MOSFETs, which is a function of time, is taken into account. The thermal paste is assumed to have a negligible thermal capacitance, and therefore its steady state value is assumed ($R_{\text{c-h}}$) [74]. The temperature swing can then be calculated as in (3.37).

$$\Delta T_{\text{j}} = T_{\text{j}} - T_{\text{CP}} = P_{L,S_1} \cdot (Z_{\text{j-c}}(t) + R_{\text{c-h}}) \quad (3.37)$$

3.4.2 Inductor Modelling

The inductors of the current shaping converter represent a high percentage of the overall volume, losses and cost of the system and therefore care needs to be taken during the design procedure. Due to the different operation modes of the system (i.e. pulsed and continuous operation), the design of the module inductors L_{i} is particularly challenging. At the maximum pulsed current, saturation of the magnetic material needs to be avoided, and at the maximum continuous current safe operation within the operating thermal limits needs to be ensured . At the same time,a relatively compact and cost efficient design needs to be achieved.

In this work the inductor design follows a Pareto-optimization rou-

tine (core volume vs. efficiency), with emphasis on minimizing the volume of the inductor core material, which is one of the defining factors of its cost. The backbone of the optimization routine are the loss and thermal models, and the thermal management system of the inductor that are presented in this section.

This section is structured as follows: At first pre-selected parameters of the inductor, that set the basis for its optimization and limit its scope are described. Later on, the reluctance model is given followed by the fundamental loss models. Finally, the thermal models for non-potted and cores potted in epoxy resin inside an aluminum box are given.

a. Pre-selected Parameters

As will be shown during the optimization procedure (Section 3.6), the volume of the core can be massively reduced, and its thermal performance can be greatly improved if it is placed inside an aluminum box filled with potting material with a relatively high thermal conductivity (e.g. epoxy resin). However, in order to avoid induced currents to the sides of the aluminum box, the winding should be enclosed by the core and as a result only E-shaped cores are considered for this work, with the winding placed in the center leg.

As a winding, litz wire is pre-selected due to its excellent high frequency performance and its simple mechanical integration. During the inductor optimization procedure different standard litz wire configurations, and a different number of parallel wires, are explored and the most suitable is chosen. It should be remarked that plain copper wire would also be in this case a good alternative, as the high frequency winding losses of the inductor are relatively small, due to the relatively low current ripple. In this case, copper wire has a higher filling factor and a higher overall thermal conductivity compared to litz wire. However, only litz wire is considered in the scope of this work due to its easier mechanical integration.

b. Reluctance Model

Figure 3.10a shows the core geometry of an E-shaped core that is used throughout this work, and the definitions of the needed geometrical parameters. Figure 3.10b shows the respective equivalent magnetic circuit that is used for the calculation of the total magnetic reluctance. The reluctance model provides a straightforward way of calculating the inductance. It can also be used to calculate the expected maximum flux

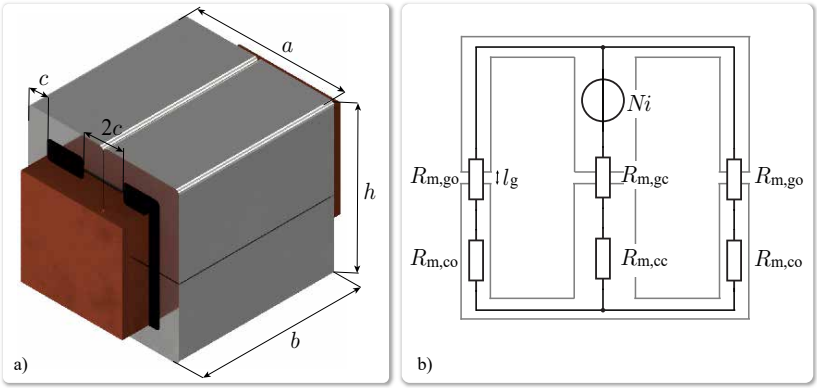

Figure 3.10: a) Core geometry and geometrical definitions. b) Equivalent reluctance model.

in the different sections of the core, in order to avoid saturation.

In this work, since the inductance value is given by the design space method described in the previous section, the total magnetic reluctance that is needed to achieve the target value is given by (3.38). The maximum flux can be calculated as in (3.39).

$$R_{\mathrm{m,t}} = \frac{N^2}{L} \tag{3.38}$$

$$B_{\max} = \frac{i_{\max} \cdot L}{N \cdot 2 \cdot b \cdot c} \tag{3.39}$$

To calculate the total reluctance $R_{\mathrm{m,t}}$, one has to calculate the reluctance of the different sections of the core. For an E-core without the air-gap, the total reluctance is given as in (3.40).

$$R_{\mathrm{m,t}} = \frac{R_{\mathrm{m,co}}}{2} + R_{\mathrm{m,cc}} = \frac{2 \cdot h + a - c}{2 \cdot \mu_0 \cdot \mu_r \cdot b \cdot c} \tag{3.40}$$

To achieve a target inductance value, an air-gap often needs to be included to increase the magnet reluctance. A benefit of inserting an air-gap is that the inductance value becomes less susceptible to variations of the relevant magnetic permeability (μ_r) of the magnetic material.

In other words, the air-gap can be chosen such that it dominates the reluctance model and therefore reduces the effect of the magnetic material properties that are often difficult to predict, and require extensive testing. In its most simplified form, the needed air-gap length can be calculated based on (3.41).

$$l_{\mathrm{g}} = \frac{\mu_0 \cdot \mu_r \cdot b \cdot c \cdot R_{\mathrm{m,t}} - 2 \cdot h - a + c}{2 \cdot \mu_r} \tag{3.41}$$

However, the effect of the fringing field around the air-gap can have a significant impact on the total reluctance of the air-gap and needs to be taken into consideration, especially for cores with a relatively long air-gap compared to their cross section. More specifically, the fringing flux increases the cross-section area of the air-gap and therefore reduces its magnetic reluctance. Neglecting the fringing flux can lead to significantly underestimating the needed air-gap length (l_{g} to achieve a certain inductance value. For the accurate calculation of the air-gap reluctance, various methods can be found in the literature [75–78]. In this work the more accurate 3D calculation proposed in [75] is followed.

c. Loss Models

For the loss calculation of the inductor existing models that can be found in the literature are used and they are briefly summarized here for completeness. Firstly, the loss mechanisms are distinguished between winding losses and core losses.

For the calculation of the core losses, the commonly used Steinmetz equation is not sufficient, as it is limited to sinusoidal excitation. In this work, the core losses are derived based on the improved generalized Steinmetz equation (iGSE), which is appropriate for piece-wise linear excitation [79].

$$P_{\mathrm{core}} = Vol \cdot C_{\mathrm{stein}} \cdot f_{\mathrm{s}} \cdot \Delta B^{\beta_{\mathrm{stein}} - \alpha_{\mathrm{stein}}} \cdot \int_0^{1/f_{\mathrm{s}}} \left| \frac{dB}{dt} \right|^{\alpha_{\mathrm{stein}}} dt \tag{3.42}$$

In (3.42), Vol is the volume of the core material, α_{stein} and β_{stein} are the Steinmetz parameters. C_{i} is given by (3.43), where C_{stein} is the third Steinmetz parameter.

$$C_{\mathrm{i}} = \frac{C_{\mathrm{stein}}}{(2\pi)^{\alpha_{\mathrm{stein}}-1} \int_0^{2\pi} 2^{\beta_{\mathrm{stein}}-\alpha_{\mathrm{stein}}} \left|\cos\theta\right|^{\alpha_{\mathrm{stein}}} d\theta} \tag{3.43}$$

One benefit of the iGSE is that it requires only the Steinmetz parameters, which can simply be extracted by the manufacturer's datasheets for the given material. However, the iGSE does not include the DC-bias losses, which might add a significant amount of losses, especially for the systems with a high DC current rating, such as the current shaping converter of DynACuSo. For the inclusion of the DC-bias losses, additional parameters and therefore extensive measurements and special measurement equipment would be needed, as discussed in [80–82]. According to [80], the influence of DC pre-magnetization on silicon steel cores, Nanocrystaline cores as well as in Ferrite cores is not negligible. Due to the lack of relevant experimental measurements and in anticipation of the measurement results of Section 3.7, where the influence of the DC bias current on the core losses is apparently negligible, the DC-bias losses are neglected in the following models and the subsequent comparisons.

Regarding winding losses, a distinction between DC winding losses and AC winding losses can be made. Due to the use of a litz wire and the relatively low current ripple, the AC winding losses are very low compared to the DC winding losses, despite the relatively high switching frequency. Nevertheless, they are included in the upcoming calculations but they could also be considered negligible without affecting the final result. For this reason, they are not further discussed in this work. The reader is pointed to [83] for a detailed derivation of the AC winding losses (i.e. skin and proximity losses).

The DC resistance of the litz wire is given by (3.44), where l is the total length of the wire, n_{s} is the number of strands and d_{s} is the copper diameter of a single strand [84]. It is remarked that the copper conductivity σ is a function of the temperature and therefore a recursive method together with the inductor thermal model described in the next subsection needs to be implemented, for the accurate winding loss extraction.

$$R_{\mathrm{DC}} = \frac{4 \cdot l}{\sigma \cdot n_{\mathrm{s}} \cdot \pi \cdot d_{\mathrm{s}}^2} \tag{3.44}$$

d. Thermal Model

As previously mentioned, apart from the magnetic saturation constrain, the core and winding maximum temperature are also thermally constrained. The worst case operating scenario for thermal feasibility arises during the continuous mode of operation. To assess the thermal performance of the inductor, a 2D thermal model is presented hereby. The thermal model is based on the following assumptions:

- Heat transfer through radiation is neglected.
- The winding is considered concentrated in the middle of the core window.
- In the case of the potted core, it is considered that the surrounding aluminum facilitates the efficient heat transfer through conduction to the cold plate. Convection to the surrounding ambient is neglected.
- In the case of the non-potted core, convection to the surrounding ambient is also neglected, as the conduction mechanism through the core to the cold plate is considered to be much more efficient.

In order to increase the accuracy of the analytical thermal model, several lumped sections of the core are considered, as shown in Figure 3.11. It should be remarked that the more core sections used, the more distributed the generation of the core losses, and therefore the more accurate the temperature calculation.

Figure 3.11a shows the different thermal resistances that need to be calculated. The winding thermal resistance $R_{\mathrm{th,w}}$ is calculated based on [85] and exploiting the symmetries that are inferred from the second assumption. Based on [85] the thermal resistance of the litz wire in the tangential as well as in the radial direction is taken into consideration and a closed form solution is found, showing good agreement with experimental results. The thermal resistance $R_{\mathrm{th,HS}}$ represents the path from the surface of the cold plate to the water channel and is explained in Section 3.4.3.

All the other thermal resistances are calculated based on the conductive heat transfer equation of (3.45), where λ is the thermal conductivity of the respective material, $l_{\mathrm{th,c}}$ is the length of the thermal path and $A_{\mathrm{th,c}}$ is the cross section area [86]. The relevant geometrical parameters that are needed to calculate the thermal resistances from the winding to the core (through the potting compound) can be derived based on the

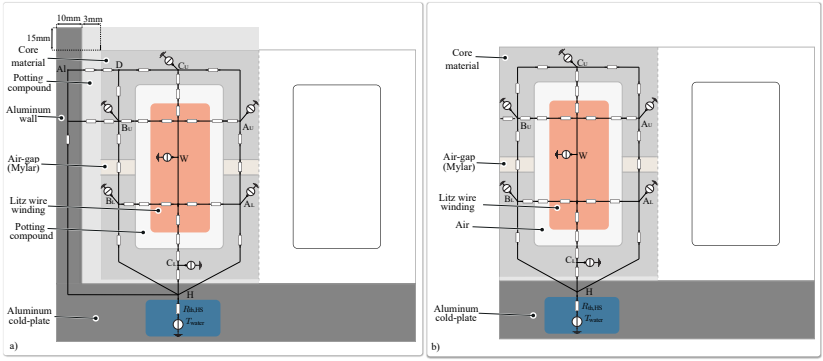

Figure 3.11: a) Thermal model of the potted inductor core, with 10 nodes. b) Thermal model of the non-potted inductor core with 7 nodes.

filling factor of winding in the core window and depend on the winding configuration that is varied during the optimization procedure. Furthermore, the aluminum wall is considered to be 10mm in width and the distance between the core and the aluminum wall is 3mm, as shown in Figure 3.11.

$$R_{\mathrm{th,c}} = \frac{l_{\mathrm{th,c}}}{\lambda \cdot A_{\mathrm{th,c}}} \tag{3.45}$$

As noted in Figure 3.11a the core is split into 6 main nodes (A_{L}, A_{U}, B_{L}, B_{U}, C_{L}, C_{U}). In each of those nodes, a power loss source is connected to represent the core losses generated in the respective section of the core. The model clearly distinguishes between the core losses generated in the upper part of the core (above the air-gap) from those generated below the air-gap. This is particularly important considering the high thermal conductivity of the material (e.g. approx. 40W/mK for silicon steel and 9W/mK for Nanocrystaline) compared to the low thermal conductivity of the material that is used as a place holder for the air-gap (e.g. approx. 0.14W/mK for Mylar). Despite its short length, the air-gap can have a significant impact on the total thermal resistance and that is why it needs to be included. Additionally for this reason, node D is created on the core as the losses generated on the top part of the core, could also be dissipated with the help of the aluminum wall through the potting material. In this case the thermal resistance of the path D-H is comparable to the thermal resistance of the path

through the air-gap.

Clearly, the model of Figure 3.11a is linear and can simply be solved using nodal analysis. The method is well-known from electrical circuit analysis textbooks and is not included in this work.

The effect of the potting material on the overall volume of the core material as well as on the boxed volume is explored in the upcoming Section 3.6. For the non-potted core, a similar thermal model can be derived, as shown in Figure 3.11b. The core is split into 6 parts too, and the losses are distributed accordingly. The heat transfer through convection to the surrounding air is neglected, as the conduction to the cold plate is considered much more efficient. In contrast to the thermal model of Figure 3.11a, the thermal interface between the winding and the core material is air, which severely affects the cooling of the inductor winding, as will be revealed in Section 3.6.

3.4.3 Cold Plate Modelling

In contrast to UnACuSo, where only pulsed mode of operation was required, the high continuous current rating of DynACuSo imposes an additional challenge when it comes to the thermal management of the system. Since the losses in the current-shaping converter as well as in the step voltage generator are high, water cooling has been pre-selected, for all converter systems in the scope of this work. It should be noted that natural convection and forced air cooling were not considered, as they would require a significantly increased system volume, to achieve sufficient heat removal [87], [88]. It should also be clarified that an optimization of the cold plate to achieve a higher power density does not take place in the scope of this work. A detailed optimization procedure for heatsinks can be found in [89]. In this work the aim of the modelling of the cold plate is rather to calculate its thermal resistance for given geometrical dimensions, that are defined by the semiconductors and magnetic components of the system.

Following the methodology described in [90], two types of heat transfer mechanisms are considered for modelling the cold plate: conduction and convection. Due to small differences between surface temperature and ambient temperature, heat transfer through radiation is neglected. The basic principles of heat transfer can be found in [86] and the governing equations are repeated in this work for completeness.

Firstly, the hereby described model assumes that heat removal via

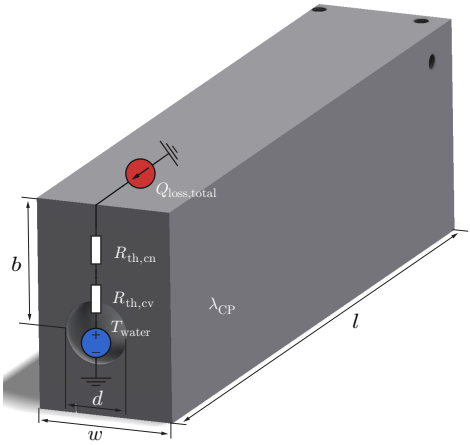

Figure 3.12: Water channel and its geometrical definitions [90].

the water channels of the cold plate occurs very efficiently and therefore instead of modelling the cold plate as a whole, and extracting one thermal resistance, each individual water channel is modeled separately, resulting in several different thermal resistances for the same cold plate. For example in this work, a different thermal resistance of the cold plate is assumed for cooling the semiconductor module and a different one for cooling the inductor, despite the fact that both are accommodated on the same cold plate.

Figure 3.12 shows an exemplary water channel and its relevant geometrical dimensions. There are two thermal resistances that need to be calculated to extract the total thermal resistance. $R_{\text{th,cn}}$ models the conduction mechanism from the channel wall to the surface of the cold plate, and can be calculated as in (3.46).

$$R_{\text{th,cn}} = \frac{b}{\lambda_{\text{CP}} \cdot w \cdot l} \tag{3.46}$$

$R_{\text{th,cv}}$ models the convection mechanism from the channel wall to the cooling medium, in this case the de-ionized water. $R_{\text{th,cv}}$ is calculated based on (3.47), where h is the heat transfer coefficient that is given by (3.48).

$$R_{\mathrm{th,cv}} = \frac{1}{h \cdot \pi \cdot l \cdot d} \tag{3.47}$$

$$h = \frac{Nu \cdot \lambda_{\mathrm{water}}}{d} \tag{3.48}$$

For the calculation of the heat transfer coefficient, the Nusselt (Nu) number needs to be calculated first. A generalized model for the calculation of the Nusselt number ($Nu_{\sqrt{A}}$) suitable for arbitrary channels with a cross-sectional area A has been deduced in [86] and the equations are given hereby for completeness.

$$Nu_{\sqrt{A}} = \left[\left(\left\{ C_2 C_3 \left(\frac{fRe_{\sqrt{A}}}{l^*} \right)^{\frac{1}{3}} \right\}^5 + \left\{ C_1 \left(\frac{fRe_{\sqrt{A}}}{8\sqrt{\pi}\epsilon^{\gamma}} \right) \right\}^5 \right)^{\frac{m}{5}} + C_4 \left(\frac{f(Pr)}{\sqrt{l^*}} \right)^m \right]^{\frac{1}{m}} \tag{3.49}$$

where:

$$l^* = \frac{l \cdot v}{\dot{V} \cdot Pr} \tag{3.50}$$

$$m = 2.27 + 1.65 \cdot Pr^{\frac{1}{3}} \tag{3.51}$$

$$f(Pr) = \frac{0.564}{\left(1 + \left(1.164 \cdot Pr^{\frac{1}{6}} \right)^{\frac{9}{2}} \right)^{\frac{2}{9}}} \tag{3.52}$$

$$fRe_{\sqrt{A}} = \left(\frac{11.8336 \cdot \dot{V}}{l \cdot v} + (fRe_{fd})^2 \right)^{\frac{1}{2}} \tag{3.53}$$

$$fRe_{fd} = \frac{12}{\sqrt{\epsilon}(1+\epsilon)\left[1 - \frac{192}{\pi^5}\tanh\left(\frac{\pi}{2 \cdot \epsilon}\right)\right]} \tag{3.54}$$

In the above equations, v is the kinematic viscosity of the fluid, Pr is the Prandtl number of the fluid, $\dot{V}$ is the volumetric flow of the fluid

at the input of the channel and ϵ is the ratio between the horizontal and the vertical dimensions of the arbitrary channel (in the case of a round channel $\epsilon = 1$). Parameters C_1, C_2, C_3, C_4 and γ are derived in [86] too as: C_1 =3.01, C_2 =1.5, C_3 =0.409, C_4 =2 and γ =0.1.

In the scope of this work, the flow of the fluid through the channel is considered to be a known input. Furthermore, it is assumed that the temperature of the cooling medium (i.e. water) does not change over the length of the channel and is also a known input. It should be remarked that this is an approximation that holds for short channel lengths with a relatively high volumetric flow. The accuracy is compromised for longer channels with lower volumetric flows. For that reason, during the design verification, the thermal resistance of the cold plate is also extracted with FEM simulations. The total thermal resistance of the cold plate could then be calculated based on the average surface temperature, or the maximum temperature (hot-spot). The methodology described hereby is followed throughout this work, for the calculation of the cold plate's thermal resistance.

As an example, a simple cold plate with a rectangular water channel that cools a semiconductor module (similar to the one chosen in this work) is studied with FEM simulations and compared with the presented analytical model. The result of the 3D-FEM simulation with a input water flow of $\dot{V}$ =10L/s, water temperature of 20°C and total

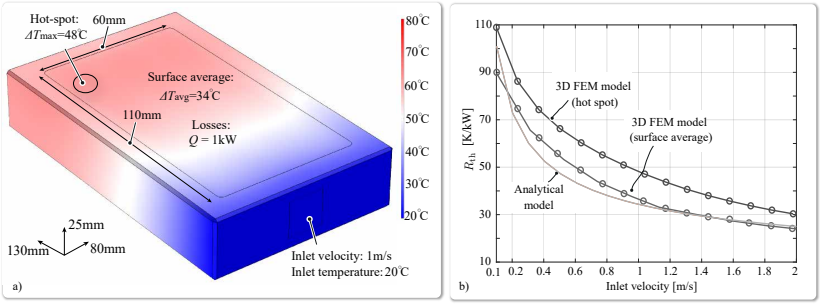

Figure 3.13: a) 3D FEM simulation of a cold plate with a water inlet velocity of 1m/s and inlet water temperature of 20°C. The cold plate accommodates a semiconductor module with 1kW losses uniformally spread across its surface. b) Cold-plate thermal resistance R_{th} as a function of the input water velocity, calculated analytically based on the cold-plate model presented in this section, and numerically with FEM simulations.

semiconductor losses of 1kW, is shown in Figure 3.13a. The losses of the semiconductor are assumed to be equally distributed throughout the module's surface.

To extract the average thermal resistance from the FEM simulation, the average temperature rise ΔT_{avg} of the surface of the semiconductor module is evaluated. The surface average thermal resistance can then be calculated as in (3.55). The maximum thermal resistance, which is the worst case scenario, since it assumes the temperature of the hot-spot, can be calculated based on the maximum temperature that arises on the surface of the semiconductor, as in (3.56).

$$R_{\text{th,avg}} = \frac{\Delta T_{\text{avg}}}{Q_{\text{loss,total}}} \quad (3.55) \qquad R_{\text{th,max}} = \frac{\Delta T_{\text{max}}}{Q_{\text{loss,total}}} \quad (3.56)$$

Figure 3.13b compares the result of the presented analytical model, with the result of the 3D FEM simulations, which act as a reference. As expected, the analytical model gives a fairly similar result with the surface average calculation from the FEM simulations. The accuracy is higher for higher volumetric flows, since for higher flows the water temperature does not change neither in the analytical model nor in the FEM simulations. On the other hand, the analytical model cannot predict the hot-spots and therefore underestimates the thermal resistance compared to the FEM hot-spot model.

In this work during the initial design and optimization of the inductor, the presented analytical model is used for a faster conversion to an acceptable result. Nevertheless, a worst-case scenario based on the FEM hot-spot model is also considered as a final validation step, to verify that the selected design does not result in unacceptably high hot-spot temperatures.

3.5 Parameter Selection

In Chapter 2 the unavoidable performance trade-offs of DynACuSo have been shorty discussed, and Table 2.2 has summarized qualitatively the effect that an increase in the values of the main parameters of the system would have in the overall system performance. In order to fulfill the specifications in terms of the achievable current gradient and load current ripple (see Table 1.2) a detailed parameter selection procedure is followed in this section. The converter and the output stage models

that were established in the previous sections act as the groundwork.

Apart from the dynamic and ripple requirements, DynACuSo needs to be able to drive highly fluctuating loads with robustness, as discussed in detail in Chapter 1. When considering such loads (e.g. HVDC-CB), repetitive large-signal load changes are expected and ensuring the robustness of the system under extreme conditions (see Figure 1.2b) is challenging. For example, in the case of an output voltage collapse, the slow switching IGBTs of the step-voltage generator (see Figure 2.6) would not be able to react fast enough and a high voltage would be applied across the equivalent inductance L_{eq} (Figure 2.2), causing the current to rise uncontrollably, as the current shaping converter would be operating outside of its operating region. This condition might potentially trigger the protection mechanisms (e.g. over-current protection) and cause the system to trip, as also documented in [23]. Increasing the bandwidth of the system in this case (e.g. by means of increasing the switching frequency f_{s}) is helpful, but unavoidable time delays due to measurement and communication as well as finite rise/fall times of the switches impose certain boundaries to the minimum reaction times of the system. In order to increase the natural robustness, the individual module inductance L_{i} must be sufficiently large, setting an upper boundary on the allowable current rise/fall.

Based on the above, a minimum inductance value can be established as in (3.57), where V_{flt} is the maximum considered fault voltage that is applied across the equivalent inductance L_{eq} for a time duration of Δt_{flt}, which represents the worst case reaction time of DynACuSo, and ΔI_{flt} is the maximum fault current that can be tolerated, before causing the system to trip. It should be noted that based on the robustness criterion of (3.57), the minimum inductance that can be used per phase, scales linearly with the number of phases. In other words the equivalent inductance L_{eq} defined in Chapter 2 as $L_{\mathrm{eq}} = \frac{L_{\mathrm{i}}}{n}$ remains constant.

$$L_{\mathrm{i}} \geq n \cdot \frac{V_{\mathrm{flt}} \cdot \Delta t_{\mathrm{flt}}}{\Delta I_{\mathrm{flt}}} \tag{3.57}$$

The robustness criterion along with the ripple and dynamic criteria[5] need to be simultaneously satisfied. When multiple design criteria need to be simultaneously met, the concept of design space is the most promising one [91]. Based on this method, that was also used for the design of a dynamic 3-phase voltage source inverter in [62], the design

[5] discussed in Chapter 2.

Table 3.1: Pre-defined parameters used in the selection procedure, shown in Figure 3.14.

Description	Symbol	Value
Number of installed M3TC stages	$N_{\min}$	1
Min. reference current	$I_{\text{ref,min}}$	300A
Min. case load resistance	R_{load}	50mΩ
Min. case load inductance	L_{load}	5µH
Max. fault voltage	V_{flt}	1500V
Max. fault duration	t_{flt}	10µs
Max. fault current	ΔI_{flt}	375A
Max. load ripple @ $I_{\text{ref,min}}$	$\Delta I_{\text{load,pp}}$	500ppm
Min. current gradient $0..I_{\text{ref,min}}$	di_{load}/dt	10A/µs

criteria define the bounds for the values of L and C on the LC-plane. In the following, the design space for the discussed system is extracted, and a selection of suitable parameters takes place.

The pre-defined parameters for the selection procedure are shown in Table 3.1, along with the target specifications. For the selection of the parameters, a DynACuSo system with just one integrated M3TC stage is assumed[6]. Furthermore, the worst case load in terms of ripple performance is assumed (minimum inductance and minimum resistance) and the minimum set-point for the reference of the current $I_{\text{ref,min}}$ is defined. $I_{\text{ref,min}}$ affects both the dynamic (see eq. (3.23)) as well as the relative load current ripple (in ppm). Additionally, the maximum fault voltage, duration and acceptable fault current are defined in order to calculate the minimum module inductance based on the robustness criterion of (3.57).

Figure 3.14a shows the selection procedure that is followed in order to extract design solutions that fulfill the specifications, for different number of interleaved phases. It should be clarified that due to the high current rating of the system, L_{i} dominates the volume (and cost) and therefore the reduction of its value needs to be prioritized over the reduction of C_{out}.

After initially defining the needed parameters shown in Table 3.1,

[6]systems with higher number of installed stages can achieve higher current gradients with the same ripple performance, as discussed in 6.6.

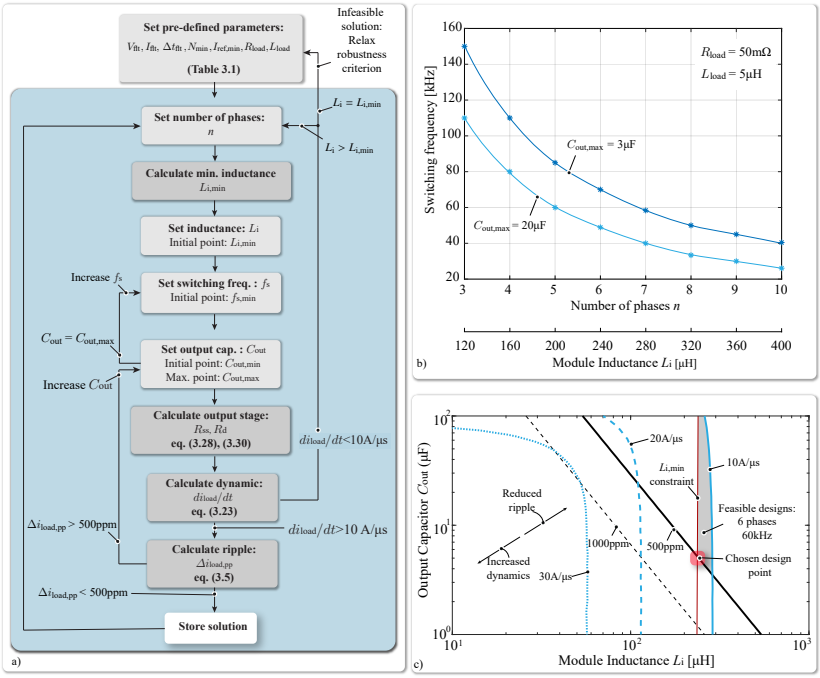

Figure 3.14: a) Flow-chart of the parameter selection procedure followed for a DynACuSo system with one installed M3TC stage. b) Solutions that fulfill the specifications for different number of interleaved phases. c) Current gradient (light blue) and current ripple (black) contour lines as a function of L_i and C_{out}, for n =6 and f_s =60kHz. The chosen design point is noted along with the feasible design space (gray area).

the number of interleaved phases is set and the minimum inductance can be calculated based on (3.57). Then, the switching frequency is selected starting from the minimum $f_{s,min}$, that results in an acceptable bandwidth (e.g. 20kHz in this work). Finally, the output capacitance is set, and the resistors of the output stage (see Figure 3.7) are calculated. As discussed in section 3.3, R_d is used for the calculation of the current gradient and R_{ss} for the calculation of the current ripple.

After selecting the output stage, the load current can be derived based on (3.23). At this stage, if the dynamic is lower than the target specification and $L_i = L_{i,min}$, there is no feasible solution in the design

space, and either the robustness criterion needs to be relaxed, or a higher number of installed M3TC stages is needed. On the other hand, if $L_\mathrm{i} > L_\mathrm{i,min}$, all the feasible solutions for the given n have been found and the algorithm increases n. If the dynamic specification is fulfilled, the load ripple is calculated. If it also fulfills the specifications, the solution is stored. Otherwise, the output capacitance is increased until an acceptable ripple is achieved. If the maximum allowed capacitance is reached, the algorithm increases the switching frequency and repeats the previous steps.

Figure 3.14b shows pairs of n and f_s that fulfill the specifications. Each n translates based on the robustness criterion into a given $L_\mathrm{i,min}$, as long as it can fulfill the dynamic requirement. Moreover it can be noted that as the number of interleaved phases increases, the resulting switching frequency is reduced, since the ripple current is reduced due to the interleaving concept. Finally, as the maximum capacitance constraint is relaxed (e.g. for larger capacitors C_out), a reduced switching frequency can be used for the same number of interleaved phases. Since thermal feasibility constraints are not inserted into this parameter selection procedure, the switching frequency does not have an upper boundary. In practice however, it is limited by the thermal constraints of the semiconductors.

To gain a better understanding of the trade-offs and the design decisions, Figure 3.14c shows the LC design space. The shaded part is the design space that fulfills the three design criteria for $n = 6$ and $f_\mathrm{s} = 60\mathrm{kHz}$. It can be seen that higher current gradients can be achieved, if a lower value is chosen for L_i, but the robustness criterion (red line) imposes a constrain to the maximum achievable gradient. Furthermore, it can be noticed that due to the high damping introduced by the proposed PAF, the effect of the output capacitance on the current gradient is minor, as it only starts to play a role at higher current gradients (notice the shape of the $30\mathrm{A/\mu s}$ contour line) and higher C_out values. It should be remarked that similar design spaces can be extracted for different combinations of n and f_s.

Based on the above, it can be concluded that increasing n can lead to a significant decrease of the switching frequency to achieve the current ripple requirement, as shown in Figure 3.14b. However, increasing the number of interleaved phases might lead to an increased system complexity, increased implementation effort and decrease its reliability. Moreover, a higher switching frequency leads to increased controllabil-

Table 3.2: Selected parameters for the current-shaping converter prototype system.

Description	Symbol	Value
Number of phases	n	6
Pulsed mode phase current	I_{pulsed}	250A
Cont. mode phase current	I_{DC}	166A
Switching frequency	f_{s}	60kHz
Module inductance	L_{i}	240µH
Output capacitance	C_{out}	4µF

ity, which is an important factor for the robustness, but also increases the complexity of the system (e.g. increased complexity of gate driver circuits) and increases the switching losses. In the end as shown in Figure 3.14c, there are multiple solutions that fulfill the specifications and the chosen design point is shown in red.

From now on in this work the system considers 6 interleaved phases, chosen mainly due to the availability and current carrying capabilities of commercial SiC devices at the time of the design. Furthermore a moderately high switching frequency of 60kHz is chosen, providing a good trade-off between complexity, (e.g. auxiliary power needed, communication link bandwidth), switching losses, current ripple and overall system bandwidth. Once n and f_{s} are chosen first the minimum L_{i} and then the minimum C_{out} that fulfill the specifications, as graphically depicted in Figure 3.14c are selected.

3.6 Inductor Optimization

Power inductors play a crucial role on the efficiency and volume of high power switching supplies. This section describes a generic optimization procedure for power inductors used in a pulsed power system with continuous current rating requirements. The module inductors L_{i} of the intended current shaping converter of the DynACuSo are used as a case scenario in the upcoming sections, and useful insights regarding the performance of different magnetic materials in pulsed power systems with high current ratings can be drawn. A comparison of thermal management concepts (potted and non-potted cores) also takes

place. The comparison reveals the advantages of using a potting material with high thermal conductivity in reducing the necessary core material. Along with those more general conclusions, the results of the optimization give a clear indication of feasible designs for the prototype module power inductors L_{i}.

Figure 3.15 shows a sketch of the inductor window and defines the geometrical parameters that are used throughout this section. A sketch of the litz wire configuration is also shown along with the definitions of the winding parameters. It should be noted that in this work only standard litz wire configurations are considered (commercially available configurations) and due to the high DC current per inductor, the optimization considers also the use of multiple parallel conductors per turn (noted as N_{par} in Figure 3.15).

A flow-chart of the optimization procedure that is followed, aiming to extract the Pareto-front, with respect to the efficiency and core volume for different core materials, is shown in Figure 3.16. This work follows a brute-force optimization procedure, in order to give a better insight on the effect of different parameters on the losses and volume of the power inductor. Furthermore, the optimization procedure uses custom sized cores. Later on, the prototype system is finally designed based on commercially available core sizes. The step-by-step optimization routine is described in the following.

- Initially, the worst-case operating conditions are defined. In the pulsed mode of operation the core should not saturate for its max-

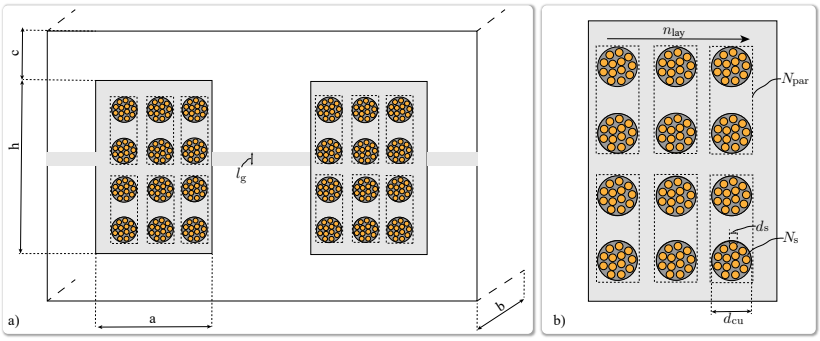

Figure 3.15: a) Inductor window and geometrical definitions. b) Litz wire configuration and parameter definitions.

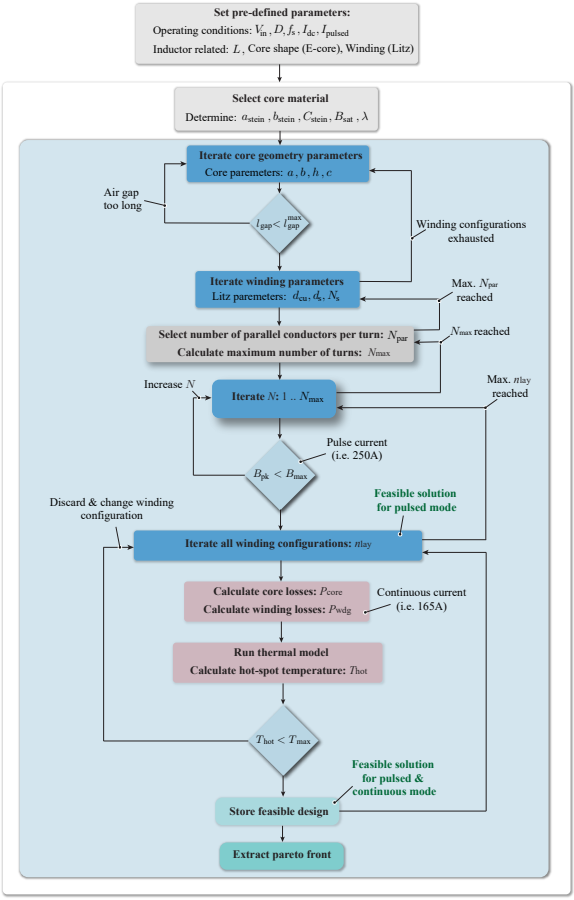

Figure 3.16: Optimization routine for the inductor core and its winding. A Pareto-front with respect to the total losses and the core volume is extracted at the end of the algorithm for the different studied core materials.

imum pulse current I_{pulsed}. Core and winding temperatures are not considered for this current rating. On the other hand, the thermal feasibility of the core is examined for the maximum continuous current of I_{DC}. In both cases the worst-case duty ratio $D = 0.5$ is considered, since it results in the highest module current ripple, and therefore the highest flux density/losses. Further-

Table 3.3: Material parameters used during the optimization procedure.

Material	B_{sat}[T]	μ_{r}	λ [W/mK]
SiFe 3% (0.1mm)	1.9	5000	40
N87 (Ferrite)	0.39	3500	3.8
Metglass 2605SA1	1.56	45000	9
Vitoperm 500f	1.2	16000	9

more, the winding type and the core shape are pre-selected. Also, the target inductance value L is usually determined based on system level specifications. For the example of the DynACuSo the inductance value is determined based on the design space driven parameter selection procedure described in Section 3.5. Based on these considerations the current waveform in pulsed and continuous mode of operation can be analytically calculated and its harmonic content can be derived.

- In the next step the core material is selected. The core material has a significant impact on the performance of the inductor, its losses, volume and cost. In this work, four different core materials are studied and their main parameters are listed in Table 3.3. The Steinmetz parameters α_{stein}, β_{stein} and C_{stein} are extracted based on the manufacturer's datasheets for the Ferrite (N87), the Amorphous (Metglass 2605SA1) and the Nanocrystaline (Vitoperm 500f) material. Specifically for the SiFe 3% material, as at the time of the analysis there was no data available for high frequency operation (above 10kHz) for the 0.1mm lamination thickness material, the loss data was extracted based on core loss measurements with sinusoidal excitation.

- Afterwards, the core geometry is chosen based on a pre-defined grid of geometrical parameters a, b, h and c (defined in Figure 3.15). As the core geometry and the core material are already selected, the reluctance model shown in Figure 3.10 can be deduced. The needed air-gap length l_{gap} for a given inductance is then calculated. The algorithm compares l_{gap} with the maximum air-gap constraint $l_{\text{gap}}^{\text{max}}$. If it is higher, then a new core geometry is chosen and the process is repeated. If it is within the limits the algorithm continues.

- The litz winding is selected based on a database of commercially available configurations. Then, the number of parallel conductors per turn N_{par} is chosen. In this work up to 5 parallel conductors are considered, and the maximum number of turns N_{max} that fit inside the window can be calculated, based on the window size and a defined filling factor ($k = 0.5$ in this work), as given by (3.58).

$$N_{\text{max}} = \lfloor \frac{k \cdot a \cdot h}{N_{\text{par}} \cdot d_{\text{cu}}^2} \rfloor \tag{3.58}$$

- The algorithm then iterates through the number of turns and checks the peak flux density B_{pk} in the core based on the target inductance, the worst case operating pulsed current and the core geometry as in (3.59). If B_{pk} is higher than the material's acceptable maximum flux density $B_{\text{max}} = 0.85 \cdot B_{\text{sat}}$, the solution is discarded and N is increased. If it is lower, then the solution is considered as feasible for the pulsed mode of operation and the algorithm continues to check its thermal feasibility.

$$B_{\text{pk}} = \frac{L \cdot (I_{\text{pulse}} + \frac{\Delta I_{\text{pp}}}{2})}{N \cdot b \cdot c} \tag{3.59}$$

- A final degree of freedom, is the number of layers n_{lay} used to realize the winding (see Figure 3.15). The number of layers affects the winding losses, and the thermal performance of the core (i.e. cooling of the winding). The algorithm iterates through all possible winding configurations with the assumption that parallel conductors of the same turn are placed on the same layer.

- Finally, the inductor is fully defined and the core and winding losses can be calculated based on the models described in Section 3.4.2, referring to the continuous operation mode. The core and winding temperatures are assessed based on the thermal model described in Figure 3.11 and the cold plate model described in Section 3.4.3. The hot-spot of the inductor is then calculated. If it is lower than the considered T_{max}[7], then the solution is stored as it is considered a feasible design for both the pulsed, as well as the continuous mode of operation.

[7] 100°C for this work assuming a 20°C inlet water temperature.

- When all the possible configurations are exhausted and all the feasible solutions are determined, the algorithm draws the Pareto-front (core volume vs. efficiency) for a given material. Based on the Pareto-front an optimum solution can be selected for the given material. Afterwards, a new material is chosen and the algorithm is repeated.

Table 3.4 lists the geometrical/realization constraints considered in the optimization routine. All the following results use the same constraints.

3.6.1 Optimization Results: Potted Cores

Taking the needed specifications of the module inductors L_i as a test case, Figure 3.17 depicts the volume of the core versus the efficiency for all the investigated designs with potted cores[8] and the different materials along with their respective Pareto-front.

It should be clarified that the core volume plotted in Figure 3.17 includes only the volume of the core material, excluding the cold plate, the potting material and the surrounding aluminum box, which constitute a large part of the total volume. In fact as a result of the cooling concept, the core material used (i.e. core volume) can be drastically reduced and therefore the cost of the design in general is reduced. This

[8] the thermal model for potted cores has been shown in Figure 3.11a

Table 3.4: Geometrical/Realization constraints used in the optimization.

Description	Symbol	Considered range
Window length	a	10..50mm
Core length	b	60..340mm
Core leg size	c	5..30mm
Window height	h	20..100mm
Air-gap length	$l_\mathrm{gap}^\mathrm{max}$	5mm
# of parallel conductors	N_par	1..5
# of turns	N_max	1..40
# of layers	n_lay	1..4
Filling factor	k	0.5

is in fact the primary driving factor for the design choice in this work. Furthermore, the efficiency of the inductor is shown for the operating point where the thermal evaluation takes place, namely: $V_{\text{in}} = 800\text{V}$, $I_{\text{out}} = 166\text{A}$ and $D = 0.5$. The total losses depend on the operating point and therefore the inductor efficiency at higher duty cycles is higher (i.e. higher output power and lower losses).

Figure 3.18 depicts the Pareto fronts of the different materials in a single graph for comparison. It can be seen that SiFe 3% can achieve lower core volumes due to its higher saturation flux as well as its higher thermal conductivity. On the downside, it is the least efficient studied material, and especially at high frequencies it is associated with elevated

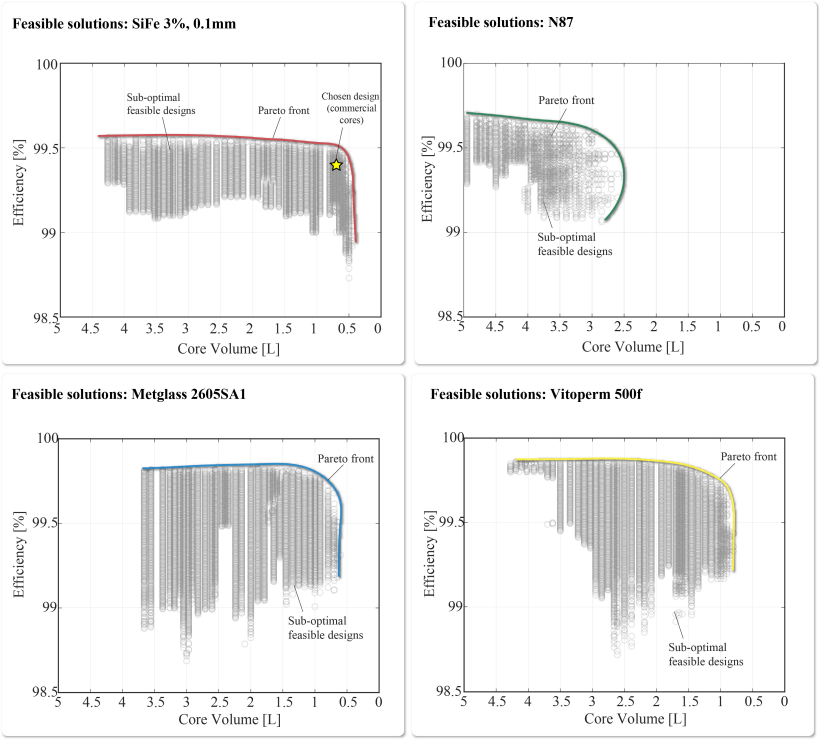

Figure 3.17: Inductor optimization results for the investigated core materials. All the examined feasible solutions are shown along with the respective Pareto-fronts.

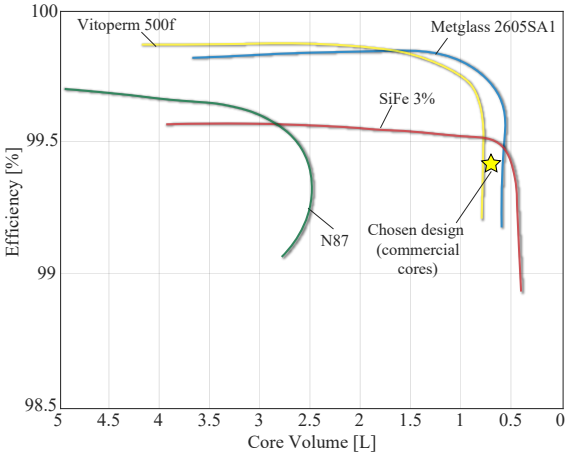

Figure 3.18: Comparative evaluation of the investigated core materials for cores potted in an aluminum box. Epoxy resin with high thermal conductivity is assumed ($\lambda = 1.2\text{W/mK}$). The star point indicates the chosen design, based on commercially available cores.

core losses. Nevertheless it should be kept in mind that using thinner laminations (e.g. 0.05mm) would improve the efficiency of the core, at the expense of a higher cost.

The Amorphous material (Metglass 2605SA1) and the Nanocrystaline material (Vitoperm 500f) result in significantly more efficient designs compared to SiFe 3%, but cannot achieve its low core volume performance, mainly due to their lower saturation flux density. Lower volumes for those two materials are essentially discarded during the initial step where the algorithm checks the feasibility of the core in the pulsed mode of operation. Nevertheless, the resulting inductor losses are approximately cut in half for both of those materials compared to SiFe 3% for the same core volume.

Despite its wide adoption in power electronic converter systems, the Ferrite N87 material is the least suitable material for the considered application. Due to its low saturation flux density, it requires very high core volumes to achieve the pulsed operation mode specifications (higher core cross section, higher number of turns).

3.6.2 Optimization Results: Non-potted Cores

To further investigate the effect of the potting material on the inductor design, this section follows the same optimization procedure presented in Section 3.6, but this time for non-potted cores. It should be highlighted that the only difference lies on the thermal model used to assess the thermal feasibility of the design (see Figure 3.11).

Figure 3.19 shows the optimization results and all the investigated designs for the case of the non-potted cores for the studied materials. The Pareto-fronts of the potted cores are shown in dotted lines too for an easier comparison. As expected the core volume needed in all cases is significantly higher than in the potted case, which would result in an increase in the cost for the realization of the core. It is also worth noting that in the case of potted cores, the saturation limit is reached for the designs on the Pareto-front, signifying an increased utilization of the core material. In the case of the non-potted cores however, the designs are thermally limited and their saturation flux density is lower.

For the case of the SiFe 3% material it can be seen that the minimum achievable core volume is approximately 2.2L, which is an increase of approximately 4.5 times compared to the core volume for the potted core (approx. 0.5L). The efficiency of the design is reduced too. This can be attributed to the fact that in the case of the non-potted designs, the losses of the winding cannot be efficiently dissipated, and therefore a ratio with more core losses and less winding losses is reached. It should also be highlighted that in the case of the non-potted designs, the winding losses that can be dissipated within the thermal limits are drastically reduced. As a result feasible designs include a lower number of turns, which in fact increases the core losses (and reduces the winding losses) due to a higher saturation flux density ripple for the same current ripple. This results in disproportionally increased core losses and less efficient designs.

Regarding the Amorphous and Nanocrystaline material, an increase in core material volume of approximately 3 times compared to the core material volume for the potted core is noted. However, the efficiency is still high in both cases. As indicated on the exemplary designs noted in Figure 3.19, the tendency of the optimization for both of these materials is to use a small core with more turns and more winding losses when the core is potted, as the winding losses can be efficiently dissipated. More turns for a fixed inductance then reduce the maximum flux density and enable the use of smaller cores. The low volume designs of the potted

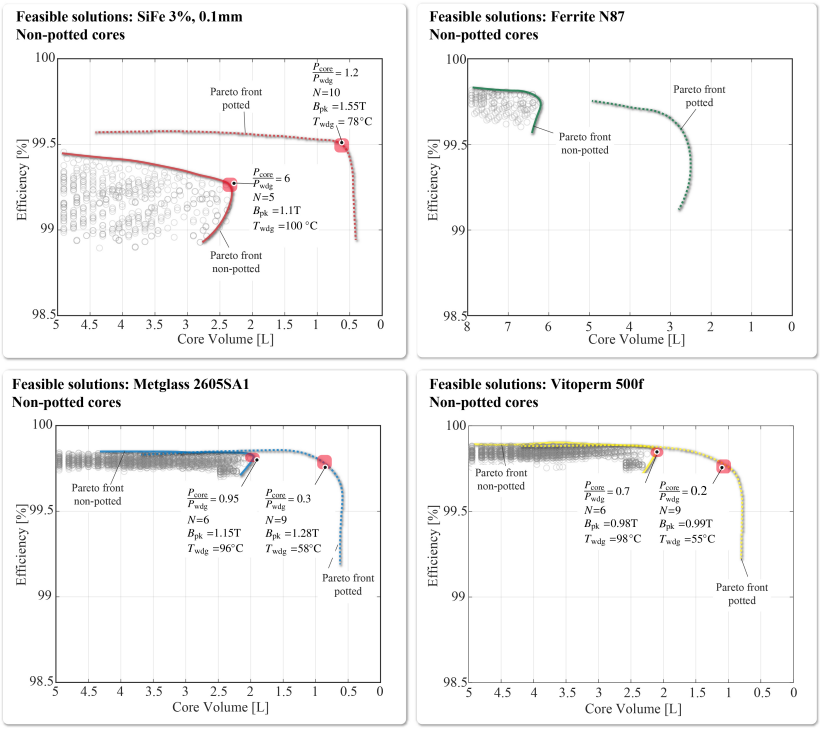

Figure 3.19: Inductor optimization results for the investigated core materials for non-potted cores. All the examined feasible solutions are shown along with their respective Pareto-fronts. The Pareto-fronts of the potted cores are shown in dotted lines. *Note:* For the case of N87 material the x-axis is different compared to the other materials.

cores are not thermally limited but rather magnetically limited, as also indicated in Figure 3.19. On the other hand, the non-potted designs for both materials have a $\frac{P_{\text{core}}}{P_{\text{wdg}}}$ ratio closer to 1, and are both thermally and magnetically limited.

Figure 3.20a compares in a single graph the Pareto-fronts for the non-potted and potted designs. All in all a significant reduction in the core material used (3-5 times) can be achieved for all the cases, when the core is potted. Furthermore, in the non-potted designs the Amorphous and Nanocrystaline material are both significantly more

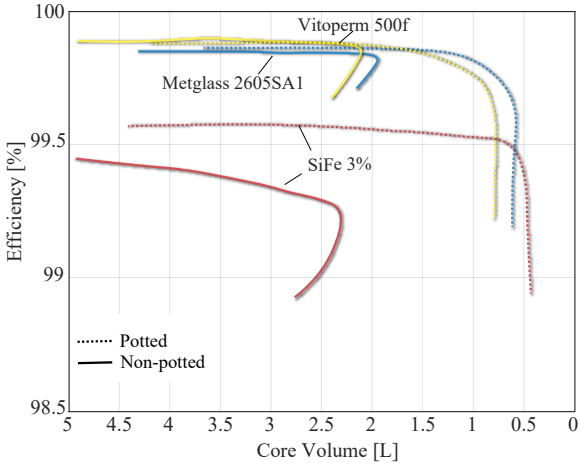

Figure 3.20: a) Comparative evaluation of the Pareto-fronts for the investigated core materials. b) Comparative evaluation of the Pareto-fronts with respect to the boxed volume, for different materials

efficient as well as smaller in volume compared to the SiFe 3%. This is expected since the non-potted designs are thermally limited, and as a result the slight advantage that SiFe 3% has due to its higher saturation flux density is vanished. As a general rule it can be observed that the non-potted optimal designs include cores with less number of turns in order to reduce the DC winding resistance (see equation 3.44) and longer designs (geometrical coefficient b) in order to increase the cooling surface and achieve thermal feasibility.

3.6.3 Optimization Results: I_{DC} Scaling

So far the ratio $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ has been assumed to be 66.67%, with the current in pulsed mode being 250A and the continuous current being 166A per module. In this section the effect of the ratio $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ in the optimal design of the inductor is investigated. In the following the current in pulsed mode is kept at 250A and the ratio $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ is varied between 10% and 100%, by changing the continuous current rating of the inductor current I_{DC}. The investigation takes place for potted and non-potted cores, and is shown here for the chosen SiFe 3% material with 0.1mm laminations as well as for the amorphous Metglass

2605SA1 material that was proven as a promising alternative.

For a fair comparison, instead of plotting the Pareto-front of every solution, a cost function is devised hereby in order to always consistently pick the optimum point from the Pareto-front. The cost function assigns in this case the same weight to the core material volume and the losses. After iterating through all feasible solutions for the pulsed mode of operation, the volume and the losses for every current ratio are found and the feasible solutions for both modes are extracted. The volume and the loses are then normalized based on the minimum volume and minimum losses of every current ratio point respectively. The aim is then to minimize function f shown in (3.60), for every current ratio point.

$$f(I_{\mathrm{DC}}) = 0.5 \cdot \frac{P_{\mathrm{losses,total}}(I_{\mathrm{DC}})}{P^{\mathrm{min}}_{\mathrm{losses,total}}(I_{\mathrm{DC}})} + 0.5 \cdot \frac{Vol_{\mathrm{i}}(I_{\mathrm{DC}})}{Vol^{\mathrm{min}}_{\mathrm{i}}(I_{\mathrm{DC}})} \tag{3.60}$$

Figure 3.21 shows the optimal design core material volumes for SiFe 3%, as a function of the current ratio $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$, for potted and non-potted designs (note that y-axis is in logarithmic scale). The figure also shows the range of feasible core volumes in each point. The upper boundary (7L) is simply given by the design space definition at the start of the optimization problem. The lower boundary is constrained either magnetically or thermally.

It can be concluded that for SiFe 3%, potting the core starts bringing benefits from the 20% current ratio and on, as for lower continuous current ratings, the optimal designs are magnetically constrained. As the current ratio is increased, potting becomes more and more beneficial and notably it is associated with almost 9 times smaller core material at a $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ of 80%. For the 100% $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ ratio, the non-potted case does not have a feasible design in the design space. It should be clarified that Figure 3.21 depicts the volume of the core material and not the total volume. The total volume would be significantly higher for the potted cores compared to the reported one, since the aluminum box around the core occupies a relatively large amount of space.

An identical analysis is conducted for the amorphous material, shown in Figure 3.22. It can be seen that despite of the use of a more efficient core, potting is clearly beneficial as it results in approximately 40% core material volume savings, starting already from an $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ of 20%.

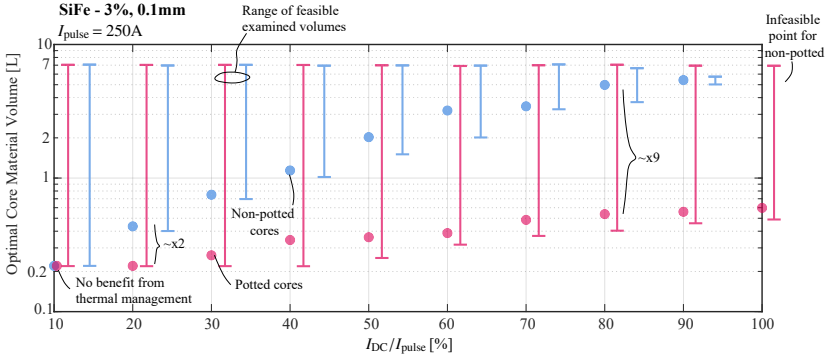

Figure 3.21: Optimal core material design points for SiFe 3% with 0.1mm lamination thickness, as a function of the current ratio $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$, for potted (red) and non-potted (blue) designs. The range of feasible examined volumes is also shown.

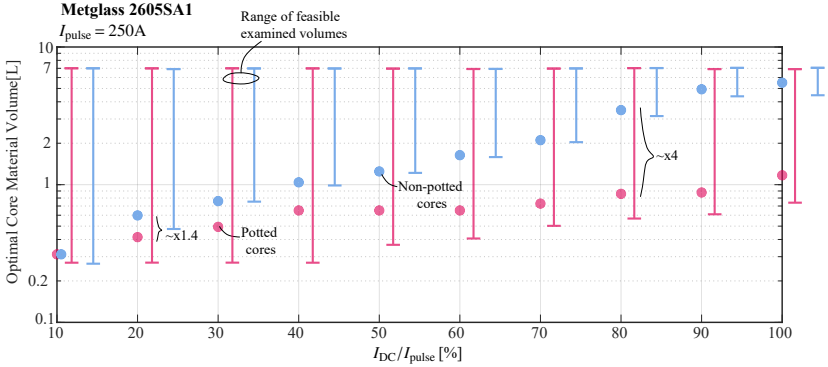

Figure 3.22: Optimal design points for Metglass 26S051A, as a function of the current ratio $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$, for potted (red) and non-potted (blue) designs. The range of feasible examined volumes is also shown.

Similar to the SiFe 3% case, the higher the $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ the higher the benefits of potting the core as expected. Notably approximately 4 times smaller core can be used at an $I_{\mathrm{DC}}/I_{\mathrm{pulsed}}$ of 80%. Nevertheless, the potting benefits in this case are less pronounced compared to the SiFe case, as the material is a lot more efficient and better trade offs between core and winding losses can be found.

3.6.4 Prototype Inductor and Verification

In this section the developed prototype inductor is shown and experimental measurements verify its design. Based on the above considerations, SiFe 3% with 0.1mm lamination thickness is selected as the core material for the inductors of the current shaping converter, as it offers a significantly better trade-off between performance and realization cost compared to Metglass and Vitoperm 500f. Furthermore, high efficiency is of high importance for the designed system, but not its primary goal. In Figure 3.18, the chosen design point is also shown. The designed prototype lies close to the Pareto-front of the SiFe 3% material and its parameters are driven by the availability of the components (e.g. commercially available core size, availability of litz wire winding). The parameters of the designed core are summarized in Table 3.5.

Initially, for spacing reasons the inductor is split into two cores placed next to each other and connected in series, as shown in the

Table 3.5: Technical parameters and calculated performance of the designed inductor.

Description	**Symbol**	**Value**
Core material	-	SiFe3%-0.1mm
Potting material	-	Polyurethan cast resin
Geometrical parameters	(a,b,c,h)	(19, 158, 10.3, 57) mm
Litz wire	(d_{cu}, d_{s}, N_{s})	(3.7mm, 0.095mm, 735)
Winding isolation	-	Kapton (2x63µm)
Number of turns	N	12
Parallel conductors	N_{par}	3
Number of layers	n_{lay}	3
Air gap size	l_{gap}	1.6mm
Max. induction	B_{pk}	1.57T
Calculated core losses	P_{core}	250W
Calculated wdg. losses	P_{wdg}	180W
Calculated total. losses	P_{wdg}	470W
Calculated temperature rise	ΔT_{hot}	77°C
Core volume	Vol_{i}	0.61L
Efficiency @ D =0.5	η_{nom}	99.3%

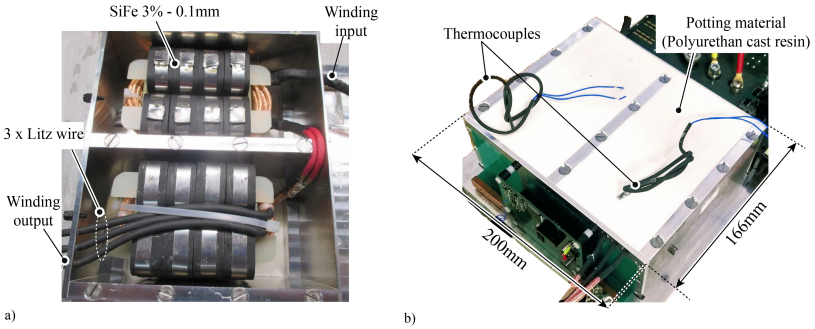

Figure 3.23: a) Prototype inductor cores connected in series inside the aluminum box, forming the module inductor L_i, before potting. b) Final assembly of the prototype inductor potted inside the aluminum box. The two thermocouples are placed on the winding for thermal verification.

pictures of Figure 3.23. The aluminum box is also extended in length for easier mechanical integration. The picture of Figure 3.23a shows the aluminum box before potting is applied while Figure 3.23b shows the final assembly of the potted cores along with the total dimensions of the module inductor.

The inductance of the prototype core is measured with a high current inductance analyzer, for pulsed inductance measurements under high current [92]. This measuring method allows the measurement of the inductance value as a function of the current. Furthermore, both the incremental (small signal) as well as the secant inductance (large signal) can be measured. In this application, the incremental inductance is relevant for ripple calculations around a certain operating point, while the secant inductance (often called transient inductance) is mostly relevant for the transient calculations (e.g. dynamic performance). The definitions of incremental and secant inductance are given in Figure 3.24

Figure 3.25 shows the measured values of the incremental and secant inductance as a function of the current, using a pulsed inductance measurement device [92]. Initially it can be noted that the intended nominal inductance value of 240µH is achieved, verifying the reluctance model used in the design phase of this work. The variation between the individual inductances is rather small ($\approx \pm 1\%$) and can be attributed to manufacturing tolerances (e.g. air-gap length).

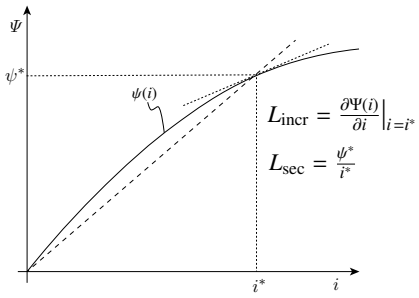

Figure 3.24: Definition of the incremental and the secant inductance used in this work. The incremental inductance is often referred to as small signal inductance. The secant inductance is often referred to as transient, dynamic or large signal inductance.

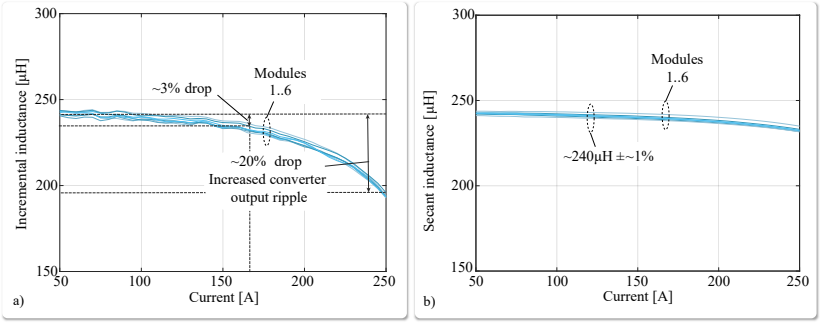

Figure 3.25: Measured inductance of all six prototype inductors with a high current inductance analyzer [92]. a) Incremental inductance measurement. b) Secant inductance measurement.

Furthermore, the secant inductance remains stable throughout the operating region and therefore the dynamic considerations during the design phase are valid. However, the incremental inductance starts dropping at around 150A and the design loses approximately 20% of its nominal inductance value till the 250A maximum pulsed current rating is reached. The drop can be attributed to the high DC bias that causes the relative permeability of the material to drop. This behavior along with the variation of the individual inductance values of the different modules, will result in an increase of the expected worst case steady

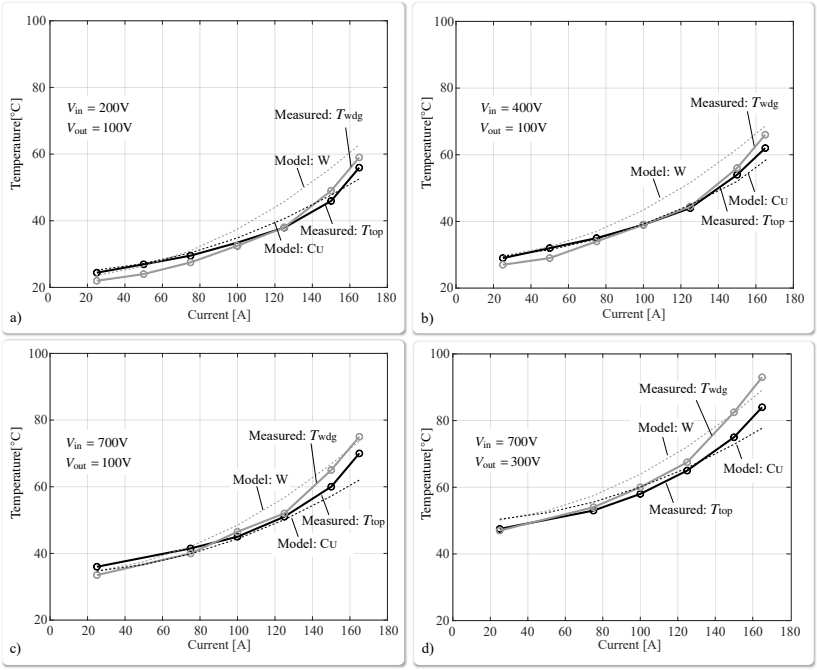

Figure 3.26: Thermal measurements performed for various operating points, for the prototype core. The temperature of the winding is measured with a thermocouple and the temperature at the top of the core with a thermal camera. a) $V_{\text{in}} = 200\text{V}$, $V_{\text{out}} = 100\text{V}$. b) $V_{\text{in}} = 400\text{V}$, $V_{\text{out}} = 100\text{V}$. c) $V_{\text{in}} = 700\text{V}$, $V_{\text{out}} = 100\text{V}$. d) $V_{\text{in}} = 700\text{V}$, $V_{\text{out}} = 300\text{V}$.

state ripple at the output of the current shaping converter. Therefore it needs to be taken into consideration when assessing the performance of the current source in terms of its steady state accuracy (see Sections 3.8 & 6.6).

To verify the feasibility of the core throughout the intended operating range, thermal measurements have been performed for various operation points. The temperature of the winding measured with the installed thermocouples as well as the temperature at the top of the core is measured and shown in Figure 3.26. By varying the input and output voltage, the current ripple is varied and as a result the core losses. On the other hand, the increased current ripple has a negli-

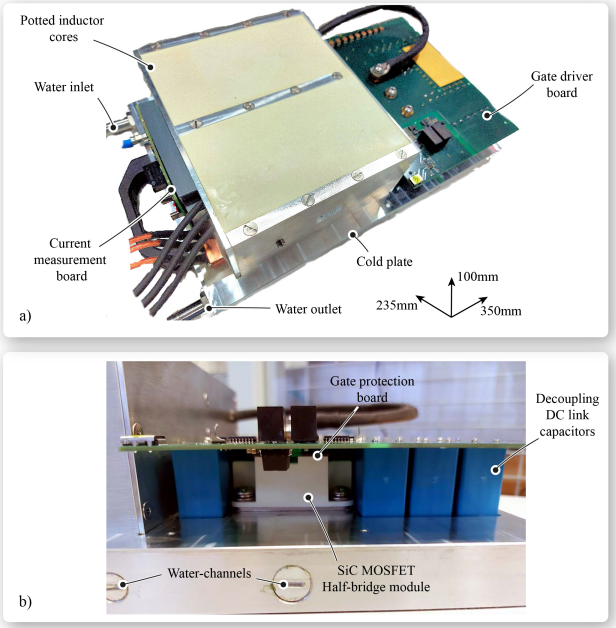

Figure 3.27: Pictures of a prototype module of the current-shaping-converter. The module can provide approximately 115kW of output power with a power density of 14kW/L. Total dimensions: 235mm x 100mm x 350mm.

gible effect on the winding losses for the prototype design, which are mainly determined by the DC current. At $V_{\text{in}} = 700\text{V}$, $V_{\text{out}} = 300\text{V}$ and $I_{\text{out}} = 165\text{A}$, which is the limit of the laboratory continuous power supply (50kW), the winding temperature reaches approximately 95°C. All the measurements are taken at steady state (after approximately 45 minutes the core reaches its steady state) and are performed for an inlet water temperature of 20°C and a water flow of approximately 10L/min.

Figure 3.26 shows also the temperatures resulting from the thermal model of Figure 3.11, for nodes W and C_U. It can be concluded that the model exhibits an acceptable accuracy (less than 15% error depending on the operating conditions) in predicting the temperature of the winding (node W) and the top of the core (node C_U).

3.7 Prototype Module Design

In this section the design of the prototype module that constitutes the backbone of the current-shaping converter is shown along with experimental verification of its performance. Pictures of the developed module are shown in Figure 3.27. It can be seen that apart from the potted inductor cores that consist a large part of the overall volume, decoupling/commutation DC-link capacitors close to the semiconductor module are included in the design to improve its switching performance. Furthermore, a relatively large PCB gate-driver power board is used, which also conducts the full continuous current (see Section 3.7.2). Finally a separate current measurement board that senses the module current is connected at the output of the inductor. The dimensions of the module are shown in the graph too. The module is designed for providing continuously 166A. The output voltage of the module is limited by the maximum duty ratio of the switches and the input voltage. For a DC-link of 800V and a maximum duty ratio of 0.95, the output voltage would be approximately 710V, which would result in a total output power of approximately 115kW. Overall the designed module achieves a rather conservative (for a non-isolated water cooled DC-DC converter) power density of 14kW/L.

At first, the overall efficiency of the design is measured and compared with the calculated one. Furthermore, a straightforward procedure to breakdown the losses of the module based on experimental measurements is shown. Later on, a closer look is taken into the design of the gate-driver board and the switching performance of the SiC device. Finally, a short section describes the design of the measurements (current and voltage), that is essential for the control of the system, and further experimental waveforms verify the operation of the prototype module.

3.7.1 Measured Efficiency and Loss Breakdown

The efficiency and the resulting power losses of the prototype module are measured with the LMG670 precision power analyzer [93]. The schematic of the setup is shown in Figure 3.28a, where the current sensors and voltage measurements are direct inputs to the power analyzer (noted with blue and green color respectively). The current through the inductor is controlled by the converter module and the input voltage while input/output voltage sources are in voltage control mode. By

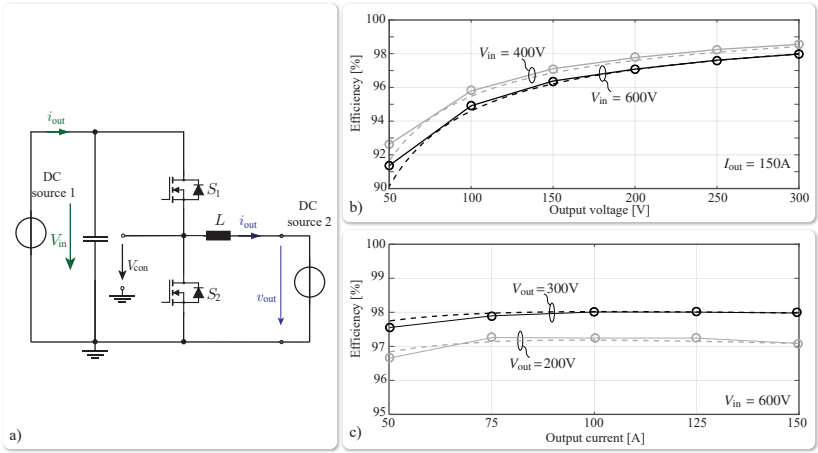

Figure 3.28: a) Schematic of the experimental setup used for measuring the efficiency of the prototype. b) Measured (solid) and estimated efficiency (dashed) as a function of the output voltage, for input voltages $V_{\text{in}} = 400\text{V}$ (gray curve) and $V_{\text{in}} = 600\text{V}$ (black curve) and output current $I_{\text{out}} = 150\text{A}$. c) Measured (solid) and estimated (dashed) efficiency as a function of the output current, for output voltage $V_{\text{out}} = 200\text{V}$ (gray curve) and $V_{\text{out}} = 300\text{V}$ (black curve), and input voltage $V_{\text{out}} = 600\text{V}$.

changing the output voltage, the operation point and therefore the ripple of the current is changed. This has an influence on the efficiency of the system. The input power and output power are then calculated by the power analyzer and the losses of the system can be determined. The efficiency is then calculated as $\eta = \frac{P_{\text{out}}}{P_{\text{in}}}$.

Figure 3.28b shows the measured efficiency of the system as a function of the output voltage for two different input voltages of 400V and 600V. Furthermore, Figure 3.28c shows the measured efficiency as a function of the output current, for two output voltage scenarios of 200V and 300V and a constant input voltage of 600V. In these figures, the estimated efficiency based on the presented loss models is also shown. It should be highlighted, that due to the limitations of the testing setup, the system cannot be operated with a power higher than 50kW, and therefore measurements only up to 50kW are shown. All in all it can be said that the results appear to be in line with the calculations.

Analyzing the measured losses as a function of the voltage and cur-

rent, can give further insights into the breakdown of the losses and the share of the losses that are dissipated in the core, the winding and the semiconductors respectively. Initially, by applying a short circuit at the output of the converter, and with the input power supply in current control mode, the conduction losses (winding losses and semiconductor losses) can be measured as a function of the current, and they are shown in Figure 3.29a. The figure also depicts the calculated conduction losses, based on the winding DC resistance and the semiconductor on-resistance, verifying the validity of the calculations used during the design/optimization procedure. It should be highlighted that in practice the measured losses in this scenario include also some ripple-induced losses, since the input power supply does not output a purely DC current. Nevertheless, in this case the ripple current was measured to be less than 5A and the ripple frequency was approximately 4kHz, making the assumption valid in practice.

Figure 3.29b shows the switching losses of the semiconductor device as a function of the output current, measured with a double pulse test experiment at an input voltage of $V_{\text{in}} = 600\text{V}$ (gray) and $V_{\text{in}} = 700\text{V}$ (black). A schematic of the setup is shown also in Figure 3.29b. The current measurement i_{semi} is performed with a 30MHz Rogowski coil

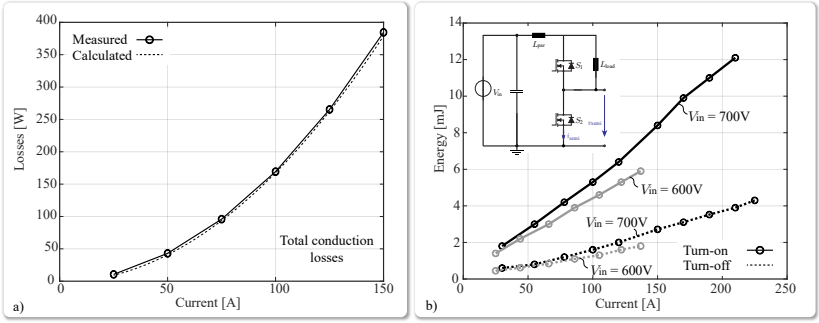

Figure 3.29: a) Measured (solid) and calculated (dashed) total conduction losses as a function of the output current. The total conduction losses include the conduction losses of the semiconductor as well as the winding losses of the inductor. b) Switching losses of the SKM260MB170SCH17 measured with a double pulse test procedure for two different input voltage levels $V_{\text{in}} = 600\text{V}$ (gray curve) and $V_{\text{in}} = 700\text{V}$ (black curve). The turn on loss (solid) energy and turn off loss energy (dashed) are shown too.

[94] and the voltage measurement with a standard 500MHz passive voltage probe (Lecroy PP007-WS-1).

Based on those measurements, the total measured losses can be completely broken down into the following:

- Conduction losses including the semiconductor and the winding conduction losses noted as P_{dc}.
- Switching losses of the semiconductor module noted as P_{sw}.
- Core losses noted as P_{core}.

Figure 3.30 depicts the total measured (solid) and calculated (dashed) losses, as a function of the output voltage for two different operating currents. Firstly, it is worth noting that the calculation is sufficiently accurate with an error smaller than 10% in the entire operating range. Additionally, assuming that the effect of the ripple current (and therefore the variation of the output voltage) on the switching and conduction losses is negligible, it can be concluded that the variation of the

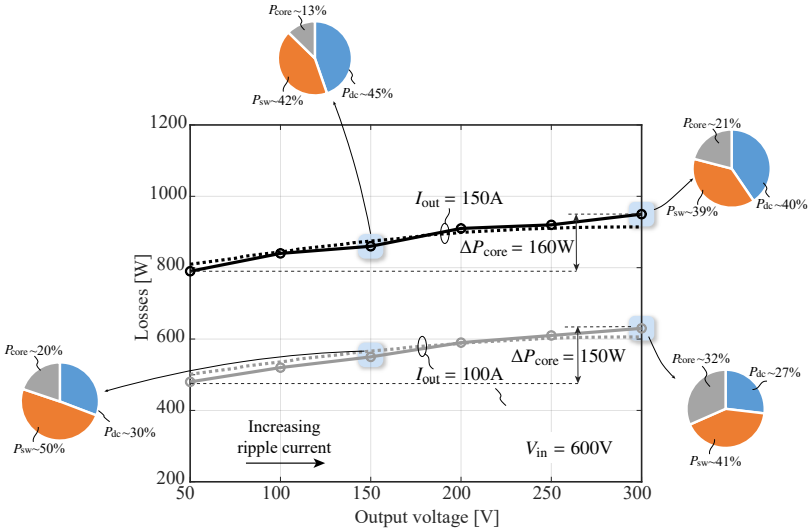

Figure 3.30: Total measured (solid) and calculated (dashed) losses, as a function of the output voltage for an output current of 100A (gray line) and 150A (black line). The loss breakdown for four different operating scenarios is also shown.

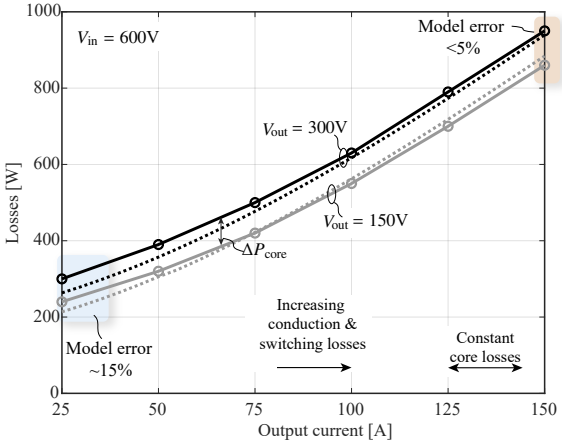

Figure 3.31: Total measured (solid) and calculated (dashed) losses, as a function of the output current for an output voltage of 150V (gray line) and 300V (black line).

total measured losses as a function of the output voltage, for a given output current, occurs solely due to the variation of the core losses, noted as ΔP_{core}. In other words, the switching losses P_{sw} and the conduction losses P_{dc} remain approximately constant for a given operating DC current, throughout the operating output voltage range of the system. It can be observed that ΔP_{core} is approximately equal for both DC operating scenarios, and therefore there is no evident influence, due to DC current bias on the core losses, at least up to 150A. As a reminder, the effect of the DC-bias on the core losses has also been neglected during the design procedure.

Another insight that can be gained by Figure 3.30 is that the contribution of the switching losses on the overall losses of the module is the highest. The contribution varies between 39% and 50%, and it is attributed mainly to the hard switching (high turn on losses) and the relatively high switching frequency of 60kHz.

Finally, Figure 3.31 shows the measured and calculated losses as a function of the output current, for two output voltage scenarios (150V and 300V). Based on the above the difference in losses between the two scenarios is attributed mainly to the core losses, which also remain unchanged for increasing output current, as the DC-bias effect has been

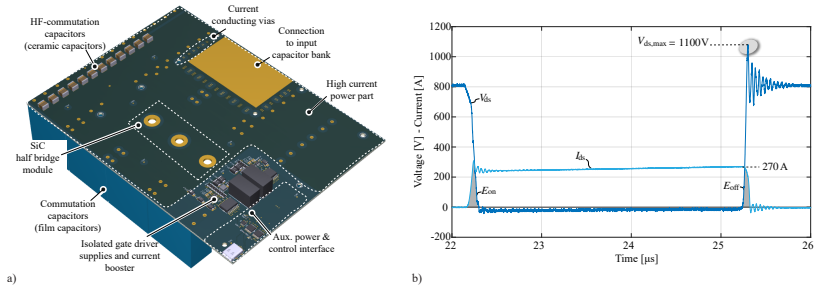

Figure 3.32: a) CAD illustration of the prototype gate driver power board and its main components. b) Results of the double pulse test with input voltage of 820V and total turn-off current of 270A.

proven to be negligible based on the insights gained from Figure 3.30.

In Figure 3.31 it is also highlighted that the accuracy of the model in the low output current region is significantly lower than in the high current region. Since the conduction losses (see Figure 3.29a) are accurately calculated, and the modeled switching losses are calculated based on an accurate fit of the measurements shown in Figure 3.29b, these results are suggesting that the core losses are underestimated. In this way as the share of the core losses in the total losses of the system is decreased, for higher output currents, the error of the model is decreased. Nevertheless, for the case of V_{out} 300V it is found that the core losses are underestimated by approximately 20% (model: 160W, measured: 200W).

3.7.2 Prototype Boards

The developed hardware and verification measurements of the gate driver and the current/voltage measurement boards of the converter module are shown in more detail in this section, as those play a significant role for the controllability and performance of the converter.

a. Gate driver

Figure 3.32a depicts the hardware prototype of the gate driver power board. The board is split into its high power part, with the full DC-link voltage and the high continuous current (166A) conducted through the PCB, and its low power part, which is driving the gates of the

half-bridge module. Several decoupling/commutation capacitors (film capacitors) are placed symmetrically around the module (i.e. total capacitance of approximately 170μF), in order to minimize the parasitic inductance, that is responsible for the voltage overshoot during turn-off, to improve the switching performance, and increase the switching speed. Furthermore, ceramic capacitors are placed on the board to further attenuate high frequency oscillations. It should be highlighted that the film capacitors provide the module with the ability to operate completely autonomously, without any connection to an external input capacitor bank.

Additionally, the board is designed to conduct the full 166A of continuous current, when it is operating in the continuous mode. For this reason it consists of 4-layers, with copper thickness of 70μm. Two layers are used for the connection to the DC+ and two layers for DC-. The current is spread through the layers with current conducting vias that are also visible in Figure 3.32a.

According to the IPC-2221A standard [95], the current capability of a conductor with certain cross section A and allowed temperature rise ΔT is given by:

$$I = k \cdot \Delta T^{0.44} \cdot A^{0.725} \tag{3.61}$$

where I is the current in amperes, A is the cross section in square mils, ΔT the temperature rise in °C and k is a constant such that:

$$k = 0.048 \text{ for outer layers} \tag{3.62}$$

$$k = 0.024 \text{ for inner layers} \tag{3.63}$$

Based on the above, a ΔT of approximately 30°C is expected at 166A. However since there are areas with a lower width for the current to flow, the board is expected to have some hot-spots. Nevertheless the conservative design allows for sufficient margin. Based on measurements with a thermal camera, the worst case temperature arises at the input of the current (100°C at 166A), where a clip-connector is used enabling an easier mechanical integration of the module. It was found that the rest of the board does not exceed 60°C, for an ambient temperature of 25°C.

The gates of the half-bridge module are controlled independently by dedicated signals that are interfaced with the master controller. A USB-C connector is used as it can transmit the auxiliary power (24V and approximately 4W of auxiliary power) together with 5 differential pairs.

Differential transmitters/receivers are placed on the board to receive the gate signals and transmit feedback to the master controller from the gate drivers in case of a fault (e.g. desaturation detection in case of short circuit). Isolated gate drivers are used together with isolated supplies to power both gates of the half-bridge. Since the maximum output current of the gate driver is not enough to charge the gate fast, a booster stage (current mirror) is also used, to increase the switching speed of the SiC half-bridge module [96]. Finally, for over-current protection, a desaturation circuit is used together with the gate driver IC [97].

Figure 3.32b depicts the switching performance of the lower side switch of the half-bridge with 820V DC-link voltage,and approximately 240A turn on current and 270A turn-off current. The drain-source current and drain-source voltage are shown and the switching energies can be extracted (used in the efficiency calculations previously). It can also be noted that a relatively clean turn-off transient is achieved, with only a few oscillations, and a maximum voltage of approximately 1.1kV, leaving sufficient margin of 100V till the nominal breakdown voltage of the MOSFET is reached.

b. Current measurement

The measurement of the module current is essential for the closed loop control of the system and constitutes a defining factor for the maximum dynamics and precision that can be effectively controlled. Understanding the feedback loop, its performance, limitations and uncertainties is also important for the modelling and development of the converter's closed loop control system. Consequently the current sensor, as well as its analog and digital electronics part need to be carefully selected.

Starting from the current sensor, it is necessary to use a DC-AC sensor able to measure a minimum of 270A, with a desired bandwidth of at least 300kHz to limit the analog delay and ensure proper dynamic performance. Those specifications alone, limit the selection significantly, as regardless of the current sensing technology that is used, the higher the current amplitude that needs to be measured, the lower the achievable bandwidth gets. In this work, a current sensor based on the anisotropic magneto-resistance effect (AMR) is used (CFS1000 [98]), providing an isolated measurement, with a bandwidth up to 500kHz. The sensor requires a U-shaped bar to conduct the current underneath the IC. The U-shaped bar is shown in more detail in the mechanical design of Figure

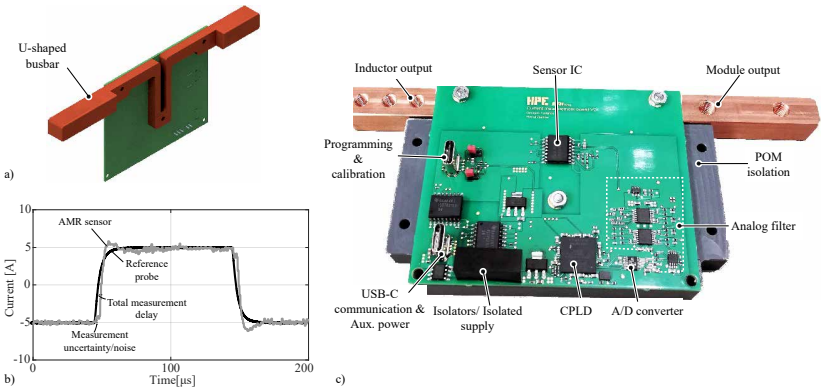

Figure 3.33: a) Side view of the mechanical design of the U-shaped bar that conducts the current, and produces the needed magnetic field sensed from the AMR sensor. b) Measurement of a 10A pulse current with the developed sensor (digitally measured on the CPLD) compared to the output of a reference current probe. c) Picture of the assembled prototype board.

3.33a[9]. A downside of the selected sensor is its relative low accuracy for the needs of the application, in the range of 1.5% after calibration. However, a higher accuracy combined with high bandwidth and high current range would result in the selection of a high-end, costly sensor. This selection clearly has a negative impact on the overall accuracy of DynACuSo.

Figure 3.33c, shows the developed prototype board, and highlights its most important parts. Apart from the current sensor IC, an analog filter is included in order to filter the inevitable noise that arises from the switching actions and distorts the measurement. The analog stage adds a calculated delay of approximately 3µs to the measurement. Moreover, a 13-bit ADC is used with a maximum sampling rate of 5MSps. The total sensitivity of the measurement is approximately 10mV/A, with approximately 100mA per LSB. Additionally, the board includes a dedicated FPGA. The FPGA produces the necessary clocks to the ADC, and receives the measurement. The on board FPGA then communicates the values to the FPGA of the main controller through differential digital isolators via the USB type-C interface also shown in

[9]the manufacturer provides also a software tool for the proper design of the busbar and the placement of the IC.

Figure 3.33c. The communication link runs with a clock of 60MHz (limited by the digital isolators) which corresponds to a maximum sampling frequency of 960kSPs.

Figure 3.33b shows a measurement of a current pulse with a reference probe, compared to the output of the total measurement chain, that is received by the main controller. Based on this measurement, the total delay of the current measurement loop can be found (approx. 6μs), along with the total measurement noise (±0.5A), as noted on Figure 3.33b. It should be highlighted that the measurement noise corresponds to approximately 3 bits and a large proportion of it arises from the isolated supply. The noise could be improved with an additional filter at the output of the isolated supply, for improved accuracy and control. Nevertheless, these insights are necessary for the design of the current control loop.

c. Voltage measurements and output stage

The input and output voltage need to be measured in order to ensure a precise control of the system and facilitate the controller, reducing the effort of the actuator. The voltage levels can be used in the control-scheme as feed-forward terms for the calculation of the duty cycle. More specifically, the input voltage levels V_1 and V_2 of the capacitor bank are changing slowly so there is no need for a high bandwidth/fast sampling measurement. A conventional RC voltage divider circuit is used, with a low bandwidth, to attenuate any possible high frequency noise arising from the switching actions, and the analog signals are sampled with a sampling rate of 200kSps.

On the other hand, the output voltage v_c experiences very fast changes, especially due to the damping of the output stage during transient operation, as described in Section 3.3. The output voltage measurement needs to be performed with a high bandwidth voltage divider and it also needs to be sampled fast in order to minimize the digital delays. In this work a compensated RC voltage divider has been used[10], together with an analog filter with a cut-off frequency at 400kHz, to reduce the noise that arises from the switching actions, similar to the one used for the current measurements. Furthermore, a 13-bit ADC is used and the communication link runs with a clock of 60MHz (limited by the digital isolators) which corresponds to a maximum sampling frequency

[10]the compensated RC divider features a theoretically infinite bandwidth, that is practically only limited by the parasitics of the SMD components on the PCB.

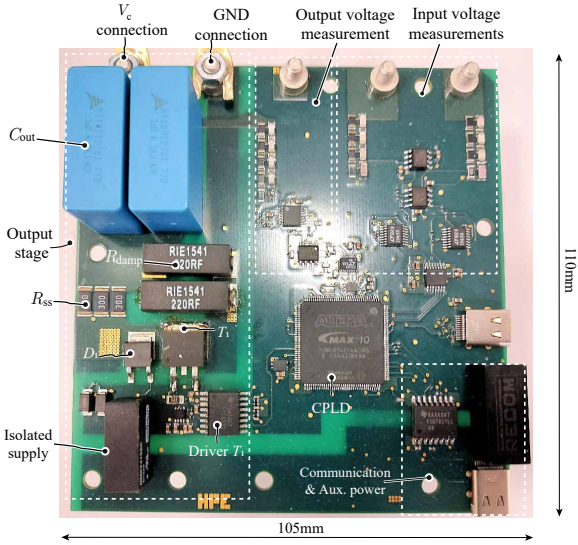

Figure 3.34: a) Top layer of the voltage measurement and the output stage (PAF).

of 960kSPs. The analog and digital delays are then identical to the ones of the current measurement board. In Figure 3.34, the board with the three voltage measurement circuits is shown and the main components of the circuits, the on-board FPGA and the communication interfaces are also visible. For the synchronization of all the measurements, the clock of the main controller is received and the three measurements are transmitted differentially.

Additionally Figure 3.34 depicts the prototype PAF output stage with the damping network and the semiconductors. The PAF is conveniently placed on the same board, and uses the on-board FPGA for the control of the switching actions. Large, pulse-proof damping resistors R_{d} are used, as they have to dissipate a large amount of power for a short time duration during the transient, while the steady state resistors R_{ss} have to conduct the continuous ripple current. The worst case losses for the R_{ss} do not surpass 3W and to ensure sufficient margin 6 parallel resistors (2512 SMD package) are used. The semiconductors (IGBTs and diodes) are chosen to have a breakdown voltage of 1.2kV and due to the low RMS current of the damping branch, low cost devices with

Table 3.6: Components of the output stage filter.

Description	Symbol	Part number
Output capacitor	C_{out}	B32774D0205K000
Steady state resistance	R_{ss}	CRCW251230R0JNEG
Damping resistance	R_{d}	S5-220RF1
Silicon IGBTs 1.2kV	T_1/T_2	HGT1S10N120BNST
SiC Diodes 1.2kV	D_1/D_2	C4D02120E-TR

relatively low current ratings can be chosen. The IGBTs are arranged in a common emitter configuration and therefore a single isolated power supply can be used to supply both gate drivers. Furthermore, standard gate drivers are used with a boost circuit (current mirror) in order to enhance the switching speed of the devices. Finally, a dedicated differential pair of the USB type-C interface is used to transmit the signal to turn-on/off the switches of the PAF from the main controller. The component part numbers of the active output stage are listed in Table 3.6.

3.7.3 Converter Module Operation

To validate the overall transient performance of the converter module and its PAF output stage, experimental results are shown hereby. Figure 3.35a shows the module current with a 100A step current reference, an input voltage $V_{\text{in}} = 700\text{V}$, and a purely resistive load of 0.7Ω. The module current of Figure 3.35a is measured with a DC-2MHz current probe (Lecroy CP500) and the module is controlled by the adaptive hybrid controller, that is described in Chapter 4 [48]. The module manages to achieve a current gradient of $2.6\text{A}/\mu\text{s}$.

Figure 3.35b shows the operation of the converter module, controlled with an open loop scheme for a current pulse of 165A, an input voltage 700V, and a resistive- inductive load of 0.75Ω and $50\mu\text{H}$. The module current (blue waveform) as well as the load current (red waveform) are shown, in order to assess the transient performance and verify the operation of the PAF output stage. During the current rise, the damping branch is enabled and it can be noted that the load current is almost identical to the module current, despite the large load inductance. Once the current reference is reached, the main controller informs the

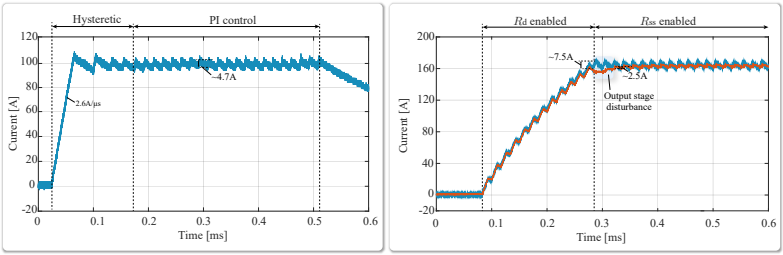

Figure 3.35: Experimental results of the converter module. a) Closed loop control of a single module: 100A current pulse with an input voltage $V_{\text{in}} = 700\text{V}$, and a purely resistive load of 0.7Ω. b) Open loop control of a single module with the PAF output stage included: 165A current pulse with an input voltage $V_{\text{in}} = 700\text{V}$, and a resistive- inductive load of 0.75Ω and $50\mu\text{H}$.

PAF (through the dedicated interface) that the transient is over. The switches of the PAF are then turned on and a small disturbance on the load current can be noted, as highlighted in Figure 3.35b. As expected, after the disturbance, the load current follows the module current, but its ripple is significantly reduced.

3.8 Prototype Current Shaping Converter

The assembled complete prototype system of the current shaping converter and its main components is shown in Figure 3.36. The six modules are placed in a large aluminum box. All modules and measurement boards communicate with the master controller via the USB type-C interface cables that are visible in the picture. The total dimensions of the system are also noted in Figure 3.36. For an easier maintenance and mechanical assembly, the modules can be slided in their respective positions in the aluminum box, and they are connected to the input busbars with a clip connector. The output busbar can be connected either to the step voltage generator or directly to the load for autonomous operation of the current shaping converter). The return busbar is also depicted in Figure 3.36, providing a connection to the load and to the middle point of the input capacitor bank.

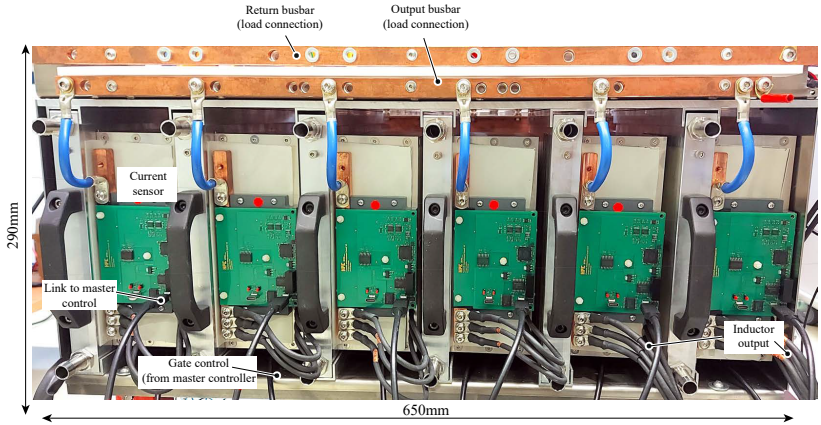

Figure 3.36: Picture of the prototype current shaping converter system with the 6-phase interleaved modules connected in parallel.

3.8.1 Experimental Results

To validate the operation and performance of the current shaping converter, various experimental results are included hereby. The following results depict the module currents measured with a DC-2MHz current probe, with a maximum range of 500A [99], the output voltage is measured with a 100MHz differential voltage probe [100] and the load current is measured with a 16MHz Rogowski coil with a maximum range of 1.2kA. It should be noted that current references of a maximum 1kA and a maximum flattop length of 500µs are shown here, to minimize measuring errors introduced by the droop of the Rogowsky coil.

Figure 3.37, shows the operation of the prototype system with a triangular reference (approximately 2.5A/µs ramp up and down). The load in this case is mainly resistive ($R_{\text{load}} = 0.3\Omega$) and a parasitic inductance of approximately $L_{\text{load}} = 4\mu\text{H}$ arises due to the loop connection to the load. The system is controlled in this case by a closed loop PI controller with a single update rate. Further details regarding the control structure are discussed in Section 4.1.5. In the magnified version it can be seen that the modules are well balanced and interleaving is achieved. The load current ripple is not visible since it is very small compared to the total current range that is measured.

Figure 3.38, shows the operation of the prototype system with a

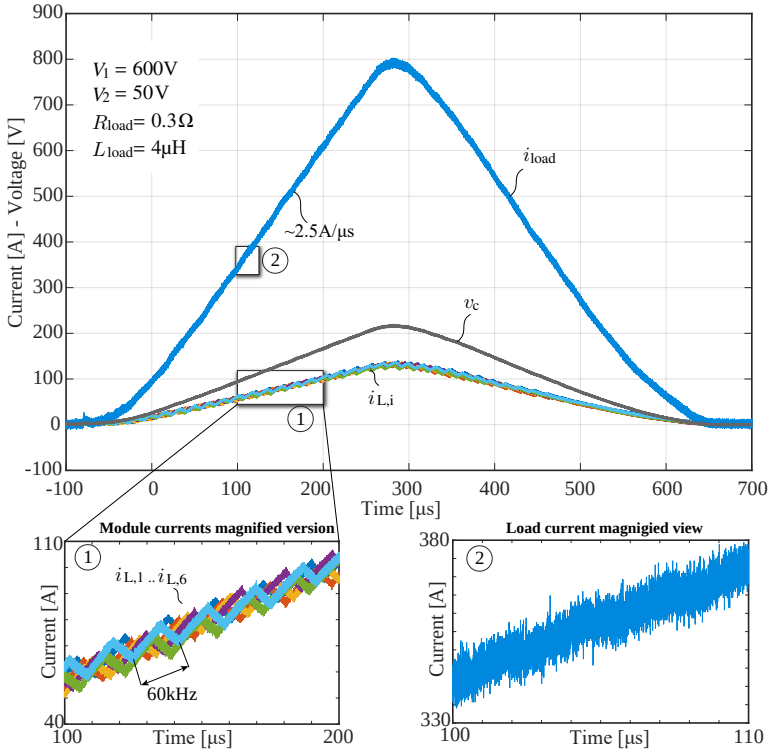

Figure 3.37: Experimental verification of the prototype current shaping converter system with a 2.5A/µs triangular reference. The module currents, the output voltage (gray) and the total load current (light blue) are shown. Experiment parameters: $V_1 = 600$V, $V_2 = 50$V, $R_{\text{load}} = 0.3\Omega$ and $L_{\text{load}} = 4\mu$H.

1000A, 500µs step reference current. The system in this case is controlled by the developed adaptive hybrid controller, which is described in detail in Section 4.1.5. Based on the magnified version of the step up dynamic, it can be seen that despite the reduced input voltage ($V_1 = 600$V) and the absence of the step voltage generator, the system manages to achieve a dynamic of over 10A/µs during step up. Additionally, it can be seen that the overshoot during the rise remains small, due to the high damping resistance used in the output stage. It should be clarified, that the higher ripple of the load current during the

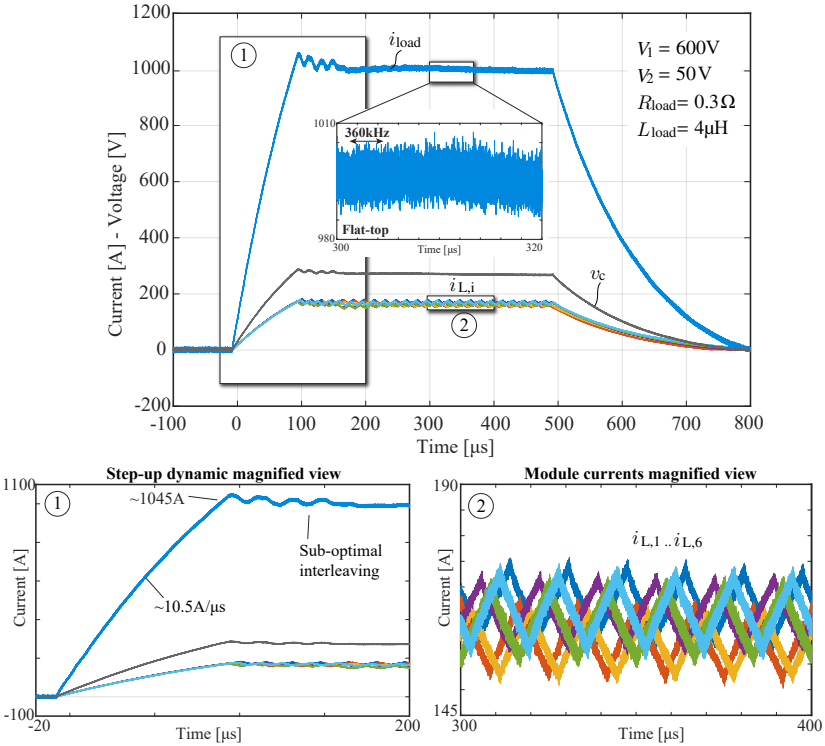

Figure 3.38: Experimental verification of the prototype current shaping converter system with a 1000A step current reference, controlled by the adaptive hybrid controller described in Section 4.1.5. The module currents, the output voltage (gray) and the total load current (light blue) are shown. Experiment parameters: $V_1 = 600\text{V}$, $V_2 = 50\text{V}$, $R_{\text{load}} = 0.3\Omega$ and $L_{\text{load}} = 4\mu\text{H}$.

initial switching cycles after reaching the desired reference, is due to the imperfect interleaving, and is also a result of the adaptive hybrid controller used to control the output current.

Furthermore, the flattop performance of the load current can be seen, and a 360kHz ripple component can be identified. However, it is noted again that due to the limited resolution of the load current measurement (Rogowsky coil with a sensitivity of 5mV/A), the accuracy and ripple of the load current cannot be accurately quantified. This result acts also as the motivation behind the work performed in Chap-

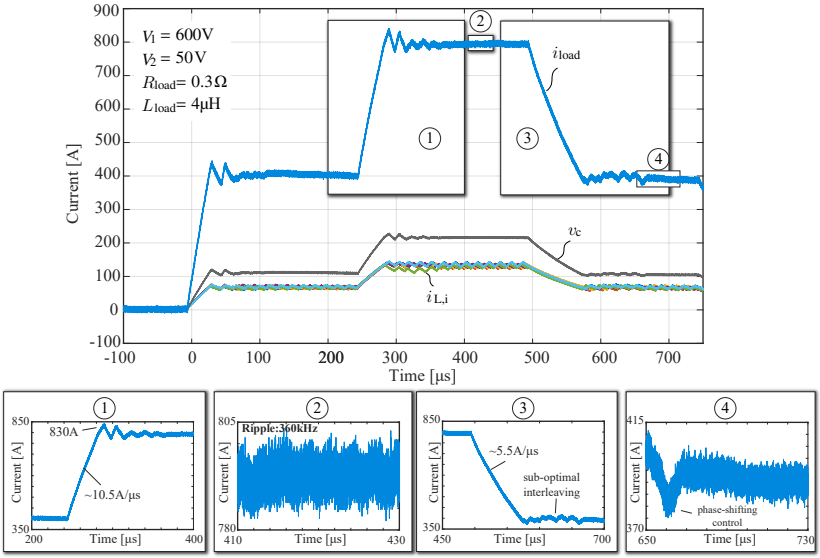

Figure 3.39: Experimental verification of the prototype current shaping converter system with a staircase-like reference sequence of 400A-800A-400A, controlled by the adaptive hybrid controller described in Section 4.1.5. The module currents, the output voltage (gray) and the total load current (light blue) are shown. Measurement parameters: $V_1 = 600\text{V}$, $V_2 = 50\text{V}$, $R_{\text{load}} = 0.3\Omega$ and $L_{\text{load}} = 4\mu\text{H}$.

ter 5, where a specially designed current transformer is developed to quantify the ripple of the current with precision and high sensitivity. Moreover, in the magnified version of the module currents, a slight imbalance is observed, which can be attributed to the sub-optimal tuning of the current sensor measurements. Nevertheless, the module currents are interleaved.

Finally, Figure 3.38 shows the operation of the current shaping converter system with a staircase-like waveform reference current in a 400A-800A-400A sequence. The prototype is again controlled by the adaptive hybrid controller and achieves a highly dynamic performance during both step up transients. During the step down transient, the dynamic is lower due to the absence of a the step voltage generator that could provide additional negative voltage. In addition, the sub-optimal interleaving is highlighted again during the initial switching cycles after

the reference current is reached, as a result of the actions of the adaptive hybrid controller. Due to the phase-shifting controller however, at steady state the module currents are interleaved and the total load current exhibits a 360kHz main ripple component. These control actions of the adaptive hybrid controller are explained in Section 4.1.5.

3.8.2 Overall autonomous performance

Finally in this section the overall dynamic and ripple performance of the developed prototype current shaping converter when operated autonomously (without the step voltage generator) is examined. The expected dynamic and ripple of the load current is calculated as a function of the load at different current set points in the operating range, with a minimum current of 300A. For every load combination, the resistors of the output stage R_{ss} and R_d are calculated based on equations (3.28) and (3.30), with Q=0.1 respectively.

For the calculation of the dynamic performance, the nominal inductance value (i.e. 240µH) is used for the module inductances, since as

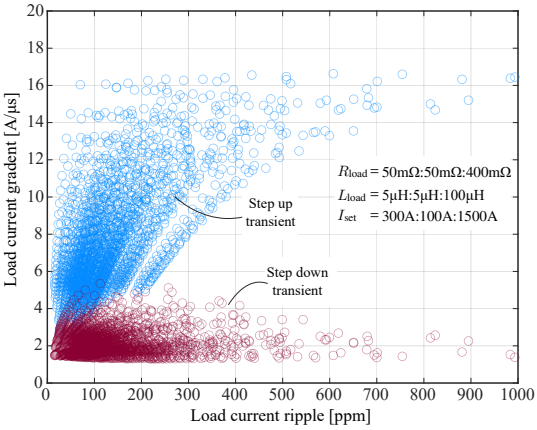

Figure 3.40: Calculated autonomous (no installed M3TC stages) performance of the current shaping converter operating. The current ripple is given in ppm. Both step up and step down performance is assessed hereby. Input parameters: $V_1 = 750$V, $V_2 = 50$V, $R_{load} = 0.05..0.4\Omega$ with a step of 0.05Ω, $L_{load} = 5..100\mu$H with a step of 5µH, and $I_{out} = 300..1500$A with a step of 100A.

shown in Figure 3.25 the secant inductance remains constant regardless of the operating bias current, and the individual inductances are almost identical. Regarding the ripple calculation however, the measured incremental inductances are modeled and fitted with a second order polynomial function. Therefore the value of the inductance in the calculations of the converter current ripple as a function of the current can be used for the calculation of the converter current ripple $\Delta i_{\mathrm{con,pp}}$, and since every inductance is slightly different, the full analytical solution of (3.13)-(3.15) needs to be used for a precise calculation of the load current ripple $\Delta i_{\mathrm{load,pp}}$.

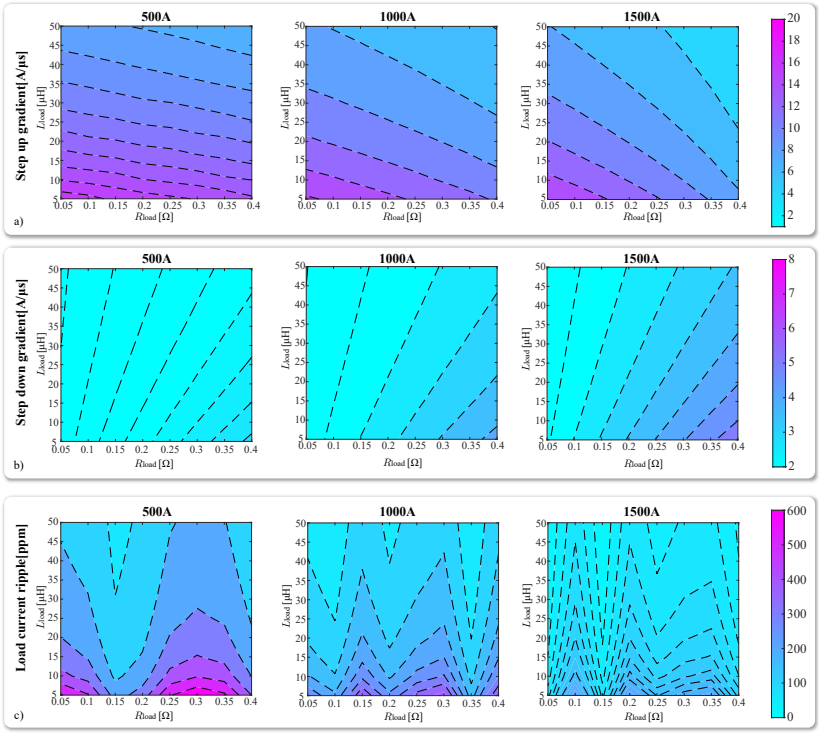

Figure 3.41: Calculated autonomous (no installed M3TC stages) performance of the current shaping converter as a function of the load for three different operating currents 500A, 1000A and 1500A. a) Step up gradient. b) Step down gradient. c) Load current ripple in ppm.

Figure 3.40 shows the calculated performance of all studied operation points for the current shaping converter. The studied operation points are noted in the picture. The current gradient varies between approximately 1.5A/µs and 17A/µs, depending on the load and the set point current. Similarly, the ripple current varies between 10ppm and 1000ppm. To calculate the current ripple in ppm, the calculated $\Delta i_{\mathrm{load,pp}}$ is divided every time by the respective operating current amplitude.

Figure 3.40 summarizes the overall performance of the current shaping converter but fails to give further insights regarding the role of the load and the operating current. To gain more insight, Figure 3.41 depicts the step up gradient, step down gradient and the ripple as a function of the load resistance and load inductance, for 3 different operating set-point currents.

Regarding the step up gradient it can be noted that for all three current set-point scenarios, the gradient is higher for lower R_{load} since the output voltage is lower, allowing for increased control margin. Furthermore, higher L_{load} requires a high output voltage to increase the current fast, and therefore the gradient is reduced. Between the different operating points, it can also be noted that the 500A set-point results in higher gradients due to the decreased output voltage. Regarding the step down gradient, the higher R_{load} and higher set-point current increases the output voltage, which facilitates the transient. Low R_{load} exhibit low current gradient even for low L_{load} due to the inability of the system to produce a negative voltage (only -50V can be applied across the module inductance). Based on these graphs it is clear that in order to achieve high dynamic performance in the step down, at least one step voltage generator stage should be included in the prototype system.

Lastly, the load current ripple $\Delta i_{\mathrm{pp,load}}$ is shown in Figure 3.41c. The converter current ripple $\Delta i_{\mathrm{pp,con}}$ depends on the duty cycle and therefore, the R_{load} and the operating current play a significant role as can be depicted in Figure 3.41c. Increasing the L_{load} and the operating current clearly decreases the ripple in ppm, as expected. Figure 3.41 can act as a guideline of the expected performance of the DynACuSo when the current shaping converter is operated autonomously.

Interim Summary

Multi-phase interleaved buck converters are employed in a wide range of modern power electronics systems, as they combine a high current rating, with a low current ripple, and an inherently simple hardware and software design. These systems are also especially suited for high-end current sources with high dynamic and low ripple requirements, such as the DynACuSo. However in these applications, design particularities render some of the common modelling assumptions invalid and therefore more detailed modelling of the converter output ripple for arbitrary loads has been performed in this chapter, taking into consideration among others the possible inductance asymmetries and the output voltage ripple.

Furthermore the output stage of such a system, despite its low volume plays a defining role in the overall performance and output current quality. In this chapter a passive adaptive output stage filter (PAF) suitable for systems with high dynamics, but also low ripple and high quality load current waveforms, has been presented. The PAF employs semiconductor switches to adapt the filter impedance and achieve a high cut-off frequency and high damping during the transients, and a relatively low cut-off frequency favoring ripple attenuation in steady state. After modelling the converter system, its output stage, and main components, a specification driven design space methodology has been followed in order to select a set of parameters that can theoretically fulfill given dynamic, load ripple and robustness specifications. After all, a six phase topology has been chosen, with each module switching at 60kHz and a module inductance of 240µH for the current shaping converter of the DynACuSo.

Particular emphasis has been given on this chapter in the optimization of power inductors for pulsed power systems, with high pulsed and continuous current rating. A generic optimization procedure has been determined, for such systems and the module inductors of the current shaping converter of the DynACuSo have been used as a case study. Various magnetic materials have been studied and Pareto-optimum designs for potted and non-potted cores have been identified for each material. In general, the potted designs have been proven to allow a lower core material volume which is a major factor to reduce the system's cost. Furthermore, the Amorphous and Nanocrystaline materials showed higher efficiency but SiFe 3% with 0.1mm lamination thickness

has been selected for the prototype system due to its lower cost. The Ferrite material N87 has been shown to be unsuitable for the chosen application. In particular for the selected SiFe 3% material the potted designs have achieved a notably higher efficiency and a significantly lower core material volume (approximately 5 times less core material volume). The prototype inductor has been verified experimentally, under various conditions and the accuracy of the governing models (loss and thermal models) ha been assessed, showing an accuracy between 5%-15% depending on the operating conditions. The efficiency of the system has also been measured experimentally, exhibiting approximately 98% measured efficiency with an output current of 150A, input voltage of 600V and an output voltage of 300V.

Finally, the prototype current shaping converter of the DynACuSo has been developed and experimental results verified its operation, under various scenarios. The prototype system has been shown to achieve more than 10A/μs, during step up transients. Last but not least, based on the presented dynamic and steady state models, the overall autonomous performance of the current shaping converter has been calculated. The gradient that can be achieved during step up has been shown to vary between 2A/μs and 17A/μs, depending on the connected load, while the gradient at step down varies between 1.5A/μs and 5A/μs, due to the absence of a sufficient negative voltage (only -50V available without the M3TC stage). The load current ripple also depends heavily on the operating conditions and the load, varying between 10ppm and approximately 1000ppm.

4

Systematic Evaluation of Control Concepts for Interleaved Buck Converters

Motivation

High bandwidth and precise current sources with the ability to deliver pulsed as well as arbitrary/controllable current waveforms are emerging nowadays, finding a broad spectrum of applications, such as power hardware-in-the-loop simulations (P-HiL) [27–32, 101, 102], driving accelerator magnets for medical and fusion energy applications [35–41, 103] or testing equipment for HVDC grids [8, 14–17, 19, 25]. The specifications of these applications are ever increasing, as they often require a high current rating combined with high dynamic (i.e. low rise/settling time) and a low ripple with good reference tracking capability.

In order to fulfill these specifications, a combination of optimized hardware and control design is usually necessary. The hardware optimization includes the selection of a proper topology and its parameters. The topology and the parameters are often chosen based on a specification-driven design space methodology, aiming to find a design space with solutions which are theoretically able to meet the specifications[1] [91, 104]. On the other hand, high-end systems do not afford to partly sacrifice their performance due to sub-optimal control and there-

[1] this methodology has been followed during the design of the DynACuSo, as discussed in Chapter 3.

fore, the control design needs to ensure that it makes the most out of the chosen topology and ensures that the full potential is successfully met. This often requires customized solutions, that differ depending on the needs of the application. Nevertheless, the choice of controller depends both on the the topology that is chosen as well as the current waveforms that are required.

Multi-phase, interleaved buck converter systems show great potential when operating as current sources, due to their high current rating and low ripple, combined with a very good dynamic performance and inherent control simplicity. However, regarding their control strategy various alternatives exist. The most widely used current control approach for interleaved DC-DC converters is the use of linear average-based current control methods (e.g. PI control) [105]. This method uses the average current of each phase in order to provide precise reference tracking while ensuring a constant switching frequency and equal current sharing between the phases. Despite its benefits and its simplicity, the maximum achievable bandwidth of this concept is compromised by inevitable closed-loop delays (i.e. measurement, communication and power stage delays). The concept has been applied in multi-phase converters implemented as a conventional PI control in [23], as an LQR-based state feedback control in [106] and H-infinity control in [107].

Another widespread control scheme that is often used for interleaved systems is the hysteretic controller [108, 109]. Due to its simple implementation, intuitive design and near optimal large signal properties, it is particularly attractive for highly dynamic systems. However, in its conventional form, it suffers from i) switching frequency jittering, that results in imprecise interleaving and therefore increased ripple, ii) inaccurate reference tracking and iii) imbalanced current sharing between the phases, in the presence of parameter mismatch.

Furthermore driven by the increased computational power of modern micro-controllers and FPGAs, model predictive control structures (MPC) have gained popularity recently. In MPC, an optimization problem is formulated and solved in each step in order to achieve the control objectives without violating pre-defined constraints. Generally in DC-DC power electronic converters, a longer prediction horizon leads to improved performance and stability of the MPC [110]. However, the growing need for higher switching frequencies imposes strict limitations to the maximum computation time required to solve the aforementioned optimization problem and practically results in a rather limited predic-

tion horizon [111]. Specifically for current control of buck converters, where the plant is a relatively simple single-input single-output (SISO) system without any cascaded loops and constraints for states, a long prediction horizon does not provide a significant benefit, and therefore MPC schemes constitute an attractive solution to increase the system's performance.

The aforementioned control concepts are well suited for systems such as the current shaping converter of DynACuSo, and identifying the best possible solution requires an in-depth evaluation of their performance under different conditions. To do so, a systematic evaluation is needed, based on pre-defined performance evaluation indicators and a well-defined optimization routine. Additionally, since many applications of the DynACuSo include a strictly specified step current waveform, in the course of this work, an adaptive hybrid controller specifically designed for step transients is proposed, and evaluated against four prominent control schemes: i) the conventional PI controller with a single update rate, ii) the PI controller with a fast execution rate, equal to the sampling frequency instead of the switching frequency iii) the LQR-based state feedback controller (SFC) and iv) the MPC. The detailed evaluation reveals the trade-offs in their performance and ad-

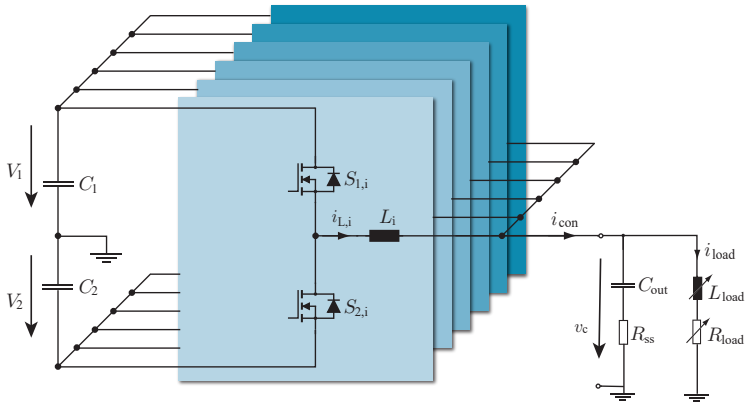

Figure 4.1: Schematic of the 6-phase interleaved current shaping converter of the DynACuSo, used as a test-bench for the evaluation of the different control schemes.

Table 4.1: Parameters of the studied 6-phase interleaved converter of the DynACuSo acting as a test-bench.

Parameter	Symbol	Value
Rated output current	i_{con}	1000A
Rated output voltage	v_{c}	600V
Upper DC-link capacitor voltage	V_1	750V
Lower DC-link capacitor voltage	V_2	50V
Module inductance	L_{i}	240µH
Module switching frequency	f_{sw}	60kHz
Output capacitance	C_{out}	3µF
Damping resistance	R_{ss}	5Ω

vantages/disadvantages in their employment. The most suitable controllers are also developed and their performance is experimentally demonstrated with the current shaping converter of the DynACuSo.

4.1 Modelling & Control Schemes

At first this section presents the investigated control structures as well as the necessary models and analytical expressions that are used to describe and simulate their performance. For a fair evaluation of all the different control structures, the feedback loop consisting of the current/voltage measurements, the necessary filters and digital delays are identical for all structures. It should be noted that the signal conditioning necessary to ensure a good measurement integrity is tailored for high power dynamic applications where the presence of high switching noise is pronounced in the system's sensors. As a test-bench for the evaluation of the controller's performance, the current shaping converter of the DynACuSo is assumed, and its topology is shown in Figure 4.1. The parameters are listed on Table 4.1.

The power stage and the feedback loop are identical for all the discussed control structures and the main assumptions for the common elements of the control loop are listed below.

- The available measured states of the system are the individual module currents $i_{\mathrm{L,i}}$, the output voltage v_{c} and the input capacitor

voltages V_1 and V_2. Since V_1 and V_2 are only slowly changing, their measurements are assumed to be ideal and possible delays are neglected.

- The power semiconductor stage (half-bridge) is assumed to be ideal, with a turn-on delay that is equal to the interlocking time. For the considered setup a rather conservative interlocking time of 500ns is assumed Since modern devices are assumed, the rise/fall times are considered to be significantly lower than the interlocking time, and therefore they are neglected. The on-state resistance of the switches is also neglected, as it does not influence the control performance and can be compensated. It should be noted that the power stage is modeled with the detailed switching model and not with a sub-cycle average model [112]. The power stage is signified in the following schematics with the blocks "Power stage delay" and "Switching stage" (see Figure 4.2).

- The module currents $i_{\mathrm{L,i}}$ are measured with a DC-500kHz bandwidth current sensor. The output voltage v_{c} is measured with a compensated RC voltage divider, with an assumed bandwidth of 500kHz. To filter the high frequency harmonics of the analog signal, an analog low pass filter is included, with a cut-off frequency of 400kHz in the design of both $i_{\mathrm{L,i}}$ and v_{c} measurement circuits[2]. The analog delay can be expressed as:

$$G_{\mathrm{analog}}(s) = e^{-s \cdot T_{\mathrm{sense}}} \tag{4.1}$$

  The sensors together with the analog filter are responsible for an analog signal delay T_{sense} of approximately 3µs, that is modeled in the following schematics by the block "Sensor delay" (see Figure 4.2).

- The sampling frequency of $i_{\mathrm{L,i}}$ and v_{c} is considered to be 960kHz, which is 16 times faster than the switching frequency of each individual module. Oversampling allows the reduction of the digital delays of the measured states, and enables the use of a controller that can be executed faster than the switching period, as will be discussed later. The digital delay is expressed as in (4.2).

[2] the current/voltage measurements were demonstrated in section 3.7.2

$$G_{\text{digital}}(s) = e^{-s \cdot N \cdot T_{\text{sample}}} \tag{4.2}$$

In this study, a delay of two sampling periods ($N = 2$) is assumed (i.e. one for the sampling of the ADC locally in the converter's module, and one for the serial communication of the measured value to the master controller). The digital delay of the system is modeled in the following schematics with the block "Sampling delay" (see Figure 4.2).

- Due to oversampling, some of the instances might coincide with switching actions resulting in noisy sampled values (a problem that is pronounced in high power converters due to the presence higher than usual noise). An intuitive and low delay method to filter out these values is to use a "median filter", that buffers k samples, sorts them and picks their median value. The transfer function of this median filter can be expressed as in (4.3), where the symbols $\lfloor$ and $\rfloor$ are used to signify the floor function.

$$G_{\text{median}}(s) = e^{-s \cdot \lfloor k/2 \rfloor \cdot T_{\text{sample}}} \tag{4.3}$$

In this study a median filter with $k = 3$ is used both in the current as well as in the voltage measurement of the studied system and results in a digital delay of an additional sampling frequency.

- In order to avoid possible static errors, and minimize the influence of the ripple a "moving average filter" is often used in converter systems, with an average frequency equal to the ripple frequency of the measured state. The transfer function of the moving average filter is shown in (4.4), where m is the number of samples of the moving window.

$$G_{\text{avg}}(s) = \frac{1}{m} \cdot \frac{1 - e^{-s \cdot m \cdot T_{\text{sample}}}}{1 - e^{-s \cdot T_{\text{sample}}}} \tag{4.4}$$

In this study, a moving average window is applied on the current measurements of the control loop, with $m = 16$.

- A conventional saw-tooth shaped PWM modulator is assumed in this work with a finite resolution that is defined by the switching frequency and the maximum clock frequency of the controller (i.e. 100MHz). The transfer function of the PWM module can be modeled as a Zero-Order-Hold (ZOH) block with a sampling frequency equal to the update speed of the controller (T_{exc}), or equivalently the update rate of the duty cycle that acts as a reference signal for the modulator. It should be observed that having an update rate higher than the sampling frequency is of no benefit. The transfer function of the PWM is then given by (4.5). Note that a faster execution speed for the controller (i.e. lower T_{exc}) leads to a lower PWM delay and therefore an improved performance is expected.

$$G_{\mathrm{PWM}}(s) = \frac{1 - e^{-s \cdot T_{\mathrm{exc}}}}{s} \tag{4.5}$$

4.1.1 PI with a Single Update per Switching Period

Due to its robustness, intuitive design and wide application in industrial systems, the PI control structure with a single update per switching period acts as the benchmark for this study. For interleaved converters each phase can control its current individually, and the sawtooth-shaped carriers used for the generation of the PWM can be phase-shifted to

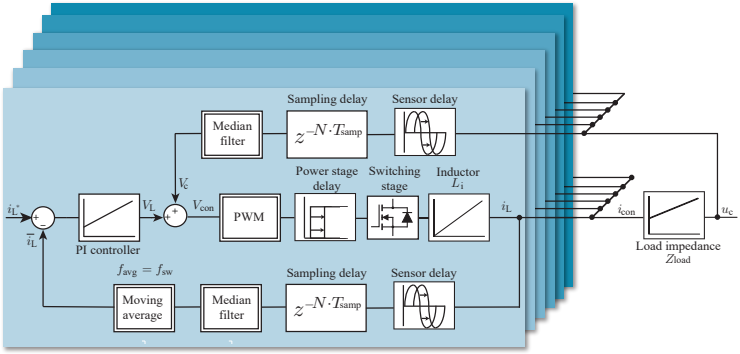

Figure 4.2: Schematic of the PI closed loop control structure for a 6-phase interleaved converter system.

result in an interleaved total converter current i_{con}. For optimum interleaving a phase-shifting controller can also be added and various methods that account for imbalances between the phases can be used [23, 113, 114]. The phase-shifting controller is discussed in section 4.1.5 for completeness, but its operation is irrelevant for the present study. It should also be noted that an external control loop for the total converter current can be included, but a preliminary study quickly showed that it offers no particular benefit to the performance of the overall system. The feedback control structure including the control delays and the converter plant is shown in Figure 4.2.

In this conventional implementation, the controller of each phase is updating its output (duty cycle) once per switching period. More specifically, the duty cycle is updated at the start of a new modulation cycle and as a result phase 1 updates its duty cycle at time instants [0, T_{sw}, $2T_{\mathrm{sw}}$, ..], phase 2 updates its duty cycle at time instants [$\frac{1}{6}T_{\mathrm{sw}}$, $\frac{7}{6}T_{\mathrm{sw}}$, $\frac{13}{6}T_{\mathrm{sw}}$, ..] and so on. This strategy guarantees a constant switching frequency under any circumstances, but also results in a relatively high delay as can be deduced from (4.5). For the studied system with a 60kHz switching frequency per module the delay of the PWM module based on (4.5) is $T_{\mathrm{exc}} = 16.67\mu\mathrm{s}$. For this control structure, the aim of the optimization procedure (Section 4.2) is to identify the optimum gains K_{p} and K_{i}.

4.1.2 PI with a Fast Update Rate

In contrast to the conventional PI control implementation, in this scheme the control output is updated multiple times per switching period. A common variance of this control structure is the PI controller that updates its reference duty ratio twice per switching period [115]. In this study however the control output is updated at every sampling period (i.e. 16 times per switching period), aiming to maximize the control performance and harness the fast switching capabilities of the latest generation of SiC devices. More specifically with this scheme the control output updates the duty cycle of all phases simultaneously at time instants [0, T_{samp}, $2T_{\mathrm{samp}}$, ..]. The control structure is identical to the one shown in Figure 4.2. For the studied system the only modelling difference is that the PWM module is modeled as in (4.5), with $T_{\mathrm{exc}} = 1.04\mu\mathrm{s}$.

Furthermore, while the conventional implementation results in a

constant switching frequency, updating the duty cycle multiple times may result in a higher switching frequency, especially during transients. Consequently a switching frequency limiter should also be implemented, to ensure that the semiconductors remain within their safe operating area, increasing the control complexity compared to the conventional scheme. Another downside of this scheme is that it usually requires a high-end control hardware with the capability to perform fast operations, and a power stage that consists of fast switching semiconductors that are able to execute the control commands accurately. As in the previous case, the aim of the optimization procedure for this control structure (Section 4.2) is also to identify the optimum gains K_p and K_i.

4.1.3 State Feedback Controller

In general, state space design allows the control engineer to have a better overview of the system and implement an optimized control law, achieved by pole placement or by LQR-tuning solving an optimization problem [116, 117]. Observer-based state feedback controllers have been shown to allow increased bandwidth compared to conventional PI controllers, as delay information can partly be accounted for during the observer design [118].

The control structure used in this study is shown in Figure 4.3. At

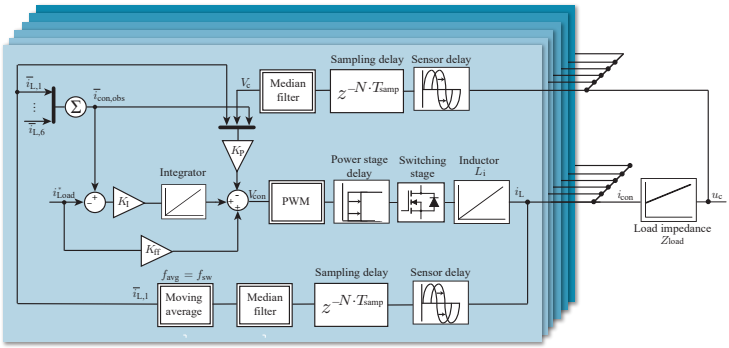

Figure 4.3: Schematic of the state feedback controller with a simple observer, for a 6-phase interleaved converter system.

first it should be highlighted, that the load current of the investigated current source converter is not directly measured. Due to its high nominal amplitude (more than 1kA) and its high bandwidth, an expensive sensor would be required[3][52]. Therefore, the total converter current $i_{\mathrm{con,obs}}$ is calculated by simply adding the available module currents $i_{\mathrm{L,i}}$ and the load current i_{load} is assumed to be approximately equal to i_{con}, which is guaranteed by the design of the output filter[4]. On the other hand, an observer based on the state space representation of the system (e.g. Leunberger observer) could be used for the reconstruction of i_{load}, accounting for the output stage parameters as well as the feedback loop delays. This approach is not followed in this study, in order to provide a fair comparison with the previously described controllers in terms of their complexity, and the treatment of the feedback loop. Furthermore, reducing the complexity of the controller allows the use of a faster execution rate, which benefits the system transient performance, as pronounced in Section 4.3.

Additionally as shown in Figure 4.3, an integral action is included for i_{load}. A preliminary study has showed that the integrator in this case improves the tracking capability of the system as well as its transient performance. Another option would be to include an integrator in the module currents $i_{\mathrm{L,i}}$ instead. In that way possible imbalances between the phases would also be mitigated. However, this approach is not followed in this study as the differences between the individual phases are considered to be negligible.

The formulation of the state feedback control problem and the calculation of the relevant matrices (namely K_{P}, K_{I} and K_{FF}) and reference signals are detailed in [119] and [120], but they are also summarized hereby for completeness.

Initially, the feed-forward gain K_{FF} of dimension 7×1 based only on $r_{i_{\mathrm{load}}}$ can be calculated from equations (4.6)-(4.8), with all the phases getting the same reference of 1/6 of the total reference, while the total reference $r_{i_{\mathrm{load}}}$ is applied on the observed state $i_{\mathrm{con,obs}}$, which is simply the sum of measured module currents $i_{\mathrm{L,i}}$.

$$\bar{N} \cdot r = K_{FF} \cdot r_{i_{\mathrm{load}}} \tag{4.6}$$

$$r = \begin{bmatrix} \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & 1 \end{bmatrix} \cdot r_{i_{\mathrm{load}}} \tag{4.7}$$

[3] a more extensive discussion takes place in Chapter 5.

[4] a suitable output stage has been demonstrated in Section 3.3.

$$K_{FF} = \bar{N} \cdot \begin{bmatrix} \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & \frac{1}{6} & 1 \end{bmatrix}^{\top} \tag{4.8}$$

$$\bar{N} = N_{\mathrm{u}} + K_{\mathrm{P}} \cdot N_{\mathrm{x}} \tag{4.9}$$

The gain matrices N_{u} and N_{x} can be calculated based on (4.10). In case the feed-through matrix D is zero, equation (4.10) simplifies to (4.11).

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} N_{\mathrm{x}} \\ N_{\mathrm{u}} \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{4.10}$$

$$\begin{cases} C \cdot N_{\mathrm{x}} = I \\ B \cdot N_{\mathrm{u}} = -A \cdot N_{\mathrm{x}} \end{cases} \tag{4.11}$$

The system matrices A, B and C correspond to the state space representation of a generalized dynamic system as given in (4.12), where x is the state vector, u the input vector and y the output vector. If the system is controllable and all its states are known, it can be stabilized by the state feedback law in (4.13) [120].

$$\begin{cases} \dot{x} = A \cdot x + B \cdot u \\ y = C \cdot x + D \cdot u \end{cases} \tag{4.12}$$

$$u = -K_{\mathrm{P}} \cdot x \tag{4.13}$$

For the interleaved converter system of Figure 4.1 the state space system is given by (4.14)-(4.19).

$$A = \begin{bmatrix} 0 & \cdots & 0 & \frac{-1}{L_1} & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \cdots & 0 & \frac{-1}{L_6} & 0 \\ \frac{1}{C_{\mathrm{out}}} & \cdots & \frac{1}{C_{\mathrm{out}}} & \frac{-R_{\mathrm{ss}}}{L_{\mathrm{p}}} & \frac{-1}{C_{\mathrm{out}}} + \frac{R_{\mathrm{ss}} R_{\mathrm{load}}}{L_{\mathrm{load}}} \\ 0 & \cdots & 0 & \frac{1}{L_{\mathrm{load}}} & \frac{-R_{\mathrm{load}}}{L_{\mathrm{load}}} \end{bmatrix} \tag{4.14}$$

$$B = \begin{bmatrix} \frac{1}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{1}{L_2} & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & \frac{1}{L_6} \\ \frac{R_{\mathrm{ss}}}{L_1} & \frac{R_{\mathrm{ss}}}{L_2} & \cdots & \frac{R_{\mathrm{ss}}}{L_6} \\ 0 & 0 & \cdots & 0 \end{bmatrix} \tag{4.15}$$

$$C = \begin{bmatrix} 1 & 0 & \cdots & 0 & 0 \\ 0 & \ddots & \ddots & \vdots & \vdots \\ \vdots & \ddots & 1 & 0 & 0 \\ 0 & \cdots & 0 & 0 & 1 \end{bmatrix} \tag{4.16}$$

$$x = \begin{bmatrix} i_1 & i_2 & i_3 & i_4 & i_5 & i_6 & v_\mathrm{c} & i_\mathrm{load} \end{bmatrix}^\top \tag{4.17}$$

$$u = \begin{bmatrix} V_\mathrm{con,1} & V_\mathrm{con,2} & V_\mathrm{con,3} & V_\mathrm{con,4} & V_\mathrm{con,5} & V_\mathrm{con,6} \end{bmatrix}^\top \tag{4.18}$$

$$y = \begin{bmatrix} i_1 & i_2 & i_3 & i_4 & i_5 & i_6 & i_\mathrm{load} \end{bmatrix}^\top \tag{4.19}$$

In the above, L_p is defined as the parallel combination of the module inductances L_i connected in parallel to L_load, as in (4.20).

$$\frac{1}{L_\mathrm{p}} = \sum_{i=1}^{6} \frac{1}{L_\mathrm{i}} + \frac{1}{L_\mathrm{load}} \tag{4.20}$$

In order to allow for cancellation of possible static errors that arise due to modelling errors the proportional system is augmented with the integrator, given in (4.21). The new control input that stabilizes the system is then given by (4.22).

$$\begin{bmatrix} \dot{x} \\ \dot{x}_I \end{bmatrix} = \underbrace{\begin{bmatrix} A & 0 \\ C_I & 0 \end{bmatrix}}_{\tilde{A}} \begin{bmatrix} x \\ x_I \end{bmatrix} + \underbrace{\begin{bmatrix} B \\ 0 \end{bmatrix}}_{\tilde{B}} u - \begin{bmatrix} 0 \\ 1 \end{bmatrix} r_I \tag{4.21}$$

$$u = -K\tilde{x} = -\begin{bmatrix} K_P & K_I \end{bmatrix} \begin{bmatrix} x \\ x_I \end{bmatrix} = -K_\mathrm{P} \cdot x - K_\mathrm{I} \cdot x_\mathrm{I} \tag{4.22}$$

In this work a preliminary analysis has showed that integral control in each module phase does not provide any particular benefit and therefore integral control is applied only on the total observed current $i_\mathrm{con,obs}$. Then the reference r_I of the state space system (4.21) simply becomes the total reference r_{i_load}, and the matrix C_I is given by (4.23). In turn the integral state x_I is defined by $\dot{x}_I = i_\mathrm{load} - r_{i_\mathrm{load}}$.

$$C_I = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}^\top \tag{4.23}$$

Finally in order to calculate the gains K_{P} and K_{I}, the unconstrained LQR optimization problem is formulated for the state space system [121]. The Q and R matrices are formed as in (4.24)-(4.25). Q is a 9×9 matrix and R is a 6×6. For the currents $i_{\mathrm{L,i}}$ the same weight w_{i} is assigned.

$$Q = \mathrm{diag}[w_{\mathrm{i}}, .., w_{\mathrm{i}}, w_{\mathrm{v}}, w_{\mathrm{icon}}, w_{\mathrm{int}}] \tag{4.24}$$

$$R = w_{\mathrm{R}} \cdot I_6 \tag{4.25}$$

For the state feedback control structure, the aim of the optimization procedure (Section 4.2) is to identify the optimum weights w_{i}, w_{v}, w_{icon}, w_{int} and w_{R}, that in turn result in the optimum gain matrices K_{P} and K_{I}.

4.1.4 Model Predictive Controller

Model predictive control (MPC) determines the next control action by solving an optimization problem at every time step. For power electronic systems, depending on the type of the optimization problem, MPC methods are mainly classified into two different types: i) the finite control MPC (FCS-MPC) and ii) the continuous control set MPC

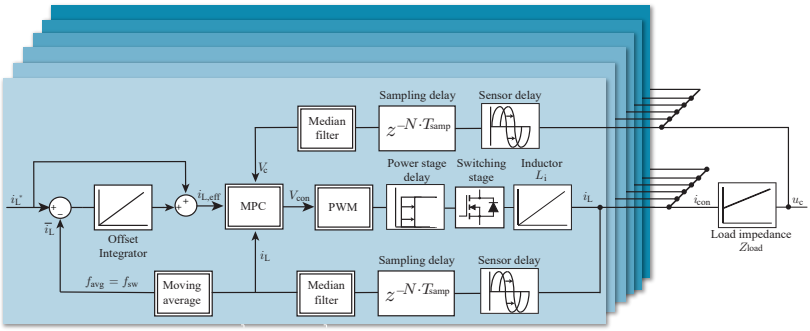

Figure 4.4: Schematic of the MPC closed loop control structure for the 6-phase interleaved converter system.

(CCS-MPC) [122], [123]. The FCS-MPC takes into account the switching behavior of the converter and formulates an integer optimization problem for deciding the switch signals directly. On the other hand, the CCS-MPC typically solves a convex optimization problem to compute a continuous control signal and generates switching signals of power semiconductors with a modulator. In this paper, a CCS-MPC is formulated and compared such that a fair comparison with the other control schemes can be made. Note that the use of CCS-MPC ensures constant switching frequency, since the control output is updated once per period[5], and allows straightforward current sharing between the interleaved phases.

The schematic of the controller is shown in Figure 4.4. Each phase computes its duty cycle at every switching interval ($1/f_{\mathrm{sw}}$) and triangular carriers are used for the generation of the PWM. Note that the PWM carriers are phase-shifted and so are the MPC computation instances, just like in the case of the PI with a single update rate.

The plant model for each phase corresponds to the differential equation (4.26), where R_{p} represents the sum of the parasitic resistances of the semiconductor devices and the phase inductor, and V_{con} is the averaged converter voltage over one switching interval.

$$\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} = -\frac{R_{\mathrm{p}}}{L} \cdot i_{\mathrm{L}} + \frac{1}{L} \cdot (V_{\mathrm{con}} - V_{\mathrm{c}}) \tag{4.26}$$

The next state of the current can be discretized as in (4.27), where a, b and f are coefficients that can be determined based on (4.26), assuming that V_c stays constant during a switching period.

$$i_{\mathrm{L}}[k+1] = a \cdot i_{\mathrm{L}}[k] + b \cdot V_{\mathrm{con}}[k] + f \cdot V_c[k] \tag{4.27}$$

The optimization problem can then be formulated in a linear MPC format, aiming to find the future control input that minimizes the difference between the predicted current state and the current reference.

[5]executing the MPC with a fast update rate would significantly increase the burden on the control platform and is not considered in this work.

$$\min_{\mathbf{U}[k]} \sum_{l=1}^{N} \left\| i_{\mathrm{L}}[k+l] - i_{\mathrm{L}}^{*}[k+l] \right\|_{\mathbf{Q}}^{2} \tag{4.28a}$$

$$\text{subject to} \quad -V_2[k] \leq V_{\mathrm{con}}[k+l] \leq V_1[k] \tag{4.28b}$$

In (4.28), $\mathbf{U}[k] = [V_{\mathrm{con}}[k], \cdots, V_{\mathrm{con}}[k+N-1]]^{\mathrm{T}}$ is the future control input, N is the prediction horizon, $\mathbf{Q} \geq 0$ is a weighting matrix and $\|\mathbf{z}\|_{\mathbf{Q}}^{2}$ denotes a 2-norm with the weighting matrix. V_1 and V_2 are the voltage levels of the split DC-link.

Since long prediction horizons do not provide much benefit for current control of SISO systems, $N = 2$ is chosen in the course of this work. A short prediction horizon simplifies the implementation of the control scheme. Additionally, as shown in Figure 4.4 an offset integrator is used in the MPC structure to account for inevitable model mismatches [124]. The integrator is enabled only when the average module current $i_{\mathrm{L,avg}}$ reaches approximately its steady-state (i.e. within a 5% tolerance band), and it is associated with a gain K_{i}. Finding the optimum K_{i} that minimizes the performance evaluation indicators is the goal of the upcoming optimization procedure in the case of the MPC, in Section 4.2.

$$i_{L,\mathrm{eff}}^{*} = i_{L}^{*} + \sum K_i \cdot T_{\mathrm{sw}} \cdot (i_{L}^{*} - i_{L,\mathrm{avg}}) \tag{4.29}$$

Moreover, in order to avoid excessive overshoot during transients, a simple prediction of the future current state delay model of the current/voltage measurement is used. More specifically, the delay model simply adds the contributions of the discussed delays and expresses them as a first order delay system. Ignoring these delays during the MPC design would result in an unacceptable control behavior, especially during step transients.

Finally, regarding the implementation of the MPC, the prediction model is represented in a linear system and only polytopic constraints are applied on control inputs. As a consequence the resulting optimization problem is a quadratic programming (QP) problem, and an explicit MPC method as proposed in [125] can be utilized. The explicit MPC handles the optimization process offline and enables implementation at fast rates, without excessive usage of control platform resources [126].

4.1.5 Adaptive Hybrid Controller

In literature various hybrid controllers have been utilized, combining the advantages of different control schemes and providing an overall improved performance both in transients as well as in steady state. Such a hybrid controller that uses a PID controller in combination with a sliding mode scheme was presented in [127]. The presented control concept exhibited time-optimal response and good disturbance rejection capability. Although the concept is particularly interesting, its conceptual complexity due to its non-linear nature and high implementation cost makes it impractical, as highlighted in [128]. The hybrid controller in [129] showed improved large signal disturbance rejection capability in voltage regulation mode and in [130] an MPC-based, constrained optimal hybrid controller was introduced, making use of look-up tables based on a sophisticated model of the converter.

In general, the hysteretic controller provides excellent, near time-optimal transient performance. Particularly its digital implementation however suffers from switching frequency jittering that prevents the interleaving of the module currents at steady state [109]. To achieve a good performance at steady state, accurate measurements are needed at high sampling rates, which is extremely challenging for high power DC-DC converters with already high switching frequencies operating in noisy environments. Apart from that, the precision of the hysteretic controller in steady state is severely downgraded due to parasitic elements and sensing delays that need to be compensated [131].

On the other hand, the PI control ensures accurate current sharing between the individual phases, precision in steady state and design simplicity. Due to its constant switching frequency, it can provide robust interleaved operation, when it is combined with a phase-shifting controller. However, its transient performance is limited due to the unavoidable closed loop delays that decrease the achievable bandwidth and in general keeping the module currents interleaved during transients hinders the ability of the controller to harness the full potential of the topology, when it comes to its reaction to transients.

The hybrid combination of the PI & hysteretic controller could result in a potential concept with excellent transient and steady state performance, and it is particularly interesting for dynamic current sources operating with step transients. In this section an adaptive hybrid controller for interleaved converter systems is presented. The proposed scheme performs particularly well when delivering step transients, and

proposes an algorithm to achieve low disturbance transition between the two modes of operation.

At first, Figure 4.5 gives an overview of the proposed interleaved hybrid controller for a 2-phase system[6], but the extension to an n-phase system is straightforward, simply by adding identical slave modules in parallel. Each module's control system consists of an average current mode control scheme (e.g. PI combined with phase-shifting controller) and an adaptive hysteretic mode along with a supervising algorithm, that determines the control mode that is used.

[6]the feedback loop is simplified for clarity.

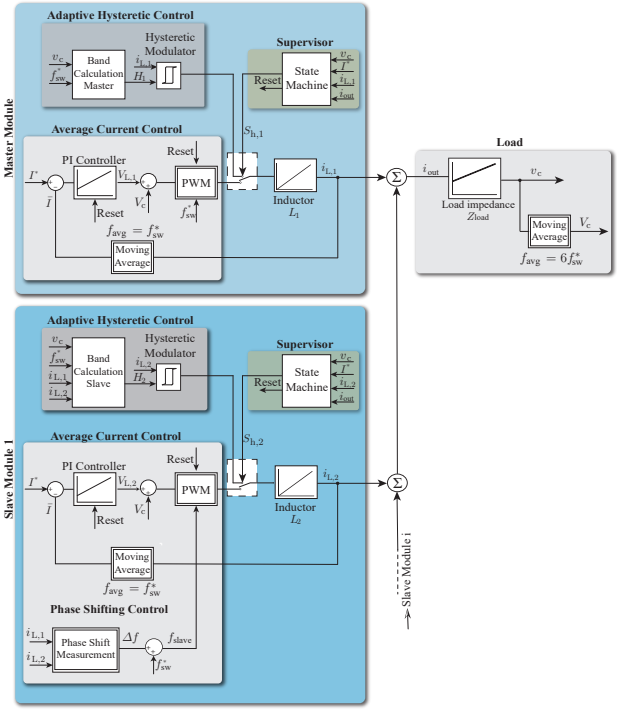

Figure 4.5: Simplified schematic of the proposed interleaved hybrid control scheme with two modules (one master & one slave). The slave module consists of: i) an average current mode controller (PI control and phase-shifting control) which is enabled during steady state, and ii) an adaptive hysteretic mode controller, which is enabled during transients.

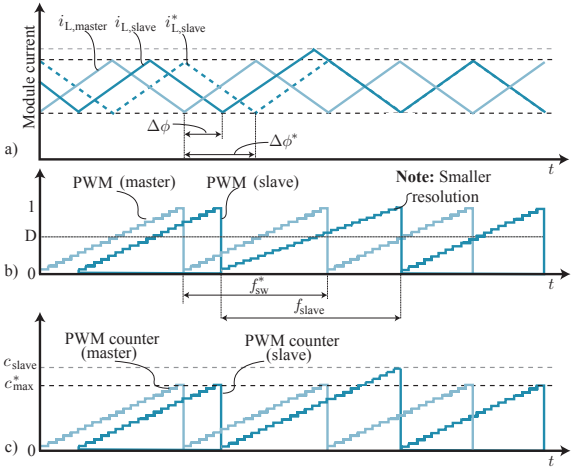

Figure 4.6: Operation of the phase-shifting controller. a) Master and slave module currents. b) Master and slave digital PWM. c) Master and slave PWM counters. In this scenario, the measured phase-shift $\Delta\phi$ is smaller than the reference phase-shift $\Delta\phi^*$ so the slave's PWM maximum counter c_{slave} is increased according to (4.31), decreasing the switching frequency f_{slave}, and shifting $i_{\text{L,slave}}$ to its reference position $i^*_{\text{L,slave}}$, within one switching period.

a. Operation at Steady State and Non-Step Transients

At steady state the average current mode is enabled[7] consisting of a PI controller and a phase-shifting controller, as shown in Figure 4.5. It should be clarified that any other average current control scheme can be used (e.g. state feedback control etc.) but for this work a PI controller is considered. Since the PI controller was described in more detail in section 4.1.1 only the operation of the phase-shifting control is given hereby.

At the start of each switching cycle, the relative phase difference $\Delta\phi$, between the master's module current $i_{\text{L,master}}$ and the slave's module current $i_{\text{L,slave}}$, is measured. As shown in Figure 4.6, $\Delta\phi = 1$ is defined such that $i_{\text{L,slave}}$ is lagging $i_{\text{L,master}}$ by one switching period, while $\Delta\phi = -1$ is defined such that $i_{\text{L,slave}}$ is leading $i_{\text{L,master}}$ by one switching period. It is then clear that: $|\Delta\phi| \leq 1$. Similarly, the relative reference phase shift of each slave module $\Delta\phi^*$ depends on the total number of

[7] it is also enabled during non-step transients.

phases n and is given by (4.30).

$$\Delta\phi^* \in \left\{ -\frac{n-1}{n}, \ldots, -\frac{1}{n}, \frac{1}{n}, \ldots, \frac{n-1}{n} \right\} \tag{4.30}$$

Accurate interleaving is achieved by adjusting the switching frequency of the slave module f_{slave}. A switching frequency adjustment of a digital PWM, simply requires a change in the resolution of its clock, as shown in Figure 4.6b. This modification is implemented with a change in the maximum value of the counter of the slave's PWM c_{slave} compared to the reference maximum counter value c^*_{max} of the master's PWM, as shown in 4.6c. The value of c_{slave} is then given by (4.31).

$$c_{\text{slave}} = c^*_{\text{max}} + (\Delta\phi^* - \Delta\phi)\, c^*_{\text{max}} \tag{4.31}$$

With this method, interleaving is ideally achieved within one switching cycle. However, it should be noted that a slight disturbance is introduced in the converter output current i_{con} during the switching cycle in which the resolution change occurs, due to the increased ripple and sub-optimal interleaving. In order to avoid high disturbances, the switching frequency change can be limited to a certain percentage of the reference switching frequency. This method would clearly then require more than one switching cycles to lead to optimal interleaving.

b. Operation with Step Transients

The adaptive hybrid controller makes use of the excellent large signal properties of the hysteretic controller, when a step transient is initiated. The ideal operation of the controller for a system with two modules is shown in Figure 4.7.

At $t = t_0$: A reference change is detected and the hysteretic controller is enabled, i.e. the status of the signal $S_{\text{h},1}$ for the master and $S_{\text{h},2}$ for the slave (Figure 4.5) is changed from 0 to 1. Initially, the hysteresis band is set to a low value (H_0) in order to avoid a large overshoot of the converter output current i_{con}, since the interleaved operation is lost and the current ripples of $i_{\text{L},1}$ and $i_{\text{L},2}$ are added[8]. Setting the hysteresis band to a low H_0 value could cause a temporary increase in the switching frequency that only lasts however for one switching

[8] in fact a small phase-shift will always be present when the transient is initiated from an interleaved state.

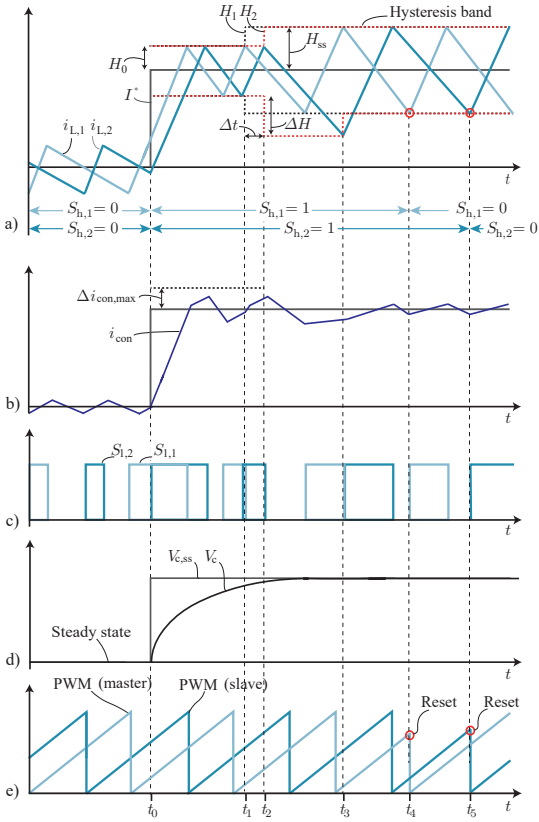

Figure 4.7: Operation of the interleaved hybrid controller during a step transient for an interleaved system with two modules: a) Master and slave module currents. b) Converter output current i_{con}. c) Switching pulses of the upper switch of the master and slave module. d) Average converter output voltage V_c and steady state voltage $V_{c,ss}$. e) PWM counter of the master and slave module.

cycle. The initial band H_0 can be set based on the maximum allowed overshoot of the converter output current $\Delta i_{out,max}$, as $H_0 = \frac{\Delta i_{out,max}}{n}$, since in the worst case the current ripples of all the module currents are added. As shown in Figure 4.7b, the maximum limit of $\Delta i_{out,max}$ is not hit due to the small phase-shift between $i_{L,1}$ and $i_{L,2}$. However, the ripple of i_{con} is relatively large as the interleaved operation is lost.

At $t = t_1$: The current of the master module reaches its peak value $I^* + H_0$ for the second time and the average converter output voltage V_c is almost settled. The hysteresis band calculation block samples the average voltage V_c and updates the hysteresis band of the master module to approximately its steady state value H_{ss}, given by (4.32).

$$H_{ss} = \frac{1}{2Lf_s}\left(1 - \frac{V_2 + V_c}{V_1 + V_2}\right)(V_2 + V_c) \tag{4.32}$$

At $t = t_2$: The slave's current reaches its peak value $I^* + H_0$ and the time shift Δt between the two currents is measured. The slave's band calculation block then re-calculates the hysteretic band of the slave module and adjusts it by ΔH, in order to restore the interleaved operation of the system in the next switching period. The adjustment ΔH can be calculated based on (4.33), where Δt^* is the ideal time shift for interleaved operation.

$$\Delta H = (\Delta t^* - \Delta t)\frac{S_1 S_2}{S_2 - S_1} \tag{4.33}$$

In (4.33), S_1 and S_2 are the slopes of the triangular current rise/fall which for the considered buck-type converter are given in (4.34).

$$S_1 = \frac{V_1 - V_c}{L} \qquad\qquad S_2 = \frac{-V_2 - V_c}{L} \tag{4.34}$$

At $t = t_3$: The interleaved operation is achieved and the hysteretic band of the slave becomes equal to the steady state value H_{ss}. It can be observed in Figure 4.7b that the ripple of i_{con} reduces significantly after the adaptation, since the current ripples are canceled out. It should be noted that possible inaccuracies in the phase-shift between the module currents must be expected due to the non-ideal characteristics of the hysteretic control and the fact that the average output voltage V_c is affected by the band adaptations (phase-coupling). However, the error will be corrected by the phase-shifting controller at steady state, as previously described.

At $t = t_4$: The master's current reaches the lower limit of the hysteresis band and V_c has settled, so the signal $S_{h,1}$ changes its status enabling the average current mode and the PWM clock of the master module is reset.

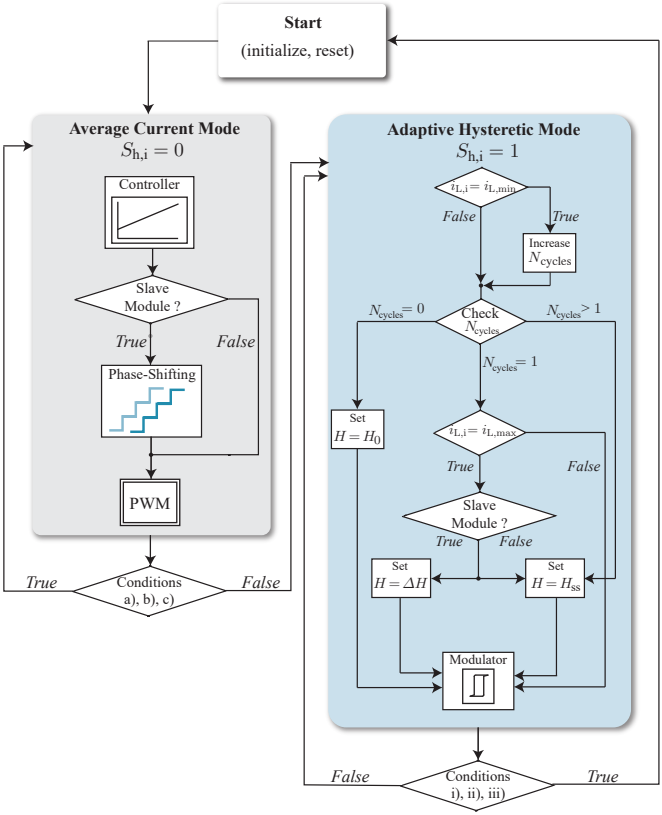

Figure 4.8: Flowchart of the interleaved hybrid controller. In average current mode, the supervisor checks conditions a)-c). In hysteretic mode, the supervisor checks the mode-shifting conditions i)-iii).

At $t = t_5$: The slave's current reaches the lower limit of the hysteresis band and the signal $S_{h,2}$ changes its status setting the slave module to average current mode and the PWM clock of the slave is reset.

It should be highlighted that phase-shifting the module currents already in the hysteretic control mode is crucial for the smooth return of the controller to the PI mode and the minimization of the disturbance. This technique leads to a faster return to interleaving, and therefore lower ripple. It should also be observed that in the presence of feedback time delays, appropriate compensation is necessary in order to avoid

excessive overshoot/undershoot of the module currents.

Time delays can have a particularly deteriorating effect on the hysteretic mode of control of highly dynamic converters, as the set boundaries for the current are not met leading to excessive ripple and overshoot [109]. Fortunately, when the total current measurement delay of the feedback loop is known[9] accounting and compensating for it is fairly simple. As a result of the time delay compensation, the current threshold values need to be adjusted according to (4.35), where t_{delay} is the total delay of the current feedback loop. $H_{\text{r,comp}}$ is subtracted from the upper current boundary, while $H_{\text{f,comp}}$ is added to the lower current boundary.

$$H_{\text{r,comp}} = S_1 \cdot t_{\text{delay}} \qquad H_{\text{f,comp}} = -S_2 \cdot t_{\text{delay}} \tag{4.35}$$

It should be pointed out, that the voltage measurement delay can also be compensated, but that would require a knowledge/estimation of the output load. The additional calculations needed could also put excessive workload for the controller, resulting in computational delays that hinder the ability of the controller to react in time[10]. For these reasons, simply a compensation voltage constant ($V_{\text{c,comp}}$) is established in this work, and it is applied by simply adding it to the measured voltage V_{c} during rise of the currents, or subtracting it from the measured voltage V_{c} during the fall of the currents. Depending on the load, the compensation can be tuned (e.g. look-up tables can be formed). Due to the common coupling of the phases this simplified voltage compensation leads eventually to sub-optimal interleaving and a violation of the intended operation of the hysteretic controller (i.e. violation of the set current boundaries). Among other reasons, this is another motivation of using a hybrid controller instead of a simple time compensated adaptive hysteretic, and shifting to the PI mode once steady state is established.

d. Control Algorithm

The flowchart of the proposed adaptive hybrid controller is shown in Figure 4.8, where the states of the supervising state machine and the step-by-step operation of the average mode as well as the adaptive

[9] usually an estimation/measurement is available.

[10] eventually a more precise implementation would require a more powerful control platform.

hysteretic mode are given. When the system is at steady state the supervisor of each module checks the mode-shifting conditions a)-c) (same for all modules) [48].

a. $|I^*[k] - I^*[k-1]| \leq \Delta I^*$

b. $|i_\mathrm{L} - I^*| \leq \Delta I_\mathrm{thr}$

c. $|dv_\mathrm{c}| \leq \Delta V_\mathrm{thr}$

If one of these conditions is violated, the supervisors change their output signal $S_\mathrm{h,i}$ from 0 to 1 and all the modules enter the hysteretic mode simultaneously.

Condition a) checks the reference current which is a known input for the controller. The knowledge of the reference current helps in distinguishing between step transients with sufficient amplitude, that require the use of the hysteretic mode and slower transients that can be handled by the PI mode, and therefore do not result in temporary loss of the interleaved operation. ΔI^* is chosen according to the needs of the application.

Conditions b) & c) check the output converter current i_con and the weighted voltage derivative dv_c, that is defined in (4.36), in order to detect a possible violation of the thresholds ΔI_thr and ΔV_thr, which could be caused by load disturbances. The threshold I_thr acts as a natural protection limit for the system as it ensures that the converter does not trip due to over-current. Additionally, by monitoring the change of the output voltage, the control system can detect load disturbances faster, especially when a low output capacitance C_out is used (e.g. current source applications), as also highlighted in [48]. Since the voltage derivative can be sensitive to noise, the weighted voltage derivative acting as a low pass filter, is used.

$$dv_\mathrm{c}[k] = 0.5dv_\mathrm{c}[k-1] + 0.5(v_\mathrm{c}[k] - v_\mathrm{c}[k-1]) \tag{4.36}$$

The fine tuning of the thresholds ΔI_thr and ΔV_thr depends on the requirements of the application. These conditions offer a superior disturbance rejection capability when large signal disturbances occur (e.g. sudden change of load). For applications where large signal disturbances at steady state are not expected, these conditions are not needed.

When the control system is in adaptive hysteretic mode, the supervisor of each module checks the mode-shifting conditions i)-iii):

i. $i_{\mathrm{L,i}} = i_{\mathrm{L,min}} = I^* - H$

ii. $N_{\mathrm{cycles}} \geq 2$

iii. $|dv_{\mathrm{c}}| < \Delta V_{\mathrm{thr}}$

If all of these conditions are met, the supervisors change their output signal $S_{\mathrm{h,i}}$ from 1 to 0, so that the average current mode is activated again and the integral part of the controller along with the PWM clock are reset. In contrast to the previous case, each module's supervisor changes its output signal $S_{\mathrm{h,i}}$ at a different time instant, as can be seen in Figure 4.7 too.

Condition i) ensures that the mode-shifting happens at the start of a new switching cycle and the saw-tooth shaped PWM counter is reset (Figure 4.7e). In this way, the duty cycle of the PI controller is immediately applied, turning on $S_{\mathrm{i,1}}$ resulting in an increasing $i_{\mathrm{L,i}}$. Moreover, condition ii) checks the number of hysteretic cycles of the module. As shown in Figure 4.8 the adaptation of the hysteretic band occurs when $N_{\mathrm{cycles}} = 1$. Therefore, this condition ensures that the adaptation has occurred before a mode-shift happens, so the phase-shift of the module currents is near-optimal before the controller shifts to the PI mode. Finally, condition iii) ensures that the output voltage has settled before the mode can be changed. The control output of the average mode is almost at its steady state value and only small adaptations are needed. For highly dynamic sources with low output capacitors C_{out} this condition is essentially always fulfilled when conditions i) & ii) are fulfilled, but it is included here for completeness.

The full schematic of the controller with the detailed feedback loop is shown in Figure 4.9. To evaluate the performance of the adaptive hybrid controller in the following study, its algorithm is simulated. It should be noted that the band calculation block and the hysteretic modulator (Figure 4.9) do not result in additional loop delays but they require a relatively high performing control platform to perform the needed calculations in time. In the case of the adaptive hybrid controller the optimization procedure of Section 4.2 simply optimizes the PI controller as described in Section 4.1.1.

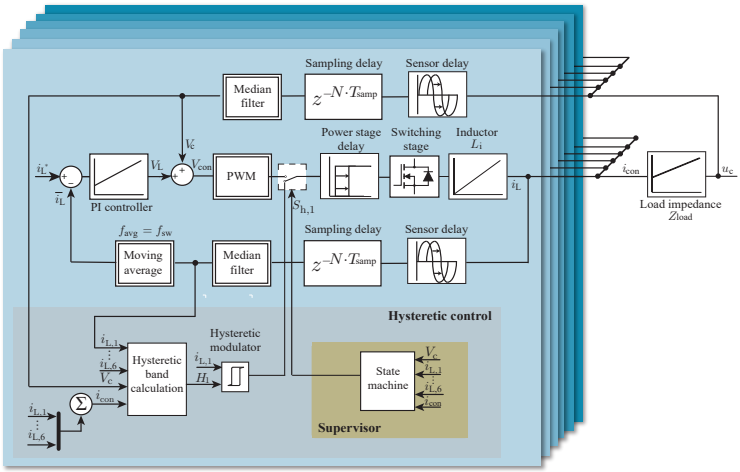

Figure 4.9: Schematic of the hybrid controller designed specifically for the 6-phase interleaved converter system.

4.2 Controller Optimization

In this section each of the previously presented controllers is optimized in a systematic way based on the performance evaluation indicators, defined in Section 4.2.1. Furthermore, based on these indicators the ideal system performance is defined and the physical limits of the system are explained in Section 4.2.2. Finally in Section 4.2.3, a general optimization procedure is shown, and the choice of a suitable cost function that needs to be minimized is discussed.

4.2.1 Performance Evaluation Indicators

To evaluate the performance of the controller, the following indicators are defined and are graphically depicted in Figure 4.10.

- Overshoot constraint: The peak of the converter current $i_{\mathrm{con,max}}$ should be lower than a pre-defined percentage Q of the commanded reference I^*_{con}. This acts as a constraint in the optimization procedure that follows, and the solutions that do not fulfill this requirement are simply discarded.

$$Q = \frac{I^*_{\text{con}} - i_{\text{con,max}}}{I^*_{\text{con}}} \tag{4.37}$$

- Switching frequency constraint: When the sampling frequency is higher than the switching frequency and the update rate of the duty ratio is also higher than the switching frequency, the converter modules might switch with a frequency higher than the intended one. In order to protect the switches from overheating and ensure that the semiconductors remain within their safe operating area, a maximum average switching frequency within a defined time window $\bar{f}^{\max}_{\text{window}}$, needs to be set. The average switching frequency $\bar{f}_{\text{window}}$ is then calculated as in (4.38), where N is given by (4.39), and $p[k]$ is 1 if a rising edge is detected for switch $S_{1,\text{i}}$ (Figure 4.1) and 0 otherwise.

$$\bar{f}_{\text{window}} = \left(\frac{1}{N} \cdot \sum_{k=1}^{N} p[k] \right) \cdot \frac{1}{T_{\text{samp}}} \tag{4.38}$$

$$N = \frac{t_{\text{window}}}{T_{\text{samp}}} \tag{4.39}$$

In (4.39), t_{window} is the time window within which the average switching frequency $\bar{f}_{\text{window}}$ is evaluated and it is a designer's

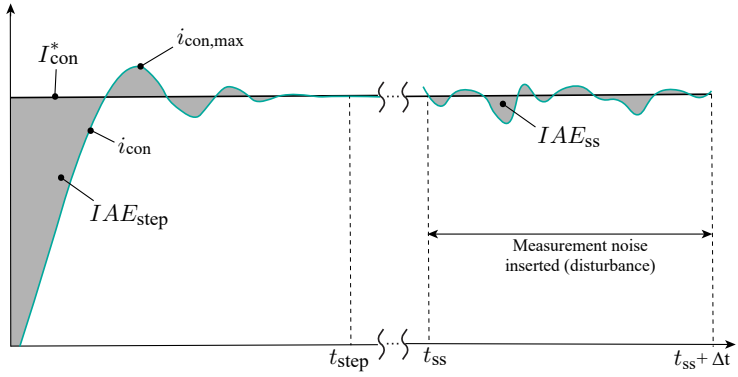

Figure 4.10: Graphical representation of the performance evaluation indicators.

choice, that depends on the thermal limits of the semiconductor devices. For example in this work a t_{window} of 0.5ms is used and a maximum average switching frequency $\bar{f}^{\max}_{\text{window}}$ is 10% higher than the intended switching frequency (66kHz).

- Transient Performance: The transient performance is evaluated based on the integral absolute error (IAE_{step}) of the total converter current i_{con}. During the optimization procedure for consistency reasons the IAE_{step} is always evaluated through the same simulation model, till a selected time t_{step}. The IAE_{step} is defined then as in (4.40).

$$IAE_{\text{step}} = \int_0^{t_{\text{step}}} |I^*_{\text{con}} - i_{\text{con}}(t)| \; dt \; [\text{A} \cdot \text{s}] \tag{4.40}$$

- Steady State Performance: The steady state performance and the disturbance rejection of the controller are evaluated based on the integral absolute error (IAE_{ss}) of the total converter current i_{con} for a specified duration Δt_{ss} after the steady state is achieved (t_{ss}), as defined in (4.41), under the presence of measurement noise.

$$IAE_{\text{ss}} = \int_{t_{\text{ss}}}^{t_{\text{ss}}+\Delta t_{\text{ss}}} |I^*_{\text{con}} - i_{\text{con}}(t)| \; dt \; [\text{A} \cdot \text{s}] \tag{4.41}$$

The time duration Δt_{ss} is chosen appropriately in order to study the impact of the low frequency harmonics that are induced in the controlled currents due to actions of the closed loop control system. Clearly Δt_{ss} depends then on the studied system and the control requirements. For example for the studied system, a $\Delta t_{\text{ss}} = 1$ms has been chosen, in order to study the effect of sub-harmonic content down to 1kHz.

In high power electronic systems like the prototype system of Figure 4.1, measurement noise may arise for a variety of reasons[11]. For this study a realistic noise model has been constructed based on measurements performed on the prototype boards presented in section 3.7.2. The noise model for the current measurements $i_{\text{L,i}}$ is assumed to follow a Gaussian distribution with a mean value of

[11] e.g. switching actions of the power stage, ripple of the reference voltage of the analog measurement circuitry, etc.

0A and a variance of 1A, as noted in (4.42). Similarly, the voltage measurement v_c is assumed to follow a Gaussian distribution with a mean value of 0A and a variance of 1V, as in (4.43).

$$i_{\text{noise}} \sim \mathcal{N}(0,\, 1) \qquad (4.42) \qquad v_{\text{noise}} \sim \mathcal{N}(0,\, 1) \qquad (4.43)$$

It is worth mentioning that the noise model is a random variable and in order to compare the results of different simulations, the same seed is used in the random number generator which produces the random noise. Therefore the same random numbers are generated in every simulation and a comparison is possible. Furthermore, as a worst case scenario the same seed is used for the random noise of all $i_{\text{L,i}}$ measurements.

4.2.2 Ideal System Performance

Based on the described performance evaluation indicators, the ideal control performance can be derived. The ideal controller is defined in this study as the controller that has its performance limited only be the physical constraints of the converter system. In the case of the transient performance, the ideal controller has a zero overshoot ($Q = 0$) and IAE_{step} is limited only by the control loop's plant (practically the switching stage and module inductor L_{i}). Similarly, the minimum IAE_{ss} is only limited by the ripple of the total converter current i_{con} in the considered operation point. In other words, the ideal controller is able to reject the disturbances introduced by the noise sources of the measurements and achieve a flattop accuracy that is only limited by the unavoidable switching ripple. Based on these considerations the reference transient evaluation indicator IAE^*_{step} as well as the steady state one IAE^*_{ss} can be calculated. These serve as normalization factors in the optimization procedure that follows.

4.2.3 Optimization Procedure

Figure 4.11 shows the optimization procedure that is followed for the identification of the optimal gains of the described control structures. The procedure is the same for every control structure and the only difference lies on the gains that need to be identified. More specifically for the PI controllers the aim is to extract the K_{p} and K_{i} parameters, while for the state feedback controller the weight inputs to the LQR

method w_i, w_v, w_load, w_int and w_R need to be identified. Likewise the aim of the optimization of the MPC essentially involves the extraction of the optimum K_i, that is used once the reference is almost achieved and essentially determines the IAE_ss performance of the controller[12].

Initially a discrete search grid for the gains is defined along with the overshoot constraint Q_max, which is usually given by the specifications of the system, and the maximum average switching frequency constraint $\bar{f}^\mathrm{max}_\mathrm{window}$ which is given by the hardware design limitations of the system. Furthermore, the performance of the ideal controller can be calculated based on the physical limitations of the studied system and the ideal performance evaluation indicators IAE^*_step and IAE^*_ss can be calculated for the intended operation point.

Next, the cost function that needs to be minimized is defined. The considered cost function takes the form given in (4.44).

$$f(IAE_\mathrm{step}, IAE_\mathrm{ss}) = w_\mathrm{step} \cdot \frac{IAE_\mathrm{step}}{IAE^*_\mathrm{step}} + w_\mathrm{ss} \cdot \frac{IAE_\mathrm{ss}}{IAE^*_\mathrm{ss}} \tag{4.44}$$

In (4.44), IAE^*_step and IAE^*_ss are used as normalization factors and the design weights w_step and w_ss can be chosen according to the controller design goals of the application. For the present study equal weight factors ($w_\mathrm{step} = w_\mathrm{ss} = 0.5$) are chosen for the transient and the steady state performance.

Thereafter, the algorithm iterates through the different controller designs by choosing gain combinations and executing the appropriate models/simulations. At first, the step transient simulation is executed and the resulting overshoot is checked against the maximum overshoot requirement, which acts as a design constraint. If the overshoot is higher than the maximum allowable overshoot, new gains are chosen and a new simulation is executed. If the overshoot is within the allowable limits, the algorithm goes on and executes the steady state simulation, where the noise models for the current and voltage measurements are inserted, as previously described. The algorithm then calculates the average switching frequency $\bar{f}_\mathrm{window}$, based on (4.38) and checks if the $\bar{f}^\mathrm{max}_\mathrm{window}$ constraint is violated. If it is violated, a new controller design is chosen and the procedure is repeated.

Afterwards, the performance indicator factors IAE_step and IAE_ss as well as the respective cost function can be calculated based on (4.40),

[12] in MPC K_i affects also IAE_step but to a lesser extent.

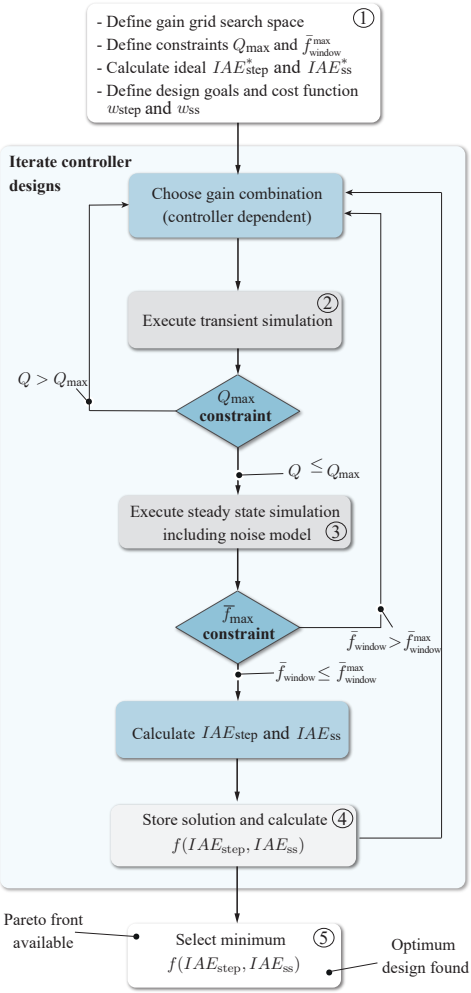

Figure 4.11: Flowchart of the general optimization procedure suitable for every controller scheme.The gain combination needs to be selected at the beginning of each iteration and depends on the control scheme.

(4.41) and (4.44). The solution is then stored and the algorithm chooses a new controller design point and repeats the described procedure. Fi-

nally after all the described steps have been executed for all the gain combinations, the algorithm chooses the optimum point which corresponds to the controller design that results in the minimum value for the cost function $f(IAE_{\text{step}}, IAE_{\text{ss}})$.

4.3 Comparative Evaluation: Simulations

The current shaping converter system shown in Figure 4.1 has been used as a test-bench together with the optimization routine that was previously described, to assess the performance of the five presented control schemes. In Figure 4.12 the investigated controller designs are plotted for each control structure. More specifically the performance ratio pairs $IAE^*_{\text{step}}/IAE_{\text{step}}$ and $IAE^*_{\text{ss}}/IAE_{\text{ss}}$ for each controller design are depicted. It has to be pointed out, that the ideal controller is the one which achieves a performance ratio pair of (1,1). Furthermore, the resulting Pareto-front is also highlighted with red for each controller structure and the chosen optimum design point is highlighted with the star symbol. The transient and steady state response with the inserted noise for the chosen optimum design are also shown in Figure 4.12.

Initially, the PI with a single update per period can be compared to the PI with fast update rate. Based on the extracted Pareto fronts it can be seen that the PI with fast update rate results in both a faster transient response (i.e. higher $IAE^*_{\text{step}}/IAE_{\text{step}}$) as well as a slightly better steady state performance (i.e. higher $IAE^*_{\text{ss}}/IAE_{\text{ss}}$). This is an immediate result of the fact that when a faster update rate is used a more aggressive implementation of the controller is possible (i.e. higher control gains) without violating the overshoot constraint. Furthermore, the switching power stage is allowed to switch multiple times per switching period leading to a lower delay of the modulator, and a faster response, which is especially beneficial for large signal transients.

Based on the above, one of the initial major findings of this study is that a high sampling frequency combined with a faster execution rate can lead to a PI control implementation with a significantly better performance in step transients. In this study the optimum chosen point for an update rate that is 16 times faster than the switching frequency results in a 18% increase of the transient performance, and an 11% increase of the steady state performance compared to the benchmark implementation. As already mentioned one downside of the faster update rate is the need to allow for a possible temporary increase of the

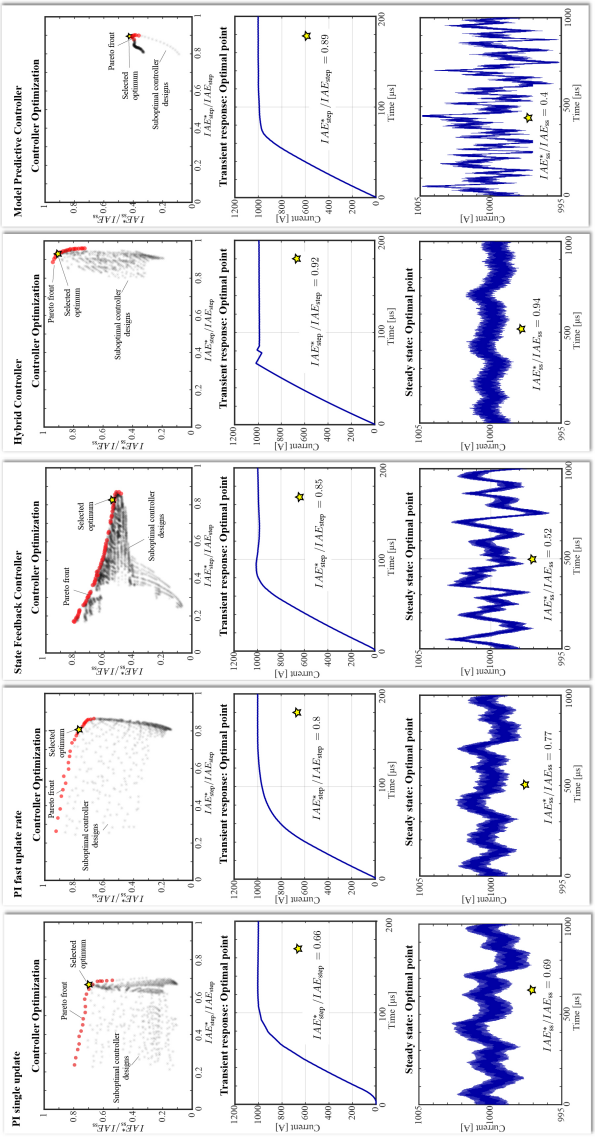

Figure 4.12: Results of the optimization procedure for all the control structures. For each control structure all the investigated controller designs are plotted based on their performance pairs ($IAE^*_{\text{step}}/IAE_{\text{step}}$, $IAE^*_{\text{ss}}/IAE_{\text{ss}}$). The closer the pair is to the ideal pair (1,1), the better the performance of the controller. The Pareto-front for each of the investigated structures is highlighted in red.

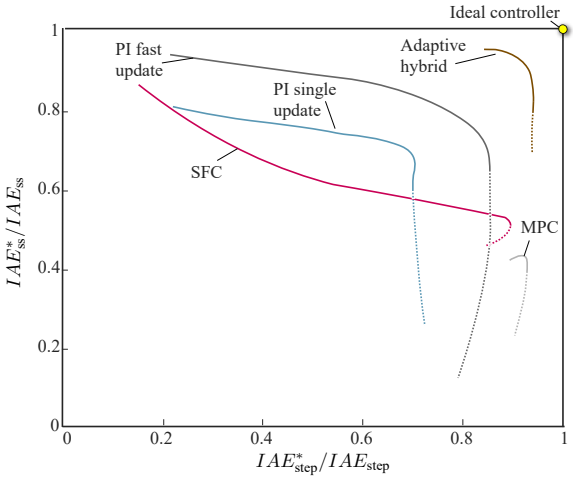

Figure 4.13: Comparison of the resulting Pareto fronts of the investigated controllers for step transients followed by a flattop.

switching frequency (explained in Section 4.2.3), as well as the need for a high performing control platform that can execute the needed calculations in each sampling step. Nevertheless due to this finding, the state feedback controller and the hybrid controller are studied only for the case of fast update rates in the upcoming results.

Regarding the state feedback controller, it can be observed that the selected optimum point has a higher transient performance compared to the PI structure, and in general the maximum transient performance that can be achieved is higher, as design points with a transient performance ratio of up to 0.9 can be reached. However, the steady state performance of the controller is significantly worse. This can be attributed to the feedback of the total converter current $i_{\mathrm{con,obs}}$ which in this case contains the added noise of all the individual current measurements $i_{\mathrm{L,i}}$. Less aggressive designs (with a lower w_{icon}) can achieve a more satisfactory steady state performance ratio (up to approximately 0.8 in Figure 4.12), but the transient response is then severely compromised. All in all it can be concluded that at the presence of measurement noise the trade-off between steady state and transient performance achievable with the state feedback controller is inferior to the trade-off achievable with a PI structure, as long as the implementation of the SFC does not

include a compensation/model of the relevant time delays, or additional conditioning of the measured values.

Regarding the adaptive hybrid controller, it offers as expected the best transient performance, which is also near the optimal for step references. In fact the increased ripple and overshoot due to the hysteretic modulation strategy and the need to return to interleaving, is the reason that the response is not time optimal (transient ratio $IAE^*_{\text{step}}/IAE_{\text{step}}$ is below 1). The use of the hysteretic controller during step transients, allows for a less aggressive controller design for steady state, leading to a high performance at flattop too. As will be shown later, this less aggressive control design has a detrimental effect on the control performance when the reference current is not a step, and the PI mode (with low gains) of the adaptive hybrid controller is used throughout the transient [49].

Regarding the MPC, its transient performance is almost as good as the achieved performance of the adaptive hybrid controller. As expected the gain of the offset integrator does not play a big role in the ratio $IAE^*_{\text{step}}/IAE_{\text{step}}$, as it is not enabled until the converter current is close to the reference. Therefore, all the studied controller designs have a similar transient performance indicator. Interestingly, the MPC implementation suffers from pronounced ripple at flattop in the presence of noise, exhibiting by far the worst performance among the investigated schemes. The result suggests that the presence of noise in the measurements has a particularly detrimental effect on the reference tracking performance of the MPC.

Figure 4.14 shows the transient performance of the optimized controllers in a single comparative graph, and Table 4.2 summarizes the performance evaluation indicators of the investigated controllers, operating under the conditions used during the optimization.

Table 4.3 gives a more complete overview of the comparative performance of the optimized control structures for different operating scenarios. In Table 4.3 the IAE performance indicator of the benchmark case (i.e. the PI with single update) is divided by the IAE performance of the respective controller. As a result a ratio higher than one corresponds to a higher performance compared to the benchmark case. Since the PI with single update is the benchmark, all case-scenarios exhibit a performance ratio of 1. Five different case-scenarios are simulated:

- **Case 1:** 1kA amplitude sine wave reference with 100Hz frequency and a resistive load of 0.2Ω.

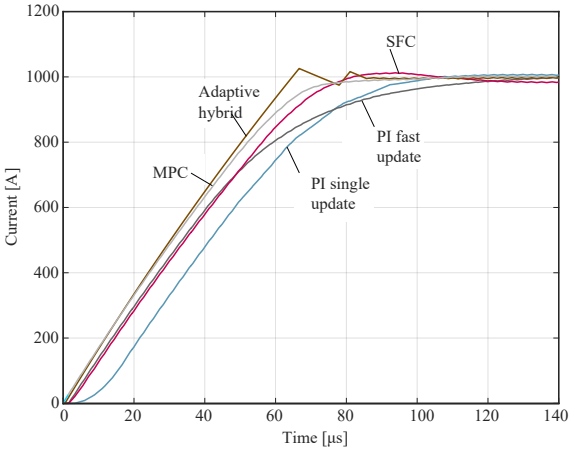

Figure 4.14: Comparative simulations depicting the transient response of the chosen optimal designs for each control structure following a step current. **PI with single update:** light blue, **PI with fast update rate:** dark gray, **SFC:** red, **Adaptive hybrid controller:** brown, **MPC:** light gray.

Table 4.2: Performance summary of optimized control structures, for the operating conditions used during the optimization procedure.

Controller	$\frac{IAE^*_{\text{step}}}{IAE_{\text{step}}}$	$\frac{IAE^*_{\text{ss}}}{IAE_{\text{ss}}}$	$Q_{\max}$
PI single update	0.66	0.69	0.7%
PI fast update	0.8	0.77	0.15%
SFC	0.85	0.52	1.25%
Adaptive hybrid controller	0.92	0.94	2%
MPC	0.89	0.41	0.36%

- **Case 2:** 1kA amplitude sine wave reference with 400Hz frequency and a resistive load of 0.2Ω.
- **Case 3:** 1kA amplitude step response with a resistive load of 0.3Ω.
- **Case 4:** 1kA amplitude step response with a resistive load of 0.4Ω.

Table 4.3: Evaluation of performance of the optimized controllers for different operating case-scenarios.

Controller	Case 1	Case 2	Case 3	Case 4	Case 5
PI single update	1	1	1	1	1
PI fast update	1.19	1.28	1.16	1.1	1.3
SFC	1.16	1.16	0.89	0.62	1.41
Adaptive hybrid	0.49	0.45	1.29	1.28	0.49
MPC	2.19	2.20	1.19	1.15	1.9

- **Case 5:** 1kA triangular waveform with 800Hz frequency and a resistive load of 0.2Ω.

In all simulations the noise models described in (4.42)-(4.43) are included too. In case scenarios 1, 2 and 5, the adaptive hybrid controller uses its average control mode (PI with fast update rate), since the hysteretic controller is not enabled for non-step transients. The performance difference compared to the PI with fast update arises from the different optimized gains. The less aggressive gains used for the hybrid controller to achieve a good steady state performance, have a detrimental effect on its performance following sinusoidal references. It can be also seen that the adaptive hybrid provides as expected the best performance in the scenarios following a step reference current.

Furthermore, the PI with a fast update rate is consistently notably better than the benchmark case by more than 10%, and its performance edge is not significantly influenced by the change of operating conditions. On the other hand, the SFC, shows a higher performance compared to the benchmark in following sinusoidal waveforms, but its performance for changing operating conditions in step references is severely affected. In case 4 in particular where the resistance of the load is doubled compared to the optimized case, the SFC shows 38% lower performance rating compared to the benchmark controller, indicating that new gains have to be found and the controller needs to be re-tuned.

More importantly, the MPC shows its performance benefits when following non-step references, where it is by far the best choice. Moreover, its performance in step transients does not seem to be affected by load changes. Overall the analysis indicates that the MPC is the better

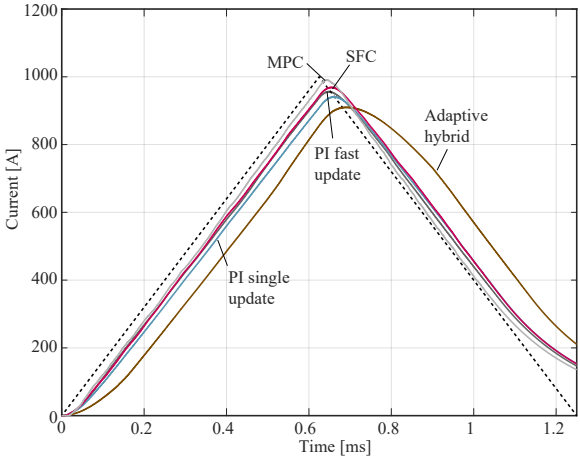

Figure 4.15: Comparative simulations depicting the transient response of the chosen optimal designs for each control structure following triangular reference current (case scenario 5). **PI with single update:** light blue, **PI with fast update rate:** dark gray, **SFC:** red, **Adaptive hybrid controller:** brown, **MPC:** light gray.

choice for following arbitrary references with different loads, among the different investigated schemes. However, its poor performance during flattop make it a rather sub-optimal choice for step transients where high flattop accuracy is required.

Case scenario 5 simulates a triangular reference current with a frequency of 800Hz and an amplitude of 1kA through the nominal for the study load of 0.2Ω. This corresponds to a current gradient of approximately 1.6A/μs which is challenging for the converter during step down due to the low control margin when the voltage is close to 0V, as can also be seen in Figure 4.15. It can be remarked that the controllers demonstrate a big difference in their performance compared to the benchmark case demonstrating in practice their comparative bandwidth. Once again the best performer is the MPC followed by the SFC and the PI with the fast update rate. It is observed that simply executing the PI controller faster results in a 30% improvement compared to the benchmark case. Furthermore, the conservatively tuned PI controller of the adaptive hybrid controller, which was the reason behind its high flattop stability performance in step references, shows again a

poor performance following non-step transients. The comparative performance of the investigated controllers to case scenario 5 is also shown in Figure 4.15.

4.4 Comparative Evaluation: Measurements

In order to validate the findings of the simulations, the most promising controllers have been developed and tested on the prototype high power 6-phase interleaved current shaping converter of the DynACuSo, presented in Chapter 3.

As described in Section 3.7.2, each converter buck module is equipped with a current measurement board that apart from the current sensor, features also an on-board CPLD to communicate with the local ADC. The current sensor IC is a high bandwidth (DC-500kHz) measurement, followed by an analog stage to reduce the switching noise and condition the signal to an appropriate range, so that it can be converted with high resolution by the ADC (approx. 100mA per LSB) [98]. The current/voltage measurements of all the modules are firstly sampled and collected locally on the CPLD, and they are then communicated with a serial communication protocol through the USB type-C type connections shown in Figure 3.36, to the master controller. This technique results in a higher communication delay time, but ensures that a low

Table 4.4: Parameters of the experimental measurements.

Quantity	**Symbol**	**Value**
Upper DC-link capacitor voltage	V_1	600V
Lower DC-link capacitor voltage	V_2	50V
Module inductance	L_i	240µH
Output capacitance	C_out	3µF
Damping resistance	R_ss	5Ω
Module switching frequency	f_sw	60.096kHz
Current/Voltage sampling frequency	f_sample	960kHz
FPGA main clock frequency	f_FPGA	100MHz
Load resistance	R_load	0.2Ω
Load inductance (estimated)	L_load	5µH

cable count and higher signal integrity is achieved. Furthermore, the communication link is operated with a 60MHz clock and results in a total sampling frequency of 0.96MSps, which corresponds to approximately 16 samples per switching period[13]. This allows the implementation of controllers with a faster execution rate, as previously described. The master controller comprises an Altera Cyclone IV FPGA with 115k logic element units, to provide a design flexibility and the ability to fit high performing controller designs. The controller samples all the measurements with the same clock, synchronizes them, and controls the modules by providing the gate signals through the appropriate interfaces (also visible in Figure 3.36).

Like-wise the voltage measurements take place in a separate PCB, they are stored locally on a CPLD, and they are communicated serially to the master controller, where they are conditioned and synchronized. The output voltage measurement comprises a compensated RC voltage divider followed by an active filter stage with a 400kHz bandwidth, and runs with a 0.96MSps sampling frequency. The measurements that follow use the parameters listed in Table 4.4. The parameters of the controllers are the result of the described optimization analysis, since the feedback loop and the system plant are identical to the ones used in the simulations. The total input DC link voltage is set to 650V, and the maximum output current used is 400A, in order for it to be within the measurement range of a commercial 500A/DC-2MHz current probe, used to measure the currents [99]. The scope acquisition frequency is set to 2.5GHz.

Figure 4.16 shows the performance of the investigated control structures with a step reference of 400A followed by a flattop. The module currents as well as the total current can be seen during the transient response, and the figure depicts as well a closer look into the flattop performance. All in all the controllers behave as expected by the simulations. The PI with a fast update rate shows a faster response time compared to the benchmark PI implementation as is also pronounced in Figure 4.17, where the transient responses of the different controllers are plotted in a single graph for comparative reasons. Furthermore, the adaptive hybrid controller shows the best transient performance and manages to return to steady state smoothly, demonstrating a small ripple due to the loss of interleaving in the first cycles after the transient.

[13] 16 samples is chosen as to simplify the design of the moving average filters and reduce the implementation effort on the FPGA side.

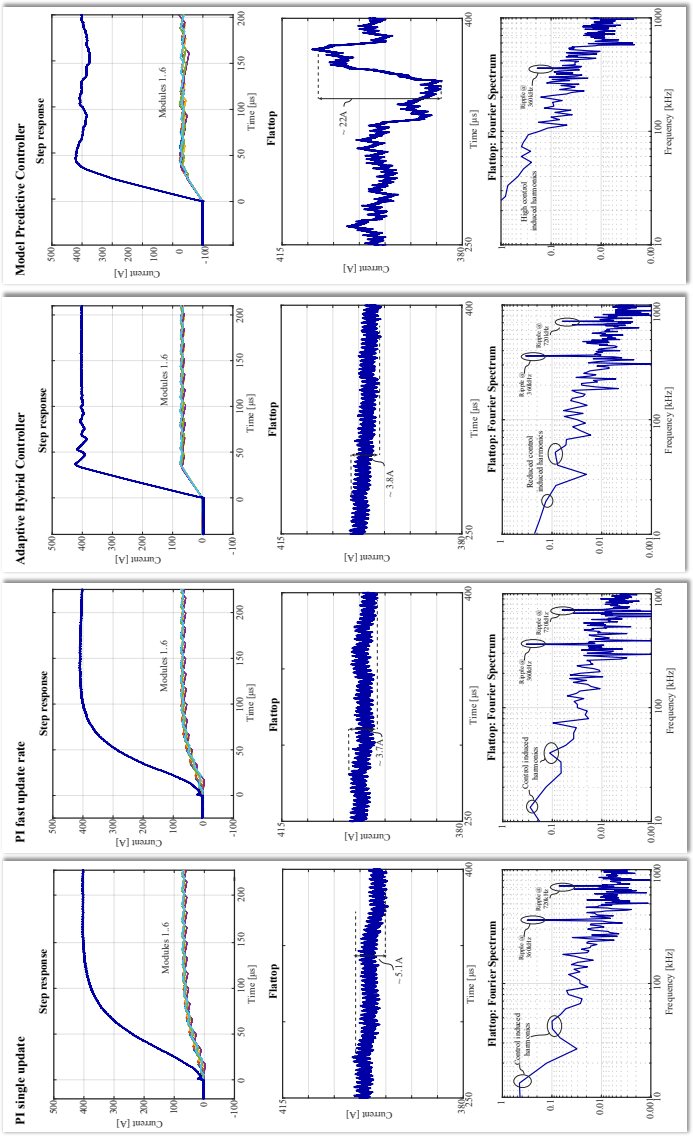

Figure 4.16: Experimental results of 400A step response transient obtained with the current shaping converter of the DynACuSo and the different investigated control structures. The parameters of the experiments are shown in Table 4.4.

Optimal interleaving in this case is achieved one switching cycle later than in the simulated case (Figure 4.12). The MPC shows also excellent transient performance, which is near time-optimal too, but results in an increased ripple around the reference point, caused by the noise of the current measurements.

At this point it should be highlighted, that the step response of Figure 4.17 cannot be directly compared to the simulated one shown in Figure 4.14 due to the difference in the reference current amplitude. The different reference current is also the reason behind the slower response of the two PI control schemes (compared to the response achieved in Figure 4.14), as their duty ratio at the beginning of the transient is significantly lower than 1, resulting in a much slower response compared to the adaptive hybrid and the MPC schemes, where a near optimal response is achieved regardless of the reference current. It should also be clarified that in the experimental implementation the PI controllers have a start-up phase at the beginning of the transient, that lasts for one switching period.

In Figure 4.17 it can also be seen that the adaptive hybrid controller, reaches the reference only slightly faster than the MPC, since both appear to be near time-optimal, and results in a similar current overshoot. However, due to the sub-optimal interleaving when operating in the hysteretic mode and the non-ideal measurements, the increased current ripple persists for a 2 additional switching periods, while the adaptations during the hysteretic mode reduce but do not eliminate the current ripple. This causes extra disturbance that was not visible in the simulations. Nevertheless, once the hysteretic mode is disabled the controller returns to PI mode and the phase-shifting controller ensures optimal interleaving soon after the transition. More experimental results with the adaptive hybrid controller have been demonstrated in Figures 3.38 & Figures 3.39

Regarding the steady state performance, the experimental results show similar tendencies with the outcomes of the conducted analysis. Notably, the MPC suffers from high disturbances that are caused by the noisy current measurements and result in an increased current ripple around the reference point. This behavior is mainly attributed to the fact that the MPC acts on the instantaneous current (result only of the median filter in Figure 4.4) and not on the result of a moving average filter like the rest of the controllers during steady state. The rest of the controllers show a good performance during flattop, that

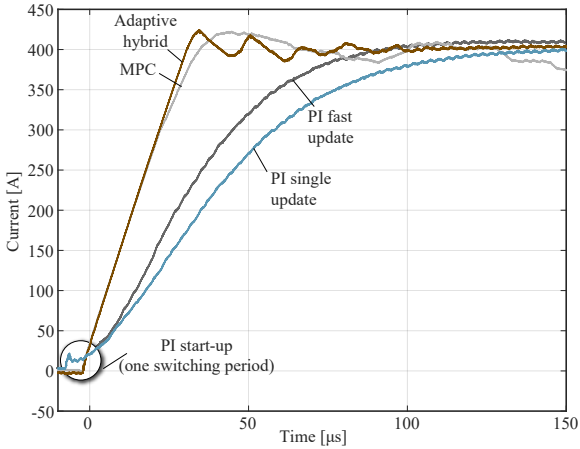

Figure 4.17: Comparative experimental results depicting the 400A step response of the chosen optimal designs for each control structure.

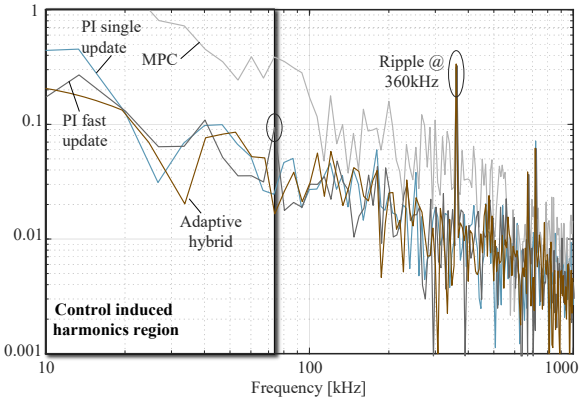

Figure 4.18: Comparative experimental results depicting the resulting Fourier spectrum of the flattop for each control structure.

could be improved if the noise of the current measurement board is further reduced[14]. During the compared 150µs of flattop, the PI with the fast update rate and the adaptive hybrid controller show a total of

[14]this might hinder however their bandwidth.

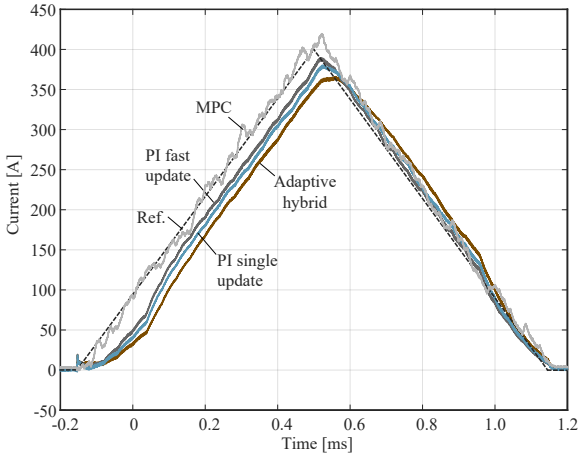

Figure 4.19: Comparative experimental results of the chosen optimal designs following a 400A triangular reference current.

approximately 3.7A of current ripple around the reference point, which is mainly attributed to the offset correction. In fact the adaptive hybrid controller shows reduced low frequency harmonics during the demonstrated operating time interval as can be deduced based on its Fourier spectrum at harmonic frequencies below 60kHz. The converter does not generate sub-harmonics in this region, and therefore the additional current frequencies arise due to the actions of the controller.

Figure 4.18, shows the resulting Fourier spectrum of the flattop for the different control structures in a single graph for comparative reasons. It is observed that the MPC results in the highest current amplitude for low frequency harmonics, and that the adaptive hybrid results in the lowest amplitude for most of the frequencies lower than 60kHz. The 60kHz range is taken as a reference, since harmonics above this frequency could be generated naturally due to sub-optimal interleaving or inductance mismatches between the phases.

Finally, Figure 4.19 shows experimental results with the optimized control schemes following a triangular reference with an amplitude of 400A, and a frequency of approximately 800Hz. The result highlights the superior performance of the MPC in following arbitrary references, as it achieves excellent tracking performance. However, it also leads to the highest ripple among the rest, due to the presence of noise in

the current measurement and its more aggressive nature. It needs to be clarified that the impact of noise is pronounced in the experiments compared to the simulations, as it is not the same for the different phases and occurs at different time instances (mainly induced because of the switching actions which are interleaved). This results in disturbances in the individual duty ratios which cause the converter system to not be optimally interleaved and leads to an increased ripple (ripple currents are added instead of being canceled out). Furthermore, Figure 4.19 highlights once again the advantage of the PI with the fast update rate over the benchmark implementation, and shows that the non-aggressive tuning of the adaptive hybrid controller which resulted in the best steady state performance during a step transient, is insufficient if high tracking accuracy is required.

4.5 Interim Summary

Dynamic controllable sources based on non-isolated interleaved DC-DC converters are a key enabling technology for various modern applications. The system level performance both regarding their transient behavior as well as their steady state can be greatly improved by employing an appropriate control strategy, that fits the needs of each particular application. In this work a rather exhaustive study has been conducted on various current control schemes for such systems.

Initially, the feedback control loop and its non-ideal components (including finite bandwidths, delays and filters) have been modeled in detail providing a common platform for a fair simulation-based investigation. Furthermore, well defined performance evaluation indicators have been proposed in order to allow a fair evaluation of results of the different control schemes not only in transient state but also in steady state. Additionally, a general grid-based brute force optimization routine based on a defined cost function in order to determine the best control gains has been proposed.

A high power 6-phase interleaved buck-type converter has been used as a test-bench for the study, and the simulation-based analysis and subsequent optimization focused specifically on the operation of the system with step transients followed by a constant flattop, including the presence of unavoidable measurement noise, which is especially pronounced in high power dynamic systems. The analysis showed that the adaptive hybrid controller, specifically developed to deliver fast current gradi-

ents in step transients, manages to achieve the best performance. The adaptive hybrid controller has been tested under various conditions in this work (see also Figure 3.38 & 3.39), and has exhibited excellent performance.

Furthermore, the study has revealed that employing a PI controller with a fast update rate can result in a significant increase of the performance of the system at the expense of slightly increased control complexity compared to the benchmark solution. Based on the analysis, the two more advanced control schemes, the LQR-based SFC and the MPC have shown great potential when it comes to their dynamic performance, but did not deliver sufficiently good results at steady state. More specifically the MPC showed a transient performance similar to the adaptive hybrid controller in step transients, but its aggressive nature hindered its ability to handle measurement noise at steady state. The MPC scheme showed also the best performance when following arbitrary/non-step references.

Finally, four of the studied five controllers (excluding the SFC which did not show sufficient potential) have been designed and tested with the current shaping converter of DynACuSo, identical to the one used as a test-bench for the simulation study. The experimental results verified the simulation analysis, showed the great potential of the adaptive hybrid controller in step transients and revealed the shortcomings of the MPC implementation in environments with pronounced measurement noise.

5

Magnified Current Ripple Measurement & Active Ripple Cancellation

Motivation

High-end switching power supplies often require a highly precise, high amplitude pulse-shaped current, while the inevitable superimposed AC current ripple should remain at ultra-low amplitudes. The specifications for these systems are ever-increasing, as they are applied in more and more demanding environments.

More specifically, the AC current ripple is a major indicator of the performance of the power supply system, and in many applications it is strictly specified . In Chapter 3 it was shown that multi-phase interleaved converters are an attractive solution for high-end applications, since they can increase the maximum output current rating while simultaneously providing a superior output ripple performance due to the inherent current ripple cancellation properties of the interleaving concept. However, it has also been shown, that in order to ensure sufficient load ripple attenuation across the entire operating region, an output filter is also required. Furthermore, in Chapter 4 it was shown that significant low frequency components can be generated due to the actions of the closed loop control, enhancing the need for a superior output filter performance.

In general it can be said that in switching power supplies, the current ripple arises as a result of two distinct mechanisms.

- **Switching related current ripple:** The current ripple arises due to the switching actions of the converter. Its harmonic content appears at the switching frequency and integer multiples of the switching frequency. The amplitude of the ripple and frequency spectrum can be analytically derived, as for example shown for an interleaved converter with arbitrary output in Section 3.2. Ideally, in interleaved converters the total output converter current contains only switching harmonics at the effective switching frequency and its integer multiples, which is n times higher than the switching frequency of the individual modules (n signifies the number of phases). However, parameter mismatches can lead to a significant ripple in frequencies starting from the switching frequency of the module and its integer multiples [51].

- **Control related current ripple:** The current ripple arises due to non-idealities of the closed loop that lead to erroneous control actions. The frequencies of those harmonics depend on the control bandwidth (i.e. control gains). Due to their random nature they cannot be simply derived analytically. They may vary from a few hundred Hz up to several kHz. Examples of control related harmonics were shown in Chapter 4, where their effect was pronounced due to the measurement noise that caused a significant additional current ripple.

When the intended output current waveform is pulse-shaped, the rise/fall of the current can be treated separately from the flattop and two distinct operating scenarios arise. With this in mind, Chapter 3 has initially showed the trade-off between transient and steady state performance and a passive adaptive output filter stage (PAF) was proposed to improve the aforementioned trade-off. The PAF output stage made use of two different output filter branches, one that is used during transients and features a high value damping resistance, and one that is used at flattop and features a low value resistance, that ensures a high quality steady state performance.

In this chapter, the option of using an active output filter, in order to improve the ripple attenuation during flattop and further reduce the load current ripple, is investigated. A schematic of the proposed active adaptive filter (AAF) concept is shown in Figure 5.1, where the passive resistance of the PAF is replaced by an active filter branch. Active filters have already been successfully utilized in the literature before,

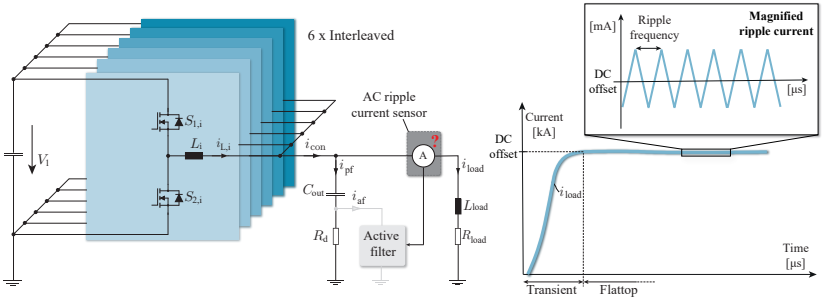

Figure 5.1: Schematic of a multi-phase interleaved buck converter, with an active filter connected at its output. An exemplary pulsed-current waveform with high DC amplitude and low AC current ripple is shown too.

as an alternative to using a high number of passive components. The importance of such filters in fulfilling high attenuation requirements has been demonstrated in [132–139].

Nevertheless, in order to achieve a high performance attenuation with the use of an active filter, the reference signal needs to be precise and in the case of interleaved high frequency converters, it also needs to feature a very high bandwidth. In other words, the ripple current of i_{load} needs to be measured with high precision and low (ideally zero) phase-delay. The precise measurement of i_{load} is very challenging and usually expensive current probes are required [140]. These probes need to feature high accuracy and wide bandwidth that often ranges from DC up to hundreds of kHz, at high current magnitudes.

Direct current-current transducers (DCCTs) are the preferred technology for high-end applications since they combine excellent accuracy in the ppm range with a high bandwidth and current ranges up to tens of kAs [141]. Likewise, optical current measurement systems, based on the Faraday effect, can also achieve high bandwidth combined with high accuracy [142]. However, both of these technologies are associated with a high development cost. On the other hand, commercially available current sensing devices, like Hall sensors, Rogowsky coils, shunt resistors and current transformers (CTs) are usually more affordable but present a trade-off between bandwidth, sensitivity and maximum current amplitude range [143]. For example measuring the AC ripple part of the exemplary current given in Figure 5.1 would be impossible with a conventional sensor due to their limited sensitivity.

In order to measure the ripple of i_{load} with high accuracy and high bandwidth, innovation in the CT design is pursued in this work. The main idea behind these investigations is that the CT blocks the DC part of the load current and allows the precise measurement of the high frequency AC, as soon as the flattop is established. To achieve this behavior, a CT with an adaptive frequency response is proposed in this work. In this way, the CT can measure sufficiently low current harmonics without compromising its settling time after the transient (i.e. faster settling time). This leads to a design that can measure pulsed currents even with short flattops.

In the following, a CT model is shortly discussed, the trade-offs in its performance in terms of frequency response and sensitivity are shown, and the parasitic components that govern its performance are identified. Moreover, the choice of parameters for the designed transformer is explained and the design procedure is shown. For improving the transient behavior of the conventional CT, a CT with adaptive burden resistance is proposed. The operational principle of the topology is explained and details about the circuit design are shown. Furthermore, experimental results verify the proposed concept. The second part of the chapter considers the design of the AAF, receiving the output of the CT as a reference. The AAF is activated shortly after the flattop of the pulse is established. The entire output stage is intended to be used autonomously, without any external signals needed for its operation. The AAF uses a high value damping resistance during the transients, just like the PAF concept introduced in Section 3.3. However, during steady state instead of a passive resistance in series to the output capacitor, it features a high bandwidth linear amplifier with relatively high gain. The models of the active filter and the re-defined output loop of the current source are then presented. The designed AAF is compared with the optimized PAF, presented in Chapter 3. Finally, detailed experimental results are used to demonstrate the ability to achieve high attenuation across a wide frequency spectrum.

5.1 Current Ripple Measurement

The current probe that is proposed in this work is based on the operation principle of a current transformer (CT). At first, a simplified model of the CT is presented and the various trade-offs are identified. Detailed models of the CT have been presented in the literature along

with experimental verification [144–147]. The modelling of the CT is shortly revised and the main equations and design trade-offs are given. Moreover, the special design considerations that need to be taken into account to fulfill the requirements of the application are described and a detailed parameter selection procedure is established.

Firstly, a detailed model of the CT is shown in Figure 5.2a. The derivation of the complete transfer function $\underline{Z}(s) = v_\mathrm{b}(s)/i_\mathrm{p}(s)$ does not allow a simple analytical approach for the design procedure due to its complexity. Therefore a simplified approach is typically followed by using a low and a high frequency equivalent model.

a. Low Frequency Model

Figure 5.2b shows the low frequency model of the CT. In this frequency range, the core losses and the parasitic capacitance C_p (usually in tens of pF range) are negligible. The leakage inductance of the secondary winding L_l is usually low compared to the magnetizing inductance and therefore its effect can also be neglected. If $R_\mathrm{b} \gg R_\mathrm{w}$ (which is the case when high sensitivity is required), the winding resistance can also be neglected. The low frequency response is then given by the transfer function in (5.1) and the dominant pole is approximately given by (5.2). The sensitivity is given by (5.3).

$$\underline{Z}_\mathrm{LF}(s) = \frac{v_\mathrm{b}(s)}{i_\mathrm{p}(s)} = \frac{R_\mathrm{b}}{N} \cdot \frac{L_\mathrm{m} \cdot s}{(L_\mathrm{m} + L_\mathrm{l}) \cdot s + (R_\mathrm{w} + R_\mathrm{b})} \tag{5.1}$$

$$f_{\text{-3dB}}^{\mathrm{LF}} \approx \frac{R_\mathrm{b}}{2\pi \cdot L_\mathrm{m}} \tag{5.2}$$

$$S \approx \frac{R_\mathrm{b}}{N}\ [\mathrm{V/A}] \tag{5.3}$$

Figure 5.3b, shows the response of the CT to a pulse current transient and is the result of its low frequency response. When i_p reaches its flattop, the output voltage starts to decrease with a time constant that is associated with $f_{\text{-3dB}}^{\mathrm{LF}}$. The voltage $v_\mathrm{b,rise}$ across the burden resistor of the CT during a rising current input in the time domain is given by (5.4). Voltage $v_\mathrm{b,ss}$ during the flattop of the pulsed current is given by (5.5), where $V_\mathrm{b,max}$ is the voltage across the burden at the end of the rise of the current pulse.

$$v_\mathrm{b,rise}(t) = \frac{L_\mathrm{m}}{N} \cdot \frac{di_\mathrm{p}}{dt} \cdot \left(1 - e^{-2\pi \cdot f_{\text{-3dB}}^{\mathrm{LF}} \cdot t}\right) \tag{5.4}$$

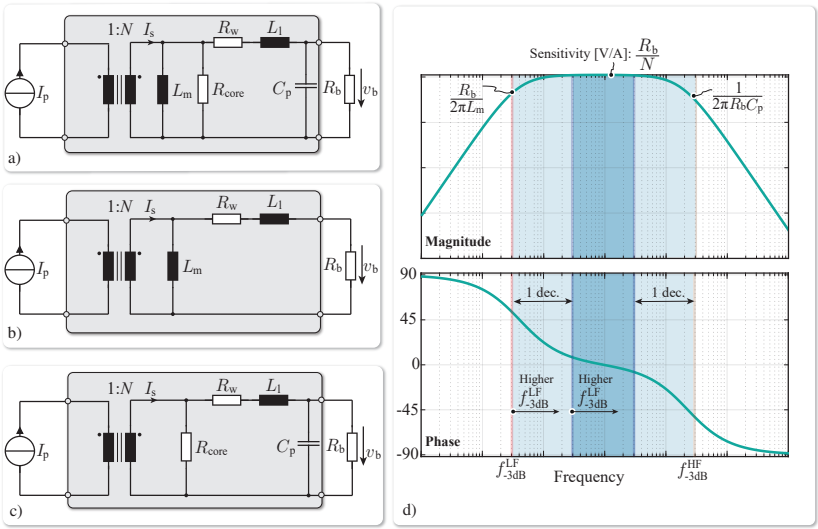

Figure 5.2: a) Conventional CT model. b) Low frequency equivalent model. c) Simplified high frequency equivalent model. d) Simplified frequency response of a CT.

$$v_{b,ss}(t) = V_{b,max} \cdot e^{-2\pi \cdot f^{LF}_{-3dB} \cdot t} \tag{5.5}$$

In most applications, the settling time of the CT is maximized in order to be able to measure lower frequencies, and extend the bandwidth of the current probe. However, in order to characterize and measure the AC current with precision even for pulses with short flattops without the need for post processing the measurement results, the settling time needs to be minimized instead. In other words the CT needs to be operated as a high pass filter, filtering the DC offset of the current and allowing the measurement of only the high frequency current ripple, shortly after the flattop is established. In order to do so, f^{LF}_{-3dB} needs to be increased, as shown in Figure 5.3b. Nevertheless, increasing f^{LF}_{-3dB} causes a decrease in the bandwidth of the CT, since it increases the minimum frequency that can be measured without a magnitude/phase error. Figure 5.2d shows the frequency range that can be measured without a magnitude error (combination of light blue and dark blue region) and the frequency range that can be measured without a phase error (only dark blue region). Clearly, a higher f^{LF}_{-3dB} would shrink these

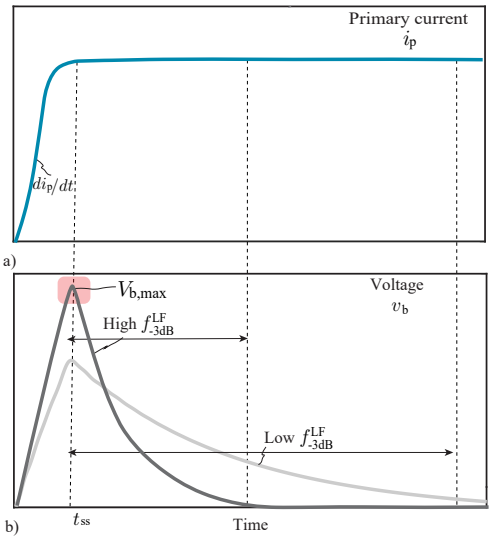

Figure 5.3: Illustration of the time-domain response of a CT to a fast transient (**light gray:** CT with a low f^{LF}_{-3dB}, **dark gray:** CT with high f^{LF}_{-3dB}).

regions and reduce the bandwidth of the current probe.

b. High Frequency Model

Figure 5.2c shows the simplified high frequency model of the CT, where the magnetization inductance is considered to be an open circuit. Furthermore, neglecting the core losses simplifies the analysis and gives a better insight into the operation of the CT. In CTs, the core losses are usually very low due to the low loss core material and especially in the chosen application due to the low amplitude AC current that needs to be measured compared to the needed CT core cross section.

In its simplified form the response of the high frequency range is dominated by the parallel combination of R_b-C_p, as also indicated in [144]. Equation (5.6) gives the transfer function of the equivalent circuit of Figure 5.2c, and (5.7) gives the dominant pole in high frequency ranges.

$$\underline{Z}_{HF}(s) = \frac{v_b(s)}{i_p(s)} = \frac{R_b}{N} \cdot \frac{1}{R_b \cdot C_p \cdot s + 1} \tag{5.6}$$

$$f_{\text{-3dB}}^{\text{HF}} = \frac{1}{2\pi \cdot R_{\text{b}} \cdot C_{\text{p}}} \tag{5.7}$$

Since the burden resistor is chosen based on the needed sensitivity, given in (5.3), it becomes evident that the parasitic capacitor of the secondary winding C_{p} needs to be minimized in order to increase the bandwidth of the CT. However, this simplified model fails to deliver accurate results as the parasitic capacitance and the mutual inductances between the turns of the secondary winding are in fact the defining factors for the high frequency response of the CT.

The equivalent model that corresponds to a more realistic high frequency behavior, taking into account the distribution of the secondary

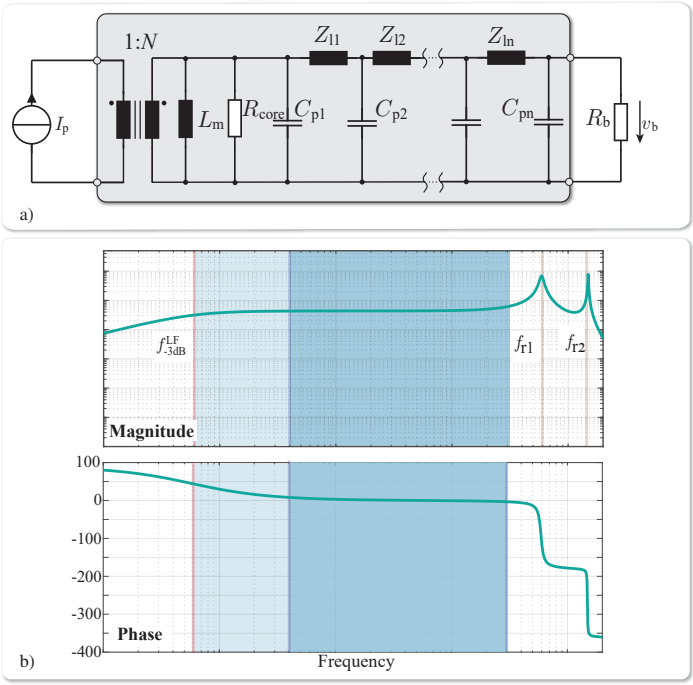

Figure 5.4: a) Detailed model of the CT with a distributed secondary winding. b) Exemplary frequency response of the CT with a distributed secondary model, for better high frequency accuracy.

winding, is shown in Figure 5.4a. Figure 5.4b shows the corresponding frequency response [146]. The distribution of the secondary winding (multiple PI sections connected in series) creates in fact resonance peaks in multiple frequencies, noted as f_{r1}, f_{r2}, in Figure 5.4b. The first resonance peak f_{r1} is defined in this work as the high frequency bandwidth point of the CT f_{-3dB}^{HF}, since it basically determines the high frequency limit of the zero phase, and the zero amplitude error regions of the CT. In fact, these resonance peaks play an important role in the design of the measurement circuit, as they may cause significant disturbance in the measured voltage across the burden resistance. Similar to modelling transmission lines, the more PI sections are included in the model, the more accurate the model becomes. Nevertheless, the complexity increases with the number of PI sections.

Despite the increased accuracy, it is evident that the additional parameters of the model (e.g. Z_{l1}, Z_{l2}, C_{p1}, etc.) complicate the calculations. The analytical derivation of these parameters depend on the geometrical characteristics of the CT and their analytical calculation is considered outside of the scope of this work. It should also be highlighted, that 3D FEM simulations for the derivation of the high frequency response would be extremely time consuming due to the small

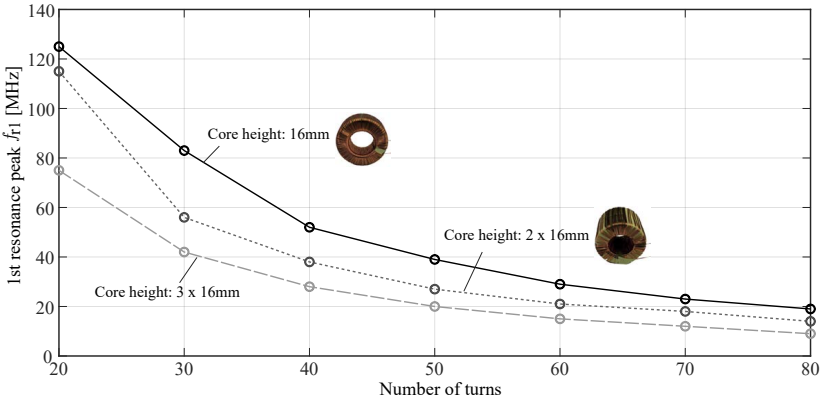

Figure 5.5: Measurements of the first resonance peak f_{r1}, for different number of turns. The measurements are repeated for different core heights, by stacking the cores, and a relation between the total wire length and the first resonance peak f_{r1} is also found. Wire diameter: 0.25mm.

Table 5.1: High sensitivity current probe specifications.

Parameter	Symbol	Value
Max. DC offset	I_{DC}	1000A
Max. ripple current	i_{AC}	$\pm$1A
Ripple frequency range	-	60kHz..360kHz
Low frequency -3dB point	$f^{\mathrm{LF}}_{\text{-3dB}}$	$<$6kHz
High frequency -3dB point	$f^{\mathrm{HF}}_{\text{-3dB}}$	$>$5MHz
Current probe sensitivity	S	$>$0.1V/A

diameter of the secondary winding[1].

On the other hand, experimental measurements of the response of different configurations of the CT can simply be performed with a frequency sweep using an impedance analyzer [148]. Therefore in this work a high frequency model is derived from experimental measurements performed for differently sized cores (i.e. different core heights), and different number of turns. Measurements of the first resonance peak are shown in Figure 5.5, using always the same wire diameter of 0.25mm. It can be seen that the thinner core designs have a significantly higher bandwidth, as the parasitic capacitance is reduced. For example a design with 40 turns and a core height of 16mm shows a bandwidth of 50MHz compared to 25MHz for a design with equal number of turns but a core height of 48mm. Based on these measurements, the first resonance peak as a function of the number of turns and the secondary winding length, can be modeled by properly fitting the experimental measurements.

5.1.1 Parameter Selection

As a test-bench to demonstrate the design procedure and the accompanying parameter selection, a set of specifications for a suitable current probe that can be applied to measure the AC ripple current of the DynACuSo is compiled and shown in Table 5.1. The maximum continuous current is set to be 1kA and the peak-to-peak current ripple $\pm$1A for continuous operation. The frequency range of the ripple current that

[1] usually CTs with a high current range use a thin secondary winding due to the large number of turns. In this work secondary winding with 0.25mm diameter is considered.

needs to be measured is between 60kHz and 360kHz. The 60kHz harmonics arise due to the inductance mismatches, that were discussed in Chapter 3, while the 360kHz is the main effective frequency of the load current ripple, due to interleaving. It needs to be emphasized, that these harmonics are the switching harmonics of the system and sub-harmonic frequencies are also present due to the control action. In order to allow the measurement of sub-harmonic frequencies without amplitude or phase dependencies, the $f_{\text{-3dB}}^{\text{LF}}$ has to be chosen as low as possible. Furthermore, the $f_{\text{-3dB}}^{\text{HF}}$ needs to be significantly higher than the maximum frequency that needs to be measured, not only to allow a better approximation of the real signal, but also to reduce the influence of the described resonant peaks that appear due to the distribution of the secondary winding of the CT.

In order to achieve the specifications listed in Table 5.1, the selection procedure for the design parameters of the CT is shown hereby. The selection procedure is based on equations (5.8)-(5.13), that describe the magnetization inductance, the maximum DC bias of the magnetic flux, the permeability drop due to the DC bias, the inductance L_{l}, the winding resistance R_{w} and the core losses P_{c}. In the following, μ_0 is the permeability of air, μ_r is the relative permeability of the core material, μ_{init} is the initial permeability without DC bias, A_{c} is the core cross section area, l_{e} is the magnetic path length, D_{w} is the winding diameter and l_{w} is the winding length. A_{L} is the permeance in $[\text{nH}/\text{T}^2]$.

$$L_{\text{m}} = \mu_0 \cdot \mu_r \cdot \frac{N^2 \cdot A_{\text{c}}}{l_{\text{e}}} = A_{\text{L}} \cdot N^2 \text{ [nH]} \tag{5.8}$$

$$B_{\text{max}} = \mu_0 \cdot \mu_r \cdot \frac{N_{\text{p}} \cdot i_{\text{p}}}{l_{\text{e}}} \text{ [T]} \tag{5.9}$$

$$\mu_r = \mu_{\text{init}} \cdot \frac{1}{(\alpha_p + \beta_p \cdot H^{c_p})} \tag{5.10}$$

$$L_{\text{l}} = \frac{292 \cdot N^{1.065} \cdot A_{\text{c}}}{l_{\text{e}}} \text{ [µH]} \tag{5.11}$$

$$P_{\text{c}} = \alpha_s \cdot B_{\text{pk}}^{\beta_s} \cdot f^{c_s} \text{ [W]} \tag{5.12}$$

$$R_{\text{w}} = \frac{4 \cdot N \cdot l_{\text{w}}}{\sigma \cdot \pi \cdot D_{\text{w}}^2} \text{ [}\Omega\text{]} \tag{5.13}$$

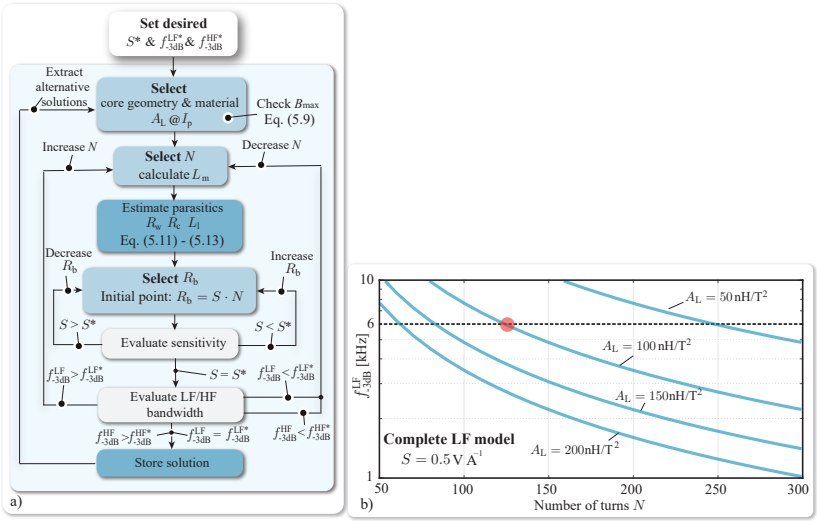

Figure 5.6: a) CT parameter selection procedure. b) Exampled of selection of number of turns N for a given resolution of 0.5V/A, depending on the needed $f_{\text{-3dB}}^{\text{LF*}}$ and the core permeance A_{L}.

Inductance L_{l} is calculated based on the empirical formula (5.11) given by the manufacturer of the iron powder cores that are considered in this work [149]. Similarly, the core losses, which are modeled with an equivalent resistance R_{core} in Figure 5.2a, are calculated based on the basic Steinmetz equation (5.12). Additionally, for the effect of the DC bias, the permeability drop at the maximum current is taken into consideration, as in (5.10). Finally, the AC winding losses (i.e. skin and proximity losses) are not taken into consideration, since they are negligible compared to the DC winding losses. The fitting coefficients (α_p, β_p, c_p, α_s, β_s, c_s) for these models are all extracted from the core manufacturer's datasheet [149].

A general selection procedure for the core geometry, the burden resistance R_{b}, and the number of turns N, is shown on a flow-chart in Figure 5.6. First, the desired sensitivity S^* is selected along with the desired $f_{\text{-3dB}}^{\text{LF*}}$ and the minimum desired $f_{\text{-3dB}}^{\text{HF*}}$. After selecting the core and the material, the procedure checks the maximum DC flux B_{max} based on (5.9), in order to avoid saturation of the core at the maximum operating DC bias current. Then the algorithm iterates N,

starting from a low value. For every N, it calculates the magnetization inductance L_{m} based on (5.8) and estimates the parasitics R_{w}, R_{c}, and L_{l} based on (5.11)-(5.13). Then, it chooses an initial point for R_{b} based on the set S^* and the simplified LF model. Finally, the complete model's response is derived and the real sensitivity S is compared with S^*. If S is lower than S^* then R_{b} is increased accordingly and the LF model is re-evaluated. On the contrary, if S is higher than S^* then R_{b} is decreased. When the needed sensitivity S^* is reached, $f_{\text{-3dB}}^{\mathrm{LF}}$ is calculated and compared with the set reference $f_{\text{-3dB}}^{\mathrm{LF}*}$. If $f_{\text{-3dB}}^{\mathrm{LF}}$ is higher than $f_{\text{-3dB}}^{\mathrm{LF}*}$ then N is increased and the procedure is repeated. If $f_{\text{-3dB}}^{\mathrm{LF}}$ is lower than $f_{\text{-3dB}}^{\mathrm{LF}*}$ then N is decreased. The final solution is stored when the desired $f_{\text{-3dB}}^{\mathrm{LF}}$ and a sufficiently high frequency bandwidth $f_{\text{-3dB}}^{\mathrm{HF}}$ are achieved simultaneously. Thereafter, the algorithm selects a different core from a core library (i.e. different size, material, A_{L}) and repeats the described procedure. It should be noted that multiple alternative solutions exist, depending on the available core permeance, and eventually the core volume.

Regarding the design of the CT, Figure 5.6b can be calculated based

Table 5.2: Main parameters of alternative current transformer designs and estimated performance.

Parameter	**Symbol**	**Design 1**	**Design 2**
Permeance	A_{L}	118nH/T^2	574nH/T^2
Turns	N	120	45
Inner diameter	d_{in}	24mm	25mm
Outer diameter	d_{out}	47mm	58mm
Core height	h_{c}	38mm	32mm
Core material	-	High Flux	High Flux
Sat. flux density	B_{sat}	1.6T	1.6T
Relative permeability	μ_{r}	26	125
Burden resistance	R_{b}	60Ω	7.5Ω
Magnetization inductance	L_{m}	1.7mH	0.467mH
Core volume	Vol	42.6mm^3	57.2mm^3
Low frequency bandwidth	$f_{\text{-3dB}}^{\mathrm{LF}}$	6kHz	2.5kHz
High frequency bandwidth	$f_{\text{-3dB}}^{\mathrm{HF}}$	5MHz	30MHz
Sensitivity	S	0.45V/A	0.15V/A

on the LF model of the CT, showing the $f_{\text{-3dB}}^{\text{LF}}$ as a function of N for different cores and a given desirable $S = 0.5\text{V/A}$. It can be observed that in general the higher the permeance A_{L} of the core, the lower the number of turns needed for a given sensitivity. As shown before, a lower number of turns leads to an increased high frequency bandwidth.

Table 5.2 shows two examples of CT designs and lists their performance parameters for a better understanding of the involved trade-offs. Both designs use iron powder cores (High-Flux [149]) as they provide a high saturation flux density, and low core losses at high frequencies. However, Design 2 uses a material with higher relative permeability, and therefore significantly higher permeance for a similar geometry. It should be emphasized that for the iron powder, the higher permeability results in a higher dependency of the permeability of the material from the DC current bias. Therefore, the L_{m} of Design 2 drops significantly (approx. 20%) for a high bias current (i.e. 1kA) compared to the almost negligible drop of Design 1 (approx. 5%) [149]. This effect has an influence on the measured bandwidth, as $f_{\text{-3dB}}^{\text{LF}}$ increases for decreased relative permeability. The $f_{\text{-3dB}}^{\text{LF}}$ listed in Table 5.2 refers to the maximum $f_{\text{-3dB}}^{\text{LF}}$, assuming the worst case operating point, for maximum DC bias current.

Additionally, it can be noted that Design 1 achieves a high sensitivity of 0.45V/A, three times higher than Design 2 due to the increased ratio R_{b}/N. However, the high frequency bandwidth suffers as the first resonance peak appearing at 5MHz, compared to 27MHz for Design 2 which features a lower number of turns. Additionally, Design 2 has a lower $f_{\text{-3dB}}^{\text{LF}}$, and therefore an increased bandwidth range. Nevertheless, the decreased $f_{\text{-3dB}}^{\text{LF}}$ would result in an increased settling time for the current after the pulse, hindering the ability of the CT to measure the ripple for pulses with a short flattop.

5.1.2 CT with Adaptive Response

Previously, the trade-off between minimum measurable frequency and settling time after a transient was highlighted. In order to allow the CT to return to steady state shortly after the flattop of the pulse is reached and enable sensing the ripple current for pulses with a short flattop, an adaptive topology is presented hereby. The topology allows to use a high $f_{\text{-3dB}}^{\text{LF}}$ during transients, in order for the CT to settle quickly after the transient and a lower $f_{\text{-3dB}}^{\text{LF}}$ during flattop, in order to

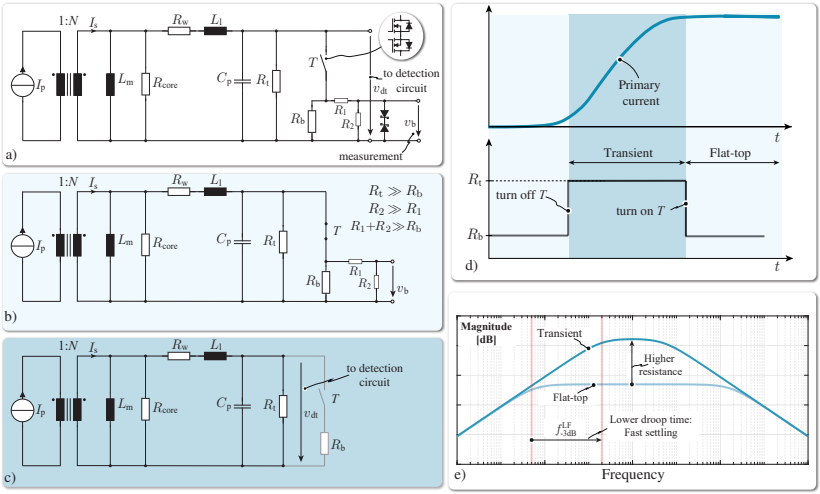

Figure 5.7: a) Proposed topology for decreased settling time. b) Steady state equivalent model. c) Transient equivalent model. d) Operational principle of the proposed CT. e) Frequency response during flattop and during transient.

extend the bandwidth of the current measurement. With this solution, the described parameter selection is simplified, as the $f_{\text{-3dB}}^{\text{LF}}$ does not anymore determine the settling time of the CT. Therefore a lower $f_{\text{-3dB}}^{\text{LF}}$ is allowed without compromising the ability of the CT to sense the ripple for pulses with a short flattop.

The proposed topology is shown in Figure 5.7a and its operational principle in Figure 5.7d. The resistance value R_t is at least one order of magnitude higher than the burden resistance R_b. Therefore, R_b dominates when switch T is on, and the circuit (Figure 5.7a) is equivalent to the circuit of the conventional CT in Figure 5.2a.

When a transient in the primary current is detected, switch T is turned off and the transient resistor R_t acts as the burden resistance. Due to its high value, $f_{\text{-3dB}}^{\text{LF}}$ is shifted to higher frequencies, and therefore the settling time of the CT is reduced, as shown graphically in Figure 5.2e. Shortly after the pulse has reached its flattop, switch T is turned on again, allowing the measurement of the full frequency bandwidth of the current ripple, as shown in Figure 5.7e. Additionally, to detect the start and the end of the transient, voltage v_dt shown in Fig-

ure 5.7a is measured. The detection circuit is critical for the operation of the topology and its implementation is discussed in detail, in Section 5.1.3.

Figure 5.7e shows the frequency response of the proposed CT in steady state (light blue) and in transient state (darker blue). It can be seen that the use of a higher resistance R_t significantly increases $f_{\text{-3dB}}^{\mathrm{LF}}$ and reduces the measurable bandwidth. Moreover, the magnitude gain of the voltage (i.e. the sensitivity) is increased, resulting in a relatively high voltage. To protect the analog components (connected in parallel to R_b, such as e.g. the oscilloscope), zener clamping diodes need to be used. However, these components and their parasitics have an influence on the resulting bandwidth of the CT. The complete circuit of the proposed topology is discussed in more detail, in Section 5.1.4.

5.1.3 Transient Detection

Ideally it should be possible to turn switch T on/off accordingly without the need for external communication interfaces (e.g. external control signal from master controller), that would signify for example the start and the end of the transient state, and the start of the flattop. A transient detection circuit is therefore crucial for an autonomous operation of the proposed current probe topology.

To make the operation autonomous, the detection circuit shown in Figure 5.8a is employed. The voltage across the transient burden resistor R_t is constantly measured, through a compensated RC voltage divider. The analog signal is then buffered, filtered by a passive filter and converted to a digital signal with an appropriately fast ADC. The output of the ADC is then sent to an FPGA. Based on the measured

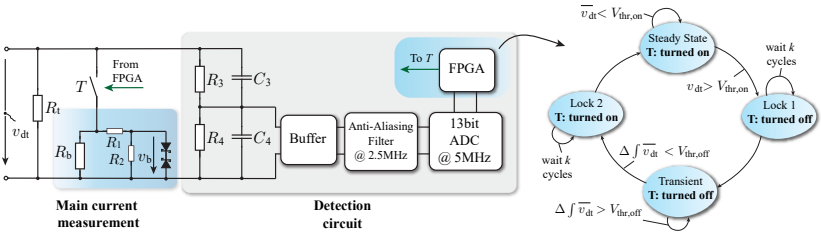

Figure 5.8: a) Circuit overview for transient detection. b) State machine of the detection algorithm.

v_{dt}, the FPGA controls switch T, according to the state machine shown in Figure 5.8b.

Starting from steady state, T is turned on. The digital value of the measured voltage v_{dt} is averaged by the use of a moving average, with an average frequency equal to the lowest frequency expected in the system (in the case of the studied system 60kHz) and compared to a threshold value $V_{\mathrm{thr,on}}$. If $\overline{v}_{\mathrm{dt}} < V_{\mathrm{thr,on}}$, the system remains at steady state.

When a transient occurs, voltage v_{dt} follows (5.4) and eventually $\overline{v}_{\mathrm{dt}} > V_{\mathrm{thr,on}}$. Switch T is then turned off and the algorithm waits for k clock cycles, to prevent it from bouncing. Then, the algorithm enters the transient state, and checks the difference of the integral of the averaged voltage between consecutive samples. If the rate of rise/fall of the integral is high $\Delta \int \overline{v}_{\mathrm{dt}} > V_{\mathrm{thr,off}}$, the system remains in transient state and T remains turned off. When $\Delta \int \overline{v}_{\mathrm{dt}} < V_{\mathrm{thr,off}}$, the system turns T on, waits for k cycles and returns to steady state.

5.1.4 Circuit Design and Component Choice

The detailed circuit of the main measurement path is shown in Figure 5.9a, along with its main parasitic components. At first, when T is turned off, a significant over-voltage may be present, the magnitude of which depends on the detection time. In order to protect the switch, an active clamping circuit is used, with a zener diode connected in series

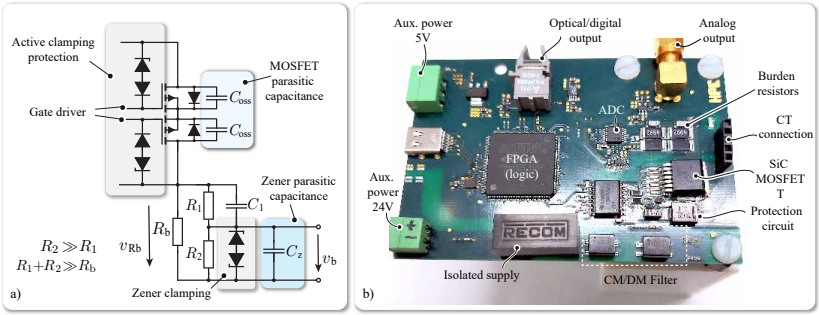

Figure 5.9: a) Detailed electrical circuit for the main voltage measurement path, and its parasitics. b) Picture of the developed CT and the respective PCB.

to a diode as shown in Figure 5.9a.

The parasitic capacitance of the MOSFET is depicted in Figure 5.9a. As long as the output capacitance C_{oss} is sufficiently low, this part does not have an influence on the performance of the circuit. Furthermore, during transients the voltage across the burden resistor is high, and the measured voltage v_{b} needs to be limited. In the circuit of Figure 5.9a, bi-directional zener diodes are used to clamp the measured voltage to the zener breakdown voltage and protect the analog circuitry that is typically in parallel to the burden resistance. However, if zener clamping is used directly in parallel to the burden resistance R_{b}, the current of the diodes will not be limited, and inevitably they will be destroyed by the inrush current. For this reason, another divider R_1 and R_2 is inserted, with $R_2 \gg R_1$. In this case, R_1 is chosen appropriately to limit the current of the zener diode during transients. The additional divider reduces the sensitivity slightly, but its effect is linear, and can be fully compensated.

A disadvantage of the circuit is that the zener diodes have also a parasitic output capacitance (C_{z}), and devices with low output capacitance need to be chosen, in order to not limit further the high frequency performance of the topology. More specifically, due to the parasitic C_{z}, shown in Figure 5.9a, another pole is inserted in the voltage measurement, due to the inclusion of the protection circuit. The transfer function assuming $R_2 \gg R_1$ is given by (5.14). In order to cancel the effect of R_1, a capacitor C_1 is inserted, effectively comprising an RC divider. C_1 can be selected according to (5.15), in order to minimize the effect of the additional circuit. Nevertheless, the parasitic capacitance C_{z} needs to be minimized, since the series combination of C_1 and C_{z}, which is approximately equal to C_{z}, appears to be in parallel to R_{b} and therefore the total impedance of the main measurement circuit $\underline{Z}_{\text{main}}$ is given by (5.16).

$$\frac{v_{\text{b}}(s)}{v_{\text{Rb}}(s)} = \frac{1}{1 + s \cdot R_1 \cdot C_{\text{z}}} \tag{5.14}$$

$$C_1 = C_{\text{z}} \cdot \frac{R_2}{R_1} \tag{5.15}$$

$$\underline{Z}_{\text{main}}(s) = \frac{1}{1 + s \cdot R_{\text{b}} \cdot C_{\text{z}}} \tag{5.16}$$

The hardware prototype of the discussed current probe is shown in

Table 5.3: Part numbers of the prototype current probe.

Description	Manufacturer	Part Number
CT core (Design 2)	Magnetics	C058195A2
MOSFET	Cree/Wolfspeed	C3M0065090J-TR
Gate driver	Texas Instruments	ISO5852SDWR
Zener Diodes (3.9V)	Diodes Inc.	GDZ3V9LP3-7DICT
Zener Diodes (500V)	Littlefuse	SMCJ300A
FPGA	Intel/Altera	10M08SCE144C8G
ADC	Analog Devices	LTC2311HMSE-12

Figure 5.9b. In the studied circuit, switch T is driven by an isolated gate driver which in turn is supplied by an isolated power supply. The main measurement is directly connected to an analog output (SMA connector). A relatively large board area is dedicated to the filters, in order to minimize the effect of the isolated switching supply on the measurement, and reduce any possible DM or CM noise present at the output. Table 5.3 lists the main selected components for the prototype PCB.

5.1.5 Experimental Evaluation

a. Steady State

In this section the two CT designs with the parameters listed in Table 5.2 are evaluated experimentally at steady state, verifying the accompanying models and their performance.

At first, the impedance of the CT seen from the secondary side, with the primary side open circuited is measured with an impedance analyzer, in Figure 5.10a. Based on the measurements, it can be observed that the CT behaves inductively for frequencies up until the self resonance frequency, which is given by the total parasitic capacitance and the total inductance ($L_\mathrm{m} + L_\mathrm{l}$). However, for frequencies higher than the self resonance, the model of Figure 5.2b, with a lumped secondary winding is inaccurate, while the model with distributed winding (2 PI sections) is sufficiently accurate. It should be noted that the additional parameters of the model of Figure 5.4a (e.g. $Z_{\mathrm{l}1}$, $C_{\mathrm{p}1}$ etc.)) are fitted in order to match the experimental results, since an analytical derivation

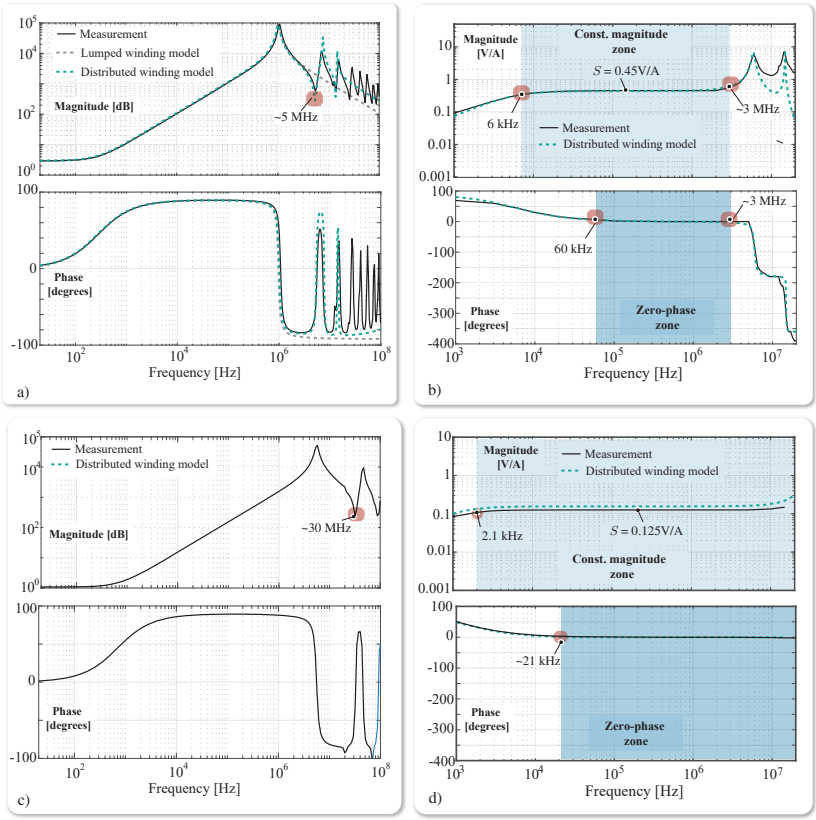

Figure 5.10: Frequency domain measurements of designed CTs (Table 5.2). a) Design 1: Output impedance. b) Design 1: Frequency response with a burden resistance (60Ω). A sensitivity of 0.45V/A is achieved. c) Design 2: Output impedance. d) Design 2: Frequency response with a burden resistance (7.5Ω). A sensitivity of 0.125V/A is achieved.

of these parameters is outside of the scope of this work.

Figure 5.10b shows the frequency response of Design 1 with a burden resistance of 60Ω. It can be seen that in frequencies below 3MHz the measurement behaves similar to the model and a sensitivity of 0.45V/A is achieved, between 6kHz and approximately 3MHz. It can be observed that an approximately zero-phase measurement is possible be-

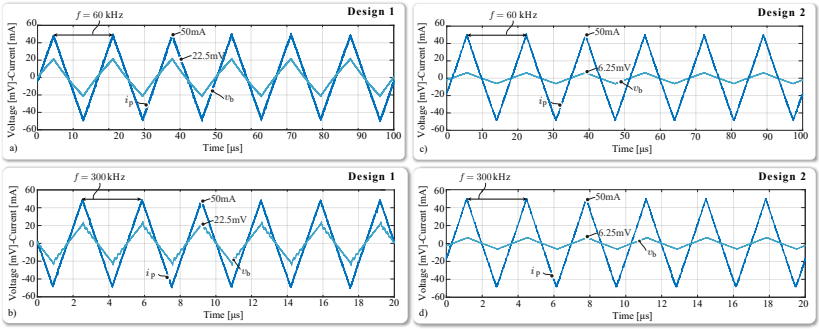

Figure 5.11: Time-domain measurements. a) Design 1: Measurements with a 50mA primary current of 60kHz. b) Design 1: Measurements with a 50mA primary current of 300kHz. c) Design 2: Measurements with a 50mA primary current of 60kHz. d) Design 2: Measurements with a 50mA primary current of 300kHz. Primary current (blue) and sensed voltage v_b (light blue).

tween 60kHz and 3MHz.

Similarly, Design 2 is evaluated in Figures 5.10c&d. Due to the lower number of turns, Design 2 exhibits a significantly higher high frequency bandwidth, with the resonance peak appearing around 30MHz, as it was expected by the fitted high frequency model of Figure 5.5. Notably, the sensitivity is lower than expected (0.125V/A instead of 0.15V/A), which could be attributed to an inaccuracy of the winding resistance and parasitic inductance models, as well as to the tolerance of the burden resistance. As the burden resistance is much lower in this case compared to Design 1, model inaccuracies/tolerances have a bigger effect compared to Design 1. Nevertheless, as shown in Figure 5.10d, Design 2 has demonstrated a bandwidth range between 2.1kHz and more than 20MHz.

Additionally, Figure 5.11 shows experimental results of the alternative designs in the time-domain. It can be observed that Design 1 can follow with precision and low phase delay, triangular currents of 60kHz and 300kHz. The achieved sensitivity is approximately 0.45V/A (constant in the relevant frequency range). It is also worth noting, that in the 60kHz case, a distortion is present, indicating that $f_{\text{-3dB}}^{\text{LF}*}$ needs to be set to a lower value, for a better measurement precision. Finally, in the 300kHz case, a ringing can be seen in the measured voltage waveform, due to the high frequency resonances and the reduced bandwidth of the

CT. Nevertheless, the issues of Design 1 in the low and high frequency range are apparently addressed by Design 2, at the expense of reduced sensitivity. It can be verified that the expected sensitivity of 0.125V/A is achieved and neither distortion at 60kHz nor ringing at 300kHz is observed. It should also be pointed out that despite its low amplitude (only 6.25mV) the measured voltage does not show any significant noise content.

b. Transient State: Single module

In the following, the proposed CT concept (Design 1) with adaptive burden resistance is experimentally validated. The experimental setup used to generate the pulsed-shaped current through the designed CT is shown in Figure 5.12a, and consists of a single high-power module of the current shaping converter. The module is operated with open loop control with a higher duty ratio during the ramp up and a lower duty ratio during flattop, achieving a constant DC offset current of approximately 110A for this measurement.

As a benchmark, a high-end current probe (Tektronix CP500 [99]) is used for sensing the load current. The probe is a DC-2MHz current measurement device which can measure up to 500A, and a sensitivity of 10mV/A. The performance of the proposed current probe for a pulsed-shaped primary current can also be depicted in Figure 5.12b, where the inferred measured current based on the v_{b} measurement is shown.

Furthermore, the effect of the detection time is examined by simply varying the threshold limit $V_{\mathrm{thr,on}}$ (simply by a software change in the FPGA), which has been described in section 5.1.3. In both cases the voltage across the burden resistor remains below 3V keeping the analog circuit safe. Furthermore, in case of the slow detection, it is evident that the clamping protection circuit, limits the measured voltage to the breakdown voltage of the zener diode. Additionally, Figure 5.12b, shows the voltage across switch T. It can be seen, that when the detection is fast, the over-voltage during the turn off of the switch is significantly lower than when the detection acts with a delay. Nevertheless, as shown in Figure 5.9, the design includes an active clamping circuit that will clamp the voltage and protect the switches, if the voltage across T exceeds 500V.

When the primary current across the CT reaches its flattop, the condition for turning on switch T is fulfilled, and the expected voltage with the sensitivity of 0.45V/A is seen across the burden resistance.

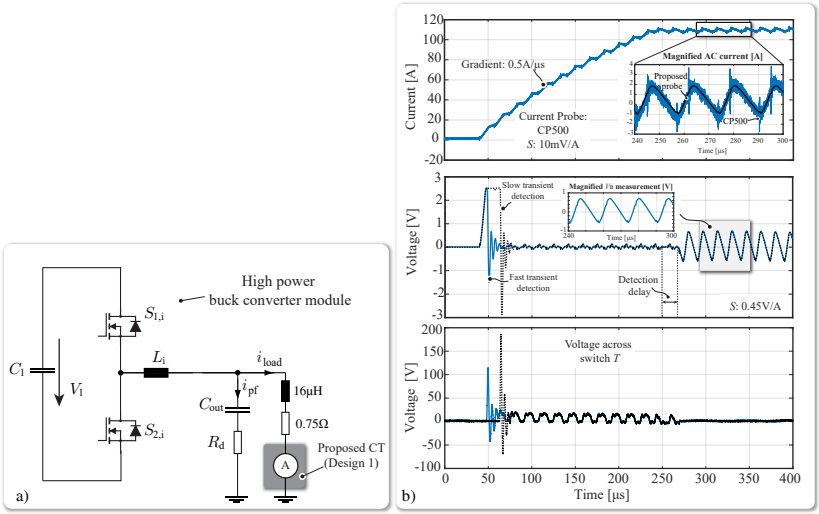

Figure 5.12: a) Schematic of the experimental setup. A high power buck module is used to generate the current. b) Experimental measurements with the proposed CT (Design 1). The load current is also sensed with the Tektronix CP500 current probe, that acts as a benchmark [99]. The voltage measurement across the burden resistance and the voltage across switch T are shown too.

The detection delay time is noted on Figure 5.12b. The detection delay occurs due to the inevitable delay of the moving average filter that is used and is described in section 5.1.3. The delay is approximately one switching period in this case (16.6µs). During flattop, the proposed current probe measures the ripple with high fidelity as shown in the magnified ripple current comparison with the benchmark probe.

c. Transient State: 6-phase interleaved source

In the following, the proposed CT concept (Design 2) is further validated experimentally in transient state with the full prototype current shaping converter providing the pulse through the CT.

Figure 5.13 shows a 415A pulse current controlled with an open loop scheme. During the ramp a higher duty cycle is kept and when the current reaches its desired value, the duty cycle is reduced accordingly to create a flattop. In this case, the Tektronix CP500 current probe acts

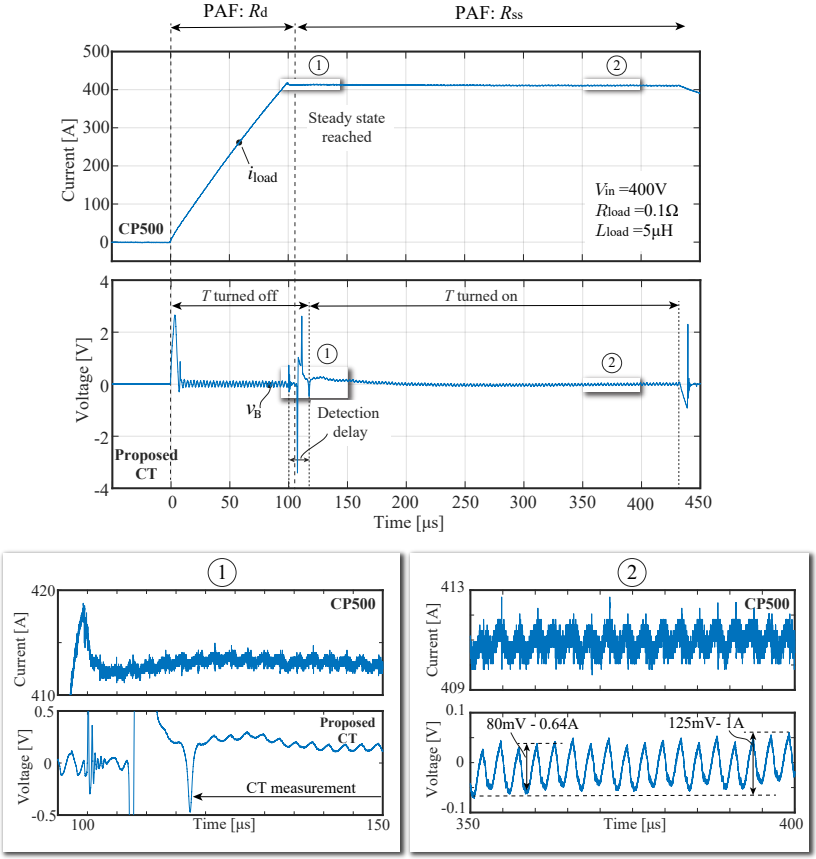

Figure 5.13: a) Experimental measurements with the current shaping converter controlled with an open loop scheme. The proposed CT (Design 2) is used to sense the load current with precision. The load current is also sensed with the Tektronix CP500. The voltage measurement across the burden resistance is shown and transformed into the corresponding current. Magnified views of transition to steady state and performance during flattop are shown too.

again as a benchmark, but it should be remarked that it would not be applicable for currents higher than 500A, which is also the region that the proposed CT is intended to be used. Evidently the CT measurement

starts shortly after the flattop is reached, with a detection delay of approximately 17µs, similar to the one noticed in Figure 5.12.

Furthermore, the low frequency behavior of the current, is captured by the CT, as signified by the offset of the voltage v_b in Figure 5.13b. Nevertheless, the 360kHz ripple is measured with precision when the steady state is reached, as depicted in Figure 5.13c. In the measured case based on the magnified view of the steady state, the current accuracy is 125mV, which corresponds to 1A, while the current ripple has a dominant frequency at 360kHz, as expected from the interleaving and a peak to peak amplitude of 80mV, which corresponds to 0.64A.

5.1.6 Comparative Simulation Results

Based on the analytical models and the performed measurements in steady state, a detailed fitted model of the proposed probe can be established for frequencies up to the resonant frequency of the transformer (i.e. ≈3MHz for Design 1). In this section, simulation results of the proposed CT are presented and the performance is compared with a conventional CT, to further highlight its benefits and demonstrate its performance. All the identified parasitic components are included (e.g. non-ideal MOSFET and zener diodes) along with the protection circuit connected in parallel to R_b, to limit v_b, as shown in Figure 5.7a. The simulated transformer parameters are given in Table 5.1 (Design 1). The transformer is simulated with the magnetic package of PLECS [112]. Communication delays and finite sampling times are also taken into consideration for the control of the detection circuit.

Figure 5.14a shows the current that excites the primary and Figure 5.14b shows the corresponding v_b with the conventional design and with the proposed topology (i.e. Figure 5.7a). The primary current is pulse-shaped with an amplitude of 1kA, and a high current gradient of 10A/µs during transient. At flattop, the simulated current ripple has a magnitude of approximately ±1A, two main frequency components at 360kHz and 60kHz and a triangular shape. This current ripple is a typical ripple at the output of an interleaved converter like the one in Figure 5.1, with each module switching at 60kHz and slightly mismatched module inductances L_i. Figure 5.14a shows also a comparison of the reference current ripple that needs to be measured and the inferred current with the proposed probe. The inferred current of the proposed probe is essentially the measured voltage v_b scaled by a fac-

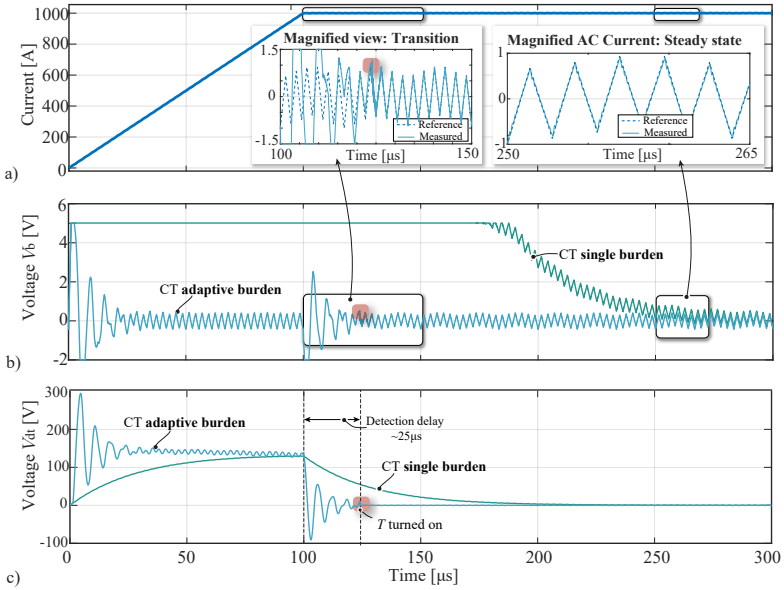

Figure 5.14: a) Primary current simulation and magnified AC ripple with 360kHz and 60kHz frequency components. b) Comparison of the sensed voltage v_b with the conventional CT (Design 1) with a single burden resistance value (green line) with the proposed adaptive burden resistance using the same CT (light blue line). The proposed topology is using an $R_\mathrm{t} = 10\mathrm{k}\Omega$. Both circuits are simulated with ideal zener clamping diodes of 4V and $R_1 = 10\mathrm{k}\Omega$ and $R_2 = 100\mathrm{k}\Omega$. c) Voltage v_dt across the output of the CT.

tor of $1/S$. It can be observed, that the CT manages to follow with precision the reference. However, the resonant behavior at high frequencies causes some oscillations on the measured current, as observed in Figure 5.11b.

Figure 5.14b, shows the measured voltage v_b with the proposed current probe, and compares it to the conventional design and the same CT. The high voltage during the transient is limited in both cases by the protection circuit (i.e. clamping diodes). It is observed that with the proposed topology, the settling time can be significantly decreased, and the AC ripple current can be measured with high precision shortly after the steady state of i_p is reached (in the simulated case the settling time is less than 25µs). The delay is a result of the moving average filter

that is used in the measurement of v_{dt}, as well as additional delays due to the non-ideal turn on times of the switch T. It is therefore observed that with the proposed probe with adaptive response, the measurement of pulsed currents with shorter flattops can be enabled, and wider bandwidth can be utilized as it does not anymore influence the settling time of the current probe after the transient.

5.2 Active Adaptive Output Filter

In the field of accelerator magnet supplies active filters connected at the output, in order to facilitate the ripple attenuation and provide a current pulse with an ultra-low ripple flattop have been investigated, and successful implementation has been demonstrated in literature [134–139]. In most of these cases however the active filter consists of a switching amplifier, and manages to achieve ripple cancellation at relatively low frequencies (a few Hz up to a couple of kHz), while the high frequency harmonics introduced by the switching actions of the switching amplifier are attenuated with the use of an output inductance, and the parallel connection of a high capacitive branch that limits the dynamic behavior of the load current, as discussed in Section 3.3. Another limitation of this concept is the control bandwidth of the switching amplifier and the constraints regarding the dynamic performance of the filter, introduced by the inclusion of the aforementioned output inductance.

In this work, an active filter based on linear amplification is investigated, designed and eventually developed and validated in order to achieve high frequency cancellation in a wide range of frequencies from a couple of kHz up to several hundreds of kHz. The advantage of using a linear amplifier is the absence of additional switching harmonics introduced by the filter, at the expense of additional losses. However, since the output current that needs to be supplied is low, the power losses have a negligible effect on the overall efficiency of the system. Moreover, with the use of high bandwidth operational amplifiers, high frequency attenuation can be achieved. The active filter which is conceptualized in Figure 5.1, uses the developed CT as a reference, and provides a current accordingly to eliminate the ripple of the load current. Due to the high sensitivity provided by the CT, the developed active filter can achieve high attenuation even at very low current ripples in the mA range. It should also be noted that the active filter branch is activated

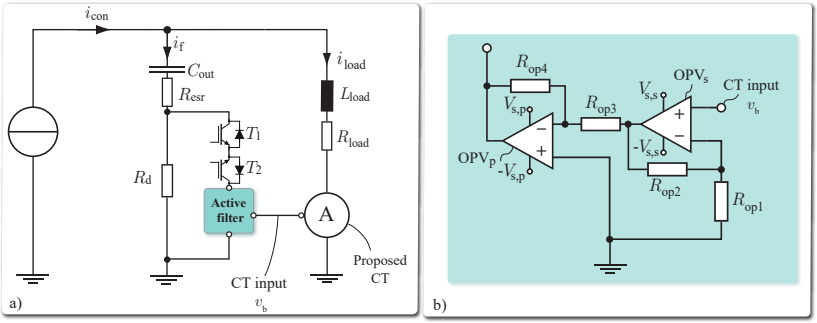

Figure 5.15: a) Simplified topology of the active adaptive filter circuit. The current shaping converter is modeled as an ideal current source. b) Circuit schematic of the active filter consisting of two op-amps. OPV_s (non-inverting amplifier) is a high speed pre-amplifier to provide amplification of the reference voltage generated by the proposed CT, while OPV_p (inverting amplifier) is a power op-amp with the ability to drive up to 1.5A of output current.

only during the flattop, and essentially replaces the resistor R_{ss} of the PAF in Figure 3.6d.

In this section at first, the topology of the investigated circuit is shortly discussed (Figure 5.15) and the feedback loop is modeled, indicating the most important design parameters of the system. After considering the effect of the parameters of the filter, the trade-offs of the system are discussed. Finally, the prototype active adaptive filter (AAF) is shown and its operation is verified experimentally.

5.2.1 Topology & Modelling

The active adaptive filter (AAF) concept is shown in Figure 5.15a. Here, the active filter is taking the place of the steady state resistance R_{ss}, which was used for the passive adaptive filter (PAF) in Figure 3.6d. Ideally the filter should provide a high quality factor (at least similar to the one chosen for the design of R_{ss}) to the loop and a better cancellation performance over a wide range of frequencies and loads. It should be highlighted that the concept of the adaptive response is the same as described in Section 3.3, as switches T_1-T_2 are turned off during the transients and turned on (enabling the active filter branch) during the

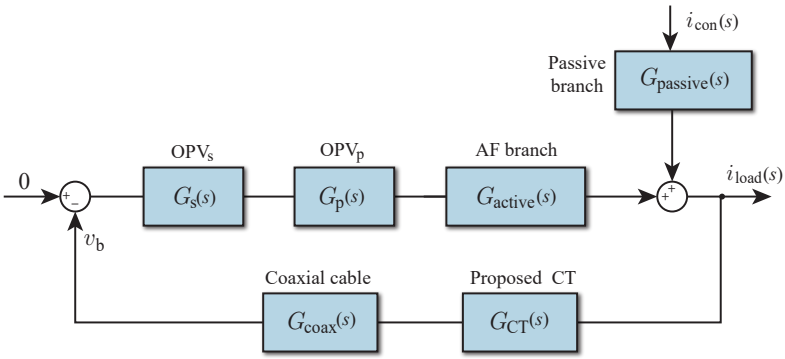

Figure 5.16: Analog feedback loop of the investigated active filter.

flattop of the pulse.

The detailed circuit of the active filter is given in Figure 5.15b. The circuit receives the input reference voltage v_b and provides initial amplification of the signal through a non-inverting amplifier. The op-amp OPV$_s$ acts as a pre-amplifier and needs to have a high gain-bandwidth product, without the need to drive a high output current. The output voltage of OPV$_s$ is further amplified with a power amplifier OPV$_p$, configured as an inverting amplifier, that needs to drive the high output current (> 1A) too. This amplifier has inevitably a lower gain-bandwidth product given by its design.

The analog feedback loop is depicted in Figure 5.16. The total closed loop transfer function G_{CL} that describes the attenuation of the current is then given by (5.17). Apart from the transfer function of the measurement transformer G_{CT}, which was described in the previous section, the feedback loop includes the coaxial cable G_{coax} that is used to connect the CT output to the the active filter board's input. In the following, the high damping branch formed by resistor R_d is neglected. Resistor R_{esr} includes both the parasitic resistance of the capacitor as well as the on-resistance of switches T_1 and T_2.

$$G_{CL} = \frac{i_{load}}{i_{con}} = \frac{G_{passive}(s)}{1 + G_{active}(s) \cdot G_p(s) \cdot G_s(s) \cdot G_{CT}(s) \cdot G_{coax}(s)} \tag{5.17}$$

in this work, the op-amps are modeled as first order low pass filters,

with their bandwidth determined based on their gain-bandwidth product GBP_s and GBP_p respectively. The transfer functions $G_\mathrm{active}(s)$, $G_\mathrm{passive}(s)$, $G_\mathrm{s}(s)$, $G_\mathrm{p}(s)$ are given by (5.18)-(5.21).

$$G_\mathrm{active}(s) = \frac{1}{R_\mathrm{esr} + \frac{1}{s \cdot C_\mathrm{out}} + s \cdot L_\mathrm{load} + R_\mathrm{load}} \tag{5.18}$$

$$G_\mathrm{passive}(s) = \frac{R_\mathrm{esr} + \frac{1}{s \cdot C_\mathrm{out}}}{R_\mathrm{esr} + \frac{1}{s \cdot C_\mathrm{out}} + s \cdot L_\mathrm{load} + R_\mathrm{load}} \tag{5.19}$$

$$G_\mathrm{s}(s) = \left(1 + \frac{R_\mathrm{op2}}{R_\mathrm{op1}}\right) \cdot \frac{1}{1 + s \cdot \frac{1+R_\mathrm{op2}/R_\mathrm{op1}}{2\pi \cdot GBP_\mathrm{s}}} \tag{5.20}$$

$$G_\mathrm{p}(s) = \frac{-R_\mathrm{op4}}{R_\mathrm{op3}} \cdot \frac{1}{1 - s \cdot \frac{R_\mathrm{op4}/R_\mathrm{op3}}{2\pi \cdot GBP_\mathrm{p}}} \tag{5.21}$$

The response of the coaxial cable with 50Ω nominal impedance is modeled with an equivalent lumped inductance L_coax and capacitance C_coax, while a R_term =50Ω termination resistor is included in the design at the receiver's end. The termination resistor is needed to avoid possible reflections that may result in oscillations of the analog signal. Moreover, the op-amp that is used as a buffer to drive the coaxial cable is neglected, since an op-amp with a high gain bandwidth product can be chosen, and its effect in the relevant operation region of the feedback loop is negligible. The response of the coaxial cable $G_\mathrm{coax}(s)$ is then given by (5.22).

$$G_\mathrm{coax}(s) = \frac{R_\mathrm{term}}{1 + s \cdot R_\mathrm{term} \cdot C_\mathrm{coax}} \cdot \frac{1}{\frac{R_\mathrm{term}}{1+s \cdot R_\mathrm{term} \cdot C_\mathrm{coax}} + s \cdot L_\mathrm{coax}} \tag{5.22}$$

5.2.2 Frequency Response & Stability Analysis

For a given current transformer design (given G_CT), the previously described models essentially allow the circuit designer to choose the gains of the pre-amplifier and the power amplifier by setting the resistances R_op1-R_op4, as well as the output capacitance C_out. The gains of the amplifiers are limited by the gain-bandwidth products GBP_s and GBP_p. In this work, as a reference for the design considerations that follow a best-in-class power op-amp with the ability to drive ±1.5A with a $GBP_\mathrm{p} = 17\mathrm{MHz}$ and a wide supply voltage range (24V) is pre-selected

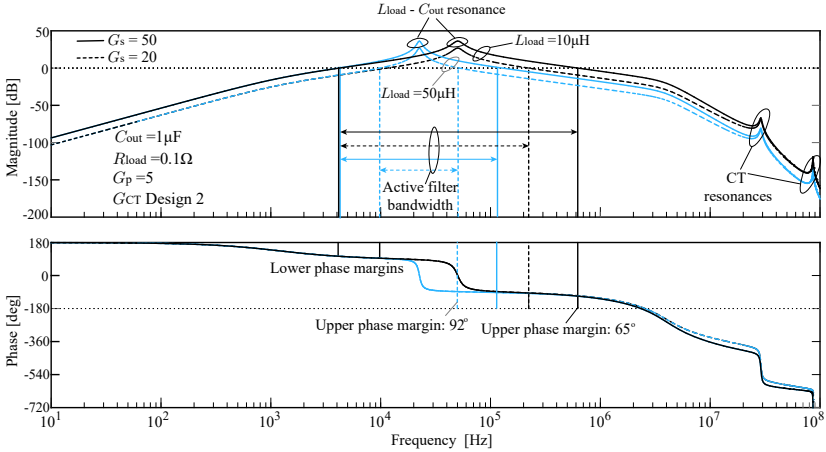

Figure 5.17: Open loop response & stability of the active filter. Four different cases are shown: i) $L_{\text{load}} = 10\mu\text{H}$ - $G_{\text{s}} = 50$ (black solid), ii) $L_{\text{load}} = 10\mu\text{H}$ - $G_{\text{s}} = 20$ (black dashed), iii) $L_{\text{load}} = 50\mu\text{H}$ - $G_{\text{s}} = 50$ (light blue solid), iv) $L_{\text{load}} = 50\mu\text{H}$ - $G_{\text{s}} = 20$ (light blue dashed). The rest of the parameters remain constant and are noted on the graph.

(Texas Instruments OPA564 [150]). For simplicity in the upcoming analysis and figures the gain of the power op-amp is set to 5 and only the gain of the pre-amplifier is changed to demonstrate the influence of the overall gain on stability and attenuation. As a pre-amplifier since there is no special requirement regarding its power levels, an operational amplifier with GBP_{s} of 400MHz is considered in the following. For the remaining of this work the current transformer Design 2 (Table 5.2) is used in the relevant calculations.

Initially, Figure 5.17 depicts the open loop response of the feedback loop shown in Figure 5.16, for different load inductances and different gains of the pre-amplifier. The open loop transfer function is given by (5.23), and gives an indication of the bandwidth of the active filter and its phase margin.

$$G_{\text{OL}}(s) = G_{\text{CT}}(s) \cdot G_{\text{coax}}(s) \cdot G_{\text{p}}(s) \cdot G_{\text{s}}(s) \cdot G_{\text{active}}(s) \qquad (5.23)$$

From Figure 5.17 it can be noted, that the open-loop transfer function has two phase margins, a lower frequency phase margin and an

upper frequency phase margin. In order to get a stable and robust closed loop system, these two phase margins must be positive and large enough. The lower frequency bandwidth is mainly determined by gain G_{s}, the output capacitance C_{out} and the low frequency bandwidth of the CT $f_{\text{-3dB}}^{\mathrm{LF}}$, but not by L_{load}. The lower phase margin for all four of the studied cases is positive. On the other hand, the high frequency gain margin depends on the L_{load} as well as on G_{s}. It can be seen that lower L_{load} inductance values lead to a lower phase margin. Moreover, higher amplifier gains result also to lower phase margins. All the studied cases result in a positive phase margin, but nevertheless a trade-off between gain and stability can be observed, based on the phase plot of Figure 5.17.

Additionally the resonance peaks of the CT transfer function are also visible in the open-loop response. The resonance peaks must be below the 0dB line, as the phase shifts by 180° at these frequencies. This effect would cause an oscillation at the resonance frequency. This observation further highlights the need for a CT with a high enough bandwidth, as the resonance peaks are shifted to the right in the frequency spectrum, where the attenuation is high. The resonance frequency is given by the design of the CT, but the peak value is influenced by the total gain and the load inductance. Based on the above it can be deduced that the active filter response needs to be stable for the lowest inductance value in the operating range.

Furthermore, the control bandwidth of the active filter is defined from the frequencies between the lower and the upper phase margin (i.e. region where the gain is positive). In this region, the filter controls its attenuation actively. This observation along with the fact that the CT's $f_{\text{-3dB}}^{\mathrm{LF}}$ influences the lower phase margin frequency, highlights again the need for a CT with a sufficiently low $f_{\text{-3dB}}^{\mathrm{LF}}$, which was facilitated in this work by the use of the proposed CT with an adaptive response. It can finally be observed that the higher the gain of the feedback loop and the lower the L_{load}, the higher the bandwidth of the active filter. Especially in the lower frequency range it is visible that a high gain can be particularly beneficial.

Figure 5.18 shows the closed loop response of the feedback loop given by (5.17). It can be deduced that a higher gain results in a lower cut-off frequency (i.e. 5kHz instead of 15kHz) and therefore higher attenuation at the low frequency range. This property is particularly beneficial as it can help in mitigating the deteriorating effect of the con-

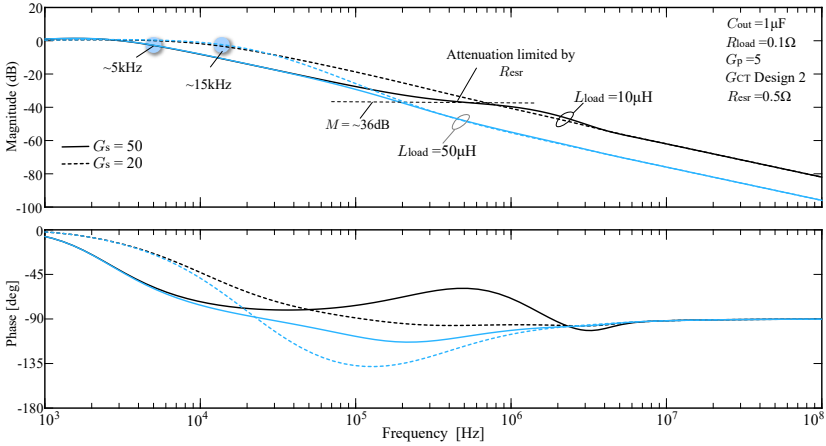

Figure 5.18: Closed loop response of the active filter. Four different cases are shown: i) $L_{\text{load}} = 10\mu\text{H}$ - $G_{\text{s}} = 50$ (black solid), ii) $L_{\text{load}} = 10\mu\text{H}$ - $G_{\text{s}} = 20$ (black dashed), iii) $L_{\text{load}} = 50\mu\text{H}$ - $G_{\text{s}} = 50$ (light blue solid), iv) $L_{\text{load}} = 50\mu\text{H}$ - $G_{\text{s}} = 20$ (light blue dashed). The rest of the parameters remain constant and are noted on the graph.

trol induced low frequency harmonics (<20kHz) in the current flattop accuracy[2]. It is also observed that the attenuation with $L_{\text{load}} = 10\mu\text{H}$ - $G_{\text{s}} = 50$ (black solid line) reaches a plateau around 600kHz. This phenomenon is attributed to the control bandwidth of the active filter, and the attenuation magnitude at the plateau is essentially limited by the total gain of the control loop, and the equivalent series resistance of the filter branch (R_{esr}). In the demonstrated case, the total loop gain is $G_{\text{gain}} = S \cdot G_{\text{p}} \cdot G_{\text{s}}$ and the equivalent parasitic resistance is assumed to be 0.5Ω. The plateau magnitude M is then given by the ratio $R_{\text{esr}}/G_{\text{gain}} \approx 36\text{dB}$. Based on the response of Figure 5.18 it can be seen that after a point the attenuation is independent of the gain of the amplifier, as the passive components dominate. Finally, it should be observed that the quality factor in all the calculated cases remains very high, as G_{CL} does not exhibit any significant gain/peak at low frequencies.

According to the presented analysis a valuable insight can be de-

[2]the effect of these low frequency harmonics was observed in Chapter 4, both with simulations as well as with experimental measurements.

rived. It has been shown that the higher the gain of the feedback loop, the lower the cut-off frequency for the same passive components, and therefore the higher the attenuation in the low frequency range. However it was also shown that the gain of the amplifier is essentially limited by the upper frequency phase margin. A phase margin higher than 60° is considered sufficient in this work. Furthermore, in practice the gain of the total loop is limited by the supply voltage of the operational amplifiers and especially the power amplifier, which exhibits the highest losses due to the need to drive a high output current. This consideration is also taken into account in the design of the prototype AAF board in Section 5.2.4.

5.2.3 Comparison with PAF

The PAF output stage has been proposed in Section 3.3, in order to be used for systems that need to deliver pulses with high dynamic and low ripple flattops. There, a high resistive branch is used during the transients and a low resistive branch dominates during steady state. A consistent way to select R_{d} and R_{ss} based on the load parameters has also been proposed, with the focus on keeping the quality factor high, in order to avoid the unnecessary amplification of harmonics in the low frequency range (lower than the switching frequency). The same concept was demonstrated in Section 5.2 for the case of the AAF, where the damping resistance R_{d} is inserted during the dynamic transients, and the active filter takes the place of the steady state resistor R_{ss} in steady state.

In Figure 5.19, the attenuation of the two proposed output stages as a function of the load inductance L_{load}, at three selected frequencies (f = 10kHz (solid), f = 60kHz (dashed) and f = 360kHz (dotted)) is evaluated. For the studied system, the attenuation of the filter at 10kHz shows an indication of the performance of the output stage in attenuating control induced frequencies. Moreover, the A attenuation at 60kHz is needed for the prototype current source to account for the remaining ripple due to inevitable mismatches in the module inductance values of the current shaping converter, while the 360kHz case is the effective switching frequency of the load current and constitutes the main frequency component of the load current. The parameters of the active and passive filters are noted also in Figure 5.19 and remain constant . The only parameter that changes is the chosen R_{ss} which is

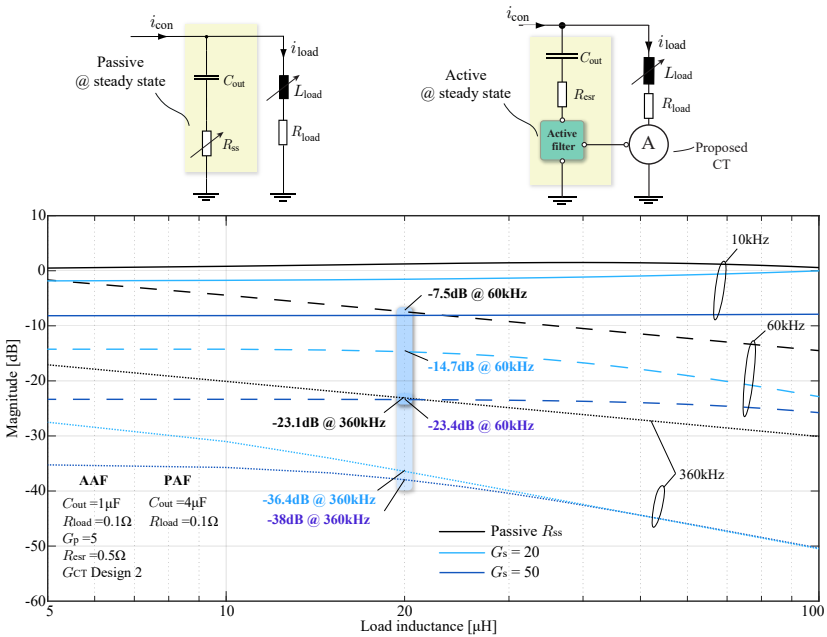

Figure 5.19: Comparison of the achieved attenuation as a function of the load inductance L_{load}, at three selected frequencies (f = 10kHz (solid), f = 60kHz (dashed) and f = 360kHz (dotted)). Three filter configurations are studied: i) PAF with R_{ss} (black), ii) AAF with $G_{\text{s}} = 20$ (light blue) and iii) AAF with $G_{\text{s}} = 50$(dark blue). All parameters (except from R_{ss}, which changes according to (3.28)) remain constant and are noted on the graph.

calculated by (3.28), since it is a function of the load inductance L_{load}. Two active filter configurations with $G_{\text{s}} = 20$ (light blue) and $G_{\text{s}} = 50$ (dark blue) are investigated.

It can be observed that in all the studied cases the AAF achieves higher attenuation, and as expected the AAF with $G_{\text{s}} = 50$ performs significantly better at lower frequencies compared to the AAF with $G_{\text{s}} = 20$. The AAF is particularly beneficial at lower frequencies, where the attenuation of the passive filter is relatively low. It is noted that for a load inductance of 20µH at 60kHz the passive solution achieves only -7.5dB, compared to -23.1dB achieved by the AAF with $G_{\text{s}} = 50$. It can also be concluded that a high gain is not particularly beneficial at at-

tenuating the 360kHz component, providing only a minor improvement for load inductances higher than 20μH.

5.2.4 Prototype AAF: Design & Verification

The prototype design of the AAF board is shown in Figure 5.20. The board is similar to the one shown in Figure 3.34, with slight modifications to accommodate the active filter part, while the R_{ss} resistors are kept and replaced with 0Ω components. Notably the board includes an analog coaxial cable input for the feedback voltage v_b of the current transformer, and an optical digital input that receives the control signal. The digital input is generated by the CPLD of the CT board, and was discussed in Section 5.1.4. The digital input controls in this case switches T_1-T_2 and allows the autonomous operation of the complete feedback loop. More specifically, when the CT's board logic (see Section 5.1.3) detects a transient, it notifies the active filter branch to turn off the switches immediately to avoid a high inrush current that might damage the operational amplifiers. On the other hand, when the CT board logic detects a return to steady state, it notifies the active filter branch to turn on the switches and enable the power op-amp OPV_p with a small delay (software setting).

In Figure 5.20, the OPV_p IC can be seen (OPA564 [150]) with an exposed pad on top to allow the external attachment of a small heatsink[3]. A separate low noise isolated power supply is used to supply OPV_p. Differential mode and common mode filters are also used to ensure sufficient power supply rejection ratio. A preliminary loss analysis and a respective thermal performance verification of the OPV_p has shown, that a supply voltage between ±5V and ±7V would be acceptable in terms of losses (maximum temperature) and provides sufficient voltage margin for driving the output current. In the end, a more conservative design with ±5V has been chosen, in order to limit the power losses and simplify the cooling concept. The maximum calculated losses of OPV_p were found to be approximately 3W and the maximum measured junction temperature[4] for a current of ±1.5A was measured at 85°.

To verify the modelling work that took place in Section 5.2.1, Figure 5.21 shows the open loop transfer function of the active filter branch,

[3]the heatsink is not shown in the picture, but it is necessary for proper cooling of the device.

[4]the chosen device features an integrated temperature sensor.

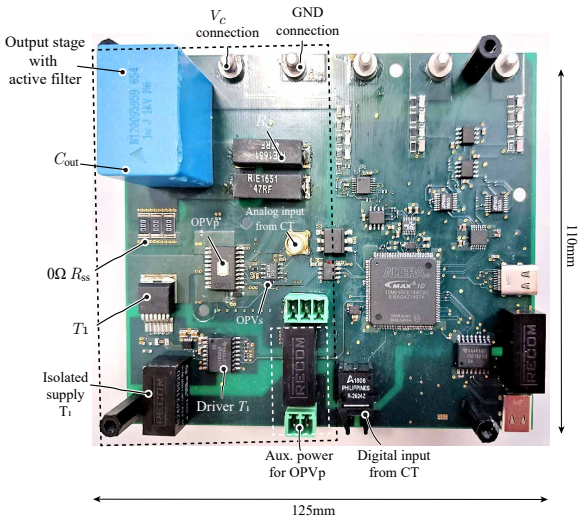

Figure 5.20: a) Top layer of the voltage measurement board with the AAF output stage. The proposed and developed PAF (shown in Figure 3.34) is replaced by the AAF. The rest of the PCB remains the same.

measured with the circuit depicted in the figure. The plotted result corresponds to the transfer function of (5.24). It should be observed that compared to the open loop transfer function of (5.23), the measured transfer function does not include the transfer function of the current transformer, the response of which is however known and verified experimentally. Nevertheless, the measurement verifies the considerations of Section 5.2.1 from the low frequency range up to several hundreds of kilohertz.

$$G_{\mathrm{OL}}(s) = \frac{i_{\mathrm{load}}}{V_{\mathrm{inj}}} = G_{\mathrm{coax}}(s) \cdot G_{\mathrm{p}}(s) \cdot G_{\mathrm{s}}(s) \cdot G_{\mathrm{active}}(s) \qquad (5.24)$$

Figure 5.22 shows the operation of the AAF during the transition period, and the cancellation it provides for 60kHz and 360kHz frequencies. Before enabling the active filter branch, the load current ripple is high as the damping branch (R_{d}) does not provide sufficient attenuation. After enabling the branch, it can be observed that the ripple is greatly reduced in both cases, and as expected the 360kHz component is essentially eliminated. It can be deduced that the prototype AAF not

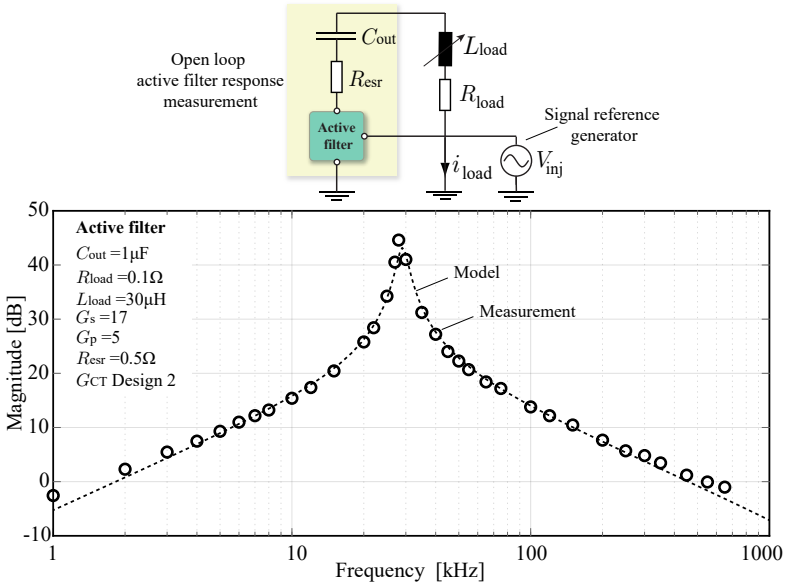

Figure 5.21: Measurement of the open loop transfer function of the active filter branch. The schematic of the measurement setup as well as its parameters are shown too. The expected transfer function based on the previously described models is also shown (dotted line).

only transitions relatively smoothly from one state to the other, but it is also able to handle extremely low load current amplitudes (less than 2mA peak to peak current), thanks to the accurate feedback of the CT.

Additionally, the closed loop performance is tested as shown in Figure 5.23, where the magnitude of $i_{\text{load}}/i_{\text{con}}$ is plotted (black scattered data points for active filter). The dotted line shows the calculated performance of the loop based on the established models and further verifies the modelling work conducted in Section 5.2.1. The gray data points depict the measured performance of the PAF output stage with a simple passive resistance R_{ss}. The parameters of the measurement setup are noted on the graph. It can be observed that excellent attenuation is achieved with the active filter up to several hundreds of kilohertz.

Finally, in Figure 5.24 the developed AAF and the proposed CT are

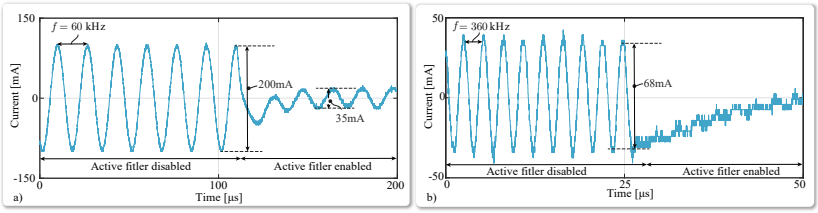

Figure 5.22: Measurements of the AAF performance during transition. Switches T_1-T_2 are initially off and they are turned on enabling the active filter branch. a) Sinusoidal load current of 60kHz. b) Sinusoidal load current of 360kHz.

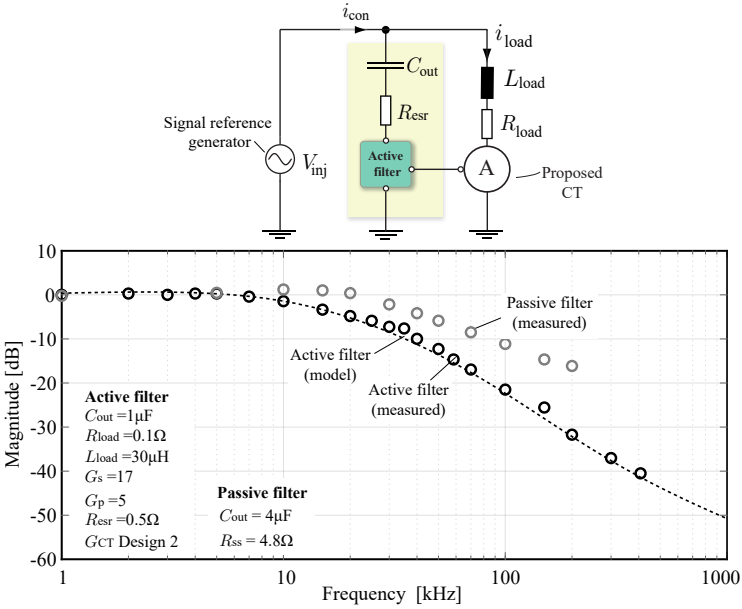

Figure 5.23: Measurement and verification of the closed loop performance of the AAF with the parameters shown in the figure. The measured performance of the PAF with a passive R_{ss} of 4.8Ω is also shown.

tested under operation with the current shaping converter of DynA-CuSo. The interleaved system is controlled with an open loop control

scheme[5] and the load is a resistive/inductive with $R_{\text{load}} = 0.1\Omega / L_{\text{load}} = 5\mu\text{H}$. The active filter gains are set to $G_{\text{s}} = 17$, $G_{\text{p}} = 5$ and the current transformer with the Design 2 set of parameters (Table 5.2) is used for this measurement too.

Figure 5.24a shows the module currents $i_{\text{L},1..6}$ and the total converter current i_{con}, measured with the Tektronix CP500 current probe [99]. The duty cycle of the modules is initially high, generating a gradually increasing current. When the desired current is reached, it is reduced to keep the current constant at flattop. Figure 5.24a also depicts the measured flattop current with the benchmark probe in a magnified view.

Figure 5.24b shows voltage v_{b} across the burden resistance of the CT, that is also the reference to the active filter branch, when it is activated. When the rise of the current starts, the CT detects the transient and R_{t} acts as the burden resistance as described in Section 5.1.2. When the flattop is established, the CT returns to its steady state operation and starts measuring, by turning on switch T and inserting the burden resistance R_{b}. Once again it can be observed that the detection delay is approximately one switching period (16μs). At that point, the CT sends also through its optical output a signal to the AAF, signifying that steady state has been reached. Initially the active filter branch stays de-activated for this test, and is only activated 200μs later, in order to clearly demonstrate the effect of the activation. Additionally, the transition of the active filter branch by enabling switches T_1- T_2 is shown with a magnified view in Figure 5.24b. A small disturbance in the load current can be observed, arising due to the rapid change of the output stage impedance. It should be noted that even this small disturbance might be unacceptable for certain applications.

Figures 5.24c&d depict the measured load current ripple before and after the activation of the active filter branch. More specifically, before the activation, only the damping resistance R_{d} set at 47Ω for this measurement is responsible for filtering the converter current ripple, and therefore a relatively high 360kHz harmonic component is measured (approximately 280mA). After the activation of the active filter the ripple is greatly reduced to less than 40mA for the 360kHz harmonic component. In this case the effect of the switching actions is pronounced, due to the low amplitude of the main harmonic compo-

[5] in order to avoid the effect of low frequency harmonics induced by the closed loop control actions, an open loop control scheme is used.

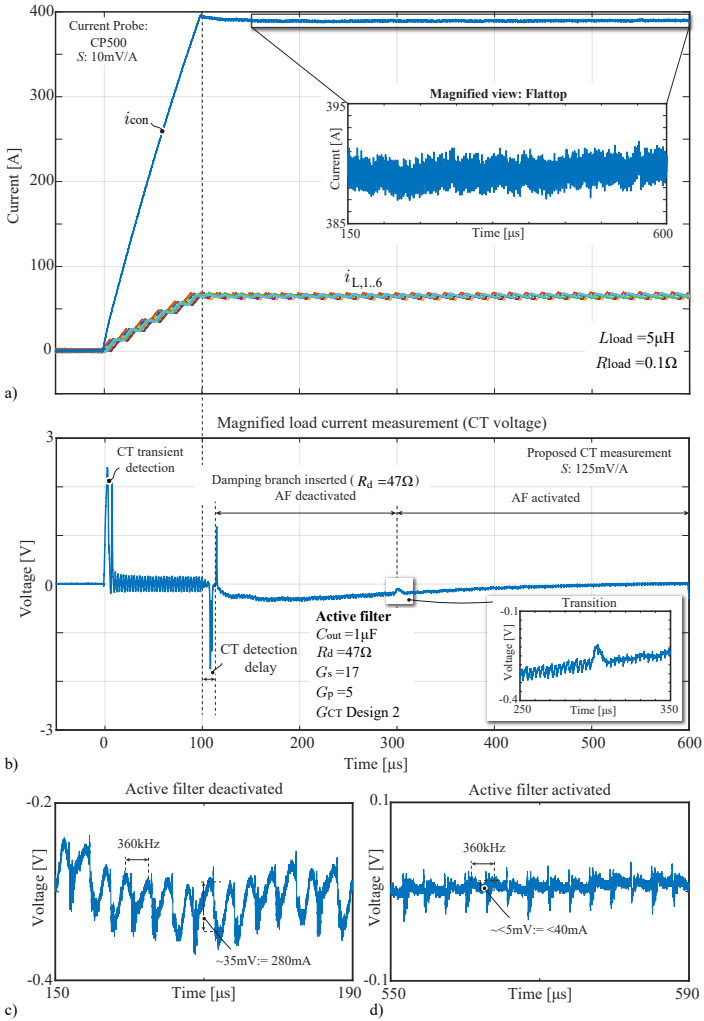

Figure 5.24: Experimental measurements with the current shaping converter controlled with an open loop scheme ($R_{\text{load}} = 0.1\Omega$ - $L_{\text{load}} = 5\mu\text{H}$). a) Module currents $i_{\text{L},1..6}$ and total converter current i_{con}. b) Voltage v_{b} across the burden resistance of the CT, and magnified view of the AAF transition. c) Magnified view of the load current ripple before the activation of the active filter. d) Magnified view of the load current ripple after the activation of the active filter.

nent of the load current ripple.

Interim Summary

This chapter dealt with the output ripple in pulsed power applications, which is a defining parameter for loads that require highly precise current waveforms. Initially a current transformer concept with a wide bandwidth, high sensitivity and low settling time, based on an adaptive burden resistance concept was proposed, and later optimized, designed and developed. It was shown that the proposed current sensor can sense low ripple currents of a few mA superimposed on current flattops up to 1kA, with high sensitivity (e.g. 0.45V/A and 0.125V/A prototypes developed). More specifically the finally used prototype current sensor can operate fully autonomously thanks to its accompanying circuitry and achieves a sensitivity of 0.125V/A, and a bandwidth between 2.5kHz and approximately 30MHz. The performed verification measurements showed that the proposed current sensor can settle quickly after the flattop is established (detection delay time 17µs) and can reveal the ripple and overall accuracy of the current flattop.

The second part of the chapter proposed an active adaptive filter stage based on linear amplification, to help further mitigate the detrimental effect of the output ripple and the control induced low frequency harmonics on the precision of the current source. The AAF uses the PAF output stage concept proposed in Section 3.3, but replaces the steady state resistance R_{ss} with an linear amplifier, that uses the feedback received by the proposed CT (amplified by a high bandwidth, low power amplifier) to attenuate the remaining load current ripple. The feedback loop has been modeled and the superiority of the solution compared to the initially proposed PAF output stage in terms of harmonic cancellation at relevant frequencies has been demonstrated. The findings have been verified experimentally with a low power setup, and frequency cancellation in ranges higher than 500kHz has been demonstrated. Finally, experimental results with the high power prototype current shaping converter of the DynACuSo have exhibited the cooperation of the proposed CT with the AAF for a pulse-shaped current.

6
Prototype System

Motivation

During the prototype development process of high power electronic systems several engineering challenges are encountered and customized solutions need to be found, while additional performance trade-offs need to be respected. The process of hardware development especially at high power levels often involves design issues that stem among others from the mechanical integration of the different subsystems, thermal management, and electrical insulation. These issue often get overlooked during the conceptual design phase. Therefore, a full-scale development is necessary as a final proof-of-concept, despite the relatively high implementation effort that is usually required. The development of the different subsystems of DynACuSo is showcased in this chapter. In parallel this chapter provides a generic framework with a step-by-step analysis, design and verification of the individual converter systems, and gives the required underlying models.

Furthermore as highlighted in the introductory chapter, one of the main motivations behind the development of DynACuSo is its deployment for future HVDC switch-gear characterization purposes. Modelling DC-breakers is by definition challenging, as the properties of the DC-arc that is formed are unknown, and valid models require extensive measurement results. Such experiments have been performed in the past, and research activities in the field continue to emerge, as already mentioned in Chapter 1. The DynACuSo however, with its high dynamics and low ripple, is significantly different than existing current sources that have been at times deployed in the exploration of the prop-

erties of the DC-arc. Therefore no relevant data can be found for the proper modelling/simulation of the operation of the source with such loads. A natural consequence of the above is that the only way to verify the operation of the system with DC-arcs is to perform experimental measurements. In this chapter, the dynamic operation of the DynACuSo with a DC-arc as a load is demonstrated experimentally. The achieved performance is believed to constitute a significant step ahead, that enables further research opportunities in the field of DC circuit breaker technology.

In this chapter, at first the input capacitor bank which is the main storage element of the system is presented and optimized. Later on, the step voltage generator concept is discussed, and the hardware prototype of the fundamental stage module, which is an integral part of the concept is presented. Experimental results also reveal the performance of the module and a well-defined design procedure is followed to make sure that the prototype remains inside its SOA for every operating condition. Afterwards, specific focus is given on the control integration of the step voltage generator into the existing closed loop control of the current shaping converter, which was evaluated in detail in Chapter 4. For the proper operation of the DynACuSo, the control of the step voltage generator should ensure on the one hand that ideally little to none additional disturbances are introduced, and on the other hand that the high voltage capabilities are harnessed, facilitating the transient performance. Experimental measurements not only verify the considerations, but also showcase the potentials of the DynACuSo. More importantly, experimental measurements demonstrate the operation of DynACuSo while it controls the current through DC-arcs under various conditions. Additionally, the interface converter system is presented for completeness and its different operation modes, along with the developed hardware are demonstrated. Finally, the overall system operation of the developed prototype is discussed, and its operational and performance limits are explored.

6.1 Input Capacitor Bank

Due to the high output power that the source needs to deliver to the load[1], sufficient energy has to be stored before the experiment takes

[1] in the pulsed operation mode.

place, in order to avoid disturbances in the local grid. During the design procedure the input voltage levels V_1 and V_2 have been assumed to be constant for simplicity, but in reality during pulsed operation for a positive current, capacitor C_1 is discharging and capacitor C_2 is charging. In order to ensure that the design assumptions are met and that the equipment remains in its SOA, V_1 and V_2 need to remain within a defined range. Consequently, proper dimensioning of capacitors C_1 and C_2 is crucial.

To begin with, electrolytic capacitors are chosen for the input capacitor bank, since they offer the highest energy density. Their relatively high parasitic resistance also helps to attenuate some of the oscillations that are caused due to the LC circuit formed by the parasitic inductance of the DC link (i.e. busbar connection to the current shaping converter) and the film capacitors used as decoupling capacitors on the individual modules (see Figure 3.27). Furthermore, two capacitors are connected in series to form C_1 due to the unavailability of electrolytic capacitors for voltage levels higher than 450V, and parallel balancing resistors are placed in each capacitor to ensure that the voltage is divided equally.

The detailed topology of the input DC-link is then shown in Figure 6.1a, where k signifies the number of C_1 capacitors connected in parallel and l the number of C_2 capacitors in parallel. For safety reasons, bleeding resistors are placed in parallel to the capacitors of C_2 too.

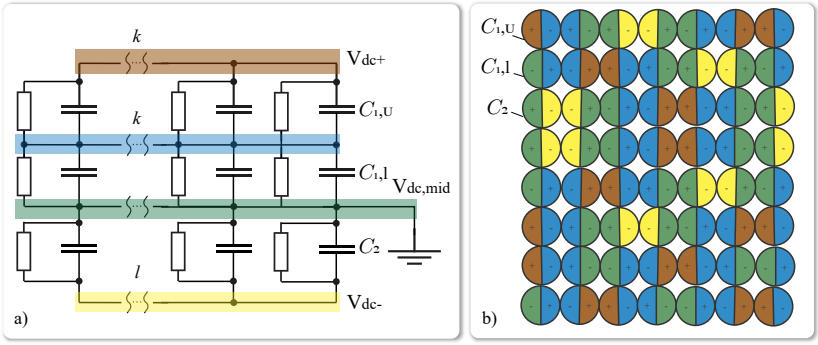

Figure 6.1: a) Schematic of the input capacitor bank with split DC-link, and two capacitors $C_{1,u}$, $C_{1,l}$ connected in series to form capacitor C_1. b). Schematic of the placement of the 56 electrolytic capacitors used in the development of the prototype input capacitor bank.

Essentially, the design of the input capacitor bank takes the form of an energy minimization problem, with constraints imposed by the maximum and minimum limits of the voltage levels. The problem can be formulated as in (6.1), where the voltage levels V_1 and V_2 are varying as a function of time, and t_p is the pulse length. Note that for the calculation of the energy of capacitor C_1 the initial voltage is used ($V_1(0)$), while for the energy of C_2 the voltage at the end of the pulse ($V_2(t_\mathrm{p})$) is used.

$$\min \quad f(C_1, C_2) = \frac{1}{2} \cdot C_1 \cdot V_1^2(0) + \frac{1}{2} \cdot C_2 \cdot V_2^2(t_\mathrm{p}) \tag{6.1a}$$

$$s.t. \quad V_1(t_\mathrm{p}) > 650\mathrm{V}, \text{for } u_\mathrm{c} = u_\mathrm{c,max} \tag{6.1b}$$

$$V_2(t_\mathrm{p}) < 100\mathrm{V}, \text{for } u_\mathrm{c} = u_\mathrm{c,min} \tag{6.1c}$$

$$V_1(t_\mathrm{p}) + V_2(t_\mathrm{p}) < 850\mathrm{V} \tag{6.1d}$$

Acting as constraints, V_1 should not be lower than 650V to allow for sufficient control margin, and V_2 should not exceed 100V. The total DC-link voltage should also never exceed 850V, in order to keep the semiconductor devices of the current shaping converter within their safe operating area. The worst case scenario for capacitance C_1 occurs for the maximum duty ratio, as the average discharge current is then

Table 6.1: Parameters of the optimum & the realized input capacitor bank.

Parameter	**Symbol**	**Value**
Optimum upper capacitance	$C_{1,\mathrm{opt}}$	130mF
Optimum lower capacitance	$C_{2,\mathrm{opt}}$	290mF
Min. upper level voltage	$V_{1,\mathrm{min}}$	658V
Max. lower level voltage	$V_{2,\mathrm{max}}$	97V
Total energy stored	$W_{\mathrm{in,opt}}$	38kJ
Realized upper capacitance	C_1	157mF
Realized lower capacitance	C_2	462mF
Total energy stored	W_in	59kJ
C_1 Part number		MAL250036153E3
C_2 Part number		MAL210242333E3

the highest, while the opposite is true for capacitance C_2. During the pulse however, the input voltage levels are changing, and therefore for a constant output voltage the duty cycle and as a result the average currents through the capacitors are also changing. Consequently the problem is solved in the time domain and the duty cycle and average currents are calculated for each time step.

The optimization result essentially gives the smallest $C_{1,\text{opt}}$ and $C_{2,\text{opt}}$ that do not violate the constraints in the two considered worst case scenarios. In reality, the availability of commercial capacitors, the need for increased design margins (e.g. $2\times$ 400V capacitors are used instead of $2\times$ 375V for C_1, for safety reasons) and the need to account for the tolerance in the capacitance value ($\pm 20\%$ according to the manufacturer [151]) leads to a significantly higher energy for the developed prototype. The optimization result, along with the prototype parameters are listed in Table 6.1.

Figure 6.1b shows the final placement of the 56 electrolytic capaci-

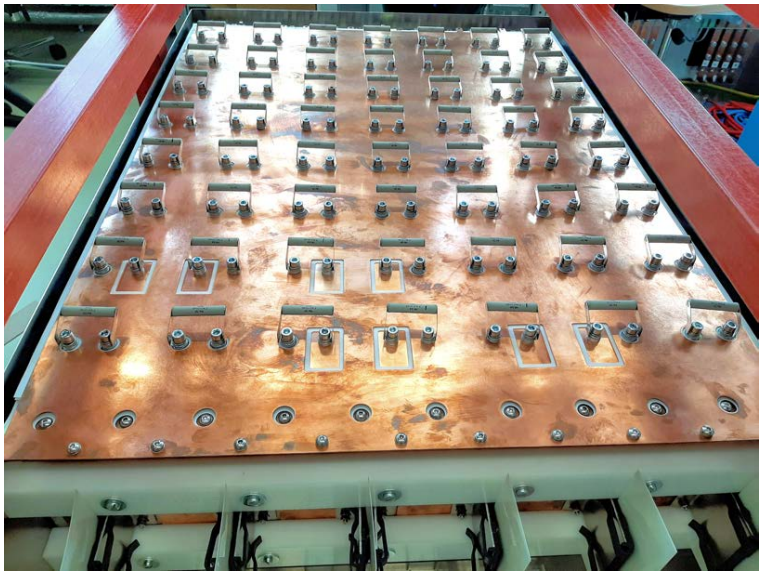

Figure 6.2: Assembled input capacitor bank of the DynACuSo consisting of 56 capacitors. Total dimensions: 620mm×847mm×230mm. Total stored energy: 59kJ.

tors forming the input capacitor bank. The different colors signify the different voltage levels, as also noted in Figure 6.1a. The capacitors are connected with wide, copper busbars with a thickness of 1mm, connected on top of each other, with a Mylar layer of 0.5mm thickness in between[2]. The assembled input capacitor bank is shown in Figure 6.2, where the balancing resistors are also visible.

6.2 Step Voltage Generator

The step voltage generator is connected in series with the current-shaping converter, as shown in Figure 2.1 and is responsible for generating a step-wise output voltage. The concept of the step voltage generator is essentially based on the Modular Multilevel Converter (MMC) with pre-charged capacitors. The capacitors are charged in parallel based on the Marx-generator concept. The step voltage generator is referred in the text as M3TC (Marx-type Modular Multilevel Converter).

The detailed topology of the M3TC stage is shown in Figure 6.3 and consists of the following main units:

- **Power module**: Conducts the total output current of the current-shaping converter and delivers a bipolar voltage at its output.
- **Energy storage unit**: Consists of a large film capacitor. The

[2]one copper busbar for each voltage level /color.

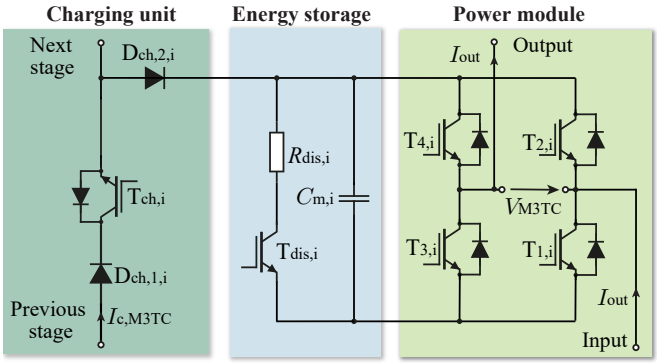

Figure 6.3: Detailed schematic of a single M3TC stage and its main parts.

first M3TC stage ($M3TC_1$) is charged to $0.5V_{st}$, while the upper stages ($M3TC_{2..9}$) are charged to V_{st} (nominal $V_{st} = 1.1kV$).

- **Charging unit**: Comprises semiconductor devices with low current rating, and ensures that all M3TC stages can be charged in parallel, regardless of their voltage level.

6.2.1 Power Module

During the last decade Modular Multilevel Converters (MMC) have made their way into industrial applications, especially in the field of HVDC. The main advantages of this topology is its modularity, its high quality output waveform and its inherent redundancy [152]. Due to the wide acceptance of the MMC topology, much of the research has focused on the investigation of different cell configurations, in order to make the most out of the topology. In [153], an exhaustive review of different MMC cell configurations has been conducted.

The UnACuSo, the predecessor of the DynACuSo, has been using half-bridge (HB) power modules, (Figure 6.4a), since a unipolar output voltage was sufficient [23]. However, based on the renewed specifications defined in Table 1.2, a bipolar output voltage is required in the new design, making the full bridge (FB) and the cross-connected (CC) configuration (Figures 6.4b&c) suitable candidates.

Figure 6.5 shows a comparison of different implementations of the M3TC in terms of their maximum voltage capabilities, and the conduction losses in by-pass mode at the rated current (1kA). It can be seen that the implementation with HB modules features the lowest losses, but does not fulfill the bipolar voltage requirement. Furthermore in

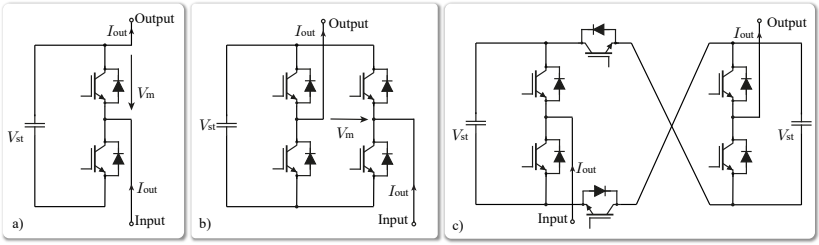

Figure 6.4: Power module configurations. a) Half-bridge (HB) module. b) Full-bridge (FB) module. c) Cross-connected (CC) module.

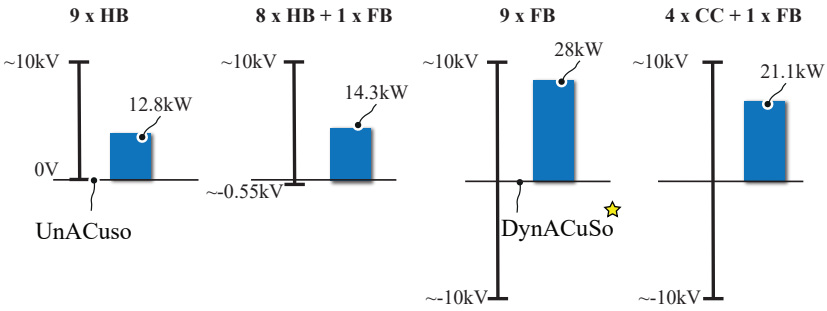

Figure 6.5: Comparison of the output voltage capabilities, and the conduction losses in by-pass mode, for different implementations of the step voltage generator.

many applications, a low negative voltage level of $0.5V_{\mathrm{st}}$(e.g. -550V) could be sufficient. In those cases, the $\mathrm{M3TC}_1$ stage can be designed as a FB module, while $\mathrm{M3TC}_{2..9}$ stages can be HB modules. In this case, the losses are only increased by 10% compared to the implementation with HB modules, as also deduced by Figure 6.5.

The case of CC modules can be of particular interest, since two of the $\mathrm{M3TC}_{2..9}$ stages could be combined into one, and 4 high voltage M3TC stages can be considered instead of 8. In this implementation $\mathrm{M3TC}_1$ is still a full-bridge module. All in all, the bipolar voltage requirements would be fulfilled and the losses could be reduced by 25% compared to the 9 FB modules implementation that is finally chosen for the DynACuSo. Nevertheless, the modularity of the system with the CC modules is reduced, and the control complexity is increased, compared to the FB configuration.

Figure 6.6 shows the current path, for a unidirectional (positive) current, in order for the FB module to deliver the three needed output voltage levels $\{V_{\mathrm{st}}, 0, -V_{\mathrm{st}}\}$. Regardless of the voltage level, there is always one IGBT switch, and one diode on the current path. This is a useful observation for the calculation of the stage losses that follows in Section 6.2.5. Additionally, it is evident, that all semiconductors need to block the total stage voltage and conduct the total output current.

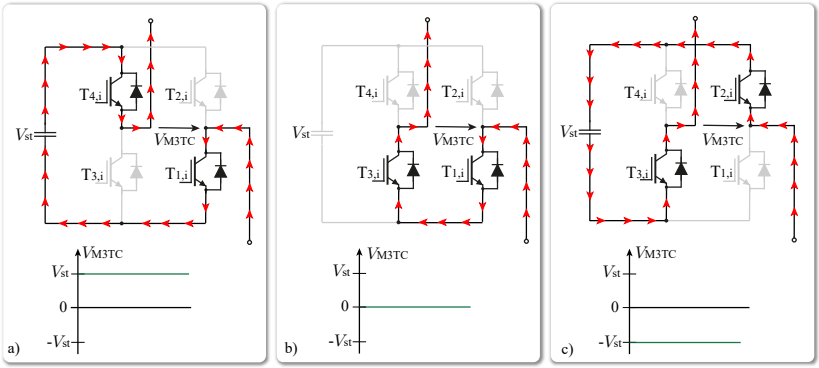

Figure 6.6: Power operation of the M3TC stage. a) Insert positive voltage. b) By-pass. c) Insert negative voltage.

6.2.2 Energy Storage Unit

The energy storage unit is an integral part of the M3TC stage, and in fact the largest in volume. Its volume is a significant part of the volume of the DynACuSo, and therefore it needs to be carefully selected. Furthermore, the energy storage unit defines the maximum capabilities of the source in terms of pulse length, at a given voltage level.

At first, based on the fundamental equations of the capacitor (6.2)-(6.5), it is relatively simple to derive (6.6), where it is shown that the capacitor volume is proportional to its energy content U. Moreover, the energy content is usually closely associated with the cost of the capacitor. As a result, minimizing the energy content would result in a minimization of not only the volume, but also the cost of the capacitor. In the following, V is the rated capacitor voltage, l is the length, A is the surface area, E_{br} is the breakdown electric field and Vol is the volume of the capacitor.

$$U = \frac{1}{2} \cdot C \cdot V^2 \quad (6.2) \qquad V = E_{\mathrm{br}} \cdot l \quad (6.3) \qquad Vol = A \cdot l \quad (6.4)$$

$$C = \epsilon \cdot \frac{A}{l} \quad (6.5) \qquad \rightarrow Vol = \frac{U}{\epsilon \cdot E_{\mathrm{br}}^2} \quad (6.6)$$

Since the rated voltage of the capacitor is chosen based on the needed modularity and availability of semiconductors (discussed in Chapter 2), only the capacitance value C_{m} and the capacitor technology are left to

be determined.

In general, aluminum electrolytic capacitors are widely applied in industrial applications, where a high volumetric efficiency (capacitance per unit volume) is needed. Commercially available aluminum electrolytic capacitors reach several Farads in capacitance value [154]. Furthermore, they have the highest energy density among standard technologies that often exceeds 700J/L [155].

On the other hand, electrolytic capacitors often suffer from increased parasitic resistance and inductance, which limits their applicability in several high-end applications. Additionally, their peak current rating is usually not specified by manufacturers. The voltage rating of commercially available electrolytic capacitors rarely exceeds 450Vdc. Consequently at least three electrolytic capacitors connected in series would be needed to form a DC-link of 1.1kV. This would lead to an increased implementation effort and impose additional challenges regarding their voltage balancing.

For pulsed current applications, film capacitors often constitute the preferred solution, due to their high rated peak current. Commercial film capacitors are available with high capacitance values in the mF range and voltage ratings in the kV range. Moreover, film capacitors have low parasitic inductance. and a lower parasitic resistance compared to electrolytic capacitors. These properties make them more suitable for applications where high performance is required. However, their energy density rarely exceeds 400J/L. Just as in the case of the UnACuSo, film capacitors is the chosen technology for the DynACuSo. A detailed investigation of the commercially available film capacitors can be found in [23].

In order to prevent irreversible material degradation, manufacturers often suggest as a rule of thumb, that capacitors should not be allowed to discharge to voltage levels lower than 60-70% of their initial voltage. This design limitation needs to be taken into consideration, in order to determine the minimum acceptable capacitance value. Figure 6.7 shows the maximum % voltage drop ΔV as a function of the capacitance value, for different pulse lengths, at the peak output current of 1.5kA. Two contour lines are plotted for total pulse length of 10ms and 20ms respectively. As noted on the graph, allowing the capacitor to discharge by 40% of its initial voltage (36% remaining of its initially stored energy) requires approximately 35mF of capacitance, while allowing it to discharge only by 20% requires at least 70mF of capacitance for a

10ms pulse at rated current. The calculations are based on equation (6.7), where t_p is the pulse flattop duration.

$$C_\mathrm{min} = I_\mathrm{out} \cdot \frac{t_\mathrm{p}}{\Delta V} \tag{6.7}$$

As capacitors are used as an energy storage unit in the M3TC, it is clear that the maximum output voltage (e.g 10.1kV when 9 M3TC stages are used), cannot be delivered throughout the pulse duration, since the stages are not charging continuously. In fact, the maximum output voltage that can be delivered to the load depends on the stage capacitance. Based on Figure 6.7, a good compromise between capacitance value (i.e. related to volume and cost) and voltage drop (i.e. related to capacitor lifetime) is to choose a capacitance of 35mF for the higher M3TC stages (at 1.1kV). For the first stage, the same energy content can be used for a similar performance, leading to a capacitance value of 140mF (at 0.55kV).

In Figure 6.8a, the maximum output voltage that can be supplied throughout a pulse by the source module, as a function of the output current and the pulse flattop duration is shown. It is highlighted, that with the aforementioned capacitance values, the maximum voltage that can be delivered throughout a 10ms pulse at the peak current is

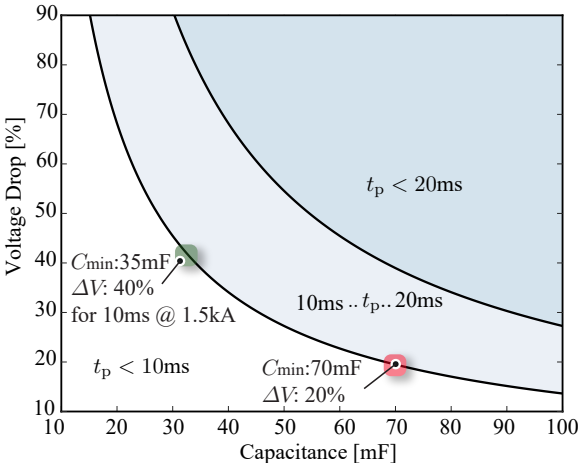

Figure 6.7: Pulse flattop duration with peak output current of 1.5kA, as a function of the stage capacitance and the voltage drop.

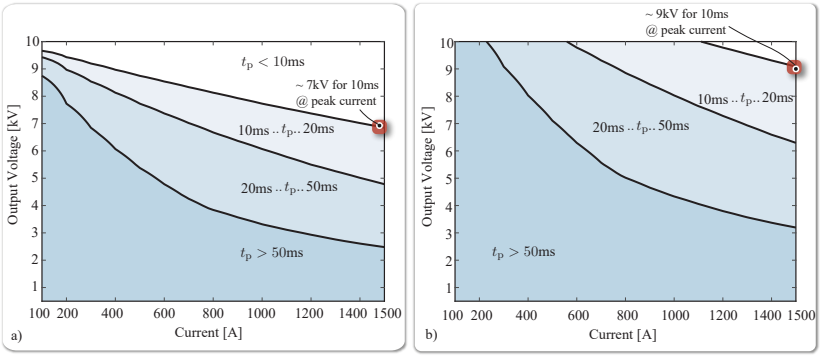

Figure 6.8: Maximum output voltage of a source module as a function of the output current and the pulse flattop duration: a) A total of 9 M3TC stages installed (no redundancy). b) A total of 12 M3TC stages installed (3 redundant stages).

approximately 7kV. It is evident that in order for the source to extend its output voltage region, either a higher capacitance value per stage needs to be selected, or redundant stages need to be included in the design.

Figure 6.8b, shows the maximum output voltage that can be supplied throughout a pulse by the source module, if 3 redundant 1.1kV

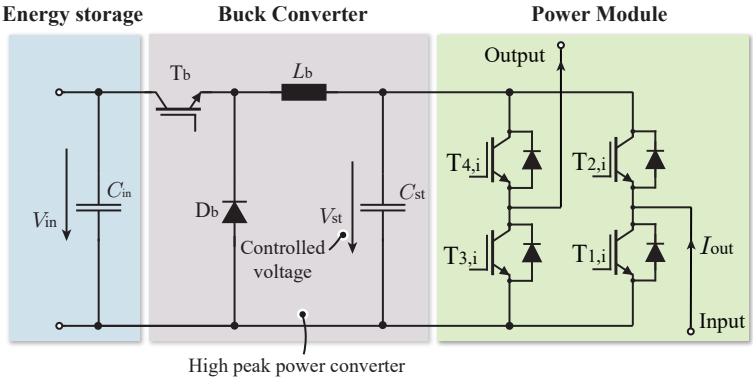

Figure 6.9: Schematic of the M3TC stage with a buck converter controlling the stage voltage. This concept is not followed in this work.

M3TC stages are included in the design (i.e. in total 12 M3TC stages). It can be seen that due to the inclusion of the redundant stages, 9kV of output voltage can be supplied for 10ms, at the peak output current.

When high output voltage is needed throughout the pulse duration, instead of using redundant stages to compensate the voltage droop, a converter (e.g. buck, boost etc.) can be employed between the energy storage capacitor and the power module, as illustrated in Figure 6.9. In this way, the converter's output voltage can be controlled, and the droop can be compensated. However, the converter needs to handle the peak output power of the stage module (1.1kV and 1.5kA), and therefore the complexity of the system is dramatically increased. Due to the added cost and complexity, this option is not investigated further. The basic concept is simply included here for completeness and future reference.

6.2.3 Charging Unit

The charging procedure of the M3TC is based on the principle of the Marx-generator. When the system is in operation, the charging unit needs to block a bipolar output voltage. When the system needs to recharge (after the pulse), it needs to connect the capacitors in parallel, while disconnecting the load [156].

For a unipolar output voltage, as in the case of the UnACuSo, a single diode is sufficient for charging the upper stage capacitors in parallel, as shown in Figure 6.10a essentially forming a solid-state Marx generator. The diodes then need to block the full output voltage, and therefore they need to have the same voltage rating as the IGBTs of the power module. The current path during charging is also depicted in Figure 6.10a with red arrows.

After charging the higher stages of the M3TC, the charging of the first stage of the M3TC can take place by turning on the respective charging switch. The supply voltage is set to 0.55kV, the diodes are blocking and the current path is depicted with blue arrows in Figure 6.10a.

The topology of Figure 6.10a cannot block a bipolar voltage at the output, and therefore another diode needs to be inserted, in series and in the opposite direction. To make the charging still possible, an IGBT switch ($T_{ch,i}$) is simply added, with an anti-parallel diode as shown in Figure 6.10b. The switch $T_{ch,i}$ is then also used to control the charging

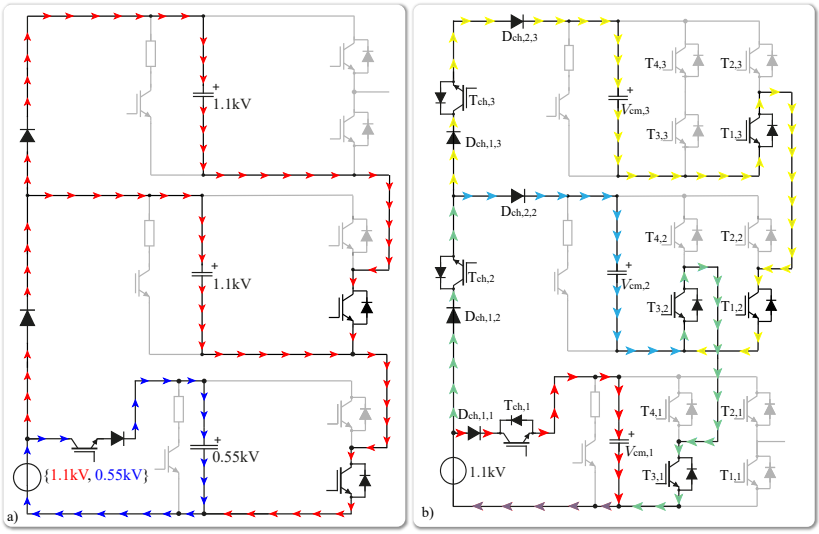

Figure 6.10: Charging operation of the M3TC stage. a) Marx-generator concept of the UnACuSo . b) Enhanced Marx-based charging topology of the step voltage generator of the DynACuSo.

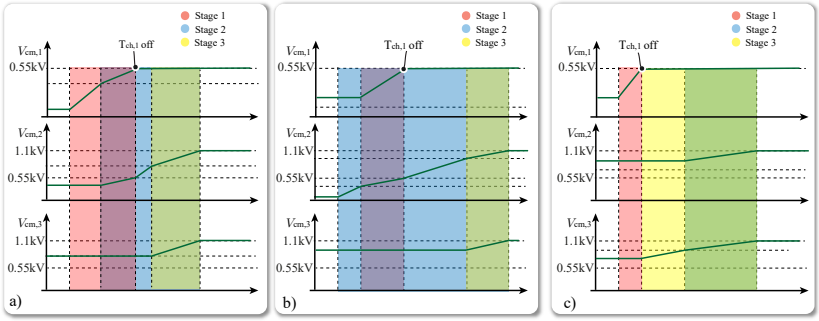

Figure 6.11: Exemplary charging of the M3TC, with three different scenarios depending on the initial voltages of the M3TC stages.

process, and can be used to charge $M3TC_1$ in parallel with $M3TC_{2..9}$. The voltage of $M3TC_1$ can then be sensed and switch $T_{ch,1}$ can be turned off, when it reaches 0.55kV, while the rest of the stages can continue to charge till the target 1.1kV voltage is reached.

Furthermore, the conventional topology of Figure 6.10a requires all higher M3TC stages to have a voltage level equal or higher than the lower ones. If this is not the case, then the diode would conduct and connect two capacitors with different voltages in parallel. Since there is no current limiting device in the conduction path, the diodes would be destroyed by the high current. This is not a problem in the case of UnACuSo since the modulation that is used, ensures that higher M3TC stages are always charged to a higher level [23]. Nevertheless, this particularity reduces the flexibility of the control of the M3TC, and does not allow a targeted selection of the M3TC stages based on their voltage level. To bypass this problem and enable the higher stage capacitors to hold a lower voltage level compared to the lower ones, an additional diode is inserted ($D_{ch,2,i}$), as shown in Figure 6.10b.

Figure 6.11 shows three exemplary charging scenarios, based on the initial voltages of the three stages of the M3TC. All devices in these scenarios are assumed to be ideal. In Figure 6.11a initially the system starts from $V_{cm,1} < V_{cm,2} < V_{cm,3}$, which is also a feasible case for the topology in Figure 6.10a. In this case, the charging power supply can be directly set to current control mode with a maximum voltage of 1.1kV and all the charging IGBTs $T_{ch,i}$ are turned on to start the charging procedure. $M3TC_1$ has the lowest voltage so it starts charging first, while diode $D_{ch,1,2}$ is blocking (red area). When $V_{cm,1} = V_{cm,2}$, diode $D_{ch,1,2}$ starts conducting, and stages 1 and 2 are charging in parallel (purple area).

When $V_{cm,1}$=550V, $T_{ch,1}$ is turned off and the $M3TC_1$ stops charging, while $M3TC_2$ continues to charge, until $V_{cm,2} = V_{cm,3}$ (blue area). Afterwards, diode $D_{ch,1,3}$ starts conducting and stages $M3TC_2$ and $M3TC_3$ are charging together, until the full voltage is reached.

In Figure 6.11b, the system starts charging from an initial position where: $V_{cm,2} < V_{cm,1} < V_{cm,3}$. Similarly, the charging power supply can be directly set to current control mode with a maximum voltage of 1.1kV and all the charging IGBTs $T_{ch,i}$ are turned on. In this case, diode $D_{ch,1,1}$ is reverse biased and diode $D_{ch,1,2}$ is conducting. As a result, only $M3TC_2$ is charging (blue area). As soon as $V_{cm,1} = V_{cm,2}$, diode $D_{ch,1,1}$ starts conducting too, and $M3TC_1$ and $M3TC_2$ are charging in parallel (purple area).

As in the previous example when $V_{cm,1}$=550V, $T_{ch,1}$ is turned off and $M3TC_2$ continues to charge (blue area). Just as in the scenario of Figure 6.11a, when $V_{cm,2} = V_{cm,3}$, diode $D_{ch,1,3}$ starts conducting

and $M3TC_2$ and $M3TC_3$ are charging together, until the full voltage is reached.

Finally in Figure 6.11c, the system starts charging from an initial position where: $V_{cm,1}<V_{cm,3}<V_{cm,2}$. Initially, $M3TC_1$ is charging (red area) until it reaches 550V, when switch $T_{ch,i}$ is turned off. At the same time instant, the power supply which is in constant current mode, will forward bias diodes $D_{ch,1,2}$ and $D_{ch,1,3}$. However, diode $D_{ch,2,2}$ is blocking since $V_{cm,2}>V_{cm,3}$ and therefore, only stage 3 is charging (yellow area). As soon as $V_{cm,2}=V_{cm,3}$, diode $D_{ch,2,2}$ becomes forward biased, and stages $M3TC_2$ and $M3TC_3$ are charging in parallel.

It can be concluded that the topology of Figure 6.10b, allows to recharge the system under all possible initial conditions of the capacitor voltages, and therefore allows for an increased flexibility in the control of the step voltage generator, compared to the charging topology of 6.10a. Clearly however, the aforementioned improvements come at the cost of increased circuit complexity, and an increased number of semiconductor devices. Nevertheless, devices with standard ratings can be used for the charging unit's semiconductors, and their contribution to the overall system cost is essentially negligible.

6.2.4 Converter Design

Based on the described operation principle, the needed semiconductor ratings are derived in Table 6.2. Index i indicates the higher M3TC

Table 6.2: Minimum ratings of semiconductor devices of the M3TC stage.

	Maximum Voltage	**Voltage Class**	**Current (RMS)**	**Current (Peak)**
$T_{k,1}$	550V	1200V	1000A	1500A
$T_{ch,1}$	550V	1200V	-	-
$D_{ch,1}$	550V	1200V	-	-
$T_{dis,1}$	550V	1200V	-	-
$T_{k,i}$	1100V	1700V	1000A	1500A
$T_{ch,i}$	1100V	1700V	-	-
$D_{ch,i}$	1100V	1700V	-	-
$T_{dis,i}$	1100V	1700V	-	-

stages (i=2..9) and index k indicates the switch number in the power module (k=1..4). The current ratings of the charging unit depend on the external power supply and the minimum RMS current values for these devices depend on the needed pulse repetition rate. Nevertheless they have relatively low current ratings, and they are not further discussed. This section focuses on the thermal design of the power module.

In the following, the loss model for the IGBT switches is shortly revised and the thermal models used for the calculation of the maximum expected junction temperature in the continuous and the pulsed mode of operation are discussed. Finally, a small section is dedicated to the calculation of the thermal resistance of the cold-plate.

a. IGBT Loss Model

A datasheet-based approach is used in order to calculate the power losses of the switches $T_{1,i}..T_{4,i}$ and their anti-parallel diodes. For the conduction losses, both the IGBT and the diode are modeled as a DC voltage source, that represents the forward voltage drop ($V_{\mathrm{on,T}}$, $V_{\mathrm{on,D}}$) connected in series with an on-state resistance ($R_{\mathrm{on,T}}$, $R_{\mathrm{on,D}}$). The average conduction losses are then given by (6.8)-(6.9). The forward voltage drop and the resistance are both temperature dependent but in a conservative approach, the worst case losses can be assumed (maximum operating temperature of 150°C).

$$P_{\mathrm{c,T}} = V_{\mathrm{on,T}} \cdot I_{\mathrm{avg}} + R_{\mathrm{on,T}} \cdot I_{\mathrm{RMS}}^2 \tag{6.8}$$

$$P_{\mathrm{c,D}} = V_{\mathrm{on,D}} \cdot I_{\mathrm{avg}} + R_{\mathrm{on,D}} \cdot I_{\mathrm{RMS}}^2 \tag{6.9}$$

For the extraction of the switching losses, look-up tables are used based on the datasheet. Since in the datasheet the switching conditions often do not match the application switching conditions (in terms of DC voltage, gate resistance and parasitics), linear scaling can be assumed when the relevant information is missing. The switching losses are then simply the product of the switching energy and the switching frequency.

In the continuous operation mode, the M3TC stages are simply by-passed, and therefore only conduction losses are present. However, in pulse mode with dynamic loads, the M3TC stages often need to switch several times within the pulse duration, and therefore significant switching losses can be expected. The switching losses are calculated based on (6.10) and (6.11), where E_{on} and E_{off} is the turn-on and turn-off switching energy of the IGBT respectively, and E_{rr} is the reverse recovery loss of the diode. The total losses for each semiconductor are

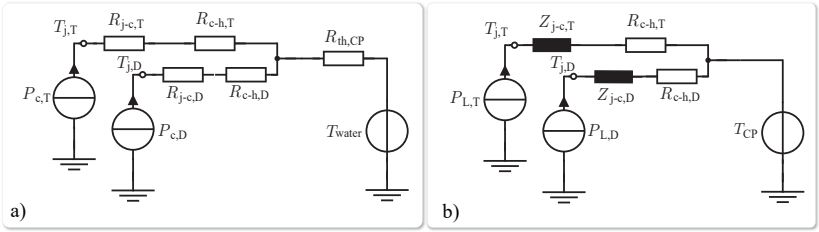

Figure 6.12: Thermal model for the semiconductor devices of the M3TC. a) Steady state model in continuous mode of operation. b) Transient thermal model in pulsed mode of operation.

then defined in (6.12) and (6.13).

$$P_{\mathrm{sw,T}} = f_{\mathrm{sw}} \cdot (E_{\mathrm{on}} + E_{\mathrm{off}}) \quad (6.10) \qquad P_{\mathrm{sw,D}} = f_{\mathrm{sw}} \cdot E_{\mathrm{rr}} \quad (6.11)$$

$$P_{\mathrm{L,T}} = P_{\mathrm{c,T}} + P_{\mathrm{sw,T}} \quad (6.12) \qquad P_{\mathrm{L,D}} = P_{\mathrm{c,D}} + P_{\mathrm{sw,D}} \quad (6.13)$$

b. Thermal Model

Since the operation profile of the M3TC is different in continuous mode compared to pulsed mode, the thermal performance of the semiconductor devices needs to be examined in both modes. Generally, in pulsed power systems, apart from the maximum junction temperature that should not exceed the absolute maximum operating temperature of the device $T_{\mathrm{j,max}}$, care must be taken regarding the maximum temperature difference ΔT_{j} due to the temperature cycles [71]. A high temperature difference ΔT_{j} between pulses can cause faster device ageing, reduce its reliability and lifetime [72], [73].

Figure 6.12a shows the steady state thermal model that can be used for the extraction of the maximum expected junction temperature in continuous operation mode. The power losses in this case include simply the conduction losses of the IGBT and the diode, and assuming that the thermal resistances of the model are known, the maximum junction temperature of the device can be estimated based on (6.14). Index s is used to signify either the index D of the diode or T of the IGBT. The steady state thermal resistances can usually be found in the datasheet.

$$T_{\mathrm{j,s}} = T_{\mathrm{water}} + (P_{\mathrm{c,T}} + P_{\mathrm{c,D}}) \cdot R_{\mathrm{th,CP}} + P_{\mathrm{c,s}} \cdot (R_{\mathrm{j\text{-}c,s}} + R_{\mathrm{c\text{-}h,s}}) \quad (6.14)$$

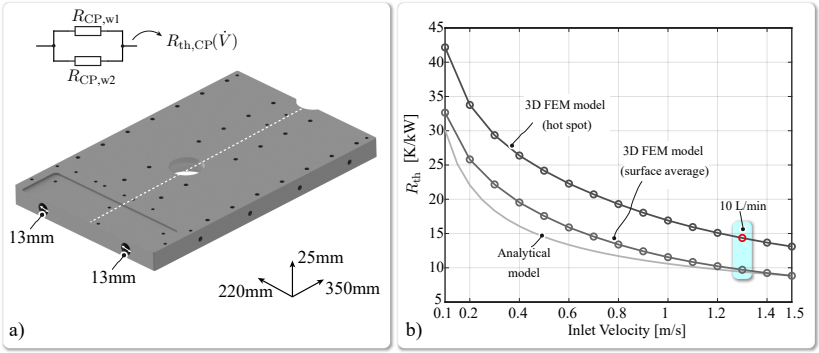

Figure 6.13: Modelling of the cold-plate of the M3TC stage. a) Cold-plate geometry. b) Cold-plate thermal resistance R_{th} as a function of the input water flow, calculated analytically based on the cold-plate model of Section 3.4.3 and numerically with FEM simulations.

Figure 6.12b shows the transient thermal model that can be used for the estimation of the maximum junction temperature swing ΔT_{j}, during the pulsed mode of operation. Due to the relatively short duration of the pulse transient (less than 10ms) the temperature of the module's case can be considered constant, since the cold-plate's thermal capacitance is large. In the model of Figure 6.12b the thermal resistance of the thermal paste ($R_{\text{c-h}}$) is assumed to have a negligible thermal capacitance, due to its negligible dimensions [74]. The junction temperature swing can then be calculated based on (6.15). During the pulse, the thermal impedance $Z_{\text{j-c,s}}$ is a function of the time, and it is given by the manufacturer's datasheet.

$$\Delta T_{\text{j,s}} = T_{\text{j,s}} - T_{\text{CP}} = P_{\text{L,s}} \cdot (Z_{\text{j-c,s}}(t) + R_{\text{c-h,s}}) \tag{6.15}$$

c. Cold-Plate Model

Due to the high current rating of the IGBTs, the selection of semiconductor devices, which are commercially available for these power ratings, is fairly limited. After a preliminary study, the PrimePACK modules from Infineon are pre-selected for the M3TC stage, as a single module can be used, and connecting multiple devices in parallel can be avoided [157, 158]. Each module consists of a half-bridge and therefore two modules need to be used per stage. The modules are relatively

large and they define the minimum dimensions of the cold-plate that can be designed, including some margins for the additional lower power electronics of the stage.

A CAD model of the cold-plate can be seen in Figure 6.13a. The aluminum cold-plate simply consists of two parallel water channels, each of them used directly under the IGBT module. The cold-plate is low cost and easy to construct and its dimensions are noted in Figure 6.13a. The symmetrical design of the cold-plate, allows each water channel to be studied individually. The total thermal resistance $R_{\text{th,CP}}$ can then be calculated as the parallel combination of the two symmetrical halves. Figure 6.13b depicts the cold-plate's total thermal resistance, as a function of the inlet water velocity, calculated with the analytical model described in Section 3.4.3, and compared to the 3D numerical FEM model of the cold-plate. The graph shows the $R_{\text{th,CP}}$ calculated with FEM, not only based on the average surface temperature of the cold-plate, but also based on the maximum hot-spot of the cold-plate. It can be observed that as expected, the analytical model is closer to the surface average FEM model and its accuracy is increased for higher inlet water velocities[3].

6.2.5 Prototype M3TC Stage

The part numbers of all the major components that are used in the M3TC prototype system are listed in Table 6.3. The choice of discharge resistance value for $\text{R}_{\text{dis,i}}$ constitutes a trade-off between the resistor RMS power rating during a full discharge and the discharge times. With the chosen values the first stage $\text{C}_{\text{m,1}}$ discharges in approximately 240s, while the upper M3TC stages $\text{C}_{\text{m,2..9}}$ in approximately 180s. The RMS power during the discharge time is for $\text{R}_{\text{dis,1}}$ 100W and 90W for $\text{R}_{\text{dis,2..9}}$. The actual RMS power of the discharge resistors is lower than the RMS power during the discharge procedure. As shown in Table 6.3, identical components are selected for the charging unit of the first and the higher stages for simplicity.

Figure 6.14 shows the complete M3TC stage prototype and its dimensions. It can be seen that the energy storage unit is by far the largest component, and dominates the volume of the stage. The design of the stage allows the M3TC module to be simply disconnected

[3]similar observations were made in section 3.4.3 regarding the cold-plate of the current-shaping converter.

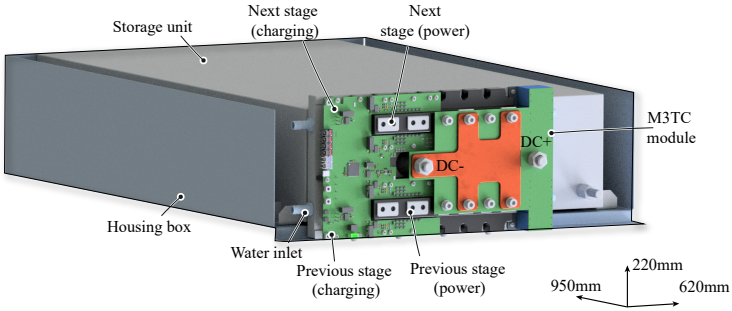

Figure 6.14: CAD design of the prototype M3TC stage, with the power module mounted on the energy storage capacitor.

from the capacitor, for an easier disassembly in case of failure. The power module connections and charging unit connections to the next and previous stages are shown also in the illustration.

Figure 6.15 shows the developed prototype M3TC module. The two power module IGBTs are mounted on the cold-plate and they are connected via busbars with a thickness of 2mm. Apart from the main board that is shown in more detail in Figure 6.16, a second board is used to mount the commutation capacitors close to the power modules. In this way, a lower parasitic inductance design is achieved improving the

Table 6.3: Part numbers of the prototype M3TC stage.

Symbol	Ratings	Manufacturer	Part Number
$T_{j,1}$	1.2kV - 1.8kA	Infineon	FF1800R12IE5P
$C_{m,1}$	550V - 140mF	Electronicon	E56 series
$R_{dis,1}$	1kΩ - 200W	Ohmite	TGHLV1K00JE
$T_{j,i}$	1.7kV - 1.8kA	Infineon	FF1800R17IP5P
$C_{m,i}$	1100V - 36mF	Electronicon	E56 series
$R_{dis,i}$	2x1kΩ - 200W	Ohmite	TGHLV1K00JE
$T_{ch,i}$	1.7kV - 40A	IXYS	IXBH42N170
$D_{ch,i}$	1.8kV - 60A	IXYS	DH60-18A
$T_{dis,i}$	1.7kV - 40A	IXYS	IXBH42N170

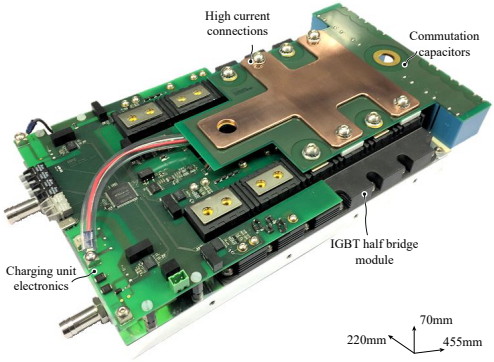

Figure 6.15: Picture of the developed M3TC module, containing the power module as well as the charging unit electronics. Total dimensions: 220mm x 70mm x 455mm

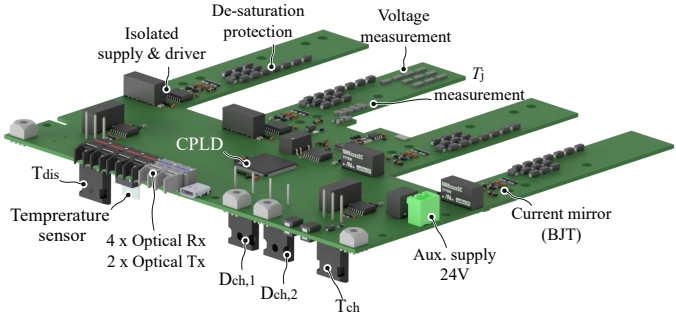

Figure 6.16: Main board of the M3TC stage, containing the CPLD for local control, communication interfaces and gate drivers for all the power module and charging unit switches.

switching performance of the M3TC stage, and enabling faster switching speeds.

The main board of the M3TC stage is shown in Figure 6.16. The main board is responsible for driving the switches of the M3TC stage and communicating with the master controller. For communication, four optical receivers and two optical transmitters are used, and a local CPLD is responsible for the local control. Each switch is driven by an isolated gate driver, and an isolated power supply is supplying

Table 6.4: Parameters of the thermal model of the prototype M3TC stages.

Symbol	$T_{k,1}$	$D_{k,1}$	$T_{k,2..9}$	$D_{k,2..9}$
V_{on}	0.85V	0.85V	0.9V	0.85V
R_{on}	0.57mΩ	0.58mΩ	0.81mΩ	0.58mΩ
$R_{j\text{-}c}$	17K/kW	28K/kW	15K/kW	30K/kW
$R_{c\text{-}h}$	11.5K/kW	13K/kW	12K/kW	14K/kW
T_{water}				20°C
$R_{th,CP}$				15K/kW
P_c@1kA	1.42kW	1.43kW	1.73kW	1.43kW
T_j@1kA	106°C	125°C	115°C	131°C

each gate driver. Furthermore, to increase the switching speed of the IGBTs, a current mirror is used, to boost the gate current for the IGBTs of the power module $T_{1..4}$ [96]. For over-current protection, a de-saturation circuit is used, together with the gate driver IC. By placing 13 de-saturation diodes, the circuit can detect an over-current of approximately 2kA and keep the power modules well within their operating region. When an over-current is detected, the gate driver IC sends within 1.5µs a fault signal to the CPLD [97].

Additionally, the main board includes a voltage measurement of the stage's capacitor voltage, This is used by the master controller for control purposes. Moreover, the junction temperature is measured, utilizing one of the NTC sensors that is available inside the IGBT modules. An additional temperature sensor in a TO-247 package is used to sense the cold-plate's temperature.

a. Thermal Limits

In this section, the thermal limits of the prototype system are explored, based on the models that were established in Section 6.2.4. The parameters used in the calculations are listed in Table 6.4.

At first, Figure 6.17a shows the maximum expected junction temperature of the power devices of the M3TC module in continuous operation. The solid lines are used for the upper stages ($M3TC_{2..9}$), and the dotted lines for the first M3TC stage ($M3TC_1$). The black lines are used for the IGBTs and the gray ones for the diodes. As shown in Figure 6.12a, the continuous operation mode considers only the con-

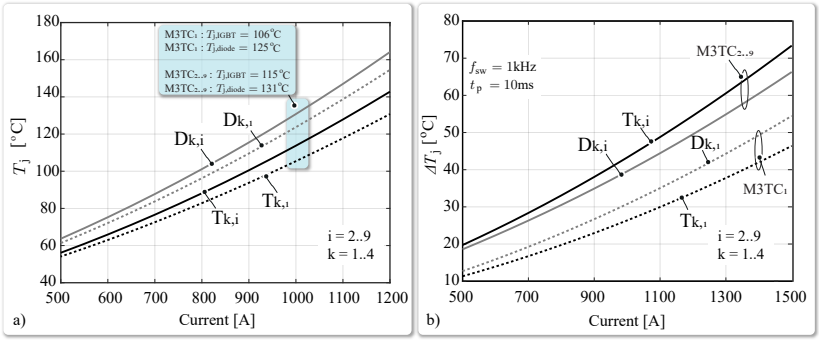

Figure 6.17: a) Thermal performance of the prototype M3TC stage in continuous operation. b) Thermal performance of the prototype M3TC stage in pulsed operation, assuming an effective switching frequency of 1kHz.

duction losses of the M3TC and does not account for any switching losses. The worst case thermal resistance of the cold-plate is assumed, extracted based on the hot-spot of the 3D-FEM model for a flow of 10L/min, as highlighted in Figure 6.13b. The diodes appear to have a higher expected junction temperature due to their higher $R_{\text{j-c}}$.

Similarly, the model of Figure 6.12b is used in order to determine ΔT_{j} in pulsed operation mode. Figure 6.17b depicts the expected temperature rise of the semiconductors of the prototype M3TC stages for a pulse of 10ms, assuming an effective switching frequency of 1kHz. The transient thermal impedance and the switching loss models are extracted from the datasheet of the devices [157], [158]. It can be observed, that even though the pulse is relatively short and the thermal transient impedance is not settled at its steady state value, the increased losses due to the switching actions, and the elevated current of 1.5kA, cause a significant ΔT_{j}, especially in the semiconductors of the upper stages ($\text{M3TC}_{2..9}$). In contrast, the maximum expected ΔT_{j} of the first stage barely exceeds 50°C, for the rated pulsed current.

It should be highlighted that when DynACuSo is operating with well known loads, the effective switching frequency of all the stages is not expected to exceed the 1kHz case, which is taken as a reference hereby. Nevertheless, when dynamic loads are connected to the output care should be taken, in order to not exceed the absolute maximum junction temperature, and to avoid high temperature swing cycles, that

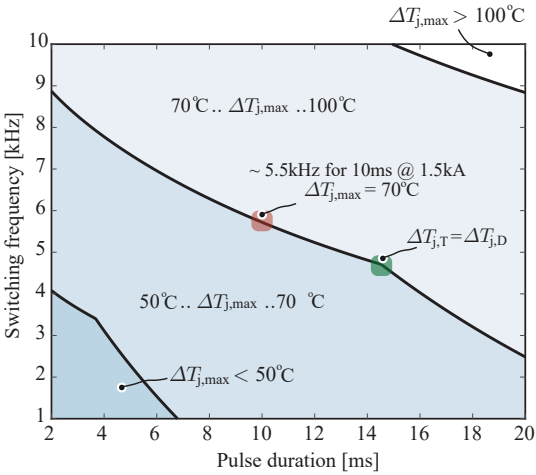

Figure 6.18: Maximum temperature swing of the semiconductor devices of $M3TC_1$ during a 1.5kA current pulse, as a function of the pulse duration and the switching frequency The contour lines for a $\Delta T_{j,max}$ of 50°C, 70°C and 100°C are plotted.

may limit the lifetime of the semiconductors. Especially for the cases of dynamic loads, the thermal design limitations of $M3TC_1$ are further investigated hereby, since especially the effective switching frequency of $M3TC_1$ can be significantly higher than $M3TC_{2..9}$, simply due to the operation principle of DynACuSo.

Figure 6.18 shows the maximum expected temperature rise of the semiconductors of $M3TC_1$ (max. of diode and IGBT) as a function of effective switching frequency and the pulse duration. The highlighted discontinuity (green point) arises from the fact that for higher switching frequency, the IGBT becomes the limiting semiconductor due to the increased switching losses while for longer pulse duration, the diode becomes the limiting device, due to the higher thermal resistance. It can be observed that frequencies above 10kHz, should be avoided even for short pulse duration, as they can lead to either high junction temperatures $T_{j,max}$ (depending on the starting case temperature before the pulse) that can destroy the devices, or high temperature swings $\Delta T_{j,max}$ that can severely limit the lifetime of the devices. It should also be noted that in pulsed mode of operation, the measurement of the junction tem-

perature based on the installed NTC sensor is not valid, since the time constant of the temperature sensor is relatively slow. Therefore, based on these findings a switching frequency limitation needs to be implemented for the switching actions of the M3TC stages, when feeding dynamic loads regardless of the junction temperature measurement.

b. Local Stage Control

Each M3TC stage is equipped with a local CPLD, in order to facilitate its control and reduce the amount of the needed communication links. Based on the information transmitted by the master controller (4 optical links for receivers), the CPLD generates the switching actions of the 6 IGBT switches of the stage.

More specifically, one optical receiver is used for the master controller's clock, which is needed for the synchronization of the source module. The same clock is distributed to all the slaves, including the current measurement board of the current shaping converter and all the M3TC stages. Furthermore, two receivers are used for the status of the power semiconductors (one for each half-bridge). Those signals are generated in the master controller and the CPLD is simply responsible for generating the complementary signals, and ensure the needed interlocking time. Additionally, the final optical receiver is used to inform the M3TC stage regarding the mode of operation of the DynACuSo.

As part of this project, a novel intensity modulation strategy suitable for isolated high speed multi-channel data transmission was investigated, designed, and developed. Its results have been presented in [44–46]. The proposed technique enables the use of a single fiber in order to transmit two data channels and their respective clock. In this way, a single optical fiber can be used instead of three, and the communication interface can be greatly reduced, without any loss of bandwidth. Experimental results have shown that the link is able to transmit data reliably with frequencies in the order of 100MHz, which is suitable for the vast majority of power electronic applications. For simplicity, this technique was not used in the M3TC stage, despite its benefits.

As previously discussed the M3TC stage has three main operating modes (operation, charging and discharging). A basic state machine is implemented in the local CPLD, shown in Figure 6.19. The variable 'Mode' is a 4-bit input that determines the operation mode of the stage, which in turn determines the status of the stage switches. In the case of

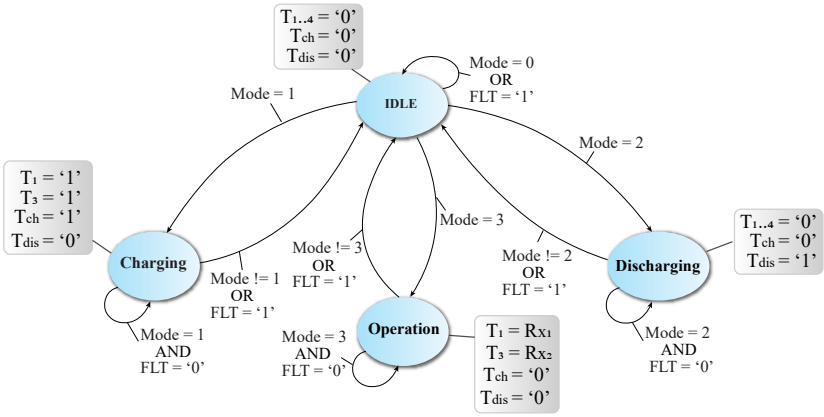

Figure 6.19: State machine implemented on the local CPLD for the control of the M3TC stage. The status of M3TC stage switches is also noted.

a fault, the state machine returns directly to the IDLE state and sends feedback to the master controller. When the state machine is in operation mode, the status of the switches T_1 and T_3 is directly determined by the two corresponding receivers R_{x1} and R_{x2}. The switches T_2 and T_4 are the complementary of T_1 and T_3 respectively, and interlocking time is also added, when there is a transition.

Regarding the two optical transmitters, the CPLD of each stage sends to the master controller the voltage measurement of the stage capacitor which is needed for control purposes (see Section 6.3), and feedback for any possible faults. A dedicated optical fiber is used for the transmission of the fault signal, in order to minimize the reaction time of the source module to a fault condition. The temperature measurements and the feedback of the gate drivers (desaturation faults) are only used locally, and can trigger possible faults if the temperature thresholds are exceeded.

c. Verification Measurements

In order to validate the design of the M3TC module, several measurements are presented here. Initially, Figure 6.20 shows single pulse tests with the nominal ratings of the 1.2kV power device used in $M3TC_1$ and the 1.7kV device used in $M3TC_{2..9}$. The figures verify that the power modules operate well within their safe operating area, with suf-

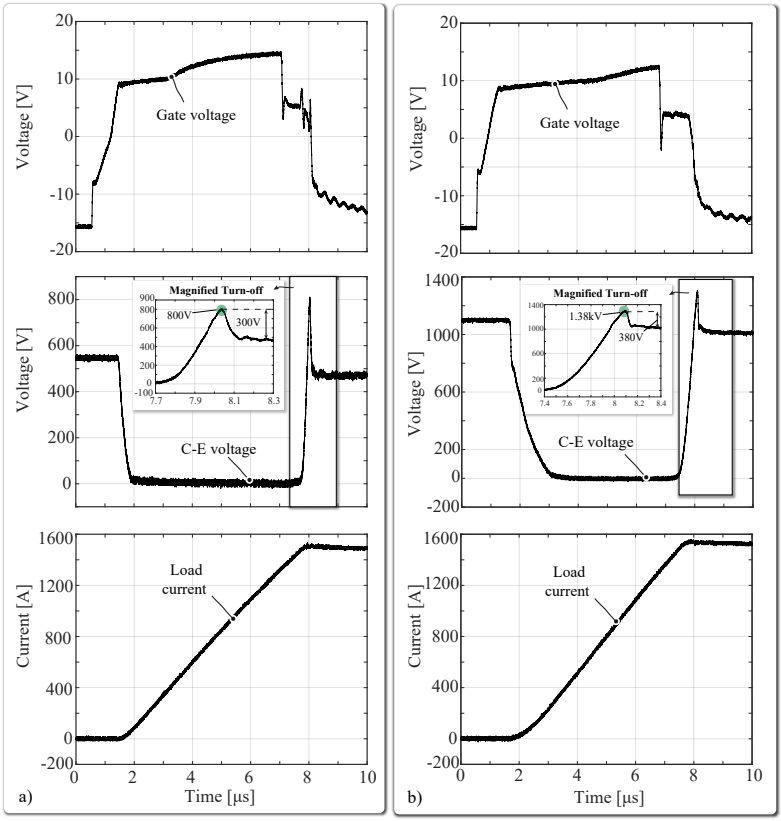

Figure 6.20: a) Single pulse test (550V - 1.5kA) of the 1.2kV power module. b) Single pulse test (1.1kV - 1.5kA) of the 1.7kV power module.

ficient margin. The low overshoot observed in both cases (800V and 1.38kV respectively) is a result of the low parasitic inductance design, which helps to improve the switching performance. Furthermore, only insignificant oscillations are noticed, and a relatively clean switching is achieved.

Figure 6.21 shows a comparison of the switching behavior of the 1.2kV and the 1.7kV switch. It can be seen that both the turn off and the turn on procedure of the 1.7kV device are significantly slower. For a better synchronization between switching actions of multiple M3TC

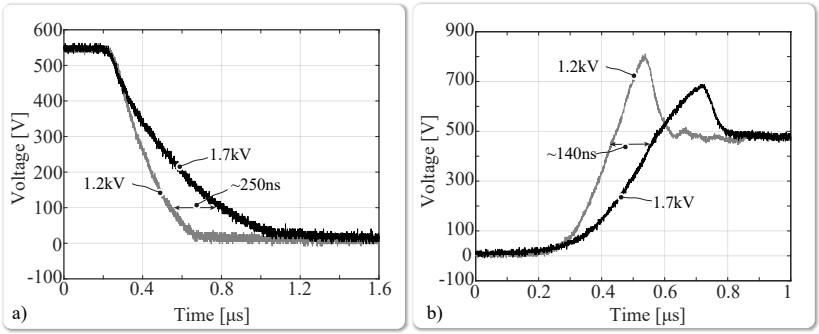

Figure 6.21: Comparison of the collector-emitter voltage of the 1.2kV and the 1.7kV device. a) Turn-on under zero current. b) Turn-off with 1.5kA and 550V.

stages, and in order to avoid possible disturbances in the output voltage due to the mismatch of the switching procedure, the noted delays (250µs and 140µs) can be compensated during the firmware design. The commutation process is explained in Section 6.3.

6.3 Control Integration of the M3TC

In the following, the control integration of the M3TC into the existing control scheme of the current shaping converter is discussed. The operation principle of the DynACuSo, under various scenarios and loads, has been described in Chapter 2. When the current shaping converter is not operating autonomously, and the system is equipped with a step voltage generator (M3TC), the controllers presented in Chapter 4 do not suffice to ensure a proper system operation. This section considers the integration of the M3TC's state machine only in the proposed adaptive hybrid controller.

The topology of DynACuSo with two integrated M3TC stages is shown for reference in Figure 6.22. The schematic includes only the electronics which process the high power, and excludes the charging interfaces for clarity.

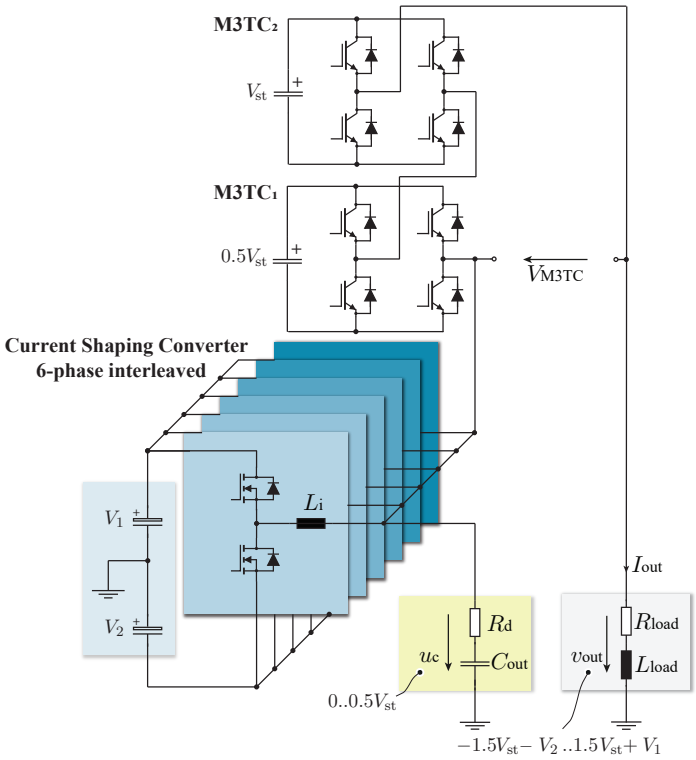

Figure 6.22: Schematic of the DynACuSo with two integrated M3TC stages. Only the power parts are included for simplicity, while the charging electronics/interfaces are not shown.

6.3.1 Normal Operation: Non-Step Transients

The operation of the M3TC state machine is shown in detail in Figure 6.24, for a step voltage generator with 2 stages and is essentially split into two parts. The normal operation, where the DynACuSo follows either non-step transients or flattops noted in light blue[4], and the dynamic operation noted in light red, where DynACuSo reacts in step transients, facilitated by the M3TC[5].

[4] operation shown in principle in Figures 2.3 & 2.4.
[5] operation shown in principle in Figure 2.5.

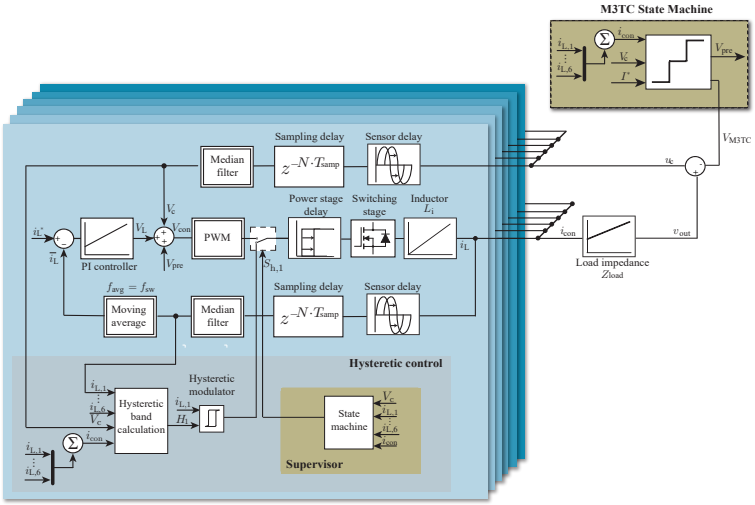

Figure 6.23: Schematic of the proposed adaptive hybrid controller with integrated M3TC state machine, for the control of DynACuSo.

Apart from the basic state machine which essentially follows the operational principle of the system, Figure 6.24 depicts also the switching actions during the transitions, in order to minimize the disturbance of the M3TC output voltage V_{M3TC} when two stages, which do not necessarily have the same semiconductor switches (e.g. M3TC stage 1 comprises 1.2kV devices while the higher stages comprise 1.7kV devices), have to be switched simultaneously. A commutation example from state 1 to state 2 is shown in Figure 6.25 along with the respective voltages of the M3TC stages.

More specifically, when $\mathrm{M3TC}_1$ and $\mathrm{M3TC}_2$ consist of different devices, the following state machine is needed to minimize the introduced disturbance: At state 1.1, switch $S_{2,2}$ is turned off, and the anti-parallel diode of $S_{2,2}$ is conducting, resulting in no change in V_{M3TC}[6]. After waiting for the interlocking time $T_{\mathrm{int,s}}$ of the 1.7kV switch $S_{2,2}$, the state machine commutes to state 1.2, by turning on switch $S_{2,1}$. Due to the turn on delay time of switch $S_{2,1}$, V_{M3TC} is not changing, and

[6]For a unidirectional current this transition is not needed. $S_{2,2}$ could be simply tuned off as it offers no advantage. Nevertheless it is included here for completeness.

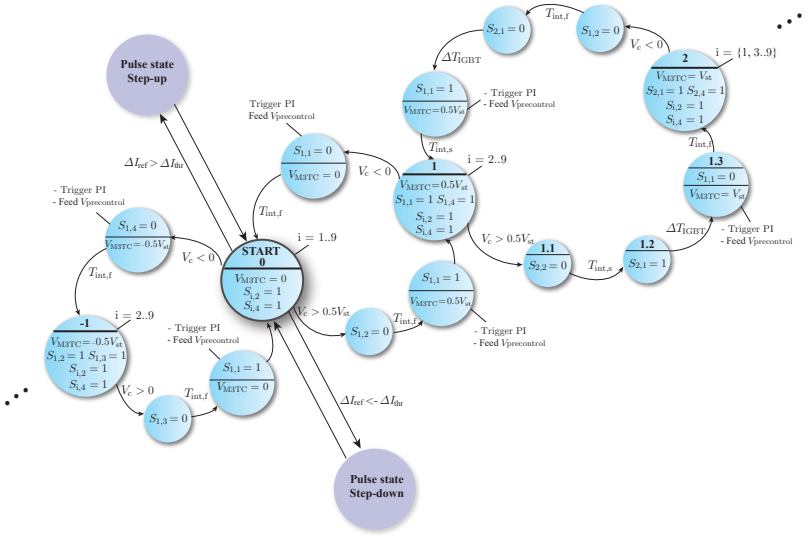

Figure 6.24: State machine of the M3TC. The algorithm uses the average output voltage v_c and the reference current I^*. When v_c exceeds the set limit $(0.5 \cdot V_{st})$, the state machine changes its state. The modulation of the state machine is performed in order to minimize the jittering due to the interlocking time of the switches. During state transitions, the state machine triggers the PI controller calculations, informing it for the upcoming change in voltage v_c. In step transients the algorithm follows a different state machine to facilitate the dynamic performance(Figure 6.27).

the state machine waits for $\Delta T_{IGBT} = T_{d,s} - T_{d,f}$, which is the delay time difference between the 1.7kV and the 1.2kV device (these times are usually found in the datasheets). In state 1.3 the state machine turns off switch $S_{1,1}$. During this state, a small disturbance is observed in V_{M3TC} due to the difference between the fall time of switch $S_{1,1}$ and the rise time of $S_{2,1}$, as can be seen in Figure 6.25b. At the end of state 1.3, switch $S_{2,1}$ is conducting and the voltage V_{M3TC} becomes equal to V_{st}. During state 1.3 the algorithm triggers the PI controller calculations and feed-forwards the voltage (V_{pre}) to the PI controllers, as shown in Figure 6.24. In this way, the transient behavior of the PI is improved and the disturbance caused by the level change is minimized.

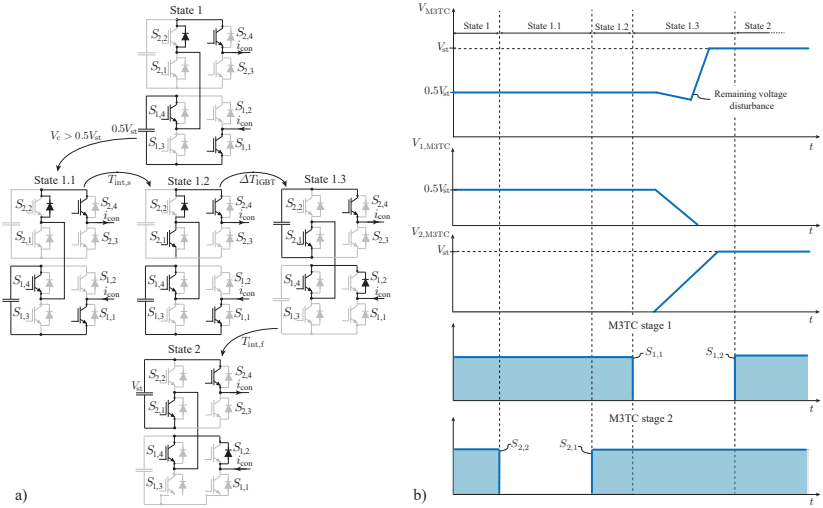

Figure 6.25: Commutation from state 1 to state 2, shown in Figure 6.24. a) Switch status during the commutation. b) M3TC voltages during commutation. The commutation strategy shown in Figure 6.25 ensures that the non-ideal switching causes only a small voltage disturbance during state 1.3. This disturbances is caused by the difference between the fall time of switch $S_{1,1}$ and the rise time of switch $S_{2,1}$.

After waiting for the interlocking time $T_{\text{int,f}}$ of the 1.2kV IGBT, the state machine commutes to state 2 by turning on switch $S_{1,2}$. In this way, the two simultaneous switching actions (turning on stage 2 and turning off stage 1) are almost synchronous resulting in only a minor remaining voltage disturbance of V_{M3TC}, that is caused by the rise/fall times of the switches. Nevertheless, the difference in rise/fall times of the switches was found to be relatively small in Figure 6.21.

Figure 6.26 shows a simulation of the DynACuSo with two installed M3TC stages, following a sinusoidal current reference of 400Hz and an amplitude of 1.5kA. The load comprises a 1.2Ω resistor and 5µH inductance. The simulation takes place in a co-simulation platform, where the actual code of the FPGA[7] is simulated for increased modelling accuracy. It is observed that the inclusion of the M3TC results only in minor disturbances. More importantly, the pre-control voltage V_{pre}

[7]implemented in VHDL.

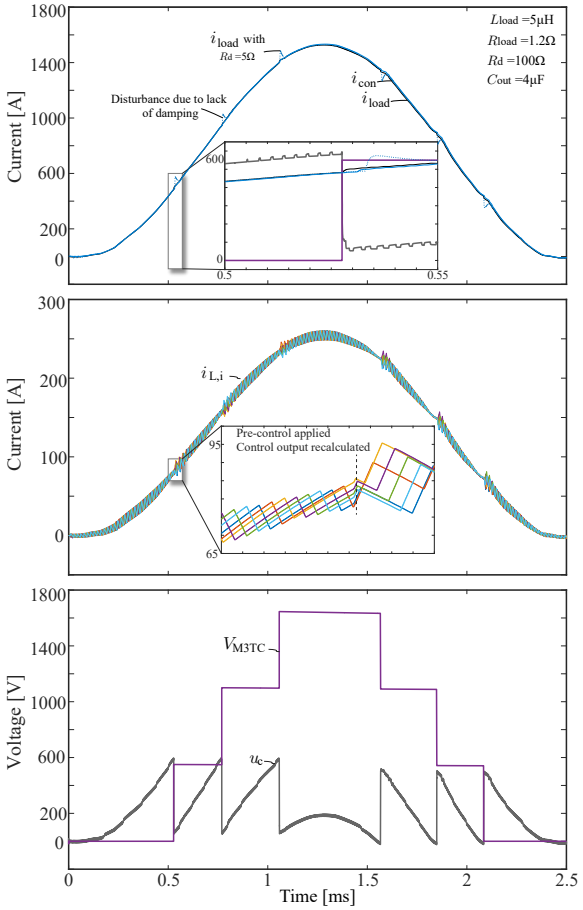

Figure 6.26: Simulation DynACuSo with two installed M3TC stages, following a sinusoidal current reference of 400Hz and 1.5kA. Magnified views of the disturbance introduced during switching of the M3TC stage is also shown.

is timely applied, and the calculation of a new duty cycle takes place resulting in module currents $i_{\mathrm{L,i}}$ that follow the reference, despite the rapid large change of the output voltage u_{c}.

It is also worth noting that the damping network ensures that the converter current i_{con} and the load current i_{load} are essentially the same,

and no in-rush current is seen at the load current, due to the rapid capacitor discharge in parallel to the current shaping converter[8]. For reference, a simulation with a damping resistance $R_\mathrm{d} = 5\Omega$, showing only the load current is depicted in Figure 6.26, where i_load in that case is shown with a dashed line. There it can be seen, that i_load is highly disturbed every time the M3TC changes its state, despite the controller being able to keep a well controlled i_con. These results signify again the importance of the output stage on the operation of DynACuSo, despite its small size. Nevertheless, the disturbance could be avoided by placing the capacitor network directly at the load side, but due to its high voltage rating, it would result in a significantly bulkier choice.

6.3.2 Dynamic Operation: Step Transients

When a step transient is initiated, the M3TC can greatly improve the performance as depicted in principle in Figure 2.5. During the current rise/fall however the current shaping converter operates outside of its operating region and therefore appropriate action needs to be taken, to avoid excessive overshoot. A detailed state machine for the case of 2 M3TC stages during a step up transient is shown in Figure 6.27. It should be noted that in this state machine the intermediate commutation states are not included for reasons of clarity.

Initially, the state machine for dynamic performance is initiated, after a step transient with an amplitude higher than ΔI_thr is given as a reference. This condition ensures that the M3TC is not enabled for low amplitude changes, for a small duration as it offers negligible benefits for those cases. At first, $\mathrm{M3TC}_1$ is inserted, and v_c collapses below 0V. As long as v_c stays below 0V, and $I_\mathrm{err} = I^* - i_\mathrm{con}$ is lower than a set threshold I_tran, the state machine keeps the first M3TC stage inserted. It needs to be highlighted that the threshold I_tran is selected according to the delay of the current measurement system, the possible delay in the reaction of the M3TC, and the maximum current gradient of the system. For example for the case of the prototype DynACuSo, the threshold I_tran is chosen to be more than 200A, since the maximum gradient is approximately 20A/µs, the total current measurement delay is approximately 7µs, and the delay for the reaction of the M3TC (including the interlocking time and the rise/fall times of the IGBT switches) is approximately 3µs. In this way there will be sufficient time from the

[8] this problem was present in [23].

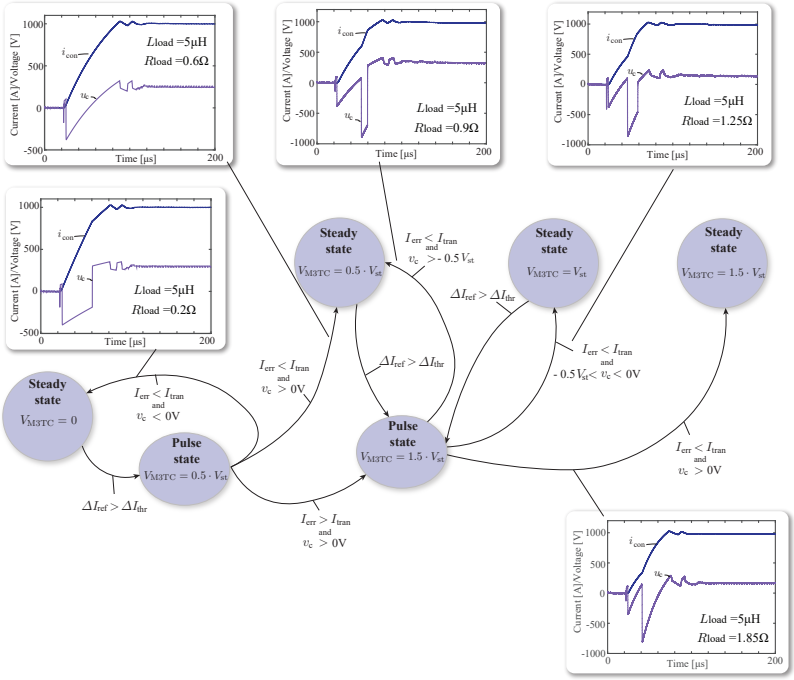

Figure 6.27: State machine of the M3TC for dynamic performance with 2 installed stages, during a step up transient. Different steady state conditions are considered depending on the steady state output voltage. Appropriate thresholds need to be considered to avoid excessive overshoots, based on the delays of the system, and the expected current gradient. Corresponding simulation results are shown.

time instant that the threshold I_{tran} is reached in the controller, until the time instant that the real total current i_{con} reaches the reference, to switch the M3TC and cause the current shaping converter to operate again within its operation region. This will allow the current shaping converter to control the current, and return to steady state.

In Figure 6.27 the simplest case occurs when I_{err} becomes less than I_{tran}, and the sampled voltage v_{c} at that instant is lower than 0V. Then the state machine decides that it does not need the additional M3TC stage voltage at steady state, so it bypasses stage M3TC_1, and

V_{M3TC} becomes 0V. Voltage v_{c} will then rise by $0.5 \cdot V_{\mathrm{st}}$, and the adaptive hybrid controller takes over, following the algorithm presented in Section 4.1.5. On the other hand, if I_{err} becomes less than I_{tran}, and the sampled voltage v_{c} at that instant is higher than 0V, the state machine would decide to keep $\mathrm{M3TC}_1$ inserted at steady state, and since the current shaping converter is already inside its operating region, the adaptive hybrid controller controls the current, bringing it to steady state with $V_{\mathrm{M3TC}} = 0.5 \cdot V_{\mathrm{st}}$.

The three last cases include the insertion of the $\mathrm{M3TC}_2$, as the resistive part of the load is higher. As the I_{err} is higher than the threshold I_{tran}, and voltage v_{c} becomes higher than 0V, the current gradient reduces. For this reason the state machine includes stage $\mathrm{M3TC}_2$, and voltage v_{c} collapses below 0V again, causing the current gradient to increase. When the current reaches threshold I_{tran}, if v_{c} is lower than $-0.5 \cdot V_{\mathrm{st}}$, the state machine bypasses completely stage $\mathrm{M3TC}_2$, and leaves only stage $\mathrm{M3TC}_1$ inserted. On the other hand, if v_{c} is between $-0.5 \cdot V_{\mathrm{st}}$ and 0V, the algorithm bypasses stage $\mathrm{M3TC}_1$, and keeps stage $\mathrm{M3TC}_2$ inserted, resulting in V_{M3TC} being equal to V_{st}. Finally, if v_{c} is higher than 0V, it keeps both stages inserted and V_{M3TC} remains equal to $1.5 \cdot V_{\mathrm{st}}$.

It must be noted that in all of these cases, v_{c} remains lower than 0V for the biggest part of the transient duration, facilitating the step up current gradient. It should also be clear than when the load is known beforehand, a more optimal insertion of the M3TC stages can be implemented. This state machine however shows the generic case, for high dynamic performance. It should also be observed from the simulated scenarios, that the voltage v_{c} exceeds the operating region of the current shaping converter, and an appropriate design needs to be employed to ensure that safe isolation distances are kept. Finally, similar case scenarios and a state machine with a similar logic can be constructed for step down transients.

6.3.3 Experimental Results

To verify the considerations regarding the integration of the M3TC in the closed loop control of the system, experimental measurements are performed with the prototype DynACuSo, and one installed M3TC stage.

At first, a triangular reference current with an amplitude of 900A

(Figure 6.28) is followed. A resistive load 0.5Ω with an estimated load inductance of 4μH is used. The stage voltage is chosen in this case to be 400V, while the input split DC-link capacitors are charged at 600V and 50V respectively. It can be observed that in this scenario the system manages to produce a a triangular waveform with approximately 2A/μs gradient, without significant disturbances introduced by the switching actions of the M3TC.

It is also noted, that when the M3TC is inserted, oscillations of its

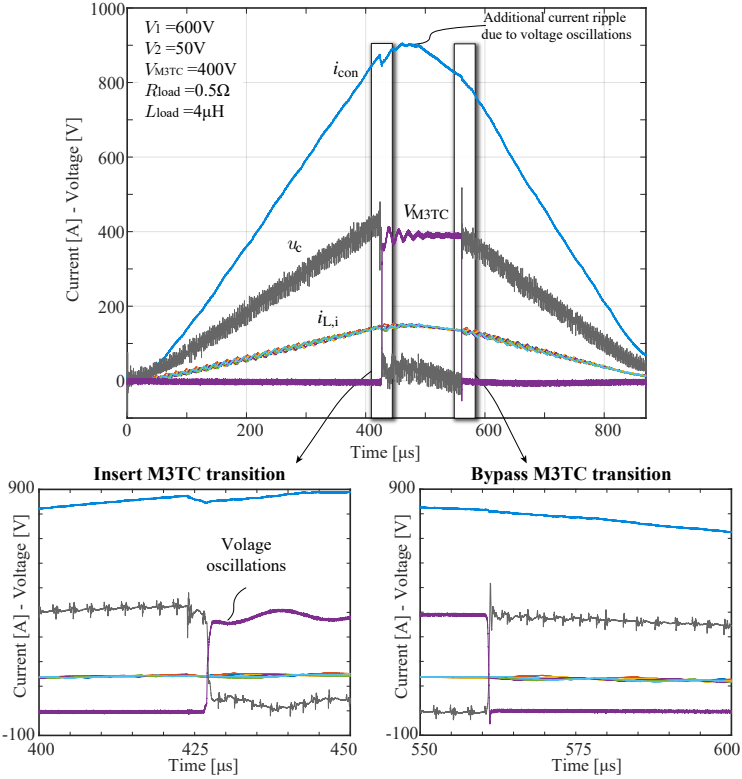

Figure 6.28: Experimental results of the complete prototype system following a triangular reference current with an amplitude of 900A. Measurement parameters: $R_{\text{load}} = 0.5\Omega$, estimated load inductance $L_{\text{load}} = 4\mu\text{H}$, $V_1 = 600\text{V}$, $V_2 = 50\text{V}$, $V_{\text{M3TC}} = 400\text{V}$.

voltage are causing some additional ripple on the output voltage u_c, which in turn causes additional i_{con} current ripple. This is attributed to the exchange of energy between two film capacitors, the one that acts as the main storage element of the stage, and the commutation capacitor that is placed next to the power IGBT modules to facilitate the switching performance (shown in Figure 6.15). Despite the low inductive path between those capacitors, the low ESR of the film inductors result in effectively very low damping and the resonant circuit that is formed causes the demonstrated oscillations. This issue could be mitigated if electrolytic capacitors were used as a main storage element of the M3TC stage. Their higher ESR would then cause additional power

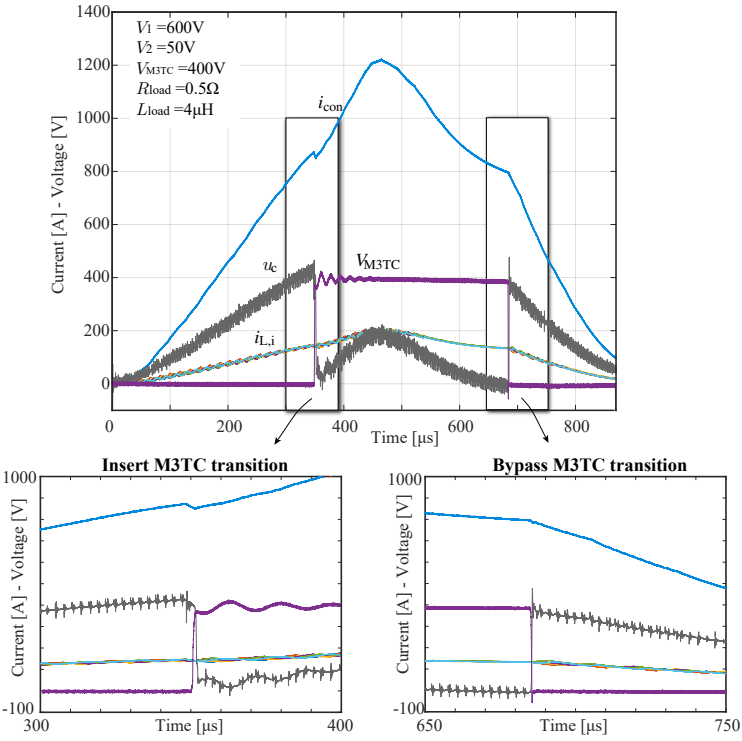

Figure 6.29: Experimental results of the complete prototype system following a triangular reference current with an amplitude of 1200A. a resistive load 0.5Ω with an estimated load inductance of 4μH.

losses, but it would also act as a damping resistance, reducing the effect of the LC resonance.

Figure 6.29 shows a similar experiment, this time with a triangular reference current with an amplitude of 1.2kA. This corresponds to a current gradient of approximately 3A/µs, and despite the fact that the system follows closely during the rise, it clearly does not manage to handle the faster gradient, when v_c is close to 0V. This behavior can be attributed to the insufficient control margin of the current shaping converter, due to the relatively low available negative voltage (-50V). This measurement demonstrates one of the shortcomings of the state machine used for the control of the M3TC. The system has the available voltage to deliver a much higher gradient than the required 3A/µs, but the state machine by design waits until v_c is below 0V, in order to decide to bypass stage $M3TC_1$. Nevertheless, the measurement result is as expected and low disturbances due to M3TC switching are caused on the i_{con}.

Figures 6.30 & 6.31 demonstrate the performance of DynACuSo in step transients and show the high dynamic potential of the topology and the control strategy, when the state machine shown in Section 6.3.2 is used together with the developed adaptive hybrid control. In Figure 6.30 a pulse current of 600A and a flattop of approximately 0.5ms is given as a reference. When the step transient is initiated the system switches to adaptive hybrid control and the M3TC stage is inserted. V_{M3TC} becomes 400V and u_c collapses below 0V. It is also observed that when the current reaches approximately 490A, the M3TC stage is bypassed and the current gradient slows down. In this case, the state machine decides to bypass the M3TC stage in steady state, as the voltage when the control decision is made, is lower than 0V. It should also be noted that the threshold of the current I_{tran}[9] was conservatively set to 250A. Nevertheless, after the M3TC is bypassed, the current shaping converter returns within its operating region and the adaptive hybrid control, controls the current as explained in Section 4.1.5.

Similarly, once the step down transient is initiated, the M3TC stage is inserted in the negative direction and its voltage becomes -400V, causing u_c to increase above 600V. In this case the oscillations, that were previously noted during the measurements with the triangular reference current, are still visible but they do not have a visible effect on the current. In the case of the step down as the current returns

[9] introduced in section 6.3.

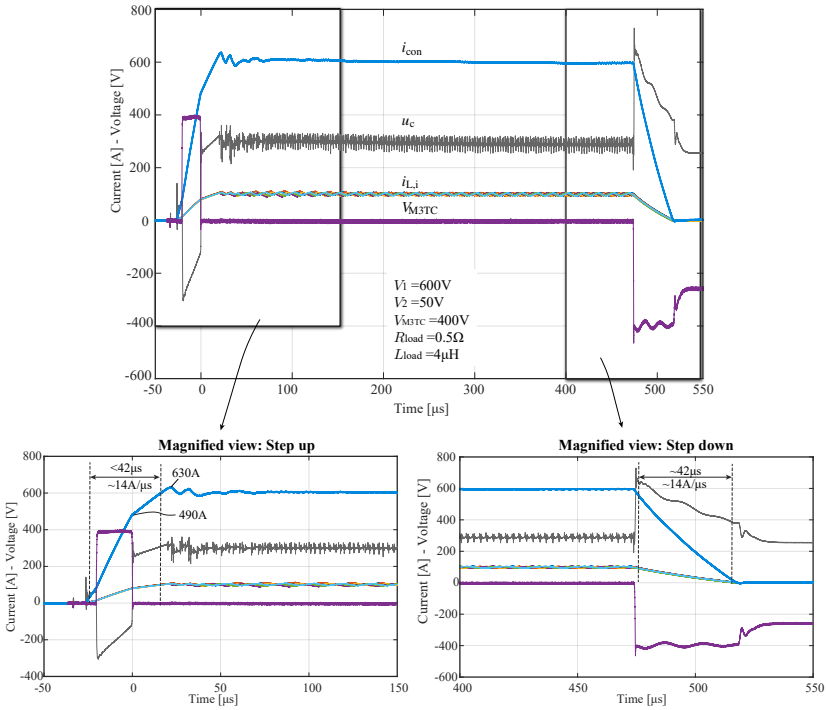

Figure 6.30: Experimental results of the developed DynACuSo following a step transient with 600A reference amplitude through a resistive load 0.5Ω with an estimated load inductance of 4µH. Magnified views of the step up and step down are shown and the dynamic performance is noted. The current reaches its reference after approximately 42µs corresponding to an overall gradient of 14A/µs.

to 0A, the current shaping converter simply turns all switches off, and the transition to 0A is uncontrolled. Nevertheless, in both cases the reference is reached within less than 42µs, corresponding to an overall current gradient of more than 14A/µs. Clearly, for a fully charged system (e.g. V_1 charged at 750V and V_{M3TC} at 550V), the achieved gradient would be even higher.

In Figure 6.31 a pulse current of 1kA and a flattop of approximately 0.5ms is given as a reference. As in the previous test case, the system switches to adaptive hybrid control, and the M3TC stage is inserted.

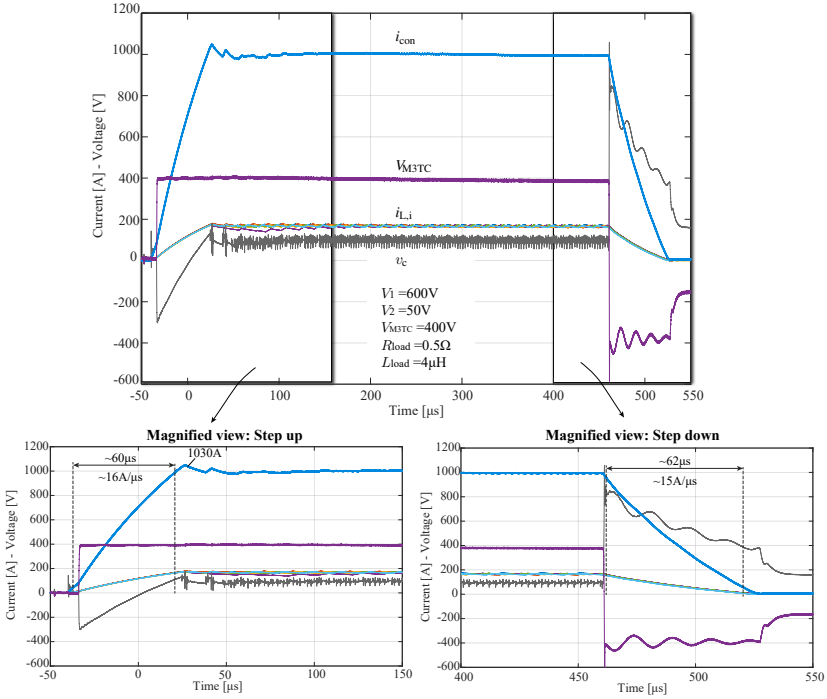

Figure 6.31: Experimental results of the developed DynACuSo following a step transient with 1000A reference amplitude through a resistive load 0.5Ω with an estimated load inductance of 4µH. The current reaches its reference after approximately 60µs corresponding to an overall gradient of 15A/µs.

V_{M3TC} becomes 400V, and u_{c} collapses below 0V. However in this case, the state machine responsible for the control of the M3TC decides to keep the stage inserted for the duration of the transient, as it is needed at steady state. It can be observed that in contrast to Figure 6.30, the current gradient during step up remains constant. The current during step up reaches 1kA in approximately 60µs corresponding to a 16A/µs overall current gradient. The step down to 0A is also facilitated by inserting the M3TC stage in the negative direction, leading to a peak v_{c} voltage of 800V, which is well outside of the operating range of the current shaping converter. A current gradient of approximately 15A/µs is achieved in this case.

6.4 Interface Converter System

The interface converter system topology is depicted in Figure 6.32. The converter acts as the interface between the commercial isolated AC/DC power supply and the current-shaping converter. The interface converter system provides the DynACuSo module with the needed flexibility to operate both in pulsed and continuous mode. The main tasks of the interface converter are:

- Charge/Discharge the input capacitor bank C_1 and C_2.
- Bypass the capacitor bank during continuous operating mode.

The topology of Figure 6.32 uses the minimum number of semiconductors in order to perform the needed tasks. It also enables the use of a standard isolated single-quadrant AC/DC power supply of up to 800V, for charging the system in pulsed mode and for supplying the needed current during continuous operation mode.

It should be clarified that the interface converter, bypasses capacitor C_2 during the continuous mode of operation. The continuous operation of DynACuSo can only be performed with capacitor C_2 completely discharged[10].

[10] in any other case, two power supplies would need to be used, with the power supply connected in parallel to C_2, acting as a sink (bi-directional, non-standard), as explained in Section 2.1.4.

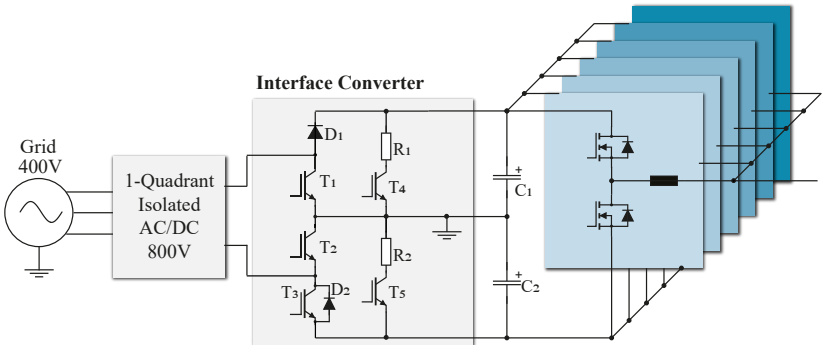

Figure 6.32: Schematic of the interface converter system that connects the input capacitor bank of the current-shaping converter with a standard single-quadrant isolated AC/DC supply.

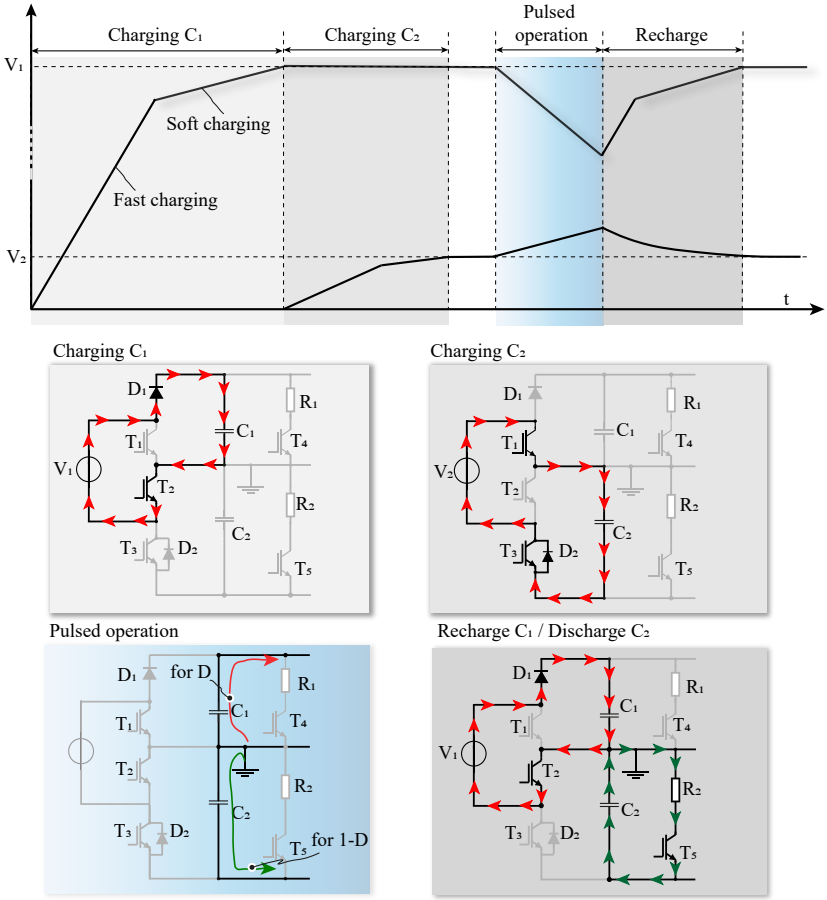

Figure 6.33: Graphical depiction of the subsequent system states in pulsed operation mode.

6.4.1 Operation Modes

Figure 6.33 graphically depicts the different states of the system during the pulsed operation mode. Initially for charging C_1, switch T_2 is turned on and diode D_1 is forward biased. A fast charging current is used for charging the capacitor up to 90% of its set-point, while the last 10% of the charging procedure takes place with a soft charging current.

For charging C_2, switch T_1 is turned on and diode D_2 is forward biased. The charging of C_2, follows the same procedure as C_1. When the charging process is finished, the system waits for the pulse.

During the pulse, for a uni-directional (positive) current, C_1 is discharged (red arrow), while C_2 is charged (green arrow), and all switches of the interface converter are turned off. After the pulse, the system should re-charge capacitor C_1 and discharge capacitor C_2, preparing the system for the next pulse. Discharging capacitor C_2 takes place through R_2, simply by turning on switch T_5.

Figure 6.34 depicts the different states of the interface converter system during the continuous operation mode. After charging only the input capacitor C_1, the supply voltage is kept at V_1, and the converter bypasses capacitor C_2, by permanently turning on switches T_2 and T_3. As shown in Figure 6.34, switch T_2 is conducting during the complete switching cycle, so it needs to be rated for the nominal current (1kA). Switch T_3 conducts only during the negative part of the switching cycle (1-D). On the other hand, diode D_1 conducts only during the positive

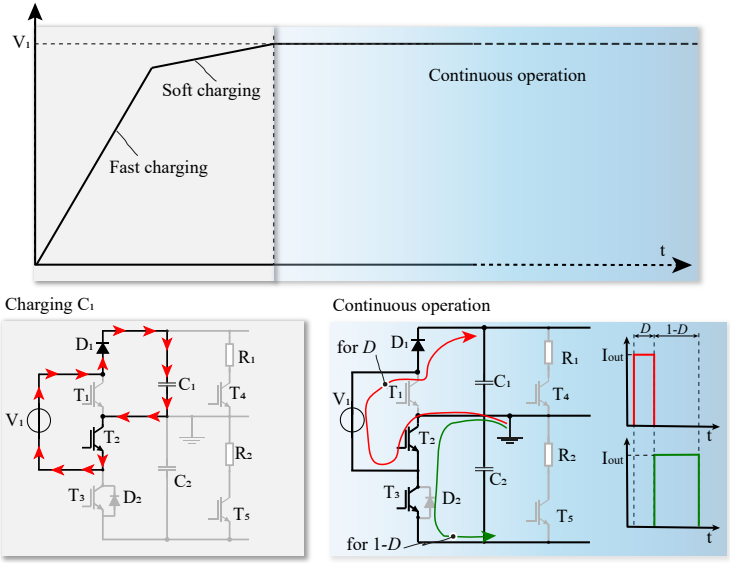

Figure 6.34: Graphical depiction of the subsequent system states in continuous operation mode.

part of the switching cycle (D). Furthermore, no switching losses are generated during continuous operation, since the switches T_2 and T_3 are permanently on, and during the negative interval (1-D), switch T_1 is blocking the supply voltage V_1. As a result diode D_1 does not generate reverse recovery losses.

Based on the above considerations, the blocking voltage and the rated current of every device can be inferred. Table 6.5 lists the ratings of the semiconductor devices of the interface converter system. For the developed prototype system, the maximum duty cycle is $D_{\max} = 0.15$[11]. The minimum duty cycle for the continuous mode of operation is assumed to be $D_{\min} = 0.05$[12]. The RMS value of a pulsed current, with amplitude I_{out} and a duty cycle of D like the one shown in Figure 6.34 is simply calculated by (6.16).

$$I_{\text{RMS}} = I_{\text{out}} \cdot \sqrt{D} \tag{6.16}$$

The charging current for the capacitors is given by the maximum RMS current of the AC/DC power supply and the necessary charging times of the system. For the prototype system the peak charging current of 30A is assumed and the charging cycle is assumed to be long enough ($>$ 180s) so the RMS current values for the devices T_1 and D_2 are irrelevant for the design. The RMS discharge current through T_4 and T_5 is determined by the choice of resistors R_1 and R_2. The current values listed on the table refer to the resistor values chosen for the prototype system, where $R_1 = 500\Omega$ and $R_2 = 33\Omega$. The RMS values listed on the table refer to the duration of the discharge, while the real RMS current through devices T_4 and T_5 is significantly lower.

6.4.2 Converter Design

Based on the above, it becomes clear, that switches T_2, T_3, and diode D_1 have a high current rating and therefore special care needs to be taken during their design. Furthermore, the rest of the semiconductors have standard ratings, and their selection is not further discussed.

Since T_2 and T_3 have similar voltage and current ratings, the same part number is chosen. For this application, since the devices are not switching with a high switching frequency, relatively low-cost 600V high current IGBTs, optimized for lower conduction are preferred. As there

[11] in continuous operation mode with 1kA rated current.
[12] used to calculate the RMS current through T_3 in Table 6.5.

Table 6.5: Current.voltage ratings of semiconductor devices of the interface converter system.

	Maximum Voltage	**Voltage Class**	**Current (RMS)**	**Current (Peak)**
D_1	800V	1200V	390A	1000A
T_1	800V	1200V	-	30A
T_2	100V	600V	1000A	1000A
T_3	100V	600V	975A	1000A
D_2	100V	600V	-	30A
T_4	800V	1200V	0.4A	1.6A
T_5	100V	600V	3A	4.25A

is no solution available for rated currents up to 1kA, multiple IGBTs need to be used in parallel.

After a preliminary comparison, the IXGN400N6B3 IGBTs from IXYS are chosen for switches T_2 and T_3, mainly due to their availability and low-cost. Additionally, the SOT-227B package allows for a compact design and easy mechanical integration. Furthermore, diode D_1 is preferred to have low conduction losses with a high current rating. Again, for these ratings, multiple diodes need to be placed in parallel to share the current and the SOT-227B package is preferred, since it allows for a simpler integration along with T_2 and T_3. After all, the DMA150E1600NA silicon diode is chosen. It should be noted that paralleling diodes should not be a problem, as long as they are thermally coupled and placed next to each other on a common heatsink [159] .

Since the interface converter needs to be placed behind the input capacitor bank, its maximum dimensions are fixed and act as constrains for the size of its cold-plate. The cold-plate consists of a single water channel and the dimensions are shown on the sketch in Figure 6.35a. Figure 6.35b depicts the cold-plate's thermal resistance (R_{th}) as a function of the inlet water velocity, calculated with the analytical model of Section 3.4.3 and compared to the 3D numerical FEM model. It can be noted that once again the analytical model is closer to the surface average FEM model, and is more accurate for higher inlet water velocity values.

A more conservative approach is followed by assuming the maximum

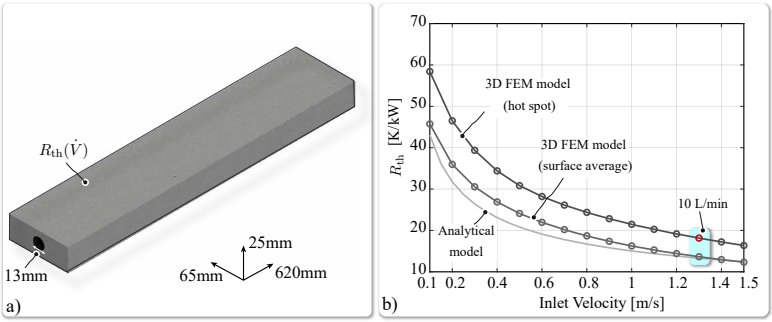

Figure 6.35: Modelling of the cold-plate of the interface converter. a) Cold-plate geometry based on system restrictions. b) Cold-plate thermal resistance $R_{\text{th.CP}}$ as a function of the input water flow, calculated analytically based on the cold-plate model of Section 3.4.3, and numerically with FEM simulations.

value of the cold-plate's $R_{\text{th,max}}$, calculated with the 3D FEM model, for a water flow of 10L/min (R_{th}=18K/kW). With the cold-plate fixed, the design procedure is straightforward, and a comprehensive flow chart is shown in Figure 6.36a. The algorithm simply iterates through the number of diodes and IGBTs that can be placed in parallel, calculates the worst-case losses (i.e. conduction losses), based on the manufacturer's datasheet, and estimates the junction temperature of the IGBT and the diode, according to the thermal model depicted in Figure 6.36b.

Figure 6.36c shows the resulting maximum junction temperature with respect to the number of semiconductors used. The main constraints that define the limits of the feasible design space are: i) the maximum operating temperature of the devices, which for both part numbers is 150°C, and ii) the maximum device count that can be placed on the cold-plate with the defined geometry (i.e. 19 devices).

Finally, the chosen design for the prototype system is highlighted on the graph. The total number of semiconductors that is used in the prototype is 13, with 3 diodes and 5 IGBTs for T_2 and T_3 respectively. Table 6.6 lists the data that was used for the calculation of the semiconductor losses and the estimation of the junction temperature. It should be noted that it was selected to use 3 diodes instead of 2 in parallel (which is also in the feasible design space), to account for possible imbalances in the loss sharing of the diodes.

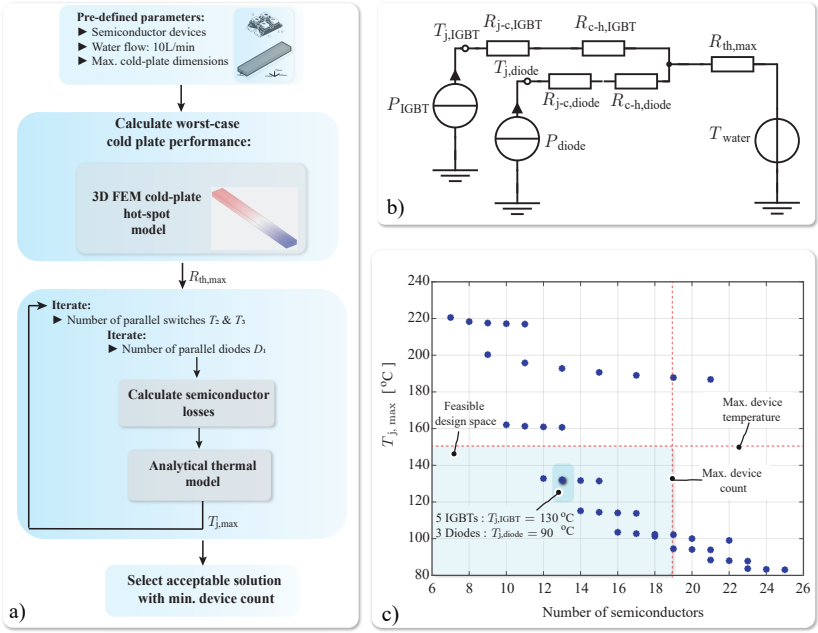

Figure 6.36: a) Interface converter design procedure. b) Analytical thermal model of the interface converter. c) Maximum junction temperature with respect to the number of semiconductors used.

6.4.3 Prototype System

The part numbers that are used in the prototype interface converter are listed in Table 6.7. The choice of resistance values for R_1 and R_2 constitutes a trade-off between the resistor RMS power rating during a full discharge and the discharge times. With the chosen values C_1 discharges in 315s, and C_2 in 70s. The RMS power during the discharge time is 70W for R_1 (35W per resistor) and 60W for R_2, which is well within the specifications of the chosen part numbers.

A picture of the CAD design of the interface converter is shown in Figure 6.37, where the different power components are noted. The first thing to notice in Figure 6.37 is that the cold-plate is split into two parts, to allow for a simpler and cheaper manufacturing. The performance of the cold-plate is however equivalent to the one calculated in the

Table 6.6: Parameters of the prototype interface converter.

Parameter	Symbol	IGBT	Diode
Average Current	I_{avg}	1000A	150A
RMS Current	I_{RMS}	1000A	390A
Forward Voltage	V_{on}	0.85V	0.8V
On-Resistance	R_{on}	3mΩ	2mΩ
Junction-Case R_{th}	$R_{\text{j-c}}$	0.125K/W	0.2K/W
Case-Heatsink R_{th}	$R_{\text{c-h}}$	0.1K/W	0.1K/W
Water Temperature	T_{water}		20°C
Heatsink R_{th}	$R_{\text{th,max}}$		0.018K/W
Parallel Devices		5	3
Total Losses	P_{loss}	2900W	220W
Junction Temperature	T_{j}	130°C	90°C

Table 6.7: Ratings and part numbers of the components of the interface converter system.

Symbol	Ratings	# of Devices	Part Number
D_1	1.6kV - 150A	3	DMA150E1600NA
T_1	1.2kV - 20A	1	IXGA20N120A3
T_2	0.6kV - 200A	5	IXGN400N60B3
T_3	0.6kV - 200A	5	IXGN400N60B3
D_2	0.6kV - 30A	1	VS-ETU3006S-M3
T_4	1.2kV - 20A	1	IXGA20N120A3
T_5	1.2kV - 20A	1	IXGA20N120A3
R_1	200W	2	TGHLV1K00JE
R_2	200W	1	TGHLV33R0JE

previous section. As mentioned before, all the components with the higher ratings are conveniently using the same package (SOT-227B), leading to a straightforward mechanical design.

Furthermore, the two PCBs that drive the switches and accommodate the lower rated components, the gate drivers, the communication interfaces and the CPLD, can be seen in more detail in Figure 6.38.

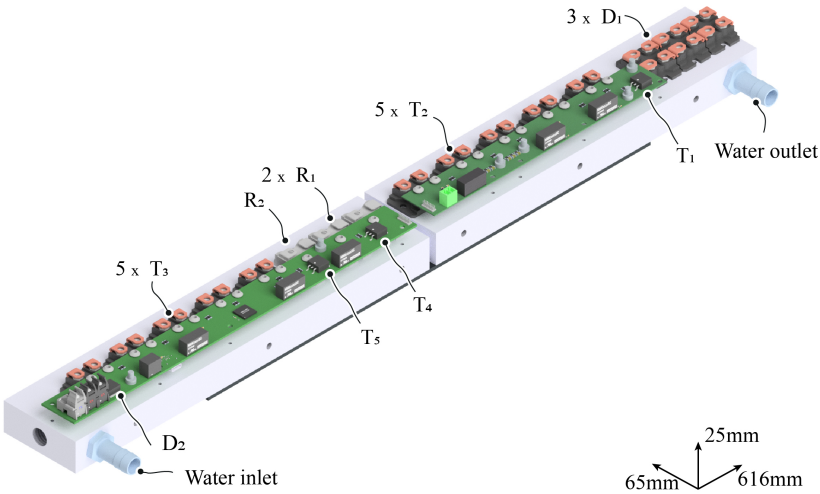

Figure 6.37: CAD design of the interface converter system.

The two PCBs communicate with each other with a flat-cable exchanging power and data signals. Each switch is driven by a dedicated isolated gate driver, which in turn is supplied by an isolated power supply (±15V). The switching speed is irrelevant for the application, so relatively high gate resistance values (40Ω) are used to drive all the switches.

The parallel devices of T_2 and T_3 are driven by one gate driver, and high values are chosen for the gate resistances (40Ω). The high gate resistances slow down the switching procedure and therefore the devices are turning on/off approximately synchronized, despite their inevitably asymmetrical gate loop design. In this way, a possible current sharing imbalance due to asynchronous switching is avoided.

Additionally, the interface converter communicates with the master controller through the use of the optical interfaces, which are also noted in Figure 6.38. More specifically, there are two optical receivers and one optical transmitter. One receiver is used for the clock signal, in order to synchronize the interface converter with the rest of the system and one that signifies the mode of operation. Based on the desired mode of operation, which is a 4-bit word that is set by the master controller, the local CPLD generates the corresponding gate signals to the switches

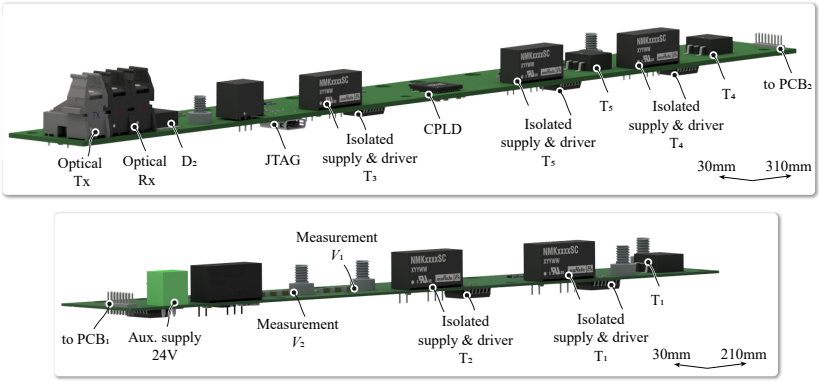

Figure 6.38: CAD illustration of the interface converter PCBs and their main components.

$T_1..T_5$. The possible combinations are listed in Table 5.4. The optical transmitter sends feedback to the master controller, in the case of faults. Furthermore, as shown in Figure 6.38, the system is equipped with two local voltage measurements, for measuring the capacitor voltage V_1 and V_2. The measurements can be used to make the local control of the interface converter autonomous.

Finally, the operational limits of the interface converter prototype system are theoretically calculated. As shown above, the limits of the converter include both the maximum output current as well as the duty cycle D of the current-shaping converter, which in fact determines the RMS current through diode D_1. Since diode D_1 has been over-dimensioned in the prototype system (max. 90°C), the initial limit of $D_{\max} = 0.15$ can be exceeded.

The key in this calculation is the determination of the real duty cycle D_{real}, which includes the compensation of the losses of the system. Starting from the power conservation in (6.17), and the average input current given in (6.18), equation (6.20) can be derived. The total power losses P_{loss} is then given by (6.19), where P_{CSC} is the total losses of the current shaping converter, P_{M3TC} the losses of the step voltage generator and P_{inter} the losses of the interface converter.

$$P_{\text{in}} = P_{\text{out}} + P_{\text{loss}} \qquad (6.17) \qquad I_{\text{in}} = D_{\text{real}} \cdot I_{\text{out}} \qquad (6.18)$$

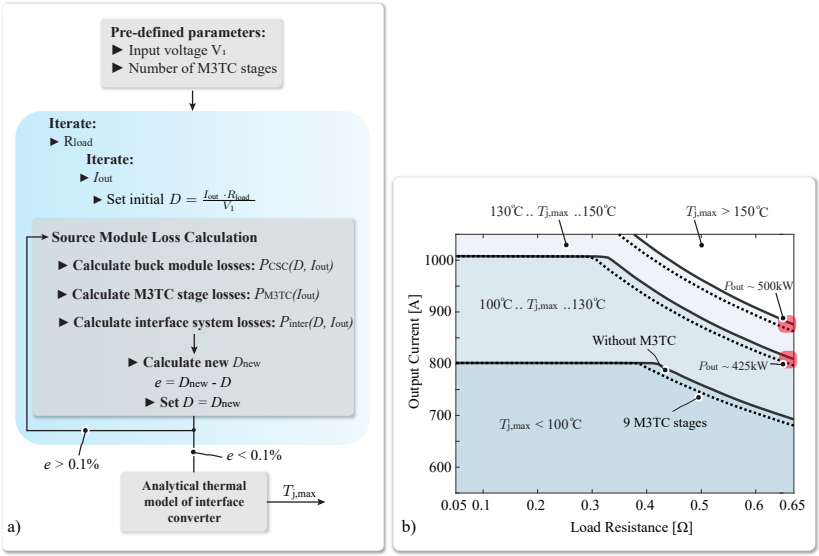

Figure 6.39: a) Recursive procedure for the calculation of the real duty cycle D_{real}, for different operating points. b) Calculated operational limits of the interface converter system for V_1 =750V.

$$P_{\text{loss}} = P_{\text{CSC}} + P_{\text{M3TC}} + P_{\text{inter}} \tag{6.19}$$

$$D_{\text{real}} = \frac{I_{\text{out}} \cdot R_{\text{load}}}{V_1} + \frac{P_{\text{loss}}}{V_1 \cdot I_{\text{out}}} \tag{6.20}$$

It is important to note here, that the losses of the interface converter as well as the losses of the current-shaping converter, are dependent on the duty cycle, which in turn is dependent on the power losses. Figure 6.39a shows the procedure that is followed to estimate the maximum junction temperature of the devices of the interface converter, using a recursive procedure to converge to the real D_{real}.

Figure 6.39b presents the operational limits of the interface converter system. The contour lines represent the temperature boundaries of 100°C, 130°C, and 150°C . The absolute maximum junction temperature of all the power devices used for the interface converter system is 150°C, but the recommended operation region is below 130°C. The

solid black line represents the boundaries of the system without M3TC stages. The dotted line represents the full scale source module with 9 M3TC stages installed. It can be noted that due to the extra losses of the M3TC stages, the operating region of the full scale source module is slightly reduced. This is attributed to the increased duty ratio that limits the operating range of the diode D_1. It should also be highlighted, that during the constant part of the boundary lines, the maximum junction temperature is the temperature of the IGBT switch T_2, which is designed to conduct a constant 1kA at 130°C (Table 6.5). Nevertheless it is concluded that the interface converter can support a continuous operation of the system in its safe operating region up to approximately 425kW. As the current shaping converter can operate with a higher power[13] in continuous mode, the 425kW is also the power limit of DynACuSo, when it operates with 1kA of continuous current.

6.5 DynACuSo: Prototype System

The assembled prototype DynACuSo with one M3TC stage is depicted in Figure 6.40a. The system is placed inside a metallic cabinet which is grounded, and sits on a GPO-3 glass polyester laminate profile, which offers high isolation to the grounded cabinet and excellent mechanical strength, flame resistance and good flame spread characteristics, for safety reasons. From the picture it can also be observed, that the interface converter is connected behind the input capacitor bank, providing connection points for the external power supply to charge the system. Also, the M3TC stage sits on an isolated potential[14], and the same concept is followed for the rest of the M3TC stages in the cabinet.

The main control unit (Ampegon UCS [160]) is conveniently placed inside the cabinet and under the current shaping converter. The control unit itself is not visible in the Figure 6.40a, but it is given in Figure 6.40b [160]. The signal interfaces to the control box are also visible in Figure 6.40a. Each module of the current shaping converter communicates with the control unit with 2 USB type-C cables[15].Furthermore, 1 additional USB type-C cable is used for the voltage measurements, which are placed on the same PCB as the output stage. Each M3TC stage communicates with the control unit through 6 optical fibers. To

[13] approx. 115kW per module, resulting in 690kW.
[14] the isolation is ensured by the GPO-3 profile dimensions.
[15] one for the gate driver board and one for the current measurement board.

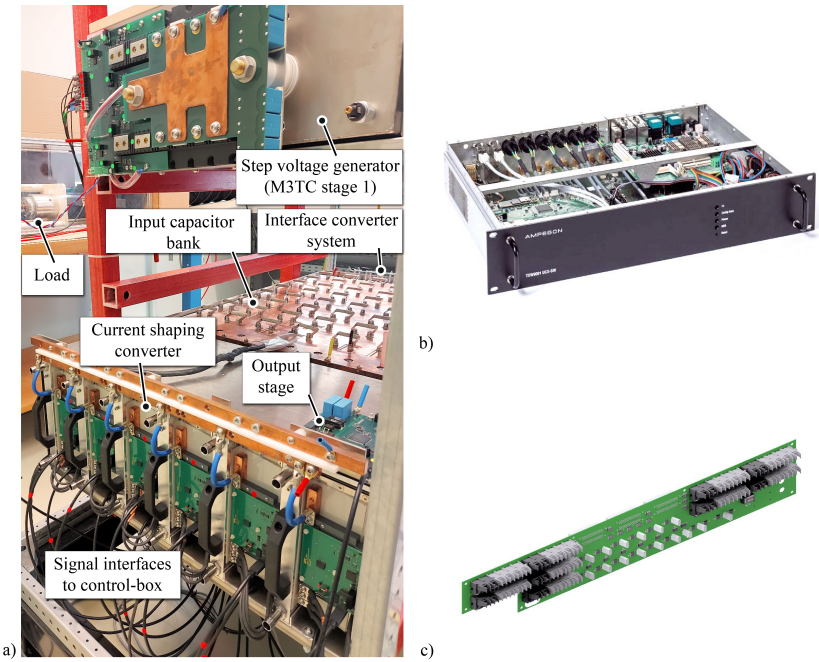

Figure 6.40: a) Picture of the fully assembled prototype DynACuSo and its main components. b) Picture of the main control unit of DynACuSo [160]. c) CAD illustration of the interface card used between DynACuSo and the main control unit.

match those signal interfaces with the control unit, an interface card is designed as an extension to the control unit. The interface card features 54 optical IOs (for up to 9 M3TC stages) and 15 USB type-C connectors (including 2 reserve connectors). A CAD illustration of the interface card is shown in Figure 6.40c. Apart from providing an interface between the control unit and the different PCBs of the DynACuSo, the interface card receives the auxiliary power and distributes it to the PCBs of the current shaping converter through the USB type-C cables.

6.6 DynACuSo: Performance Limits

Throughout this work, transient, steady state and loss models of the different converter systems of the DynACuSo have been established and a series of measurements have been successfully performed, validating the theoretical abilities of the prototype system. In this section the overall performance of DynACuSo in terms of its dynamic, output ripple and efficiency is calculated. The results act as a guideline of the overall performance limits of the prototype system. For reasons of simplicity and clarity DynACuSo modules with 1 or 2 installed M3TC stages are considered.

It should be highlighted that this section gives the maximum theoretical performance limits of the DynACuSo in terms of dynamic and ripple, based on the following two assumptions:

i. The current gradient calculation assumes that the M3TC stage is turned on/off ideally, and therefore relevant delays do not have an impact on the generated gradient.

ii. The current ripple calculation includes only the switching related harmonics, and additional ripple generated due to control actions is not included in the calculations.

The first assumption essentially neglects the impact that a premature bypass of an M3TC stage would have on the current gradient, which was visible in Figure 6.30. Such an ideal integration of the control of the M3TC stage would require knowledge of the load and appropriate timing. Regarding the load current ripple, in the following it is assumed that it is filtered by the active adaptive filter developed in Section 5.2.4. Again the transient time needed for the activation of the accompanying current transformer and the active filter itself is neglected. In the following the assumed active filter uses the parameters shown in Figure 5.23[16], while the damping resistance value R_d is chosen based on (3.30) with Q=0.1. Similar to the calculations of Section 3.8, the non-ideal real inductor characteristics are taken into consideration in the calculation of the ripple.

Figure 6.41 a&b show the calculated current gradient and load current ripple performance of the current shaping converter with only one

[16] developed and tested version.

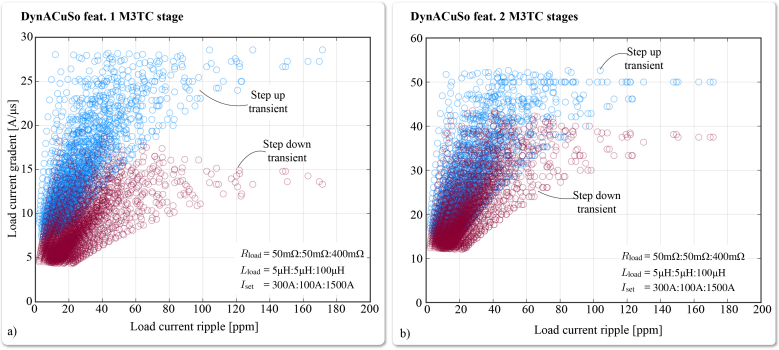

Figure 6.41: Theoretical dynamic and ripple performance range of DynACuSo for different loads and operating points with: a) 1 M3TC stage and b) 2 M3TC stages. Note that the ripple performance is not affected by the number of M3TC stages. Observe that the y-axis is different in the two figures.

M3TC stage[17] installed, and only two M3TC stages[18] respectively, for different operating current set-points and different resistive/inductive loads. To calculate the current ripple in ppm, the calculated $\Delta i_{\text{load,pp}}$ is divided every time by the respective operating current amplitude. Clearly for the investigated loads, there is a large discrepancy regarding the achievable current gradient in step up and step down for both studied systems. Nevertheless, including 2 M3TC stages roughly doubles the achievable gradient, which is expected since the additional stage essentially doubles the available input voltage, while the current ripple remains unaffected. It is also worth noting that compared to Figure 3.40, the achievable load current ripple due to the inclusion of the active filter is significantly lower and consistently below 500ppm, as the active filter provides superior cancellation especially at the 60kHz range, which is the result of inductance mismatch, and is not well filtered by the low volume passive solution with the accompanying R_{ss}.

To get further insights regarding the role of the load, and the operating current Figure 6.42, depicts the step up gradient, step down gradient, and the ripple as a function of the load resistance and load inductance, for 3 different operating currents. Figure 6.42 can ultimately act as a guideline regarding the maximum theoretical performance of

[17] charged at 550V.
[18] charged at 550V and 1.1kV.

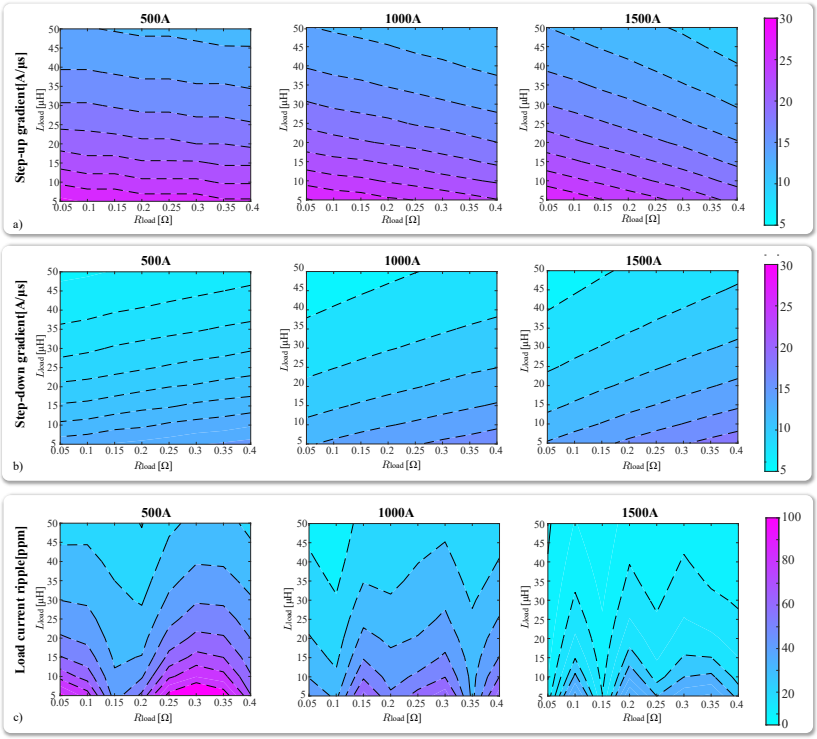

Figure 6.42: Calculated maximum theoretical performance of the current shaping converter with 1 installed M3TC stage, as a function of the load for three different operating currents 500A, 1000A and 1500A. a) Step up gradient. b) Step down gradient. c) Load current ripple in ppm. Input parameters: $V_1 = 750\text{V}$, $V_2 = 50\text{V}$, $V_{\text{M3TC}} = 550\text{V}$, $R_{\text{load}} = 0.05..0.4\Omega$ with a step of 0.05Ω, $L_{\text{load}} = 5..100\mu\text{H}$ with a step of $5\mu\text{H}$, and $I_{\text{out}} = 300..1500\text{A}$ with a step of 100A.

the DynACuSo concept. In general a high load inductance reduces the current gradient, requiring additional M3TC stages (i.e. higher output voltage) to achieve higher gradients. Additionally the resistive part of the load reduces the step up transient but increases the step down, as the higher voltage of the load is added to the available step down voltage. Similar conclusions can be drawn regarding the effect of the current amplitude. It is worth noting, that the developed DynACuSo

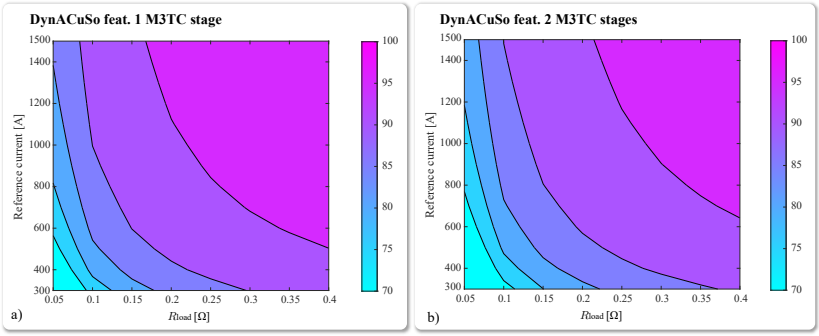

Figure 6.43: Calculated efficiency of DynACuSo as a function of the operating point for: a) 1 M3TC stage. b) 2 M3TC stages. Input parameters: $V_1 = 750\text{V}$, $V_2 = 50\text{V}$, $R_{\text{load}} = 0.05..0.4\Omega$ with a step of 0.05Ω, and $I_{\text{out}} = 300..1500\text{A}$ with a step of 100A.

prototype with 1 installed M3TC stage can deliver gradients higher than $10\text{A}/\mu\text{s}$ to loads with an inductance up to $50\mu\text{H}$ during step up. Unfortunately the step down performance is reduced to approximately $5\text{A}/\mu\text{s}$ for loads with an inductances higher than $30\mu\text{H}$.

Figure 6.43 a&b depict the overall efficiency of DynACuSo equipped with 1 M3TC stage and 2 M3TC stages respectively. The losses of the current shaping converter are calculated based on the verified loss models of Section 3.7.1. For the M3TC calculations, the models of Section 6.2.4 are considered, with the M3TC stages contributing only with conduction losses, as the switching losses are negligible in normal operation. It is worth noting that the efficiency of the system when supplying highly inductive loads with low resistance can be as low as 65% for a system with 2 installed M3TC stages, and less than 70% for a system with 1 installed M3TC stage. Based on Figures 6.41 and 6.43, it becomes clear that the higher the system performance in terms of dynamic, the more M3TC stages needed, and the lower the system's efficiency.

6.7 DynACuSo: Operation with DC-arc

In Chapter 1 the importance of switch-gear characterization for the future HVDC grid has been outlined, along with the modelling challenges

associated with it. Namely, the development and optimization of future circuit breakers relies on the understanding, and subsequent analytical or numerical modelling of the arc that is formed between the contacts, when the circuit breaker opens. In [20], a novel measurement method to determine the arc time constant has been proposed, relying on complex current waveforms, such as a staircase-like waveform, to derive the commonly used black box arc model. In [19] and [161], the method was tested with a developed current source (Figure 1.2) and significant progress in the understanding of the arc processes has been achieved.

One of the main initial goals of DynACuSo has been to be able to drive currents with fast current gradients through DC-arcs with robustness. An investigation of previous experiments conducted with the UnACuSo used with DC-arcs as loads showed, that the source was unable to ignite and control the current with robustness, leading to a premature trip of the source due to over-current [23]. These experiences led to design choices such as the inclusion of the robustness criterion[19], and the high switching frequency for the newly developed DynACuSo.

Additionally, compared to the source in [161], the DynACuSo is able to generate a current gradient that is almost 50 times faster in step up and at least two orders of magnitude faster in step down, while also having a lower ripple current at the flattop, due to the increased switching frequency and the interleaving concept. Consequently, the DynACuSo opens new opportunities regarding the exploration of the arc properties, and enable new research paths. In this section, the ability of the prototype system to drive complex current waveforms through a DC-arc is demonstrated experimentally.

Initially, Figure 6.44 shows the load that is used to emulate the behavior of a circuit breaker. A spark gap with adjustable length, formed by two metallic rods is used, together with an ignition wire with a cross section of 0.05mm^2. DynACuSo then supplies the high current through the ignition wire, which evaporates some tens of µs after the start of the experiment, igniting a plasma between the metallic rods. The plasma then conducts the current, and continues to conduct until the current is reduced to 0A by DynACuSo. The load is placed inside a plastic container, to protect the surrounding equipment from the explosion during the ignition, and a fan is also employed acting as a ventilator, to carry away the gases that are generated in the process.

Figure 6.45 depicts the generation of a staircase-like current wave-

[19] used during the parameter selection Section 3.5.

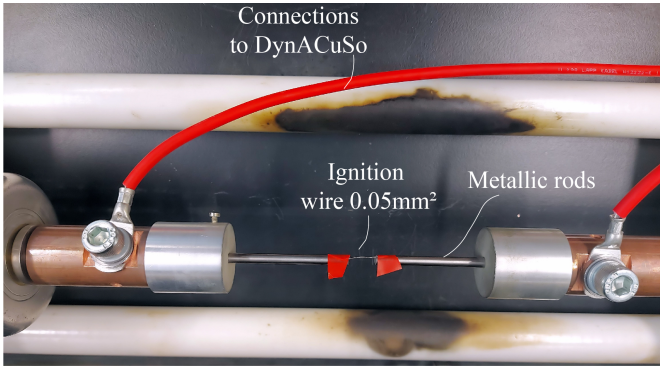

Figure 6.44: Spark gap and ignition wire used as a load to emulate the behavior of a circuit breaker. The ignition wire evaporates soon after the start of the experiment due to the high current, and plasma is generated between the metallic rods. The plasma will continue to conduct the current until the current source actively reduces it to 0A.

form with a step of approximately 500A, through the described load. In this case, the PI controller with single update rate is used (described in Section 4.1.1). The integrator is deactivated for this experiment, as stability is valued over accuracy and the static error is of little importance for the purposes of the experiment. The spark gap length is set to approximately 2cm for this measurement.

It can be observed that the current is well-controlled throughout the experiment. Especially during the current step up from 500A to 1kA, the arc voltage appears to "jump" from 50V to more than 300V, causing a disturbance in the current rise. Nevertheless, the controller deals with this fast transient smoothly and exhibits a small overshoot before settling. Furthermore, in Figure 6.45 the step down from 500A to 0A is shown, to observe the behavior of the arc when it stops conducting. This part is particularly interesting for arc modelling purposes [21].

The same experiment is repeated in Figure 6.46, this time with the adaptive hybrid controller employed to generate an even faster current gradient during step up, and verify its ability to drive dynamic loads. Interestingly this time the voltage of the arc "jumps" before the current rise and the source generates a gradient higher than 13A/µs during the step up from 500A to 1kA through the plasma. In the magnified measurement of v_c the effect of the loop inductance is also noticeable during

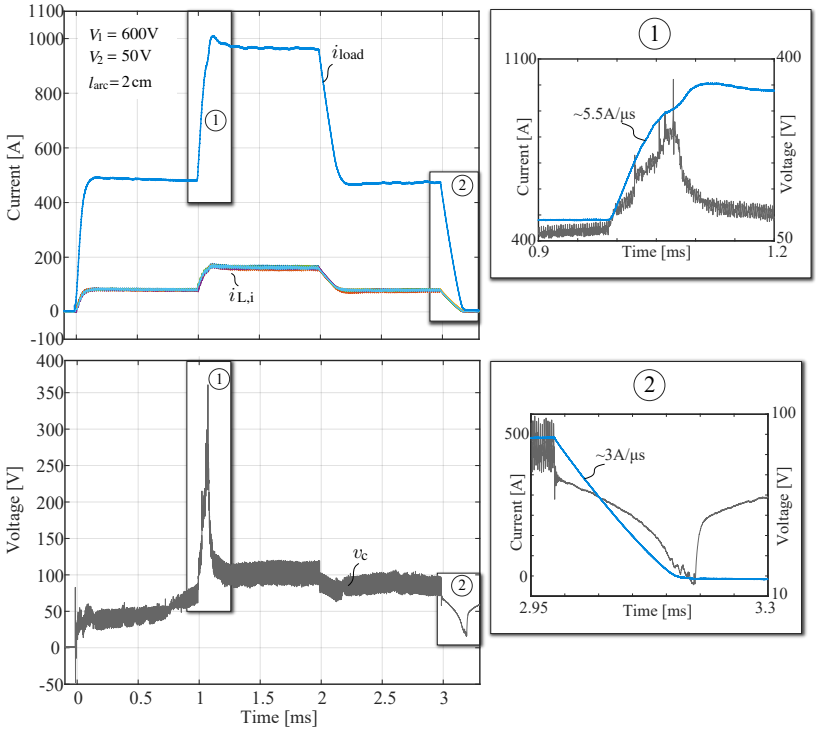

Figure 6.45: Experimental measurements of the DynACuSo without the M3TC generating a staircase-like current waveform with a step of 500A, through a DC-arc. **Controller:** PI with a single update rate. a) Converter current i_{con} and module currents $i_{L,i}$. b) Output voltage v_c. Magnified views of the current rise and fall are also shown. Parameters: $V_1 = 600V$, $V_2 = 50V$, $l_{arc} = 2cm$.

the fast rise of the current. Nevertheless, the adaptive hybrid controller settles smoothly after a small overshoot, and quickly returns to interleaved operation. In this case, before the transient a disturbance in the current is caused by aforementioned arc voltage jump. The subsequent current error is corrected by the PI controller, which is operating during flattop. It should be noted, that the step down gradient is similar to the one in Figure 6.45 and relatively slow, as the current shaping converter operates in these experiments autonomously, without the help of

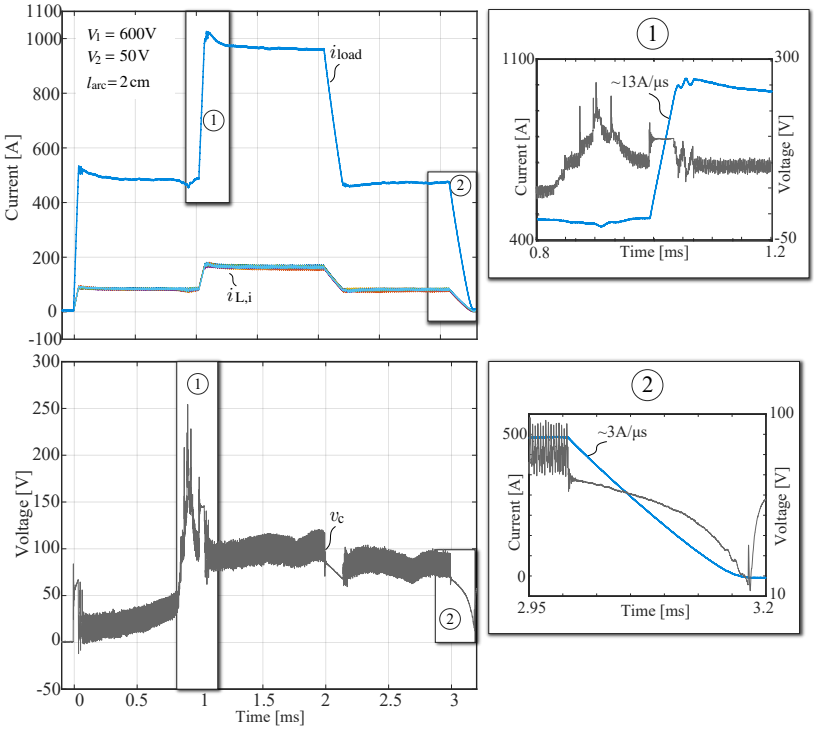

Figure 6.46: Experimental measurements of the DynACuSo without the M3TC generating a staircase-like current waveform with a step of 500A, through a DC-arc. **Controller:** Adaptive hybrid controller. a) Converter current i_{con} and module currents $i_{L,i}$. b) Output voltage v_c. Magnified views of the current rise and fall are also shown. Parameters: $V_1 = 600$V, $V_2 = 50$V, $l_{arc} = 2$cm.

an additional M3TC stage to facilitate the step down transient.

Finally, in order to demonstrate the ability of the DynACuSo to deliver a negative voltage to the arc, and therefore generate a current with a high step down gradient, Figures 6.47 & 6.48 show step transients assisted by the M3TC during step down. The M3TC stage is charged at 200V and 400V respectively, and it is simply inserted in the negative direction, when a step down transient is initiated. It can be concluded that the step down current gradient can be changed accordingly based

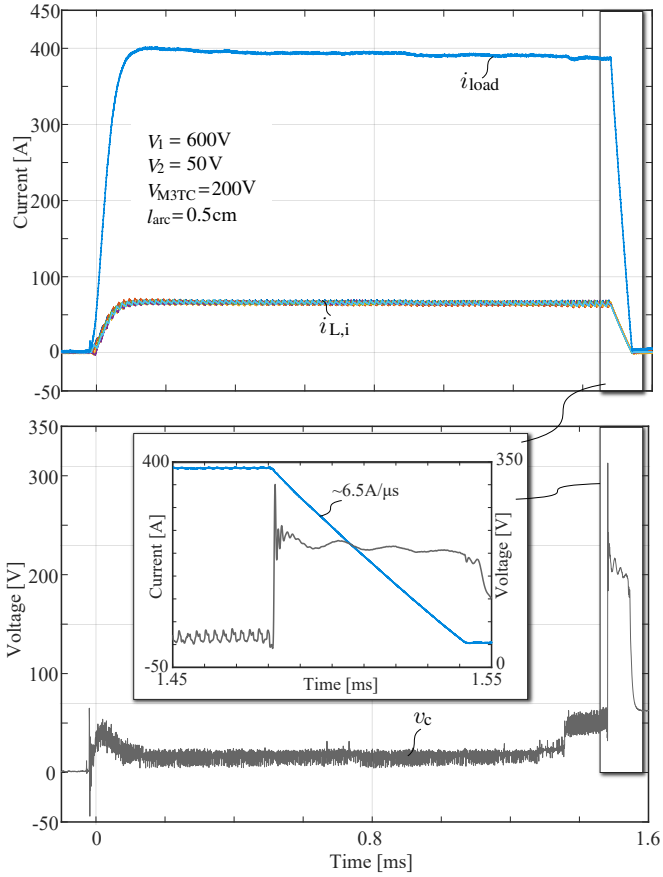

Figure 6.47: Experimental measurements of the DynACuSo with the M3TC stage assisting the step down transient of a step current of 400A through a DC-arc a) Converter current i_{con} and module currents $i_{L,i}$, b) Output voltage v_c. A magnified view of the current step down is also shown. Parameters: $V_1 = 600V$, $V_2 = 50V$, $V_{M3TC} = 200V$, $l_{arc} = 0.5cm$. A step down gradient of 6.5A/µs is achieved in this experiment.

on the voltage of the M3TC, allowing it to vary (e.g. current gradients of 6.5A/µs and 11A/µs are shown in Figures 6.47 & 6.48 respectively). As a result, the properties of the arc and its behavior just before its extinction can be studied methodically.

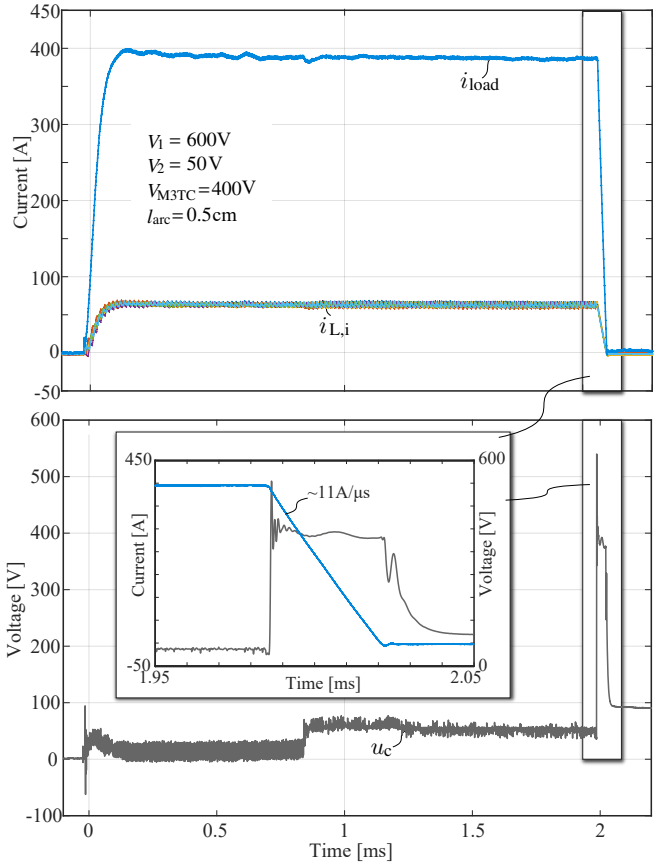

Figure 6.48: Experimental measurements of the DynACuSo with the M3TC stage assisting the step down transient of a step current of 400A through a DC-arc a) Converter current i_{con} and module currents $i_{L,i}$, b)Output voltage v_c. A magnified view of the current step down is also shown. Parameters: V_1 =600V, V_2 =50V, V_{M3TC} =400V, l_{arc} =0.5cm. A step down gradient of 11A/µs is achieved in this experiment.

Interim Summary

The different systems of the prototype DynACuSo have been presented in detail, and their performance and operational limits have been ana-

lytically calculated to provide insights into the theoretical possibilities of the developed system and its limitations. The results can be used as a guideline for future possible applications of the DynACuSo, and provide a benchmark for possible future improvements in terms of efficiency and performance of the source. More specifically, it has been shown that a DynACuSo with 1 installed M3TC stage can generate step up current gradients higher than 10A/μs through inductive loads with inductance up to 50μH. On the other hand, to generate step down gradients higher than 10A/μs, 2 installed M3TC stages are needed. Additionally, it has been shown that a load current ripple below 500ppm is possible under all operating conditions, when the AAF output stage is employed, as long as the controller does not generate additional ripple, and only the switching ripple is considered (e.g. open loop controlled flattop). A detailed modeling of the different converter systems also revealed that the DynACuSo's power limit arises from the interface converter system's diodes, and a maximum power rating of 425kW can be achieved with up to 1kA continuous current rating.

Furthermore, in order to provide a platform for future research activities, a DynACuSo module with one installed M3TC stage has been developed, along with the accompanying firmware, and its operation has been verified under various conditions. The prototype system managed to achieve very fast current gradients that exceeded the 10A/μs specification in both step up and step down transients, thanks to the collaboration of the M3TC state machine with the proposed adaptive hybrid controller, presented in Section 4.1.5. Additionally, a description of the local control of the interface converter system, and especially the M3TC stage has taken place, and further details of the communication concept and the overall prototype operation have been given.

More importantly it was shown that DynACuSo can be used to facilitate future research activities in the field of HVDC switch-gear characterization, which is expected to play a significant role in the future deployment of HVDC grids. DynACuSo has demonstrated excellent robustness when controlling the current through a DC-arc, and simultaneously managed to achieve current gradients that exceeded the 10A/μs in both step up and step down transients, generating complex staircase like current waveforms. These types of waveforms have been identified as key enabling technology for modelling the arc properties, and DynACuSo constitutes a significant step in this direction.

7 Final Words

Conclusion

Nowadays there is a plethora of power electronics converters with special topologies in operation, acting as current sources and serving a wide area of applications, ranging from diagnostics and cancer treatment in the medical world to fundamental research activities in the physics world, and from plasma confinement in fusion energy activities to engineering research activities for the future of HVDC electric grid. Exploring the limitations of such systems, and enhancing their performance is of great benefit since it does not only lead to a more efficient energy conversion, bringing the operation and construction costs down, but it can also pave the way for new applications with enhanced capabilities, opening new research opportunities. In this thesis the focus was laid on the DynACuSo, a dynamic arbitrary current source, with a modular design, aiming to fulfill a list of strict specifications that arise from a wide range of applications, like the ones mentioned above, and explore performance boundaries in terms of output ripple, dynamic and controllability/robustness. The DynACuSo is the second generation arbitrary current source. Its predecessor, the UnACuSo, was also designed and developed at the *Laboratory for High Power Electronics* at *ETH Zurich*.

After presenting the target applications and needed specifications of the system in **Chapter 1**, **Chapter 2** discusses the special topology of the DynACuSo, its particularities, and its fundamental operational principle under different loading conditions. The topology of the DynACuSo is based on the combination of a high frequency, multi-phase,

interleaved buck-type converter that is responsible for controlling the current, connected in series to a step voltage generator, based on the MMC concept with pre-charged capacitors, to increase the output voltage level. Chapter 2 presents also in a qualitative manner the arising trade-offs that point towards a holistic design approach to fulfill the compiled list of specifications.

The multi-phase, interleaved, buck-type current shaping converter is the most important component of the DynACuSo, and it is presented in detail in **Chapter 3**. A preliminary literature review has shown that existing conventional assumptions are not suitable for a multi-phase interleaved buck converter with an arbitrary output stage, acting as a current source, and therefore a more detailed approach is taken to model the system at steady state, and derive the resulting load current ripple with accuracy. Furthermore, transient models are presented to facilitate the parameter selection procedure, and a passive adaptive output filter suitable for pulsed power systems with high dynamic and low flattop ripple requirements is proposed.

After selecting the parameters of the system and presenting the governing component models used throughout this work, the inductor of the fundamental buck module is recognized as a crucial component for the efficiency, volume and cost of the module, and a detailed optimization procedure is devised. The optimization routine is generic and can be extended for any inductor operating in a pulsed power system with a reduced continuous current rating. The inductors of the current shaping converter are then investigated and useful insights from the Pareto-fronts of core volume and efficiency, regarding the suitability of different magnetic materials and thermal management concepts are extracted. Namely, SiFe-3% results in the smallest volume for potted core designs, but is also less efficient compared to Nanocrystaline and Amorphous materials. Furthermore, it is shown that potting the core into an aluminum box with a potting material featuring good thermal conductivity can result to a significant decrease (3-5 times) in the core material needed for a feasible realization, regardless of the material. In fact, potting the core in the case of SiFe-3% results in significant reductions in the core material used, already for continuous current ratings higher than 20% of the maximum current rating. Finally, the chosen SiFe-based inductor design is developed and tested, verifying the used models and considerations.

In the final sections of **Chapter 3**, the prototype 6-phase current

shaping converter is shown and experimental measurements verify its operation, performance, and the used models. The fundamental buck module system achieves an estimated efficiency that exceeds 98% in nominal power (approx. 115kW), and the interleaved system generates complex current waveforms, achieving current gradients in step up transients that exceed the specified 10A/µs. It is also shown that due to the limited negative voltage, the step down performance is limited to a maximum of 2A/µs.

In order to harness the full potential of the multi-phase interleaved buck converter, a systematic comparative evaluation of control concepts takes place in **Chapter 4**. Initially, the feedback loop is modeled in detail and suitable considerations for high power dynamic converters are taken. The study uses the current shaping converter of DynACuSo as a test-bench for the controller design evaluations. In the process, an adaptive hybrid control algorithm is developed featuring a hysteretic controller during step transients, followed by a PI controller during flattop. The systematic evaluation of five control concepts has shown that the proposed adaptive hybrid controller offers superior performance in step transients, and is especially suited for pulsed power applications with high dynamic requirements. It is also shown, that the MPC scheme is an excellent choice for arbitrary reference currents, but it is especially sensitive to measurement noise requiring additional filters in the feedback loop. Another useful outcome of the analysis is the fact that executing the conventional PI controller with a fast execution speed instead of once per switching period, can increase its performance by more than 10%. This increase clearly comes at the expense of increased implementation effort and computational power. The results of the simulations have been verified by experimental measurements with the developed current shaping converter of the DynACuSo.

Chapter 5 presents a current transformer with adaptive burden resistance, able to sense an AC current in the mA-range superimposed on a high DC current in the kA-range, with high sensitivity, only microseconds after the flattop of a step transient is reached. The sensor is particularly interesting for DynACuSo, as it allows the characterization of its flattop ripple. The developed sensor exhibits a sensitivity of 0.125V/A, a wide bandwidth between 2.5kHz-30MHz, and a settling time after the pulse of a approximately 17µs. In the second part of the chapter, the proposed sensor is used to sense the load current ripple, and feed it back to a linear operational amplifier that acts as an active

filter. The active filter achieves excellent ripple attenuation in a wide frequency range that exceeds 500kHz. All in all, the active adaptive filter stage is developed, and it is tested together with the current shaping converter of DynACuSo. The operational principle of the sensor/filter combination is verified experimentally, and it is shown that an excellent ripple attenuation is achievable down to the mA-range, thanks to the high sensitivity of the current sensor.

Finally **Chapter 6** presents the prototype system of DynACuSo in more detail, namely its input capacitor bank, its step voltage generator and its interface converter system. It also discusses the integration of the control algorithm of the step voltage generator into the proposed adaptive hybrid controller, and experimental measurements verify the benefits of the presented scheme in step transients. The DynACuSo with a single installed M3TC stage achieves experimentally current gradients of more than 15A/µs. More importantly the capability of DynACuSo to control the current with robustness, while simultaneously generating highly dynamic complex current waveforms through a DC-arc is demonstrated experimentally too. The DynACuSo manages to deliver a staircase-like current waveform with a step up current gradient of 13A/µs, and a step down gradient that exceeded 10A/µs, potentially enabling new research opportunities in the field of DC switch-gear characterization.

Outlook

This thesis presented a high power dynamic arbitrary current source with low output ripple and a modular design. The developed prototype system verified the theoretical considerations with extensive experimental measurements, and showed that the source can pave the way for research activities especially in the field of HVDC technology. With the look in the future, a possible road-map for further activities is compiled hereby focusing on three main fields to further improve/utilize the potential of the DynACuSo.

- **Control:** In this work, a thorough evaluation of different control concepts has taken place. The MPC showed an interesting performance when following current references of any shape, demonstrating the best overall dynamic performance. However, measurement results showed that it is particularly sensitive to noise,

which hinders its applicability in high power systems, where the presence of measurement noise is in general more pronounced. Further investigation, and an improved implementation of the MPC together with digital/Kalman filters would be needed to harness its full potential. Additional efforts in this field may potentially bring significant benefits to the control scheme not only of the DynACuSo but also of systems operating as current sources. Further efforts can also be devoted on the control of known, mainly inductive loads, where the full potential of the DynACuSo has not been completely harnessed.

- **Precision:** In this work it was shown that the use of an active output stage can significantly reduce the output ripple and even achieve ripple attenuation in harmonics that are significantly lower than the switching frequency. As it stands however, measurement noise causes control actions that hinder the overall precision of the DynACuSo, despite its theoretically ultra-low output ripple current capability. The control actions lead to current ripple in frequencies that are significantly lower than the switching frequency, and outside of the bandwidth of the output filter stage. To avoid these erroneous control actions when the source operates in closed loop control, further efforts need to be devoted into the improvement of the current measurements. These efforts might involve the use of different sensor technology, higher ADC precision, and/or the employment of improved analog/digital filters to attenuate the noise that arises from the low power electronics on the current measurement board.

- **Firmware & Integration:** The developed prototype was tested in the course of this work under different conditions and its operational principle, its models and its hardware/software have been verified. However, a top-level supervising control system is needed to facilitate its integration into future research projects. More specifically, a particularly interesting application for DynACuSo is its use as a Power Hardware-in-the-Loop test-bench for HVDC components and HVDC switch-gear characterization. Engineering efforts in terms of firmware design are needed in order to integrate the prototype into such a testing platform.

Bibliography

[1] M. P. Bahrman and B. K. Johnson, "The ABCs of HVDC transmission technologies," *IEEE Power and Energy Magazine*, vol. 5, no. 2, March 2007.

[2] T. K. Vrana, S. Dennetiere, Y. Yang, J. A. Jardini, D. Jovcic, and H. Saad, "The cigre B4 DC grid test system," 2013.

[3] N. Ahmed, S. Norrga, H. Nee, A. Haider, D. Van Hertem, L. Zhang, and L. Harnefors, "HVDC supergrids with modular multilevel converters — the power transmission backbone of the future," in *International Multi-Conference on Systems, Signals Devices*, March 2012.

[4] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: An overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, March 2009.

[5] E. Kontos, R. T. Pinto, S. Rodrigues, and P. Bauer, "Impact of HVDC transmission system topology on multiterminal dc network faults," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, April 2015.

[6] A. Jehle, "Design and investigation of hybrid HV-DC circuit breaker based on SF6-MCB," Ph.D. dissertation, ETH Zürich, 2021.

[7] ENTSOE, "HVDC links in system operations," *Technical Paper*, 2019.

[8] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, April 2011.

[9] S. M. Sanzad Lumen, R. Kannan, and N. Z. Yahaya, "Dc circuit breaker: A comprehensive review of solid state topologies," in *2020 IEEE International Conference on Power and Energy (PECon)*, 2020.

[10] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, 2021.

[11] R. P. P. Smeets and V. Kertesz, "Evaluation of high-voltage circuit breaker performance with a validated arc model," *IEE Proceedings - Generation, Transmission and Distribution*, vol. 147, no. 2, March 2000.

[12] T. Christen and M. Seeger, "Current interruption limit and resistance of the self-similar electric arc," *Journal of Applied Physics*, vol. 97, no. 10, 2005.

[13] R. P. P. Smeets and V. Kertész, "Application of a validated AC black-box arc model to DC current interruption," in *2nd International Conference on Electric Power Equipment - Switching Technology*, Oct 2013.

[14] M. Walter and C. Franck, "Improved method for direct black-box arc parameter determination and model validation," *IEEE Trans. on Power Delivery*, vol. 29, no. 2, April 2014.

[15] R. P. P. Smeets, A. Yanushkevich, N. A. Belda, and R. Scharrenberg, "Design of test-circuits for HVDC circuit breakers," in *3rd International Conference on Electric Power Equipment – Switching Technology*, Oct 2015.

[16] N. A. Belda and R. P. P. Smeets, "Test circuits for HVDC circuit breakers," *IEEE Transactions on Power Delivery*, vol. 32, no. 1, Feb 2017.

[17] N. A. Belda, C. A. Plet, and R. P. P. Smeets, "Full-power test of HVDC circuit-breakers with ac short-circuit generators operated at low power frequency," *IEEE Transactions on Power Delivery*, vol. 34, no. 5, Oct 2019.

[18] T. Augustin, M. Becerra, and H. Nee, "Advanced test circuit for dc circuit breakers," in *20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, Sep. 2018.

[19] M. M. Walter and C. M. Franck, "Flexible pulsed DC source for investigation of HVDC circuit breaker arc resistance," in *Int. Conf. on Gas Discharges and their Applications*, 2010.

[20] M. M. Walter and C. M. Franck, "Optimal test current shape for accurate arc characteristic determination," *IEEE Transactions on Power Delivery*, vol. 29, no. 4, Aug 2014.

[21] L. Bort, "Characterizing axially blown arcs for passive oscillation dc switches," Ph.D. dissertation, ETH Zürich, 2019.

[22] A. Ritter, "Disconnector switching in HVAC and future HVDC GIS," Ph.D. dissertation, ETH Zürich, 2018.

[23] C. Carstensen, "UnACuSo: A unipolar arbitrary current source for a hardware-in-the-loop test bench," Ph.D. dissertation, ETH Zürich, 2015.

[24] C. Carstensen and J. Biela, "10kV/30kA unipolar arbitrary voltage source for Hardware-in-the-Loop simulation systems for HVDC circuit breakers," in *14th European Conference on Power Electronics and Applications*, Aug 2011.

[25] C. Carstensen and J. Biela, "A new method for investigating the arc behaviour in HVDC circuit breakers based on a novel current source," in *European Conference on Power Electronics and Applications (EPE'12 ECCE Europe)*, Sep. 2012.

[26] K. Algarny, A. S. Abdelrahman, and M. Youssef, "A novel platform for power train model of electric cars with experimental validation using real-time hardware in-the-loop (hil): A case study of gm chevrolet volt 2nd generation," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 3510–3516.

[27] C. S. Edrington, M. Steurer, J. Langston, T. El-Mezyani, and K. Schoder, "Role of power hardware in the loop in modeling and simulation for experimentation in power and energy systems," *Proceedings of the IEEE*, vol. 103, no. 12, Dec 2015.

[28] M. Steurer, F. Bogdan, M. Bosworth, O. Faruque, J. Hauer, K. Schoder, M. Sloderbeck, D. Soto, K. Sun, M. Winkelnkemper, L. Schwager, and P. Blaszczyk, "Multifunctional megawatt scale medium voltage DC test bed based on modular multilevel converter (MMC) technology," in *International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, March 2015, pp. 1–6.

[29] P. Blaszczyk, M. Steurer, D. Soto, F. Bogdan, J. Hauer, M. Sloderbeck, and K. Schoder, "Modular multilevel converter based test bed for mvdc applications — a case study with a 12

kV, 5 MW setup," in *IEEE International Power Electronics and Motion Control Conference (PEMC)*, Sep. 2016.

[30] P. Kotsampopoulos, D. Lagos, N. Hatziargyriou, M. O. Faruque, G. Lauss, O. Nzimako, P. Forsyth, M. Steurer, F. Ponci, A. Monti, V. Dinavahi, and K. Strunz, "A benchmark system for hardware-in-the-loop testing of distributed energy resources," *IEEE Power and Energy Technology Systems Journal*, vol. 5, no. 3, Sep. 2018.

[31] K. Jha and S. Mishra, "Boost-based power amplifier for power-hardware-in-the-loop simulations," in *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Dec 2014.

[32] O. Craciun, A. Florescu, I. Munteanu, S. Bacha, A. I. Bratcu, and D. Radu, "Protection devices testing based on power-hardware-in-the-loop simulation," in *37th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Nov 2011.

[33] A. Chao and W. Chou, "Reviews of accelerator science and technology," 2013.

[34] U. Amaldi, "Particle accelerators: From big bang physics to hadron therapy," 2015.

[35] R. Visintini, "Power converters for accelerators," Baden, Switzerland, 2014.

[36] L.Sermeus, J.Borburgh, A.Fowler, M.Hourican, K.-D.Metzmacher, and M.Crescenti, "The design of the special magnets for PIMMS/TERA," *Proc. of EPAC*, Lucern, Switzerland, 2004.

[37] F. Cabaleiro Magallanes, D. Aguglia, C. de Almeida Martins, and P. Viarouge, "Review of design solutions for high performance pulsed power converters," *15th Int. Power Electronics and Motion Control Conference (EPE/PEMC)*, Sep. 2012.

[38] M. Incurvati, C. Sanelli, and I. De Cesaris, "Feasibility study of high-precision power supply for ramping dipoles of a carbon/proton medical synchrotron," *IEEE Trans. on Applied Superconductivity*, vol. 16, June 2006.

[39] J. A. Sabate, R. R. Wang, F. Tao, and S. Chi, "Magnetic resonance imaging power: High-performance MVA gradient drivers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, March 2016.

[40] J. M. S. et al., "The superconducting cyclotron and beam lines of PSI's new proton therapy facility 'PROSCAN," in *Proc. CYC Conf. Tokyo, Japan*, vol. 1, 2004.

[41] J. Sabate, M. Schutten, R. Steigerwald, Q. Li, and W. F. Wirth, "Ripple cancellation filter for magnetic resonance imaging gradient amplifiers," in *Applied Power Electronics Conf. and Exp. (APEC)*, vol. 2, 2004.

[42] D. W. Lieurance, D. D. Madura, and G. L. Snitchler, "A pulsed magnet system for a field-reversed configuration experiment," *IEEE Trans. on Applied Superconductivity*, vol. 26, no. 4, June 2016.

[43] M. W. Binderbauer, "A high performance field-reversed configuration," *Physics of Plasmas*, vol. 24, no. 5, June 2015.

[44] G. Tsolaridis, S. Fuchs, A. Jehle, M. Pritz, P. Alff, and J. Biela, "High speed, multi-channel, isolated data transmission with a single fiber based on intensity modulation," in *20th European Conference on Power Electronics and Applications (EPE'18 ECCE Europe)*, 2018.

[45] M. Pritz, S. Fuchs, A. Jehle, G. Tsolaridis, and J. Biela, "Low-cost multi-channel data transmission over a single plastic optic fibre for isolated sensing applications," in *21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, 2019.

[46] S. Fuchs, M. Pritz, G. Tsolaridis, A. Jehle, and J. Biela, "Single plastic optical fiber, multiple channel data link for sensing applications with pcb implemented transmitter and receiver," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 3, 2020.

[47] G. Tsolaridis and J. Biela, "Modular, highly dynamic and ultra-low ripple arbitrary current source for plasma research," in *21st International Conference on Pulsed Power (PPC)*, 2017, pp. 1–4.

[48] ——, "Hybrid control concept for highly dynamic buck converter systems," in *19th European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sept. 2017.

[49] G. Tsolaridis and J. Biela, "Interleaved hybrid control concept for multiphase DC-DC converters," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017.

[50] G. Tsolaridis and J. Biela, "Flexible, highly dynamic, and precise 30-ka arbitrary current source," *IEEE Transactions on Plasma Science*, vol. 46, no. 10, pp. 3382–3392, 2018.

[51] G. Tsolaridis, N. Patzelt, and J. Biela, "Output filter with adaptive damping for interleaved converters with low ripple and high dynamics," in *21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sept. 2019.

[52] G. Tsolaridis, P. Seiler, and J. Biela, "High sensitivity current transformer with low settling time, for magnified ac current measurements in pulsed applications," in *22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.10.

[53] D. Christen, "Analysis and performance evaluation of converter systems for EV-ultra-fast charging stations with integrated grid storage," Ph.D. dissertation, ETH Zürich, 2017.

[54] S. Rietmann, S. Fuchs, A. Hillers, and J. Biela, "Field bus for data exchange and control of modular power electronic systems with high synchronisation accuracy of ±4 ns," *IEEJ Trans. on Industry Applications*, vol. 8, no. 2, March 2019.

[55] L. Ni, D. J. Patterson, and J. L. Hudgins, "High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application," *IEEE Trans. on Power Electronics*, vol. 27, no. 3, pp. 1141–1151, March 2012.

[56] N. Wassinger, S. Maestri, R. G. Retegui, J. M. Cravero, M. Benedetti, and D. Carrica, "Multiple-stage converter topology for high-precision high-current pulsed sources," *IEEE Trans. on Power Electronics*, vol. 26, no. 5, pp. 1316–1321, May 2011.

[57] M. Schuck and R. C. N. Pilawa-Podgurski, "Ripple minimization through harmonic elimination in asymmetric interleaved multiphase DC–DC converters," *IEEE Trans. on Power Electronics*, vol. 30, no. 12, Dec 2015.

[58] D. Perreault and J. Kassakian, "Distributed interleaving of paralleled power converters," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 728–734, 1997.

[59] Z. Lukic, S. M. Ahsanuzzaman, A. Prodic, and Z. Zhao, "Self-tuning sensorless digital current-mode controller with accurate current sharing for multi-phase dc-dc converters," in *24th IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 264–268.

[60] R. Miftakhutdinov, "Optimal design of interleaved synchronous buck converter at high slew-rate load current transients," in *IEEE 32nd Power Electronics Specialists Conf. PESC*, vol. 3, 2001, pp. 1714–1718.

[61] D. M. Robert W. Erickson, *Fundamentals of Power Electronics*. Springer, 2001.

[62] D. O. Boillat, "Modular high bandwidth switch-mode three-phase ac voltage source," Ph.D. dissertation, ETH Zürich, 2016.

[63] H. Liu, D. Zhang, and D. Wang, "Design considerations for output capacitance under inductance mismatches in multiphase buck converters," *IEEE Trans. on Power Electronics*, vol. 32, no. 7, July 2017.

[64] P. D. Antoszczuk, R. G. Retegui, N. Wassinger, S. Maestri, M. Funes, and M. Benedetti, "Characterization of steady-state current ripple in interleaved power converters under inductance mismatches," *IEEE Trans. on Power Electronics*, vol. 29, no. 4, April 2014.

[65] M. Jaritz and J. Biela, "Output voltage ripple analysis for modular series parallel resonant converter systems with capacitive output filter," in *European Conf. on Power Electronics and Applications (EPE)*, Sept 2018.

[66] M. R. Pavan Kumar and J. M. S. Kim, "Capacitor current feedback for output filter damping in switched-mode magnet power supplies," *IEEE Transactions on Magnetics*, vol. 30, no. 4, July 1994.

[67] C. Yamazaki, E. Ikawa, T. Yoshino, K. Sato, F. Saito, S. Nakamura, H. Matsumoto, and H. Kobayashi, "Beam acceleration experiment with developed 10 MW class high-precision power supply for accelerator electromagnets," in *Int. Power Electronics Conf. (ECCE ASIA)*, June 2010.

[68] K. Li, G. Xiao, J. Liu, and Z. Wang, "Comparison of four control methods to active power filters applied in accelerator power supplies," in *IEEE 35th Annual Power Electronics Specialists Conf.*, vol. 1, June 2004.

[69] R. W. Erickson, "Optimal single resistors damping of input filters," in *Applied Power Electronics Conf. and Exp. (APEC)*, vol. 2, March 1999.

[70] Semikron, "SKM350MB120SCH17," *Datasheet*, Feb. 2018.

[71] M. Jaritz, "Solid-state modulator for generating high voltage pulses in the ms-range with high output power," Ph.D. dissertation, ETH Zürich, 2018.

[72] U. Choi, F. Blaabjerg, and S. Jørgensen, "Study on effect of junction temperature swing duration on lifetime of transfer molded power IGBT modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 8, 2017.

[73] V. Smet, F. Forest, J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani, "Ageing and failure modes of IGBT modules in high-temperature power cycling," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 10, 2011.

[74] Infineon, "Transient thermal measurements and thermal equivalent circuit models," *Application Note AN2015-10*, Nov. 2018.

[75] J. Muhlethaler, J. W. Kolar, and A. Ecklebe, "A novel approach for 3D air gap reluctance calculations," in *8th International Conference on Power Electronics - ECCE Asia*, 2011.

[76] A. Balakrishnan, W. T. Joines, and T. G. Wilson, "Air-gap reluctance and inductance calculations for magnetic circuits using a Schwarz-Christoffel transformation," *IEEE Transactions on Power Electronics*, vol. 12, no. 4, 1997.

[77] M. K. Kazimierczuk, *High-Frequency Magnetic Components*. A. John Wiley and Sons, Ltd, 2009.

[78] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics - Converters Applications and Design*. John Wiley and Sons, Ltd, 2003.

[79] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with non-sinusoidal waveforms using only Steinmetz parameters," in *IEEE Workshop on Computers in Power Electronics*, 2002.

[80] J. Muehlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under DC bias condition based on steinmetz parameters," in *International Power Electronics Conference - ECCE ASIA*, 2010.

[81] W. Chen, X. Huang, S. Cao, J. Ma, and Y. Fang, "Predicting iron losses in soft magnetic materials under DC bias conditions based on steinmetz premagnetization graph," *IEEE Transactions on Magnetics*, vol. 52, no. 7, 2016.

[82] T. Yoshioka, T. Tsuge, Y. Takahashi, and K. Fujiwara, "Iron loss estimation method for silicon steel sheet taking account of DC-biased conditions," *IEEE Transactions on Magnetics*, vol. 55, no. 6, 2019.

[83] V. C. Valchev and A. Van den Bossche, *Inductors and transformers for power electronics*. CRC Press, 2005.

[84] J. Biela, "Optimierung des elektromagnetisch integrierten serienparallel-resonanzkonverters mit eingepraegtem ausgangsstrom," Ph.D. dissertation, ETH Zürich, 2005.

[85] M. Jaritz and J. Biela, "Analytical model for the thermal resistance of windings consisting of solid or litz wire," in *15th European Conference on Power Electronics and Applications (EPE)*, 2013.

[86] J. L. V. J.H. Lienhard IV, "A heat transfer textbook," *Cambridge MA*, 2000.

[87] J. Biela and J. W. Kolar, "Cooling concepts for high power density magnetic devices," in *Power Conversion Conference*, 2007.

[88] M. Mogorovic and D. Dujic, "Thermal modeling and experimental verification of an air cooled medium frequency transformer," in *19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017.

[89] D. Christen, M. Stojadinovic, and J. Biela, "Energy efficient heat sink design: Natural versus forced convection cooling," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, 2017.

[90] M. Stojadinovic, "Bidirectional DC-DC converters for MVDC applications," Ph.D. dissertation, ETH Zürich, 2020.

[91] A. Bjeletić, L. Corradini, D. Maksimović, and R. Zane, "Specifications-driven design space boundaries for point-of-load converters," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011.

[92] Ed-k, "Power Choke Tester DPG10B Series: Description and Technical Specifications," *Datasheet*, Jan. 2021.

[93] Z. Zimmer, "LMG671 Precision Power Analyzer: Getting precise results doesnot have to be complicated," *Datasheet*, Feb. 2019.

[94] P. E. Measurements, "PEM: CWT Mini," *Datasheet*, Feb. 2020.

[95] IPC, "IPC-2221A, Generic Standard on Printed Board Design," 2003.

[96] Infineon, "External booster for driver IC," *Application Note AN2013-10*, Aug. 2014.

[97] T. Instruments, "Datasheet," *ISO5852S*, Jan. 2017.

[98] Sensitec, "CFS1000: Integrated MagnetoResistive Current Sensor," *Datasheet*, Mar. 2020.

[99] Teledyne, "CP500 current probe: Instruction manual," Jan. 2013.

[100] ——, "High voltage differential probes: HVD3605, HVD3206, HVD310x," May 2017.

[101] M. Steurer, F. Bogdan, W. Ren, M. Sloderbeck, and S. Woodruff, "Controller and power hardware-in-loop methods for accelerating renewable energy integration," in *IEEE Power Engineering Society General Meeting*, 2007, pp. 1–4.

[102] G. Lauss, F. Lehfuß, A. Viehweider, and T. Strasser, "Power hardware in the loop simulation with feedback current filtering for electric systems," in *37th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2011, pp. 3725–3730.

[103] E. Dallago, G. Venchi, S. Rossi, M. Pullia, T. Fowler, and M. Larsen, "The power supply for the beam chopper magnets of a medical synchrotron," in *37th IEEE Power Electronics Spec. Conf.*, June 2006, pp. 1–5.

[104] D. O. Boillat, F. Krismer, and J. W. Kolar, "Design space analysis and ρ– η pareto optimization of LC output filters for switch-mode AC power sources," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6906–6923, 2015.

[105] R. Li, "Modeling average-current-mode-controlled multi-phase buck converters," in *IEEE Power Electronics Spec. Conf.*, June 2008, pp. 3299–3305.

[106] H. S. Bae, J. H. Yang, J. H. Lee, and B. H. Cho, "Digital state feedback control and feed-forward compensation for a parallel module DC-DC converter using the pole placement technique," in *23rd IEEE Applied Power Electr. Conf. (APEC)*, Feb 2008, pp. 1722–1727.

[107] H. Kwakernaak, "Robust control and H-∞ optimization tutorial paper," *Automatica*, vol. 29, no. 2, pp. 255 – 273, 1993.

[108] J. Abu-Qahouq, H. Mao, and I. Batarseh, "Multiphase voltage-mode hysteretic controlled DC-DC converter with novel current sharing," *IEEE Trans. on Power Electronics*, vol. 19, no. 6, pp. 1397–1407, Nov 2004.

[109] W. Stefanutti and P. Mattavelli, "Fully digital hysteresis modulation with switching-time prediction," *IEEE Trans. on Industry Applications*, vol. 42, no. 3, pp. 763–769, May 2006.

[110] D. Mayne, J. Rawlings, C. Rao, and P. Scokaert, "Constrained model predictive control: Stability and optimality," *Automatica*, vol. 36, no. 6, 2000.

[111] P. Karamanakos, T. Geyer, N. Oikonomou, F. D. Kieferndorf, and S. Manias, "Direct Model Predictive Control: A review of strategies that achieve long prediction intervals for power electronics," *IEEE Industrial Electronics Magazine*, March 2014.

[112] J. Allmeling, W. Hammer, and J. Schönberger, "Transient simulation of magnetic circuits using the permeance-capacitance analogy," in *13th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2012.

[113] P. D. Antoszczuk, R. G. Retegui, N. Wassinger, S. Maestri, M. Funes, and M. Benedetti, "Characterization of steady-state current ripple in interleaved power converters under inductance mismatches," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1840–1849, 2014.

[114] D. Gerber and J. Biela, "Interleaving of a soft-switching boost converter operated in boundary conduction mode," *IEEE Trans. on Plasma Science*, vol. 43, no. 10, pp. 3374–3380, Oct 2015.

[115] D. O. Boillat, F. Krismer, and J. W. Kolar, "Optimization and comparative evaluation of multiloop control schemes for controllable ac sources with two-stage LC output filters," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7353–7368, 2016.

[116] V. F. Montagner and S. P. Ribas, "State feedback control for tracking sinusoidal references with rejection of disturbances applied to UPS systems," in *35th Annual Conf. of Industrial Electronics, IECON*, Nov 2009, pp. 1764–1769.

[117] F. H. Dupont, V. F. Montagner, J. R. Pinheiro, H. Pinheiro, S. V. G. Oliveira, and A. Peres, "Comparison of linear quadratic controllers with stability analysis for DC-DC boost converters under large load range," *Asian Journal of Control*, vol. 15, no. 3, pp. 861–871, 2013.

[118] C. Olalla, R. Leyva, A. El Aroudi, and I. Queinnec, "Robust LQR control for PWM converters: An LMI approach," *IEEE Trans-*

actions on Industrial Electronics, vol. 56, no. 7, pp. 2548–2558, 2009.

[119] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, "Feedback control of dynamic systems," *Pearson International Edition*, vol. 5, pp. 1160–1174, March 2001.

[120] P. Franklin and Emami-Naeini, "Feedback control of dynamic systems." Pearson, 2018.

[121] M. Jeong, S. Fuchs, and J. Biela, "High performance lqr control of modular multilevel converters with simple control structure and implementation," in *22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.10.

[122] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: advances and trends," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 935–947, 2017.

[123] D. E. Quevedo, R. P. Aguilera, and T. Geyer, "Model predictive control for power electronics applications," in *Handbook of Model Predictive Control*. Springer International Publishing, sep 2018, pp. 551–580.

[124] Y. Li, Z. Zhang, and R. Kennel, "A full state-variable predictive control of bi-directional boost converters with guaranteed stability," in *22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.7.

[125] A. Bemporad, M. Morari, V. Dua, and E. N. Pistikopoulos, "The explicit linear quadratic regulator for constrained systems," *Automatica*, vol. 38, no. 1, 2002.

[126] M. Jeong, S. Fuchs, and J. Biela, "When FPGAs meet regionless explicit MPC: an implementation of long-horizon linear MPC for power electronic systems," in *46th Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2020, pp. 3085–3092.

[127] A. Babazadeh and D. Maksimovic, "Hybrid digital adaptive control for fast transient response in synchronous buck DC-DC converters," *IEEE Trans. on Power Electronics*, vol. 24, no. 11, pp. 2625–2638, Nov 2009.

[128] S. C. Tan, Y. M. Lai, and C. K. Tse, "General design issues of sliding-mode controllers in DC-DC converters," *IEEE Trans. on Industrial Electronics*, vol. 55, no. 3, pp. 1160–1174, March 2008.

[129] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, "Time optimal, parameters-insensitive digital controller for VRM applications with adaptive voltage positioning," in *11th Workshop on Control and Modeling for Power Electronics*, Aug 2008, pp. 1–8.

[130] T. Geyer, G. Papafotiou, R. Frasca, and M. Morari, "Constrained optimal control of the step-down DC-DC converter," *IEEE Trans. on Power Electronics*, vol. 23, no. 5, pp. 2454–2464, Sept 2008.

[131] C. Song and J. L. Nilles, "Accuracy analysis of hysteretic current-mode voltage regulator," in *20th IEEE Applied Power Electr. Conf.*, vol. 1, March 2005, pp. 276–280.

[132] M. R. Pavan Kumar and J. M. S. Kim, "Capacitor current feedback for output filter damping in switched-mode magnet power supplies," *IEEE Trans. on Magnetics*, July 1994.

[133] F. Cabaleiro Magallanes, D. Aguglia, C. de Almeida Martins, and P. Viarouge, "Active damping filter for high bandwidth - Low ripple pulsed converters," in *15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, Sep. 2012.

[134] C. Yamazaki, E. Ikawa, T. Yoshino, K. Sato, F. Saito, S. Nakamura, H. Matsumoto, and H. Kobayashi, "Beam acceleration experiment with developed 10 MW class high-precision power supply for accelerator electromagnets," in *International Power Electronics Conference (ECCE ASIA)*, 2010, pp. 1526–1529.

[135] I. Marneris, R. Bonati, J. Geller, J. N. Sandberg, and A. Soukas, "The active filter voltage ripple correction system of the brookhaven AGS main magnet power supply," in *Proceedings Particle Accelerator Conference*, vol. 3, 1995.

[136] Kuang Li, Guochun Xiao, Jinjun Liu, and Zhaoan Wang, "Comparison of four control methods to active power filters applied in accelerator power supplies," in *35th IEEE Annual Power Electronics Specialists Conference*, vol. 1, 2004.

[137] Kuang Li, Jinjun Liu, Guochun Xiao, and Zhaoan Wang, "Novel load ripple voltage-controlled parallel DC active power filters for high performance magnet power supplies," *IEEE Transactions on Nuclear Science*, vol. 53, no. 3, 2006.

[138] S. C. Kim, K. M. Ha, J. Y. Huang, and J. H. Choi, "Compact output filter for switching frequency elimination at the PLC linac new magnet power supply," in *IEEE Particle Accelerator Conference*, 2007.

[139] S. C. Kim, K. M. Ha, and J. Y. Huang, "High accuracy and high stability magnet power supply by four-phase buck type DC/DC converter," in *7th Internatonal Conference on Power Electronics*, 2007, pp. 232–237.

[140] M. C. Bastos, "High precision current measurement for power converters," *CERN*, May. 2014.

[141] L. Callegaro, C. Cassiago, and E. Gasparotto, "On the calibration of direct-current current transformers (DCCT)," *IEEE Trans. on Instrumentation and Measurement*, March 2015.

[142] S. Rietmann and J. Biela, "Error induced by the optical path of a high accuracy and high bandwidth optical current measurement system," in *22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, 2020, pp. P.1–P.11.

[143] S. Ziegler, R. C. Woodward, H. H. Iu, and L. J. Borle, "Current sensing techniques: A review," *IEEE Sensors Journal*, April 2009.

[144] N. Kondrath and M. K. Kazimierczuk, "Bandwidth of current transformers," *IEEE Trans. on Instrumentation and Measurement*, vol. 58, no. 6, June 2009.

[145] L. Ghislanzoni and J. A. Carrasco, "A DC current transformer for large bandwidth and high common-mode rejection," *IEEE Transactions on Industrial Electronics*, vol. 46, no. 3, 1999.

[146] F. Costa, E. Laboure, F. Forest, and C. Gautier, "Wide bandwidth, large AC current probe for power electronics and EMI measurements," *IEEE Transactions on Industrial Electronics*, vol. 44, no. 4, 1997.

[147] J. Pankau, D. Leggate, D. Schlegel, R. Kerkman, and G. Skibiniski, "High frequency modeling of current sensors," in *14th Annual Applied Power Electronics Conference and Exposition*, vol. 2, 1999.

[148] Keysight, "Keysight E5061B: Network analyzer 5 Hz to 3 GHz," *Datasheet*, Dec. 2017.

[149] Magnetics, "Powder cores," 2017.

[150] T. Instruments, "Texas instruments OPA 564: 1.5A, 24V, 17MHz power operational amplifier," *Datasheet*, Jan. 2011.

[151] Vishay, "Aluminum Electrolytic Capacitors, Power High Ripple Current, Screw Terminals," *Datasheet*, Jul. 2020.

[152] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, 2015.

[153] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. on Power Electronics*, vol. 30, no. 1, 2015.

[154] TDK, "Aluminum electrolytic capacitors: General technical information," *Application Note*, Dec. 2019.

[155] Vishay, "Introduction, basic concepts, and definitions: Aluminum capacitors," *Application Note*, Nov. 2016.

[156] A. Kuechler, *High Voltage Engineering*. Springer, 2009.

[157] Infineon, "FF1800R12IE5," *Datasheet*, June. 2017.

[158] ——, "FF1800R17IP5P," *Datasheet*, Jan. 2017.

[159] STMicroelectronics, "Current sharing in parallel diodes," *Application Note AN4381*, July 2014.

[160] Ampegon. (1999) Ampegon control unit. [Online]. Available: https://ampegon.com/sales/

[161] L. Bort, T. Schultz, and C. Franck, "Determining the time constant of arcs at arbitrary current levels," in *23rd Symposium on Physics of Switching Arc*, vol. 6, 2019.

Curriculum Vitae

Personal Information

Name	Georgios Tsolaridis
Date of birth	21.01.1991
Place of birth	Thessaloniki, Greece
Nationality	Greek
Contact	tsolaridis@hpe.ee.ethz.ch

Education

2016 – 2021	PhD studies at the Laboratory for High Power Electronic Systems (HPE), ETH Zurich
2014 – 2016	Aalborg University, Master of Science in Power Electronics and Drives
2008 – 2014	Aristotle University of Thessaloniki, Diploma in Electrical and Computer Engineering

Practical Experience

2016 – 2016	Center of Reliability in Power Electronics, Aalborg Research Assistant
2015 – 2016	ABB Corporate Research Center, Vesteras, Sweden Research Internship in Power Electronics
2014 – 2014	Titan Cement Group, Thessaloniki Internship in Electrical Engineering