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Author(s):
Messner, Andreas; Baeuerle, Benedikt; Heni, Wolfgang; De Leo, Eva; Winiger, Joel; Habegger, Patrick; Eppenberger, Marco; Koch, Ueli; Elder, Delwin L.; Dalton, Larry R.; Leuthold, Juerg

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100 Gbit/s NRZ Data Modulation in Plasmonic Racetrack Modulators on the Silicon Photonic Platform

Andreas Messner(1), Benedikt Baeuerle(2), Wolfgang Heni(2), Eva De Leo(2), Joel Winiger(1), Patrick Habegger(2), Marco Eppenberger(1), Ueli Koch(1), Delwin L. Elder(3), Larry R. Dalton(3), Juerg Leuthold(1)

(1) ETH Zurich, Institute of Electromagnetic Fields (IEF), 8092 Zürich, Switzerland
(2) Polariton Technologies AG, 8803 Rüschlikon, Switzerland
(3) Department of Chemistry, University of Washington, Seattle, WA 98195-1700, USA
Author e-mail address: amessner@ethz.ch, leuthold@ethz.ch

Abstract Low power broadband plasmonic silicon-photonic racetrack modulators are introduced. 100 Gbit/s NRZ-OOK and 100 Gbit/s 4-PAM direct detection is demonstrated. The devices feature a bandwidth of 50 GHz, operate with 1.3 V_p and are of interest because of the low on-chip loss characteristics.

Introduction

Low-loss integrated electro-optic modulators with a high bandwidth and low power consumption are sought-after devices for optical communication links.

Recently, many concepts that address these challenges have evolved. Ring modulators feature both a low optical insertion loss and low energy consumption[1-3]. However, their electro-optic bandwidth is often limited by a long photon cavity lifetime.

On the other hand, plasmonic-organic hybrid modulators feature a very large bandwidth,[4] and a very low energy consumption,[5] but at the expense of extra optical insertion loss that are inherent to the technology.

A solution to overcome inherent losses relies on exploiting resonant configurations. The incorporation of plasmonic modulators into ring structures is hence promising. And indeed, a device with a low insertion loss of 2.5 dB, operated at 72 Gbit/s and a bandwidth exceeding 110 GHz has already been demonstrated.[6] However, the device's low Q-factor of ~30 inhibited efficient modulation so that voltage swings of 6.6 V_p were needed.

In this publication, we present introduce a silicon-photonic racetrack resonator with a built-in plasmonic modulator. 100 Gbit/s NRZ-OOK modulation has been achieved with an electrical signal of 1.3 V_p. This is enabled by optimizing the Q-factor to a value of 1250, which allows for efficient modulation, without limiting the bandwidth due to a long photonic lifetime. Measured on-chip losses of only 5 dB are not inherent to the platform and can be further reduced. It should be stressed that the electrical energy consumption of resonator-based devices is inherently loweras compared to Mach-Zehnder modulators.[7]

Plasmonically activated modulator

Fig. 1 shows the electro-optic modulator employed for this experiment. Light is coupled to and from the chip with silicon photonic grating couplers. A 33-µm-long directional coupler maps a fraction of the guided waveguide mode from the bus waveguide into the resonator section. A plasmonic-organic hybrid (POH) phase modulator[8] of 15 µm length and with a 100 nm-wide slot is included in the resonator. The gold electrodes forming the plasmonic metal-insulator-metal slot waveguide also serve as the electric contact pads for a ground-signal pico probe. The chip is coated with the electro-optic organic (OEO) material composite HD-BB--OH/YLD12-4[9].

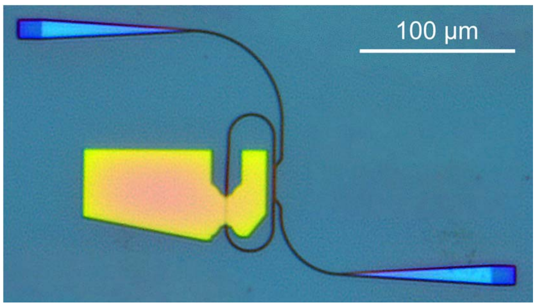

Fig. 1 Microscope image of the silicon racetrack resonator with a 15-µm-long plasmonic active section.

Device Characterization

Fig. 2(a) shows the passive on-chip transmission spectrum of the racetrack modulator. The data has been compensated for the fiber-to-chip coupling losses, which have been determined by cut-back measurements. The transmission in the on-state peaks at ~-5 dB at a wavelength of 1580 nm, and amounts to ~-7 dB at 1550 nm, where the extinction ratio is 39 dB, an indication that the critical coupling condition has been met.

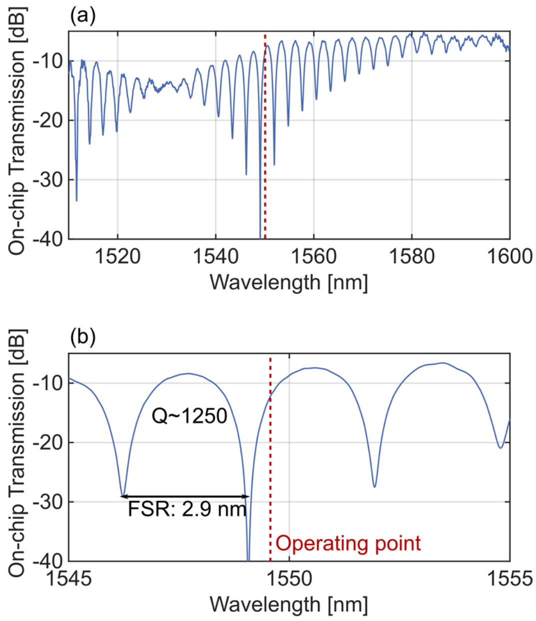

Fig. 2: Transmission spectrum around the operating point. The Q factor is approximately Q=1250, which corresponds to an electro-optical bandwidth of 50 GHz. The red line indicates the operating point. Slight thermal drift was observed upon switching on the laser.

We determined the Q-factor of the resonator by $Q = \lambda_{\mathrm{res}}/\Delta\lambda_{\mathrm{FWHM}}$ and find found a value of $Q \approx 1250$[1]. From that, the cavity lifetime can also be deduced,

$$\tau_{\mathrm{cav}} = \lambda_{\mathrm{res}} \cdot \frac{Q}{2\pi c_0} \approx 1 \text{ fs},$$

where $\lambda_{\mathrm{res}} = 1549.08$ nm is the wavelength of the resonant dip.

Following the approach of Gheorma and Osgood[10], the electrical 3-dB bandwidth can be determined to be

$$f_{3\,\mathrm{dB}} = \frac{1}{2\pi\tau_{\mathrm{f}}}\sqrt{\sqrt{2}-1} \approx 50 \text{ GHz},$$

A DC voltage of 1 V leads to a shift of the resonance wavelength by 0.12 nm. As a phase shift of 2π corresponds to a spectral shift of one full free spectral range, the device's half-wave voltage is deduced to be $12\ \mathrm{V_{DC}}$. We approximate the device by a lumped element capacitor due to its dimensions of <(100x50) µm^2. Therefore, the RF half-wave voltage is $6\ \mathrm{V_{RF}}$ due to voltage doubling.

Data Modulation Experiments

The schematic of the data modulation setup is shown in Fig. 3. A sequence of 2^{17} random bits is loaded onto a digital-to-analog converter (DAC) with 100 GSa/s, an analog 3dB bandwidth of 35 GHz, and an output voltage swing V_p between 0.1 and 0.25 V_p. The output signal is amplified to peak voltages between 0.9 and 2.25 V_p. The bias tee enables the optional tuning of the modulator's operating point by applying a DC signal.

Light from a tunable laser is fed to the chip via a grating coupler. The optical power fed to the modulator is ~3 dBm. The modulated output signal is amplified in an erbium-doped fiber amplifier, attenuated to a power level of 8-10 dBm and fed to a high-speed pin photodiode.

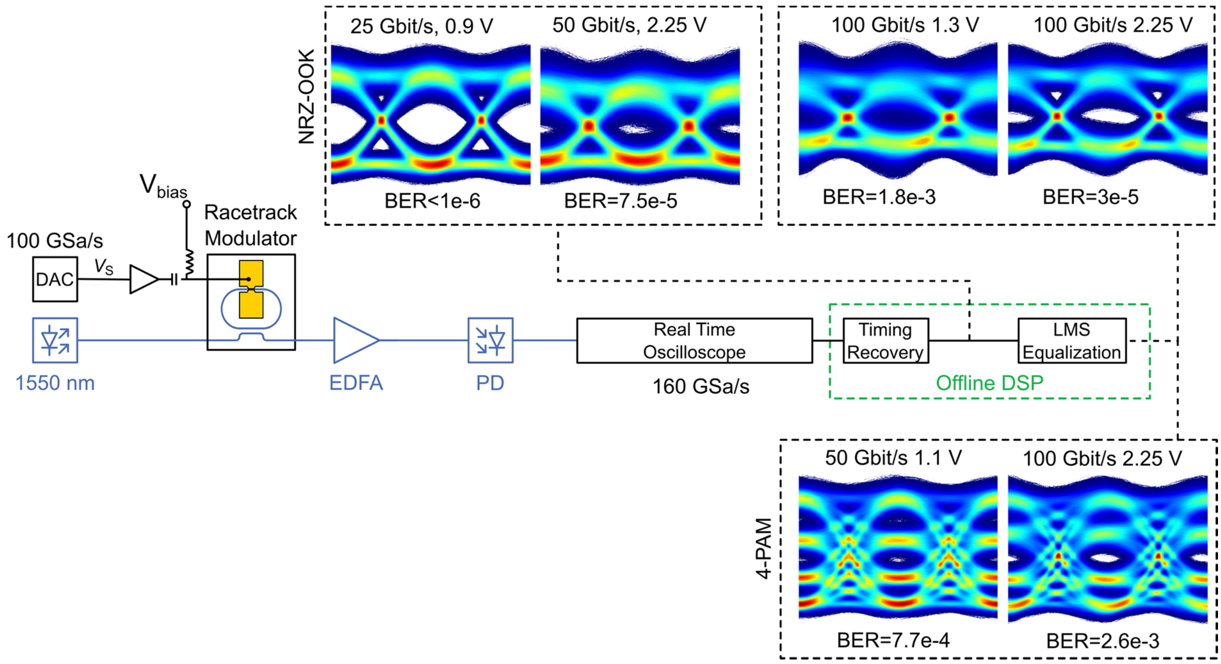

Fig. 2: Schematic of the data modulation experiment. Insets show the received eye diagrams either after TR or LMS equalization. The BERs of all measurements are below the 7% HD-FEC threshold, those of 50 and 100 Gbit/s NRZ-OOK are compliant with the Ethernet standard KP4-FEC.

A bias tee with a terminated DC port acts as a DC block between the photodiode and a realtime oscilloscope (63 GHz bandwidth, 160 GSa/s), which records the signal. The offline DSP includes timing recovery, an optional T/2-spaced feed forward equalization, a hard symbol decision and counting of the bit errors.

Tab. 1 and 2 show a detailed summary of the data measurements. Bit error ratios (BER) are always below the hard-decision forward error correction (HD-FEC) threshold of $3.8 \cdot 10^{-3}$. For data rates below 50 Gbit/s (25 GBd and 50 GBd OOK, 25 GBd 4PAM) only timing recovery without any further equalization was applied. 25 Gbit/s and 50 Gbit/s OOK signals are even compliant with the Ethernet-standard KP4-FEC limit of $2 \cdot 10^{-4}$. For 100 Gbit/s (50 GBd 4-PAM and 100 GBd OOK), a T/2-spaced feedforward equalizing (FFE) step was employed after the timing recovery. The FFE is trained with a data-aided least mean square (LMS) update over the first 30% of the received symbols and is afterwards applied statically.

Tab. 1 Summary of the NRZ-OOK data modulation experiments. TR: only timing recovery performed, LMS: timing recovery and linear equalization performed.

Data Rate [Gbit/s]	**25**	**50**	**100**	
V_p @ 50 Ω [V]	0.9	0.9	1.3	2.25
DSP	TR	TR	LMS	LMS
BER	0	$7.5 \cdot 10^{-5}$	$1.8 \cdot 10^{-3}$	$3 \cdot 10^{-5}$

Tab. 2 Summary of the 4-PAM data modulation experiments.

Data Rate [Gbit/s]	**50**	**100**
V_p @ 50 Ω [V]	1.1	2.25
DSP	LMS	LMS
BER	$7.75 \cdot 10^{-4}$	$2.57 \cdot 10^{-3}$

The on-chip losses of 5 dB are by no means a fundamental limit. The plasmonic losses can be reduced by further reduced by 2-3 dB by means of an electronic codesign of the modulator drivers.[11]

Conclusions

We have demonstrated plasmonic silicon-photonic racetrack modulators. A Q-factor of 1250 and the resulting 3-dB cutoff frequency of 50 GHz have been engineered to provide high modulation efficiency and sufficient bandwidth for 100 Gbit/s NRZ-OOK modulation with a drive voltage peak of only 1.3 V_p. The on-chip device losses of 5 dB do not represent an inherent limit of the technology as they can be further reduced.

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