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Impact of Reduced Gate-to-Source Spacing on Indium Phosphide High Electron Mobility Transistor Performance

*Diego Calvo Ruiz, Daxin Han, Giorgio Bonomo, Tamara Saranovac, Olivier Ostinelli, and Colombo R. Bolognesi**

Indium phosphide (InP)-based high electron mobility transistors (HEMTs) with an offset gate enable higher maximum oscillation frequency (f_{MAX}) values because of the resulting reduction in gate-to-source resistance. Following this approach, improved direct current (DC) characteristics and cutoff frequencies ($f_T/f_{MAX} > 410/710$ GHz with $L_G = 50$ nm) are shown with respect to centered gate devices. However, HEMTs with an offset gate show degraded noise performances compared with centered gate devices because of a higher gate leakage current. The results show that offsetting the gate closer to the source is not desirable for ultra-low-noise performance.

1. Introduction

Indium phosphide (InP)-based high electron mobility transistors (HEMTs) are widely applied in radio-astronomy and deep-space communications systems because of their high speed, high gain, and low-noise performance.[1] HEMTs currently are the fastest available transistor technology[2] due to excellent 2D electron gas transport properties and to the optimization of transistor size and device parasitics and have enabled amplification above 1 THz in monolithic microwave integrated circuits (MMICs).[3]

The introduction of an asymmetric gate recess[4,5] and its combination with reduced distance between gate and source ohmic contacts[6,7] have enabled records in maximum oscillation frequency (f_{MAX}),[8] as it can effectively reduce the drain conductance g_d and the gate-to-drain capacitance C_{GD}. The effects of these strategies on device noise properties have, however, not been reported. We here report the first study of InP HEMTs with a source offset (i.e., with a reduced gate-to-source distance) compared with devices with a gate centered in the source–drain gap in terms of radio frequency (RF) and noise performances.

2. Process Technology

Figure 1 shows a cross section of the molecular beam epitaxy-grown epitaxial layer structure used in this work, which features: semi-insulating InP substrate, AlInAs buffer, InAs/GaInAs/InP composite channel, AlInAs spacer, Si δ-doping, AlInAs Schottky barrier layer, InP etch stop, and highly n^+-doped GaInAs cap layer. The composite channel contains a 3 nm InAs inset and a 2.5 nm InP subchannel together with 1.25 and 2.75 nm GaInAs cladding layers. Van der Pauw measurements were performed at 300 and 77 K with the n^+ GaInAs cap removed, revealing that the layer stack exhibits excellent electron mobility (12 800 $cm^2 V^{-1} s$ at 300 K and 37 600 $cm^2 V^{-1} s$ at 77 K) and carrier density (2.8×10^{12} cm^{-2} at 300 K and 3.7×10^{12} cm^{-2} at 77 K). Although substituting the InP subchannel for lattice-matched GaInAs further increases the carrier mobility,[9] devices with the detailed layer structure present ultra-low-noise performance due to their reduced gate leakage currents and lowered channel impact ionization levels.[10]

Device fabrication began with the formation of the source and drain ohmic contacts by an evaporated Ge/Au/Ni/Au metal stack with a 1 μm S–D spacing. Following rapid thermal annealing (RTA) under a high flow of forming gas (5% H_2:95% N_2), device isolation was carried out by wet chemical etching using hydrochloric, phosphoric, and succinic acid-based highly selective solutions. Next, the gate region was recessed by the selective removal of the n^+-GaInAs cap layer after the patterning of a single layer of polymethyl methacrylate (PMMA) with a 30 kV electron beam exposure (EBL). As shown in **Figure 2**, the gate recess width was fixed to 200 nm, but two different distances between the source electrode and the gate recess were considered: 400 nm (symmetric, gate recess center in the S–D gap of 1 μm) and 200 nm (asymmetric). In both cases, the T-gate electrode was formed by evaporation of a Pt/Ti/Pt/Au metal stack in the center of the gate recess region to center gate foot in the recess (symmetric recess but offset gate position) after a two-step EBL process. The gates were sunk through the InP etch stop and into the AlInAs barrier as per the study given by Saranovac et al.[11] and passivated with a 15 nm Al_2O_3 layer by atomic layer deposition (ALD). Careful investigation with focused ion beam (FIB) on both structures confirmed a 50 nm gate footprint, as shown in **Figure 3**.

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Pt/Ti/Pt/Au Buried Gate
Source
Drain
GaInAs Cap
InP Etch-Stop
AlInAs Barrier
δ-Doping
AlInAs Spacer
Composite Channel
$Ga_{44}In_{56}As$ 1.25 nm
InAs Inset 3 nm
$Ga_{44}In_{56}As$ 2.75 nm
InP 2.5 nm
AlInAs Buffer
InP Substrate

Figure 1. Schematic cross section of the fabricated InP HEMTs.

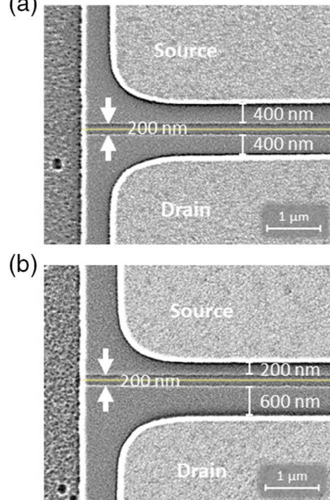

Figure 2. Scanning electron microscopy images of gate recess between source and drain ohmic contact pads for a) symmetric recess and b) gate recess 200 nm closer to the source contact. Gate footprint position is illustrated in yellow to show its mid-recess-centered position. The gate length is 50 nm for both.

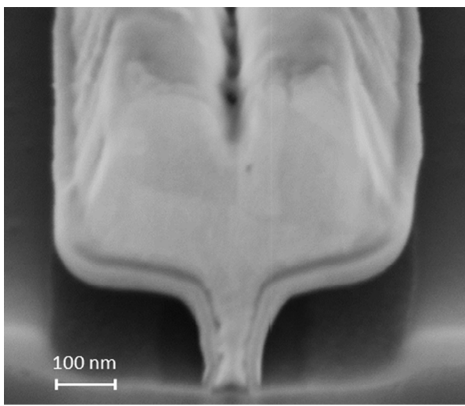

Figure 3. Cross-sectional FIB image of the fabricated gates with a gate footprint L_G of 50 nm.

To complete the fabrication, a Ti/Au overlay metallization was e-beam evaporated to enable good probing conditions.

3. Characterization

Direct current (DC) measurements were performed at 300 K with an HP4156B semiconductor parameter analyzer for representative 2 × 50 μm devices with $L_G = 50$ nm. As shown in **Figure 4**,

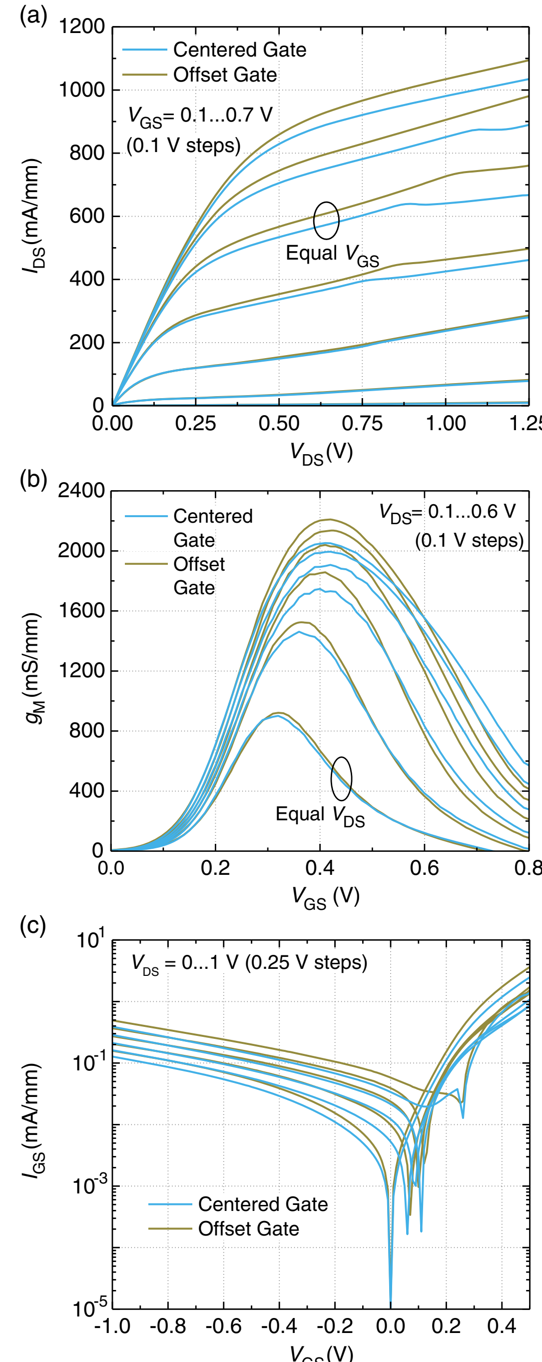

Figure 4. a) DC drain characteristics, b) transconductance, and c) diode characteristics of 50 nm gate (2 × 50) μm devices measured at 300 K.

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an offset gate closer to the source exhibits a 6% higher maximum DC output current I_{DS} and an 8% increase in maximum DC transconductance g_M. Although both structures present nearly ideal behavior (no visible Kink effect[12]), the offset gate device exhibits a higher leakage current (48% higher at $V_{GS} = 0.3$ V and $V_{DS} = 0.75$ V) due to the reduced distance with the source electrode. Simultaneously, the threshold voltage remains unchanged.

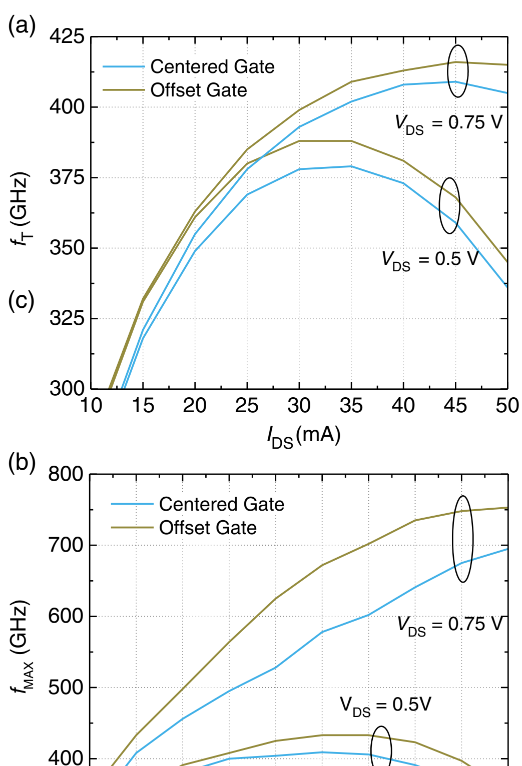
Microwave performance was measured up to 40 GHz with a power network analyzer N5247A vector network analyzer using a line-reflect-reflect-match (LRRM) calibration and on-wafer OPEN and SHORT pads with the same geometry as actual devices. The extracted current-gain and power-gain cutoff frequencies (f_T and f_{MAX}), obtained with iterative de-embedding[13] and single-pole fits to $|h_{21}|^2$ and Mason's unilateral power gain U, are plotted for each case in **Figure 5**a,b as a function of the drain current, I_{DS}, at the drain bias voltages V_{DS} of 0.5 and 0.75 V. As expected, the offset gate HEMT with a reduced gate-to-source distance shows improved RF performances, reaching a 16% higher f_{MAX} than the symmetric structure. In addition, Figure 5c shows the transistor microwave performance when biased at $I_{DS} = 40\ \text{mA mm}^{-1}$ and $V_{DS} = 0.75$ V. It should be noted that the iterative de-embedded extraction procedure provides cleaner U data compared with conventional OPEN–SHORT methods,[13] but extracted values are slightly lowered (conventional de-embedding yields $f_{MAX} > 800$ GHz instead of 732 GHz for the offset gate device).

The noise performance of our composite InAs/GaInAs/InP channel HEMTs was assessed using an HP 346C K01 noise source and an MT984AU impedance tuner, together with an MT7553 noise receiver and down-converter module from Maury Microwave via the cold-source technique.[14] Noise modeling was performed using the Keysight's Advanced Design System (ADS) software with Pospieszalski's method, i.e., assuming that parasitic resistances contribute only to the thermal noise and assigning effective temperatures to the gate (T_g) and drain (T_d) to compute the noise properties of the active chip.[15] The minimum noise figure NF_{MIN} was extracted from noise parameter measurements performed from 8 to 40 GHz. As shown in **Figure 6**, the offset gate configuration shows a degraded NF_{MIN} by up to 0.3 dB, whereas it offers a 2.9 dB higher gain at 40 GHz at a low-noise bias.

4. Discussion

Small-signal equivalent circuit analysis[16] reveals that offsetting the gate can effectively improve the small-signal transconductance g_m. As shown in **Figure 7**, the gate-to-source capacitance C_{GS} is increased, and the gate-to-drain capacitance, C_{GD}, is lowered by offsetting the gate. The opposite trend is seen for the access resistances, R_D and R_S. These tendencies in extracted elements reflect the RF improvement obtained by offsetting the gate, in accordance with Equation (1) and (2). Despite their differences, both structures benefit from the larger conduction band offsets and enhanced carrier confinement of their InAs insets and, thus, achieve superior cutoff frequencies.[17]

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{gs} + C_{gd})(1 + \frac{R_s + R_d}{R_{ds}}) + g_m C_{gd}(R_s + R_s)} \quad (1)$$



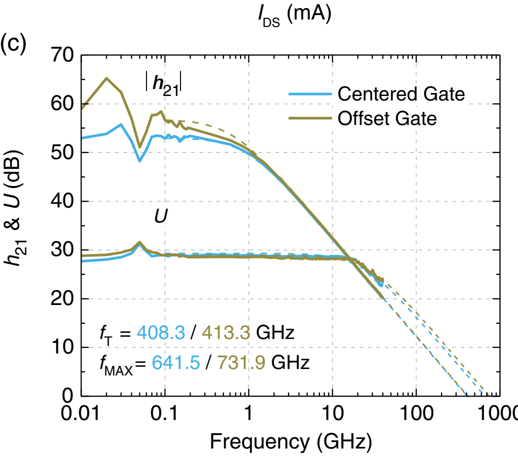


Figure 5. a) RF short-circuit current gain cutoff frequency f_T versus I_{DS} at $V_{DS} = 0.5$ V and $V_{DS} = 0.75$ V for 50 nm gate (2×50) μm devices measured at 300 K, b) maximum oscillation frequency f_{MAX} versus I_{DS} at $V_{DS} = 0.5$ V and $V_{DS} = 0.75$ V for the same devices, and c) representative de-embedded extrapolation of $|h_{21}|^2$ and Mason's maximum unilateral gain U for both considered devices biased at $V_{DS} = 0.75$ V and $I_{DS} = 40$ mA.

$$f_{max} = \frac{f_T}{2\sqrt{\frac{R_g + R_s + R_{gs}}{R_{ds}} + 2 \cdot \pi \cdot f_T \cdot C_{gd} \cdot R_g}} \quad (2)$$

To quantify the drain current increase caused by impact ionization in the channel, the impact ionization transconductance

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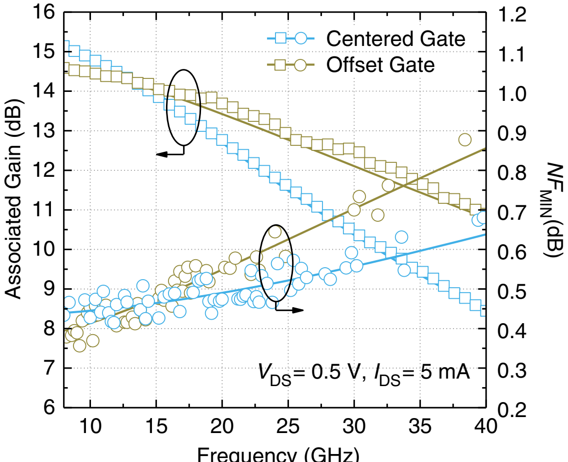

Figure 6. Measured and modeled minimum noise figure NF_{MIN} and the associated gain of the fabricated 50 nm gate (2 × 50) μm HEMTs biased at $V_{DS} = 0.5$ V and $I_{DS} = 5$ mA (50 mA mm^{-1}) at 300 K.

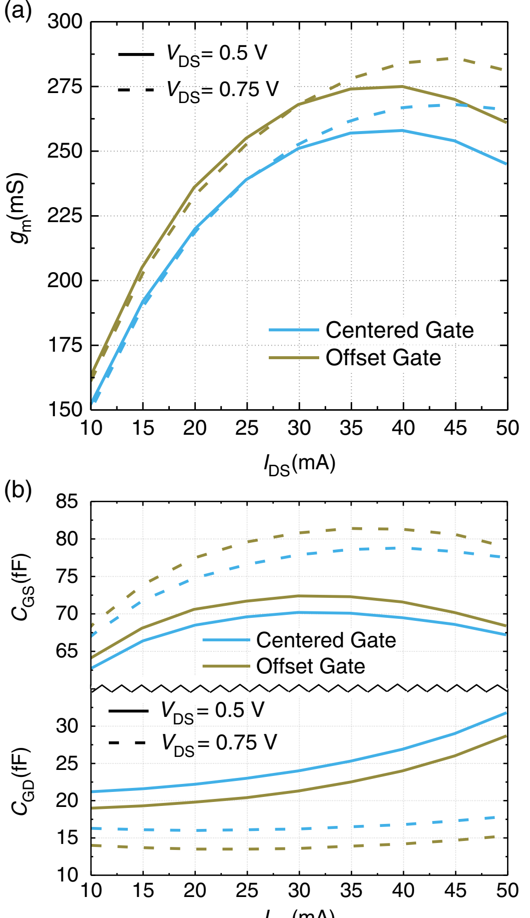

Figure 7. a) Extracted intrinsic small-signal transconductance g_M and b) gate-to-source capacitances C_{GS} and gate-to-drain capacitances C_{GD} versus I_{DS} for both considered devices biased at $V_{DS} = 0.5$ V and $V_{DS} = 0.75$ V at 300 K.

g_{im} was extracted as per.[16] Both structures present comparable g_{im} values, drastically reduced compared with those achieved in a similar structure with a 5 nm InAs inset in the GaInAs channel (9.5 nm total thickness).[10] At $V_{DS} = 0.75$ V and $I_{DS} = 15$ mA, the offset gate structure presents $g_{im} = 5.5$ mS, whereas the gate-centered device shows $g_{im} = 5.2$ mS, more than 48% lower than the g_{im} value obtained in the InAs/GaInAs composite channel structure. This improvement, in accordance with the absence of Kink effect (shown in Figure 4), is mainly due to the lowered impact ionization rate of the InP subchannel with respect to GaInAs. Therefore, a reduced channel thermal noise is experienced at high drain to source voltages V_{DS} because of the real space electron transfer from the GaInAs channel to the InP subchannel.[18]

The gate leakage current is an important parameter for noise performance.[19] As reported in Figure 4c, the gate leakage current increases when the gate is placed closer to the source electrode. Hence, this behavior leads to degradation in the measured NF_{MIN} (as shown in Figure 6) and counteracts the increased f_{MAX} values obtained by offsetting the gate.

With only a few atomic layers remaining in-between the highly conducting channel and the gate metal, the gate leakage current is mainly attributed to the tunneling quantum effect.[20] In our fabrication technology, the gate-to-channel distance is defined during the gate sink-in annealing step. After the gate metal lift-off, Pt is diffused controllably thorough the InP etch stop and part of the AlInAs barrier with nanometer precision.[11] To determine the impact of the diffusion depth of our sunk gates, an additional sample was processed in parallel using a lower Pt thickness (3 instead of 4 nm) during the gate metal evaporation with the same offset gate configuration as detailed previously. As shown in **Figure 8**a, the device with thinner Pt exhibits reduced leakage current due to the increased gate-to-channel distance (72% lower leakage at $V_{GS} = 0.3$ V and $V_{DS} = 0.75$ V). However, it also shows a 5% decrease in maximum DC output current I_{DS} and a 6% reduction in maximum DC transconductance g_M. Following the same tendency, devices with the 3 nm Pt layer present a degraded RF performance: the maximum f_{MAX} is lowered by 14% and 15% at $V_{DS} = 0.5$ V and $V_{DS} = 0.75$ V, respectively (Figure 8b). This behavior is again consistent with the extracted small-signal equivalent circuit: the extracted small-signal transconductance g_m and gate-to-source capacitance C_{GS} are reduced, whereas the access resistances are decreased due to the enlarged gate-to-channel distance. The extracted impact ionization transconductance g_{im} of devices with thinner Pt is marginally lowered at high drain bias but present similar values at both $V_{DS} = 0.5$ V and $V_{DS} = 0.75$ V compared with the structure with the 4 nm Pt layer. Because of its reduced gate leakage current, structures with thinner Pt exhibit improved NF_{MIN}, as shown in Figure 8c. Therefore, the results of devices with offset gates and thinner Pt are similar to those obtained with symmetric gate recess and thicker Pt. Despite these similarities, the noise performance of symmetric structures is not outperformed by decreasing the Pt thickness. At 40 GHz, HEMT with symmetric recess still offers an NF_{MIN} 0.5 dB lower than the device with offset gate thinner Pt.

Although several models associate high gate leakage currents with a degraded noise performance,[21,22] classical approaches also predict an improved NF_{MIN} when the cutoff frequencies

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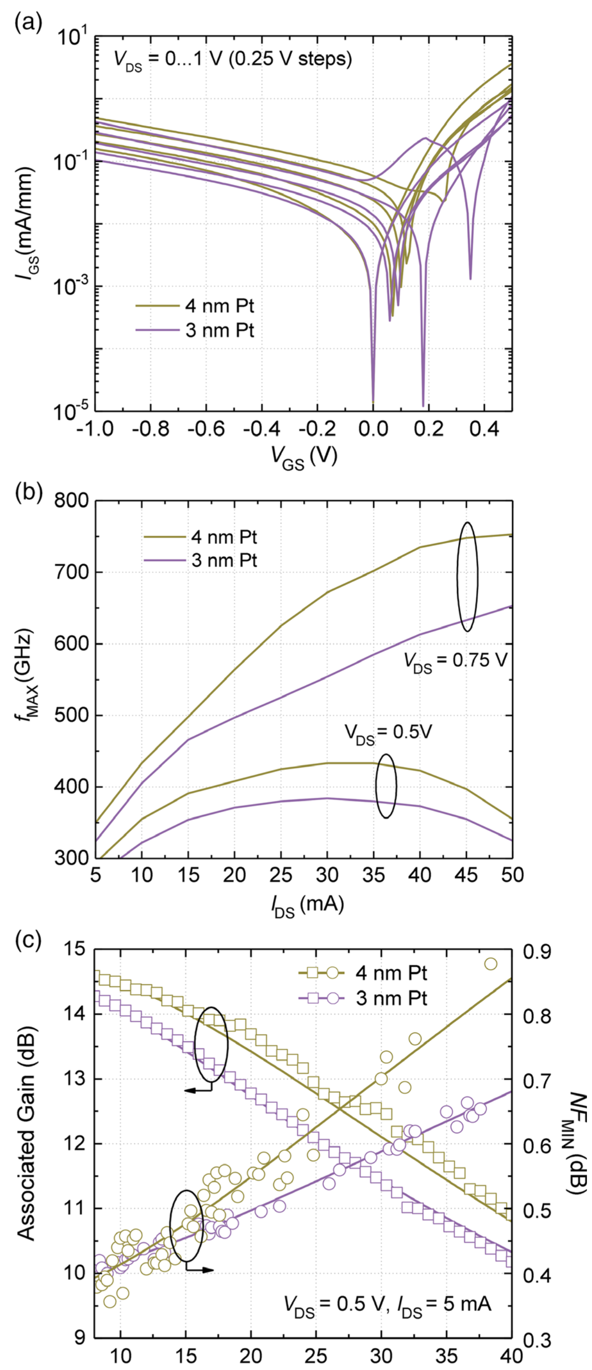

Figure 8. a) DC diode characteristics, b) maximum oscillation frequency f_{MAX} versus I_{DS} at $V_{DS} = 0.5$ V and $V_{DS} = 0.75$ V, and c) measured and modeled minimum noise figure NF_{MIN} for 50 nm gate (2 × 50) μm devices with the offset gate layout of Figure 2b with different gate Pt thicknesses at 300 K.

are improved.[23] Development of ultra-low-noise devices through offset gates confronts a tradeoff situation where improvements in f_T/f_{MAX} are correlated with degraded noise performance due to the corresponding higher gate leakage current levels. The same behavior is expected if thinner barriers and shorter gate lengths are used to achieve higher transconductances.[24] Other optimization methods to reach superior cutoff frequencies, such as the introduction of a thicker narrow bandgap material in a composite InAs/GaInAs channel, also lead to degraded noise characteristics due to the increased impact ionization levels.[9] Thus, the advanced level of maturity of current InP HEMTs entails separate development paths tailored either for high-frequency or low-noise applications.

5. Conclusion

Despite DC and RF notable peak performance improvements accrued by offsetting the gate toward the source, gate leakage current also increases and leads to a degraded noise behavior at low-noise bias conditions. High gate leakage current levels potentially arise from several mechanisms, including wave function barrier penetration or impact ionization. Devices with offset gates exhibit increased diode tunneling currents due to their reduced distance between source and gate electrodes. Although decreasing the gate Pt thickness by 1 nm can effectively reduce the gate leakage current due to the increased gate-to-channel distance, devices with such a metal gate stack also present degraded maximum DC transconductance g_M and RF performances.

The present findings reveal a tradeoff scenario where improvements in f_T and f_{MAX} are not associated with enhancements in noise performance. In fact, devices with superior RF performances tend to present a degraded NF_{MIN} due to their increased leakage current. Recent HEMT developments to reach gain at higher frequencies, such as shorter gate lengths, high mobility narrower gap channels, or thinner barriers, usually lead to higher gate leakage currents and channel impact ionization levels and thereby increase NF_{MIN} at both low and high frequencies. Therefore, the presented tradeoff between high-speed and low-noise performance may suggest different optimization paths for each application.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

direct current, gate-to-source spacing, indium phosphide high electron mobility transistors, noise characterization, radio frequency

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