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A Monolithic Bipolar CMOS Electronic-Plasmonic High-Speed Transmitter

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ABSTRACT

In order to address the challenge of increasing data rates, next generation optical communication networks will require the co-integration of electronics and photonics. Heterogeneous integration of these technologies has shown promise, but will eventually become bandwidth limited. Faster monolithic approaches will, therefore, be needed, but monolithic approaches using complementary metal–oxide–semiconductor (CMOS) electronics and silicon photonics are typically limited by their underlying electronic or photonic technologies. Here, we report a monolithically integrated electro-optical transmitter that can achieve symbol rates beyond 100 GBd. Our approach combines advanced bipolar CMOS with silicon plasmonics, and addresses key challenges in monolithic integration through the co-design of the electronic and plasmonic layers, including thermal design, packaging, and a nonlinear organic electro-optic material. To illustrate the potential of our technology, we develop two modulator concepts – an ultra-compact plasmonic modulator and, alternatively, a silicon-plasmonic modulator with photonic routing – both directly processed onto the bipolar CMOS electronics.

1 Introduction

Future communications systems will require the co-integration of electronic and photonic systems. A key example is optical transmitters: electro-optical devices that convert electrical information to the optical domain for signal transmission. Such devices should currently offer dozens of Gb/s of data speed on a compact footprint, while being cost- and energy-efficient[1]. However, data centres and computing infrastructures will shortly require Tb/s data rates in a single optical link[2,3]. This calls for parallelization and high line data rates, and to achieve such data rates, the co-integration of high-speed electronics and high-bandwidth photonics is needed.

Integration of electronics and photonics is typically achieved heterogeneously using two separate chips. Transmitters using vertical-cavity surface-emitting lasers[4] have demonstrated energy-efficient data links at up to 56 GBd[5-7]. However, such directly modulated sources are bandwidth limited and higher symbol rates are hard to achieve[1]. Externally modulated sources and external modulators offer a photonic high-speed alternative, and photonic solutions based on lithium niobate[8,9], indium phosphide[10-18], silicon[19-25] and plasmonics[26-29] have emerged for intensity modulation and direct detection (IM/DD) systems. So far, heterogeneous transmitters in bondwire assembly[14,17,25,29] have shown the highest symbol rates, achieving 222 GBd with plasmonics[29], 192 GBd with indium phosphide photonics[17], and 56 GBd with silicon photonics[25]. However, parasitics at the mismatched bondwire interface eventually constitute a bottleneck to the speed. Alternatively, three-dimensional bonding or flip-chip assemblies can reduce the interface parasitics[30], with 100 GBd operation being demonstrated using indium phosphide photonics[14]. Yet, heterogeneous integration remains a costly and non-ideal approach since two separate high-performance chips are interfacing at the most critical position of highest data bandwidth.

Monolithic integration could overcome this bottleneck and reach higher symbol rates using ultra-short direct connections known as on-chip vias. This use of a common substrate could offer a more compact footprint, simplified testing and lower costs. However, most electronic and photonic technologies rely on two incompatible material platforms, and thus new approaches are required. The silicon CMOS technology could provide a cost- and energy-efficient solution for both electronics and photonics[31-34]. A full photonic library on a zero-change CMOS platform with a 10 GBd data link has, in particular, been demonstrated[33], and has shown modulation at 40 GBd[34]. However, standard CMOS technology is bandwidth limited and cannot achieve the symbol rates of high-speed heterogeneous demonstrations. Alternative monolithic solutions relying on indium phosphide or bipolar CMOS (BiCMOS) technologies are therefore of interest. BiCMOS could be of particular value because it offers high-speed electronics and is CMOS-compatible. In addition, plasmonics is, in principle, an ideal counterpart as a photonic technology[35], offering bandwidths in excess of 500 GHz[36] and compatibility with a variety of substrate materials[37].

In this Article, we report a monolithically integrated BiCMOS electronic-plasmonic transmitter[38] that can achieve symbol rates beyond 100 GBd. The transmitter is comprised of high-speed BiCMOS electronic layers and a plasmonic layer on a single chip. The electronic layers offer a BiCMOS circuit that has been designed in line with data-centre standards and performs a 4:1 power multiplexing to deliver on-off keying (OOK) signals to the plasmonic layer above. The plasmonic layer consists of compact and high-bandwidth plasmonic Mach-Zehnder modulators (MZM). The electronic and plasmonic layers are interconnected by vias. The chips have been designed to operate at elevated temperatures and are tested in uncooled data modulation experiments. Operation at 120 GBd is demonstrated using a silicon-plasmonic MZM, and an ultra-compact modulator is created that shows operation at

100 GBd on a footprint of 29 × 6 µm^2. Neither the BiCMOS electronics nor the plasmonic technologies operate at their fundamental speed limit, suggesting that our approach could provide a route to 200 GBd and beyond.

2 Concept

Our monolithically integrated high-speed transmitter is conceptually depicted in Fig. 1. The transmitter consists of BiCMOS electronic layers (blue) and a plasmonic top layer (red), which are implemented on a common substrate and connected through electrical wires (vias). The zoom-in to the plasmonic modulator shows the direct high-speed connection of electronics with plasmonics.

In the electronic layer stack (blue), electrical signals are generated to drive the plasmonic modulators. A multiplexer (MUX), designed in agreement to data centre standards, achieves highest data rates by performing a 4:1 multiplexing. The MUX input data is either externally supplied or generated on-chip. At the MUX output, a power multiplexing stage replaces the standard output driver amplifier to achieve highest signal quality in an energy-efficient implementation[39]. The SiGe BiCMOS platform hereby not only offers highest speeds and CMOS-compatibility but also enables monolithic integration with photonic components based on the silicon technology.

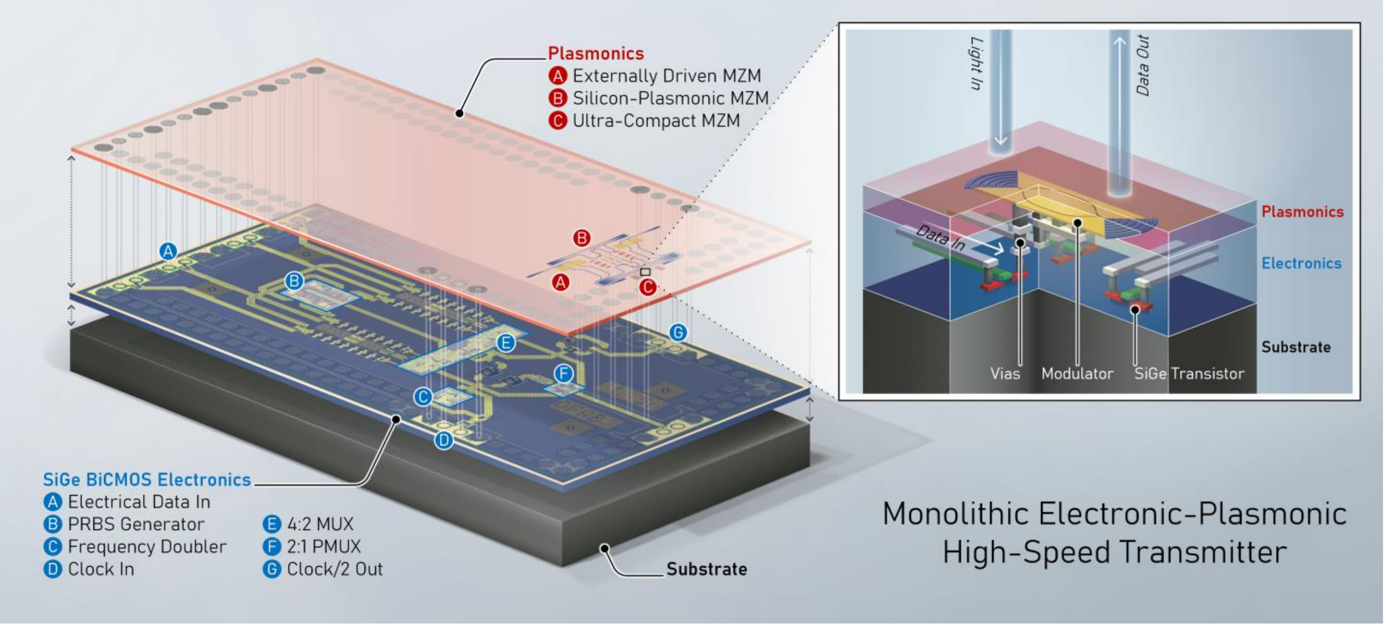


Fig. 1: Monolithic electronic-plasmonic high-speed transmitter. High-speed SiGe BiCMOS electronic layers (blue) with a top plasmonic layer (red) monolithically integrated on a common substrate (black) and connected through on-chip vias (cylinders). The electronic circuit performs a 4:1 power multiplexing onto a single high-speed data rate channel. Data inputs are either external or from an on-chip PRBS generator. The optical layer comprises plasmonic MZMs that convert the electrical signals onto intensity-modulated optical carriers. The zoom-in shows an ultra-compact monolithically integrated MZM directly driven by high-speed electronics. The compact dimensions of plasmonic devices demonstrate the perspective towards densest integration of highly parallelized transmitters as anticipated for future optical communication links.

The plasmonic layer (red) comprises silicon photonics and gold plasmonics in a top layer – photonics for passive and plasmonics for active components. In this layer, plasmonic Mach-Zehnder modulators (MZMs) convert the electrical signals into the optical domain through light intensity modulation for reception with direct detection. Plasmonic modulators, despite having increased insertion loss, are an ideal solution as they offer ultra-compact footprint[40], independence of photonic substrates[37], high electro-optical bandwidth[36], energy-efficient modulation[41] and operation at CMOS-compatible voltages[42]. The transmitter comprises two types of plasmonic MZMs on a single substrate. A silicon-plasmonic MZM using photonic waveguides[43] was implemented together with an alternative ultra-compact plasmonic MZM, where direct fiber-to-modulator coupling has been integrated into the device (see zoom-in of Fig. 1). Both modulator types have been simultaneously driven, which is possible due to the compact size and small capacity of plasmonic modulators.

The electronic layers and the plasmonic layer are connected by on-chip vias. Vias at the final power multiplexer (PMUX) stage bring the electrical output signal directly to the plasmonic modulators. The proximity of the PMUX outputs to the plasmonic modulators enables best signal quality at highest speed. Additional vias for high-speed electrical interfaces are connecting the bondpads in the top layer with the electronic circuit beneath. They give access to data input and clock in- and output. Note that the compactness of the plasmonic modulators allows describing them as electrically lumped elements. This renders their electrical impedance a design parameter and allows trading in driving voltage and energy consumption (see Methods).

Power dissipation in the high-speed electronics can lead to excess heating with temperatures hot spots above 150°C. Hence, thermal co-design of electronics, plasmonics and packaging was crucial to successfully demonstrating a monolithic transmitter (see Methods). Moreover, plasmonic switching in the modulators takes advantage of a nonlinear electro-optic effect in an organic material[44]. Here, a new nonlinear organic electro-optic (OEO) material 2:1 HLD1:HLD2[45] has been applied for the first time in a device, which enables operation at elevated temperatures. This organic material system mixes the anthracene-containing chromophore HLD1 and the acrylate-containing chromophore HLD2, and allows for crosslinking without additional agents. Its thermal stabilization has guaranteed reliable operation at temperatures beyond 120°C.

In this configuration, we demonstrate for the first time 120 GBd data modulation with a monolithically integrated transmitter.

3 Electronics

The electronics of the monolithically integrated chip needs to meet multiple demands. First, the data input interface needs to be compatible with standard data centre sources. Second, a sufficiently high voltage swing with smallest possible power consumption must be generated to drive the MZM at symbol rates of at least 100 GBd. Third, a semiconductor technology well-suited for a photonic monolithic integration is required.

The electronic circuit that forms the MUX to drive the plasmonic modulator is shown with its corresponding building blocks in Fig. 2a. The design considerations are presented in the following with the focus on the monolithical integration together with an on-chip MZM. Details concerning the circuit development and performance can be found in Refs.[46,47] for a previous version. The present implementation is detailed in Ref.[48]. A 4:1 MUX topology allows for conversion of data-centre-compatible 4 × 25 Gb/s non-return-to-zero (NRZ) on-off-keying (OOK) input signals to a 100 Gb/s NRZ-OOK output signal at the MZM. Integrated delay locked loops (DLL) align the input data to the MUX clock, see inset of Fig. 2a, and thereby automatically compensate for a timing skew between the data inputs[49]. Regarding the use of the circuit in an integrated transmitter, a trade-off between performance and power consumption has to be chosen. The presented design is optimized to reach highest performance and to provide a large flexibility in order to enable the characterization of the transmitter under various conditions (see Methods). Thanks to a wideband circuit design, the chip can be operated at flexible data rates. For this, only the input clock frequency has to be adjusted correspondingly.

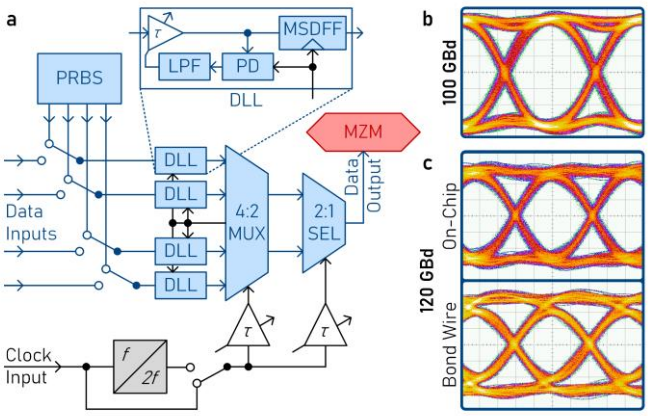


Fig. 2: Electronic 4:1 power multiplexer performance. ***a*** *Simplified block diagram of the electronics. The inset shows a DLL element comprising an adjustable time delay, a master-slave-D-flipflop (MSDFF), a phase detector (PD) and a low-pass filter (LPF).* ***b-c*** *electrical eye diagram measurements. Scaling: 2 ps/div, 200 mV/div.* ***b*** *100 GBd on-chip reference eye diagram.* ***c*** *120 GBd on-chip eye diagram compared to a 120 GBd eye diagram via a bondwire interface.*

To drive the MZM, a power multiplexer (PMUX) concept is chosen such that no additional driver amplifier is required. Instead, the final 2:1 selector (SEL) stage of the MUX directly drives the MZM. This offers several advantages[39,47]. For the present application, the good signal quality at high data rates and the low power consumption should especially be highlighted. The final 2:1 SEL has a power consumption of 0.9 W when operating with a nominal differential voltage swing of 2 V_{pp} (1 V_{pp} single-ended) at highest data rates. The PMUX concept can readily be extended to implement a PAM-4 transmitter by parallel connection of a second output stage with halved output swing and reduced power consumption. For the present design, this option is not implemented, however, it offers the potential to reach even higher data rates and higher energy efficiency. Design considerations concerning the adaption of the output interface to the MZM are presented in the Methods.

For the implementation, the BiCMOS semiconductor technology SG13G2 from IHP (adaptions in Methods) with a high transit frequency f_T = 300 GHz of the bipolar transistors has been chosen. Compared to compound technologies (e.g. InP), which offer higher transit frequencies (e.g. f_T = 400 GHz enabling the fastest MUX known so far with 222 Gb/s[29]), a BiCMOS technology brings the advantages of being cost-efficient and enabling a dense co-integration of high-speed bipolar electronics with standard CMOS signal processing. Moreover, there are developments of faster BiCMOS technologies that allow for an increase in the data rate of the presented circuit.

To assess the performance of the electronics (and of the MZM) without the need for an external data source, an on-chip pseudo-random bit sequence (PRBS) generator has been integrated and connected to the data inputs. On-chip measurements with a wafer probe at a chip variant with an electrical output interface demonstrate the performance of the electronics. The presented circuit delivers a flat operation for clock frequencies up to 90 GHz (limited by measurement equipment), which was tested by applying a 1-0-1-0 sequence[48]. Data modulation experiments show a clear open eye diagram for a data rate of 100 Gb/s, see Fig. 2b. Due to the external 50 Ω load of the measurement equipment, the voltage swing of 1.2 V_{pp} is only half of the voltage swing at an integrated high-ohmic MZM. A comparison between an on-chip measurement and when interfaced by bondwires at a data rate of 120 Gb/s shows, how bondwires reduce the eye opening by almost 20 % and hereby degrade the signal quality, see Fig. 2c. This demonstrates the advantage of monolithic integration, where no bondwires are needed.

4 Plasmonics

The plasmonic MZMs are the principal optical components in the demonstration for a monolithic integrated transmitter. Three plasmonic modulator concepts were pursued in this work and integrated in the plasmonic layer: Two silicon-plasmonic MZM concepts, one driven with the internal MUX and one externally driven as a reference, and a new ultra-compact MZM concept. All three concepts are based on the 500 GHz plasmonic modulator technology[36] and have a built-in asymmetry in order to tune the operation point in the optical domain without the need of an electrical bias. Fig. 3 introduces the new concept, depicts the co-integrated modulators and demonstrates the capabilities of monolithic integrated MZMs.

The first modulator concept is based on silicon photonic waveguides and splitters and relies on previous demonstrations from our group[27,43]. Standard single mode fibres connect to this device via grating couplers. Silicon photonic multimode interference coupler split and combine the optical carrier. A photonic delay line in one arm of the Mach-Zehnder interferometer allows choosing the MZM operation point by tuning the optical wavelength. The actual modulation is performed in two plasmonic phase modulators[50] that operate in push-pull mode. The co-integrated silicon-plasmonic MZM offers an extinction ratio of 35 dB with a total insertion loss of 25 dB. Fig. 3b depicts a scanning electron microscope (SEM) image of the two modulator arms of the actual monolithic MZM.

The second concept is the ultra-compact plasmonic MZM with a footprint of only $29 \times 6\ \mu m^2$, which is optically connected through a 24 µm pitched optical fiber array (OFA), see Fig. 3a. The direct fiber-to-slot coupling scheme shown in the inset efficiently converts an optical fiber mode directly into a plasmonic slot mode, omitting losses in intermediate photonic components[40]. Metallic y-splitters split and combine the optical carrier. Asymmetric arm lengths cause a phase difference between the two MZM arms and fix the operation point. Two plasmonic phase modulators constitute the MZM, which is driven in push-pull mode. Fig. 3c shows an SEM image of the ultra-compact modulator co-integrated with electronics, which offers an extinction ratio above 10 dB and insertion losses of 27 dB.

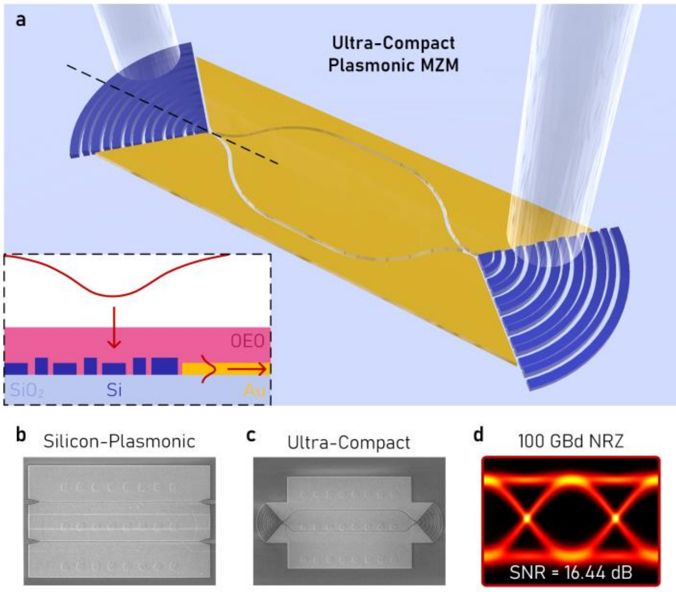


Fig. 3: Monolithic integrated plasmonic Mach-Zehnder modulators. ***a*** *Ultra-compact plasmonic MZM with a footprint of $29 \times 6\ \mu m^2$ for co-integration with electronics. The inset shows a schematic of the grating coupler for direct fiber-to-slot conversion.* ***b-c*** *SEM images of the actual monolithic modulators before OEO material deposition.* ***b*** *Silicon-plasmonic MZM and* ***c*** *ultra-compact plasmonic MZM.* ***d*** *Eye diagram of a 100 GBd data modulation experiment of a monolithically integrated MZM on the same chip using an external driver. 100 Gb/s NRZ-OOK were modulated with a BER < 10^{-5}.*

As a reference, an externally driven monolithic MZM was processed on the same chip to evaluate the performance of integrated plasmonic devices on BiCMOS chips – but without interface to the electronics. Hereby, the plasmonic modulator with insertion losses of 25 dB and an extinction ratio of 30 dB has been operated under ideal conditions at room temperature. An amplified electrical data signal (V_p = 2.71 V, V_{rms} = 1.55 V) has been applied to the modulator via an RF probe, which results in a higher voltage swing than for integrated solutions and does not need a bandwidth-limiting bondwire interface. 100 GBd data modulation was demonstrated with a bit error ratio (BER) < 10^{-5} for two-level modulation (NRZ-OOK) (setup and measurement in Methods). Fig. 3d depicts the corresponding eye diagrams. The received signal quality of 16 dB signal-to-noise ratio (SNR) indicates an enormous potential for symbol rates beyond 200 GBd[51].

5 Monolithic Integration

The monolithic integration of electronics and plasmonics was confronted with a set of challenges from platform compatibility over module assembly to high processing demands. While the electronic chips were produced in a SiGe BiCMOS foundry, the plasmonic top layer and the bondpads were post-processed directly onto the electronic chip in the in-house facilities. In a final step, chip assembly and wirebonding to a dedicated printed circuit board (PCB) as well as packaging and connectorisation were performed. The final monolithic test module is depicted in Fig. 4, where the subfigures show zoom-ins at different scales – centimetre to micrometre scale – on which the monolithic integration was optimized. Fig. 4a shows the complete test module with DC and RF connectors and a PCB bringing the differential input data, clock and DC supply to the transmitter chip. Fig. 4b shows the bondwire assembly connecting PCB and transmitter chip. Fig. 4c shows a microscope image of the monolithic transmitter chip. Electronics and plasmonics were integrated on the same chip. A zoom-in to the plasmonic devices is shown in the last subfigure, see Fig. 4d.

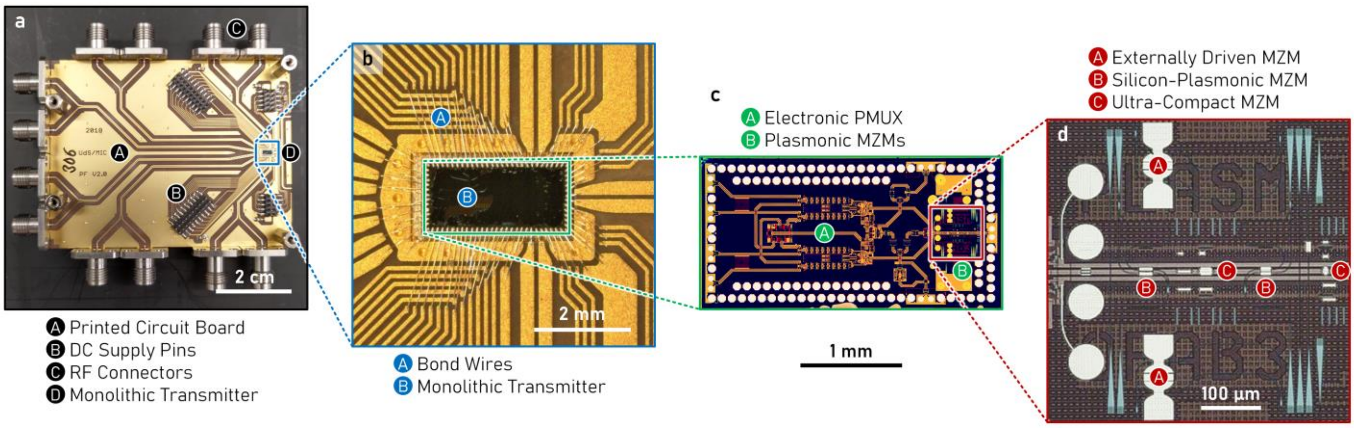


Fig. 4: Blow-up of the monolithic transmitter assembly. ***a*** *Full transmitter assembly with PCB, DC supply pins and RF connectors.* ***b*** *Monolithic transmitter chip connected via bondwires to the PCB.* ***c*** *Monolithic transmitter chip.* ***d*** *Zoom-in onto the output stage with the plasmonic MZM devices on top of the electronic driver circuits.*

The electronic chip features five output positions, which are driven simultaneously. This allows the implementation of multiple photonic components for evaluation – among which are the two plasmonic MZM concepts presented above. This placement of multiple modulators is only possible for modulators with small capacitances, whose simultaneous operation does not affect the electrical signal quality along the output transmission line. Such an adaption of the electronic MUX would not be possible with alternative photonic concepts.

A major challenge for monolithic integration is the high temperature environment in proximity to electronics. Recent demonstrations showed temperature stability in organic-based plasmonic modulators up to 75°C[41], while the electronic chips reach 150°C at the core and up to 125°C at the output stage. Thermal modelling of the transmitter chip allowed for improved placement of the modulators along the output transmission line (see Methods). Still, to prevent degradation at high temperatures, a new nonlinear organic electro-optic material 2:1 HLD1:HLD2 was developed[45]. A crosslinking procedure stabilized the organic material such that it can withstand temperature above 120°C (see Methods). On-chip temperature measurements verified uncooled operation of the monolithic transmitter at local temperatures above 112°C. This is the first demonstration of plasmonic transmitters operating in such elevated temperature environment.

6 Monolithic Transmitter Performance

The monolithic transmitter was tested in a data modulation experiment with symbol rates of up to 120 GBd under uncooled ambient air conditions and without encapsulation. The experimental setup is schematically given in Fig. 5. An RF synthesizer serves as a clock source for the electronic circuit, which generates a PRBS data sequence of 2^9-1 bits with symbol rate of twice the input clock frequency. An external laser serves as light source and delivers 5 to 11 dBm optical input power to the chip (measured in fiber before chip). Light is coupled in and out of the monolithic transmitter through optical fibres. Two types of plasmonic MZMs (see section 4) were simultaneously driven – a silicon-plasmonic MZM and an ultra-compact plasmonic MZM. The modulated optical signal was transmitted over an optical fiber link to the receiver. The signal was amplified and filtered before being received with direct detection by a single photodiode. Five million samples of the converted signal are captured using 63 GHz real-time oscilloscope with 160 GS/s. Offline digital signal processing (DSP) was applied for signal recovery and equalization. Fig. 5a and b show the eye diagrams of different data rates for the two MZM types (full details in Methods). 120 GBd were modulated with the silicon-plasmonic MZM with a BER of $1.74 \cdot 10^{-2}$ and 100 GBd with the ultra-compact design with a BER of $3.95 \cdot 10^{-2}$. The lower-speed performance of the ultra-compact MZM is associated to a non-optimal operation point of the MZM, as the device is only tuneable to the ideal quadrature operation point through a voltage bias. Here, a voltage bias in the electronic layer has been omitted in order to guarantee maximum signal quality at highest speed. Still, both BERs are below $4 \cdot 10^{-2}$ as required for successful soft-decision forward error correction[52].

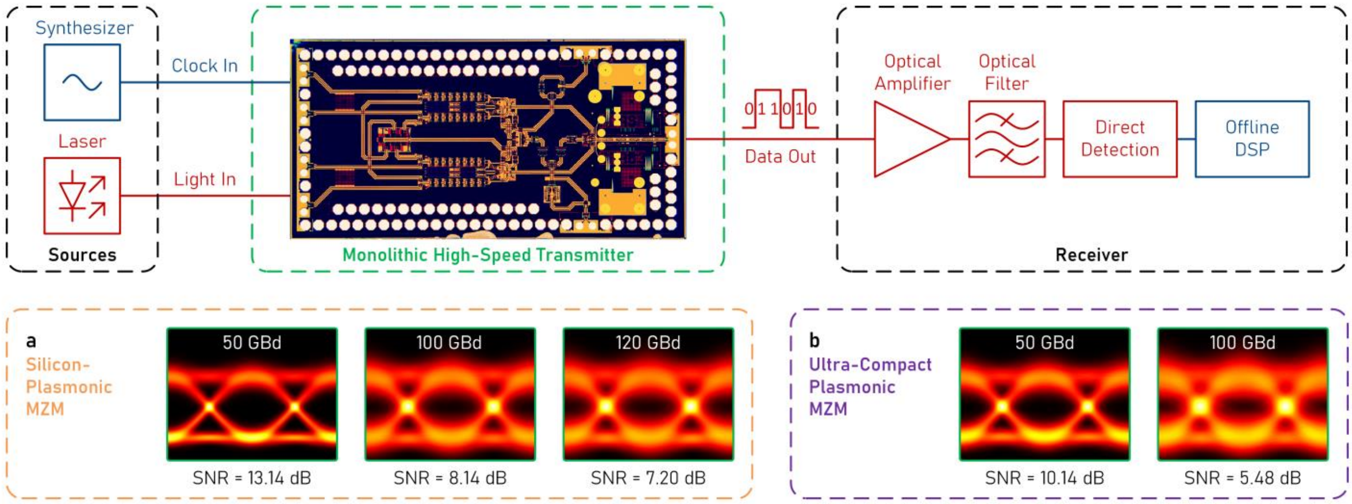


Fig. 5: Data modulation experiment with monolithic transmitter. The transmitter is operated using on-chip PRBS generation. The symbol rate thereby corresponds to twice the input clock. Optically, light from a laser source is coupled to the plasmonic MZMs, where it is modulated before being transmitted via a fiber link. At the receiver, the optical signal is amplified and filtered before being launched to a direct detection receiver. ***a*** *Eye diagrams and SNR for 50, 100 and 120 GBd as obtained with the silicon-plasmonic MZM.* ***b*** *Eye diagrams and SNR for 50 and 100 GBd measured with an ultra-compact plasmonic MZM.*

7 Conclusions

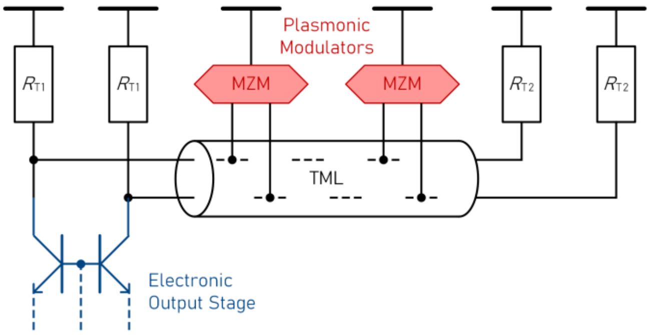
Our approach offers a solution to a key challenge in next generation communication networks – the high-speed co-integration of electronics and photonics – and provides a route to overcome the speed limitations in current transceiver systems. We developed a monolithic integration platform that combines high-speed BiCMOS electronics with high-bandwidth plasmonics connected through direct on-chip interfaces. The platform offers high-speed data transmission, achieving symbol rates beyond 100 GBd. This was achieved through the co-design of electronics and photonics, including thermal design and a nonlinear organic electro-optic material. Both the BiCMOS electronics and plasmonic technologies are not yet at their limits, and symbol rates beyond 200 GBd should be possible.

8 Methods

8.1 Electronic Advantages of Monolithic Integration

Due to the monolithical integration of photonics and electronics on a single chip, the design of the output interface as shown simplified in Extended Data Fig. 1 can be adapted to the MZM load. In contrast, for systems with an external MZM, the output impedance of the electronics (R_{T1}) is typically designed as 50 Ω to match the characteristic impedance of transmission lines (TML). As the MZM (R_{T2}) is typically matched to 50 Ω to terminate the far end of the external TML, the voltage swing at the MZM is only half the source voltage swing for an open output ($R_{T2} \rightarrow \infty$). In case of the monolithically integrated plasmonic MZM, a termination at both ends is not required as the size of the MZM is small and thus can be assumed as electrically lumped. Thus, a single termination that acts as a simple load resistor is sufficient, which doubles the output voltage swing compared to an external MZM without an increase in current consumption. In principal, because of the low MZM load capacitance, the matching can also be chosen larger than 50 Ω, which even decreases the current consumption further. For the current implementation, however, a concept is chosen, where an on-chip TML is matched at one end only by its characteristic impedance of 50 Ω ($R_{T1} \rightarrow \infty$, R_{T2} = 50 Ω). This allows multiple positions to place the MZM and thus gives a degree of freedom for the experiments by choosing an optimal position with respect to temperature, signal quality and integration processing. In our experiments, four MZMs are positioned at dedicated positions along the TML. In the design of the electronics, the MZM capacitance is modelled by an increase in the distributed TML capacitance. The related TML inductance is designed for a wave impedance of 50 Ω. That allows for a single 50 Ω termination at the end of the TML whereby the signal amplitude along the TML (i.e. at each of the MZMs along the TML) is approximately constant.

In addition to the advantages of the single termination of the lumped MZM, the monolithic integration significantly reduces parasitic inductances and capacitances of the output interface as the interconnect length between output stage and MZM is much shorter than for a heterogeneous approach as neither bondpads nor bondwires are required. This lead to a higher bandwidth at the MUX-MZM interface.



Extended Data Fig. 1: Simplified interface between electronic output stage and plasmonic Mach-Zehnder modulator (MZM). Typically, both output stage and modulator are terminated by 50 Ω. In our case, the plasmonic MZM can be modelled as electrically lumped, which allows for single-end termination. Hence, the driving voltage is doubled without increase in energy consumption. Additionally, such an approach allows tuning of the output impedance to specific needs.

8.2 Adaption of BiCMOS Process & Post-Processing

To enable the monolithic integration of plasmonic modulators on a BiCMOS electronic chip, the standard BiCMOS fabrication process has been adapted. Normally, the BiCMOS platform does not provide a flat topography at the end of the backend of line (BEOL) process and inter-metal vias are not directly accessible. To enable electronic-plasmonic integration, the top-metal2 interconnect level and passivation were omitted and the chemical-mechanical polishing process was optimized to allow for both low resistance access to the interconnect vias (about 2 Ω per electrode or 16 Ω per via) and a smooth surface for modulator post-processing with a root mean square roughness of 0.35 nm.

The post-processing of the plasmonic modulators was performed directly on top of the BiCMOS electronic chip and aligned to the driver's output vias. The passive silicon-photonic structures were etched into a 220 nm thick silicon layer, which was deposited at 300°C in plasma-enhanced chemical vapour deposition. The plasmonic modulators were structured using a lift-off process for 150 nm of gold deposited by electron-beam evaporation. In a last step, the OEO material was deposited by spin-coating. In order to stay below the thermal budget of a BiCMOS electronic chip, all processes were performed at temperatures not exceeding 300°C.

8.3 Specifications of the Transmitter Module

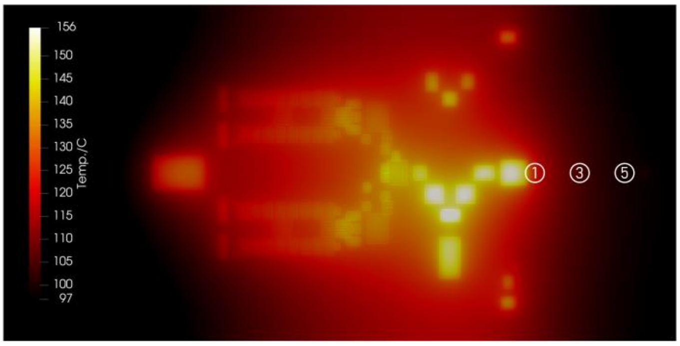
The main specification of a transmitter module is its performance in terms of maximum symbol rate, which was targeted in this demonstration. However, side specifications such as energy consumption and active device area are becoming more and more relevant with increasing integration. Extended Data Fig. 2 shows both active area and power consumption for each of the electronic circuit parts. The final 2:1 SEL and the high-speed clock distribution (50 GHz) are the critical electronic components that have to be integrated on the transmitter chip. The other circuit parts are optional and are implemented to show advanced functionalities and for testing purposes. First, a 4:2 MUX is implemented in order to allow external data input at 25 GBd as in former data centre standards for NRZ. Second, a circuit for input data alignment allows compensating for a timing skew on-chip. Third, a reference clock out is added as an optional feature for clock synchronization in the measurement system. Further, a frequency doubler serves as an alternative way to reach high-speed clock frequencies exceeding externally available speeds. Last, an on-chip PRBS generator offers convenient and fast testing capabilities without external data input and complements the external data inputs. Regarding the power consumption, the consumed energy-per-bit amounts to 28 pJ/b for the critical on-chip circuit parts and 99 pJ/b for the full transmitter electronics including all optional features. To analyse the data rate per unit area, the footprints of the plasmonic modulators have to be measured. The area of the silicon-plasmonic MZM covers 13,000 µm^2, while the ultra-compact plasmonic MZM occupies an extremely compact area of only 400 µm^2. By adding these values to the active area of the critical electronic components, a data rate per unit area of 2.39 Tb/s/mm^2 for the silicon-plasmonic and of 2.65 Tb/s/mm^2 for the ultra-compact transmitter is found.

Circuit Parts	Active Area	Power
Final 2:1 SEL (MZM driver)	13,200 µm^2	0.9 W
High-speed clock distribution (50 GHz)	24,150 µm^2	1.9 W
Subtotal for critical components	**37,350 µm^2**	**2.8 W**
4:2 MUX	60,500 µm^2	1.4 W
Input data alignment	288,000 µm^2	2.4 W
Reference clock output	24,000 µm^2	0.9 W
Frequency doubler	35,200 µm^2	0.7 W
PRBS generator	101,000 µm^2	1.7 W
Total for all components	**546,050 µm^2**	**9.9 W**

Extended Data Fig. 2: Active area and power consumption per circuit part. The operation-critical functions (2:1 SEL and clock distribution) are separated from the optional parts for advanced functionalities and for measurement purposes.

8.4 High Temperature Environment

Monolithic transmitters experience a high temperature environment due to power consumption on smallest areas. This has a significant influence on the transmitter performance. The temperature distribution on a transmitter chip has therefore been computed in simulations. The power is dissipated mainly in the transistors and resistors in the electronic layers and the released heat is conducted to the chip backside, which is coupled to a heat sink using a thermally conductive adhesive. The thermal model consists of the chip, which is discretized as an FEM tetrahedral mesh, and the adhesive modelled by its thermal surface resistance to the heat sink, which is considered as a constant temperature constraint. As the adhesive coverage of the chip backside is not known exactly, two cases are considered: ideal and reduced thermal conduction to the heat sink. The temperature map for the reduced case is depicted in Extended Data Fig. 3. A maximum temperature of 156°C has been simulated at the core, which decays just below 100°C towards the chip edges. Multiple output positions to place the modulator have been implemented. Beneath every odd output position and beneath the MUX core, a temperature diode has been placed to measure the local on chip temperature. The measured values from a purely electronic chip and a post-processed transmitter chip are stated in the table inset of Extended Data Fig. 3. The electronic chip thereby agrees well with the ideal conducting simulation, while the post-processed transmitter chip experiences about 20°C higher temperatures. The same difference is found in simulations for lower thermal conduction to the substrate. Therefore, the temperature rise is assumed to be caused by the adhesive for transmitter assembly on the PCB.



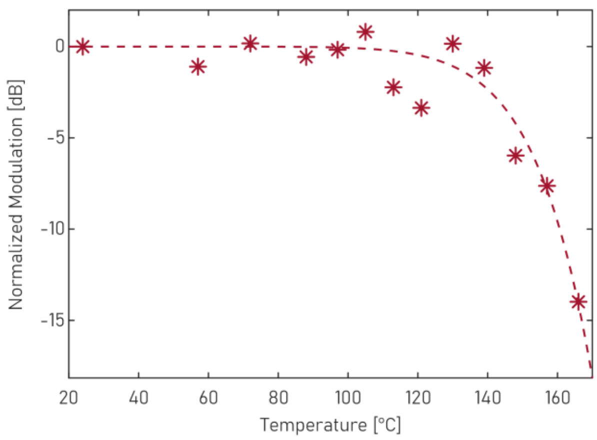
Position	Core	MZM1	MZM3	MZM5
Simulated (ideal thermal cond.)	135°C	106°C	88°C	82°C
Simulated (reduced thermal cond.)	156°C	124°C	112°C	106°C
Measured (w/o post-processing)	151°C	106°C	91°C	81°C
Measured (with post-processing)	156°C	123°C	112°C	101°C

Extended Data Fig. 3: Temperature map of monolithic transmitter. Thermal simulations of the electronic circuit revealed the temperatures listed in the table inset, which have been compared to measurements with on-chip temperature diodes. Ideal and reduced thermal conduction to the substrate match well with measurements on a raw electronic chip and a post-processed transmitter chip, respectively.

8.5 Temperature-Stable Nonlinear Organic Electro-Optic Material

Temperature-stable nonlinear organic electro-optic (OEO) materials are a requirement for stable operation of monolithic integrated plasmonic modulators. Besides temperature stability, the OEO material should maintain its high electro-optic activity and large intrinsic bandwidth. The OEO material composite 2:1 HLD1:HLD2 exhibits exactly these properties[45]. The material's glass temperature can rise by up to 100°C to a maximum of 175°C using a crosslinking procedure while keeping a maximum thin-film electro-optic coefficient r_{33} of about 286 pm/V at 1310 nm wavelength. A thermostability measurement over 500 hours at 85°C in a vacuum oven confirmed the long-term stability (99%) of the organic material.

In this work, we applied the OEO material 2:1 HLD1:HLD2 for the first time in an actual device and demonstrated data modulation at temperatures above 112°C. The OEO material was poled with a poling field of 180 V/µm and crosslinked at 150°C. Note that the monolithic modulators were connected to the electronics during this process. The in-device temperature stability was evaluated by steadily increasing the chip temperature and measuring the modulation efficiency using a sinusoidal signal at 60 GHz phase modulated onto an optical carrier at 1550 nm wavelength. Extended Data Fig. 4 depicts the measurement results. The in-device OEO performance shows stable operation up to 140°C after which the performance starts to degrade. The small dip at about 120°C is associated to fluctuations in the measurement setup due to fiber instabilities because of thermal fluxes.



Extended Data Fig. 4: Temperature stability of the nonlinear organic electro-optic material. Stable operation until about 140°C was measured with a drastic degradation when reaching the glass temperature of 150°C. The small dip at 120°C is due to thermally induced setup fluctuations. The trend line (dashed) serves to guide the eye.

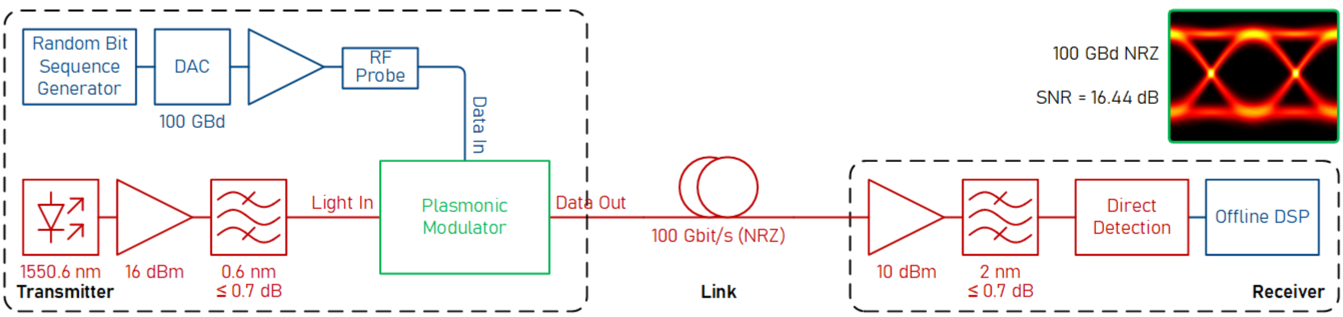
8.6 Characterization of Monolithic Modulators

The two plasmonic modulator concepts were characterized in optical transmission measurements. Typical silicon-plasmonic MZMs achieve fiber-to-fiber insertion losses of 17 dB. In this first monolithic implementation, the insertion losses are higher, which is attributed to the following reasons. First, monolithic integration requires the use of polycrystalline or amorphous rather than crystalline silicon in the photonic sections. Second, longer Mach-Zehnder configurations were chosen to guarantee sufficient modulation margin. The monolithic silicon-plasmonic modulators were measured to deliver 25 dB total insertion loss (fiber-to-fiber) at a wavelength of 1549 nm with a large extinction ratio exceeding 35 dB. Through cut-back measurements, the losses can be attributed to 5.5 dB per grating coupler, 1 dB per photonic-plasmonic converter and 12 dB plasmonic propagation loss in a 20 µm long and 75 nm wide plasmonic slot waveguide. The ultra-compact plasmonic MZM was showing fiber-to-fiber losses of 16.5 dB in test structures. These losses are assigned to 6.5 dB plasmonic propagation loss, 4.5 dB per grating coupler and y-splitter, and an extra 1 dB fiber array insertion loss. In the monolithic version, the total transmission was −27 dB (on-state equivalent). The additional losses come from a longer plasmonic modulator section (14 dB in a 24 µm long modulator) and slightly lower grating coupler and splitter efficiency (6 dB). With progress in technology, we anticipate total insertion losses to reach values below 10 dB for plasmonic modulators. Lower losses can be achieved e.g. by introducing a differential signal operation[42], which will allow to reduce the modulator length by a factor two, or by improving the nonlinear efficiency of the crosslinked OEO material[45]. Thus, the fundamental plasmonic losses can be reduced below 5 dB. Further, by transferring the plasmonic modulator technology to photonic fabrication sites, the fiber-to-chip coupling losses can be reduced to values below 2 dB alongside with a reduction in silicon waveguide propagation losses[53].

The electro-optic performance of plasmonic modulators using the OEO material 2:1 HLD1:HLD2 was measured on a reference plasmonic phase modulator. For this purpose, the OEO material was stabilized for high-temperature environments using a crosslinking procedure, aged for 28 days and measured at 100°C. At 60 GHz, a voltage-length product of $V_\pi L$ = 240 Vµm was extracted for a phase modulator. For the monolithic Mach-Zehnder modulators demonstrated in this work, it can be halved to 120 Vµm and corresponds to a V_π voltage of 6 V. From the voltage-length product, a nonlinear electro-optic coefficient r_{33} = 100 pm/V is estimated.

8.7 Externally Driven Monolithic Modulator

On the monolithic transmitter chip, separate modulators for external drive have been integrated as a reference for the characterization of the monolithic modulators, which are internally driven by the MUX. These modulators have not been connected to the underlying BiCMOS circuit, but equipped with contact pads to be externally driven via an RF probe. The passive characteristics were almost identical to the aforementioned integrated devices. Total insertion losses (IL) of 25 dB and an extinction ratio of 30 dB were measured. For the data modulation experiment, see Extended Data Fig. 5, the on-chip electronics has been turned off to measure the modulator performance at ideal room temperature. A 100 GBd electrical signal is generated using random bit sequence generator and an external DAC (MICRAM DAC4). The signal is then amplified and applied to the modulator via an RF probe. A tuneable external cavity laser source (9 dBm maximum output power, 100 kHz linewidth) generates the optical carrier at 1550.6 nm. The power of the laser can be adapted to power levels between 3 and 16 dBm by means of an amplifier. A subsequent band-pass filter (0.6 nm, IL ≤ 0.7 dB) suppresses the amplifier noise. This way, the modulator's performance can be tested for a large dynamic range of input powers. The plasmonic modulator converts the electrical signal onto the optical carrier before the data is transmitted over a back-to-back optical fiber link. At the receiver, the modulated signal is amplified to 10 dBm, band-pass filtered (2 nm, IL ≤ 0.7 dB) and received in a direct detection scheme (70 GHz photodiode with 0.6 A/W responsivity, 63 GHz real-time oscilloscope with 160 GS/s). In-house offline DSP is applied for signal recovery and equalization. 100 Gb/s NRZ were transmitted with a BER below 10^{-5} and an SNR of 16.44 dB.



Extended Data Fig. 5: Data modulation experiment for externally driven monolithic plasmonic modulator. An amplified external source applies the electrical signal to the modulator. 100 GBd NRZ-OOK has been modulated and transmitted to the receiver for direct detection. The insets show the received optical eye after equalization.

8.8 Monolithic Transmitter Data Modulation Experiment

In this section, more details on the monolithic transmitter data experiment is given.

The monolithic transmitter has been tested in a data modulation experiment. To evaluate the BER, five million samples of the modulated signal are captured using 63 GHz real-time oscilloscope with 160 GS/s. Offline DSP has been used for signal recovery and equalization. For the latter, a linear equalization with 101 filter taps and nonlinear mapping with pattern length of 7 have been applied as required for high-speed data modulation and compensation of nonlinearities in the complete communication system. Note that the first few filter taps show the most significant improvement[42].

For the silicon-plasmonic MZM, data experiments with 50, 100 and 120 GBd were performed at a wavelength of 1551.7 nm with chip input powers of 8, 11 and 11 dBm, respectively. This corresponds to power ranges of 1.5 to 4.5 dBm into the modulator on the chip, -10.5 to -7.5 dBm at the modulator output and -17 to -14 dBm in the optical fiber at the output. 50 GBd were modulated with a BER of $1.93 \cdot 10^{-5}$ (SNR of 13.14 dB) below the KP4 FEC limit of $2 \cdot 10^{-4}$ [54]. 100 and 120 GBd were modulated with a BER of $9.21 \cdot 10^{-3}$ (SNR of 8.14 dB) and $1.74 \cdot 10^{-2}$ (SNR of 7.20 dB), respectively. Both BERs are below the SD-FEC limit of $4 \cdot 10^{-2}$ [52].

For the ultra-compact plasmonic modulator, 50 and 100 GBd data modulation was tested using an optical carrier at a wavelength of 1559 nm with 5 and 9 dBm chip input power. The corresponding powers are -1.5 and 2.5 dBm at the modulator input, -15.5 and -11.5 dBm at the modulator output, and -22 and -18 dBm in the fiber at the output. 50 GBd were modulated with a BER of $1.36 \cdot 10^{-3}$ (SNR of 10.14 dB) below the hard-decision FEC limit of $3.8 \cdot 10^{-3}$ [55] and 100 GBd with a BER of $3.95 \cdot 10^{-2}$ (SNR of 5.48 dB) below the SD-FEC limit.

Data Availability Statement

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

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Author Contributions

U.K., C.H. and J.L. designed the plasmonic platform. C.U., H.H. and M.M. designed the BiCMOS electronic platform. U.K., C.U., H.H. and Y.F. developed the monolithic integration process. C.H., W.H. and M.A. contributed to the design and testing of the monolithic modulator. W.H., B.B., B.I.B. and A.J. contributed to the data modulation experiment. H.X., D.L.E. and L.R.D developed the temperature-stable organic material. E.M. and B.P. contributed to the design process. L.Z., S.L. and A.K. coordinated the wafer fabrication process. D.T., N.K. M.M. and J.L. designed and coordinated the project. All authors contributed to drafting of the manuscript.

Competing Interest

C.H., W.H., B.B. are involved in activities toward commercializing high-speed plasmonic modulators at Polariton Technologies Ltd. The other authors declare no competing interests.