SiC Versus Si-Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors

SiC vs. Si – Evaluation of Potentials for Performance Improvement of Inverter and DC-DC Converter Systems by SiC Power Semiconductors

J. Biela, M. Schweizer, S. Waffler, and J.W. Kolar

***Abstract*—Switching devices based on wide band gap materials as SiC offer a significant performance improvement on the switch level (specific on-resistance, etc.) compared to Si devices. A well known example are SiC diodes employed for example in inverter drives with high switching frequencies. In this paper, the impact on the system level performance, i.e. efficiency, power density, etc., of industrial inverter drives and of DC-DC converter resulting with the new SiC devices is evaluated based on analytical optimisation procedures and prototype systems. There, normally-on JFETs by SiCED and normally-off JFETs by SemiSouth are considered.**

I. Introduction

The continuous development of improved power semiconductors is a key enabling factor for propelling the constantly increasing demand for higher power density (P/V) and higher efficiency (η) in many power electronic applications. Recently, the technological progress in manufacturing power devices based on wide band gap materials as for example silicon carbide (SiC) or gallium nitride (GaN), resulted in a significant improvement of the operating voltage range for unipolar devices and of the switching speed and/or specific on resistance compared to silicon power devices. In [1] the current status of SiC switching devices with respect to specific on-resistance, maximal blocking voltage, specific capacitance, etc. is summarised. In Table I some basic information about the SiC devices is given.

With these new devices, a question arises as to what increase in system level performance may be achieved by the improvements obtained at device level. Such performance indicators include the power density and efficiency of the power electronic converter. In [1] this influence has been investigated for single phase PFC systems. Moreover, the demand on the system level has been transferred to a desired profile for the semiconductors, which is compared with the performance offered by the new SiC devices.

In the area of low voltage motor drives numerous papers about the comparison of Si IGBT and SiC switching devices – mainly SiC JFETs - have been published. There, usually the Si devices in matrix converters [2], [3] or standard inverters [4], [5] are replaced by SiC devices and the change in the system performance is evaluated. Depending on the operating point and the switching frequency [3], the SiC devices facilitate a significant performance improvement – especially regarding the switching loss. This is due to the lack of diode reverse recovery and IGBT tail current which are observed with Si devices. The conduction loss of the SiC devices depend on the chip area, since the applied devices are all unipolar ones. Consequently, the efficiency comparison is also dependent on the considered chip areas.

The lower switching loss of the SiC devices and the related freedom of being able to increase the switching frequency does not influence the achievable power density of standard VSI except for the cooling system, which could be reduced, when the losses are lower. However, the higher possible switching frequencies at low switching loss are advantageous for DC-DC converter systems, since they allow to reduce the size of the inductor and/or transformer [6]. This is especially true at medium voltage levels [7], [8], where fast switching devices based on silicon are non-existent and where new and ultra efficient converter systems are required for future energy distribution networks [9].

As in literature usually only a pure replacement of the

TABLE I: Current status of relatively mature SiC switches. Since the allowed drain current I_D depends significantly on the cooling conditions, the values should just give a hint on the capabilities of the respective switch for operation at higher junction temperatures (125°C or higher). The (specific) on-resistance is given for 25°C. The Si IGBT and the Si diode are part of the FP15R12W1T4 module by Infineon.

	$V_{(\mathrm{BR})\mathrm{DSS}}$	I_D	$R_{\mathrm{DS(on)}}$	A_{Chip}
JFET (SiCED)	500V	∼5A	0.2Ω	5.76mm^2
JFET (SiCED)	1.2kV	∼5A	0.33Ω	5.76mm^2
JFET (SiCED)	1.2kV	∼17A	0.12Ω	17.3mm^2
JFET (SiCED)	6.5kV	∼5A	3.3Ω	5.76mm^2
JFET (SemiSouth)	1.2kV	>15A	0.125Ω	4mm^2
MOSFET (Cree)	1.2kV	>20A	0.075Ω	16.6mm^2
MOSFET (Cree)	10kV	∼10A	0.5Ω	65.8mm^2
	Si Reference Devices			
IPP60R099CP	650V	31A	0.09Ω	28mm^2
STY112N65M5	650V	59A	0.019Ω	≈71mm^2
	$V_{(\mathrm{BR})\mathrm{DSS}}$	I_N	V_F	
Si IGBT +	1.2kV	15A	0.8V	17.5mm^2
Si Diode	1.2kV	15A	0.9V	10.7mm^2
Si IGBT +	1.2kV	15A	0.8V	17.5mm^2
C2D10120 (SiC)	1.2kV	22A	0.8V	9.8mm^2

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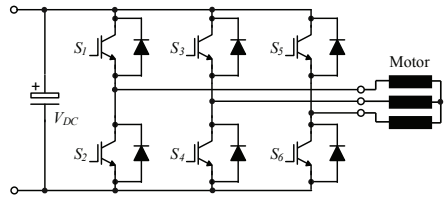


Fig. 1: Schematic of a 2-level inverter for low voltage standard motor drives.

switching devices by SiC ones and no optimization/adaption of the operating points to the new devices has been presented, in section II first the influence of the SiC devices on industrial inverter drives is investigated. There, also the link between the demands on the system level and the resulting required profile of the switching elements is discussed. Thereafter, DC-DC converter systems are considered in section III, where also medium voltage DC-DC converters for future energy distribution systems are included. There, the new switching devices based on wide band gap materials offer a tremendous performance improvement compared to state-of-the-art Si technology. In all the considerations, a limitation of the junction temperature below 175°C and the data of the SiC switches presented in Table I is assumed. Furthermore, the comparison is always based on the chip area and not on the current rating of the devices provided in the data sheets of the manufactures, as the chip area is proportional to the costs and the current ratings are very much dependent on the application, the switching frequency and the cooling conditions.

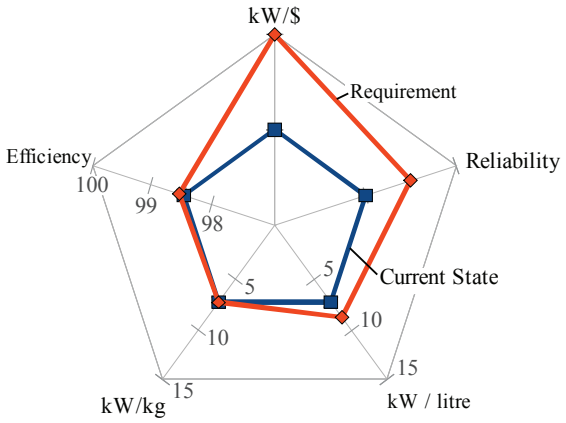
II. Inverter

Low voltage (<1000V) industrial drives are an important power semiconductor application area. There, mainly two-level inverters operating at switching frequencies in the range of 4kHz to 16kHz and at a DC link voltage in the range of 600V are used (cf. Fig. 1). In niche applications, also matrix converters offering bidirectional power flow and three-level converters for higher operating frequencies can be found.

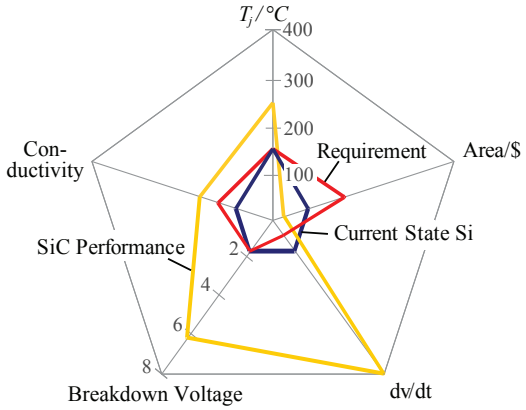
Due to the high winding inductance of the motors, there is generally no need for higher operating frequencies as shown in Fig. 2a) except for special high speed applications, where the fundamental is significantly higher than 50Hz and the inductance values usually decrease. Also there is no special need for higher kW/kg and/or extreme power densities in most applications. Only in integrated motor drives a higher power density would be desirable, but in this application with an improved cooling system the requirements often can be met. Since the efficiency of the standard inverters is already quite high and substantially exceeds the efficiency of the motor, there is (generally speaking) no further requirement for increased efficiency in comparison to Silicon based converters.

A major driving force are the costs, where a significant reduction could result in a more wide spread application of inverter drives. In some areas also a higher reliability is also required, which, however, is difficult to meet with high temperature operation/devices.

The system requirements are translated to the switch level in Fig. 2b), where the current status for silicon devices is shown



(a) System level requirements



(b) Component level requirements and performance.

Fig. 2: a) Radar chart of the system requirements for low voltage industrial drives, where in blue (=100%) the current status and in red the desired values are shown. Based on the system requirements, the radar chart in b) for the switching devices is derived, where the current status with silicon devices (=100%) is shown in blue, the requirements on the switch level in yellow and the offered performance of SiC devices in red. The numbers are based on the prototype system presented in [10].

as reference level (=100%) in blue, the resulting requirements in yellow, and the performance achievable with SiC devices in red. There it could be seen that the achievable switching speed of SiC and even of Si devices is not required. Often even the Si IGBTs are slowed down in order not to damage the motor winding isolation/bearings with high dv/dt values and to reduce EMI. Also the high breakdown voltages and the high possible junction temperature of SiC does not is not required in low voltage drives. Only the better conductivity of SiC, resulting in a smaller chip area, and the higher achievable efficiency could be beneficial for inverter systems, in case the costs do not increase. There the high costs for SiC devices are a significant limit at the moment.

After the more general remarks, the effect of SiC devices on a real prototype system with the specification given in Table II are discussed. There, the following scenarios are considered:

- How much chip area is required for achieving an efficiency of 98.3%?
- How much chip area is required for keeping the power density constant at 25kW/dm^3 (considering just the cool-

TABLE II: Specifications of the inverter system.

Nominal Power	7.5kW
DC Link Voltage	700V
Switching Frequency	4kHz
Current Phase Displacement	30°
Modulation Index	0.9
Output Voltage	364V$_p$
Output Current	15.9A$_p$
CSPI	15W/(K dm^3)
Ambient Temperature	25°C
Junction Temperature	175°C
Thermal Resistance R_{j-HS}	30K/(W mm^2)

ing system)?

- How much chip area is required for an ultra efficient drive with an efficiency of 99.3%, i.e. 1% more than the prototype system?

and besides the silicon IGBTs with Si-/SiC-diodes also the 1.2kV JFETs and MOSFETs as listed in Table I are considered.

In Fig. 3 the results for the mentioned scenarios are presented. The results are based on some simplifying assumptions. First it has to be noticed, that only pure silicon performance has been analysed, so additional losses of fans or digital control electronics will not be considered. The conduction loss are modelled with the typical simplified device behaviour namely

$$P_{Cond,IGBT}(I) = V_{f,T} \cdot I + R_{on,T} \cdot I^2 \quad (1)$$

$$P_{Cond,Diode}(I) = V_{f,D} \cdot I + R_{on,D} \cdot I^2 \quad (2)$$

$$P_{Cond,JFET}(I) = R_{DS(on),J} \cdot I^2 \quad (3)$$

$$P_{Cond,MOSFET}(I) = R_{DS(on),M} \cdot I^2. \quad (4)$$

The parameters are dependent on the junction temperature. For the bidirectional devices JFET and MOSFET the loss characteristic in forward and reverse current direction are assumed to be the same. With the low switching frequency of 4 kHz, the switching losses of JFET and MOSFET are much lower than its conduction losses and will be neglected. The switching losses of IGBT and Diode are modelled with the switching energies linearly scaled [11].

$$E_{On,T}(V,I) = E_{OnT,nom} \cdot \frac{V}{V_{nom}} \cdot \frac{I}{I_{nom}} \quad (5)$$

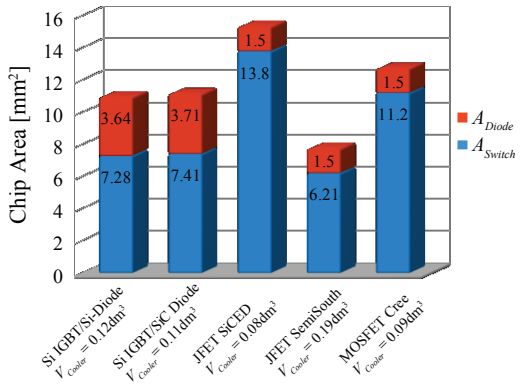
$$E_{Off,T}(V,I) = E_{OffT,nom} \cdot \frac{V}{V_{nom}} \cdot \frac{I}{I_{nom}} \quad (6)$$

$$E_{On,D}(V,I) = 0 \quad (7)$$

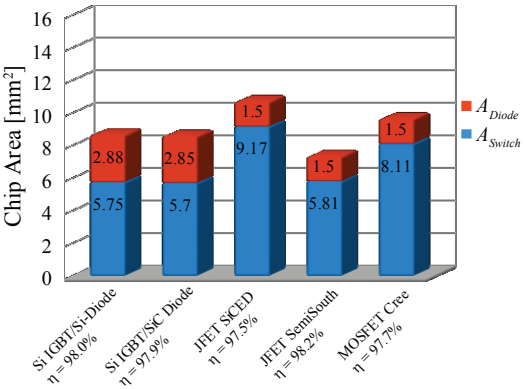
$$E_{Off,D}(V,I) = E_{OffD,nom} \cdot \frac{V}{V_{nom}} \cdot \frac{I}{I_{nom}} \quad (8)$$

The nominal values are taken from datasheet values of a newest generation IGBT from Infineon (1.2 kV, 15 A) with parameters as listed in Table I. For the implementation variant with SiC antiparallel diodes, the diode turn off energy is assumed to be zero and the IGBT turn on energy is assumed to be 30% smaller due to the missing diode reverse recovery effect.

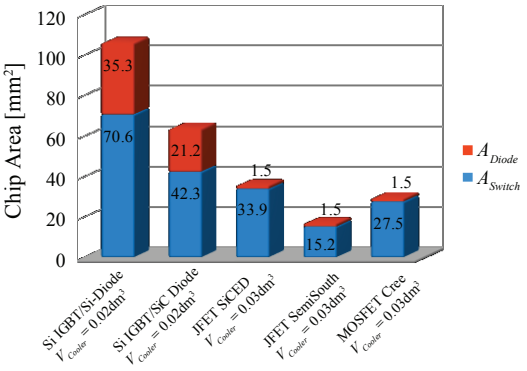
The device losses of the inverter system are calculated analytically for a symmetric space vector modulation strategy. The



(a) Chip area for an efficiency of 98.3%



(b) Chip area for fixed volume of 0.3dm^3.



(c) Chip area for an efficiency 98.3% + 1%.

Fig. 3: Chip area of 1.2kV SiCED JFET, the 1.2kV SemiSouth JFET, the 1.2kV Cree MOSFET and for a Si-IGBT with Si- and with SiC diode for three different cases: a) all systems have an efficiency of 98.3%, b) all systems have a volume of 0.3dm^3 and c) chip area required for an efficiency increase of 1%, i.e. for 99.3%.

well-known results for the average conduction and switching losses will not be repeated here but could be found in [11], [12]. In a further step the on-resistances of all devices are made area dependant (cf. [13]) with the generic formula:

$$R_{On} = R_{On,nom} \cdot \frac{A_{Chip,nom}}{A_{Chip}} \quad (9)$$

For the dependance of the switching energies on the die size no general trend could be observed. They are assumed to stay

constant for the considered chip area range.

In a same way the thermal resistance $R_{th,J-S}$ for each device is made area dependent. The nominal value of the resistance of 30 K/(W·mm^2) was fitted with a data sheet study in [13] and is used for all dies independent of technology

$$R_{th,J-S} = \frac{R_{th,J-S,Anom}}{A_{Chip}}. \tag{10}$$

Finally a forced air cooling system with a Cooling System Performance Index (CSPI) of 15W/(K dm^3) is assumed. This allows for complete inclusion of the thermal model into the optimisation process.

$$R_{th,S-A} = \frac{1}{CSPI \cdot Vol_{HS}} \tag{11}$$

The heat sink temperature can be calculated with the total losses of the inverter system

$$T_{HS} = T_{Amb} + P_{Total} \cdot R_{th,S-A} \tag{12}$$

The junction temperature of each chip die is given by

$$T_{J,Die} = T_{HS} + P_{AVG,Die} \cdot R_{th,J-S} \tag{13}$$

Now, the set of equations can be solved for the different scenarios defined above. For each scenario the junction temperature is assumed to be 175°C. This implies that the fundamental output frequency is high so that the average device losses can be used and no time behaviour of the thermal model has to be considered.

For a fixed efficiency, the formulas directly lead to the chip areas and size of the necessary heat sink. For the IGBT with antiparallel diodes the chip size of the diode is assumed to be half of the IGBT chip size in order to reduce a degree of freedom.

Due to the reverse recovery losses of the internal diodes of the SiC JFETs and the SiC MOSFETs, antiparallel Schottky diodes are assumed, which only conduct shortly during the interlocking delay. In the rest of the time the current is flowing in reverse direction through the channel of the unipolar device. Consequently, the area of the SiC diodes could be relatively small and is assumed to be 50% of the SiC diode area of the IGBT+SiC diode combination.

It is interesting to note that for a constant ambient temperature (e.g. 25°C) the equations define a minimum efficiency for which a cooling solution exists. If the efficiency is chosen to be lower than this minimum, the resulting chip dies are so small that the temperature drop from junction to sink gets higher than the maximal 150°C and the heat sink size grows to infinity.

For a fixed heat sink size the formulas directly lead to the necessary chip sizes and the resulting inverter efficiency. Finally, the increase in area for a high performance 99.3% inverter efficiency (pure silicon) is calculated. It can be noted that the chip area of IGBT and diode has to be increased to unrealistic values showing the advantages of SiC JFETs and MOSFETs for ultra high efficiency motor drives.

The higher efficiency achievable with SiC devices is for example very interesting for renewable energy conversion (photovoltaic inverter) where a special focus is put on efficiency. There, the higher costs for the SiC devices could be compensated by saved energy. In general, however, it is not important if the losses are saved at the generator or at consumer side, – except for the losses due to energy transmission/distribution.

In automotive industry besides the efficiency, also the higher possible operation temperature is advantageous due to high ambient temperatures if the power electronic converter is mounted close to a combustion engine. There, the remaining components as e.g. capacitors, control electronics or gate drives are the limiting factors besides reliability issues. Furthermore, with a water cooler also the smaller footprint of the SiC devices could be advantageous with respect to costs.

The higher possible junction temperatures also could improve the robustness of the converter systems in case of overload situations. Replacing Si bipolar devices with fast SiC unipolar switches also requires to consider the parasitics in the layout and the mechanical design more carefully, due to the fast switching transients.

III. DC-DC Converter

The second application area considered in this paper are DC-DC converter, which are split in low voltage converter – non-isolated and isolated – and in high voltage isolated DC-DC converter, which will be discussed below. But before, the general requirements for low voltage DC-DC converter in telecom and in automotive applications are evaluated based on the net diagrams given in Fig. 4.

The most important issue on the system level is cost, since in both areas there is quite a high cost pressure and a very competitive market. In the automotive area also the weight of the converter and the power density are an important criteria, since the first directly influences the fuel efficiency and the second results from the limited available space. The latter is also true for telecom systems, as the costs for floor space are high. Also for both application areas the efficiency has become more and more important in the last years due to rising energy costs and environmental concerns, which is especially true for renewable energies and energy storage [14]. Especially, in the automotive area with its harsh environmental conditions (e.g. vibrations, temperature) the reliability should be very high, which is difficult, especially if one thinks of high temperature operation. The reliability is also an important issue in telecom supplies as a shut down of a data centre is very expensive.

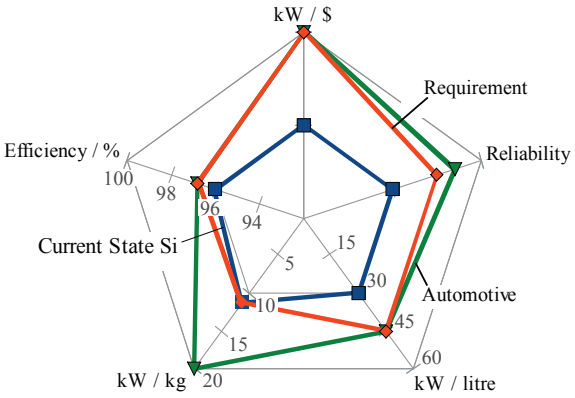
These system level criteria result in the requirements for the switches as shown in Fig. 4b), where the current status is shown as reference value (=100%) and where also the achievable performance of SiC devices and the demands on switches in the automotive and the telecom area are given. There, mainly the higher conductivity per area of SiC devices and the higher junction temperature for automotive applications meet the demands. The higher blocking voltage capability and the improved switching performance are not required, since the operating voltages are usually limited to a few hundred volts and soft switching could be achieved with very small additional effort. As with the other applications,

the higher costs of SiC devices are a major drawback and this significantly limits the area of the SiC devices which could be used at the same cost level, what influences the achievable system performance – especially the efficiency. The two low voltage systems considered now, support this statement.

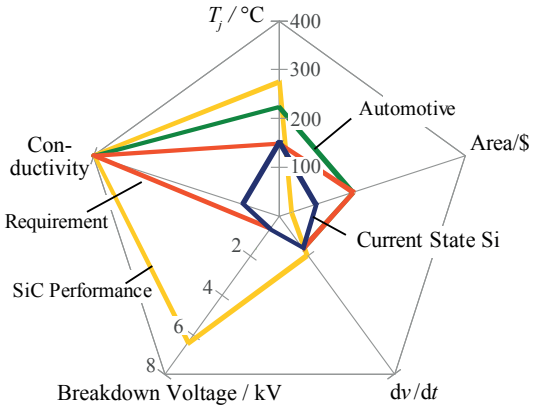
A. Low Voltage Converter

1) Non-Isolated, Automotive DC-DC Converter: First, a DC-DC converter without galvanic isolation is considered. A typical application area of such a converter are Hybrid Electrical Vehicles (HEV) or Fuel Cell Vehicles (FCV), where the converter is used for power management between the batteries, Super Capacitors and/or fuel cells [15], [16]. In these systems, often a bidirectional power flow for providing energy during acceleration and storing energy during braking is required.

A converter for this application has to meet the prevalent automotive requirements, such as being a low cost design, and minimising the component size and count. This can be achieved by increased switching frequency and interleaved operation of multiple converter phases. Fixed frequency operation is desired due to EMI restrictions and a highly compact design and a low overall weight are required.



(a) System level requirements



(b) Component level requirements and performance.

Fig. 4: Radar charts of the system and component level requirements for non isolated DC-DC converter are shown. There, the numbers show typical values for the system depicted in Fig. 7.

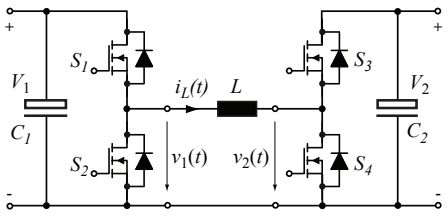


Fig. 5: Bidirectional buck-boost converter with the specifications given in Table III for automotive applications.

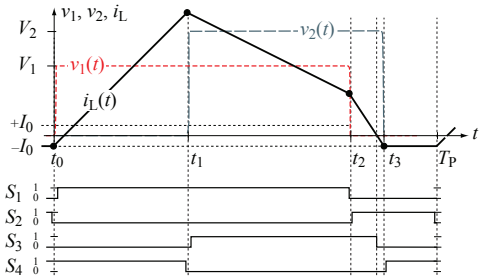


Fig. 6: Waveforms of the primary and secondary voltage and the inductor current.

In Fig. 5 a schematic of the considered bidirectional DC-DC converter consisting of 4 switches, an inductor and two capacitors is shown. The specifications of the converter are listed in Table III and the most important waveforms of the converter are given in Fig. 6. There, the primary v_1 and the secondary voltage v_2 as well as the inductor current i_L and the gate signals S_ν are given and it could be seen, that in contrast to a normal buck boost converter a negative current flows in the inductor between t_3 and T_P. With this special modulation method a soft switching of the converter could simply be achieved by control and the efficiency could be increased. Further details about the control method are given in [17] and in [18] a similar structure is presented, where the chip area is reduced by using snubbers, which, however, increase the circuit complexity and costs for the passive components.

A picture of the Si reference prototype system is given in Fig. 7. This has been used to validate the analytical converter models presented in [19], which are used in the following to compare the achievable performance of Si and SiC devices. The reference system is based on IXYS IXFB82N60P devices, where for switch S_1/S_3 four MOSFETs and for switch S_2/S_4 three MOSFETs are used in parallel in order to achieve the required efficiency of $\geq$95% in the complete input and output voltage range. For S_1/S_3 more MOSFETs are used since the RMS currents for these switches are higher and thus also the converter efficiency benefits from an unbalanced distribution of the chip area. The prototype system utilises a water cooler and can operate with a coolant temperature of up to 80°C. Furthermore, six 12kW units are interleaved for reducing the ripple current at the input/output.

For comparing the performance of the Si devices with SiC ones, it is assumed that the IXFB82N60P are replaced by the more recent STY112N65M5 from ST, which have a much lower specific on resistance.

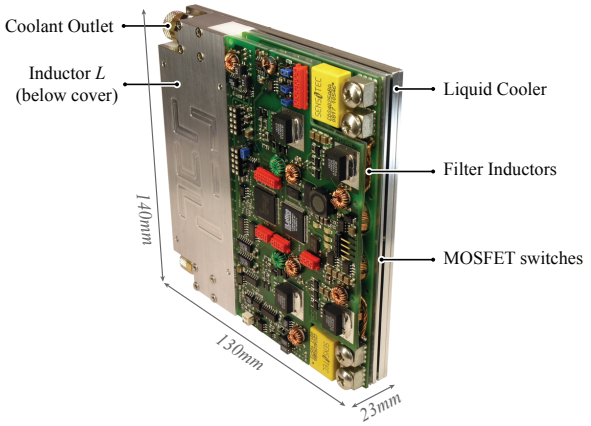


Fig. 7: Photo of the bidirectional buck boost converter with 150V...450V input and output voltage, 12kW nominal power and a switching frequency of 100kHz.

TABLE III: Specifications of the automotive DC-DC converter shown in Fig. 7.

Parameter	**Value**
Voltage Range V_1	150V...450V
Voltage Range V_2	150V...450V
Output Power	-12kW...12kW
Switching Frequency	100kHz
Maximum Current I_{max}=I_1=I_2	40A
Required Efficiency η_{req}	$\geq$95% for P>0.1P_{max}
Ripple Amplitude $\hat{\tilde{v}}_1$	1V
Ripple Amplitude $\hat{\tilde{v}}_2$	1V

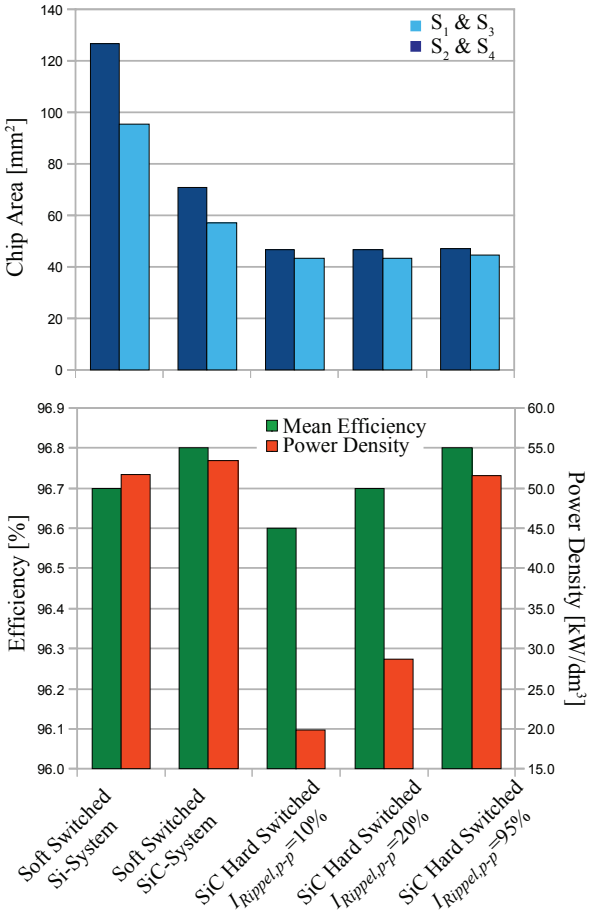


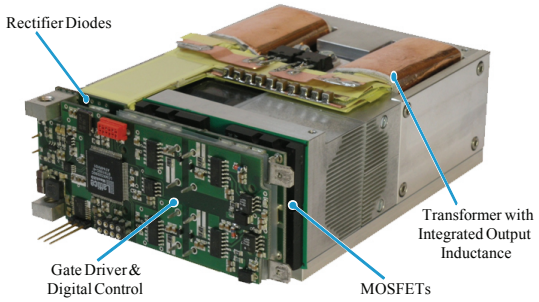
Fig. 8: Calculation results for a non isolated DC-DC converter with Si MOSFET and/or SiC JFET scaled on the basis of the 500V JFET by SiCED. For the SiC devices soft switching conditions as well as hard switching are considered. In case of the hard switching different limits for the peak-to-peak ripple current in the inductor are assumed. In all considered systems the minimal efficiency in the whole operating range is higher than 95%, the mean efficiency usually is significantly higher. In the upper half the required chip areas for the 4 switches and in the lower graph the efficiency and the theoretical power density are given.

In the upper half of Fig. 8 the resulting chip area for the 4 switches and in the lower half the mean efficiency as well as the power density for the different considered soft and hard switching systems are given. In the efficiency the conduction loss of the switches, the core and HF winding losses of the inductor and the power required for the control are considered. The power for the water pump is neglected. Also the volume for the water pump is not considered in the power density. Instead, it is assumed that 25% volume must be added to account for the interconnections, isolation, geometrically not matching housings, etc. The depicted prototype shows a reduced power density in comparison to the results provided in this paper, mainly because of the larger volume required by the IXYS IXFB82N60P MOSFETs and the inductor made of planar cores. The analytical calculations assume an optimised inductor built with E-cores that results in a reduced volume. Additionally, the prototype is equipped with measurement circuitry, such as current sensors, that only would be required once in a multi-phase converter design.

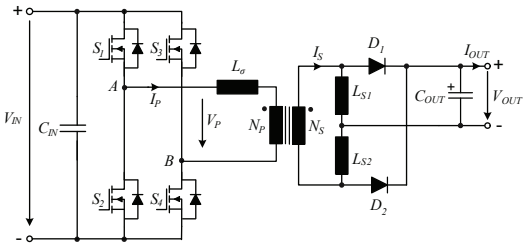
By utilising 500V SiCED JFETs and adapting the chip area, so that also the SiC system has a minimal efficiency of 95% in the whole operating range, the performance listed in the 2nd column of Fig. 8 is achieved. Due to the lower specific on resistance and the resulting limitation of the minimal chip area by thermal constraints, the mean efficiency of the SiC system is slightly higher. Also the power density increases slightly, due to the reduced volume required for the semiconductors.

In the 3^{rd},4^{th} and 5^{th} column the results for operation under hard switching conditions with 500V SiCED JFETs are shown. There, different limits for the peak-to-peak ripple currents have been assumed, which results in a smaller inductance value, if the ripple is larger. This also increases the power density of the system. In case of a 95% ripple, i.e. almost discontinuous operation, the power density becomes maximal. There, the value and the volume of the boost inductor is larger as in case of the soft switched systems, but the volume reduction due to much smaller required chip area (i.e. also smaller cooling system) outweighs this. The relatively low dependency of the chip area on the ripple current in case of the hard switched system results since the RMS current does not depend so much on the current ripple but on the DC component of the current. Furthermore, the efficiency is slightly higher than the desired 95% since the chip area is limited by thermal constraints, so that the R_{DSon} is smaller than necessary.

In case of soft switching conditions, with SiC the chip area could be reduced to approximately 60% of the Si chip area.



(a) 5 kW prototype of the proposed 400V/48..54V DC-DC converter: Height: 1U, volume: 0.56dm^3, power density: 147W/in^3 (9kW/dm^3).



(b) Circuit schematic of the phase-shift full bridge converter with current doubler rectifier.

Fig. 9: Phase-shift DC-DC converter with current doubler output.

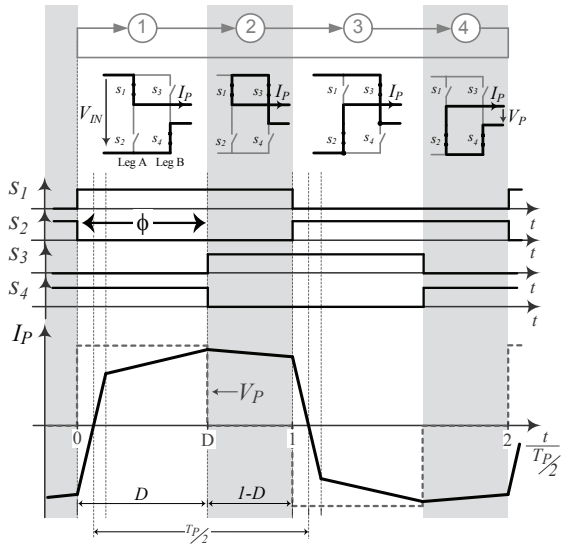


Fig. 10: Waveforms of the primary current and voltage of the current doubler rectifier at nominal power operating with phase shift modulation.

In the calculations performed for evaluation the performance of the different devices, for the inductor an E-core with air gap made of N87 material, a maximal flux density of B_{max}=0.3T, a maximal temperature of T_L=100°C has been assumed. For the winding litz wire is used and the current density is limited to 5A/mm^2. Further details on the inductor optimisation can be found in [19].

2) Isolated DC-DC Converter: A large market for isolated DC-DC converter in the kW range are telecom power supplies, where often full-bridge converter with soft switching or some kind of resonant converter are applied. These converter types meet the demands for high power density and for high efficiency – an issue which became more and more important due to rising energy costs. But first of all initial costs are very important, which results in a relatively simple and robust design.

In Fig. 9 the circuit schematic and a photo of a full bridge converter with current doubler, which fulfills these requirements, is shown and in Table IV the specifications of the converter are given. The design of the converter is based on an optimisation algorithm, which also includes the thermal and the electromagnetic design of the converter besides the electrical model. Further details on the design and the optimisation procedure can be found in [20] and on the thermal design in [21]. The converter has been built for validating the models and is based on 500V MOSFETs APT50M72B2 from Microsemi.

In Fig. 10 the basic waveforms for the primary current and the primary voltage are given. Due to the leakage inductance L_σ of the transformer and the phase shift modulation, all four switches operate under ZVS condition resulting in negligible switching loss at a very low effort on circuit and control side. Consequently, only the conduction loss and therewith the on-resistance of the switches is interesting. For achieving ZVS conditions and zero switching loss the switches require a minimum output capacitance, which depends on the switching speed. With a smaller capacitance value the switching loss increase, but can help to increase part load efficiency.

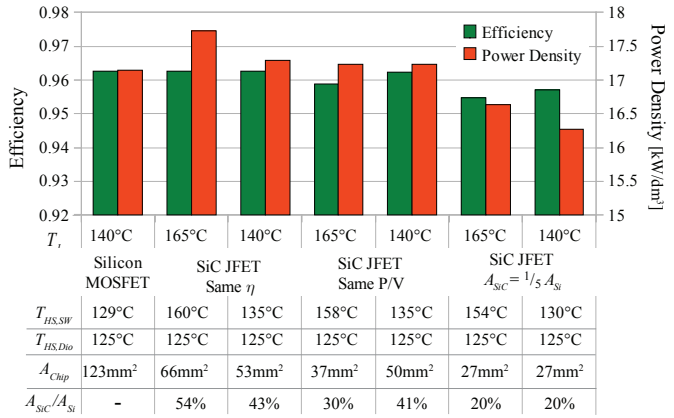
In spite of the negligible switching losses, the optimal switching frequency of the converter, which results in maximal power density, is just 200kHz. Increasing the frequency results in a smaller power density and efficiency as explained in [22]. There, it is also shown, that for achieving a maximal efficiency of the considered converter systems, the switching frequency must be lower than the mentioned 200kHz.

Based on the optimisation procedure, the full-bridge converter has been optimised with the data of the 650V MOSFET STY112N65M5 from ST on the silicon side and of the 500V normally on JFET from SiCED on the SiC side. There, the following assumptions have been made:

- Core material: N87 from EPCOS ($T_{Max} \leq 115\,°C$)
- Windings: Foil windings ($T_{Max} \leq 125\,°C$)
- Center tapped secondary winding
- Rectifier diode: APT100S20 from Microsemi
- Cooling system performance index: 23 (for transformer and semiconductor heat sink)
- Max. junction temp. $T_{j,max} \leq 140\,°C$ for Si MOSFET
- Max. junction temp. $T_{j,max} \leq 140/165\,°C$ for SiC JFET

TABLE IV: Specifications for the proposed IT DC-DC converter.

Input Voltage	400 V
Output Voltage	48. . . 54 V
Output Power	5 kW
Output Ripple Voltage	300 mV$_{pp}$
Max. Ambient Temperature	45 °C
Max. Height	1 U (≈ 44 mm)
Power Density	9kW/dm^3



T_j	140°C	165°C	140°C	165°C	140°C	165°C	140°C
	Silicon MOSFET	SiC JFET Same η		SiC JFET Same P/V		SiC JFET $A_{SiC}=1/5\,A_{Si}$	
$T_{HS,SW}$	129°C	160°C	135°C	158°C	135°C	154°C	130°C
$T_{HS,Dio}$	125°C	125°C	125°C	125°C	125°C	125°C	125°C
A_{Chip}	123mm²	66mm²	53mm²	37mm²	50mm²	27mm²	27mm²
A_{SiC}/A_{Si}	-	54%	43%	30%	41%	20%	20%

Fig. 11: Efficiency and power density for the isolated DC-DC converter with Si MOSFETs (STY112N65M5) and/or the 500V JFETs for the cases where the SiC chip area is scaled so that the converters have the same efficiency η or the same power density P/V and for the case where the chip area of the SiC devices is 1/5 (A_{SiC}=1/5A_{Si}). For the SiC devices a 140°C and a 165°C limit for the junction temperature and separate heat sinks for the Si rectifier diodes and the switches of the full-bridge have been assumed. Below the graph the temperature $T_{HS,SW}$ of the heat sink for the switch and $T_{HS,Dio}$ for the heat sink of the rectifier diodes is given. The switching losses, which are relatively low, are evaluated based on measurements with the Si MOSFET and are assumed to be in the same range for the SiC devices.

In Fig. 11 the results for the cases, where the chip area is adapted, so that the efficiency and/or the power density is the same for the Si and the SiC based converter and for the case, where the chip area of the SiC devices is fixed to a fifth of the Si MOSFET, are shown. In all cases, results for a junction temperature limit of the SiC JFET of 140°C and of 165°C are shown and it is assumed that the switches of the full-bridge are mounted on a different heat sink than the output rectifier diodes. With a junction temperature limit of 165°C the heat sink temperature reaches a peak temperature of 160°C, which requires a thermal isolation between the heat sink and the other components. In general, the heat sink temperature is relatively close to the junction temperature in an optimised design, since the thermal resistance between junction and heat sink is relatively small. Consequently, with a junction temperature limit of 165°C also the heat sink temperature is high.

The calculated peak power density of 17.7kW/dm^3 also has to be considered against the background of the high heat sink temperature, because a thermal isolation is not included in the power density calculation, so that in the real system the power density might be lower. Basically, it is important to note, that in the power density only the net component volume is included, i.e. the power density decreases to roughly 2/3 (for systems without thermal isolation) in the final system, due to air in between the components required for insulation and due to geometrically not matching housings of the components.

For achieving the same efficiency with SiC devices as with the Si MOSFET approximately 43% to 54% of the chip area is required for the SiC JFET. Due to the high heat sink temperature the size of the cooling system decreases and therefore the power density increases to 17.7kW/dm^3 for a junction temperature limit of 165°C.

The same power density could be achieved if the SiC devices have 30% to 40% of the Si MOSFET chip area. There, with a lower junction temperature approximately the same efficiency could be achieved with the SiC devices as the on-resistance increases with junction temperature.

B. High Voltage Converter

The benefit of SiC devices in low voltage applications is basically limited to some efficiency and/or power density increase – depending on the topology/application to a greater or lesser extent. However, with SiC devices no major new application area is enabled, except for environments with high ambient temperature. Moreover, the high costs of SiC devices and the new processing technology required for SiC often will constrict the application of the new devices in low voltage systems.

Considering medium voltage levels, where new applications for example in future energy distribution are emerging [23], [24], SiC devices could offer a functionality and performance, which is not achievable with Si devices. In [25] for example a 5kV to 700V isolated bidirectional DC-DC converter operating at 50kHz is presented, which shows outstanding efficiency and power density enabled by the performance of SiC devices. The converter is based on the dual active bridge topology, which has soft switching conditions, bidirectional power flow and a relatively simple control [26].

On the 5kV side, a cascode connection of normally-on 1.2kV JFETs and a low voltage (40V) Si MOSFET as shown in Fig. 12 (a Super Cascode) is used. With this configuration a blocking voltage of 6×1.2kV=7.2kV and very fast transients as presented in [27] can be achieved. The voltage balancing of the JFETs is inherently achieved with avalanche diodes and additional small RC networks, so that the whole Super Cascode could be controlled just via the gate of the Si-MOSFET and basically operates like a single switch.

The conduction losses in the DC-DC converter can simply be decreased by increasing the chip size of the JFETs and the MOSFET and efficiencies in the range of 99% are possible with the SiC JFETs. Due to the ZVS operation, the high operation frequency is possible resulting in a very compact and low weight design. This could be for example very advantageously used in wind generators, where the weight of the power electronic conversion system directly influences costs and size of the mechanical design of the tower/nacelle.

In future, the operating voltage level of the Super Cascode will increase further, for example by applying 6.5kV JFETs. In Fig. 13 measurement results of such JFETs operating in a half bridge connection are given. Based on these, a Super Cascode with operating voltages of more than 20kV will be possible, which will enable new converter concepts in this voltage range.

Besides the semiconductors, also other issues, as for example the transient voltage distribution in the magnetic components, the packaging and the low inductive/capacitive design meeting the requirements for high insulation voltages must be solved, before fast, ultra compact and efficient SiC based power electronic converter systems in the voltage range higher than 10kV will be available. However, with the functionality

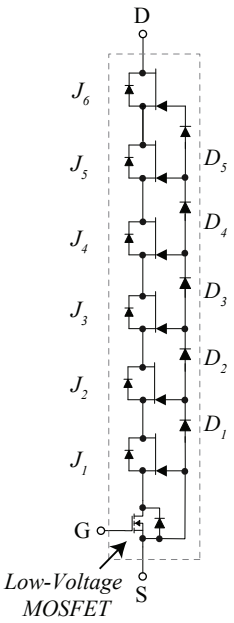


Fig. 12: Schematic of a Super Cascode consisting of 6 series connected SiC JFETs and a silicon low voltage MOSFET. At 5kV, 5A and 25°C the Super Cascode has approximately 3.3mJ turn on losses, which decrease almost linearly to 1.2mJ for 0A. Due to the phase shift operation the turn off losses are negligible [27].

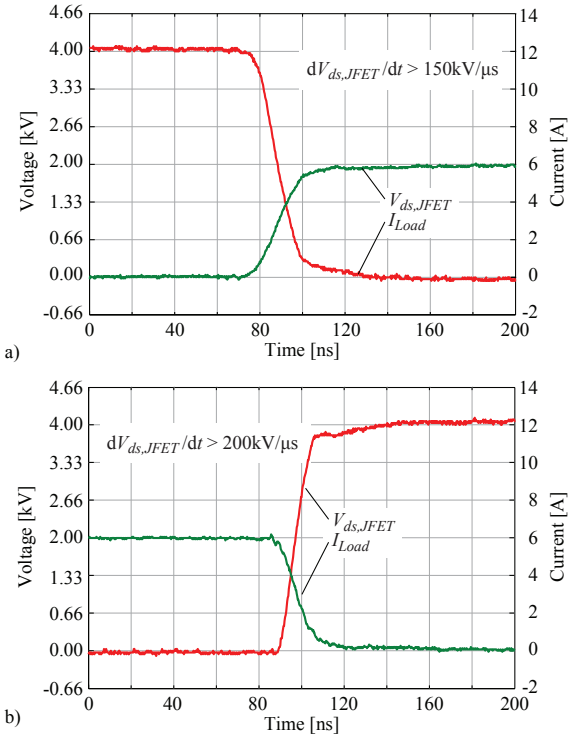


Fig. 13: a) Turn on and b) turn off switching transients of 6.5kV JFETs in cascode connection operating as half bridge with ohmic load. The switches show outstanding transient performance enabling new converter concepts in the medium voltage range.

of such systems the energy distribution and integration of fluctuating renewable energy sources will significantly change in the future.

IV. Conclusion

Considering low voltage inverter drives limited to a few kHz switching frequency, the SiC switching devices do not offer a performance boost compared to Si IGBTs, as a relatively high SiC chip area is required in order to achieve the same system performance as with Si. Just in ultra high efficient drive systems (>99%) with SiC devices a significantly smaller chip area is required as the unipolar devices allow a approximately linear conduction loss reduction by increasing the chip area. This high efficiency could be advantageously used in converter systems for renewable energy e.g. photovoltaic, where the high costs for SiC will pay back to the reduced losses and long operating time. In automotive industry the higher possible junction temperature could be advantageous due to increased ambient temperatures if the converter is mounted close to a combustion engine. Furthermore, with SiC chips a smaller footprint of the modules is possible.

In the area of low voltage DC-DC converter, where very often soft switching conditions can be achieved with very low effort, SiC devices mainly offer the possibility to reduce the chip area for a desired efficiency. This could help to increase the power density as has been shown using the example of a non isolated bidirectional buck-boost converter, where the chip area approximately could be reduced to 50% for achieving the same performance with SiC devices. Also for isolated DC-DC converter, for which a phase shift converter with current doubler rectifier has been evaluated in the paper, the main benefit is an improvement of power density and/or efficiency or the reduction of the chip area to approximately 35% at the same performance. There, however, the costs for the SiC devices play an important role, since these benefits often can be realised by significantly increasing the costs for the semiconductors. This might change in future if the price of SiC devices drops.

In future, the SiC devices could show a significant advantage compared to unipolar Si devices, if the output capacitance of the SiC switches could be reduced significantly as shown in [28] for GaN devices. This would reduce the switching losses in hard switched applications resulting in a better efficiency and/or a more compact design.

Considering higher power levels and voltages in the medium voltage level range, the picture changes substantially, since in this area SiC devices offer a function and a performance, which is not achievable with Si devices. In the paper a 5kV DC-DC converter operating at 50kHz with an efficiency of approximately 99% is discussed. Such converters will play a significant role in future (renewable) energy distribution and will allow a significant performance boost.

Also in applications as e.g. accelerators or pulsed-power converters for medical systems, where a high output voltage is required, high voltage SiC diodes offer a significant advantage, as these enable a reduction of the total voltage drop across the rectifier resulting in lower losses.

Especially in such a high voltage system, but also in the considered low voltage converters, passive components, isolation issues and converter design must not be neglected, since these often limit the system performance as much as the

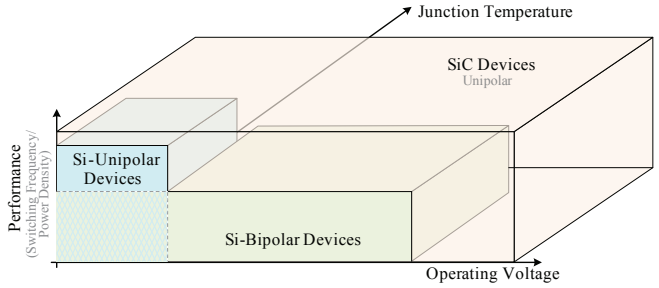


Fig. 14: Nowadays SiC devices offer only a small performance improvement with respect to efficiency/power density in the lower operating voltage range compared to current Si MOSFETs. With increasing operating voltages the performance improvement increases significantly, especially as there are only bipolar Si switching devices, which are relatively slow, available. The maximal possible operating temperature of SiC devices is significantly higher than the one of the Si devices.

switches do. A good example are motor drives, where the dv/dt often must be reduced even if applying nowadays IGBTs, in order not to harm the isolation of the windings or to limit capacitive charging currents.

The results for the different systems could be summarised as shown in Fig. 14, where a clear performance improvement with SiC devices is shown at higher operating voltage levels, where no unipolar Si devices are available. With current SiC devices, there is no significant performance improvement compared to unipolar Si devices and considering the costs, SiC devices have a clear disadvantage, as the reduction of chip area is relatively small compared to the cost ratio between Si and SiC. This is also confirmed by the results, which are presented in [1] for a single phase PFC converter, where some of the JFETs by SiCED show a lower performance than the Si switches and only the JFETs by SemiSouth show an slight improvement from 99.09% to 99.14% efficiency. Therefore, it is also important to bare in mind, that the SiC devices are relatively young and definitely will improve significantly in future.

Besides SiC also other wide band gap materials as for example gallium nitride (GaN) shows interesting material properties and theoretically enables a tremendous reduction of the specific on resistance, which has an even lower theoretical limit than SiC. The GaN devices have a lower gate charge and also the output capacitance is smaller [28], which reduces switching losses mainly in hard switched applications. Furthermore, the processing of the material is simpler and might allow a faster decrease of production costs than is possible with SiC [29], [30].

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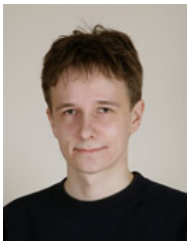

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Johann W. Kolar (M'89 SM'02) studied industrial electronics at the University of Technology Vienna, Austria, where he also received the Ph.D. degree (summa cum laude). From 1984 to 2001 he was with the University of Technology in Vienna, where he was teaching and working in research in close collaboration with the industry. He has proposed numerous novel converter topologies, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter concept. Dr. Kolar has published over 300 scientific papers in international journals and conference proceedings and has filed more than 75 patents. He was appointed Professor and Head of the Power Electronics Systems Laboratory at the Swiss Federal Institute of Technology (ETH) Zurich on Feb. 1, 2001. The focus of his current research is on ultra-compact intelligent AC-AC and DC-DC converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and active EMI filtering, multi-disciplinary simulation, bearing-less motors, power MEMS, and wireless power transmission.