10kV/30kA Unipolar Arbitrary Voltage Source for Hardware-in-the-Loop Simulation Systems for HVDC Circuit Breakers

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Keywords

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Abstract

In this paper a novel topology for an unipolar arbitrary voltage source for high power Hardware-in-the-Loop Simulation Systems is presented. The maximal output voltage is 10 kV and a maximal output current of 30 kA can be provided for a duration of 20 ms with a maximal current gradient of 200 A/μs. The system enables in-depth research and future developments of circuit breakers for future multi-point DC transmission systems.

1 Introduction

The change from centralised conventional electrical power generation to distributed and fluctuating renewable energy sources requires a change in power transmission and distribution system technology. Currently existing AC grids reach their limits when dealing with these new power sources, necessitating more high voltage DC transmission systems (HVDC) in the future. This could finally be enhanced to a HVDC super grid (see e.g. DESERTEC project, [1]).

In multi-point DC transmission systems, new circuit breaker concepts are required for isolating faulty grid parts in case of a failure. Thus far, switches for AC grids, which are enhanced to handle DC currents of up to 4 kA [2, 3, 4] are utilised for this task. However, research on DC grids has shown, that much higher failure currents (up to 30 kA) have to be expected, so that further investigations on new DC circuit breaker concepts are required [5].

For investigating / testing DC circuit breakers two different kinds of energy sources have been used up to now. During the tests a current pulse with a high peak amplitude is flowing through the circuit breakers simulating a short circuit. Simple test setups use a capacitor for energy storage and connect the capacitor through a switch to a serial combination of an inductance and a resistor to provide a smooth current, which is then interrupted by the analysed circuit breaker [6]. This is a very simple solution, which is easy to control, but the drawback is a limited influence on the current/voltage waveforms except by changing the circuit elements.

More advanced setups use power electronic converters to provide a high current at low voltage. This simulates the conduction time of the circuit breaker during a fault situation. The high voltage, which occurs while interrupting the current, is generated by a spark gap that is triggered to connect a pre-charged capacitor parallel to the circuit breaker [7, 8, 9]. This is called synthetic test setup and is a typical approach in high voltage engineering because no high power supply is needed. However, based on this setup the current and voltage cannot arbitrarily be shaped in order to investigate the circuit breaker during the turn-off process in detail.

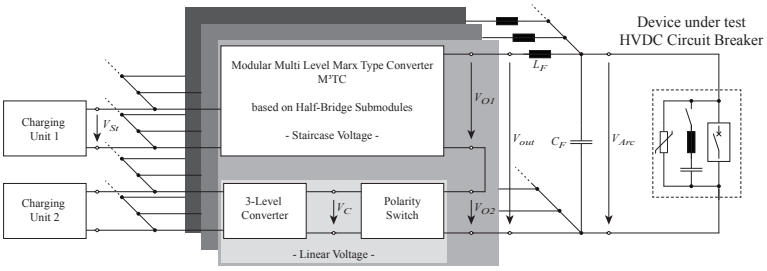

Figure 1: Basic concept of the proposed Unipolar Arbitrary Voltage Source (UnAVoSo) consisting of 21 parallel sources, which each is a combination of a stair case voltage source (M^3TC) and a low voltage linear source.

Table I: Specifications of the Unipolar Arbitrary Voltage Source (UnAVoSo).

Output voltage V_{out}	10 kV
Output current I_{out}	30 kA
Max. current gradient $^{di}/_{dt}\,\vert_{max}$	200 $^{A}/_{\mu s}$
Operation period T_{Pulse}	20 ms
Charging period	5 min

The latest research uses a buck converter to create arbitrary current/voltage waveforms [5] . A small buck inductance enables high current rise rates and the possibility to simulate the behaviour of a HVDC grid during fault conditions. Thus, this setup combines the good controllability of a synthetic test setup and the realistic conditions of the capacitor based solution. However, the switching losses of the semiconductor restricts the operation to several hundred switching transitions, limiting the maximum current amplitude and current shaping possibilities.

In order to overcome these limitations, a novel concept for an advanced Unipolar Arbitrary Voltage Source (UnAVoSo) for a Hardware-in-the-Loop Simulation System (HiLSS) as shown in Fig. 1 is presented in this paper. Based on previous studies on circuit breakers and faults in HVDC transmission systems, the maximal output voltage of the new system is set to 10 kV, with the system able to provide output currents of up to 30 kA for a period of up to 20 ms (cf. Table I). During the turn-off process of the circuit breaker, high transient voltages and currents can occur, and as a result the system must be able to generate signals with a current rise rate of up to 200 $A/\mu s$. A typical current shape of UnAVoSo is depicted in Fig. 15e).

The energy required during one turn-off process of the circuit breaker is provided by capacitors in order to avoid disturbances of the supplying grid. In the HiLSS the current through the circuit breaker is measured and the voltage across the inductance L_F is adjusted so that a predefined current flows. However, it is also possible to control the voltage shape V_{Arc}. After each turn-off action, the energy storage capacitors can be recharged during 5 minutes.

In section 2, a detailed description of the operating principle of the unipolar arbitrary voltage source is given. The two subsystems of the converter – the voltage submodules and the 3-level converter – are investigated in section 3 and 4. The control of the system is described in section 5 and the results are shown in section 6 by simulation models, and finally a prototype system is discussed in section 7.

2 Operating Principle

Considering the challenging specifications listed in Table I, conventional linear amplifier concepts and also hybrid concepts based on a switch-mode power supply combined with a linear amplifier as presented in [10], cannot be applied to generate the required voltage/current. This approach would result in high conduction/switching losses that would prevent high efficiency due to the high operating voltage/current. Therefore, in [5] a buck converter is used, which applies 4.5 kV IGBTs to generate a single 3 kV arbitrary shape voltage pulse. For increasing the output voltage to 10 kV a series connection of IGBTs would be necessary. However, even in the basic 3 kV source the switching losses are too high, so that only a limited number of switching transitions can be performed before the junction temperature hits the thermal limit.

Therefore, the presented arbitrary voltage source is based on a series connection of half bridge-submodules (Fig. 3, Modular Multi-Level Marx-Type Converter, M^3TC) generating a staircase output voltage V_{O1} as shown in Fig. 2d with voltage steps $V_{St} = 1.1\,\text{kV}$. In order to fill up the gaps between the voltage steps and generate a smooth output voltage, continuous voltage source is connected in series to the staircase voltage generator. Based on this approach the operating voltage of the continuous voltage source is significantly reduced, so that fast switching IGBTs can be used. This in combination with the lower operation voltage results in drastically lower switching losses and boosts the efficiency. Because of the large output currents, the converter system is split up into 21 parallel connected modules, that each provides a current of up to 1.4 kA.

The detailed operating principle can be seen in Fig. 2, where the generation of a linearly rising output voltage V_{Out} (Fig. 2e) is shown. Starting at $V_{Out} = 0\,\text{V}$ ($t = t_1$), all submodules are turned off, i.e. $V_{O1} = 0\,\text{V}$ and the continuous voltage

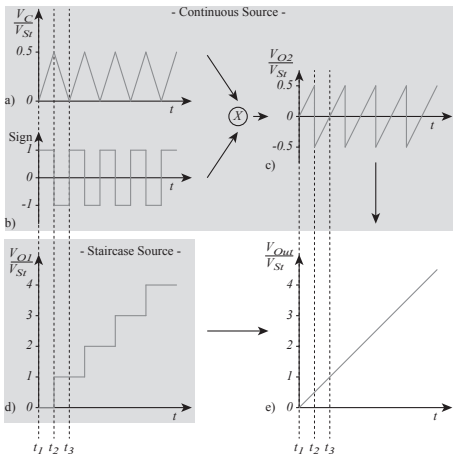

Figure 2: Output voltages of the different converter systems related to the step voltage V_{St}: a) Output voltage V_{O1} of the 3-level inverter, b) sign of the Polarity Change Unit, c) output voltage V_{O2} of the Polarity Change Unit, d) output voltage of M^3TC and e) total system output voltage V_{Out}.

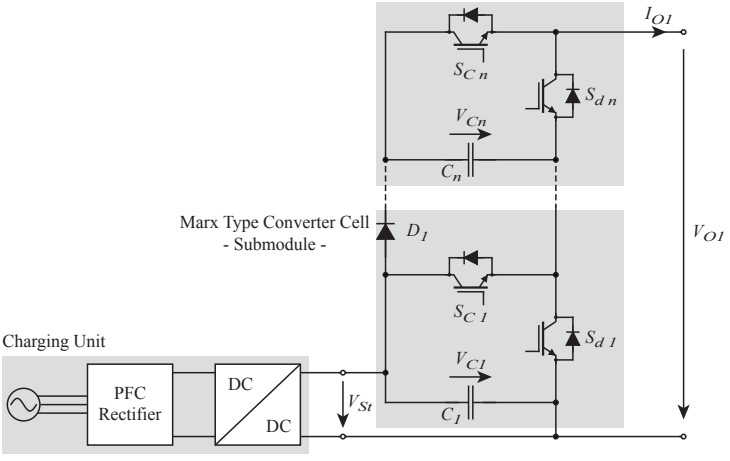

Figure 3: Modular Multi-Level Marx-Type Converter (M^3TC) with charging circuit for capacitors C_n.

source generates a linearly rising output voltage V_C. This voltage is connected via the Polarity Change Unit with a positive sign to V_{O2}. As soon as V_{O2} is $\frac{V_{St}}{2} = 550\,\text{V}$ ($t = t_2$), the first submodule is turned on, so that $V_{O1} = V_{St} = 1.1\,\text{kV}$. At the same time the polarity of V_{O2} is changed from +550 V to -550 V (Fig. 2b and c), so that the sum of the two voltages V_{O1} and V_{O2} is equal to 550 V. Then, because of the negative sign of the Polarity Changer, the amplitude of V_{O2} is linearly decreased to 0 V, so that the sum $V_{O1} + V_{O2}$ increases to 1.1 kV. When V_{O2} becomes 0 V ($t = t_3$), the polarity of V_{O2} is changed again and V_{O2} rises with V_C again.

Consequently, for a linear rising voltage, V_C has to be a triangle voltage, which in the considered case of $V_{Out,max} = 10\,\text{kV}$ has to have a nine times ($\frac{V_{Out,max}}{V_{St}} = 9$) higher frequency than V_{Out} and an amplitude of $\frac{V_{St}}{2}$ (Fig. 2a). The Polarity Changer performs a periodic sign change (Fig. 2b), so a saw tooth signal with an amplitude between -550 V and +550 V is generated (Fig. 2c).

3 Modular Multi-Level Marx-type Converter

The M^3TC is a combination of a modular multi-level (M^2C) converter ([11], [12]) and the charging concept applied in Marx generators. The M^3TC consists of nine stages, that each could provide a voltage of 1.1 kV (Fig. 3). A stage consists of a capacitor C_n for energy storage, two IGBTs S_{Cn}/S_{dn} and a charging diode. By turning on IGBT S_{Cn}, capacitor C_n is connected in series to the main circuit so that $V_{Cn} = 1.1\,\text{kV}$ is added to V_{O2}. In case S_{Cn} is turned off, current I_{O1} flows through the free-wheeling diode of S_{dn} and the stage adds $\approx 0\,\text{V}$ to V_{O2}. Each stage can be turned on/off separately allowing the output voltage to change in 1.1 kV increments.

As a result of this topology the used IGBTs have to perform less than ten switching actions during one pulse in the operation period T_{Pulse} (c.f. Fig. 15e). Thus they can be chosen with a low forward voltage drop in the on-state.

3.1 Energy Storage

Due to the fact, that the UnAVoSo cannot be supplied directly from the supply grid, the capacitors C_n have to provide the energy during the single output pulse with the total length T_{Pulse}. For this purpose film capacitors have been utilised with a low parasitic inductance and a high peak current.

The output current of each M^3TC module causes a voltage drop $\Delta V_{C,n}$ at the capacitor C_n which can be adjusted by the capacitance. On the other hand a large capacitance stores a large amount of energy and the ratio between stored energy W_C and used energy ΔW_C decreases (Eqn. (1)).

$$\frac{\Delta W_C}{W_C} = 1 - \frac{V_{C,2}^2}{V_{C,1}^2} \tag{1}$$

To evaluate and to demonstrate the limits of different capacitance values for C_n in Fig. 4 the voltage drop ΔV_C is shown to be dependent of the chosen capacitance and the average output current I_{out} within $T_{Pulse} = 20\,\text{ms}$. Considering a maximal output current $I_{out,max}$ of 1.4 kA per M^3TC module and an average output current $I_{out,avg} = 0.5 \cdot I_{out,max} = 700\text{A}$, a capacitor of 36 mF is chosen as a compromise to use 58 % of the capacitor's energy and to provide at the end of the operation period 65 % of the maximal output voltage V_{St}. In the worst case condition with $I_{out,avg} = 1.4\,\text{kA}$ the voltage at the end of the test period T_{Pulse} would be 29 % of V_{St}. This value could be increased afterwards by connecting additional capacitors in parallel.

To charge capacitors C_n between two pulses the concept of a Marx generator is used [13]. By switching IGBTs S_{dn} on, all capacitors are connected in parallel with the help of diodes D_n, so that a DC-DC converter can charge them (cf. Fig. 5). To avoid large currents between the capacitors, which are only limited by the diodes D_n and the switch S_{dn} and caused by balancing the voltage of the capacitors, it is essential that the voltage distribution fulfills: $V_{Cn} \leq V_{C(n+1)}$. This is realised by the control during operation described in section 5.

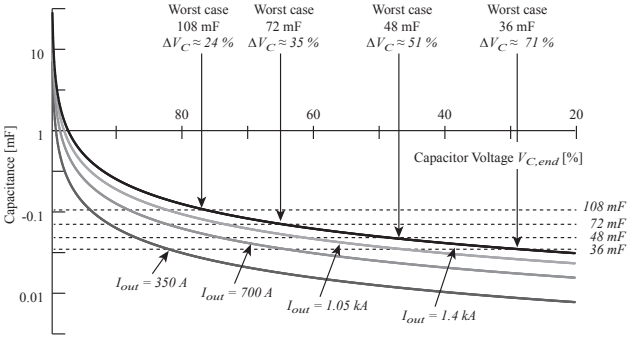

Figure 4: Achievable output voltages $V_{C,end}$ at the end of an operation period $T_{Pulse} = 20\,\text{ms}$ concerning different capacitances C_n and different average output currents $I_{out,avg}$.

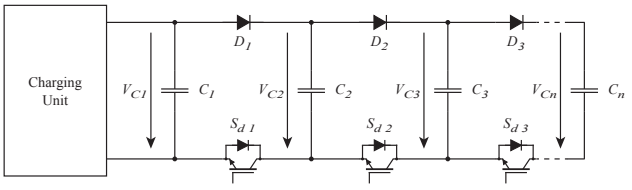

Figure 5: Equivalent circuit of M^3TC modules during charging period of the capacitors C_1 to C_n. For charging the capacitors all the IGBTs $S_{d,1} \ldots S_{d,n}$ are turned on.

4 3-Level Inverter & Polarity Change Unit

The continuous voltage source (Fig. 6) consists of an asymmetrical 3-level inverter and a H-bridge circuit for polarity changing. As shown in Fig. 6 the capacitor C_{out} is charged respectively discharged by six interleaved 3-level inverters which are coupled by using separate output inductors ($L_1, ..., L_6$). The Polarity Change Unit (PCU) connects this capacitor C_{out} with positive (using switches $S_{PS,1}$ and $S_{PS,4}$) or negative (using switches $S_{PS,2}$ and $S_{PS,3}$) polarity to V_{O2}.

Due to the voltage adding concept as presented in section 2 the continuous voltage source requires a high output signal frequency and a high slew rate. This can be achieved by using a high switching frequency, but with the disadvantage of large switching losses. To solve this, the converter uses zero-voltage-switching (ZVS) to reduce the switching losses and interleaving to reduce the current ripple.

An asymmetrical 3-level inverter is chosen because only positive voltages V_C must be generated. To enable fast switching IGBTs with $V_{CE,max} = 600\,\mathrm{V}$ are chosen, so that with an operating voltage range of 400 V per IGBT an output voltage range of 800 V of the 3-level inverter results. To control the inductor current I_L, it is necessary to apply positive and negative voltages V_L. Considering the range of V_C from 0 V to 550 V the 3 output levels are chosen as $V_{3L,neg} = -125\,\mathrm{V}$, $V_{3L,MP} = 275\,\mathrm{V}$ and $V_{3L,pos} = 675\,\mathrm{V} = 550\,\mathrm{V} + 125\,\mathrm{V}$. Thus it is possible to apply at least $V_L = \pm 125\,\mathrm{V}$ across the inductor.

To enable ZVS it is necessary to use a discontinuous current mode (DCM) to generate both a positive and a negative current during a switching cycle (cf. Fig. 10 and [14]). Therefore, the output inductance of the 3-level inverter has to be chosen to provide fast current gradients.

Concerning the maximal output current of a M^3TC module with $I_{out,max} = 1.4\,\mathrm{kA}$, a projected switching frequency of $f_{3L,period} = 10\,\mathrm{kHz}$ and a minimal voltage across L_{total} of $V_L = 125\,\mathrm{V}$, which is caused by the difference between the maximal output capacitor voltage $V_{C,max} = 550\,\mathrm{V}$ and the maximal positive voltage $V_{3L,pos}$, the value of L_{total} can be calculated. L_{total} represents the inductance of the 3-level inverter, if the system is realised without interleaving and only one 3-level inverter (c.f. section 5).

$$dI_L = 2 \cdot I_{out,max} + I_{C,change} = 3kA \qquad dt = \frac{1}{f_{3L,period}} = 100\mu s$$

$$V_L = V_{C,max} - V_{3L,pos} = 150V \qquad L_{total} = 5\,\mu\mathrm{H} \tag{2}$$

Because of using 6 interleaved inverter, the output current has to be divided equally to all inverters. By choosing $L_n = 6 \cdot L_{total}$ the maximal current gradients are reduced to 1/6 and the output current is also reduced by a factor of six. The choice of parameter for a 3-level inverter is listed in Table II.

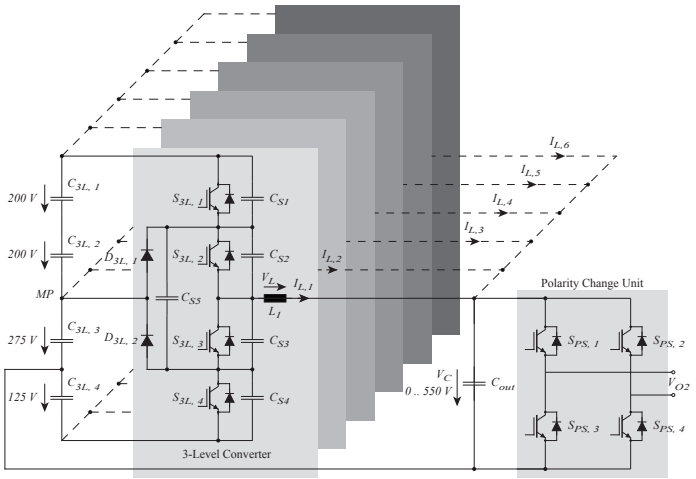

Figure 6: 6 times interleaved 3-level inverter with Polarity Change Unit (PCU) for generating a continuous arbitrary voltage V_{O2}.

Table II: Components of the 3-level inverter.

Name	Value	Condition
$C_{3L,1}, ..., C_{3L,4}$	53 mF	-
$C_{S1}, ..., C_{S4}$	40 nF	$V_{CSn} = 200\,\mathrm{V}$
C_{S5}	1 μF	$V_{CS5} = 200\,\mathrm{V}$
C_{out}	600 μF	$V_{out} = 550\,\mathrm{V}$
$L_1, ..., L_6$	30 μH	$V_L = 800\,\mathrm{V}$

5 Control of UnAVoSo

The control of UnAVoSo, depicted in Fig. 7, consists of a controller part, a stage selector, the M^3TC stages, 3-level inverter plus Polarity Change Unit (PCU) and the main output inductor.

The controller (1) is consists of three elements: To compensate the error between the reference value I_{ref} and the real output current I_{out} a PI controller is utilised. To improve the response time of the system for current gradients a PD controller is additionally used as pre control to deviate the reference value. Thus a gradient of $I_{out,ref}$ generates immediately a voltage step of $V_{out,ref}$. The third part of the controller adds the arc voltage V_{Arc} to $V_{out,ref}$ as a pre control to avoid large changes of the output current I_{out} affected by a change of load voltage V_{Arc}.

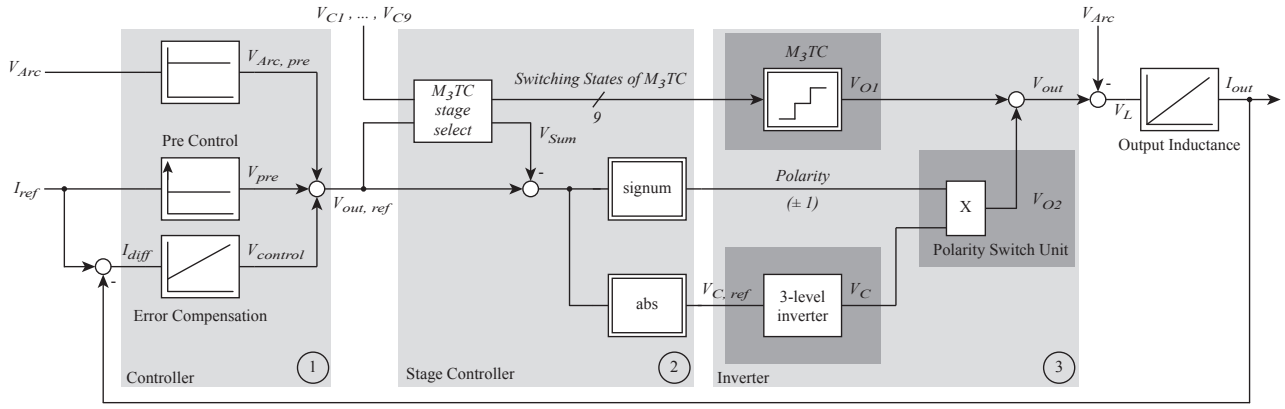

Figure 7: Control of UnAVoSo consisting of a controller part, a stage selector to convert the reference value $V_{out,ref}$ to switch states of M^3TC and PCU and $V_{C,ref}$ for the 3-level inverter.

5.1 Model of the 3-Level Inverter

The use of a variable length of the switching period T_{period} in combination with interleaving the six 3-level inverters requires the prediction of the output currents I_{Ln} and voltage V_C for a whole period in advance to allow the synchronisation of the inverters. Thus the control of the 3-level inverter system is based on a mathematical model of an inverter module, which is approximated using Taylor series expansion.

To identify the model's description the equivalent circuit shown in Fig. 9 is used based on a voltage source V_{3L} describing the inverter output voltage V_{Con}, the total inductance and a constant output current $I_{out,0}$. Because of the relatively large main inductance L_F and the switching period $T_{period} \approx 100\,\mu$s this current can be assumed constant.

$$V_L = L_{total}\frac{dI_L}{dt} \qquad I_C = C_{out}\frac{dV_C}{dt} \tag{3}$$

$$V_L = V_{Con} - V_C \qquad I_L = I_C + I_{out} \tag{4}$$

Differential Eqn. (3) and Eqn. (4) have been combined and solved by using initial values $I_L = I_{L,0}$ and $V_C = V_{C,0}$ at $t = 0$ (Eqn. (5)).

$$I_L(t) = \sqrt{\frac{C_{out}}{L_{total}}}\sin\left(\frac{t}{\sqrt{L_{total}C_{out}}}\right)\left(V_{Con} - V_{C,0}\right) + \cos\left(\frac{t}{\sqrt{L_{total}C_{out}}}\right)\left(I_{L,0} - I_{out,0}\right) + I_{out,0} \tag{5}$$

The stage selector (2) converts the continuous voltage signal $V_{out,ref}$ to switching states of the M^3TC and the PCU and calculates a reference signal for the 3-level inverter system. The detailed stage selection of M^3TC is shown in Fig. 8. In the beginning of the calculation all M^3TC stages are assumed to be switched off, so the output voltage $V_{O1} = V_{sum} = 0\,$V. Based on the measured capacitor voltages V_{Cn} of M^3TC, there is a comparison, if the difference between the reference value $V_{out,ref}$ and the voltage V_{sum}, which represents the voltage of the turned on M^3TC stages, is larger than half the capacitor voltage V_{Cn}. If this statement is false, it is possible to generate this difference by using the 3-level inverter. Otherwise an additional stage has to be turned on and that voltage V_{Ci} is added to V_{sum}. At the end of a calculation cycle there is a delay of $50\,\mu s$ to avoid fast oscillations. By always starting with the first M^3TC stage to be turned on, it is secured, that the condition for recharging $V_{Cn} \leq V_{C(n+1)}$ is fulfilled at every time.

Corresponding to Fig. 2 the sign of the difference between $V_{O1} = V_{sum}$ and $V_{out,ref}$ is used to control the state of the Polarity Switch Unit, while the reference signal $V_{C,ref}$ for the 3-level inverter is the absolute value of this difference.

The 3-level inverter includes an additional control and modulation part, which is depicted in Fig. 13 and will be described in the following subsections.

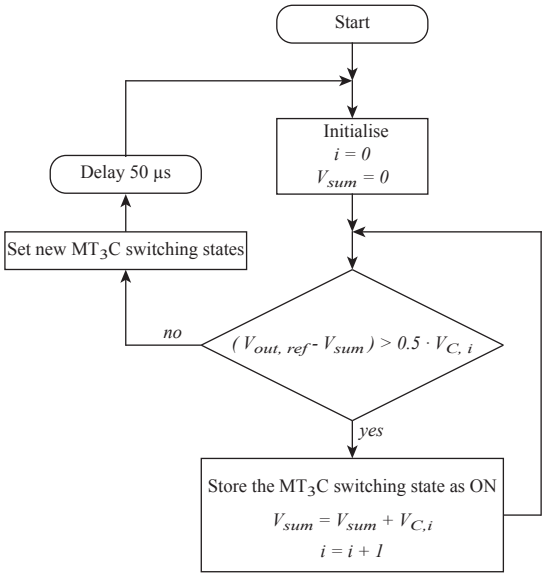

Figure 8: Algorithm to convert the voltage control signal V_{out} to switching states of M^3TC and of the Polarity Switch and calculate the value $V_{C,target}$ for the 3-Level Inverter System.

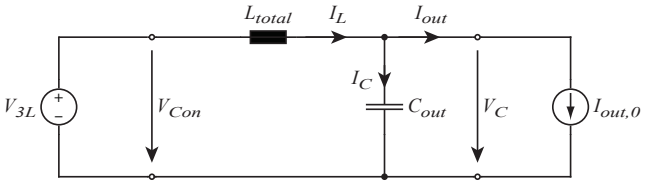

Figure 9: Equivalent circuit diagram of the combined 3-level inverter with inverter output voltage V_{Con}, inductance $L_{total} = \frac{1}{6}L_i$, capacitor C_{out} and the output current $I_{out,0}$, which is assumed to be constant.

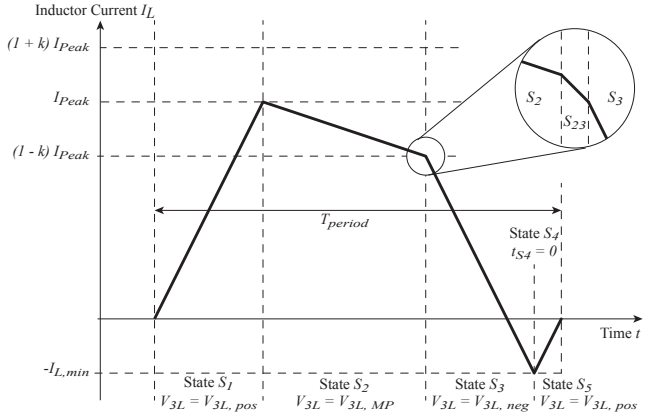

Figure 10: Inductor current I_L with a positive I_{peak} value using DCM to provide ZVS with $V_C > V_{3L,MP}$ because of reaching $I_L = (1-k)I_{Peak}$ at the end of state S_2.

To achieve a high dynamic, capacitor C_{out} is chosen to be as small as possible. Thus a voltage ripple ΔV_C is expected due to the non constant current I_C (Eqn (6)).

$$V_C(t) = V_{Con} - L_{total}\frac{dI_L}{dt} \tag{6}$$

To realise the calculation in a digital controller system, the equations are approximated by a Taylor series expansion. The current I_L is approximated by a 3rd degree Talor polynomial and the voltage V_C by a 2nd degree polynomial.

5.2 Modulation of the Master 3-Level Inverter

To enable interleaving the modulation of the 3-level inverter system is divided into a master inverter and 5 slave inverters, which are synchronised and time shifted to the master.

To provide ZVS it is necessary to use a discontinuous current mode (DCM) and generate at each switching period both a positive and a negative inductor current I_L with an amplitude of at least $I_{L,min}$ (see Fig. 10). This is necessary to discharge the capacitors C_{Sn} before turning on the IGBTs. The peak current I_{Peak} is used as control variable.

DCM is realised by a state machine, depicted in Fig. 11, that can generate both positive and negative current peak values. For positive peak currents I_{Peak} state S_1 is used to generate this current by using $V_{3L} = V_{3L,pos}$. S_2 uses $V_{3L} = V_{3L,MP}$ and I_L will reach for $V_{3L,neu} > V_C$ the upper respectively for $V_{3L,neu} < V_C$ the lower limit of a range defined around I_{Peak} by the factor k. The following state S_3 is used to generate a negative current peak with an amplitude of $-I_{L,min}$. State S_4 is not used with positive peak currents. The last state S_5 uses $V_{3L} = V_{3L,pos}$ and decreases the negative current I_L to zero.

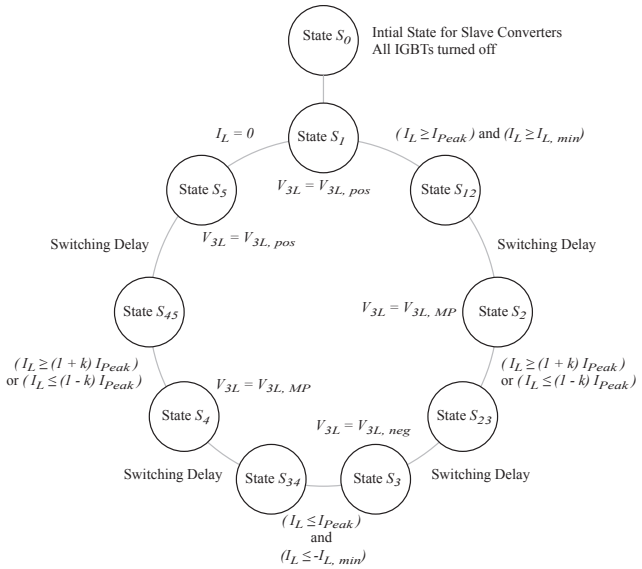

Figure 11: State machine to control the interleaved, ZVS, frequency variable 3-Level inverter System including the start state S_0.

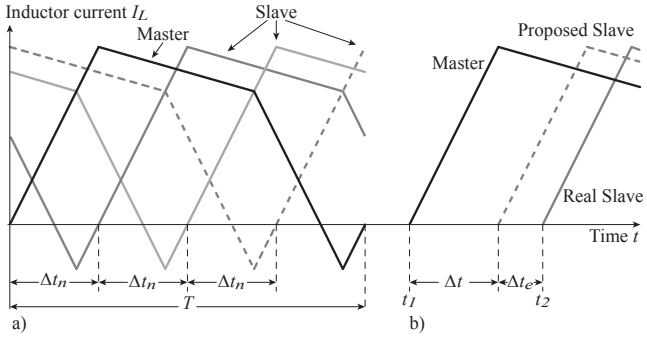

Figure 12: Interleaving and synchronisation of the 3-level inverter with a) adjusted offset of Δt_n and b) error calculation Δt_e.

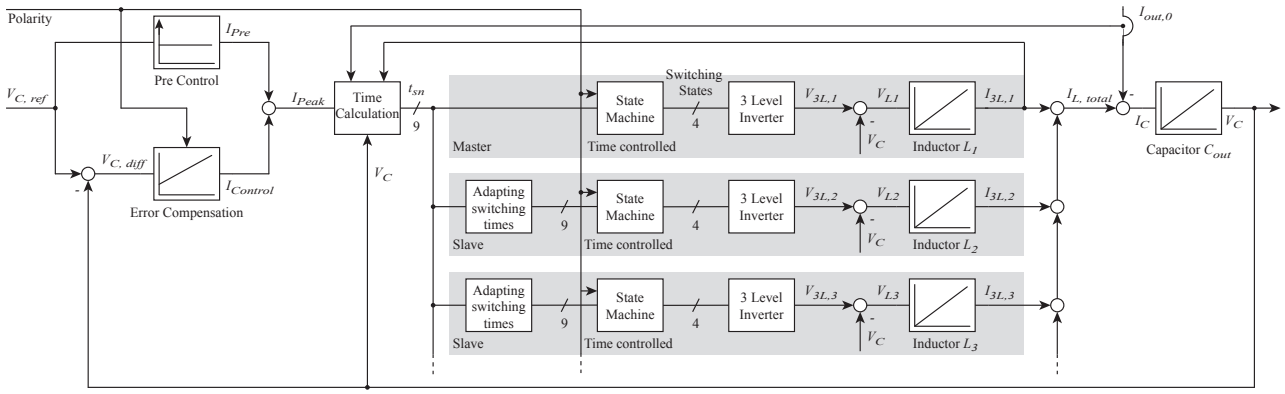

Figure 13: Control of the 3-level inverter system consisting of a PI- and a PD-controller, a module to calculate the times for the different states, a master inverter system and 5 slave inverter systems.

For negative peak currents, caused by a negative polarity of the PCU, the states S_1 and S_3 are used to generate the current ripple of $+I_{L,min}$ for ZVS, while state S_4 is used instead of S_2. States $S_{12},...,S_{45}$ are for the interlock delay.

For achieving interleaving, at beginning of state S_1, a whole cycle of the state machine is calculated in advance based on the mathematical model. For this purpose the Talyor approximation of Eqn. (5) has been transformed to calculate the time t_{Sn}, that is needed to reach a certain current $I_L(t_{Si})$, based on the initial conditions at the beginning of each state ($V_{C,0} = V_{C,S(i-1)}$, $I_{L,0} = I_{L,S(i-1)}$, V_{Con}, $I_{out,0}$). By using the time t_{Si} and the approximated equations of (5) and (6), $I_{L,Si}$ and $V_{C,Si}$ at the end of the state are calculated. This is done for all states ($i = 1,...,5$), so that the time of the period is approximately $T_{period} = \sum t_{Si} + 4 \cdot t_{Interlock}$.

The master 3-level inverter is controlled by these calculated times. To compensate current offset errors at the end of a period (i.e. $I_L(T_{period}) \neq 0$), the time t_{S5} is recalculated at entering state S_5 using real measurements as initial conditions $I_{L,0}$ and $V_{C,0}$.

5.3 Modulation of the Slave 3-Level Inverters

Each of the five interleaved converter has its own time-based state machine $SM_{S,j}$ ($j = 1,...,5$) and as soon as they enter state S_1 the switching times are copied from the time calculation unit (cf. Fig. 13). For interleaving it is necessary, that the beginning of a cycle of the slave state machines j is time shifted to the beginning of the master cycle by

$$\Delta t = j \cdot \Delta t_n \;=\; \frac{j}{n} T_{Period}. \tag{7}$$

To adjust the time offset between the single inverters for a positive peak current I_{peak}, the time t_{S2} of state S_2 is additionally recalculated by using Eqn. (8) (see Fig. 12).

$$t_{S2,new} = t_{S2} - \Delta t_e \;=\; t_{S2} - (t_2 - t_1 - \Delta t) \;=\; t_{S2} - (t_2 - t_1 - \frac{j}{n} T_{period}) \tag{8}$$

Because of changing the time for S_2 an current offset error is generated. This error is compensated by adapting the times for state S_3. Using the new times $t_{S2,new}$, $I_L(t_{S2,new})$ and $V_C(t_{S2,new})$ are recalculated and based on this new initial conditions, the time t_{S3} is computed.

For negative peak currents the times for the states S_4 and S_5 are used in the same way to synchronise interleaving.

The complete control of the 3-level inverter system is depicted in Fig. 13. The reference value I_{peak} for the modulation part is generated by a PI controller for error compensation and a PD controller to improve the step response time.

By changing the state of the PCU the sign of the output current $I_{out,0}$ is inverted. In order to enable a fast response to this large current gradient, the polarity signal is monitored. As soon as the polarity is switched, the times t_{Sn} of both master and slave state machines, beginning with the current state, are recalculated. Due to this interruption of the normal modulation process, interleaving is disturbed and has to be synchronised again.

6 Simulation Results

For designing the system and evaluating the performance, the proposed system has been modelled in detail in GeckoCircuit^{TM}. There, also the thermal design of the system considering switching and conduction losses is included in the simulation model.

The simulation results of the prototype system, which is described in section 7, are shown in Fig. 15. A typical current wave form (see Fig. 15e) consists of an arc ignition period (1) between 0 ms and 10 ms, a constant current (3) between 12 ms and 22 ms and typically a fast current gradient (4) at 22 ms to 22.07 ms to the peak current.

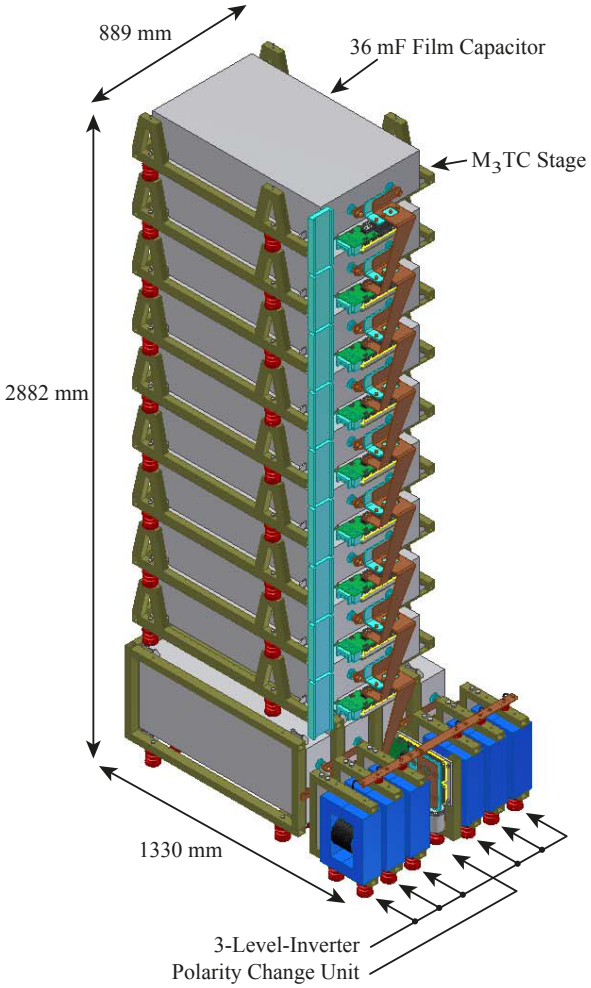

Figure 14: 3D Model of one UnAVoSo module, including nine M^3TC stages, six 3-Level Inverters including supply capacitors in the bottom part and in between the Polarity Change Unit.

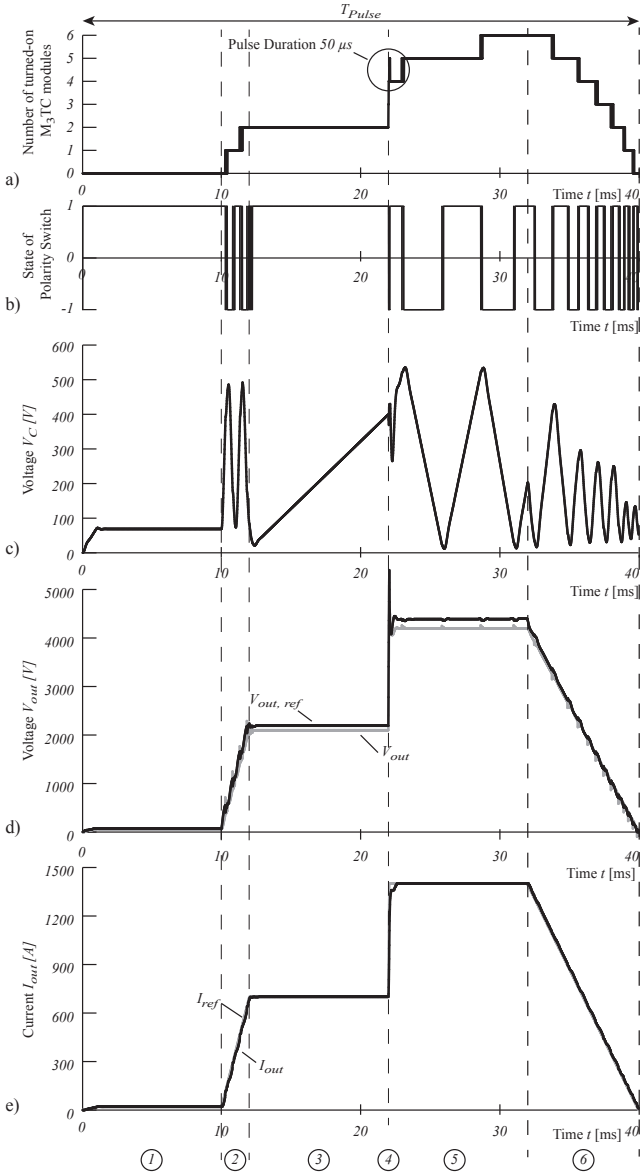

Figure 15: Simulation result of the prototype system generating a typical current shape, showing (a) the numbers of switched on M^3TC modules, (b) the state of the Polarity Change Unit, (c) the output voltage V_C of the 3-Level Inverter System, (d) the voltage control signal V_{out} and the real output voltage $V_{UnAVoSo}$ and (e) the target current signal I_{target} and the real output current I_{out}.

During the arc ignition (1) the current I_{out} is controlled only by the 3-level inverter system due to low arc voltage and low current. By adjusting the arc, the current is increased to a constant current (2), using the combination of M^3TC, PCU and 3-level inverter system (see Fig. 15a), b) and c). During period (3) the voltage drop ΔV_{Cn} of the M^3TC stages has to be compensated by increasing the voltage V_C of the continuous source. The fast current gradient (4) is mainly generated by switching two additional M^3TC stages, while the 3-level inverters system remains almost at the same output level.

Period (5) provides again a constant current $I_{out} = I_{out,max}$, causing a voltage drop ΔV_{Cn} and this has to be compensated by adding more M^3TC stages.

The more detailed simulation result of the 3-level inverter system, shown in Fig. 16, presents a triangle output voltage V_C with an amplitude of 550 V and a constant output current $I_{out,0} = 800$ A which polarity must be changed when the gradient of $V_{C,ref}$ changes. The ripple of the output current $\sum I_{L,n}$ after switching $I_{out,0}$, shows, that the inverter control has to synchronise the interleaving again. Furthermore, the adaptation of the inverter output current requires approximately 100 μs which causes a voltage ripple on the output voltage V_C, which will be reduced by optimising the controller in the next steps.

In Fig. 17 the synchronised interleaving of the 3-level inverter is shown. The currents of the separate inverters are distributed equally (Fig. 17b) and adjusted in every single cycle by readjusting the switching times (Fig. 17a). Due to interleaving, the ripple of the total output current is very small and the voltage ripple on V_C (Fig. 17c) is minimised. Further the output voltage $V_{Con,1}$ of one inverter (Fig. 17c) rises relatively slow during switching due to ZVS conditions.

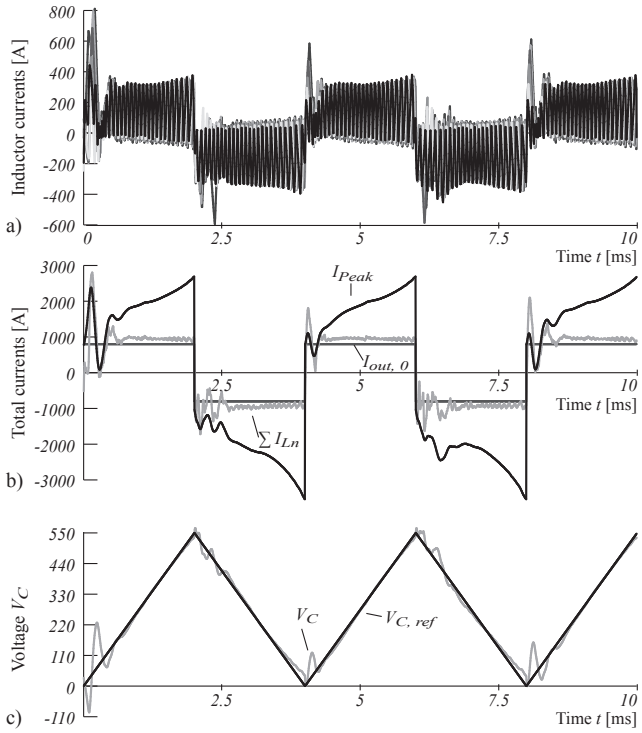

Figure 16: Simulation result of the 3-level inverter system, showing (a) the six interleaved inductor currents I_{Ln}, (b) the sum of these currents and the for control purposes used peak current value I_{Peak} and (c) the reference voltage $V_{C,ref}$ and the real capacitor voltage V_C for an output current $I_{out,0} = 800\,\mathrm{A}$.

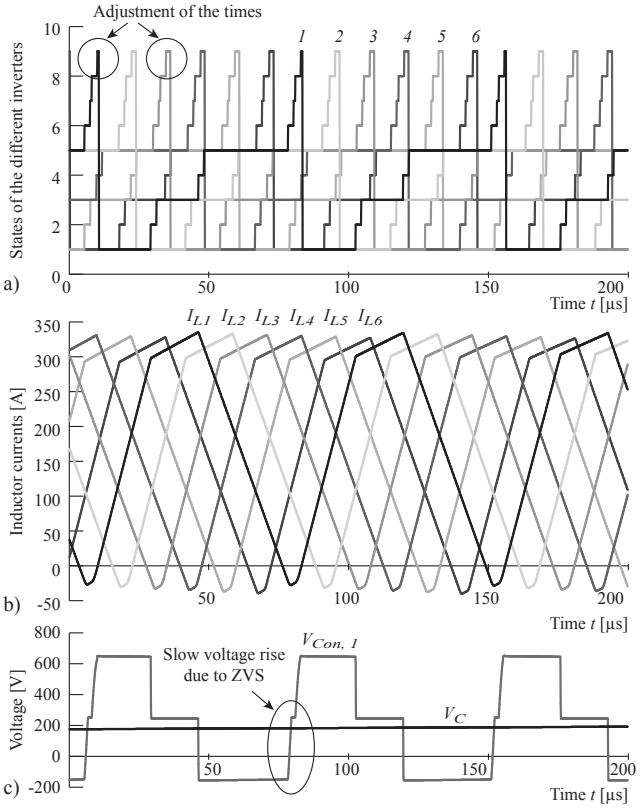

Figure 17: Simulation results of the interleaved 3-Level Inverter System, showing (a) the states of the six state machines, (b) the inductor currents I_{Ln} and (c) the capacitor voltage V_C and the inverter output voltage $V_{Con,1}$ including slow rising gradients caused by ZVS.

7 Prototype System

Based on the simulation results a prototype system of one module ($I_{out,max} = 1.4\,\mathrm{kA}$, $V_{out,max} = 10\,\mathrm{kV}$) has been designed. The main components and the required number of devices are listed in Table III. To minimise overvoltages the parasitic inductance has been reduced by using integrated 3-level switches as well as wide copper bus bars.

The main limitation for generating high dynamic current gradients by switching at high frequencies is the junction temperature, so that the switching losses must be reduced and the thermal design of the system is crucial. Based on the simulation, described in section 6, the thermal losses of the semiconductors have been estimated (see Fig. 19). Due to pulse operation and the thermal capacitances, the losses could exceed the loss values given for steady state operation.

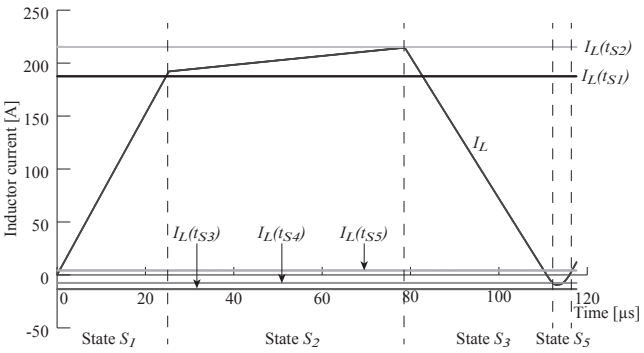

Figure 18: Validation of the model by simulation results, showing the inductor current I_{Ln} during one switching period and the estimated currents at the end of the different states I_{S1}, ..., I_{S5}.

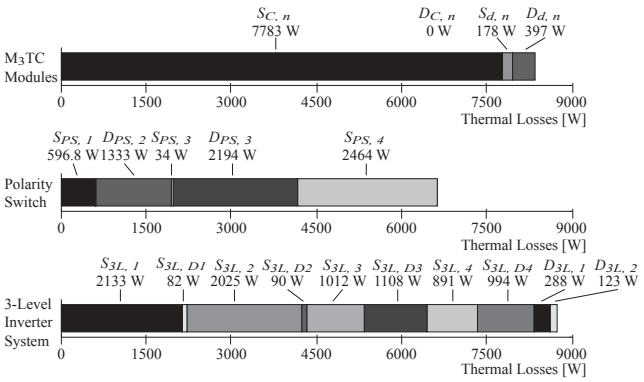

Figure 19: Calculated thermal losses of UnAVoSo with $P_{V,total} = 28.73\,\mathrm{kW}$ for the shown case in Fig. 15, differentiated by M^3TC, Polarity Switch and 3-level inverter system.

Table III: Main components of the Unipolar Arbitrary Voltage Source (UnAVoSo).

Circuit Part	Quantity	Type	
M^3TC	9	36 mF / 1100 V Film Capacitor	Electronicon E56.N88-366290
	9	Dual-IGBT-Module 1.7 kV 1.4 kA	Infineon FF1400 R17 IP4
Polarity Switch	2	Dual-IGBT-Module 1.2 kV 1.4 kA	Infineon FF1400 R12 IP4
3-Level Inverter	4	53 mF / 200 V Film Capacitor	Electronicon E56.N88
	3	600 μF / 600 V Film Capacitor	Electronicon E63.L95-184G10
	6	3-Level IGBT-Module 600 V 400 A	Semikron SKM 300 MLI 066 T
	6	30 μH / 800 V Inductance	

8 Conclusion

In the paper, a novel concept for an unipolar arbitrary voltage source based on modular submodules generating voltage steps in combination with a continuous voltage source compensating the voltage steps for high power applications such as hardware-in-the-loop simulation systems of DC circuit breakers is presented. With this concept a high current slew rate and a high efficiency can be achieved. For improving the system efficiency, interleaving and ZVS switching of the 3-level inverter are implemented. The proposed topology is validated by simulations and a prototype system is designed for an output voltage of 10 kV and 1.4 kA.

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