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Low-Cost Multi-Channel Data Transmission over a Single Plastic Optic Fibre for Isolated Sensing Applications

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Keywords

≪Communication for Power Electronics≫, ≪Data Transmission≫, ≪Measurement≫

Abstract

The growing need for higher efficiency in converter systems and in power electronic systems in general has led to the implementation of more complex and sophisticated control algorithms. Often, the controller unit is separated from the sensors and the data has to be transmitted via an isolated channel. Plastic optical fibers are utilized for this task due to their low cost, high robustness and easy handling. In order to reduce the number of fibers, intensity modulation can be used to transmit multiple signals over a single optical fiber. A recently introduced modulation scheme with an additional intensity level indicating the clock allows a simple clock recovery at the receiver. In this paper, three receiver concepts based on this modulation scheme are presented for medium data rates in the range of 20 - 50 Mbps which is sufficient for most power electronic applications. The low complexity and small footprint of the proposed concepts facilitate the system integration. Furthermore, a more compact system can be designed due to the lower number of necessary fibers and corresponding transmitter and receiver circuits.

1 Introduction

Many modern power electronic systems require high-speed communication interfaces for transmitting measured signals (e.g. voltage and current) to a central controller in order to achieve a dynamic and precise control [1–3]. In case of medium or high voltage applications, the communication channel needs to provide sufficient isolation and is therefore often realised with step-index plastic optical fibers (SI-POF). POF offer noise immunity, low-cost, high robustness and easy handling, making them an attractive solution for medium and high power converter systems. Typical POF lengths in these applications are within some 10's of meters.

A simple way to implement a robust communication link is to transmit the digitized measurement data via one dedicated fiber per signal. Additionally, the corresponding clock has to be transferred to the receiver to allow a synchronized sampling of the incoming data stream. The resulting relatively high number of required POFs (and the resulting wiring effort) as well as usually expensive transmitter and receiver components are a decisive disadvantage of this approach. Many transmitters/receivers and POFs also limit the practically achievable power density of a converter system.

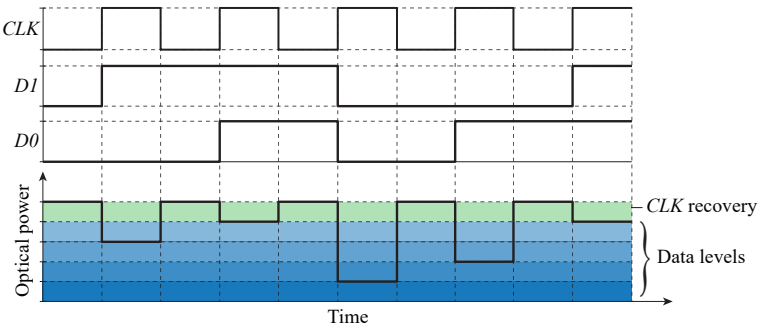


Table I: 2 channel PAM-DCD modulation

CLK	*D1*	*D0*	→	I_{LED}
0	x	x	→	I_{peak}
1	1	1	→	$0.75 \cdot I_{\text{peak}}$
1	1	0	→	$0.5 \cdot I_{\text{peak}}$
1	0	1	→	$0.25 \cdot I_{\text{peak}}$
1	0	0	→	0

Fig. 1: PAM-DCD modulation scheme using five intensity levels to transmit two data channels and the clock. The highest level (green) is used to indicate the clock to allow a simple clock recovery.

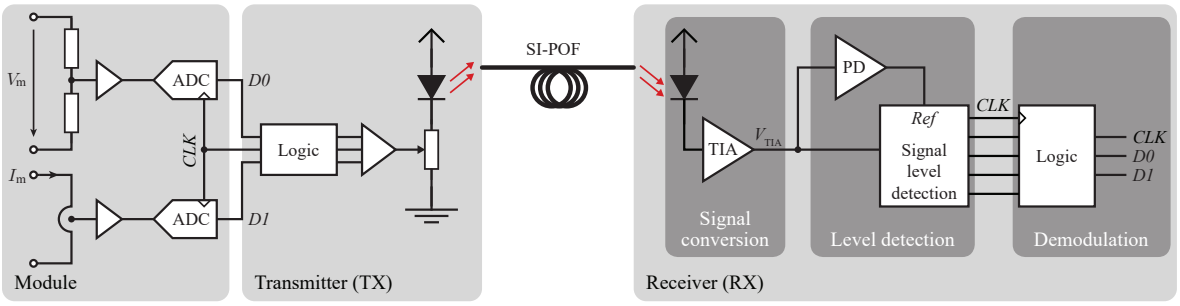


Fig. 2: Block diagram of the optical communication system for transmitting two data channels (e.g. voltage/current measurement of a converter module) and the clock with the PAM-DCD modulation.

An approach to reduce the number of POFs is to use time-division multiplexing as e.g. shown in [4]. Two data streams are interleaved and transmitted over a single fiber. This leads to a reduction of the effective data rate per signal by 50 %, which limits the transmission speed of this technique. The principle in [4] requires an additional second fibre to transmit the clock associated with the data.

The additional transmission of the clock signal via a dedicated fiber can be avoided by using coding schemes such as 8b/10b or Manchester encoding [5,6]. This allows to transmit the (time-division multiplexed) data together with the clock over a single fiber. However, the effective data rate is decreased because coding bits must be added to the data stream. This results in an increasing communication delay. With Manchester encoding, one bit of data is encoded as two bit of transmitted data (1b/2b encoding). While keeping the en-/decoding simple, this increases the number of clock cycles necessary to transmit the data by a factor of two. With 8b/10b encoding this major disadvantage is weakened but not eliminated. At the transmitter, an encoder has to implemented. This is usually done with look-up-tables stored in a complex programmable logic device (CPLD) or a FPGA. At the receiver, a decoder based on the same technology has to be implemented. Besides this, usually dedicated clock recovery ICs are used to synchronize the receiver logic with the transmitted data stream. All this significantly increases the system complexity. More details will be presented later in this paper.

In terms of transmission speed, the best performing approach to reduce the number of fibers is wavelength-division multiplexing. Here, different light sources with clearly separated spectra are used to transmit multiple signals over a single fiber. However, at the receiver expensive optical filters are required to demultiplex the signals [7]. Therefore, this solution is associated with high system complexity and cost.

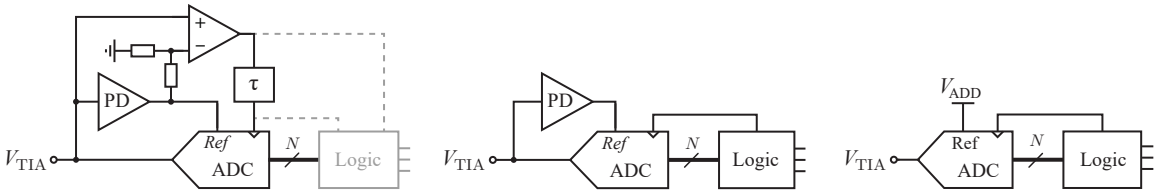
The use of intensity modulation and direct detection is a promising alternative that provides high data rates while maintaining relatively low complexity and costs. In this modulation scheme, the transmitted signal contains M discrete levels of different intensities which is known as pulse amplitude modulation (PAM). Each level represents a combination of data bits and consequently multiple signals can be transmitted over a single fiber at high speed [8].

In [9], a novel modulation scheme based on PAM is proposed, which allows a simple clock recovery at the receiver (direct clock detection - DCD). This PAM-DCD scheme introduces an additional level to indicate the clock signal as shown in Fig. 1 for two data signals $D0$, $D1$ and the transmission clock CLK. In this case, within every clock cycle, a data level which represents $D0$, $D1$ and the following clock level, are transmitted. Consequently, the baud rate is equal to the transmission clock or half the data rate. A higher data rate can be achieved simply by introducing more data levels in the modulation scheme. Beside the PAM-DCD scheme, [9] discusses transmitter and receiver implementations for high-speed communication as well. However, the high-speed implementations are relatively complex and costly. Therefore, low complexity receiver concepts based on analog-to-digital converters (ADC) for medium-speed communication interfaces in the range of 20 Mbps to 50 Mbps are proposed in this paper.

The paper is organized as follows: Section 2 shortly repeats the principles of PAM-DCD and introduces three alternative level detection circuits with lower hardware complexity compared to the implementations proposed in [9]. The detailed hardware design of these three concepts is described in Section 3. Section 4 presents measurement results for the developed hardware prototypes. Additionally the differences between the concepts are highlighted. In section 5, a communication link based on 8b/10b encoding is analyzed and compared to the proposed concepts.

2 Concept of PAM-DCD

In the following, an overview of the considered PAM-DCD based communication interface is presented. Fig. 2 shows the block diagram of the communication system for an exemplary use case where voltage V_m and current I_m of a converter module are measured and transferred to a central control unit. The data streams $D0$ and $D1$



a) SC-AR circuit b) AC-AR circuit c) AC-FR circuit

Fig. 3: Circuits of different level detection concepts regarded in this paper. a) Synchronously clocked level detection with adaptive reference (SC-AR) provided by the peak detector based on a N bit ADC. The simple clock recovery circuit with the delay element τ allows to synchronize the ADC with the incoming data stream. b) Asynchronously clocked level detection with adaptive reference (AC-AR) requires oversampling of the signal. c) Asynchronously clocked receiver with fixed reference (AC-FR) significantly reduces the hardware complexity of the design by performing the peak detection in the digital domain.

are supplied to the transmitter. Subsequently, the two data streams and the associated clock are mapped on five different intensity levels (cf. Fig. 1) by modulation of the current which flows through the light-emitting diode (LED). The truth table of the transmitter circuit and the corresponding levels are shown for clarity in Tab. I.

The receiver can be subdivided into three major parts (Fig. 2):

1. In the signal conversion circuit, a current proportional to the incident optical power is generated by a photodiode. The magnitude of the photocurrent is dependant on the length of the POF. A transimpedance amplifier (TIA) converts the current to a voltage V_{TIA} and and provides additional gain.
2. The level detection part as presented in [9], consists of a peak detector (PD) and a signal level detection circuit. As shown in Fig. 1, the highest level is transmitted in every clock cycle and is used for clock recovery as well as a reference for the signal level detection circuit. This reference signal is generated by the PD. In [9], an analog PD is used and the level detection is implemented with discrete comparators which allows a high-speed operation.
3. The last part is the demodulation stage that regenerates the data streams *D0, D1* from the detected signal levels. The receiver logic used for level detection and demodulation can be implemented in the control unit or in a dedicated integrated circuit (CPLD, FPGA or DSP).

2.1 Level Detection Concepts

After the basic concept of PAM-DCD has been explained, three different concepts for the level detection part of the receiver are proposed in the following. The general aim is to reduce the complexity and the part count of the level detection concept previously presented in [9] by using an ADC instead of comparators. The three level detection circuits differ in the complexity of the analog circuits, which results in a different part count and PCB footprint. These and other parameters are compared in Sec. 4.2 later in this paper.

Synchronously Clocked, Adaptive Reference (SC-AR)

Fig. 3a shows a synchronously clocked, adaptive reference circuit (SC-AR) very similar to the circuit proposed in [9]. The only difference is that an ADC instead of a voltage divider plus three comparators is used for the signal level detection. The dynamic adjustment of the ADC reference voltage by the analog peak detector (PD, cf. Sec. 3.2) ensures a reliable communication over a long POF because the least significant bit voltage (LSB) of the ADC scales down proportionally with the signal strength. Consequently, the thresholds for the level detection can be set to a fixed digital value. Moreover, the peak voltage is used to generate the recovered clock signal by providing it as reference to a comparator (via a voltage divider as shown in Fig. 3a). In order to synchronize the recovered clock with the data valid window, a delay element τ is inserted. This delay can be implemented as a discrete element or in the receiver logic. However, by using a discrete delay element the shown circuit is fully functional without additional logic as it does not rely on an external clock. An ADC with a sampling rate in the range of the transmission clock can be used because oversampling is not necessary in this concept due to the data synchronous clocking. The SC-AR has the highest complexity of all presented receivers and consequently the largest printed circuit board (PCB) footprint. The necessary large reference voltage range of the ADC limits the number of commercially available components.

Asynchronously Clocked, Adaptive Reference (AC-AR)

The receiver complexity can be reduced by omitting the clock recovery with the comparator and providing an external clock as shown in the asynchronously clocked, adaptive reference circuit (AC-AR) in Fig. 3b. In order to reliably detect the levels, the TIA output signal has to be sampled by the ADC after the steady-state is reached. Therefore, the ADC needs to be operated at a higher sampling rate compared to the SC-AR. The required sampling frequency of the ADC is determined by two parameters: The transmission clock period T_{TX} and the rise

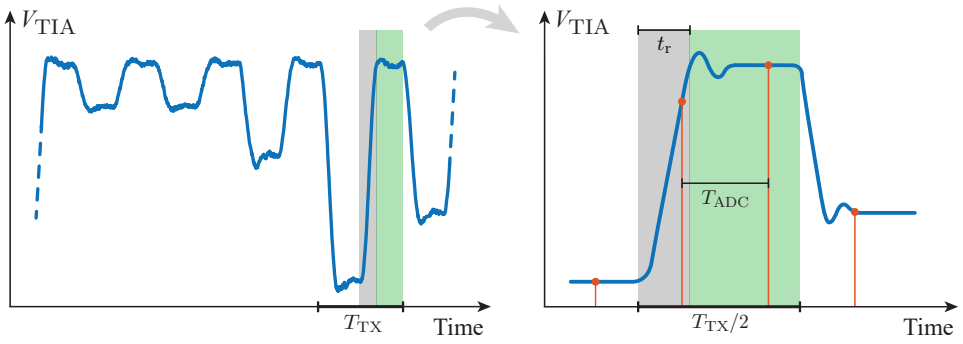


Fig. 4: Determination of the required ADC sampling rate. The sampling interval T_{ADC} should be smaller than the worst case steady-state time of the TIA output signal according to $T_{\mathrm{ADC}} < T_{\mathrm{TX}}/2 - t_{\mathrm{r}}$, with the transmission clock period T_{TX} and the signal rise time t_{r}.

time of the TIA output t_{r} at maximum signal swing. Obviously, a higher transmission clock requires a smaller sampling interval. Likewise, a lower TIA bandwidth leads to increased signal rise and fall times which results in a shorter steady-state time interval of the signal. As shown in Fig. 4, the sampling interval T_{ADC} needs to fulfill the requirement

$$T_{\mathrm{ADC}} < T_{\mathrm{TX}}/2 - t_{\mathrm{r}}\,, \tag{1}$$

for a correct sampling of the peak of the signal. Therefore, the TIA should provide a relatively high bandwidth in order to relax the bandwidth requirements for the ADC. Note that an anti-aliasing filter is not deployed in the signal chain because the ADC is used to detect discrete levels in the signal and a precise reconstruction of the analog waveform is not necessary. Moreover, the anti-aliasing filter would increase the signal rise and fall times requiring a higher ADC sampling rate.

Asynchronously Clocked, Fixed Reference (AC-FR)

A further reduction in complexity can be achieved by using a fixed reference for the ADC as shown in the asynchronous clocked, fixed reference circuit (AC-FR) in Fig. 3c. The low number of components results in a small PCB footprint of the receiver, which provides flexibility and facilitates the integration in existing systems. The bandwidth requirement for the ADC is the same as in the AC-AR. However, a digital peak detection needs to be implemented to derive the level thresholds which requires a larger number of logic elements. In contrast to the previous concepts, the LSB voltage does not scale down with the incident optical power and therefore, the available bits of the ADC are not optimally used for increasing POF lengths. Without adaption of the ADC reference voltage, this limits the maximum length of the POF.

3 Analog Circuit Design and Logic Implementation

In the following, the detailed designs of the analog circuits and the required logic for the different level detection circuits are explained.

3.1 Transimpedance Amplifier (TIA)

A single stage TIA as shown in Fig. 5a is used to convert the photocurrent I_{ph} to a usable voltage signal. This circuit shows a low complexity and allows to achieve a high bandwidth because the output signal swing V_{TIA} is decoupled from the relatively large photodiode junction capacitance C_{d}.

The gain of the TIA is set by resistor R_{f} in the feedback path. Typically, the expected photocurrent amplitude is in the range of a few hundreds of µA and needs to be converted to a voltage signal with several volts in magnitude. Therefore, a relatively large R_{f} in the kΩ range has to be used. Together with the input capacitance of the operational amplifier OPA_1 and C_{d}, this results in a large phase lag in the feedback path which causes stability problems. In order to compensate the phase shift and to obtain a stable circuit, a feedback capacitance C_{f} is connected in parallel to R_{f}. The dimensioning of C_{f} is critical because it also reduces the circuit bandwidth [10]. The bootstrap circuit based on JFET T_1 is introduced for increasing the bandwidth by reducing the voltage variation across C_{d}. At high frequencies, the open loop gain of OPA_1 starts to decline and a residual signal swing V_{diff} will occur at its inverting input port. This voltage variation is also present across C_{d} and results in a capacitive current which reduces the usable photocurrent. By connecting JFET T_1 in source follower configuration, a feedback loop with

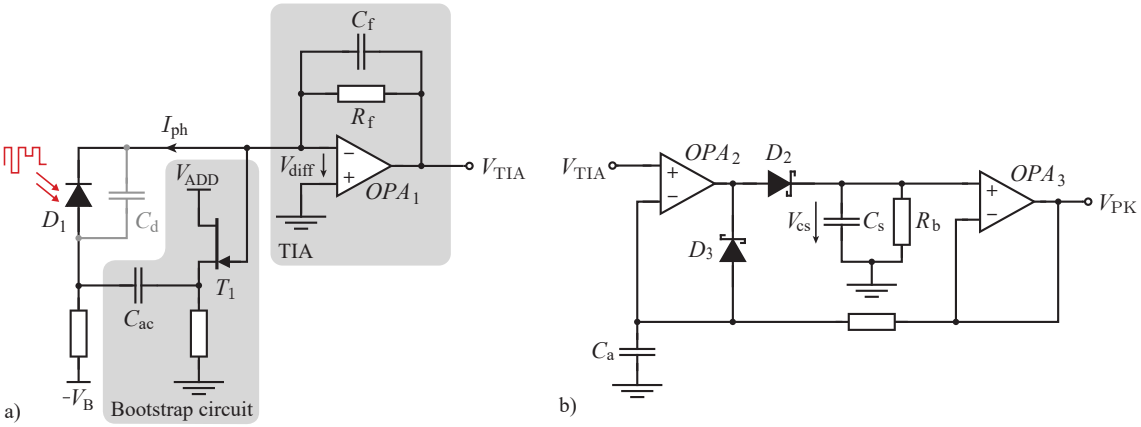


Fig. 5: a) Single stage TIA circuit with bootstrapped photodiode b) Analog peak detector.

approximately unity gain from the cathode to the anode of the photodiode is realized. The feedback loop significantly reduces the capacitive current resulting in an improved transient response. The AC-coupling capacitance C_{ac} allows that the photodiode can be biased independently from the bootstrap circuit. Given that a low noise JFET is used, the bootstrapping has a positive effect on the noise performance of the TIA as well. It reduces the high frequency noise by reducing the influence of the input referred noise voltage of OPA_1 on the output voltage [11]. A SPICE simulation of the shown circuit resulted in a particularly low output referred noise voltage of 208 μV_{RMS} which is essential for detecting a high number of signal amplitude levels.

An important parameter for the receiver design is the signal rise time at the output of the TIA. According to [12], the signal rise time can be estimated with the circuit bandwidth f_{3dB} as $t_r = {}^{0.35}/_{f_{3dB}}$. The bandwidth of the TIA is given by

$$f_{3dB} = \sqrt{{}^{f_{gbw}}/_{2\pi R_f(C_f+C_d)}}, \tag{2}$$

with the gain-bandwidth product f_{gbw} of OPA_1. Consequently, the rise time can be decreased by a faster OPA, by using lower gain or by a smaller C_d. A simple approach to reduce this capacitance is to increase the photodiode reverse bias voltage V_B which results in a downscaling of C_d proportional to ${}^{1}/_{\sqrt{V_B}}$ [10].

3.2 Analog Peak Detector

An implementation of the analog PD used in Fig. 3a/b for dynamic ADC reference adjustment and clock recovery is shown in Fig. 5b. Its basic principle is to store the magnitude of the peak voltage as a charge in capacitor C_s. Schottky diode D_2 only conducts if the output voltage of OPA_2 is higher than the voltage V_{cs} such that the highest positive voltage of the input signal is tracked. Note that OPA_2 has to compensate the forward voltage drop of D_2. This implies that the PD needs to operate on a supply voltage higher than the expected maximum TIA output voltage. An additional Schottky diode D_3 is added in the feedback path which prevents saturation of OPA_2 at the lower rail for input voltages smaller than V_{cs}. Bleeding resistor R_b is added in parallel to C_s to follow temporary changes in the signal strength. Its value is chosen such that the time constant $\tau_{RC} = R_b C_s$ is much bigger than the signal period to ensure that the accuracy of the PD is not impaired. The smallest detectable peak voltage is determined by the product of R_b and the input bias current of OPA_3 [11]. Capacitor C_a is introduced to delay the response in the feedback path. The value of C_a adjusts the overshoot caused by OPA_2 and provides the possibility to optimize the circuit for certain input amplitude ranges. The noise performance of the analog PD is particularly important because it is used as a reference for the ADC in the level detection circuit. According to SPICE simulations, the analog PD shows a low output referred noise voltage of 450 μV_{RMS}. This noise voltage can be reduced further by using a larger capacitor at the reference input of the ADC.

In order to achieve a good detection accuracy even for fast input signals, an operational amplifier with low input capacitance, high gain-bandwidth product and high slew rate should be chosen for OPA_2. Furthermore, it should be capable of driving large capacitive loads. OPA_3 should feature a low input bias current if a high dynamic range is desired.

3.3 Logic Implementation

In the case of SC-AR and AC-AR type receivers, the complexity of the digital circuity is low. Since the peak detection is performed by the use of the described dedicated analog circuit, the threshold voltages/values for the level detection do not need to be derived from the peak and are fixed. With an SC-AR type level detection circuit,

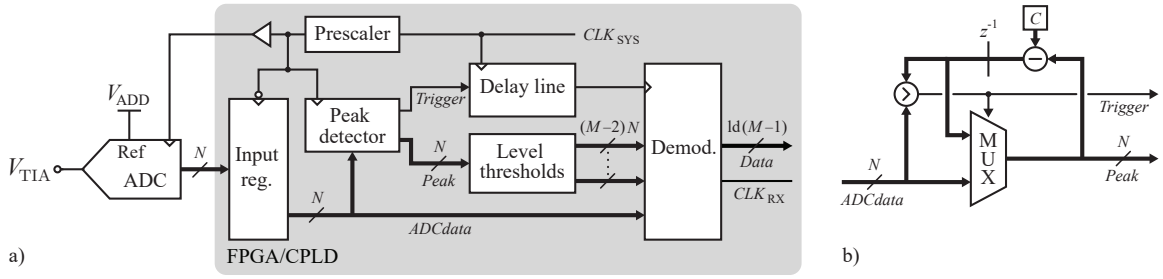


Fig. 6: a) Block diagram of the digital implementation for the AC-FR circuit, b) data dependency graph of the digital peak detection.

the clock for the ADC is supplied by the external comparator. In order to provide a stable duty cycle, the comparator signal is fed to a phase-locked loop (PLL) within the FPGA and the PLL output is used to clock the ADC. The PLL is also used to generate the necessary delay for synchronization with the data valid window. SC-AR uses the least digital resources and the discretized TIA signal can directly be demodulated.

Fig. 6a shows the block diagram of the digital datapath for AC-FR circuit. The TIA output signal is sampled by the ADC with a suitable sampling rate and the N bits are registered at the FPGA. First, the peak needs to be detected which is done by the digital PD shown in Fig. 6b. Its functionality is similar to the analog PD: The most recent peak in the *ADCdata* signal is stored in a register and decremented by a constant value C every clock cycle. This is done to react on temporary changes of the signal's strength. If a new signal peak occurs, the value in the register is updated. Additionally, the *Trigger* signal is asserted to indicate that a new peak was detected. Subsequently, the *Trigger* signal is delayed to align it with the data valid window of the received signal. The level thresholds for the demodulation are derived from the peak voltage with combinational logic. For $M-1$ data levels, $M-2$ thresholds are necessary with a width of N bits. At the rising edge of the *Trigger* signal, the *ADCdata* signal is demodulated.

4 Experimental results

In order to validate the performance of the proposed receiver concepts, a prototype is designed and shown in Fig. 7 together with the transmitter. The prototype implements all three receiver circuits on a single PCB. The used components are listed in Tab. II. Note that low-cost parts are used for this implementation and that higher data

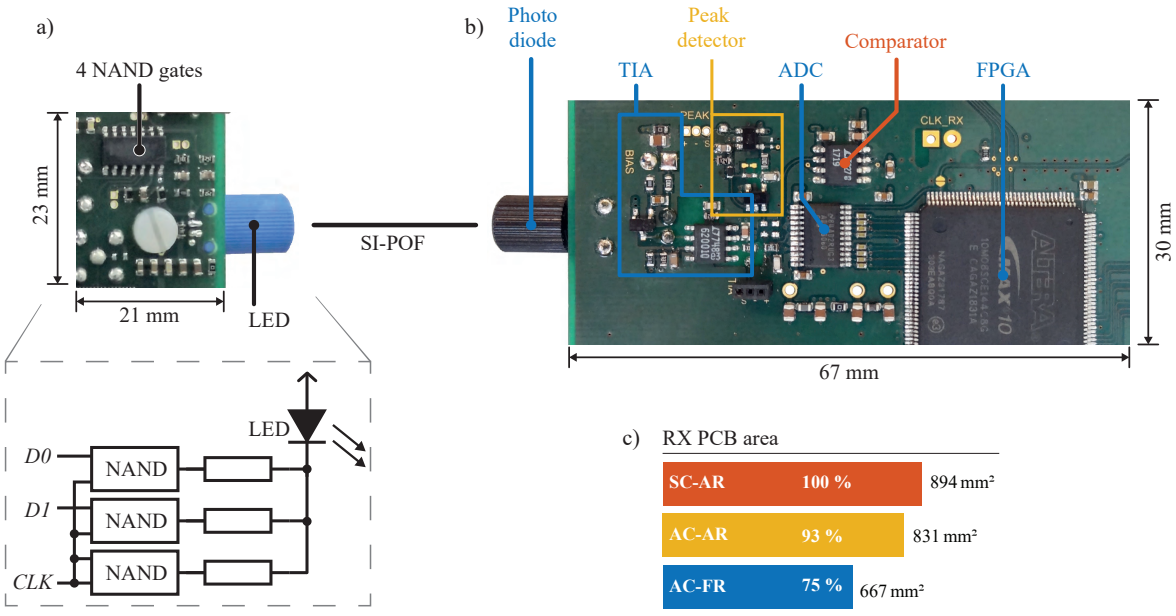


Fig. 7: a) Five level transmitter PCB implementation and simplified schematic used for the presented measurements, b) Experimental receiver prototype which integrates the three proposed receivers: components with blue markings are used for all three proposed level detection circuits. The components with yellow markings are used for the AC-AR and SC-AR circuit only. The components with red markings are exclusively required for the SC-AR circuit, c) graphical comparison of the PCB area occupied by the different concepts presented in this paper.

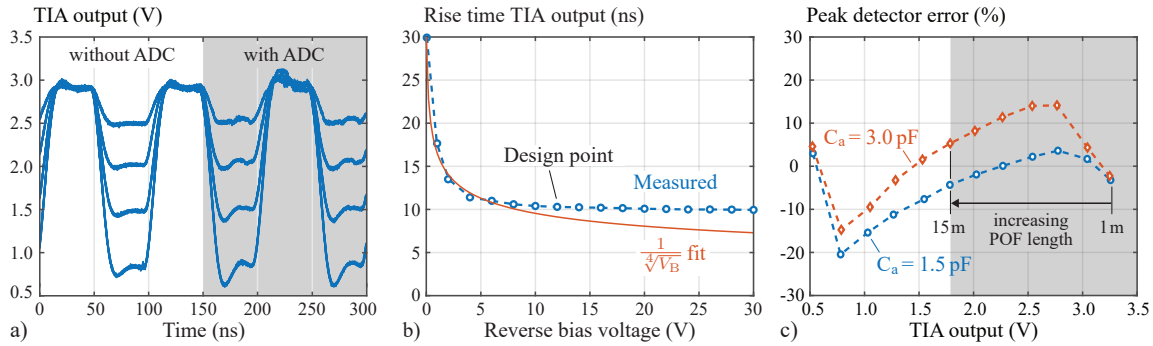


Fig. 8: Experimental results of the analog circuits: a) eye diagrams of the TIA output for a 10 MHz transmission clock with and without a connected ADC, b) rise time of the TIA output, c) accuracy of the analog peak detector. C_a is defined in Fig. 5b.

rates could be achieved with different components. Furthermore, the PCB is designed to provide easy access to the signals and is therefore not optimized for size. With other device packages and a denser layout, the overall PCB footprint could be decreased significantly. In the following, the measurement results for the analog circuits as well as for the three receivers are presented and compared.

4.1 Results for the analog circuits

The TIA provides a gain of 75 dB and generates a maximum output voltage of 3.3 V for the highest expected photocurrent. Fig. 8a shows its eye diagram with five levels for a transmission clock of 10 MHz. Note, that the PAM-DCD eye diagram differs from a standard PAM eye diagram because the signal returns to the highest level in each clock cycle. Without the ADC connected to the TIA, the TIA output signal shows well separated levels with a low overshoot on the signal. If the ADC is connected to the TIA output, the overshoot increases in the worst case up to 20 %. This behavior is caused by the additional capacitance of the ADC at the TIA output and can be counteracted by increasing the feedback capacitance C_f. According to (2), the bandwidth is reduced by a larger C_f and the response is slowed down. Furthermore, the TIA signal is slightly distorted in case the ADC is connected. This is caused by the changing capacitance depending on the state of the sample-and-hold stage [13]. These two effects need to be considered in the TIA design especially if the voltage difference between two adjacent levels is getting small, e.g. by using more levels or by using long POFs.

As mentioned before, the rise time of the TIA output signal is an important parameter and determines the required sampling rate of the ADC as shown in (1). The rise time can be reduced by increasing the reverse bias voltage of the photodiode as depicted in Fig. 8b. Up to a reverse bias voltage of 8 V, the rise time decreases as expected proportional to $1/\sqrt[4]{V_B}$. Above this voltage, the parasitic capacitances from the interconnections become dominant and no substantial improvement is achieved. Therefore, the photodiode does not need to be biased with its maximum sustainable reverse voltage and lower voltages can be used which simplifies the supply design. In the prototype, V_B is fixed to 12 V, which is already available as a supply voltage.

Fig. 8c shows the accuracy of the analog PD. The used OPA has a relatively high input bias current of 4 µA. Therefore, the smallest detectable peak is in the range of 500 mV with a used bleeding resistor of 120 kΩ. This is well below the expected peak voltages for POF lengths in the range of 1 - 15 m. With a capacitor of $C_a = 1.5$ pF,

Table II: Components used in the PAM-DCD transmitter and receiver prototypes.

	Component	**Part number**	**Manufacturer**
Transmitter	LED	IF-E99B	Industrial Fiberoptics
	NAND gates	CD74ACT08	Texas Instruments
Receiver	Photodiode	SFH250V	Avago
	JFET	CPH3910	ON Semiconductor
	OPA (TIA)	LT6200-10	Analog Devices
	OPAs (Peak Detector)	AD8061	Analog Devices
	Schottky diodes	D_2: BAS40-02L	Infineon
		D_3: DB2L33500L	Panasonic
	Comparator	LT1719	Analog Devices
	ADC	ADC08060	Texas Instruments
	FPGA	MAX10	Altera/Intel

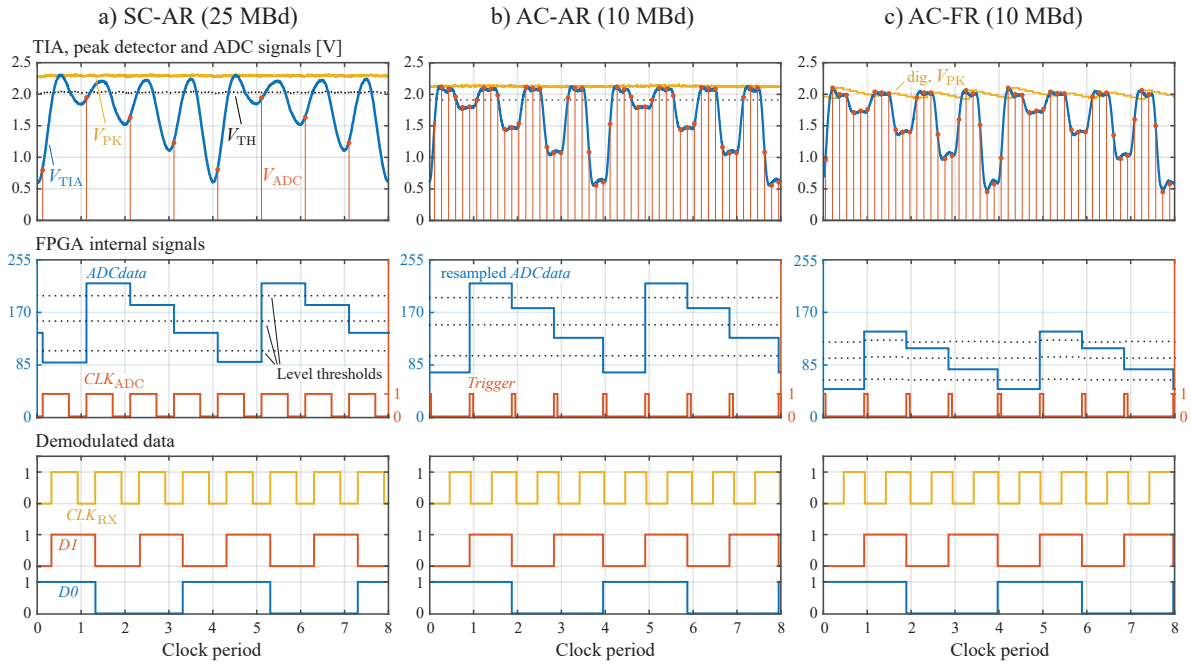


Fig. 9: System level measurement results with a 10 m POF for the proposed level detection circuits using two data channels.

the maximum expected error for the peak is $-4.7\,\%$ in the corresponding TIA output range. If longer POFs are used, the accuracy can be improved by increasing C_a. The time constant of the parallel network of bleeding resistor and storing capacitance is 67 µs, therefore the PD is able to follow even fast changes of the peak voltage.

4.2 System level comparison for communication over a 10 m POF

In Fig. 9, measurements for the full transmission path including all receiver concepts are shown. For the SC-AR circuit in Fig. 9a, a higher transmission clock had to be used in order to fulfill the minimum speed requirement of the ADC due to the data synchronous clocking. Therefore, the corresponding measurements are shown at a higher baud rate.

For both the SC-AR and the AC-AR type receivers, the analog PD reliably tracks the maximum signal voltage and automatically adjusts the ADC reference. In the SC-AR circuit, a threshold voltage V_{TH} is derived from the peak voltage V_{PK} which is provided to the comparator to recover the clock of the received signal. After delaying and stabilizing the duty cycle of the comparator output signal with a PLL, it is used as clock CLK_{ADC} for the ADC. The demodulation of the data is achieved by simply comparing the *ADCdata* signal with the fixed level thresholds.

In the AC-AR circuit, shown in Fig. 9b, the TIA output is oversampled. As before, the *ADCdata* signal is compared with fixed level thresholds due to the automatic ADC reference adjustment. If the *ADCdata* signal reaches the highest level, a signal is asserted to indicate that a new clock period starts. This signal is delayed such that it is aligned with the data valid window and is subsequently used as the *Trigger* signal in the demodulation stage to resample the *ADCdata* signal. The demodulation of the resampled *ADCdata* signal is done in the same way as in the SC-AR circuit.

The AC-FR circuit, shown in Fig. 9c, does not rely on an analog PD and the ADC reference voltage is fixed. Therefore, the resolution of the chosen 8 bit ADC is not used as efficiently as in the other two concepts. The level thresholds are derived from the digitally detected peak in the *ADCdata* signal. Similar to the AC-AR circuit, a *Trigger* signal is generated whenever a new peak occurs and aligned with the data valid window.

Further parameter comparisons of the three concepts in terms of circuit complexity and performance are given in Tab. III. The AC-FR receiver shows a 25 % smaller PCB footprint compared to the SC-AR circuit as also shown in Fig. 7c. The simple demodulation of the received data results in a low usage of logic elements. Interestingly, the number of used logic elements does not significantly differ for the three circuits due to the elaborate optimization of the datapath at compile time. Note, that due to the required PLL for the SC-AR receiver, the FPGA/CPLD required for the AC-AR and AC-FR receiver types is even cheaper than the one for the SC-AR receiver. In order to verify the reliability of the three designs, Bit-Error-Rate (BER) tests were performed with pseudo-random generated data over a runtime of 15 h and with a 10 m long POF. Under laboratory conditions, the BER was determined to be less than 10^{-12} for all receivers which shows the high robustness of the proposed concepts.

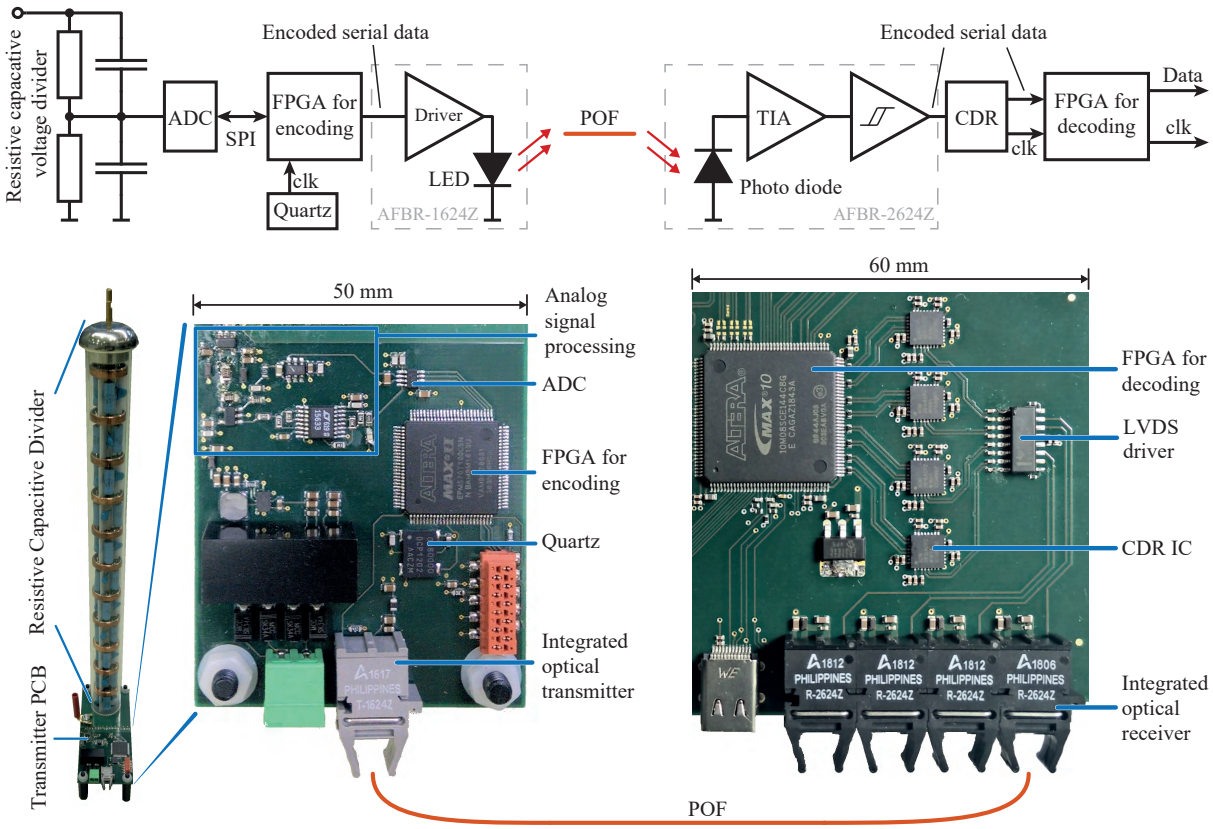


Fig. 10: Top: Simplified schematic of a 8b/10b based transmitter (left) and receiver (right) for a MV voltage divider. Bottom: according PCBs. The receiver PCB implements 4 channels. Each of them occupies a separate CDR IC. For both encoding at the transmitter side and decoding at the receiver side, translation LUTs are implemented on CPLDs/FPGAs. To implement multiple channels per transmitter and POF, time-division multiplexing has to be used. Note, that as pointed out in the schematic, the opto-electronic parts (LED driver, TIA, etc.) are fully integrated (cf Tab. IV). The maximum baud rate of the used optical transmitters/receivers is 50 Mbd.

5 Comparison with existing solutions

Looking at available integrated optical transmitters/receivers, an alternative solution using only a single fiber to transmit clock and data is using 8b/10b encoding together with a dedicated clock and data recovery (CDR) IC to recover the clock at the receiver side. A hardware implementation of both, transmitter and receiver on a PCB is shown in Fig. 10. The transmitter PCB is part of a voltage divider to measure AC and DC voltages in the medium voltage (MV) range.

A major drawback of the 8b/10b based CDR is the necessity of storing Look-up-Tables (LUTs) on the transmitter side to do the encoding. In the shown hardware implementation this is realised with a CPLD/FPGA. If more than one measurement value has to be transmitted, time-division multiplexing has to be added, which causes additional complexity to the transmitter side.

Table III: Comparison of the different receiver concepts.

	Parameter	SC-AR	AC-AR	AC-FR
PCB design	Supplies	3.3 V, 5 V, 12 V	3.3 V, 5 V, 12 V	3.3 V, 12 V
	Area	894 mm^2	831 mm^2	667 mm^2
	Component count	105	98	84
FPGA usage	ADC sampling rate	25 MHz	62.5 MHz	62.5 MHz
	Combinational elements	23	23	23
	Sequential elements	29	30	30
	PLL used	yes	no	no
	Baud rate	25 MBd	10 MBd	10 MBd
	Bit rate @ 2 channels	50 Mbps	20 Mbps	20 Mbps

Apart from this, the encoding is based on the parallel data that has to be sent. Assuming an ADC with a serial interface (as e.g. SPI), the captured value of the divider voltage has to be de-serialized, encoded and serialized again for the transmission, such that a comparably large communication delay results. The delay can be calculated as

$$\Delta T_{\text{comm, CDR}} = \underbrace{N \cdot T_{\text{SPI}}}_{\text{de-serialisation of ADC data}} + \underbrace{(c \cdot N + K) \cdot T_{\text{t}}}_{\text{time-division multiplexing \& serialization}}$$

where T_{SPI} is the SPI clock period of the ADC, N is the number of bits of the ADC, T_{t} is the transmission clock period, c is the number of measurements sharing the fibre with time-division multiplexing (number of channels) and K is the number of bits needed for the encoding (depends on the number of bits that actually has to be sent). Note, that the time required for encoding/decoding within the CPLD is neglected.
With the PAM-DCD modulation scheme presented in [9] and applied in this paper, a simple logic IC (NAND logic) can be used to implement the modulation on the transmitter side, which results in a extremely compact and low complexity solution.
The transmission delay with the used modulation scheme is always lower than for a comparable 8b/10b based CDR system, because there is no need to de-serialize the data from the sensor ADC before transmitting, such that the communication delay is

$$\Delta T_{\text{comm,PAM-DCD}} = N \cdot T_{\text{SPI}},$$

no matter how many channels c are implemented. Therefore, if the physical delay of the LED, the POF and the TIA is neglected, no additional delay results compared to a direct electrical connection to the ADC. All in all, the modulation from [9] is faster by

$$\Delta T_{\text{comm,PAM-DCD}} - \Delta T_{\text{comm,PAM-DCD}} = (c \cdot N + K) \cdot T_{\text{t}},$$

which is particularly large for slow (and therfore cheap) two level LED/Photodiode/TIA combinations or for high number of channels c.

6 Conclusion

In this paper, three concepts for an ADC based optical receiver are presented which are compatible with the PAM-DCD scheme proposed in [9]. The receiver circuits allow the realization of an optical link which is capable of transmitting multiple signals with their clock over a single POF at data rates of 20 - 50 Mbps while maintaining a low BER.
Compared to existing solutions, the proposed concepts provide more flexibility in terms of used levels per symbol and a smaller PCB footprint. Furthermore, no additional coding is necessary for a robust clock recovery at the receiver which results in a lower communication delay than in comparable digital communication interfaces. In time critical applications, this can be a major advantage.

The demodulation of the received data is realized with a low number of logic elements. Therefore, it is possible to implement the receiver logic in FPGAs/CPLDs already existing in the system. Moreover, two of the three proposed concepts do not need an additional PLL for the clock recovery which is often a scarce resource in cost efficient logic programmable logic devices (PLD).

The shown optical communication interface potentially reduces the system size and costs of e.g. a converter system due to the lower number of necessary POFs and components compared to other commonly used communication interfaces.

Table IV: Components used in the 8b/10b based transmitter and receiver prototypes (Fig. 10).

Type	**Part number**	**Manufacturer**
Transmitter LED	AFBR-1624Z	Avago
Encoding FPGA	MAX II	Altera/Intel
Receiver Photodiode & TIA	AFBR-2624Z	Avago
LVDS driver	SN65LVDS391DR	Texas Instruments
CDR IC	ADN2816ACPZ	Analog Devices
Decoding FPGA	MAX10	Altera/Intel

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