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Optimization of Hybrid Current-Injection Circuit Breakers including Mechanical Switch Limitations

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Keywords

≪HVDC≫, ≪Multiterminal HVDC≫

Abstract

Circuit breakers with current injection enable fast interruption of fault currents in DC grids. Independent of the topology, a high number of semiconductors and capacitors is required. The minimum required number of semiconductors and capacitors depend mainly on the system voltage and the maximum fault current. However, also the MS characteristics have considerable influence on the required number of semiconductors and capacitors. Therefore, in this paper the influence of the MS characteristics on the arc extinction and the influence of the arc voltage on the DC-CB design is presented. In addition, optimization procedures for current injection circuit breaker are presented, which include the MS characteristics and four different possibilities to include the arc voltage. Finally, three DC-CB topologies are compared in terms of number of semiconductors and capacitors.

1 Introduction

In recent years, interest in bulk HVDC transmission has significantly increased due to the need for offshore and long distance energy transmission with low losses. Additionally, voltage source converters (VSC) enable a power reversal without the need for a voltage reversal, being a first step to a meshed multi-terminal DC grid with low transmission losses [1].
One of the major remaining problems of HVDC transmission is to turn lines rapidly off, especially in case of a fault in meshed DC grids. Besides turning off the complete DC grid [2], DC circuit breaker (DC-CB) are an attractive solution. Such DC-CB must interrupt a (fault) current in the line, must block an increasing transient interruption voltage (TIV) across the DC-CB, and must dissipate the remaining energy in the line inductances for deenergizing the lines. To interrupt a current and block the TIV, DC-CB can use either mechanical switches (MS), semiconductor switches or in so called hybrid circuit breaker (HCB) a combination of both, which combines the fast interruption of semiconductors with the low on-state losses of MS.

In HCBs, a MS conducts with low conduction losses the current in normal operation and the semiconductors generate a zero current condition (ZCC) in the MS during the interruption in order to generate a fast turn off. The ZCC is generated by injecting a current pulse into the MS in opposite direction of the fault current. Although different current-injection concepts exist, the basic tasks are the same for all of them:

- Generate rapidly a ZCC in the MS
- Limit the $\mathrm{d}v/\mathrm{d}t$ of the voltage across the MS
- Block the same maximum voltage as the MS

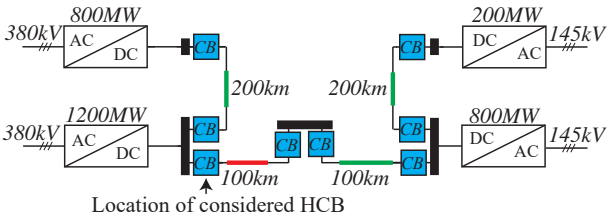

Fig. 1: Exemplary block diagram of a 4-terminal symmetric monopolar DC grid [3] including cables (green) and overhead lines (red), which is used for the optimization of the current-injection DC-CBs.

Of special importance is that the arc in the MS is successfully extinguished and does not reignite. Therefore, the $\mathrm{d}i/\mathrm{d}t$-$\mathrm{d}v/\mathrm{d}t$ characteristic of the MS must be included in the optimization. Additionally, the arc voltage increases the $\mathrm{d}i/\mathrm{d}t$ and should therefore also be included in the optimization of a DCCB. However, both have been neglected in literature so far.
Therefore, this paper shows first that the $\mathrm{d}v/\mathrm{d}t$ and therefore the MS has a strong impact on the minimum required number of semiconductors and the minimum required capacitive energy storage for CI branches in DCCB (section 2). Thereafter, the $\mathrm{d}i/\mathrm{d}t$ -$\mathrm{d}v/\mathrm{d}t$ -characteristic of the MS and different arc voltage models are discussed in section 3. Finally, in section 4.1 and section 4.2 is shown how the MS is included in the optimization for three different topologies . The optimization results are presented in section 4.3.

2 Principle design limits of the CI branch

In this section, the minimum required number of semiconductors and amount of capacitive energy storage for a HCB with CI-branch (Fig.2) are determined. Equations are given for the general case and results are presented for the grid shown in Fig.1.

General operating principle of DC-CB with CI branch

After a fault is detected, the MS in the main current branch is opened while conducting current (Fig.3). This causes an arc, which is extinguished by the CI branch after the MS opening time T_{open}. This is performed by injecting the current I_{CI} into the MS in opposite direction of the fault current. After the current injection time T_{com}, the arc is extinguished and the voltage across the DC-CB increases during $T_{rise,DC}$ to the voltage V_{DC}, respectively during T_{rise} to the maximum TIV $V_{TIV,max}$. Afterwards, the current is commutated to the energy absorber.

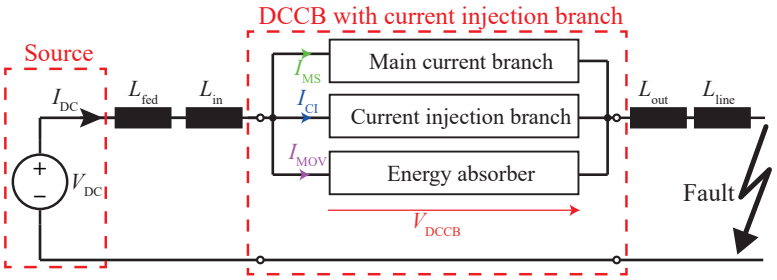

Fig. 2: Simplified model of a HCB with CI branch. The main current branch conducts in normal operation. The CI-branch is used for the turn-off. The energy absorber is used to dissipate the remaining energy in the line inductances after the turn-off.

Minimum required number of semiconductors and amount of capacitive energy storage for the CI branch

The main task of the CI branch is to generate a ZCC with a low $^{di}/_{dt}$ before the ZCC. Additionally, the CI branch must limit the voltage slope of the TIV below the maximum allowed $^{dv}/_{dt}$ to avoid a reignition of the arc and it must block the maximum TIV $V_{TIV,max}$. To block the maximum TIV $V_{TIV,max}$, the CI branch uses semiconductors [4], capacitors (Fig.11) or a combination of both (Fig.13). With these three requirements, it is possible to define a minimum required number of semiconductors and a minimum amount of capacitive energy storage for the CI branch. The minimum required number of semiconductors is described with the minimum installed semiconductor power $P_{s,min} = V_{s,max} I_{s,max}$, respectively with $E_{s,min} = V_{s,max} \int I_s \mathrm{d}t$, where $V_{s,max}$ is the maximum blocking voltage of the semiconductors and $I_{s,max}$ the maximum semiconductor current. The minimum required amount of capacitive energy storage is described with $E_{C,min} = {}^1/_2 C_{min} V_{C,max}^2$, where $V_{C,max}$ is the maximum capacitor voltage.

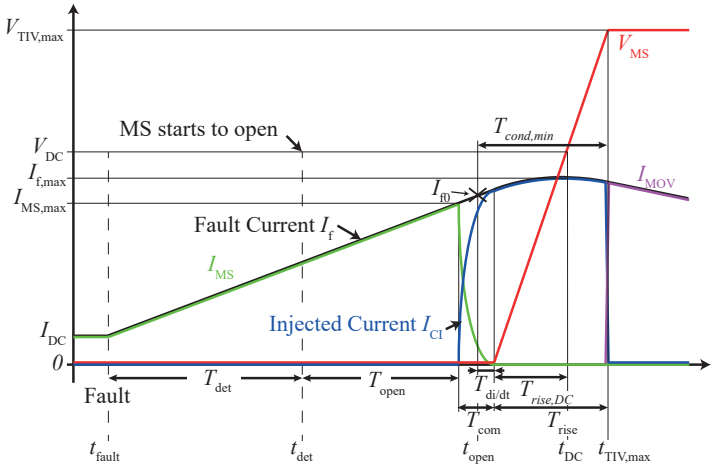

Fig. 3: Basic timeline of a fault current interruption with a DC-CB with CI branch.

The maximum blocking voltage of the semiconductors $V_{s,max}$ can be used as free parameter in the optimization of the CI-branch. Accordingly, the maximum capacitor voltage is $V_{C,max} = V_{TIV,max} - V_{s,max}$ with the common use of $V_{TIV,max} = 1.5 V_{DC}$ [5] to block the maximum TIV $V_{TIV,max}$. The maximum current in the semiconductors $I_{S,max}$ is equal to the maximum fault current $I_{f,max} = I_f(t_{DC})$ at $t_{DC} = t_{open} + {}^{V_{DC}}/_{(dv/dt)}$, where V_{MS} is equal to V_{DC}, and depends on the maximum allowed $^{dv}/_{dt}$ of the MS. The semiconductor current integrated over time $\int I_s \mathrm{d}t$ depends on the conduction time of the CI-branch, which consists of two time intervals. The first time interval T_{com} is the time required for generating the ZCC. During this time, the $^{di}/_{dt}$ must be low for a short period before the ZCC, approximately $T_{di/dt} = 20 \ldots 30 \mu s$ for SF6 [6], in order to allow the arc plasma to cool down. This results ideally in $T_{com} = T_{di/dt}$. In the second time interval T_{rise}, the CI branch limits the $^{dv}/_{dt}$ of the TIV after the arc extinction and therefore conducts the current until the maximum TIV $V_{TIV,max}$ is reached. This results in $\int I_s \mathrm{d}t = \int_{t_{open}-T_{com}}^{t_{open}+T_{rise}} I_f(t) \mathrm{d}t$. The minimum required capacitance C_{min} depends on the maximum allowed $^{dv}/_{dt}$ of the MS and the maximum fault current $I_{f,max}$ with $C_{min} = {}^{I_{f,max}}/_{dv/dt}$. These equations results in the minimum required number of semiconductors and the minimum amount of capacitive energy storage for the CI branch:

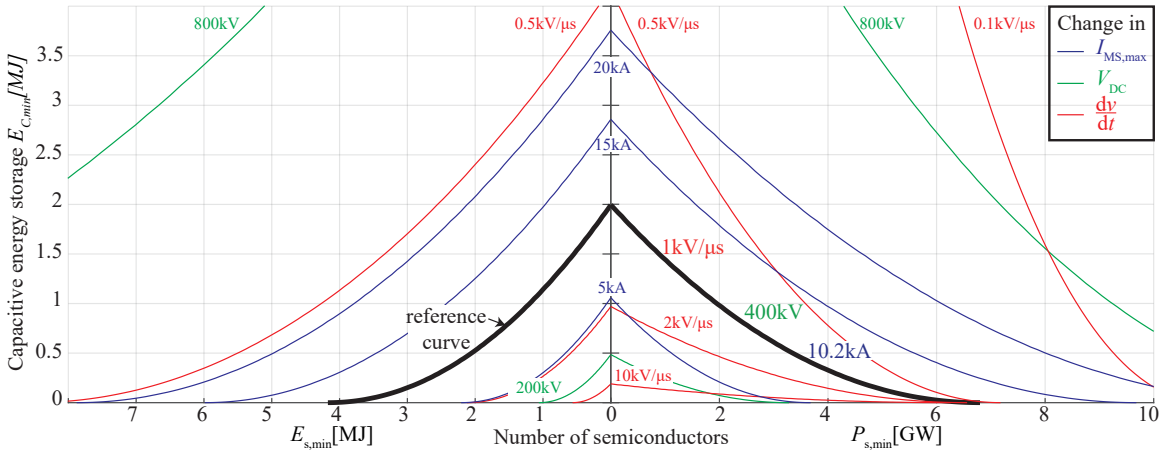

Fig. 4: Pareto fronts for the minimum required amount of capacitive energy storage $E_{C,min}$ and the semiconductor numbers described with P_S and E_S. The black curve shows the pareto front for a DC-CB designed for $I_{MS,max} = 10.2kA$, $V_{DC} = 400kV$ and $dv/dt = 1kV/\mu s$. The other curves show the influence of the DC voltage V_{DC} (green), the maximum MS current $I_{MS,max}$(blue) and the slope of the TIV dv/dt (red). The graph is generated with the generalized equations for the grid shown in Fig.1

$$E_{C,min} = \frac{1}{2} \frac{I_f(t = t_{open} + T_{rise,DC})}{dv/dt} V_{C,max}^2 \quad (1)$$

$$P_{s,min} = V_{s,max} I_f(t = t_{open} + T_{rise,DC}) \quad (2)$$

$$E_{s,min} = V_{s,max} \int_{t_{open}-T_{com}}^{t_{open}+T_{rise}} I_f(t)\mathrm{d}t \quad (3)$$

There exists a trade-off between the minimum required number of semiconductors and the amount of capacitive energy storage for the CI branch as can be seen in Fig.4). The minimum required number of semiconductors and the amount of capacitive energy storage depend heavily on the DC voltage and the maximum MS current, which cannot be changed by the DC-CB except by using a faster MS. However, the allowed dv/dt does not only depend on the MS, but also on the current slope di/dt before the ZCC. This can be utilized to decrease the minimum required number of semiconductors and amount of capacitive energy storage by generating a low di/dt and allowing a relatively high dv/dt, which is shown in section 4.

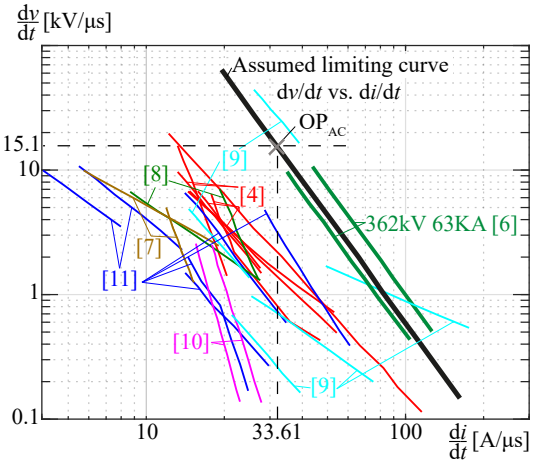

Fig. 5: Maximum allowed voltage slope dv/dt after the arc extinction depending on the current slope di/dt before the arc extinction presented in [6–12]. In black the assumed curve is shown.

Remark: Components for the pulse generation

In addition to the components described in (1)-(3), additional components may be required to generate the current pulse. However, topologies exist, which can generate the pulse current with only the minimum number of semiconductors and amount of capacitive energy storage [13] (see section 4.2). Therefore, the equations actually represent a good approximation of the minimum required number of semiconductors and amount of capacitive energy storage.

3 MS parameters in the optimizations

In this section, the MS parameters in the optimization are described. In section 3.1, the influence of the current slope di/dt before the ZCC and the voltage slope dv/dt after the arc extinction are discussed. In section 3.2, the arc modeling is discussed.

3.1 Current and voltage slope as parameter at the arc extinction

In the previous section, the limits for the di/dt and the dv/dt of the MS during the fault clearing have been assumed to be constant. However, the arc extinction and the probability of a reignition of the arc depends on various parameters as for example the isolation medium, the contact size, the contact material, the contact forms, etc. Additionally, the maximum allowed voltage slope dv/dt after the arc extinction depends also on the current slope di/dt before the ZCC. According to [6], the relationship is approximately $\frac{dv}{dt} \sim \frac{k}{(di/dt)^m}$. A compromise between low di/dt and low dv/dt can be for example used to decrease the minimum required number of semiconductors and the amount of capacitive energy storage by generating a low di/dt before the ZCC and allowing a relatively high dv/dt after the ZCC.

This requires the knowledge about the detailed relationship between $^{di}/_{dt}$ and $^{dv}/_{dt}$. Data about the interruption limits of fast MS for DC current breaking is rare. Therefore, in this paper a combination of AC circuit breaker (AC-CB) interruption behavior and of switching times of available fast MS is assumed.

An AC-CB designed for $63kA$ and $60Hz$ experiences a worst case current slope of $^{di}/_{dt} = \omega\sqrt{2}I_{rms}cos(\omega t) = 33.6A/\mu s$. With the standard surge impedance of lines for short line faults $Z = 450\Omega$, this results in a worst case $^{dv}/_{dt} = Z^{di}/_{dt} = 15.12^{kV}/_{\mu s}$. With those two parameters the operating point OP_{AC} in Fig.5 is defined. The same result can also be obtained by using the rate of rise of recovery voltage (RRRV) factor $0.24^{(kV/\mu s)}/_{kA}$ for rated voltages between $245kV$ and $800kV$ [14].
For the slope of the $^{dv}/_{dt}$-$^{di}/_{dt}$-characteristic, the slope of the $63kA$-CB presented in [7] has been used. With this, the black limiting curve for the $^{dv}/_{dt}$ and the $^{di}/_{dt}$ of the assumed MS in Fig.5 is given.
For the opening time of the CB $1+3ms$ ($T_{sep}+T_{block}$) are assumed, which is relatively fast, but comparable to ultra-fast-disconnectors ($2ms$ [15]) and vacuum-CBs ($2.3ms$ [16]). The assumed MS parameters are summarized in Tab.I.

Table I: Assumed parameters of the MS.

Time to contact separation T_{sep}	$1\ ms$
Time to maximum blocking capability $T_{sep}+T_{block}$	$1\ ms+3\ ms$
Maximum current	$63\ kA$
Maximum blocking voltage	$600\ kV$
Maximum $\frac{di}{dt}$ vs. maximum $\frac{dv}{dt}$	black curve in Fig.5
Assumed $^{dv}/_{dt}$-$^{di}/_{dt}$-characteristic	$dv/dt \sim \frac{2.4}{(di/dt)^{2.85}}$

3.2 Arc voltage during the current injection

Beside the parameters for a successful arc extinction, the arc voltage of the MS is important for the DC-CB design. The arc voltage can be used for excitation of a resonance circuit [20] or can be beneficial for the commutation of the fault current to parallel branches [21, 22]. However, the arc voltage can be disadvantageous for current-injection DC-CB since the arc voltage increases for decreasing currents. This leads to an increased $^{di}/_{dt}$ especially close to the ZCC. Accordingly, the arc voltage must be taken into account in the optimization of the CB. This can be done with different arc models (AM), which strongly influence the time for computing the models:

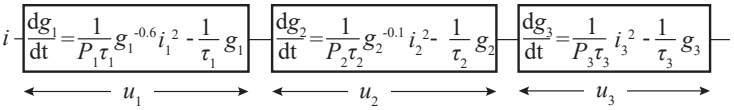

Fig. 6: Composite black box model of an arc, which combines the classical Cassie-model, the Mayr-model and a hybrid model [17–19].

Fig. 7: Assumed arc parameters of the black box model in Fig.6 from [18].

P_1	P_2	P_3	τ_1	τ_2	τ_3
$3178.64\cdot10^6$	$139.61\cdot10^3$	$6345W$	$2.541\mu s$	$0.5082\mu s$	$0.1016\mu s$

AM1: The simplest possibility to include the influence of the arc is to include enough inductance and capacitance in the CI-branch to ensure the low $^{di}/_{dt}$. This can be a feasible possibility for Vacuum Circuit Breaker (VCB), where the arc voltage is relatively low [23]. However, this is not a feasible solution for Gas Circuit Breaker (GCB), where the arc voltage is in the range of a few kilo volt [18].

AM2: A second possibility is to use a physical model of the arc within the optimization, which typically is, however, quite complex and lead to a high computation time [12]. Therefore, this method is not considered in this paper.

AM3: The arc can also be modeled with a so called black box model [18]. Black box models can be used for determining the arc voltage without calculating the physical processes and they correctly describe the interaction between arc and surrounding grid [24, 25]. However, the model parameters depend heavily on the used MS and the operation point during the measurement [17, 18]. Therefore, measurements for the used MS are required to include the MS in the optimization.
Since no data for a SF6 MS for $400kV_{DC}$ is available, scaled up data for a $245kV$ SF6 AC-CB [18] is used in the optimizations in this paper (Tab.7). The used black box model is the composite black box model from [17, 18] (Fig.6). Hereby, the arc voltage is scaled proportional to the system voltage, since the arc voltage is proportionally to the arcing distance [24, 26] and the breakdown voltage

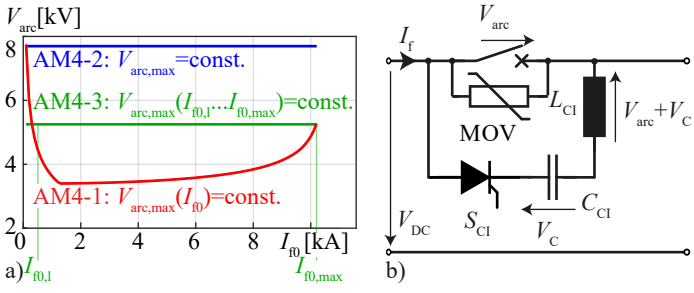

Fig. 8: a) Voltages resulting from the different arc models. AM4-1 uses a maximum arc voltage, which depends on the fault current. AM4-2 uses a maximum arc voltage independent of the fault current. AM4-3 uses a maximum arc voltage independent of the fault current, but uses the maximum arc voltage of AM4-1 in the current range between $I_{f0,l} \approx 500A$ and the maximum fault current $I_{f0,max}$. b) The arc voltage drives with the capacitor voltage the pulse current. Therefore, the arc model has a strong impact on the optimization for low initial capacitor voltages $V_C = V_{C0}$.

is proportional to the arcing distance [27]. However, the parameters depend also on the arcing time, $^{di}/_{dt}$ and the degradation of the contacts [28]. An additional disadvantage is that the model cannot be solved analytically, which also results in a high computation time. The black box model is therefore only used for the optimization in section 4.1.

AM4: A fourth possibility is to use first a minimum arc voltage in the optimization to prove that a ZCC can be generated and then a maximum arc voltage to prove that the $^{di}/_{dt}$ is sufficiently low. The maximum $^{di}/_{dt}$ occurs for the maximum arc voltage, since the arc voltage increases the driving voltage of the pulse current (Fig.8b). The maximum arc voltage is afterwards verified by using the black box model for the solution of the optimization.
In this paper, this method is used in three variants: **AM4-1:** A constant maximum arc voltage $V_{arc,\text{AM4-1}}(I_{f0})$ that depends on the fault current value I_{f0} of the point in time when the MS reaches the maximum contact distance. With arc model AM4-1, the most accurate prediction of the arc voltage results since the maximum arc voltages depends strongly on the fault current I_f. At high fault currents I_f, the $^{di}/_{dt}$ at the ZCC is low and the resulting maximum arc voltage is relatively high (Fig.9). For low fault currents, the arc voltage is relatively high due to the low heating of the arc. **AM4-2:** A constant arc voltage $V_{arc,\text{AM4-2}}$ independent of the fault current is assumed, which is equal to the maximum value of model AM4-1. The arc model is easier to implement, but uses an arc voltage, which is for most fault currents much higher than for arc model AM4-1. **AM4-3:** A constant arc voltage $V_{arc,\text{AM4-3}}$, which uses the maximum arc voltage of AM4-1 in the current range $I_{f0,l} - I_{f0,max}$, where the influence of the $^{di}/_{dt}$, which depends on the arc voltage, is important. The arc model is also easier to implement than AM4-1, but more accurate than AM4-2 . However, the lower limit of the current range $I_{f0,l} - I_{f0,max}$ must be justified as will be done in section 4.3.

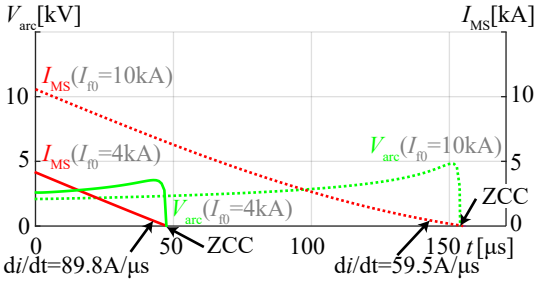

Fig. 9: Arc voltage before the ZCC generated with the black box model (AM3) for a fault current of $4kA$ and $10kA$ ($C_{CI} = 14\mu F$, $L_{CI} = 1.2mH$ and $V_{C0} = 104kV$). The decreasing current leads to a decrease of the conductivity and therefore to higher arc voltages, especially for low current slopes $^{di}/_{dt}$ where the arc has time to cool down (dashed line).

The 4 variants of including the arc voltage in the optimization of the topologies in section 4.1 are shown in Fig.10. For the DC-CB with adapted pulse current in section 4.2 only the constant arc voltage $V_{arc,\text{AM4-3}}$ is used, since a complete optimization with black box model for all cases would result in a long optimization time.
In the following section 4.1, the benefit of including the MS limitations in Tab.I and the arc voltage in the optimization is shown for a simple LC-circuit, while section 4.2 shows the same for a topology specialized for generating a low $^{di}/_{dt}$.

4 DC-CB optimization including MS limitations

In the following section, the optimization of the CI branches shown in Fig.11 and Fig.13 based on the MS limitations given in section 3 is presented. As reference case, the four terminal grid of [3] in Fig.1 is used. The corresponding data for the grid, the used MMCs and the lines are given in Tab.II-IV.

4.1 Optimized current-injection with LC-circuit

The optimization of a CI branch for a fixed amplitude pulse current is presented in this subsection for two variants. In the topology in Fig.11a), the TIV is blocked only by the capacitor, whereas in the topology in Fig.11b) the capacitor and the semiconductors block the TIV together. Accordingly, the energy absorber *MOV* in Fig.11a) is parallel to the CI branch, whereas the *MOV* in Fig.11b) is distributed parallel to the semiconductors and the capacitor in order to limit the maximum voltage across the semiconductors and the capacitor.

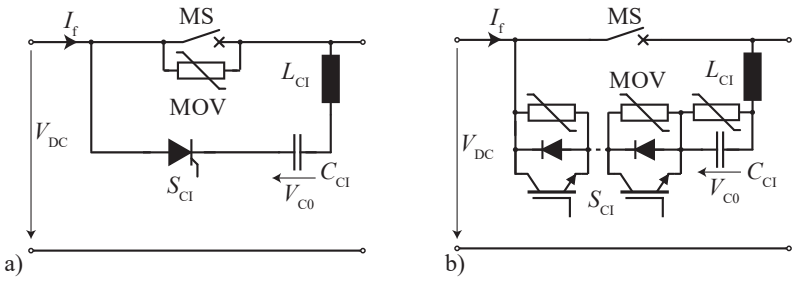

Fig. 11: DC-CB with LC-injection: a) Capacitor C_{CI} blocks the TIV b) The semiconductors and the capacitor C_{CI} block the TIV together.

Operating principle

The operation principle is basically the same for both topologies. In case of a fault, the MS is first completely opened. Then, the semiconductors S_{CI} are turned on and a current with an amplitude higher than that of the worst case fault current is injected in the MS. The slope $^{di}/_{dt}$ of this current is limited by inductor L_{CI}. Once the ZCC

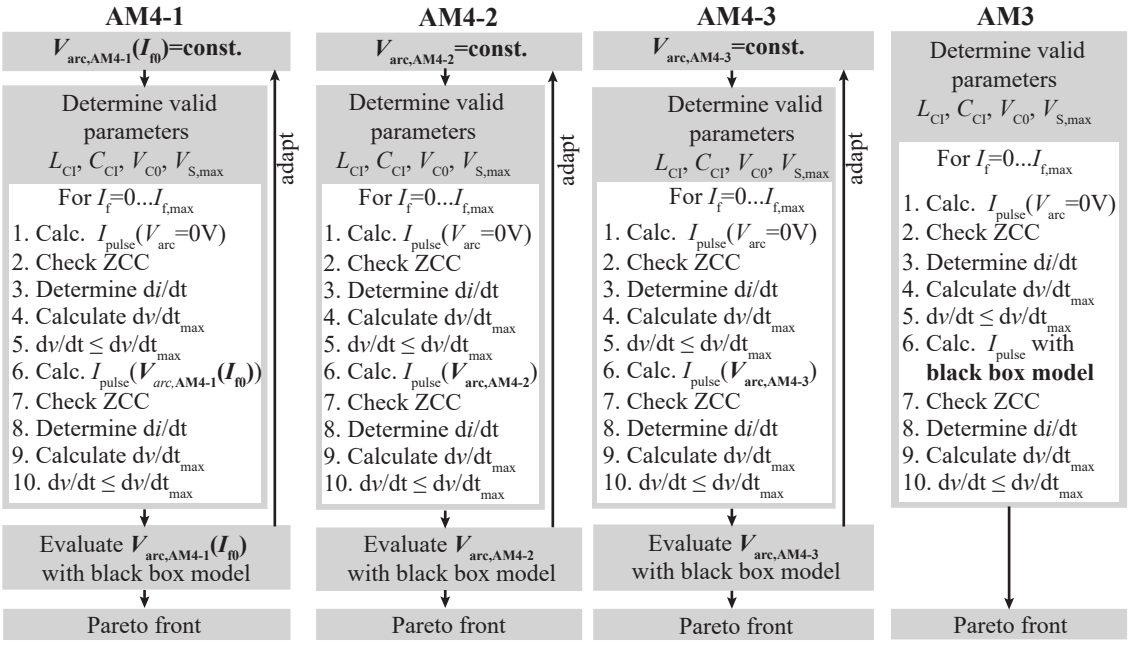

Fig. 10: Four optimization procedures for the topologies shown in Fig.11, which include the arc voltage with four different models. In the procedure with arc model AM4-1, a time-invariant maximum arc voltage is assumed, which depends on the initial fault current I_f. In the procedure with arc model AM4-2, a global constant maximum arc voltage is assumed. Arc model AM4-3 is similar to model AM4-2 but takes only the maximum arc voltage into account, where the $^{di}/_{dt}$ is critical. Arc model AM3 is the black box arc model.

is reached, the arc is extinguished. The fault current is then commutated to the CI branch, where capacitor C_{CI} is charged, which leads to an increasing TIV across the MS. The slope of the voltage across the MS $^{dv}/_{dt}$ is limited by capacitor C_{CI}. With the topology in Fig.11b), the semiconductors can additionally be turned off if a higher $^{dv}/_{dt}$ is possible, respectively are turned off after the capacitor is completely charged. As soon as the maximum TIV is reached, the current is commutated to the energy absorbers MOV, which dissipate the remaining inductive energy of the line.

Optimization methods

In the optimization of the topologies in Fig.11, the aim is to minimize the maximum amount of capacitive energy storage E_C and the minimum required number of semiconductors i. e. P_S and E_S. Both topologies are optimized with the 4 variants for including the arc voltage shown in Fig.10. In the methods AM1-3, a global constant minimum and maximum arc voltage is used. As minimum 0V has been chosen, which is a conservative assumption, which allows to generate a ZCC independent of the arc voltage. The maximum arc voltage is determined iteratively by checking the arc voltage of the solutions with the black box model. In method AM3, the arc is included with the black box model shown in Fig.6 and the parameters in Tab.7. However, also zero arc voltage is assumed as worst case to ensure a ZCC.

Table II: Data of the considered DC grid.

Nominal direct voltage V_{DC}	400 kV
Maximum overvoltage	1.5 PU (600 kV)
Assumed detection time	2.0 ms
Current limiting inductances	$2 \times 60mH$
Maximum MS current $I_{f0,max}$	$10.2kA$

Table III: Parameters of the AC-DC converters (MMCs) [3].

Arm reactor	$L_{arm} = 29mH$
Module on-state resistance	$R_{on} = 1.361m\Omega$
Number of submodules	$n = 200$
Transformer leakage inductance	$X_t = 35mH$
Transformer winding losses	$R_t = 0.363m\Omega$
Short circuit ratio (AC-Grid)	$SCR = 37.5$
Fraction $\frac{X_{ac}}{R_{ac}}$	$\frac{X_{ac}}{R_{ac}} = 10$

Table IV: Parameters of the cable / overhead line (OHL) [3].

		Cable	OHL
Line inductance	L_{line}	2.615 mH/km	0.8273 mH/km
Line resistance	R_{line}	0.011 Ω/km	0.0133 Ω/km
Line capacitance	C_{line}	0.2185 mF/km	0.0139 mF/km

For all variants of including the arc voltage, capacitance C_{LI}, inductance L_{LI}, initial capacitor voltage V_{C0} and maximum semiconductor voltage $V_{S,max}$ are varied. The maximum capacitor voltage results with $V_{C,max} = V_{TIV,max} - V_{s,max}$. The maximum capacitor voltage $V_{C,max}$ and the maximum semiconductor voltage $V_{S,max}$ have, however, a minimum for the topology in Fig.11b), which depends on the initial capacitor voltage V_{C0}. The varistors MOV parallel to the semiconductors and the capacitor have to block the initial voltage V_{C0}, where the varistors MOV should not conduct any current At the maximum TIV, the varistors MOV conduct the maximum fault current. Accordingly, the maximum blocking voltage $V_{S,max}$ and $V_{C,max}$ are due the varistor characteristics at least a factor of approximately $2.2-2.4$ higher than V_{C0} . During the optimization, first the pulse current is calculated and then it is checked if for all fault currents a ZCC exists. Next, the $^{di}/_{dt}$ at the ZCC and resulting maximum allowed $^{dv}/_{dt}$ are calculated for fault currents $I_f = 0...I_{f,max}$. Then, it is checked if the actual $^{dv}/_{dt}$ is below the maximum allowed $^{dv}/_{dt}$. All valid parameter sets are finally used for determining the best parameters.

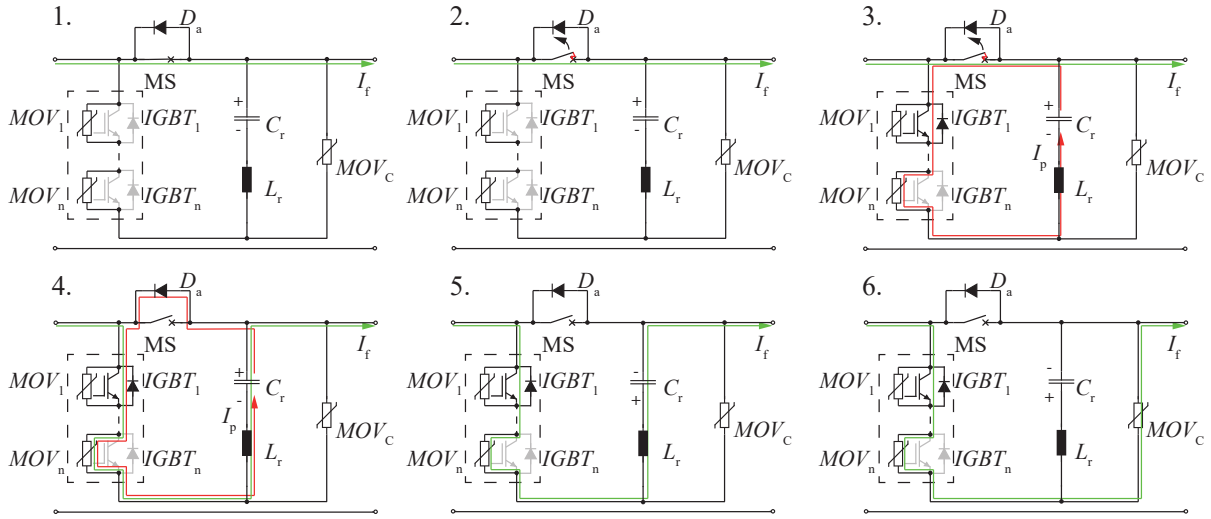

Fig. 12: Operation principle of the HCB-APC divided in 6 steps: 1) Fault detection 2) MS opening 3) Interruption 4) Conduction of diode D_A 5) TIV increase 6) Energy dissipation.

4.2 Current-injection with Adaptable Pulse Current (APC)

In this section, the optimization including the MS limitations for the HCB with adaptable pulse current injection in Fig.13 is presented. Adaptable pulse current means that the number of turned-on semiconductors depends on the fault current and therefore the pulse current amplitude is adapted to the fault current amplitude.

Operating principle

To generate the pulse current, a series connection of a precharged capacitor C_r, an inductor L_r and switching modules (SM) is used [13]. Each SM consists of an IGBT and a parallel varistor.
The turn-off procedure of the HCB in case of a fault is performed in 6 steps (Fig. 12):

- **Fault detection** (Fig. 12-1): First the line current through the MS increases until the fault is detected.
- **MS opening** (Fig. 12-2): After the fault is detected, the MS is opened resulting in an arc. The line current increases further.
- **Interruption** (Fig. 12-3): Shortly before the MS is completely open, a pulse current I_p is generated by turning on a number of IGBTs. The number of turned on IGBTs depends on the fault current I_f. The ideal timing is that the current in the MS becomes zero just when the MS has reached its maximum contact distance / is fully open.
  To generate a low $^{di}/_{dt}$ before the arc extinction, the pulse current is adapted to the fault current. This is achieved by adapting the number of turned on IGBTs depending on the fault current I_f, respectively by adapting the number of MOVs N in the C_rL_r circuit. The general strategy is to increase the pulse current fast at the beginning by including only a small number of MOVs and then to achieve a pulse current with a low $^{di}/_{dt}$ shortly before the peak pulse current by including additional MOVs. The exact control sequence can be found in [29].
- **Conduction of diode** D_A (Fig. 12-4): After the arc is extinguished, diode D_A starts to conduct and prohibits a negative initial transient interruption voltage (ITIV) across the MS until the pulse current becomes lower than the line current.
- **TIV increase** (Fig. 12-5): After diode D_A blocks, the MS prohibits a current in the MS branch and the fault current charges capacitor C_r while the MS regains its full blocking capability. During this and the next step, the TIV across the MS can be influenced by inserting or removing MOVs in the fault current path by turning on or off a few IGBTs. This allows to share the TIV between capacitor C_r and the series connection of IGBTs so that neither of them must be able to block the full TIV.
- **Energy dissipation** (Fig. 12-6): As soon as the voltage across capacitor C_r is high enough to commutate the fault current to MOV_C, the energy of the lines is dissipated in MOV_C and varistors $MOV_1 - MOV_n$ (depending on turned on IGBTs).

Optimization

In the optimization of the DC-CB in Fig.13, the aim is to minimize the maximum amount of capacitive energy storage E_C and the minimum required number of semiconductors. The optimization process is given in Fig.14. First, the parameters of the grid, which influence the interruption must be determined. These are the maximum fault current $I_{f,max}$, the maximum change of the fault current $\Delta I_{f,max}(\Delta t)$ and the energy to dissipate. The maximum change of the fault current $\Delta I_{f,max}(\Delta t)$ is used to determine for which range the pulse current must have a low $^{di}/_{dt}$, since the fault current can change after the fault current measurement while the pulse current rises.

The energy determines in the second step how many MOV are required and hence the voltage current characteristic of a turned-off switching module. In the third step, the parameters of the CI branch are determined. For the optimization the arc voltage is included with method AM4-3. As minimum arc voltage $0V$ is used. The constant maximum arc voltage is iteratively determined by checking the maximum arc voltage of the solutions of the optimization with the black box model and, if necessary, adapting constant maximum arc voltage. In the optimization, the capacitance C_r, the inductance L_r, the initial capacitor voltage V_{C0} and the maximum semiconductor voltage $V_{S,max}$ are varied. The maximum capacitor voltage results with $V_{C,max} = V_{TIV,max} - V_{s,max}$. As the topology in Fig.11b), $V_{C,max}$ and $V_{S,max}$ must be at least a factor of approximately $2.2 - 2.4$ higher than V_{C0} due to the varistor characteristics. Different pulse currents can be generated depending on the time, when the first and the second switching operation takes place (t_1 and t_2) and the number of varistors which are in the pulse current path after the first (N_1) and after the second (N_2) switching operation. In the optimization, the pulse currents are calculated before it is checked if for all fault currents I_f suitable pulse currents can be found. If at a common point of time before the MS is completely open a successful combination t_1, t_2, N_1 and N_2 will be possible for all fault currents, the parameters of the pulse circuit can be used [29]. All valid parameter sets are finally used for determining the best parameters.

4.3 Optimization results

In this section the optimization results of the topologies in Fig.11 and Fig.13 are presented. The pareto front of the number of semiconductors represented by P_S and the maximum amount of capacitive energy storage E_C are shown in Fig.15. E_S is hereby neglected since for these topologies P_S is the limiting value for the semiconductor numbers for 4.5kV-IGBTs and high voltage thyristors.
If no semiconductors are used to block the TIV (Fig.11a), the maximum capacitor voltage is equal to the maximum TIV $V_{TIV,max}$. Therefore, if the maximum required capacitive energy storage E_C should be low, the initial capacitor voltage V_{C0} must be high and the capacitance value low. This high initial capacitor voltage V_{C0} must be blocked by the semiconductors and the low $\mathrm{d}i/\mathrm{d}t$ generated with high inductance values. An additional disadvantage of the high initial capacitor voltage V_{C0} is that the maximum ITIV is also high. On the other hand, low initial capacitor voltages V_{C0} results in low semiconductor numbers.

If semiconductors are used to block the TIV (Fig.11b) and Fig.13), the pareto front has a low initial capacitor voltage V_{C0} for low numbers of semiconductors and for high numbers of semiconductors (e.g. design E and D in Fig.15). Low number of semiconductors are achieved if only a small initial capacitor voltage V_{C0} must be blocked and most of the TIV is blocked by the capacitance. Low maximum amount of capacitive energy storage E_C can be achieved if only a small initial capacitor voltage V_{C0} must be blocked and most of the TIV is blocked by the semiconductors. In both cases, the inductance value is low, but the capacitance value is high. In between those two cases, the TIV distribu-

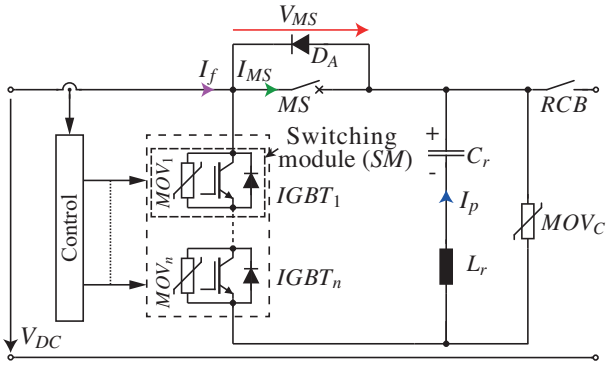

Fig. 13: DC-CB with Adaptable Pulse Current (APC) injection. The series connection of switching modules and capacitor C_r block the TIV.

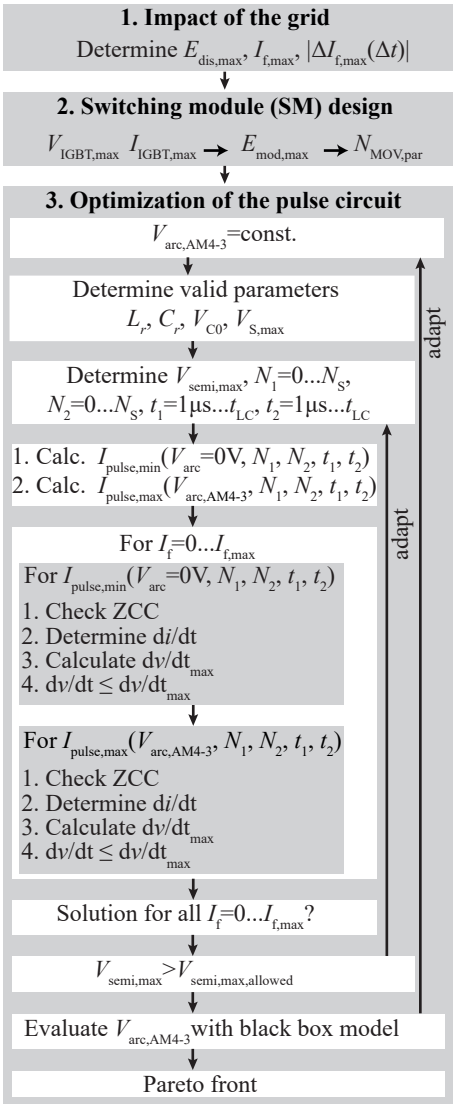

Fig. 14: Optimization of the DC-CB with adaptable pulse current. Compared to the DC-CBs in Fig.11, the influence of the grid on the fault current must be taken into account, since the pulse current is adapted to the fault current. In the optimization, the different pulse currents, which can be generated by changing the turned-off IGBTs, respectively by changing the MOVS in the pulse circuit, are calculated. Different pulse currents can then be used for different measured fault currents.

tion changes from blocking nearly the full TIV with semiconductors to blocking the full voltage with the capacitor. The maximum initial capacitor voltage V_{C0} is reached at $128kV$, when semiconductors and capacitor both block approximately $300kV$, which results from the factor $2.2 \ldots 2.4$ from the MOV characteristic.

In general, the maximum required capacitive energy storage E_C can be substantially decreased with topologies, which block the TIV with a combination of semiconductors and capacitors. For a low capacitive energy storage, this can also be achieved with a lower number of semiconductors. However, due to the fact that the semiconductors with MOV in parallel block only a lower initial capacitor voltage V_{C0}, this is not the case if the topologies in Fig.11b) and Fig.13 block only a small part of the TIV with the semiconductors. The break-even point is approximately at $V_{S,max} = 184kV$ (design B and C in Fig.15).

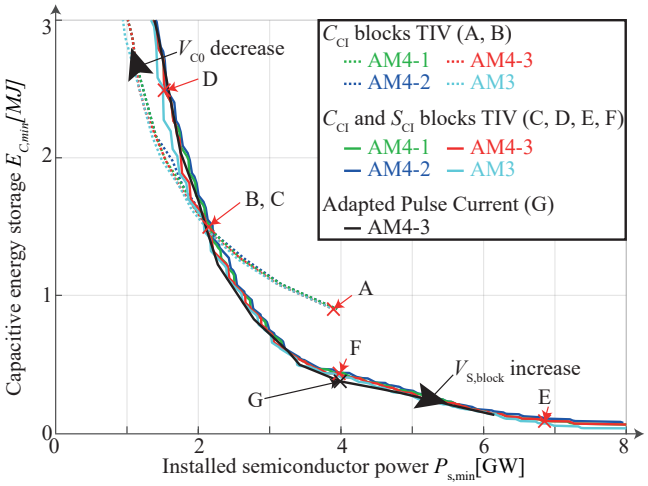

Fig. 15: Pareto front of the CI branches. The topology, where only the capacitor blocks the TIV varies on the pareto front with varying initial capacitor voltage V_{C0}. The topology where the semiconductors and the capacitor block together the TIV and the topology with adapted pulse current vary on the pareto front with the maximum semiconductor blocking voltage $V_{S,block}$. The parameters for the designs A-G are given in Tab.V

For both topologies with single current pulse the $\mathrm{d}i/\mathrm{d}t$ vs. $\mathrm{d}v/\mathrm{d}t$ behavior is as shown in Fig.16. For low currents the $\mathrm{d}i/\mathrm{d}t$ is high, but the $\mathrm{d}v/\mathrm{d}t$ is far below the maximum allowed $\mathrm{d}v/\mathrm{d}t$ since the capacitor is due to the low fault current only slowly charged. For currents close to the maximum fault currents, the $\mathrm{d}i/\mathrm{d}t$ is so low that the resulting maximum allowed $\mathrm{d}v/\mathrm{d}t$ is very high. The critical fault currents are approximately between $6 - 8kA$, where the $\mathrm{d}i/\mathrm{d}t$ of the pulse current is still high and results in a relatively low maximum allowed $\mathrm{d}v/\mathrm{d}t$ but the capacitance is quickly charged due to the high fault current. This is also the fault current range, which is most difficult for the topology with adapted pulse current. In this fault current range the topology can adapt the $\mathrm{d}i/\mathrm{d}t$ only slightly since a ZCC must be still ensured. Therefore, the $\mathrm{d}i/\mathrm{d}t$ can only be slightly decreased and the benefit of adapting the pulse current is relatively low.

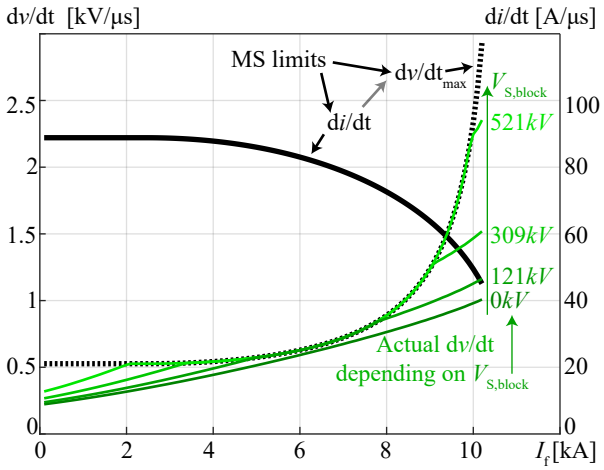

Fig. 16: Current slope $\mathrm{d}i/\mathrm{d}t$ before the ZCC (solid black line) depending on the fault current I_f ($C_{CI} = 11\mu F$, $L_{CI} = 1.5mH$ and $V_{C0} = 128kV$). The maximum allowed $\mathrm{d}v/\mathrm{d}t$ after the ZCC (dashed black line) results from the $\mathrm{d}i/\mathrm{d}t$ and the $\mathrm{d}i/\mathrm{d}t$-$\mathrm{d}v/\mathrm{d}t$-characteristic of the MS (Fig.5). The actual $\mathrm{d}v/\mathrm{d}t$ (green) can be controlled to some degree depending on the maximum blocking voltage of the semiconductors $V_{S,block}$. As can be seen, the actual $\mathrm{d}v/\mathrm{d}t$ is close to the maximum allowed $\mathrm{d}v/\mathrm{d}t$ for $V_{S,block} = 0kV$ between 6 and 8kA. Therefore, this current range defines the minimum required capacitance value of C_{CI}. For currents below 2kA, the maximum allowed $\mathrm{d}v/\mathrm{d}t$ is not reached. Therefore, the increased arc voltage for low currents can be neglected.

Fig.16 additionally shows the effect of the high numbers of semiconductors for blocking the TIV. With a high number of semiconductors for blocking the TIV, the $\mathrm{d}v/\mathrm{d}t$ can be adapted to the maximum allowed $\mathrm{d}v/\mathrm{d}t$ for a wide range of the fault current.

In the following, the impact of the different arc models on the system design is investigated. For high V_{C0}, the impact of the relatively small arc voltage on the pulse current (i.e. the system design) could be neglected (Fig.15). However, for relatively low V_{C0} values the influence of the arc voltage must be considered. While arc model AM4-1 uses a maximum arc voltage, which depends on the fault current I_{f0}, a constant maximum arc voltage of $7796V$ is assumed for arc model AM4-2. Model AM4-3 assumes a arc voltage $V_{arc,\mathrm{AM4\text{-}3}} = 5252V$, which is below the actual maximum arc voltage for low fault currents I_f. However, since the $\mathrm{d}v/\mathrm{d}t$ is below the maximum allowed $\mathrm{d}v/\mathrm{d}t$ for fault currents $I_f < 2kA$, the increased arc voltage for low fault currents can be neglected and the arc model AM4-3 can be used, which results with lower computation times in a pareto front comparable to the pareto front of the black box model.

5 Conclusion

The performance of DC-CB is limited by the performance of the MS and external parameters as the current limiting inductance. The focus of the optimization of DC-CB is on minimizing the number of semiconductors and the amount of capacitive energy storage, which results in minimal costs.

Table V: Corresponding values of the capacitance C_{CI}, the inductance L_{CI}, the initial capacitor voltage V_{C0} and the maximum semiconductor blocking voltage $V_{S,block}$ for the points on the pareto front presented in Fig.15

		A	B	C	D	E	F	G
C_{CI}	$[\mu F]$	5	8	17	23	52	13	12
L_{CI}	$[mH]$	4.5	2.3	0.8	0.6	0.25	1.2	1
V_{C0}	$[kV]$	332	184	76	56	24	104	100
$V_{S,block}$	$[kV]$	0	0	198	125	544	342	350

This paper shows in a first step that for a DC-CB the minimum number of semiconductors and amount of capacitive energy storage depend on the maximum fault current, the system voltage and the operating point of the MS. Therefore, the characteristic of the MS and the arc voltage should be included in the design procedure of the DC-CB, which is shown for three different DC-CB topologies. The first topology generates a pulse current with a fixed amplitude and blocks the TIV only with a capacitor. The second topology generates a pulse current with a fixed amplitude and blocks the TIV with a combination of capacitors and semiconductors. The third topology adapts the pulse current amplitude to the fault current and blocks the TIV with a combination of capacitors and semiconductors. By blocking the TIV with a combination of capacitors and semiconductors, the amount of capacitive energy storage can be decreased up to 50% for the same number of semiconductors. There, the semiconductors must then be able to switch off. By adapting the pulse current amplitude, the amount of capacitive energy storage can be additionally decreased by 7%.

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References

[1] C. Franck, "HVDC Circuit Breakers: A Review Identifying Future Research Needs," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 998–1007, April 2011.

[2] D. Schmitt, Y. Wang, T. Weyh, and R. Marquardt, "DC-side fault current management in extended multiterminal-HVDC-grids," in *9th Int. Multi-Conf. on Systems, Signals and Devices (SSD)*, March 2012.

[3] *Guide for the Development of Models for HVDC Converters in a HVDC Grid*. CIGRE, 2014.

[4] W. Wen, Y. Huang, T. Cheng, S. Gao, Z. Chen, X. Zhang, Z. Yu, R. Zeng, and W. Liu, "Research on a current commutation drive circuit for hybrid dc circuit breaker and its optimisation design," *IET Generation, Transmission Distribution*, vol. 10, no. 13, pp. 3119–3126, 2016.

[5] *Technical requirements and specifications of state-of-the-art HVDC switching equipment*. CIGRE, 2017.

[6] G. Frind, *Experimental Investigation of Limiting Curves for Current Interruption of Gas Blast Breakers*. Boston, MA: Springer US, 1978, pp. 67–94.

[7] K. Arimatsu, Y. Yoshioka, S. Tokuyama, Y. Kato, and K. Hirata, "Development and interrupting tests on 250kV 8kA HVDC circuit breaker," *IEEE Trans. Power App. Syst.*, vol. PAS-104, no. 9, Sept 1985.

[8] S. Tominaga, H. Kuwahara, K. Yoshinaga, and S. Sakuma, "Estimation and performance investigation on slf interrupting ability of puffer-type gas circuit breaker," *IEEE Trans. Power App. Syst.*, vol. PAS-98, no. 1, pp. 261–269, Jan 1979.

[9] S. M. G. Ali, H. M. Ryan, D. Lightle, D. W. Shimmin, S. Taylor, and G. R. Jones, "High power short circuit studies on a commercial 420kV, 60kA puffer circuit breaker," *IEEE Power Eng. Rev.*, vol. PER-5, no. 2, pp. 47–47, Feb 1985.

[10] R. D. Garzon, "Rate of change of voltage and current as functions of pressure and nozzle area in breakers using SF6 in the gas and liquid phases," *IEEE Trans. Power App. Syst.*, vol. 95, no. 5, pp. 1681–1688, Sept 1976.

[11] S. Taylor, G. R. Jones, and S. M. E. Kholy, "Relationship between circuit-breaker performance and nozzle blocking, contact evaporation and particle production," *IEEE Proc. - Sci., Measurement and Technology*, vol. 141, no. 6, pp. 508–512, Nov 1994.

[12] H. Ryan and G. Jones, *SF6 Switchgear*, ser. IEE power engineering series. P. Peregrinus, 1989. [Online]. Available: https://books.google.ch/books?id=aOjrLTYGOz8C

[13] A. Jehle and J. Biela, "Hybrid circuit breaker for HVDC grids with controllable pulse current shape," in *19th Eur. Conf. on Power Electronics and Appl. (EPE ECCE Europe)*, Sept 2017.

[14] D. Dufournet, "Transient recovery voltages (TRVs) for high-voltage circuit breakers part 1," 2013. [Online]. Available: http://www.ewh.ieee.org/soc/pes/switchgear/presentations/tech_pres.html
[15] P. Skarby and U. Steiger, "An ultra-fast disconnecting switch for a hybrid HVDC breaker - a technical breakthrough," *Cigre Symposium, Alberta,Canada*, Sep 2013.
[16] B.-C. Kim, Y.-H. Chung, H.-D. Hwang, and H.-S. Mok, "Development of HVDC circuit breaker with fast interruption speed," in *9th Int. Conf. on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, June 2015, pp. 2844–2848.
[17] H. Urai, Y. Ooshita, M. Koizumi, N. Yaginuma, M. Tsukushi, and R. P. P. Smeets, "Estimation of 80kA short-line fault interrupting capability in an SF6 gas circuit breaker based on arc model calculation," in *17. Int. Conf. on Gas Discharges and Their Appl.*, Sep. 2008, pp. 129–132.
[18] A. Ahmethodzic, M. Kapetanovic, K. Sokolija, R. P. P. Smeets, and V. Kertesz, "Linking a physical arc model with a black box arc model and verification," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 18, no. 4, pp. 1029–1037, August 2011.
[19] H. A. Darwish and N. I. Elkalashy, "Universal arc representation using EMTP," *IEEE Trans. Power Del.*, vol. 20, no. 2, pp. 772–779, April 2005.
[20] B. Pauli, G. Mauthe, E. Ruoss, G. Ecklin, J. Porter, and J. Vithayathil, "Development of a high current HVDC circuit breaker with fast fault clearing capability," *IEEE Trans. Power Del.*, vol. 3, no. 4, pp. 2072–2080, Oct 1988.
[21] W. Faust, "Switching arrangement for disconnecting high-voltage direct-current lines," US Patent 3 651 374, Mar. 21, 1972.
[22] D. Ergin and H.-J. Knaak, "DC voltage switch for switching a short interruption," WO Patent 2 014 117 807, Aug. 7, 2014.
[23] R. P. P. Smeets, E. P. A. van Lanen, M. Popov, and L. van der Sluis, "In search for performance indicators of short-circuit current interruption in vacuum," in *23rd Int. Symp. on Discharges and Electrical Insulation in Vacuum*, vol. 1, Sep. 2008, pp. 79–82.
[24] M. M. Walter, *Switching arcs in passive resonance HVDC circuit breakers*. ETH Zurich, 2013.
[25] M. K. Bucher, *Transient Fault Currents in HVDC VSC Networks During Pole-to-Ground Faults*. ETH Zurich, 2014.
[26] V. V. Terzija and H. . Koglin, "New approach to arc resistance calculation," in *2001 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No.01CH37194)*, vol. 2, Jan 2001, pp. 781–787 vol.2.
[27] A. Küchler, *Hochspannungstechnik: Grundlagen - Technologie - Anwendungen*, ser. VDI-Buch. Springer, 2005. [Online]. Available: https://books.google.ch/books?id=osqLf_MZMr0C
[28] R. P. P. Smeets and V. Kertesz, "Evaluation of high-voltage circuit breaker performance with a validated arc model," *IEE Proc. - Generation, Transmission and Distribution*, vol. 147, Mar 2000.
[29] A. Jehle and J. Biela, "Design procedure and control of a hybrid circuit breaker with adaptable pulse current injection," in *Int. Power Electronics Conf. (IPEC-Niigata 2018 -ECCE Asia)*, May 2018, pp. 1509–1516.