# High Speed, Multi-Channel, Isolated Data Transmission with a Single Fiber based on Intensity Modulation

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# High Speed, Multi-Channel, Isolated Data Transmission with a Single Fiber based on Intensity Modulation

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## Keywords

"Optical Link", "Data Transmission", "Intensity Modulation", "Plastic Optical Fiber"

## Abstract

In modern medium voltage power electronic systems, the need for high bandwidth data transmission, often through optical fibers is growing. In the most common solution multiple fibers are required in order to transmit multiple signals, which increases the overall system cost and its complexity. In this paper, a high-speed (up to 200Mbps) optical link is introduced which enables the transmission of multiple data signals and their respective clock through a single fiber. The method is based on a light intensity modulation technique and transmits a multi-level signal with a single fiber, resulting in a high bandwidth isolated communication link.

## 1 Introduction

In medium voltage converter systems, there is often the requirement to fast measure multiple values (e.g. output voltage/current), for achieving a dynamic control with improved performance [1], [2]. Due to the high operating voltages, the measurement data often needs to be transmitted via optical fibers [3]. The simplest way to transmit digitized measurement data is to use one dedicated fiber per signal, as shown in Fig. 1a. However, apart from the measurement data, the corresponding clock needs to be transmitted for a reliable synchronization at the receiver's end. This leads to a high number of expensive optical links.

One method to eliminate the need for an additional fiber to transfer the clock signal, is to utilize encoding/decoding schemes (e.g. 8bit/10bit Manchester encoding). In this way, the data signal is transmitted along with its respective clock in one bit stream, as shown in Fig. 1b and the clock must be recovered at
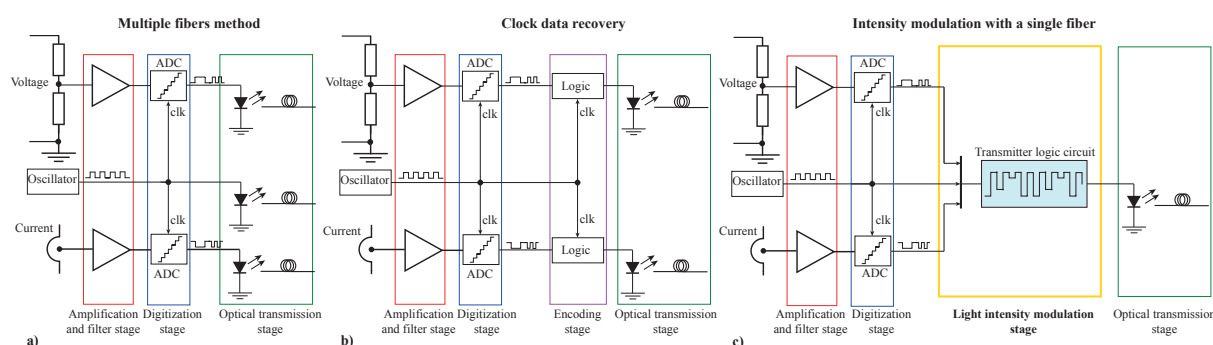


Figure 1: Comparison of optical transmission interfaces for two data streams. a) Multiple fibers method. Two data signals are transmitted by the use of three optical fibers with no bandwidth loss, b) Clock data recovery. The data transmission interface uses an encoding stage in order to transmit the clock signal together with the respective data signal. The method requires one fiber less at the expense of an encoding stage and slightly decreased bandwidth. The method needs a high decoding effort in the receiver's side. c) Intensity modulation with a single fiber. The method transmits two data signals and the respective clock with a single optical fiber without any loss of bandwidth.
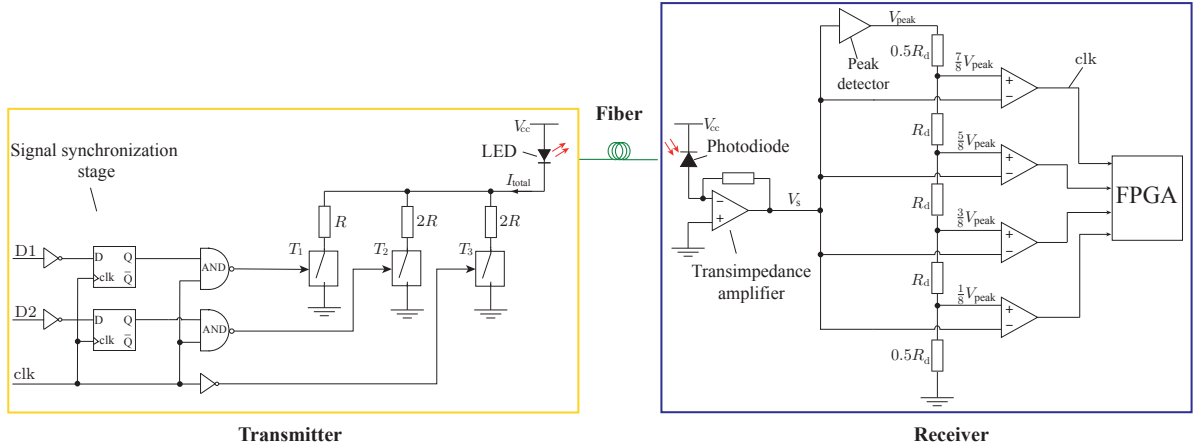
Figure 2: Simplified schematic of the proposed communication interface. The transmitter side consists of a synchronization stage and a logic stage that drives three channels. Each channel is hereby represented for simplicity by an ideal signal controlled switch. The intensity of the total bias current through the LED depends on the combination of the enabled channels that conduct. Five discrete levels of intensity can be generated. The receiver side consists of a photodiode, a transimpedance amplifier, a peak detector, a voltage divider and four comparators.

the receiver's end, using clock recovery techniques. However, this method increases the effort in terms of software/hardware and leads to a bandwidth reduction due to the additional bits used in the encoding stage. Another way to decrease the number of optical links is by using time-division multiplexing, to transmit more than one data signal into a single bit stream. This method is demonstrated in [4], where the authors transmitted two digital signals along with their respective clock signal with the use of two optical links. However, this method results in a 50% bandwidth reduction and is therefore more suitable in applications that do not require a high transmission bandwidth.

On the other hand, intensity modulation and direct detection (IM-DD) is used in optical communication systems [5]. This method results in an increasing bit rate capacity of a given optical fiber link, a decreasing system cost and complexity and an increasing reliability [6]. In principle, the transmitted signal consists of several voltage levels. Each voltage level represents more than one data bit, allowing for a higher bandwidth at the expense of a reduction in the signal-to-noise ratio (SNR). In [7], the benefits of multilevel optical transmission over POF have been demonstrated. In [8] multi-level signals with different wavelengths were generated and transmitted through a single line, achieving high bandwidth. However, due to the need for additional hardware, the cost and complexity of the method is increased. Likewise, in [9] a multi-level signal is generated on the transmitter side which contains several data streams and which is transmitted via the optic fiber to the receiver. Nevertheless, the physical limitations of the optical data transmission in terms of bandwidth with light-emitting-diodes (LEDs) and photodiodes have been widely reported in the literature [10]. In order to overcome the speed limitations, dedicated drive circuits have been employed showing data rates that surpass 100Mbps [11], [12].

In this paper, a simple implementation of the intensity modulation-direct detection optical interface system is proposed, in order to transmit multiple measurement signals (voltage and current) along with their clock via a single fiber (cf. Fig. 1c) [13]. In section 2, the operating principle of the proposed interface and its underlying logic is explained. Furthermore, the limitations of the system in terms of its static and transient performance are demonstrated and further adaptations to the initial principle are proposed in order to ensure the usability of the data transmission link under any conditions. Additionally, several driving methods for the LED and the photodiode are combined for improving the link's performance. In section 3, details regarding the modeling of the components of the system are given and the concept is validated with detailed SPICE simulations. Finally, section 4 summarizes the main outcomes of the paper.

Table I: Truth table for the proposed transmitter circuit and the resulting levels of the current amplitude.

| clk | D1 | D2 | | $T_1$ | $T_2$ | $T_3$ | | $I_{total}$ |
|-----|----|----|----|-------|-------|-------|----|-------------|
| 0 | x | x | $\rightarrow$ | 1 | 1 | 1 | $\rightarrow$ | $I_{peak}$ |
| 1 | 1 | 1 | $\rightarrow$ | 1 | 1 | 0 | $\rightarrow$ | $0.75 \cdot I_{peak}$ |
| 1 | 1 | 0 | $\rightarrow$ | 1 | 0 | 0 | $\rightarrow$ | $0.5 \cdot I_{peak}$ |
| 1 | 0 | 1 | $\rightarrow$ | 0 | 1 | 0 | $\rightarrow$ | $0.25 \cdot I_{peak}$ |
| 1 | 0 | 0 | $\rightarrow$ | 0 | 0 | 0 | $\rightarrow$ | 0 |

## 2 Basic Concept

### 2.1 Transmitter Side

The simplified schematic of the proposed optical link for two data channels is shown in Fig. 2. The transmitter side consists of discrete logic gates that drive three channels. For simplicity, the channels are represented in Fig. 2 by ideal signal controlled switches that are connected through resistors to the cathode of a Light Emitting Diode (LED). When the logical signal is "1" the switch is conducting and there is current flow in the channel. When the logical signal is "0" the switch is blocking and there is no current flow in the channel. The current amplitude at the cathode of the LED is the sum of the currents in the three channels and clearly depends on the status of the logic gates. The intensity of the light (optical output power) produced by the LED is then defined by the combination of channels that conduct. The truth table of the transmitter circuit is depicted in Table I, where the different combinations of the three signals are mapped into a unique current intensity amplitude. It should be highlighted that the level $I_{peak}$ represents the clock signal. The circuit is designed so that the peak current level $I_{peak}$, appears in every clock cycle regardless of the status of the data signals. As shown in Fig. 3, as soon as the clock becomes 0 the signal through the LED returns to its peak value and therefore the clock can be recovered.

The ideal operation principle of the transmitter circuit is shown in Fig. 3, where the clock signal (clk), the data signals (D1/D2) and the total current through the LED ($I_{total}$) are depicted. The data signals are synchronized with the rising edge of the clock, with the use of D flip-flops shown in Fig. 2. The current through the LED is then generating a light signal through the optic fiber, as shown in Fig. 4 (i.e. light intensity) [14].
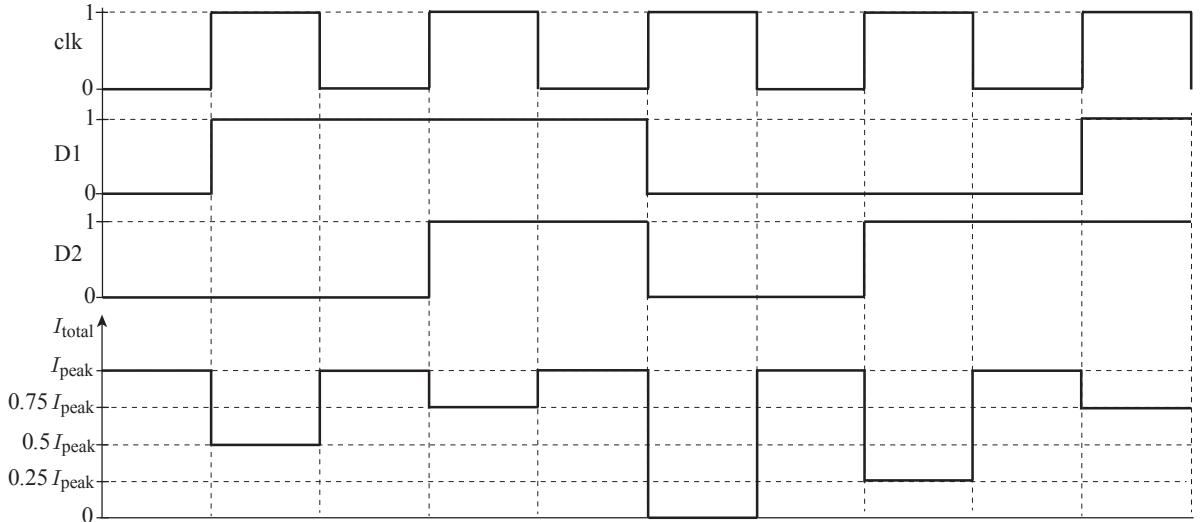


Figure 3: Ideal operation of the transmitter circuit. The different combinations of clock and data signals result in a unique current amplitude level in the LED, according to Table I. The data signals are synchronized with the clock signal and they change status only at the rising edges of the clock signal. The synchronization can be implemented with flip-flops but this stage is omitted for simplicity.
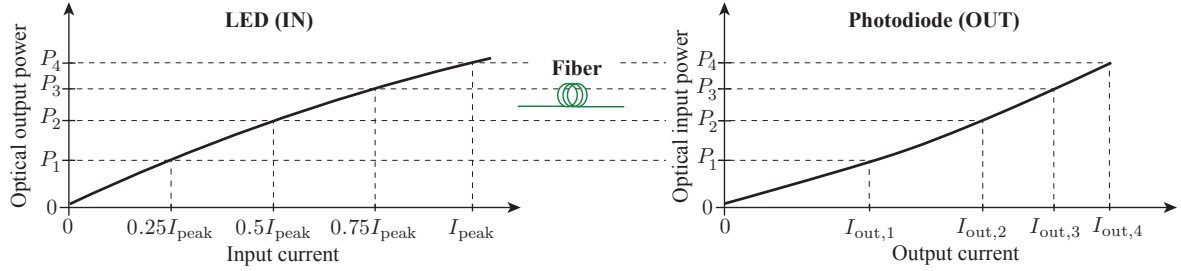
Figure 4: Exemplary operation principle of the LED (IN) and the photodiode (OUT). The relation between the input and output current is approximately linear.

## 2.2 Detailed transmitter side circuit

In LED-based optical communication systems, achieving high bit rates can be rather challenging due to the physical limitations of the diode itself. These limitations arise on the one hand due to the recombination of the carriers and on the other hand due to the diode's diffusion capacitance [11]. In order to decrease the rise and fall times of the LED, suitable drive circuits have been proposed [10]. The schematic of the drive circuit used in this work can be seen in Fig. 5a and the equivalent circuit of a single channel in Fig. 5b. When the logic gate's output is high, the channel acts as a source and the current $I_{ch}$ is positive. On the contrary, when the logic gate's output is low, the channel acts as a sink and the LED's current $I_{LED}$ is increased.

In Fig. 5, a current peaking stage follows the logic stage, where high output current, high bandwidth logic gates are used. The current peaking stage is formed by the parallel combination of resistor $R_{i,1}$ and capacitor $C_i$. The value of the capacitor is determined empirically by measurements of the performance of the transmitter. In general, a higher capacitance leads to a faster response, due to the higher overshoot of the current, as can be depicted in Fig. 6. However, a high capacitance value leads to increased oscillations during the transmission and eventually degrades the signal quality at the receiver's end. In the end, a compromise between performance and signal quality has to be made. Based on the performed measurements, the highest value of $C_i$, that does not lead to an overshoot at the receiver's end is chosen and the measurement of its transient response is shown in Fig. 6 for a single channel. Using a capacitor $C_i = 22\text{pF}$ leads to a significant decrease in both the rise and the fall times of the signal at the receiver's end. It must be noted, that the combination of the transmission through the optical fiber and the photodiode acts as a low-pass filter, attenuating the overshoot of the current at the transmitter's side and therefore the signal quality is not degraded at the receiver's end, as can be seen in Fig. 6b where the output voltage of the photodiode is shown.

Additionally, in order to improve the performance of the LED, a pre-bias current is applied, simply by plac-



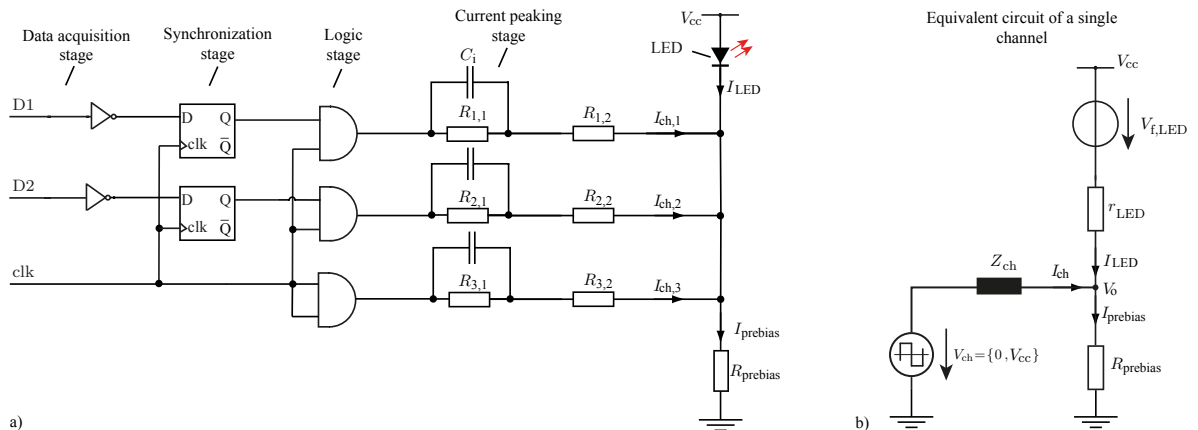Figure 5: a) Schematic of the proposed transmitter circuit. A pre-bias resistor ($R_{prebias}$) is used in order to improve the transient performance of the circuit. Also, a current peaking capacitor $C_i$ is included in every channel. The current peaking capacitor greatly improves the transient performance of the transmitter, as shown in Fig. 6. b) Equivalent circuit of a single channel of the transmitter circuit.
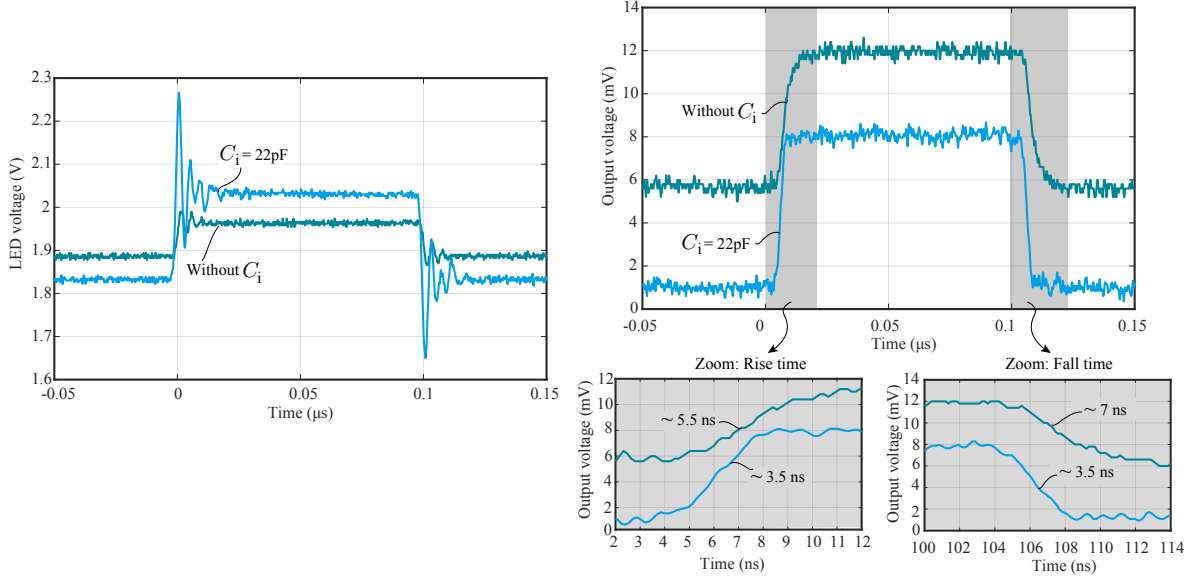
Figure 6: Comparative transmitter circuit measurements of the circuit in Fig. 5, without the current peaking capacitor and with a current peaking capacitor $C_i = 22\text{pF}$ a) Output voltage across the LED. It is evident that the inclusion of capacitor $C_i$ leads to a significant overshoot in the LED voltage. b) Output voltage of the photodiode measured across a $50\Omega$ shunt resistor. It can be noted that the inclusion of capacitor $C_i$ leads to a 40% decrease in the rise time and 50% decrease in the fall time for the part number used. The overshoot of the LED voltage is attenuated by the fiber/receiver circuit.

ing a pre-bias resistor $R_{\text{prebias}}$. The value of the pre-bias current is experimentally tuned with the appropriate $R_{\text{prebias}}$. Moreover, the sum of resistors $R_{i,1}$ and $R_{i,2}$ is determined by the necessary current level. A rule of thumb suggests to assign 2/3 of the total resistance of each channel to the $R_{i,1}$ and 1/3 of it to $R_{i,2}$ [15]. The total resistance of each channel is determined based on the desired current levels and the equivalent circuit shown in Fig. 5b. It is important to note that due to the non-linearity of the current to output light intensity curve, shown in Fig. 4, the total resistances of each channel might have to be adjusted, according to the characteristics of the optical transmitter-receiver combination.

## 2.3 Receiver Side

The main component at the receiver side is the photodiode that absorbs photons and generates a current ($I_{\text{out}}$) that is proportional to the absorbed optical power, as shown in Fig. 4 [16]. The current amplitude generated is usually a few µA and a transimpedance amplifier (current to voltage converter) is used in order to amplify and convert it into a voltage signal $V_s$, as shown in Fig. 2. The multi-level signal $V_s$ is fed to a peak detector [17], which automatically adapts the highest level of the voltage (corresponding to the $I_{\text{peak}}$ level at the transmitter side). It is worth noting that the peak level occurs in every clock cycle regardless of



Figure 7: Receiver side logic. The different possible outputs of the comparators are shown. The FPGA takes this input and maps it into the corresponding level.

the data signals, allowing the detecting circuit to automatically adapt the different voltage levels, based on the detected $V_{\text{peak}}$. In this way, the circuit can compensate for variations of the light intensity at the receiver side due to changes in temperature, different fiber length or component tolerances. The reference voltage levels of the comparators are generated using the output of the peak detector $V_{\text{peak}}$ and a voltage divider.
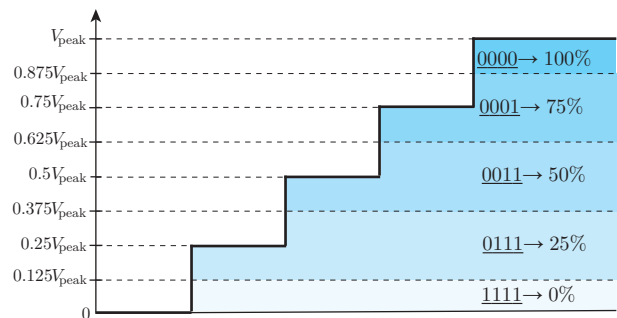
Then, the output signals of the comparators are fed to an FPGA which maps it into the corresponding combination of clock and data signals, as shown in Fig. 7. For example, any voltage signal between $0.125V_{peak}$ and $0.375V_{peak}$ is mapped to the binary number 0111, where the most significant bit is the output of the first comparator. This corresponds to $0.25I_{peak}$ which maps to D1 low and D2 high (Table I).

## 2.4 Detailed receiver side circuit

The schematic of the proposed circuit, shown in Fig. 8, consists of two gain stages that provide the amplification for processing the received signal. The structure of separated stages is used because it allows to operate the amplifiers at a lower gain in order to achieve a higher bandwidth.

The photodiode is operated in photoconductive mode by applying a reverse bias voltage $V_{bias}$. The reverse bias greatly improves the performance of the photodiode since it reduces its junction capacitance and improves its linearity, at the expense of slightly higher dark and noise currents [18]. In order to get the optimum transient response, the highest reverse bias that can be sustained by the photodiode is supplied across its terminals. Furthermore, a bootstrap circuit is employed to further improve the transient performance of the diode. The bootstrap configuration reduces the effective input capacitance of OP1 and allows the use of a smaller feedback capacitance $C_f$ which effectively increases the bandwidth of the circuit [19]. The capacitor $C_{AC}$ allows to bias the photodiode and the JFET separately and therefore use a high reverse bias to further reduce the photodiode's junction capacitance and increase its performance.

The photocurrent is subsequently converted to a voltage by a transimpedance amplifier (TIA) with a gain that is set by feedback resistor $R_f$. A critical component in the circuit design is feedback capacitor $C_f$ which is required to stabilize the circuit and compensate the phase lag introduced by the capacitive load on the inverting input of the operational amplifier and the feedback resistor [20]. The values of $C_f$ and $R_f$ are selected based on the gain and bandwidth requirements of the application.

In order to prevent saturation effects, operational amplifier OP1 is biased at a potential $V_{ref}$ with sufficient voltage difference to the negative rail. This reference voltage is applied to the subsequent differential to single-ended voltage amplifier forming a pseudo-differential circuit, that improves the signal integrity. Additionally, $V_{ref}$ is also applied to the anode of the photodiode, as shown in Fig. 8. Thus, the static reverse voltage of the photodiode is effectively increased.

For the generation of the threshold voltages, an active peak detector circuit is employed as illustrated in Fig. 2. The operational amplifier OP3 compensate the forward voltage drop of Schottky diode $D_1$ and the input peak voltage is stored in capacitor $C_{peak}$. To react on temporarily changing peak voltages due to changing conditions, a bleeding resistor $R_{bleed}$ is added in parallel. In order to improve the transient
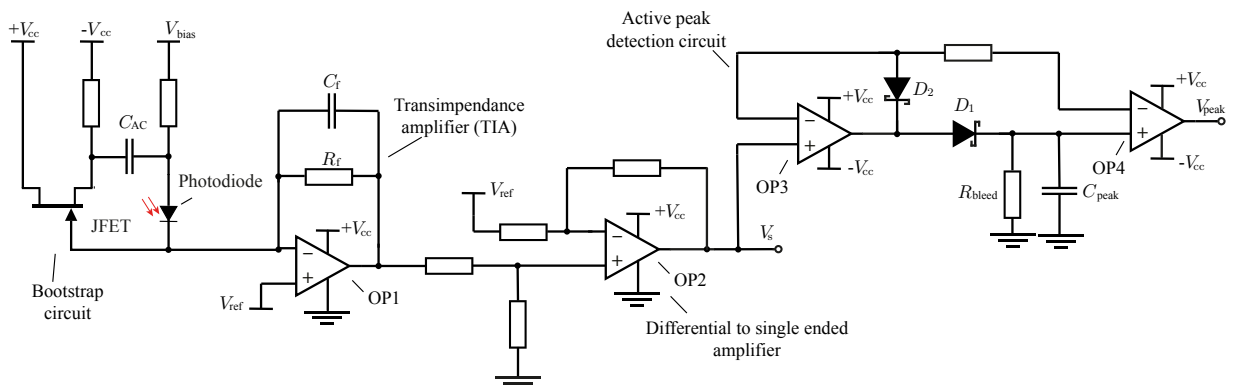


Figure 8: Schematic of the receiver circuit. A bootstrap circuit is employed for increasing the performance of the photodiode, along with a reverse bias voltage. A pseudo-differential signal is generated in order to increase the signal's quality. The schematic of the active peak detection circuit is also visible. The diode $D_1$ and the capacitor $C_{peak}$ are playing an important role in the performance of the peak detection. Four different supply voltages are noted on the schematic. $+V_{cc}$ and $-V_{cc}$ are the supply voltages of the active components (typ. 5V), $V_{ref}$ is the offset voltage for the single ended to pseudo differential conversion (typ. 2.5V) and $V_{bias}$ is the reverse bias of the photodiode (typ. -24V).

Table II: Components used in SPICE simulations

| Type | Part Number | Manufacturer | Spice Model |
|---|---|---|---|
| Transmitter | IF-E99B | Industrial Fiber Optics | Not available |
| Receiver | SF250 | Avago/Broadcom | Not available |
| Op-amp (TIA) | LTC6268-10 | Analog Devices | Available |
| Op-amp (peak detector) | OPA659 | Texas Instruments | Available |
| Comparators | MAX9602 | Maxim Integrated | Available |
| JFET | CPH3910 | ON Semiconductor | Available |
| Schottky Diodes | BAS40 | Infineon | Available |
| AND Gates | CD74ACT08 | Texas Instruments | Available |

response of the peak detector, the second Schottky diode $D_2$ is added in the feedback path. This diode clamps the output of the operational amplifier and therefore prevents saturation at the negative rail. The minimum width of a pulse that the peak detector can accurately detect is mainly determined by the slew rate and the maximum output current of operational amplifier OP3, capacitor $C_{peak}$ as well as the reverse recovery time of Schottky diode $D_1$. The latter has a significant effect on the performance when operated at high speeds because the reverse recovery current of the Schottky diode increases for higher $di/dt$ and can exceed the normal forward rated current of the diode [21]. Therefore, for this application Schottky diodes with particularly low reverse recovery times are chosen.

Moreover, additional buffer and filter stages can be added to the circuit path in order to improve the signal integrity, but are not shown here for simplicity. Finally, the multi-level signal $V_s$ passes through the comparator stage and gets sampled by the FPGA, as shown in Fig. 2. The proposed modulation scheme significantly facilitates the clock and data recovery and consequently the complexity of the digital data-path is reduced.

## 3 Modeling and Simulation Results

In this section, the operation of the proposed interface is validated with SPICE simulations with non-ideal components. With these detailed SPICE models, the maximum achievable bandwidth of the proposed communication interface is investigated. The circuit components used in the simulations are listed in Table II where the availability of spice models provided by the manufacturer is also shown.

Due to the unavailability of the manufacturer's SPICE models for the LED and the photodiode, suitable behavioral models that capture the main characteristics of these components are utilized. The models used in the SPICE simulations for the LED and the photodiode are shown in Fig. 9. The static I-V characteristic of the LED is modeled with the Shockley equation to fit the data provided by the manufacturer [22] and its transient performance is modelled by the inclusion of the parallel junction capacitance $C_j$.

In order to capture the non-linear behavior of the optical communication link, the relation between input current (LED current) and output current (receiver current) for the chosen transmitter-receiver pair is mod-



Table III: Model parameters

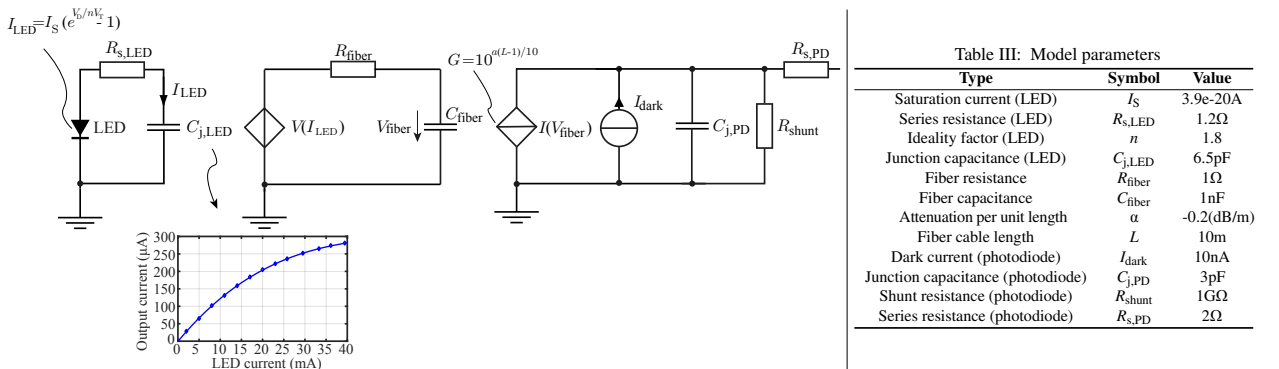| Type | Symbol | Value |
|---|---|---|
| Saturation current (LED) | $I_S$ | 3.9e-20A |
| Series resistance (LED) | $R_{s,LED}$ | 1.2Ω |
| Ideality factor (LED) | $n$ | 1.8 |
| Junction capacitance (LED) | $C_{j,LED}$ | 6.5pF |
| Fiber resistance | $R_{fiber}$ | 1Ω |
| Fiber capacitance | $C_{fiber}$ | 1nF |
| Attenuation per unit length | α | -0.2(dB/m) |
| Fiber cable length | $L$ | 10m |
| Dark current (photodiode) | $I_{dark}$ | 10nA |
| Junction capacitance (photodiode) | $C_{j,PD}$ | 3pF |
| Shunt resistance (photodiode) | $R_{shunt}$ | 1GΩ |
| Series resistance (photodiode) | $R_{s,PD}$ | 2Ω |

Figure 9: Behavioral models for SPICE simulation of the optical link. The LED, the fiber cable and the photodiode are modeled and their parameters are shown in Table III. Note: The circular shape is used for independent sources while the rhombus shape is used for dependent sources.

eled with a current dependent voltage source as shown in Fig. 9. The characteristic was measured for the particular pair and the result is shown also in Fig. 9. Moreover, the fiber acts as a low pass filter with a certain bandwidth that is usually defined by the manufacturer. This behavior is modelled with the $R_{fiber}C_{fiber}$ combination.

The voltage across the capacitor is then fed to the voltage-dependent current source $I_{PD}$ which represents the photodiode. The gain $G$ of the dependent current source $I_{PD}$ represents the attenuation introduced in the optical fiber and is a function of the fiber's length, as can be seen in Fig. 9. Furthermore, the parallel current source $I_{dark}$ models the photodiode's dark current, resistor $R_s$ represents its equivalent series resistance and resistor $R_j$ its shunt junction resistance under zero bias conditions. Capacitor $C_{j,PD}$ models the transient behavior of the photodiode according to the manufacturer's data-sheet.

Fig. 10 shows the result of the detailed SPICE simulation of the proposed optical communication link. The transmitted signals clk, D1 and D2 are depicted and the transmission frequency is 100MHz in this case, which corresponds to a rate of 200Mbps. With this rate, the data of a 12-bit ADC could be transferred with a 8MSps sampling frequency for two data channels simultaneously.

Moreover, Fig. 10 shows current $I_{LED}$ through the LED. As expected $I_{LED}$ has 5 discrete amplitude levels that correspond to 5 different voltage levels of the multi-level signal $V_s$ at the output of the transimpedance amplifier. In Fig. 10, the effect of the current peaking is also visible in the waveform of $I_{LED}$, which appears to have a slight overshoot during the transients. The received signal $V_s$ is clearly distorted compared to the ideal one shown in Fig. 3, due to the finite rise/fall times of the simulated components. The circuit automatically detects the peak level $V_{peak}$ and adjusts the reference values of the comparators accordingly.
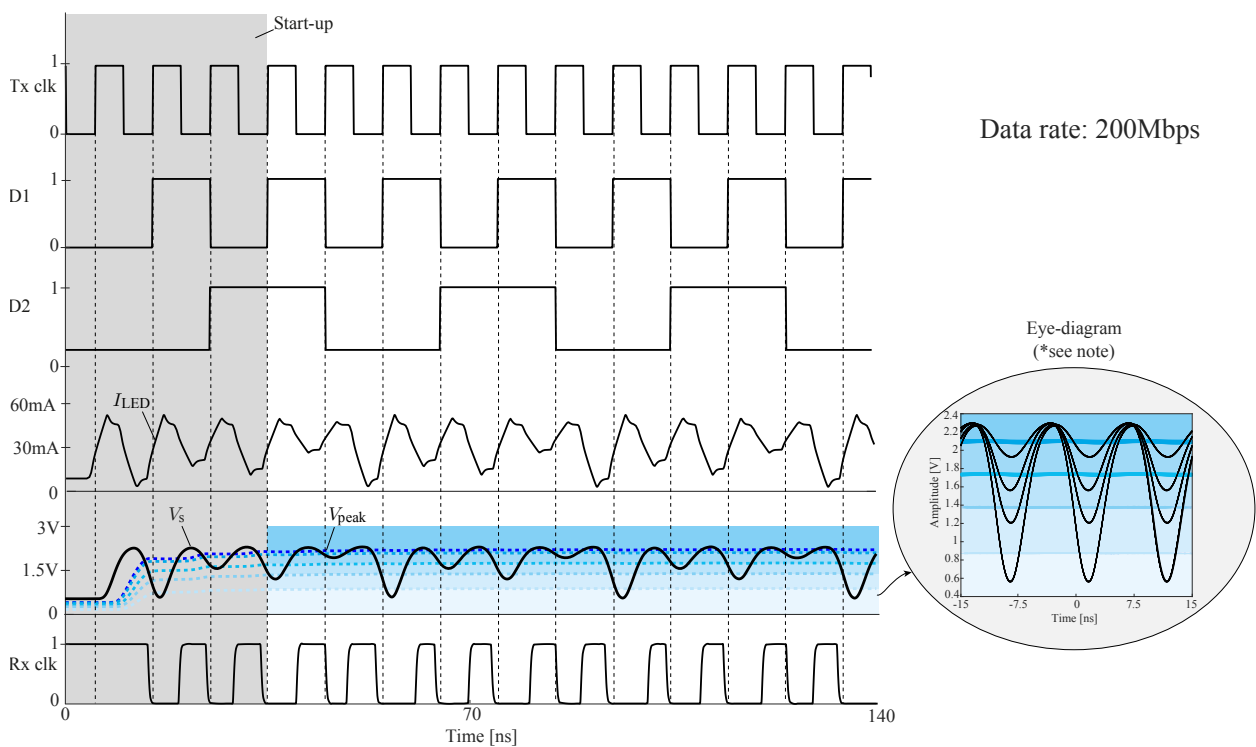


Figure 10: SPICE simulation of the proposed communication interface with SPICE-modeled components. The output signal has a rate of 200MBps and corresponds to approximately 8MSps sampling frequency with a conventional 12-bit ADC. The current $I_{LED}$ through the LED is shown and the effect of the current peaking circuit is also evident. The output voltage of the transimpedance amplifier $V_s$ along with the different voltage reference levels of the comparators and the output voltage of the peak detector $V_{peak}$ can also be depicted. Furthermore, the received clock is found, verifying the accurate transmission of the necessary information. Sidenote: Due to the modulation, every transition is between the peak level and the respective lower level, which is the reason that the eye-diagram does not look like a common eye-diagram.
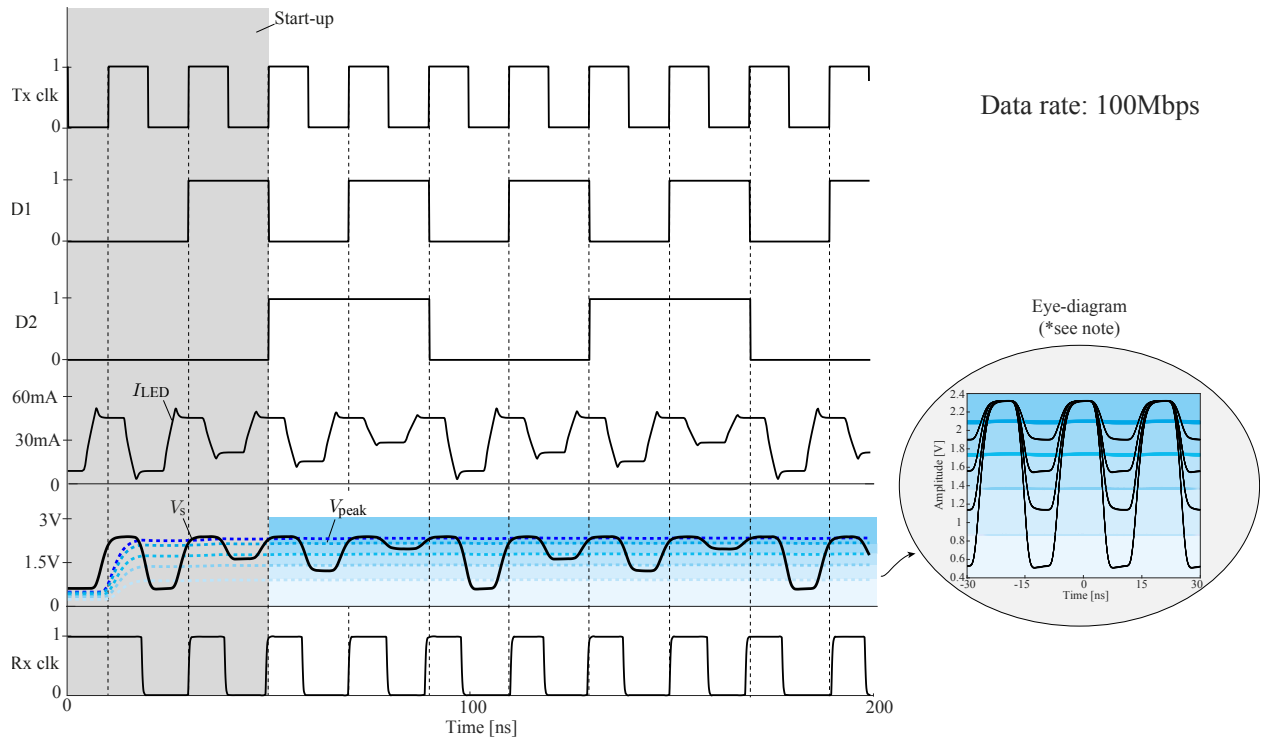
Figure 11: SPICE simulation of the proposed communication interface with SPICE-modeled components. The output signal has a rate of 100Mbps and corresponds to approximately 4MSps sampling frequency with a 12-bit ADC. Sidenote: Due to the modulation, every transition is between the peak level and the respective lower level, which is the reason that the eye-diagram does not look like a common eye-diagram.

It must be noted that due to the non-linearity of the transmitter-receiver pair that was simulated, the values of resistors $R_{i,1}$ and $R_{i,2}$ were slightly modified in order to allow enough margin for the level detection and therefore, the voltage levels at the comparators are not symmetrical, as opposed to the ideally symmetrical case discussed in Fig. 7.

Despite the inevitable signal distortion, the multi-level signal $V_s$ manages to transfer the necessary information, as can be seen in the waveform of the received clock. The received clock has the same frequency as the transmitted clock following an initial start-up transient, which lasts for approximately 4 clock cycles, until the peak detector settles to a steady state peak value of $V_{peak}$.

Fig. 11, shows the result of the detailed SPICE simulation of the proposed optical communication link with a data rate of 100Mbps. It is evident that the multi-level signal $V_s$ is less distorted in this case compared to the 200MBps transmission. This corresponds to a sampling frequency of 4MSps for a 12-bit ADC, which is still a sufficient sampling frequency for most of the power electronics related applications.

## 4  Conclusion

This paper presents an optical link suitable for an isolated, high speed multi-channel data transmission. Initially, the basic operating principle of the multi-level signaling method is described. Moreover, the transmitter and receiver circuits are described in detail and particular attention is paid to the crucial components, limiting the maximum bandwidth and accuracy. Furthermore, detailed SPICE simulations are performed, including non-ideal components and detailed models of the LED, photodiode and the optical fiber. The simulations show that the circuit can operate with a bit rate up to 200Mbps, which corresponds to a clock frequency of 100MHz and a sampling frequency above 8MSps using 12-bit ADCs. All in all, the paper demonstrates the ability of the interface to transmit up to three signals with a single optical fiber, eliminating the need for additional expensive optical fibers or encoding/decoding schemes that increase the complexity of the interface and reduce its bandwidth.

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