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Highly Accurate Virtual Dynamic Characterization of Discrete SiC Power Devices

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***Abstract*—Optimized low-inductive layouting of the package interconnections and external PCBs and bus-bars are necessary to benefit from Silicon Carbide (SiC) power devices, which allow inherently very fast switching transitions. In this paper, a comprehensive modeling procedure for highly accurate virtual dynamic characterization of discrete SiC power devices is described taking into account the 3D geometry of the internal and external interconnections of package as input. The modeling requirements are discussed on an example of a commercial 1.2 kV, 80 mΩ SiC Power MOSFET in a standard TO-247 package (Cree C2M0080120D). The software tools, Simplorer, Saber, Q3D and LTSpice, commonly used for modeling and simulation of power modules, are evaluated with respect to their modeling capabilities for SiC devices.**

I. Introduction

For the design of full SiC power modules, the parasitic inductances and capacitances of the package layout have to be significantly reduced when comparing to the standard packages used for Silicon power devices. In the course of developing new packaging technologies, together with electro-thermal modeling as e.g. presented in [1], a computationally efficient and accurate modeling of interconnections for predicting Electromagnetic (EM) behavior of SiC power semiconductor packages increases in importance. The software tools, based on different numerical techniques, are typically used for the estimation of these parasitics in the frequency-domain. The dynamic characterization of semiconductor devices is a time-domain analysis and the transformation of the frequency-dependent elements to a time-domain simulation is a challenging task [2]. Moreover, authors frequently report only the commutation (power) loop inductance omitting the information on the frequency, and/or the consideration of mutual inductive and capacitive couplings. Accordingly, taking into account all these challenges, this paper presents a comprehensive modeling of dynamic performance of a discrete SiC power MOSFET based on the state-of-the-art modeling tools commercially available.

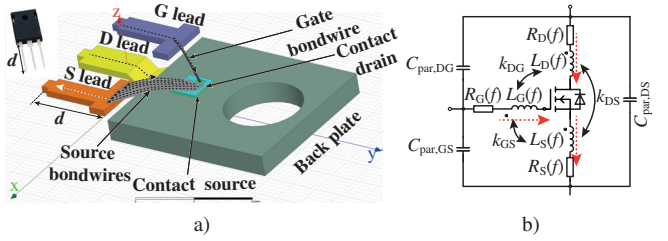
II. EM modeling using ANSYS Q3D

The parasitics of a power module's interconnects have a significant influence on its dynamic performance, together with the semiconductor device capacitances. The EM modeling including the estimation of over-voltages, current ringing, and current sharing between paralleled devices is not only useful for optimizing the dynamic performance but also for improving reliability. A very accurate way to extract parasitics is three-dimensional (3D) modeling of the package geometry based on different numerical techniques like the Finite Element Method (FEM) and the Boundary Element Method (BEM).

A. Extraction of Parasitics using ANSYS Q3D

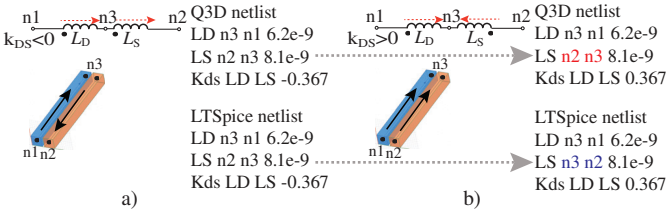
In this section, we investigate the capabilities of the ANSYS Q3D Extractor, a state-of-the-art software tool frequently used in engineering practice for extracting the parasitics of power electronics components and systems. The basic modeling block in Q3D is a net consisting of electrically connected conductors. Each net contains one sink port ($sink$) and one or multiple source ports ($source_i$, $i = 1...N$). The partial inductance and resistance of every current path defined between $source_i$ and $sink$ is calculated in the defined frequency range. Q3D treats nets as equipotential and "infinity" as ground, which implies that the self-capacitance is placed between the net and the ground and the mutual-capacitances are between the net and other nearby nets. This means that there is no capacitive coupling between $source_i$ and $sink$ in the same net. Accordingly, Q3D can be used to estimate the capacitive coupling between two nets, but it lacks to model the high frequency (HF) capacitive behavior of a net, e.g. the parasitic HF capacitance of a wire cannot be modelled by Q3D.

Due to the skin and proximity effects, the resistance of a conductor increases with frequency and the inductance shows a decreasing trend [3]. With tendency to minimize the stray inductances of full SiC power module packages below 30 nH [4], there is a need to model the stray inductances of power module's interconnects with a very high accuracy and the difference between DC and AC inductance [5] must be taken into account. For low frequencies (referred to as DC range), Q3D employs a volume based FEM mesh assuming the current distribution at the full cross section of conductors, i.e. $d \ll \delta$, where d is the minimum conductor thickness and δ is the skin-depth. For high frequencies (referred to as AC range), a surface (BEM) mesh is used, assuming that the current flows only on the conductor surface, i.e. $d \gg \delta$. Furthermore, the computational core of Q3D requires a frequency sweep from a very low ($f < f_{\mathrm{DC}}$) up to a very high ($f > f_{\mathrm{AC}}$) frequency in order to accurately estimate the partial inductances and resistances at the specific mid-frequency ($f_{\mathrm{DC}} < f < f_{\mathrm{AC}}$), when d is of the same order as δ. As it is verified in this



a) b)

Fig. 1: EM modeling of a TO-247 package: a) a photo of C2M0080120D and its Q3D model, and b) the equivalent lumped circuit including the parasitic capacitances ($C_{\mathrm{par,DS}}$, $C_{\mathrm{par,GS}}$, $C_{\mathrm{par,DG}}$), the frequency-dependent inductances (L_{D}, L_{S} and L_{G}) and resistances (R_{D}, R_{S}, and R_{G}) and the mutual inductive couplings (k_{DS}, k_{DG}, k_{GS}).



a) b)

Fig. 2: Equivalent lumped circuit of a current loop and its LTSpice and Q3D netlists with a) neg. coupling and b) pos. coupling.

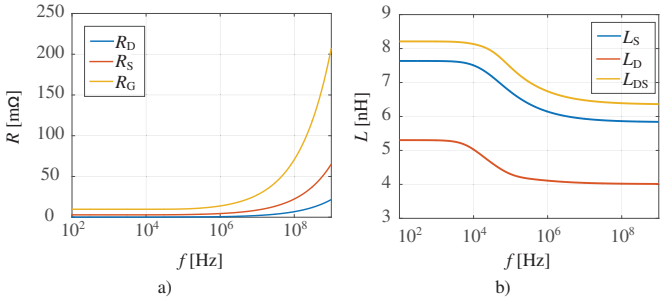
paper, ANSYS Q3D can be used to accurately estimate the inductances and resistances of power modules in the frequency domain. Modeling of parasitics using Q3D in literature was not always precise. For example, in [6], it is stated that the modeling in Q3D should be performed at each frequency separately instead of using the frequency sweep mode, which could lead to inaccurate estimation of AC inductance.

B. Circuit-Electromagnetic Coupled Modeling

With the values of the parasitic inductances, capacitances and resistances obtained from Q3D, an equivalent lumped circuit of the modelled 3D conductor structure can be built and simulated together with the power semiconductor devices in circuit simulators such as Linear Technology LTSpice, Synopsys Saber or ANSYS Simplorer. The Q3D model of a standard TO-247 package and an equivalent lumped circuit of the package with the mutual capacitances connected between the package terminals are shown in Fig. 1a and 1b, respectively.

Q3D can automatically generate a Spice netlist of the equivalent circuit, which has a form of T-sections as shown in [2]. When analyzing this netlist, it can be observed that it does not contain the full information on the signs of mutual inductive couplings, and hence, it has to be modified to be correctly used in a circuit solver, as illustrated in Fig. 2. The Q3D netlist does not represent the current direction correctly as it keeps the same node sequence for both positive and negative coupling.

Another challenge of the circuit-electromagnetic modeling approach is to specify the frequency of interest for which an equivalent lumped circuit is generated, for example, the switching frequency is used in [7], and the critical frequency associated to the device fall time in [8]. During the switching transients of SiC devices, the interconnects and the external conductors of the power module conduct the current pulses



a) b)

Fig. 3: The frequency-dependent inductance of TO-247 package interconnections calculated in Q3D: a) the partial resistances of drain, source and gate nets, and b) the partial inductances of drain and source nets, L_{D} and L_{S} respectively and the drain-source loop inductance ($L_{\mathrm{DS}} = L_{\mathrm{D}} + L_{\mathrm{S}} + 2M_{\mathrm{DS}}$, $M_{\mathrm{DS}} = k_{\mathrm{DS}}\sqrt{L_{\mathrm{D}}L_{\mathrm{S}}}$, $k_{\mathrm{DS}} < 0$) for $d = 5\,\mathrm{mm}$.

with very fast rise/fall time, $t_{\mathrm{r}}/t_{\mathrm{f}}$, of approximately 10 ns to 50 ns. Using the rule of thumb for relating the bandwidth of the signal with its rise time [9], the fast response of SiC devices defines the equivalent modeling frequency for the switching transients in the range of several MHz to 35 MHz. For this frequency range, the parasitic inductances of the TO-247 package asymptotically approach their AC values, as it can be seen in Fig. 3b.

It should be emphasized that ANSYS provides automatic coupling between the electric and electromagnetic domains in Simplorer. In particular, a 3D model of power module package from Q3D can be exported to Simplorer as an equivalent circuit or as a state-space model [10]. The state-space model preserves the frequency dependent values of the parasitic parameters and the problem of selecting the right modeling frequency as previously described can be skipped. However, the accuracy of this modeling approach fully depends on the simulation capabilities of Simplorer for modeling SiC power devices. The accuracy of the Simplorer simulations is presented in the next section in comparison to two other circuit simulators, LTSpice and Saber.

III. Comparison of Circuit Simulators

Virtual dynamic characterization of power semiconductor modules strongly depends on the accuracy of power device models implemented in the circuit simulator. In this section, three commercial circuit simulators LTSpice, Simplorer (v18), and Saber (v2016.3), are analyzed from the aspect of modeling SiC Power MOSFETs using a simple Double Pulse Test (DPT) circuit configuration shown in Fig. 4a with a SiC power MOSFET (Cree C2M0080120D) as Device Under Test (DUT) and a SiC Schottky diode (C4D20120D) as the freewheeling diode.

LTSpice uses compact models of SiC power devices provided by the device manufacturer, while Simplorer and Saber use behavioral power device models, which are parametrized via the characterization tools implemented in these circuit simulators. The characterization tool in Simplorer takes as input the device static ($I_{\mathrm{DS}}(V_{\mathrm{DS}})$, $I_{\mathrm{DS}}(V_{\mathrm{GS}})$) and dynamic ($E_{\mathrm{ON}}$, E_{OFF}, t_{ON}, t_{OFF}) characteristics from datasheets or measurements and automatically parametrizes the internal behavioral power MOSFET model to fit the given waveforms

and values [11]. On the other hand, Saber offers more freedom in setting up the parameters of the behavioral device model, taking the static characteristics and the MOSFET capacitance curves as input. The results are furthermore compared with the Sentaurus TCAD mix-mode simulation as reference, which is based on numerical modeling of the physical MOSFET structure using the C2M0080120D model from [12] and a compact LTSpice model of the diode. TCAD mix-mode simulations can provide very accurate results, however, they are computationally intensive and typically used for the analysis of smaller circuits.

The turn off waveforms, $I_{\mathrm{DS}}(t)$ and $V_{\mathrm{DS}}(t)$, are presented in Fig. 4b to show the differences between the device models. It can be observed that there is a relatively good matching between the waveforms from LTSpice, Saber and TCAD, where the Saber curves demonstrate a higher time delay and the oscillations with a higher amplitude than LTSpice. The waveforms from Simplorer show a significant deviation from TCAD simulation curves, which can be attributed to the model parametrization procedure resulting in inaccurate fitting the given static MOSFET characteristics. Here, it should be noted that the LTSpice compact model of the MOSFET includes three resistances (R_{add}, see Fig. 4a) in parallel to the parasitic package inductances providing necessary damping. The manufacturer set $R_{\mathrm{add}} = 10\,\Omega$, however, by varying R_{add} in the range from $1\,\Omega$ to $20\,\Omega$, we observed that smaller values of R_{add} provided better matching with the TCAD results and with the measurements as presented in the next section. The similar effect of R_{add} is observed also in the Saber simulations. Accordingly, at the current stage, LTSpice and Saber can be used potentially for virtual dynamic characterization of SiC power modules, however, the available LTSpice and Saber models for power SiC devices should be further improved in order to perform simulations in a more defined and accurate way.

IV. Virtual Dynamic Characterization

A virtual dynamic characterization of the discrete SiC Power MOSFET, Cree C2M0080120D (DUT), is performed based on the Q3D electromagnetic modeling of the TO-247 package and the PCB layout of the DPT test circuit [13] used for measuring the dynamic performance of the SiC MOSFET. A Cree SiC power diode, C4D10120D ($\mathrm{D}_{\mathrm{DUT}}$), is used as the freewheeling diode. The measurements are performed at the temperature of $T = 25\,^{\circ}\mathrm{C}$. A simplified circuit model of the measurement setup and the Q3D model of the PCB layout are shown in Fig. 6a and 6b, respectively.

To reduce the complexity of the equivalent lumped circuit representing the HF behavior of the package and the PCB layout, the dominant parasitic parameters have to be determined [14]. In the first approximation, the mutual resistances, the mutual inductive couplings with a coupling coefficient below 0.1, and the mutual capacitances below $1\,\mathrm{pH}$ calculated by Q3D are neglected. The mutual capacitances are connected between the sinks of nets instead of using the T-section circuit model. In the next step, this simplified equivalent circuit is included into LTSpice for a complete circuit simulation. The parasitics used in the circuit simulator correspond to the values extracted in Q3D at the frequency of $20\,\mathrm{MHz}$ that can be associated with a pulse rise time of approximately $17.5\,\mathrm{ns}$. LTSpice was the first choice for the circuit simulator in this case, as the LTSpice compact device models are available and frequently used in engineering practice. The dynamic performance was measured with the vertical mounting of the MOSFET onto the PCB for two lengths of MOSFET terminals: $d = 5\,\mathrm{mm}$ and $10\,\mathrm{mm}$ (see Fig. 1a). The current was measured using a T&M TTSDN current shunt (SSDN-414-05) inserting an inductance of $1.4\,\mathrm{nH}$ in the commutation loop. The proposed modeling procedure is verified comparing the simulated and measured current and voltage switching waveforms, $V_{\mathrm{DS}}(t)$, $V_{\mathrm{GS}}(t)$, and $I_{\mathrm{S}}(t)$. It should be emphasized that a signal pulse generator with a rise time of $300\,\mathrm{ps}$ was used to measure the time delays between the current and voltage probes in order to calculate the switching energies from the measured current and voltage waveforms with a very high accuracy. A good matching between the measured and simulated switching waveforms is achieved and shown in Fig. 5 for the test experiment with $d = 5\,\mathrm{mm}$. The comparison between the measured and simulated switching energies, E_{ON} and E_{OFF}, is presented in Table I. The relative error of less than $10\,\%$ is achieved in all experiments. Accordingly, the presented modeling approach, neglecting the small mutual inductive and capacitive couplings, can be used to predict the switching transients of a discrete SiC Power MOSFET with a very high accuracy. Furthermore, an equivalent circuit of the measurement setup without the parasitic capacitances calculated in Q3D is simulated to illustrate the importance of modeling both inductive and capacitive effects. By removing the capacitive effects the modeling error is significantly increased as shown Table I. An analysis of the mutual parasitic capacitances of the PCB layout shows that the electric field coupling between the signal line (L), the power line (HV), and the GND line, c.f. Fig. 6, has a negative influence on the switching performance, and hence, it has to be optimized.

V. Conclusion

This paper presents a highly accurate virtual dynamic characterization of a discrete SiC power MOSFET analyzing the capabilities of three commercial circuit simulators. Moreover, a way of extracting package parasitics using the well-known ANSYS Q3D tool is described in detail, providing a useful information about influential modeling aspects. Therefore, the results of this paper can be used as a guideline for a very accurate dynamic characterization of SiC power modules by means of circuit-electromagnetic coupled modeling.

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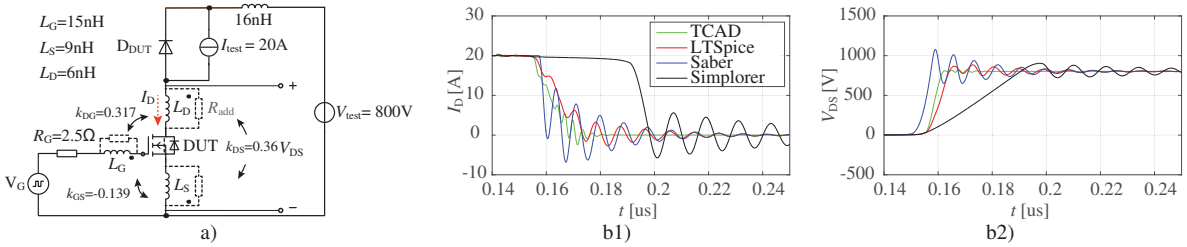

Fig. 4: Comparison between the circuit simulations, LTSpice, Saber, Simplorer, and TCAD mix-mode: a) the DPT circuit configuration, and b) the simulated turn-off waveforms, $I_{\mathrm{DS}}(t)$ and $V_{\mathrm{DS}}(t)$ (at $T = 25\,^{\circ}\mathrm{C}$).

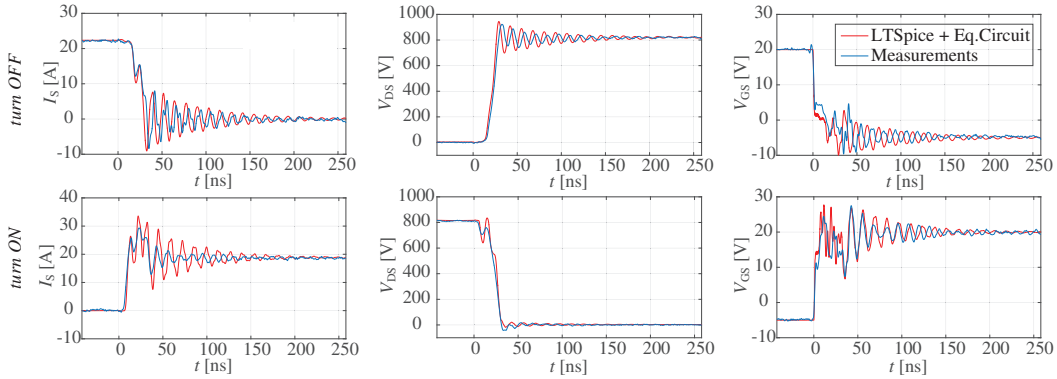

Fig. 5: Comparison between the measurement and the LTSpice simulation ($R_{\mathrm{add}} = 5\,\Omega$) of the turn on and off switching waveforms for $d = 5\,\mathrm{mm}$.

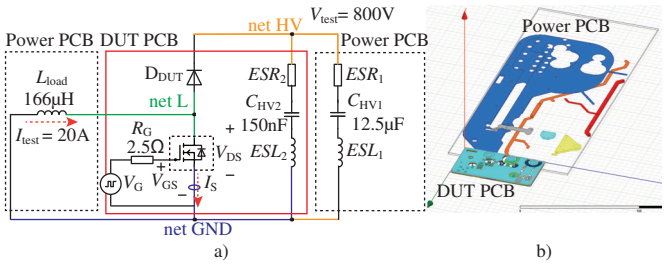

Fig. 6: DPT test circuit used for the verification: a) the simplified circuit implemented in LTSpice for the simulation of switching transients, and b) Q3D model of the external PCBs layout. The gate voltage $V_{\mathrm{G}} = -5\,\mathrm{V}/20\,\mathrm{V}$. DUT is tested for the blocking voltage of 800 V and the current of 20 A. $ESL_{1,2}$ and $ESR_{1,2}$ are the self-parasitics of the high voltage capacitors C_{HV1} and C_{HV2}.

TABLE I: Measurements and simulation results for turn on, E_{ON}, and turn off, E_{OFF}, switching energies (* shows the modeling results without capacitive effect).

$E_{\mathrm{ON}}/E_{\mathrm{OFF}}$	$d = 5\mathrm{mm}$		$d = 10\mathrm{mm}$	
	E_{ON}	E_{OFF}	E_{ON}	E_{OFF}
Meas	280μJ	81.3μJ	364.7μJ	92μJ
LTSpice	259μJ *(191)	79 μJ *(71.5)	348μJ	95μJ
Rel. Err	-7.5% (-32%)*	-3.1% (-12.3%)*	-4.6%	3.3%

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