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Analysis of thin thermal oxides on (0001) SiC epitaxial layers

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Abstract. In this study, electrical properties of MOS capacitors with varying oxide thicknesses have been investigated. The oxide growth was performed at 1050°C without any further post-oxidation annealing steps resulting in oxide thicknesses between 2 nm and 32 nm. Capacitance-Voltage measurements revealed a decreasing density of interface defects for increasing oxide thickness suggesting a deterioration of the interface at the initial stage of the growth.

Introduction

Although Silicon Carbide (SiC) represents the most mature material for wide-bandgap high-voltage power electronic devices, the inversion channel of SiC metal-oxide-semiconductor field effect transistors (MOSFETs) is still strongly affected by low mobility and low performance reliability. These problems are related to the large amount of both interface defects and near-interface traps generated during thermal oxidation.

In early literature, it was suggested that during oxidation, especially for thick oxides, a high density of interface states (D_{it}) could occur due to carbon accumulation at the interface [1]. A deterioration of the interface with increasing thickness, in this case in the range of d_{Ox} = 5 – 75 nm, was later reported in [2]. More recently, R.H. Kikuchi *et al.* [3] suggested an ideal process window in terms of oxidation temperature with T = 1100 – 1300 °C, but a deterioration of the interface would occur not just during later stages of the oxidation process but already during the temperature ramp-up when the chamber is not within the suggested temperature range. The group succeeded in minimizing oxidation by-products of thin (~15 nm) oxides by using a rapid thermal process (with ramp rates up to 600 °C/min) obtaining close-to-ideal interfaces ($D_{it} \sim 10^{11}$ $eV^{-1}cm^{-2}$) without further post-oxidation annealing (POA) processes. Here, instead of using high ramp rates, the time of the oxide growth at the plateau temperature of 1050°C is increased in order to make the influence of the ramping comparably short.

Experiment

For this study, 10 x 10 mm pieces of the same 4° off-oriented n-type 4H-SiC Si(0001) face substrates (CREE) have been processed. The effective carrier density and thickness of the epitaxial layer were 4 x 10^{15} cm^{-3} and 15 μm, respectively. Prior to thermal oxidation, all samples were cleaned in a heated Caro's acid for 10 minutes and dipped in HF (10%) for 2 minutes.

The samples were loaded into the oxidation furnace immediately after the cleaning and dry oxidation was performed at 1050 °C with an O_2 gas flow of 11 SLPM and a ramp-up and ramp-down in N_2 with a ramp rate of 10 K/min.

One sample (referred to as "0 min oxidation") did not receive an oxidation step in O_2 but was ramped up and down in N_2 atmosphere without an oxidation step in-between. The obtained oxide thicknesses, ranging from d_{Ox} = 2 nm to d_{Ox} = 32 nm, were determined ex-situ by both capacitance-voltage (CV) and grazing incidence X-ray reflectivity (XRR) measurements.

Note that although the formation of a native oxide layer of up to 10 Å has been observed after a wet cleaning process [4], we did not find any indication of native oxide after our cleaning step neither by XPS nor CV measurements.

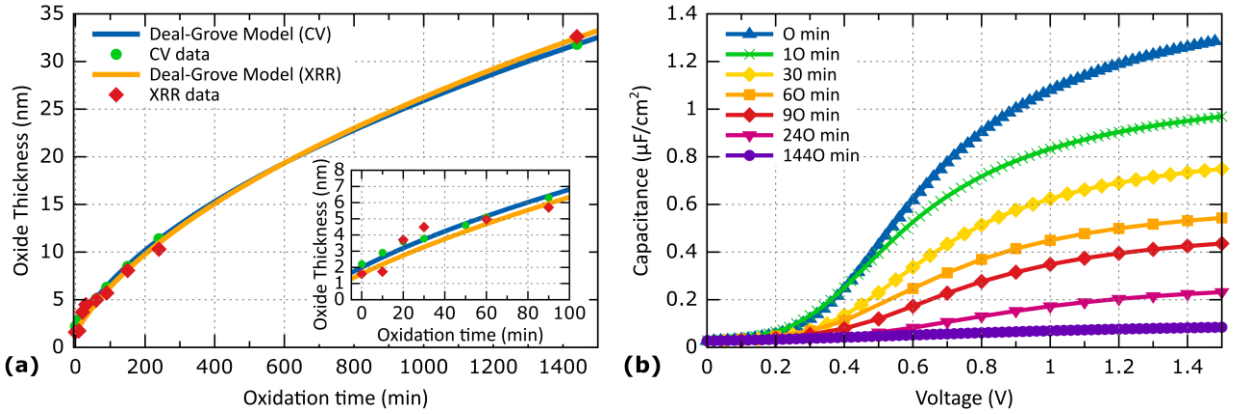

Fig. 1: (a) Extracted oxide thicknesses from the CV data and comparison with XRR data. The inset is a zoom of the first 100 min of oxidation. (b) Capacitance-voltage analysis at 1MHz.

MOS devices were fabricated by depositing 500 nm Al on the oxide and 100 nm Ni on the substrate. The MOS capacitors with radii of 200 μm and 300 μm were analyzed by high-frequency (1 MHz) CV measurements to obtain the SiO_2 oxide thickness and the interface state density D_{it}. Current-voltage (IV) measurements were conducted to determine the leakage current through the oxides. All measurements were conducted at room temperature and repeated on 10 devices to assess the device-to-device variability.

In addition to the MOS capacitors, lateral n-channel MOSFETs have been fabricated on 4° off-oriented n-type 4H-SiC Si(0001) face wafers, with epitaxial p-type SiC (15 x 10^{15} cm^{-3}) as the channel region. Source and drain (S/D) N+ regions were formed by implantation with phosphorous, followed by high-temperature activation. The cleaning prior to the oxidation and the oxide growth at 1050°C for 1440 min were done as described above, resulting in an oxide thickness of d_{Ox} = 32 nm.

For the gate contact, 100 nm Ni was deposited using e-beam evaporation. After a wet-etch for the gate definition and a dry-etch process for opening the oxide below the S/D region, 100 nm Ni were deposited for the S/D contacts. A final rapid thermal anneal (1000°C in forming gas) was performed to decrease the contact resistance of source and drain. All nMOSFET devices had gate channel areas of 100 μm x 180 μm and similarly sized gate and S/D contact pads. Field effect mobilities of the MOSFET devices were then obtained by transconductance measurements.

Results and Discussion

Fig. 1(a) shows the obtained oxide thickness for different oxidation times, extracted both via XRR measurements and CV measurements (Fig. 1(b)). From the electrical analysis, assuming an ideal dielectric constant of $\varepsilon_{r,eff}$ = 3.9 and using the McNutt-Sah method [5] to compensate for leakage currents, the different oxide thicknesses can be extracted. A systematic overestimation of d_{Ox} from the CV data is consistent with what was found in Ref. [6] and indicates a lower real effective oxide dielectric constant of $\varepsilon_{r,eff}$ *~3.66*.

We also fitted both data using the Deal-Grove model, obtaining the following fitted parameters (CV: B = 58.8 nm^2/hr, B/A = 3.72 nm/hr; XRR: B = 54.3 nm^2/hr, B/A = 3.69 nm/hr) for the CV and XRR data, respectively.

The IV characteristics for MOS capacitors with different d_{ox} are shown in Fig. 2. While very thin oxides (0 min – 30 min) are dominated by direct tunneling current [7], thicker ones are dominated by Fowler-Nordheim tunneling [8] with an extracted barrier height of $\Phi_{B,exp}$ = 2.84 eV (close to the ideal value of $\Phi_{B,theory}$ =2.7 eV).

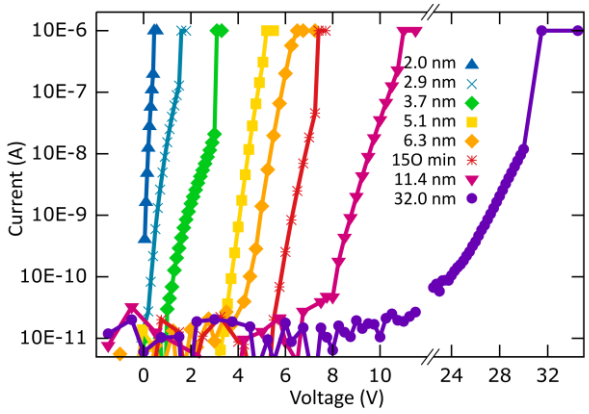

Fig. 2: DC current-voltage curves to determine the leakage current at the flatband for the different oxidation processes.

Fig. 3(a) shows the conductance-voltage (G_p-V) curve measured at a frequency of 1 MHz for each oxide thickness. The density of interface states D_{it} is determined by the relation [9]:

$$D_{it} = \frac{1}{qAf}\frac{G_p}{\omega}\Big|_{max} \quad , \tag{1}$$

where ω is the frequency of the measurement, A is the area of the MOS contact and f is a parameter that depends on the fluctuation of the surface potential.

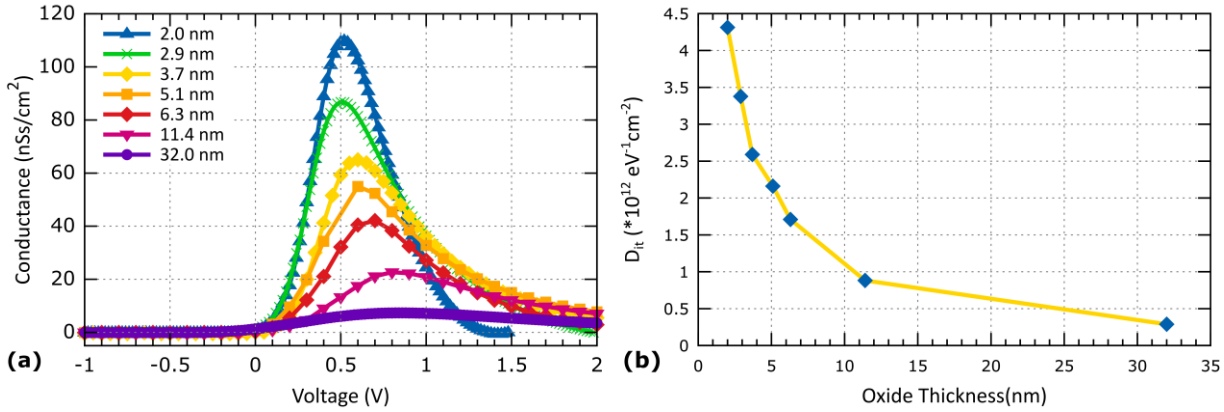

Fig. 3: (a) G_p-V data at 1MHz. (b) Density of interface state traps extracted from G_p-V data.

From the conductance peaks, D_{it} values were determined for all MOS capacitors and are given in Fig. 3(b) as function of oxide thickness. The strong decrease of the interface state density for increasing oxidation times supports the hypothesis of an interface degradation during the initial stage of the oxidation process and is in good agreement with Ref. [3]. In fact, the sample which was only exposed to the heating-up and cooling-down in N_2, without an oxidation step in-between, shows the highest measured D_{it}, thus supporting the idea of a degradation of the interface during the ramping of the chamber.

In addition, lateral nMOSFETs with a thermally grown oxide of d_{Ox} = 32nm (1440 min, 1050°C) were electrically characterized to see whether the low defect density at the interface is consistent with a high mobility. Fig. 4(a) shows the transfer characteristics (I_D-V_G) of the MOSFETs taken in the linear region at a drain voltage of V_{DS} = 0.5 V. From these measurements, the field effect mobility μ_{FE} was determined using [10]:

$$\mu_{FE}(V_G) = \frac{L}{C_{Ox}WV_{DS}} g_M(V_G) \quad , \tag{2}$$

where g_M is the transconductance, L and W are the channel length and width and C_{Ox} is the gate capacitance per unit area. The extracted mobility is plotted in Fig. 4(b) with peak mobilities of $\mu_{FE} \approx$ 35 $cm^2V^{-1}s^{-1}$ which is consistent with the low D_{it} measured for MOS capacitors with the same oxide

thickness. The fairly high mobility is an encouraging result for a thermal oxidation process without any further post-oxidation anneal and shows a favorable improvement to earlier reported channel mobilities of similarly fabricated devices [11].

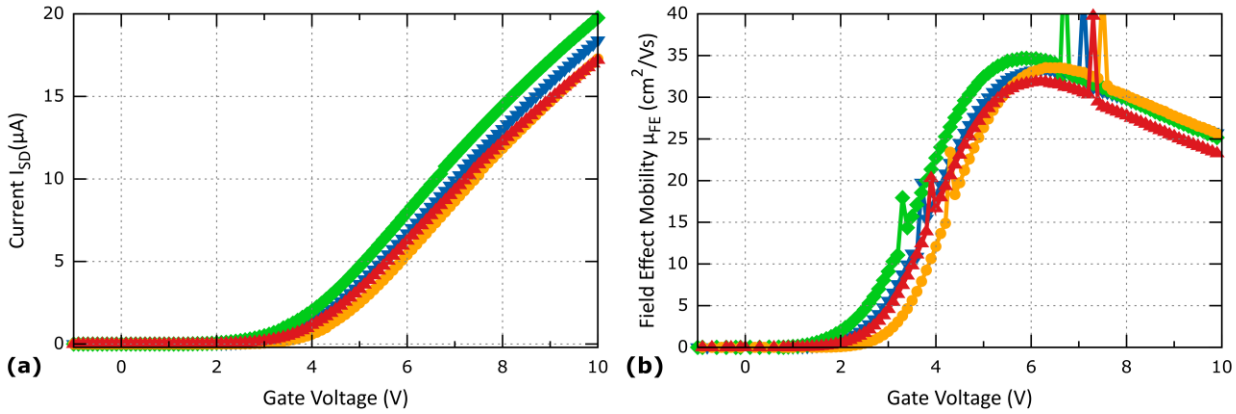

Fig. 4: (a) Drain current (I_{SD}) as a function of gate bias for four randomly selected lateral n-type MOSFETs with a 32nm-thick oxide, measured for several devices. (b) Field effect mobility μ_{FE} as a function of the gate voltage determined by the MOSFETs' transfer characteristics.

Summary

In this paper, we compared the electrical characteristics of various MOS capacitors with different oxide thicknesses and showed a reduction of the interface state density for increasing oxide thicknesses down to $D_{it} = 1.1\times10^{11}$ $eV^{-1}cm^{-2}$ for $d_{Ox} = 32$ nm. For lateral MOSFETs with the same oxide thickness, field effect mobilities of $\mu_{FE} \approx 35$ $cm^2V^{-1}s^{-1}$ were measured. These results indicate that a low defect density and high mobilities can be achieved by a controlled low temperature thermal oxidation process without further POA steps.

Acknowledgments

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