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A Low-Power CMOS Bluetooth Transceiver

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Contents

Abstract

This work describes the design and implementation of a highly integrated, low-power Bluetooth transceiver realized in a 0.18 μm CMOS technology. The target applications are small portable devices, like wrist-watches and smart cards, with particularly tight constraints on power consumption and size.

The receiver has a low-IF architecture with an intermediate frequency of 2 MHz. This architecture allow implementation of the channel filter in monolithic form, avoiding thus the need for an external bulky and expensive filter necessary with the traditional superheterodyne architecture. The implemented active filter is of g_m-C type and includes a current-controlled oscillator to support the realization of an automatic frequency-tuning control loop.

One of the most critical aspects in the realization of a low-IF receiver is the generation of accurate quadrature LO signals needed to suppress the image response of the receiver. The required LO signals are generated by a precise phase-splitter implemented with a digital divide-by-two frequency divider. The measured image-reject ratio is 28 dB, and is limited (by design) by the polyphase filter used to recombine the in-phase and quadrature signal paths.

The transmitter is a two-point modulator based on an integer-N phase-locked loop. Its architecture is almost as simple and therefore as adequate for a low-power implementation as an open-loop modulation scheme, but it does not suffer from the high sensitivity to noise plaguing the latter. The implemented modulator features a selectable loop bandwidth used to achieve a short lock time and a low modulation distortion.

The complete transceiver includes an on-chip antenna switch, and

consumes 26 mA at 1.8 V in receive mode and 23 mA in transmit mode. The design shows the feasibility to implement a highly integrated transceiver in a cost effective technology at a very modest power consumption level.

Riassunto

Questo lavoro descrive la progettazione e la realizzazione di un chip ricetrasmettitore per Bluetooth implementato in una tecnologia CMOS 0.18 μm. Il dispositivo è stato progettato per applicazioni con requisiti particolarmente restrittivi per quel che riguarda il consumo di potenza e le dimensioni fisiche del sistema, come ad esempio orologi da polso e smart cards.

Il ricevitore ha un'architettura low-IF con una frequenza intermedia di 2 MHz. Quest'architettura permette la realizzazione del filtro di canale in forma monolitica e dispensa così il ricevitore da un filtro esterno, voluminoso e costoso come quello richiesto da un ricevitore tradizionale di tipo supereterodina. Il filtro di canale implementato è di tipo g_m-C ed include un oscillatore controllato in corrente per permettere la realizzazione di un sistema di controllo automatico della frequenza centrale del filtro.

Uno degli aspetti più critici della realizzazione di un ricevitore low-IF è la generazione delle componenti in fase e quadratura dell'oscillatore locale necessarie per sopprimere la risposta alla frequenza immagine del ricevitore. Detti segnali sono generati mediante una precisa rete di sfasamento implementata con un divisore di frequenza per due digitale. La soppressione misurata è di 28 dB ed è limitata (da progetto) dal filtro polifase usato per ricombinare i segnali I e Q.

Il trasmettitore è un two point modulator basato su una maglia ad aggancio di fase a rapporti interi. La sua architettura è altrettanto semplice e di conseguenza altrettanto idonea per una realizzazione a basso consumo di potenza quanto quella di un modulatore a maglia aperta, ma, diversamente da quest'ultima, non soffre di alta sensibilità al rumore. Per ottenere un breve tempo d'aggancio e una bassa distor-

sione, la larghezza di banda dell'anello può essere cambiata durante il funzionamento.

Il ricetrasmettitore è completato da un commutatore d'antenna integrato e consuma 26 mA a 1.8 V in ricezione e 23 mA in trasmissione. Esso dimostra la realizzabilità di un ricetrasmettitore ad alto livello d'integrazione in una tecnologia a basso costo e con un consumo molto contenuto.

Chapter 1

Introduction

1.1 Motivation

During the last decades, progress in microelectronic and very large scale integration (VLSI) technology gave rise to a revolution in wireless communications. Although during the first half of the nineties, thanks to highly integrated digital ICs and in particular of digital signal processors (DSPs), commercial services making use of advanced digital modulation schemes were deployed, the RF part of the transceivers were still implemented with discrete transistors and passive components. For instance, the RF part of a typical GSM mobile handset in 1994 was made up of more than 400 discrete components [1].

The vast acceptance of certain services and in particular that of cellular mobile phones, created a large and highly competitive market. The pressure to reduce manufacturing costs, size, and power consumption; to increase the reliability of products and the constant evolution of IC technologies have triggered the industry to develop solutions with a higher degree of integration. Today, the RF part of a GSM chipsets requires around 50 discrete components [1] and even higher integrated solutions are entering the market.

With the introduction of sub-micron CMOS technologies, the performances of Si MOS transistors began to be acceptable for analog high-frequency applications which until then were implemented with III-V compound semiconductors or Si bipolar or BiCMOS technologies.

With CMOS as the most cost effective IC technology, much work was done to investigate and develop RF circuits using this technology. The introduction of sub-micron CMOS technologies also arouse interest for the possibility to integrate a whole system on a single piece of silicon: a so-called *System on a Chip* (SoC). Due to the very high development costs, and to the low flexibility, a SoC realization of a system will remain confined to few applications with an extremely large market.

In parallel to the explosion of the wireless communication market, another market was growing very fast: that of portable computing devices, including laptops, personal digital assistants (PDAs), and their various peripheral devices. In 1997, as it was evident that mid-low performance highly integrated radio transceivers could be realized at low cost, a group of major telecom and PC companies, identified the desire for wireless local connectivity between electronic devices. In 1998, Ericsson, Nokia, IBM, Toshiba, and Intel formed a Special Interest Group (SIG) to create a standard radio interface with the purpose to eliminate the need for cables and the corresponding connectors ("cable replacement") and to simplify data communications between electronic devices and their peripherals, allowing connectivity to occur without any explicit user interaction [2, 3]. This radio interface was named Bluetooth and the fist version of the specifications was published on the Internet [4] in the mid of 1999.

The first Bluetooth ICs were announced a few month after disclosure of the specifications. Most of them were highly integrated solutions with a power consumption of at least 120 mW. Such a power consumption is adequate for most devices such as laptops, PDAs and mobile phones, but not quite adequate for other much smaller devices such as the ones developed by the industrial partners of this project Asulab SA and Acter AG. For this reason the two mentioned companies decided to initiate this project[1] with the goal to develop a highly integrated Bluetooth transceiver with a power consumption adequate for wrist-watch and smart-card applications.

The radio spectrum used by Bluetooth is the license-free Industrial, Scientific, and Medical (ISM) band centered around 2.45 GHz. This

[1] Also in cooperation with the Laboratory of Electromagnetics and Acoustics (LEMA) of the Swiss Federal Institute of Technology, Lausanne, Switzerland and funded by the Swiss Commission for Technology and Innovation (KTI; Project 4764.1).

high frequency is not very convenient for applications requiring the lowest power consumption such as the ones targeted here. In particular other license-free ISM bands at lower frequencies are available. The reasons to adopt the Bluetooth standard in spite of this disadvantage are summarized hereafter:

- In Bluetooth, the connectivity is based on peer communications; that is, no access point or base station is necessary to establish communications.
- As a large number of companies have shown interest in Bluetooth, it is highly probable that in the near future a lot of devices will be equipped with Bluetooth connectivity capabilities.
- Even though several ISM bands are available, the one centered around 2.45 GHz is the only one available worldwide.

1.2 Structure of the Thesis

This thesis describes the design and implementation of a prototype Bluetooth transceiver developed in a commercial 0.18 μm CMOS technology, and is organized in nine chapters.

Chapter 2 gives an overview of the Bluetooth system. The chapter describes purposes, and limitations of this wireless technology, and gives a summary of its main air-interface characteristics.

Chapter 3 discusses the receiver and transmitter architectures considered for our design, and points out the strengths and weakness of each one.

The first part of Chapter 4 deals with the details of the Bluetooth physical layer. The motivations behind the choice of a low-IF receiver architecture and a two-point modulator architecture for the transmitter are given in the second part of the chapter, as well as the detailed planning of the system.

Chapter 5 discuss the main challenges related to the use of a deep submicron CMOS technology for the design of RF and analog circuits, and lists some important parameters of the particular technology used for this project.

The main part of the thesis is constituted by Chapters 6 and 7, where the details of the design of each block of the receiver and of the

transmitter are presented. Most of the blocks have been characterized separately, and the results are also presented here.

The performance of the complete transceiver is described in Chapter 8.

Chapter 2

The Bluetooth System

2.1 System Overview

The Bluetooth technology has been developed with the goal to enable electronic devices such as cordless or mobile phones, modems, headsets, PDAs, computers, printers, projectors, and so on to communicate via short-range ad hoc radio connections. The main user scenarios envisioned during development of the technology were focused on traveling business people: if portable devices would have reliable and simple-to-use wireless connectivity capabilities, they could leave cables and connectors at home. Although most portable devices at the birth of the Bluetooth project were already equipped with infrared links (IrDA), this technology had (and has) several limitations: it requires direct line-of-sight, is sensitive to direction, has limited range, and can only be used as point-to-point link. Furthermore, incompability between devices was not infrequent. Although Bluetooth was not developed as a replacement for infrared links, the lessons learned from this technology were exploited to develop a better standard.

In contrast to most radio systems in commercial use today, Bluetooth is not based on a cellular radio architecture. Its architecture is based on *ad hoc* peer-to-peer connectivity: any device equipped with a Bluetooth radio can make a connection to any other Bluetooth enabled device. There is no wired infrastructure with base stations or access points for coordination and synchronization of communications.

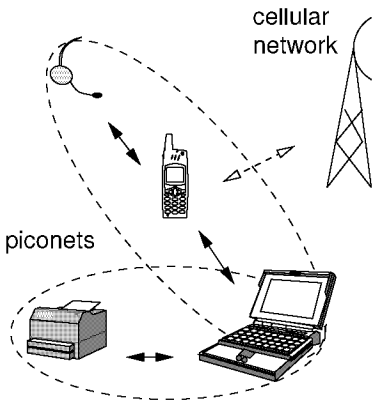


Figure 2.1: *Scatternet composed of two piconets.*

This puts special demands on the connection establishment procedure, which should combine a short setup time with a low-power standby mode. Although not fix, the typical On/Off duty cycle of a unit is below 1% [2].

The Bluetooth system provides a point-to-point or point-to-multipoint connection. In the point-to-multipoint connection, the channel is shared among several units. Two or more units sharing the same channel form a so called *piconet*. The device initiating the connection acts as the master of the piconet, whereas the other unit(s) acts as slave(s). In a piconet there can be up to seven slaves. Multiple piconets with overlapping coverage areas form a so-called *scatternet*. Slaves can participate in different piconets in a time-division multiplex basis. In addition, a master in one piconet can be a slave in an other piconet. At any one time, there can only be one master per piconet since the master identity and clock specify the channel parameters such as frequency-hopping sequence. The piconets shall not be time- or frequency-synchronized. Figure 2.1 shows a scatternet composed of two piconets in a typical application example.

Bluetooth units are classified into three power classes. A class three unit is allowed to transmit at a maximum power level of 1 mW. This should be enough to establish a link over a range of approximatively

Power Class	Output Power (mW)			Power Control
	Maximum	Nominal	Minimum	
1	100	-	1	Yes
2	2.5	1	0.25	No
3	1	-	-	No

Table 2.1: *Power classes.*

10 m. The maximum range of a class one radio is approximatively 100 m. Table 2.1 summarizes the maximum, nominal, and minimum power levels of the various classes.

2.2 Bluetooth Air Interface

Bluetooth operates in the license free 2400–2483.5 MHz ISM band. Since this band is open to anyone and for any application (as long as it satisfies governmental regulations), radio systems operating in this band must cope with unpredictable sources of interference, such as microwave ovens, cordless phones, and baby monitors. To combat interference and fading Bluetooth uses frequency hopping spread spectrum. The band is divided into 79 channels of 1 MHz bandwidth:

$$f_i = 2402 + i \cdot \text{MHz};\ i = 0, \ldots, 78. \tag{2.1}$$

In order to comply with governmental out-of-band regulations, two guard bands are used: one of 2 MHz at the lower band edge and one of 3.5 MHz at the upper band edge. The frequency-hopping sequence, on average, visits each channel with equal probability and has a nominal frequency of 1600 hops/s.

Full duplex transmission is achieved through time division duplex (TDD). The communication channel is divided into slots of 625 μs. On the channel, information is exchanged through packets. Each packet is transmitted on a different hop frequency. A packet nominally covers a single slot, but can be extended to cover up to five slots. In order to support multimedia applications that mix voice and data, Bluetooth defines two link types:

- synchronous connection-oriented link (SCO) and

Packet Type	FEC	Maximal Rate (kb/s)		
		Symmetric	Asymmetric	
			Forward	Reverse
DM1	2/3	108.8	108.8	108.8
DH1	no	172.8	172.8	172.8
DM3	2/3	258.1	387.2	54.4
DH3	no	390.4	585.6	86.4
DM5	2/3	286.7	477.8	36.3
DH5	no	433.9	723.2	57.6

(a) ACL link

Packet Type	FEC	Maximal Rate (kb/s)
HV1	1/3	64.0
HV2	2/3	64.0
HV3	no	64.0

(b) SCO link

Table 2.2: *Link packet types and achievable data rate.*

- asynchronous connection-less link (ACL).

SCO links are symmetrical point-to-point connections, typically used for audio. An SCO connection is established by reserving slots at regular time intervals. ACL links support symmetrical and asymmetrical, packed-switched, point-to-multipoint connections and are used for bursty data transmissions. Table 2.2 shows the data rates achievable with the various available packet types. The difference between the packet types lies in the length of the packets and in the error correction scheme used. The raw data rate (or symbol rate) is 1 Mb/s.

The modulation is Gaussian Frequency Shift Keying (GFSK) with a nominal modulation index of 0.32. GFSK is a kind of binary *continuous phase* frequency shift keying (CPFSK). It is a widely used modulation scheme which allows for low-cost implementations. The

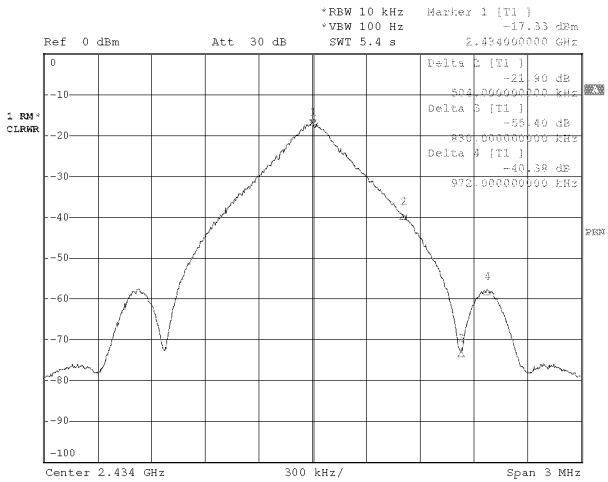


Figure 2.2: *Spectrum of a Bluetooth modulated carrier signal.*

conceptually simplest CPFSK modulator is just a voltage controlled oscillator (VCO) directly modulated by the data stream. The use of independent oscillators to realize a CPFSK modulator is impractical as, by switching from one oscillator to another, phase discontinuities are introduced. These discontinuities are unwanted as they increase the required channel bandwidth beyond the signal bandwidth.

To improve spectral efficiency over what is feasible with binary CPFSK modulation, GFSK makes use of a smoothing filter. The data stream is first passed through a Gaussian pulse-shaping low-pass filter; the resultant waveform is then used to modulate the VCO. The increased spectrum efficiency is traded off for the introduction of some inter-symbol-interference (ISI). The Gaussian filter bandwidth is specified in terms of a bandwidth-symbol period product (BT). Bluetooth specifies a BT of 0.5 which corresponds to a 3 dB filter bandwidth of 500 kHz. The spectrum of a Bluetooth modulated carrier signal is shown in Fig. 2.2.

Another attractive property of GFSK is the fact that it is a constant envelope modulation scheme and as such permits the use of power efficient amplifiers in the transmitter and limiting amplifiers in the re-

Frequency Band	2402-2480 MHz
Channel Spacing	1 MHz
Number of Channels	79
Symbol Rate	1 Mb/s
Modulation Type	GFSK (BT=0.5)
Modulation Index	0.32
Nominal Hopping Frequency	1.6 kHz

Table 2.3: *Basic Bluetooth air interface parameters.*

ceiver.

The main Bluetooth air interface parameters are summarized in table 2.3. Some more details are given in Appendix A.

Chapter 3

Transceiver Architectures

In this chapter we describe the various receiver and transmitter architectures considered for the design described in this thesis. Every architecture has its own advantages and disadvantages and each one requires trade-offs between different parameters. No architecture can be claimed to be *the* best one with respect to every aspect.

The choice of the architecture affects the design of the hole system and is thus a fundamental one. In order to make a good choice, several factors have to be considered, the most important ones being: power consumption, performance, cost, size, weight, integration level, complexity, and time to market. The minimum required performance is dictated by the Bluetooth type approval. The relative weight of all other factors are determined by the application at hand. As the transceiver developed here targets very small devices such as smart-cards and wrist-watches, a small size and a low power consumption are key requirements. In particular, as power consumption sets dimensions and type of the battery, it also has a major impact on size, weight, and cost of the system.

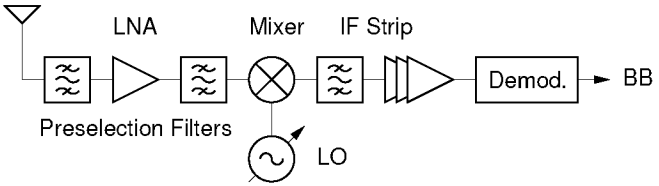


Figure 3.1: *Block diagram of a single conversion Superheterodyne receiver.*

3.1 Receiver Architectures

3.1.1 Superheterodyne

The Superheterodyne architecture has been patented by Edwin H. Armstrong in 1920 [5]. Due to the very high performance achievable with this architecture, it is by far the most widely used receiver architecture since the thirties. The key concept behind this architecture is the use of the heterodyne principle to convert the incoming signal to a fixed, usually lower frequency called intermediate frequency (IF), where most of the receiver selectivity and amplification occur.

Figure 3.1 shows the block diagram of a single conversion superhet receiver. The signals picked up by the antenna are first filtered by a so-called preselection filter and amplified by a low noise amplifier (LNA). The signals are then further filtered by a second preselection filter and applied to the RF input of a mixer. The mixer performs a multiplication of the incoming signals with the signal provided by a local oscillator (LO). This operation converts both the signal at $f_{LO} + f_{IF}$ and the signal at $f_{LO} - f_{IF}$ to the same IF frequency. As at the output of the mixer the two signals can no longer be discriminated, the unwanted of the two signals, called *image*, has to be suppressed prior to mixing. The aim of the preselection filters is therefore not only to suppress strong out-of-band signals which could saturate the front-end of the receiver, but also to suppress the image signal, located at a frequency of $2f_{IF}$ apart from the desired one.

The receiver is tuned by changing the frequency of the LO. The main selectivity is provided by the channel filter at the fixed IF. No tuning is needed in the channel filter. This is a significant advantage, since the

implementation of a filter with a fixed passband characteristic is much easier than the implementation of a tunable filter. Furthermore, due to the lower frequency, channel selection at the IF requires a less selective filter (relative bandwidth) than performing the full selection at RF.

The IF strip also provides most of the receiver gain, including, if needed, an automatic gain control (AGC) loop. The use of a fixed, relatively low frequency simplify the design of the amplifiers, reduce the risk of oscillations and lower power consumption.

The IF frequency has to be chosen with care. A low IF frequency simplifies the design of the IF strip, but makes suppression of the image a difficult task. On the contrary, a high IF, while relaxing the design of the image-reject filter, impose more stringent requirement on the IF strip. The first IF frequency is commonly chosen to be 5–10 % of the carrier frequency. For systems with demanding selectivity specifications, more than one IF frequency can be used. This, of course, comes at the cost of complexity.

The primary drawback of the superheterodyne architecture is its inadequacy for high levels of integration. The required high-Q, low-loss, low-distortion filters are well beyond the capabilities of current integrated technologies. Consequently, external passive high-Q filters are generally used, usually implemented with ceramic filters, SAW filters, or sometimes with LC filters. In order to accommodate standards with different bandwidths, an array of selectable channel filters is required.

3.1.2 Low-IF

The low-IF architecture is closely related to the superheterodyne. The main difference lies in the way the image signal is dealt with.

As told by the name itself, a low-IF receiver is a superheterodyne receiver using a very low IF frequency. Common choices are just one or two times the signal bandwidth. By choosing such a low IF frequency it becomes possible to use monolithically integrable filters to perform channel filtering. The price to pay is an image signal very close to the desired one which can not be filtered by a preselection filter.

There are two ways to "solve" the image problem. One way is to let the image frequency fall exactly between two channels [6], where ideally there is only noise. By doing so, the noise figure of the receiver is worsened by at least 3 dB. In practice, due to the sidebands of the sig-

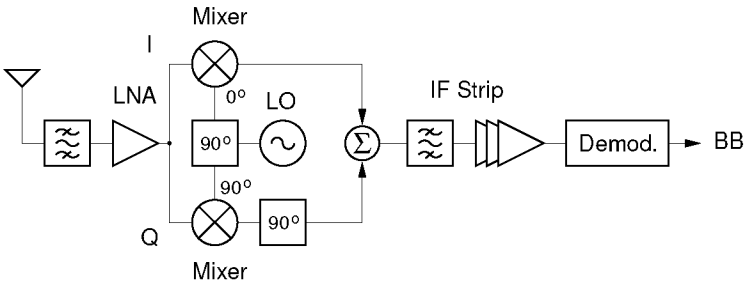


Figure 3.2: *Block diagram of a Low-IF receiver using an image-reject mixer.*

nals, more degradation is to be expected. Furthermore, as the spurious receiver response is not really eliminated, there are two LO frequencies which tune the same channel.

Another better way to deal with the image problem is to use an image-reject mixer (IRM). A block diagram of a Low-IF receiver using an image-reject mixer is depicted in Figure 3.2. An image-reject mixer is a trigonometric solution to a filtering problem and consists of two mixers driven by quadrature LO signals and a 90° phase shifter. Consider the wanted signal and its image:

$$S(t) = A_S \sin[(\omega_{LO} + \omega_{IF})t] \tag{3.1}$$

$$M(t) = A_M \sin[(\omega_{LO} - \omega_{IF})t + \Delta\phi]. \tag{3.2}$$

The signals at the output of the mixers are:[1]

$$G[S(t) + M(t)] \sin(\omega_{LO} t) = \frac{G}{2}[A_S \cos(\omega_{IF} t) + A_M \cos(\omega_{IF} t + \Delta\phi)] \tag{3.3}$$

on the I path, and

$$G[S(t) + M(t)] \cos(\omega_{LO} t) = \frac{G}{2}[A_S \sin(\omega_{IF} t) - A_M \sin(\omega_{IF} t + \Delta\phi)] \tag{3.4}$$

[1] At the output of the mixers there are also higher frequency components. As for the present discussion they are irrelevant, and in a practical realization they are filtered, they have been neglected.

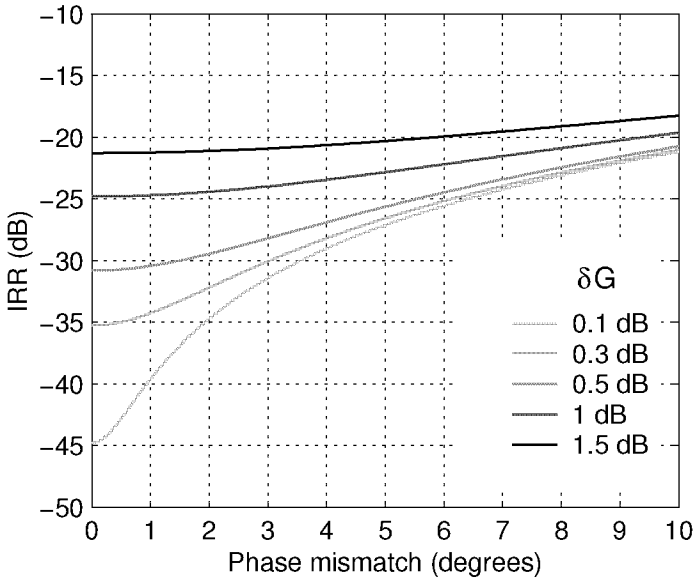


Figure 3.3: *Image-rejection ratio as a function of phase and gain mismatch between I and Q paths.*

on the Q path, where G represents the mixer gain. After a phase shift of 90° on the Q path, the I and Q signals are summed together. While the components of the wanted signal are added in phase, with ideal I and Q paths, the image is completely suppressed. As the image gets suppressed by a subtraction, the amount by which it is attenuated is a sensitive function of the gain δG and the phase mismatch $\delta\varphi$ between the I and Q paths (including any quadrature error of the LO signals). The image rejection ratio (IRR) can be calculated with the help of the following equation:

$$IRR = \sqrt{\sin^2(\frac{\delta\varphi}{2}) + \left(\frac{\delta G}{2G}\right)^2 \cos^2(\frac{\delta\varphi}{2})} \tag{3.5}$$

Figure 3.3 shows the IRR as a function of $\delta\varphi$ for various δG. The difficulty of achieving an IRR higher than 35 dB is apparent.

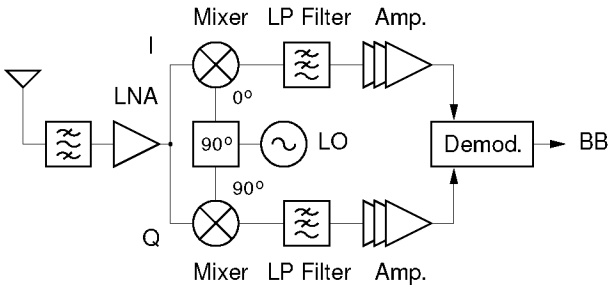


Figure 3.4: *Block diagram of a direct conversion receiver.*

Due to the good matching characteristics of components of the same type on integrated circuits, integrated technologies are well suited for the implementation of image-reject mixers. Monolithically integrated image-reject mixers with an IRR of approximatively 30 dB can be produced with good yield and without the need for trimming. Values considerably higher than this require trimming or a calibration loop [7].

Although the signal at the image frequency can not be filtered by an RF filter, a low-Q preselection filter is usually required to attenuate out-of-band signals and alleviate blocking problems.

3.1.3 Direct Conversion

During the last decade, the direct conversion receiver architecture has received much attention, as it is the architecture with the potential for the highest integration. The direct conversion architecture can be considered as an extrapolation of the low-IF architecture to an IF with a carrier frequency f_{IF} of zero.[2] However, from a technical point of view, it suffers from a few problems which are unique to this architecture and which require particular consideration [8, 9, 10].

Figure 3.4 shows the block diagram of a direct conversion receiver. The mixer translates the center of the desired channel directly to baseband. Adjacent channels can thus be suppressed by a more flexible and

[2] For this reason, a direct conversion receiver is also sometimes called a *zero-IF* receiver.

easier to implement low-pass filter.[3] Although by doing so there is no image frequency in a strict sense, the lower half of the signal spectrum itself is folded to the positive frequency axis and overlap with the upper half of the spectrum. In order to distinguish the lower from the upper half of the spectrum and thus recover the information provided by the *phase* of the signal, a vector detection scheme with quadrature LO signals and in-phase (I) and quadrature (Q) baseband paths is required. Any gain and phase mismatch between the two paths causes a leakage of power from one half of the spectrum to the other. However, whereas the signal at the image frequency in a low-IF receiver can be much stronger than the desired signal, the lower and the upper half of the spectrum of a signal have nearly the same power content. Thus, while a *strong* image signal could completely mask the wanted signal, the typical gain and phase mismatch errors between the two branches of a direct conversion receiver cause "only" a slight degradation of the receiver bit error rate (BER).

The most serious problem plaguing direct conversion receivers is the DC-offset issue: the receiver has to be able to distinguish between the low frequency components of the signal, which ideally extend down to DC, and DC-offset errors arising in the baseband signal paths. One source of offset errors is device mismatch. DC-offsets caused by device mismatch are in the order of 1–5 mV and are thus much larger than the signal of interest which is in the order of a few hundreds of microvolts. Due to the large gain of the baseband strips, in order to avoid saturation, these errors need to be removed. As mismatch-induced errors are constant or varies very slowly, they can be removed with the help of a calibration loop.

Another more troublesome source of offset errors is that caused by LO re-radiation. Because of the limited reverse isolation of mixers and LNAs,[4] some fraction of the LO power may leak to the antenna. The power reaching the antenna gets partially reflected at the interface between LNA and the antenna, thus going back to the RF port of the mixer and demodulating to DC. Since the impedance of the antenna is a function of the surrounding environment, this DC-offset component

[3] In effect, a bandpass filter centered at DC when the negative frequency axis is also considered.

[4] But also because of unavoidable spurious paths (e.g. through power supply and ground lines).

is not constant and a calibration loop may thus not work effectively. This problem is particularly serious in frequency hopping systems since both, reverse isolation and antenna impedance are also functions of frequency. Self-mixing problems are also caused by signals picked up by the antenna and leaking to the LO port.

A second problem (also afflicting low-IF receivers) caused by that part of the LO power reaching the antenna is that the re-radiated signal lies at the center of the channel and may thus disturb nearby receivers tuned on the same frequency (one or two channels apart in case of a low-IF receiver).

A further problem affecting direct conversion receivers is AM detection: any even order nonlinearity in the RF section rectifies amplitude modulated interferer signals and make them indistinguishable from the desired one. Constant envelope modulated interferer signals may also cause problems due to the amplitude modulation introduced by fading and other multi-paths effects.

Flicker noise, which can be orders of magnitude larger than thermal noise, may be an additional factor limiting the achievable sensitivity, especially in CMOS implementations. Even though some circuit tricks to alleviate flicker noise problems, such as chopper stabilization [11], may be used, a technology with low flicker noise may be needed.

To solve the above summarized problems, most of the direct conversion receivers developed to date use AC coupled baseband strips. This of course cuts off part of the spectrum of the desired signal and may only be used with systems employing modulation schemes with a low DC content, as e.g. the large index FSK used with some paging standards [12, 13] or with broadband systems as e.g. the IEEE 802.11b wireless LAN [14, 15] and the WCDMA [16] standards. Many companies are developing calibration schemes to enable the use of the direct conversion receiver architecture also with systems employing modulation schemes with high DC content and in particular with GSM [1].

3.2 Transmitter Architectures

3.2.1 Direct Conversion

Figure 3.5 shows the block diagram of a direct conversion transmitter. The topology is the same as that of a direct conversion receiver where

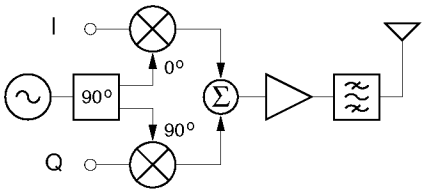


Figure 3.5: *Direct conversion transmitter architecrure.*

the direction of all signals has been reversed: the I and Q baseband signals are directly translated to the channel frequency by a quadrature modulator. Here, any phase $\delta\varphi$ and gain δG mismatch between the two baseband strips gives rise to leakage of power from one sideband to the other resulting in distortion of the modulation.

In case of a transmitter, thanks to the relatively high input signals level, the DC-offset and flicker noise problems making the implementation of a direct conversion receiver difficult are less of a problem. Even so, the DC-offset needs to be minimized as it gives rise to LO feedthrough which overlaps with the modulated carrier. A second source of LO feedthrough are the mixers: to keep the spurious emission to an acceptable low level, the mixers need to be well balanced double balanced mixers (DBM). Also, since the mixers are the main source of inter-modulation products, they need to have a low distortion characteristic.

In medium and high power transmitters, the modulated output of the power amplifier (PA) can disturb the LO signal [17]. This can be avoided by separating the PA output spectrum from the oscillator frequency using the offset-LO principle: the required carrier frequency f_{RF} is generated by two oscillators working at a frequency of $f_{RF} \pm f_{IF}$ and f_{IF} respectively. The desired frequency is then generated with the help of a mixer, while the image needs to be suppressed by a filter.

The direct conversion transmitter architecture can be used to generate any kind of modulation and is suitable for high integration. It is widely used in mid-high performance transmitters. Its main drawback is the need for two highly linear mixers and two baseband signals which are usually generated by two D/A converters.

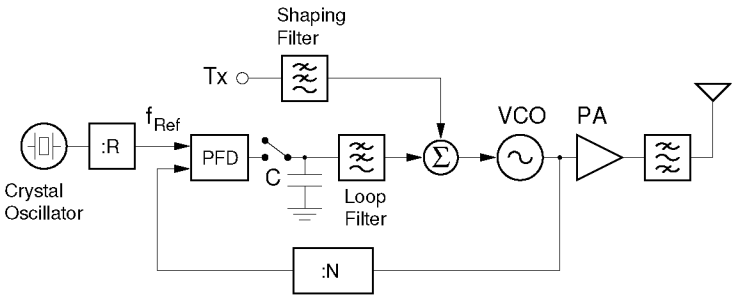


Figure 3.6: *Open-loop modulation transmitter architecture.*

3.2.2 Open Loop Modulation

The so called open loop modulation architecture is the simplest way to frequency modulate the carrier of the transmitter of a time division duplex/time division multiple access (TDD/TDMA) system. The block diagram of an open loop modulation transmitter is shown in Figure 3.6.

TDD/TDMA systems like Bluetooth and DECT, specify a short channel switching time. This sets the maximum allowed synthesizer lock time which for Bluetooth is 220 μs. The dynamics of a phase locked loop (PLL), which is the most widely used kind of synthesizer, is almost entirely determined by the loop filter. To satisfy the Bluetooth specifications with a second order loop filter, the PLL loop bandwidth has to be at least 20 kHz. The maximal loop bandwidth on the other hand is dictated by stability considerations. To have a stable output frequency with low spurious content, the loop bandwidth has to be lower than about 1/10th the reference frequency. In an integer-N PLL, the reference frequency in its turn sets the minimum frequency step size of the synthesizer and is thus specified by the standard to be implemented.

To frequency modulate the carrier generated by the synthesizer, the baseband signal Tx can be added to the loop signal at the input of the VCO. In order not to introduce distortion however, the loop bandwidth must be significantly lower than the lowest frequency component of the modulating signal (see below) which for Bluetooth is around 320 Hz. This is clearly not possible if the lock time specification has to be

met. One possible solution to this issue is to open the synthesizer loop during the modulation intervals and modulate the VCO in "fly-wheel" mode [18, 19].

This solution is in principle very simple and does not require any extra components. In practice, however, some problems may limit the achievable performance. The main potential sources of problems are listed hereafter:

- Any leakage current from the VCO tuning varactor diode, from the loop filter components and from the PLL charge pump, cause a drift of the carrier center frequency.
- Undesired perturbations such as the turn-on transient of the power amplifier, can shift the output frequency. As the center frequency during transmission is not controlled, the mean frequency will remain shifted until the end of the transmit slot.
- The mean oscillator frequency is particularly sensitive to changes in supply voltage (frequency pushing) and to any change of load impedance (load pulling).

Notwithstanding these problems, open loop modulation is used in several commercial DECT transceivers [20, 21].

3.2.3 Two Point Modulation

Another way to extend the FM response of a PLL down to DC, involves the application of modulation to both the VCO and the reference oscillator simultaneously. This scheme is called two point modulation. The block diagram of a transmitter based on a single loop PLL synthesizer modulated by way of two point modulation is depicted in Figure 3.7.

The single loop PLL synthesizer consists of a VCO, two digital frequency dividers, a phase-frequency detector (PFD), a loop filter, and a reference oscillator. The purpose of the loop is to make the phase of the VCO precisely tracks the phase of the reference oscillator. Although the PLL is nonlinear, when the loop is locked,[5] it can be accurately described by a linear model [22].

[5] A PLL is said to be locked, when the frequency of the divided VCO signal is the same as the frequency of the reference oscillator and the output of the PFD is proportional to the phase difference of the two signals.

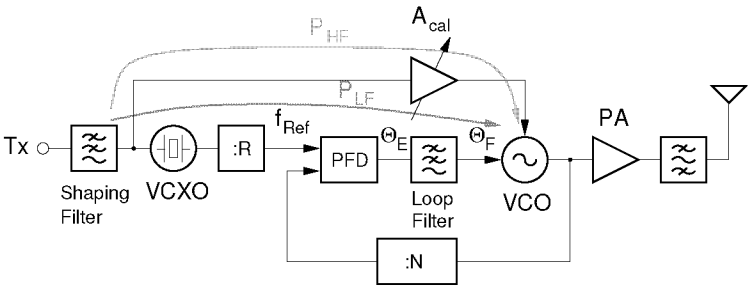


Figure 3.7: *Two point modulation transmitter architecture.*

The transfer function describing the instantaneous VCO angular frequency ω_o when the modulating signal V_{FM} is applied to the VCO input (path P_{HF} in Figure 3.7) is

$$T_{HF}(s) = \frac{sK_{FM}}{s + \frac{K_{VCO}K_{PFD}F(s)}{N}} \tag{3.6}$$

where K_{VCO} is the VCO gain when driven from the input connected to the loop filter, K_{FM} is the VCO gain when driven from the modulation input (including amplifier A_{cal}), K_{PFD} is the phase-frequency detector gain factor, N is the divider constant of the divider dividing the VCO frequency, and $F(s)$ is the loop filter transfer function, which has a low-pass characteristic and often is chosen to have the following form:

$$F(s) = \frac{K_o}{s} \cdot \frac{1 + s\tau_z}{1 + s\tau_p} \tag{3.7}$$

$T_{HF}(s)$ has a high-pass characteristic: the output frequency can only be modulated at rates greater than the PLL loop bandwidth. For modulation rates lower than the PLL loop bandwidth, the phase error introduced by the modulating signal is corrected by the action of the loop and does not appear at the output.

On the other hand, the transfer function describing the instantaneous VCO angular frequency ω_o when the modulating signal V_{FM} is

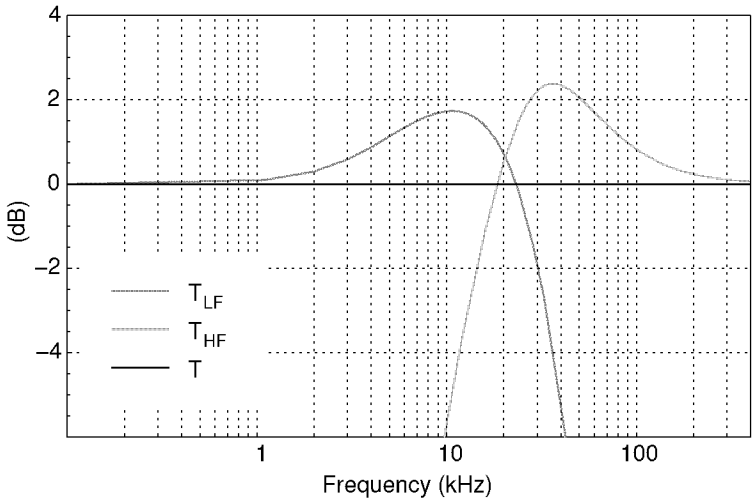


Figure 3.8: *Two point modulator partial and total FM transfer functions normalized to K_{FM}.*

applied to the reference oscillator (path P_{LF}) is

$$T_{LF}(s) = \frac{\frac{K_{VCO}K_{PFD}K_R F(s)}{R}}{s + \frac{K_{VCO}K_{PFD}F(s)}{N}} \tag{3.8}$$

where R is the divider constant of the divider dividing the reference oscillator frequency, and K_R is the gain of the reference oscillator whose output frequency must also be capable of being modulated by a voltage signal. $T_{LP}(s)$ has a low-pass characteristic which means that through this path the PLL output frequency can only be modulated at rates slower than the loop bandwidth. For rates faster than this, the synthesizer is not fast enough to follow the changes.

To obtain a modulator with a modulation bandwidth extending from DC to frequencies higher than the loop bandwidth, the synthesizer has to be modulated through both paths simultaneously:

$$T(s) = T_{HF}(s) + T_{LF}(s) \tag{3.9}$$

Inserting (3.6) and (3.8) in the above expression it can be shown that if

$$K_{FM} \cdot R = K_R \cdot N \tag{3.10}$$

$T(s)$ simplify to

$$T(s) = K_{FM} \tag{3.11}$$

That is, if Equation (3.10) is satisfied, the two point modulator becomes a modulator with a flat response extending from DC to an upper limit determined by the VCO modulation bandwidth, independently from the PLL loop bandwidth. The loop bandwidth can thus be chosen according to other specifications such as the maximum lock time.

The partial FM transfer functions $T_{LF}(s)$ and $T_{HF}(s)$ together with the total FM transfer function $T(s)$ of a two point modulator based on a type 2 third-order loop with a bandwidth of 20 kHz and a phase margin of 55° are illustrated in Figure 3.8. The curves have been normalized to K_{FM}.

One disadvantage of this architecture is the need for a voltage controlled crystal oscillator (VCXO) in place of a conventional crystal oscillator. Moreover, in order to satisfy Equation (3.10), the gain of the VCXO or the gain of the VCO needs to be calibrated. This can be achieved by inserting a variable gain amplifier (or attenuator) in one of the two paths P_{LF} or P_{HF} as exemplified by the amplifier A_{cal} in Figure 3.7. Fortunately, the BER performance seems not to be very sensitive to gain mismatches between the two paths [23].

Often, in a transceiver, the reference frequency of the PLL is also used as basic clock frequency for the baseband processor. The effects of the slight frequency change introduced by the two point modulator on the operation of the latter have thus to be taken into account. In case of problems, the reference frequency for the main synthesizer has to be generated with a separate crystal oscillator or with the help of a second PLL using the baseband crystal oscillator as reference frequency. In the latter case, the reference frequency of the main PLL can be modulated by choosing a very low secondary loop bandwidth and by applying the low-frequency components of the modulating signal to the VCO of the secondary loop.

The reference oscillator is not the only place where the low-frequency modulation components can be injected into the loop. An alternative

point is e.g. in front of the loop filter. A simple analysis however shows that to achieve *frequency* modulation down to DC, an ideal integrator is needed. Even though a TDD/TDMA system like Bluetooth provides enough time intervals during which the integrator can be reset, modulation through the reference oscillator is particularly attractive as the VCXO automatically performs the needed integration without the need for extra circuitry.

The use of a *fractional-N* PLL allows for an extra method to modulate the frequency of a synthesizer. As a fractional-N PLL allow a very fine control of the frequency, the modulation information can directly be added to the nominal divide value controlling the carrier frequency. By including a digital compensation filter, this method allows to digitally modulate the carrier at rates slower and faster than the loop bandwidth [24]. The main disadvantage of this method is the fact that the compensation filter depends on the PLL loop filter.

Chapter 4

System Planning

In the previous chapter we have discussed in general terms receiver and transmitter architectures capable of providing the performance required by Bluetooth. For each one, we have pointed out the various trade-offs, merits, and weaknesses.

Here, we first analyze the requirements relevant for the RF transceiver dictated by the Bluetooth standard. The Bluetooth type approval specify test conditions for a complete system. Some specifications as e.g. the nominal output power are directly applicable as requirements for one or more parts of the transceiver. Others need to be translated in a metric appropriate for the design of the transceiver front-end. For instance, the receiver sensitivity is specified as a maximal BER given a reference signal. The BER in its turn depends from the type of demodulator/detector used and from the noise generated by the front-end. Thus after having specified the kind of detector to be used, the noise figure can be used as a better metric for the receiver front-end.

Next, we will identify the most appropriate architecture compatible with the target applications, and finally we will assign the required performance figures to each block of the system.

4.1 Transceiver Requirements

4.1.1 Receiver Specifications

The relevant requirements for the design of the receiver are sensitivity, selectivity, blocking, and intermodulation.

As previously said, the sensitivity of the receiver is specified in terms of BER. The receiver must be able to demodulate a -70 dBm Bluetooth modulated signal with a maximal BER of 0.1%. For ease of implementation, and to reduce power consumption, the GFSK modulated signal is demodulated with a sub-optimal limiter/discriminator detector. For 10^{-3} BER, such a detector needs an input SNR of 18 dB in case of a nominal modulation index of 0.32, and of 19 dB in case of the smallest allowed modulation index of 0.28 [25]. Thus, at room temperature, with a 1 MHz receiver noise bandwidth (BW), the maximal allowed receiver noise figure at the antenna is

$$\begin{aligned} NF &= -70 \text{ dBm} - 10\log(kT) - 10\log(\text{BW}) - \text{SNR} \\ &= 25 \text{ dB} \end{aligned} \tag{4.1}$$

where k is Boltzmann's constant ($1.3807 \cdot 10^{-23}$ J/K) and T is the temperature in Kelvin.

Due to nonlinearity in the receiver front-end, interfering signals picked up by the antenna create harmonic and intermodulation products which may degrade or even prevent reception of the wanted signal. In particular, if the input contains two signals at f_1 and f_2, a nonlinearity of order n produces components at

$$f_{n,i} = i \cdot f_1 \pm (n-i) \cdot f_2 \qquad i = 0, \ldots, n \tag{4.2}$$

Whereas even order intermodulation products falling on top of the desired signal can be substantially reduced by using an appropriate preselection filter, odd order intermodulation products can not be reduced by filtering prior to the final channel selection. In particular, a third order distortion in the presence of two interfering signals, one k channels and the other $2k$ channels from the desired signal, causes an intermodulation product to fall at the frequency of the desired signal. As usually the nonlinearity of third order is the most significant one, the linearity of a receiver is adequately specified in terms of the third order intercept point (IP3). The IP3 is the extrapolated power level at which the third

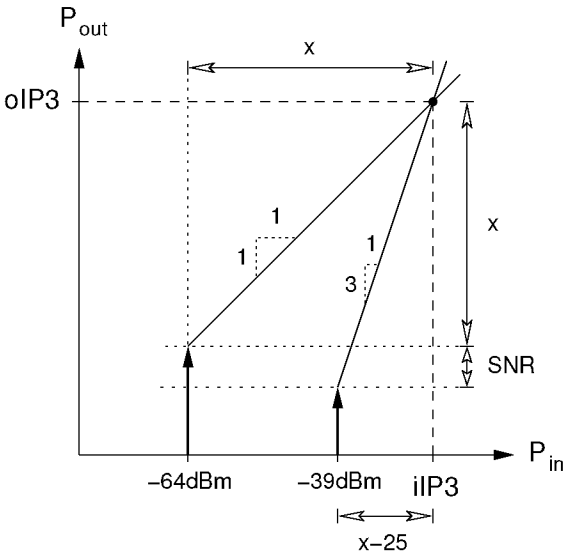


Figure 4.1: *Third order intercept point specification.*

order intermodulation products reach the power level of the desired signal. A Bluetooth unit has to demodulate a -64 dBm reference signal with a maximal BER of 0.1% in presence of two -39 dBm interfering signals (with k=3,4, or 5). This translates in an input IP3 of -17 dBm at the antenna (Fig. 4.1).

The reception of a signal can also be disturbed by a single strong interferer. The single tone interference (or blocking) specification of a receiver determines several requirements including

- the total channel selectivity,
- the minimal required image-rejection,
- the compression point of the various blocks, and
- the phase-noise characteristics of the VCO.

The phase-noise of the LO is constrained by the blocking specification due to reciprocal mixing: in the same way as the wanted signal present

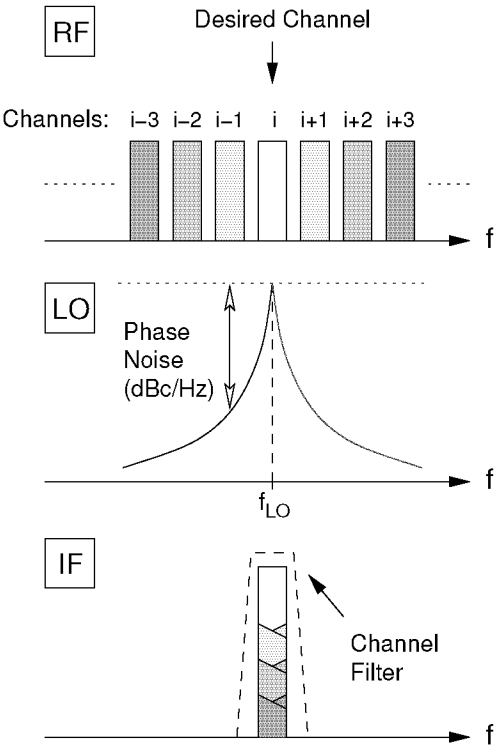


Figure 4.2: *Reciprocal mixing due to the VCO phase noise.*

at the input of the mixer is converted to IF by the LO spectral power concentrated at f_{LO}, any interfering signal at $\pm\Delta f$ from the desired signal frequency is also converted to IF by the power present in the sidebands of the LO spectrum at $f_{LO} \pm \Delta f$. Any strong interferer converted to IF can no longer be discriminated from the wanted signal (Fig. 4.2). The only effective way to reduce reciprocal mixing is by improving the spectral purity of the LO. The blocking specifications for Bluetooth are summarized in Figure 4.3. The interference performance on co-channel and adjacent 1 MHz and 2 MHz channels are specified for a -60 dBm reference signal (drawn in gray). All other specifications

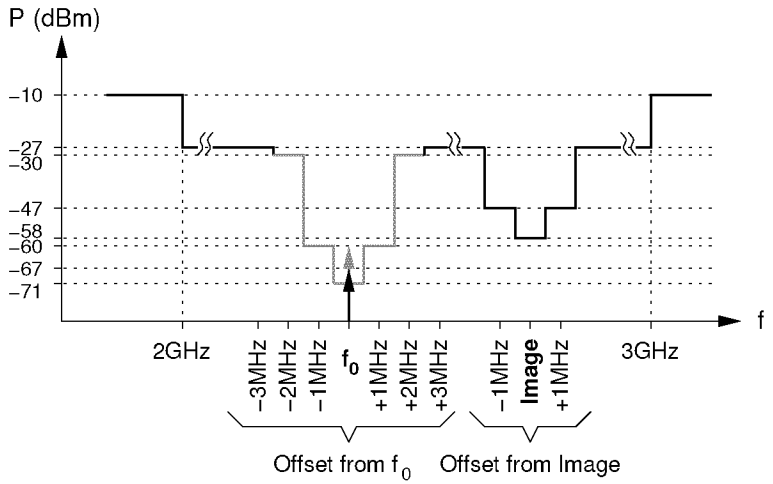


Figure 4.3: *Bluetooth blocking specification summary.*

are specified for a -67 dBm reference signal (drawn in black). From these data we calculate the phase-noise requirements as

$$\begin{aligned} L(\Delta f) &= \frac{C}{I_{\Delta f}} - \frac{C}{I_{\text{co-channel}}} - 10\log(BW) \qquad (4.3) \\ &\Downarrow \\ L(2\text{MHz}) &= -101 \text{ dBc/Hz} \\ L(3\text{MHz}) &= -111 \text{ dBc/Hz} \end{aligned}$$

where $C/I_{\Delta f}$ is the minimal specified desired signal to interferer ratio and $C/I_{\text{co-channel}}$ is the co-channel interference resistance which is 11 dB. These represent absolute minimal requirements. For the design we add a 3–6 dB margin.

From the same data it is apparent that a modest image-reject ratio of 20 dB already fulfill the specifications. From Fig. 3.3, this translates in phase $\delta\varphi$ and amplitude δG errors smaller than 9° and 1 dB respectively.

Selectivity and 1 dB compression point ($\text{CP}_{1\text{dB}}$) for each block of the system can only be specified once the IF frequency and the gain of

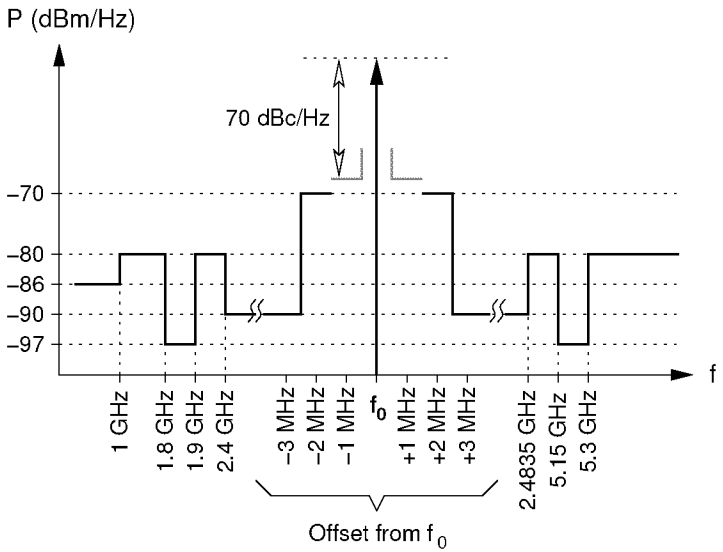


Figure 4.4: *Bluetooth spurious emission mask.*

the blocks have been fixed.

The Bluetooth specification allows five spurious responses frequencies at frequencies with a distance of at least 2 MHz from the wanted signal, where the requirements dictated by the blocking mask shown in Fig. 4.3 are not met. At these spurious responses, a relaxed interference resistance of C/I = -17 dB shall be met.

4.1.2 Transmitter Specifications

The relevant requirements for the design of the transmitter are output power level, modulation accuracy, and spurious emissions.

As already mentioned, Bluetooth units are subdivided in three power classes (Tab. 2.1). We focus on the implementation of a class 2 device whose nominal output power is 0 dBm. A power control is not required and the emitted power is allowed to be between -6 dBm and 4 dBm.

In order to avoid disturbing other Bluetooth units or other radio systems, spurious transmitter emissions should be minimized. Figure 4.4

shows the maximum in-band and out-of-band spurious emission levels permitted by the standard.[1] The specifications at ±500 kHz (drawn in gray) are relative to the carrier power, all other specifications (drawn in black) are absolute power levels. The standard admits up to three in-band exceptions.

The modulation characteristics are specified in terms of modulation-index tolerance, carrier frequency stability and drift rate. The nominal modulation index is 0.32, however, in order to allow low-cost implementations, it may range between 0.28 and 0.35. The initial carrier frequency must be within ±75 kHz from the nominal channel frequency. In addition, during transmission of a packet, the center frequency is admitted to drift by ±25 kHz in a one slot packet and by ±40 kHz in a three or five slot packet. The maximum permitted instantaneous drift rate is 400 Hz/μs.

4.2 Transceiver Planning

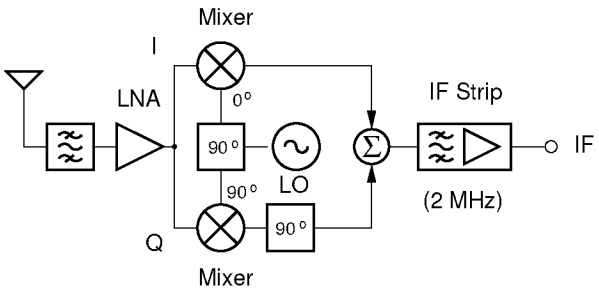
4.2.1 The Receiver

The first step in the planning of the receiver, is the choice of the architecture: due to the high DC content of the spectrum of a GFSK modulated signal, the direct conversion architecture is not very suited for Bluetooth. To choose between the superheterodyne and the low-IF a first compromise is required: on the one hand, having the lowest number of circuits running at RF, the superheterodyne is the architecture of choice to minimize power consumption. On the other hand, the low-IF is the architecture of choice to achieve the highest level of integration. Together with our project partners, we decided to opt for a low-IF architecture, primarily to avoid the need for an external bulky[2] IF filter. Moreover, in order to minimize power consumption, we decided to implement a transceiver with just the minimal required performance.

The block diagram of the receiver is shown in Fig. 4.5. Below it a table shows the voltage gains, noise figures (NF), input 3rd order intercept points (iIP3), and input 1 dB compression points (CP_{1dB}).

[1] Figure 4.4 shows the "operation mode" requirements. The standard also states "idle mode" requirements.

[2] An adequate SAW filter such as [26] measures 11.4x5x2 mm.



	RF Filter	LNA	Mixer	IF Strip
Gain (dB)	–2	12	10	60
NF / $\bar{e}_n$	2 dB	5 dB	18 dB	40 nV/$\sqrt{\text{Hz}}$
iIP3 (dBu)		–16	–4	6
1dB CP (dBu)		–26	–14	–4

Figure 4.5: *Receiver plan.*

The only point of the receiver where the impedance is required to be 50 Ω is at the input of the LNA. The LNA is in fact preceded by a ceramic preselection filter [27] which has to be terminated at both sides with its characteristic impedance which, in this case, is 50 Ω. The impedance of all other interfaces can be freely chosen and is best selected during the design of the circuits. For this reason, in our plan the iIP3s and the CP_{1dB}s are expressed in dBu, which is defined as dBV referred to the voltage generated by 1 mW on 50 Ω, i.e. 223.6 mV rms. MOSFETs are in fact voltage controlled devices whose nonlinear characteristics are best specified by voltage levels. In addition, as at video frequencies and for impedances lower than about 100 kΩ the noise contributed by the equivalent input noise current source of a MOSFET is negligible compared to that contributed by the equivalent input noise voltage source, the noise of the IF strip has been specified in terms of an input voltage noise spectral density (VNSD).

The choice of the receiver IF frequency requires a trade off between power consumption and noise. A low IF frequency is helpful for the

Center Frequency f_0	2 MHz
Tuning Range	± 20 %
Minimum Attenuation	
$f_0 \geq 3$ MHz	51 dB
$f_0 + 2$ MHz	41 dB
$f_0 + 1$ MHz	11 dB
f_0 - 1 MHz	11 dB
f_0 - 2 MHz	41 dB

Table 4.1: *Channel filter selectivity requirements.*

implementation of a low power IF strip, but, due to the high flicker noise of CMOS technologies, a too low frequency may excessively degrade the noise performance of the receiver. As a good compromise an IF of 2 MHz has been chosen.

To relax somewhat the linearity requirements of the IF strip, and in particular of the channel filter, only 20 dB of gain have been allocated prior to it. The filter will be of g_m-C type since to realize a given filtering function they seems to require the lowest power compared with other filter types. Due to the low supply voltage of 1.8 V, and to the difficulty of implementing linear transconductors, the channel filter will be the block limiting the upper end of the dynamic range. In addition, due to the high noise generated by low power transconductors and to the low gain of the front-end, the channel filter will also be the block contributing the most to the overall noise figure which for the plan shown is 19 dB.

The selectivity requirements for the channel filter are listed in Table 4.1 and can be realized with the series connection of a 5th order elliptic low-pass filter with a cutoff frequency of 2.55 MHz and a 3th order Chebyshev high-pass filter with a cutoff frequency of 1.4 MHz, both with an in band ripple of 0.3 dB. An asymmetric filtering function minimize the number of poles and thus power consumption and noise of the filter. Due to process, temperature and supply voltage variations, the center frequency of the filter has to be tunable, with a tuning range of about ±20%.

4.2.2 The Transmitter

Bluetooth is a TDD system, and as such it allow the use of one VCO for both the receiver and the transmitter. The moderate VCO phase noise requirements, allow the use of a fully integrated oscillator. To cover the 3.3% relative frequency bandwidth of the ISM band taking into account a spiral inductor spread of ±5% and a MOS varactor spread of ±10%, a minimum relative tuning range of 20% is required. In addition, as the VCO has to be embedded in a phase-locked loop, an even wider tuning range is required, since the slope of the oscillation frequency vs. controlling voltage curve and thus the gain K_{VCO} of a VCO with a MOS varactor, changes rapidly at the extremes of the range. Although the tuning range capability of a VCO can be extended by switching in tuning elements selectable from weighted arrays, this strategy has been discarded to avoid the calibration step which would be needed to select the right tuning elements for the desired center frequency.

The large tuning range required by the VCO has the disadvantage to make the oscillator very sensitive (high K_{VCO}). An open-loop transmitter architecture has thus to be avoided. The direct conversion architecture, on the other hand, guarantees good performances and is by far the most widely used architecture in commercial products, but, from the power consumption point of view, it is not very attractive. The two-point modulation architecture, on the contrary, is not widely used, but it has the potential to provide the necessary performance with a very low power consumption penalty. For this reason and in order to gain some experience with this architecture our industrial partners were very interested in the implementation of a two-point modulator.

Figure 3.7 depicts the block diagram of the transmitter. To reduce the number of external components, simplify the PCB board, and reduce costs, the output of the power amplifier (PA) shares the same pin with the input of the LNA, that is, the transceiver includes an on chip Rx/Tx switch (not shown in the figure). Therefore, as the input of the LNA must be protected from strong out-of-band signals by a preselection filter, the output of the PA is also connected to the same filter. The consequences concerning the design of the PA are:

- in order to compensate for the attenuation of 2 dB introduced by the filter, the PA must provide a nominal output power of 2 dBm.
- To properly terminate the filter, the output impedance of the PA

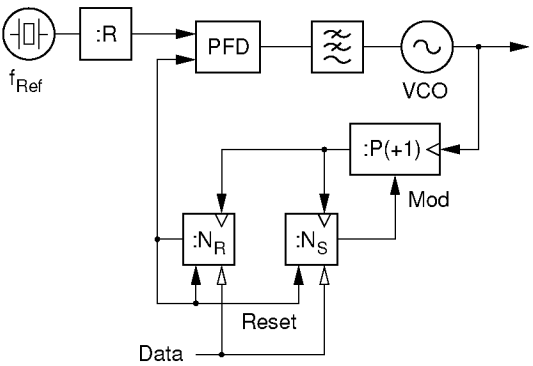


Figure 4.6: *Pulse swallowing frequency synthesizer.*

has to be 50 Ω.

- Any out-of-band spurious signal such as harmonics generated by nonlinearities of the PA are greatly attenuated by the filter.

In addition, since the amplifier is driven by the frequency synthesizer which is also active during the receive time slots, the PA must provide an off state with high signal attenuation. Any spurious signal emitted by the PA during the receive time slots becomes in fact a receiver blocking signal 2 MHz from the desired signal.

The transmitter is based on an integer-N PLL, the reference frequency of which has to be a multiple of 1 MHz. For the present prototype implementation we use 13 MHz as, being the reference frequency used in GSM phones, good quality, low cost crystals are widely available. The minimum required VCXO tuning range to properly modulate the carrier frequency is ±66 ppm. To allow for manufacturing tolerances and temperature variations, we target a tuning range of ±90 ppm.

Concerning power consumption, one of the most critical components of the transmitter is the frequency divider dividing the VCO frequency. Since a fully programmable counter working at the VCO frequency is not practical, we realize the divider by the common pulse swallowing technique shown in Fig. 4.6 [22]. By combining a fast but simple prescaler P with two programmable counters N_R and N_S, any

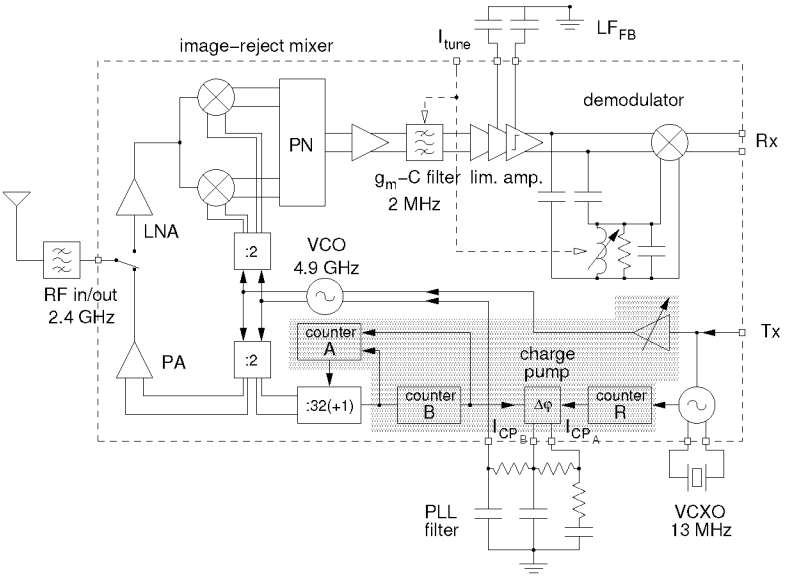


Figure 4.7: *Block diagram of the complete transceiver.*

division ratio $N_R + P \cdot N_S$ larger or equal to $P \cdot (P-1)$ and with $N_R \geq N_S$ can be achieved. The simplest and most power efficient dual modulus prescalers are those with P being a power of two. To cover all of the Bluetooth channels the maximal possible value for P is 32. The programmable counters R, N_R, and N_S work at frequencies lower than 80 MHz. Therefore, a standard cell implementation does not present any disadvantage. Since for the implementation of our prototype no library was available, the programmable counters and the phase-frequency detector (PFD) have not be implemented.

The block diagram of the whole transceiver is depicted in Fig. 4.7. The dashed line represent the border of the IC. The gray area shows the part of the system which has not been implemented on the prototype. The details of the implemented blocks are discussed in Chapters 6 and 7.

Chapter 5

0.18 μm CMOS Technology

For the present design a 0.18 μm foundry CMOS process was used. CMOS is not the best technology choice from the performance point of view. The gain and noise characteristics of analog circuits are in fact strongly dependent from the transconductance g_m of the active devices. Even though the transit frequency f_T of modern deep-submicron CMOS technologies is comparable to that of silicon (Si) bipolar ones, the g_m-to-current ratio of MOS transistors is always lower than that of BJTs. Hence, an implementation with a Si bipolar technology, or with a technology with a higher carrier mobility such as a GaAs MESFET or BJT process would result in a lower power solution, or in a solution with a better performance at the same power consumption level.

On the other hand, CMOS offers very large scale integration capabilities, is cost effective, and is the technology with the most extensive catalog of libraries and intellectual property (IP) cores, ranging from standard-cells to microprocessors. CMOS is thus the most appropriate technology for the implementation of a single chip solution, which was the main motivation behind the choice of a CMOS process.

5.1 CMOS for RF and Analog Design

From the RF designer point of view, the main challenges of a deep-submicron CMOS technology are:

- *Low supply voltage*: one of the disadvantages of deeply scaled CMOS technologies for analog designs is the low supply voltage. The supply voltage is decreased to limit electrical fields within the devices and thus avoid breakdown. As scaling is mainly driven by digital designs to increase density and speed, the threshold voltage V_T of the devices is not scaled proportionally. This is because the leakage currents of digital circuits depend, to first order, exponentially on $-V_T$. This trend limits the number of devices that can be stacked, and frequently precludes the use of cascode structures which are often used to reduce the Miller capacitance, increase the small-signal drain-source impedance, and to accurately copy bias currents of matched circuits. Moreover, the maximal practical overdrive voltage ($V_{GS}-V_T$) which sets the small signal linearity of a MOS device, and the maximal swing of internal nodes are also reduced.

- *1/f noise*: Flicker noise of MOS transistors can be represented by an equivalent gate voltage noise generator

$$\overline{v_{1/f}^2} = \frac{K_F}{WLC'_{ox}f^{AF}} \cdot \Delta f \tag{5.1}$$

  where K_F and AF are process dependent parameters, C'_{ox} is the gate oxide capacitance per unit area, W and L are the width and length of the transistor's gate, and f is the frequency. It is not uncommon for the flicker noise to be the dominant noise component well into the megahertz range. As an example, whereas the thermal voltage noise spectral density referred to the gate of a $W = 100$ μm, $L = 0.18$ μm nMOS transistor biased in saturation and with $g_m = 10$ mS is 1.06 nV/$\sqrt{\text{Hz}}$, the flicker noise at 2 MHz of a transistor integrated with the technology used for this project with the same geometry is 6.7 nV/$\sqrt{\text{Hz}}$. From Eq. (5.1) it is clear that flicker noise can be reduced by increasing the active area $W \cdot L$ of the transistor, but this also results in an increase of the transistor's parasitic capacitances and may not alway be

convenient. In spite of the fact that the power of $1/f$ noise is concentrated at "low" frequencies and is therefore unimportant in linear high frequency circuits such as amplifiers, it may play an important role in high frequency nonlinear circuits such as mixers and oscillators, and in the IF strip of a low-IF or direct conversion receiver.

- *Substrate Coupling*: The relatively highly doped common substrate not only influences the electrical characteristics of the transistors, but it also creates unwanted feedback paths between different nodes of the same circuit, and even between different circuits [28]. Moreover, the substrate also limits the maximal quality factor Q of resonant structures and in particular of integrated spiral inductors to values around 5–10.

5.2 The TSMC Process

Some important characteristics of the TSMC 0.18 μm CMOS process used for this project are summarized in Table 5.1. This CMOS process is based on a p-type substrate, and has 1 poly and 6 metal layers. The process offers a thick top metal option for the implementation of "high-Q" spiral inductors, which unfortunately was not available on MPW runs. The process also offers (optional) high-quality metal-insulator-metal (MIM) capacitors.

To reduce noise coupling through the substrate the process offers a high energy Deep-N-Well (DNW) implant. A DNW surrounded by an N-Well strip may be used to isolate p-type regions (called R-Wells) from the substrate. This way the isolation between different parts of the IC can be greatly improved [29]. This feature can be effectively used to isolate sensitive parts of analog circuits from fast switching digital circuits.

Process	Substrate	p-type/Triple Well
	Metals	6 layers
	Supply Voltage	1.8 V
	L_{min}	0.18 μm
	t_{ox}	32/70 Å
Capacitor	MIM	1 fF/μm^2
Resistors	poly	311 Ω/□
	N-diff.	59 Ω/□
nMOS	V_T	0.42 V
	K'_n	201 μA/V^2
	Peak f_T	62 GHz
	Peak f_{max}	37 GHz
	BV_j	3.6 V
pMOS	V_T	-0.5 V
	K'_n	48 μA/V^2
	Peak f_T	23 GHz
	Peak f_{max}	20 GHz
	BV_j	-3.6 V

Table 5.1: *Some important parameters of the TSMC 0.18 μm CMOS process.*

Chapter 6

Design of the Receiver

6.1 Nonlinear Distortion of MOSFETs

In this section, we estimate the magnitude of the intermodulation products generated by the nonlinear I-V characteristic of a MOS transistor. In particular we calculate the input referred third order intercept point of a common source amplifier assuming that the I-V characteristic of the transistor is the dominant nonlinearity. The results are useful as a yardstick during the first phase of the design.

We describe the characteristic of the device as [30]

$$I_d(v_{GS}) = \frac{\beta}{2[1+\theta(v_{GS}-V_T)]}(v_{GS}-V_T)^2 \tag{6.1}$$

where β is the transconductance factor, and θ is a mobility degradation factor which for the used process is around 3 V^{-1}. Since the intermodulation specifications describe *low level* nonlinearities, we expand the above I-V characteristic in a Taylor series and truncate it after the third order component:

$$\begin{aligned} I_d(v_{GS}) &\approx I_{d0} + \frac{\partial I_d}{\partial v_{GS}}\delta v_{GS} + \frac{1}{2!}\frac{\partial^2 I_d}{\partial v_{GS}^2}\delta v_{GS}^2 + \frac{1}{3!}\frac{\partial^3 I_d}{\partial v_{GS}^3}\delta v_{GS}^3 \\ &= I_{d0} + a_1\delta v_{GS} + \frac{a_2}{2!}\delta v_{GS}^2 + \frac{a_3}{3!}\delta v_{GS}^3 \end{aligned} \tag{6.2}$$

When two signals of equal amplitude are applied to the input, i.e. $\delta v_{GS} = A[\sin(\omega_1 t) + \sin(\omega_2 t)]$, the third order component of the Taylor

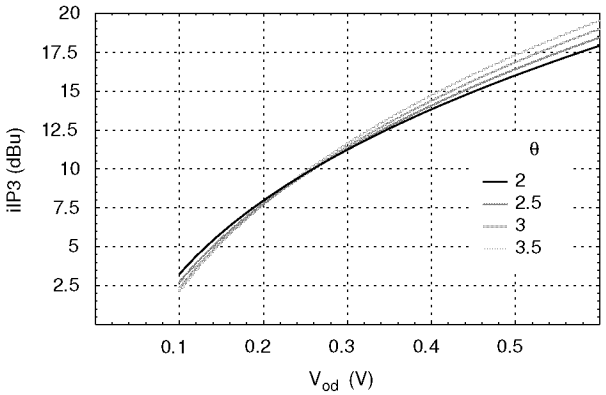


Figure 6.1: *Input referred third order intercept point of a MOS transistor.*

expansion generates the following sidebands:

$$\frac{a_3}{3!}\delta v_{GS}^3 = \frac{a_3}{6}\cdot\frac{A^3}{4}\{3\sin[(\omega_1-2\omega_2)t]+3\sin[(2\omega_1-\omega_2)t]\}+\ldots \quad (6.3)$$

The third order intercept point is defined as the signal level at which the above sidebands have the same amplitude as the input signals amplified by the first order term $a_1 \cdot \delta v_{GS}$ and can thus be calculated as:

$$a_1 \cdot A = \frac{a_3}{6}\cdot A^3\frac{3}{4} \quad (6.4)$$

$$\Longrightarrow \quad A = \sqrt{8\left|\frac{a_1}{a_3}\right|} \quad (6.5)$$

Inserting the values of a_1 and a_3 calculated from (6.1) we obtain:

$$A_{rms} = \frac{A}{\sqrt{2}} = \sqrt{\frac{2}{3}}\sqrt{\frac{v_{od}\left(1+\theta v_{od}\right)^2\left(2+\theta v_{od}\right)}{\theta}} \quad (6.6)$$

where v_{od} is the overdrive voltage defined as

$$v_{od} := V_{GS0} - V_T \quad (6.7)$$

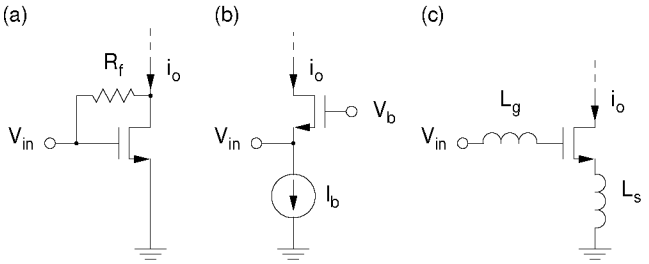


Figure 6.2: *LNA input stage configurations.*

and V_{GS0} is the gate-source bias voltage. We see that the iIP3 is a function of v_{od}. The higher the overdrive voltage, the higher the iIP3 (Fig. 6.1). At overdrive voltages lower than about 100 mV, the transistor enters the moderate inversion part of the I-V characteristic which deviates substantially from (6.1). At overdrive voltages lower than 0 V the transistor is in weak inversion and its characteristic becomes exponential [31]. As a result, the iIP3 for $v_{od} \lesssim 100$ mV degrades rapidly approaching a value of $-12.7+20\log(n)$ dBu for negative values, where n is the slope factor which for the used process is 1.43.

6.2 Low Noise Amplifier

The characteristics of the LNA to be realized are shown in Fig. 4.5. In addition, to properly terminate the preselection filter, a 50 Ω input impedance is required. The 12 dB of gain can be implemented with a single stage amplifier, and, to avoid the need for a balun, we use a single-ended topology.

For this design the three input stage configurations depicted in Fig. 6.2 have been considered: configuration (a) makes use of feedback to realize a broadband input matching. Due to feedback the stage is very linear and relatively insensitive to parasitics, but to realize the required input impedance and gain it requires a large transconductance and thus a large current. Configuration (b) is a common-gate stage. The input impedance is defined by the transconductance g_m of the transistor. By making $g_m = 20$ mS a broadband 50 Ω input imped-

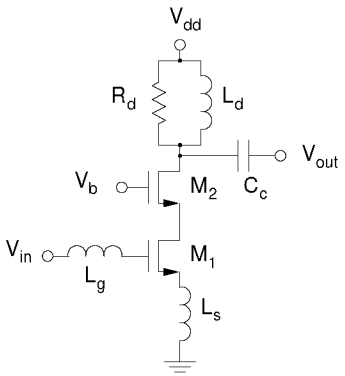


Figure 6.3: *Simplified schematic of the LNA.*

ance is realized. The linearity of the stage is poorer than that of (a), but it is still much better than required for this application (Fig. 6.1). The minimum achievable noise figure is 2.2 dB.[1] Configuration (c) is a common-source stage in which the gate-source capacitance C_{gs} of the transistor is embedded in a matching network to transform the capacitive input impedance of the transistor to 50 Ω. For Q greater than one, the matching network formed by L_s, L_g, and C_{gs} also provides some voltage gain between the input and the gate-source terminals of the transistor so that the effective transconductance of the stage $G_m = i_o/V_{in}$ is larger than the transconductance g_m of the transistor. Therefore, to achieve the specified gain, a lower current is required than with a common-gate configuration. On the negative side, the voltage gain of the matching network degrades somewhat the linearity of the stage, but not to the point to preclude its use for the application at hand. Due to the tight constraint on power consumption we have decided to use configuration (c).

Figure 6.3 shows the schematic of the complete LNA (without biasing). An analysis of the circuit with an idealized transistor model including only the transconductance g_m and the gate-source capacitance C_{gs} provides the following design equations for the input impedance Z_{in}, the voltage gain A_v, and the noise factor F_{id} calculated consider-

[1] Assuming $\gamma = 2/3$.

ing only the drain noise current source of M_1:

$$Z_{in} = j\omega(L_s + L_g) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_s}{C_{gs}} \tag{6.8}$$

$$\begin{aligned} A_v &= G_m \cdot Z_L \\ &= -jQ \cdot g_m \cdot Z_L \\ &= \frac{Z_L}{j\omega_0 L_s} \end{aligned} \tag{6.9}$$

$$F_{id} = 1 + \gamma \frac{1}{Q^2 g_m R_s} \tag{6.10}$$

Here R_s is the source resistance and Z_L is the total load impedance which is the parallel connection of R_d, L_d, the output impedance of the cascode stage, and the capacitive load C_L provided by the mixer driven by the LNA. The inductor L_d is used to tune-out C_L and the parasitic drain-bulk capacitance of M_2 so that for the design only the real part of the load impedance has to be considered. Resistor R_d is used to lower the quality factor Q_L of the load resonator and to precisely set the gain of the amplifier. Cascode transistor M_2 is used to improve the unilaterality of the amplifier. One of the functions of the amplifier is in fact to minimize the emission of spurious signals coming from the LO through the mixer.

From (6.9) and (6.10) it is evident that a high Q simultaneously reduces the noise factor and the required g_m. On the other hand, a high Q also reduces the bandwidth of the matching network, and, if made too high, calibration becomes necessary. As the matching network has to be integrated along with the amplifier, to limit the impact of component tolerances, the quality factor Q has to be limited to values in the range of 2–3. From (6.9) it is also apparent that the transconductance of the input stage G_m is set by L_s. A high G_m requires a small L_s which can readily be realized with a short bonding wire. L_g and L_d are implemented as on-chip spiral inductors. The values of the components used to implement our prototype are listed in Table 6.1.

The current required by the amplifier is 1.2 mA and is set by linearity requirements. Transistor M_1 is in fact biased at the boundary

R, L, C		M_1, M_2	
L_g	7.5 nH	W	104x2.5 μm
L_d	6.1 nH	L	0.18 μm
L_s	1.8 nH	g_m	18 mS
R_d	250 Ω	I_d	1.2 mA
C_c	3.7 pF		

Table 6.1: *LNA Design Values.*

between strong and moderate inversion ($V_{gs} - V_T \approx 80$ mV). A further reduction of the current (without a change in transistor geometry) would have made the linearity of the system dependent upon moderate inversion characteristics which are not well modeled and thus difficult to predict and to control. A simultaneous reduction of current and transistor width in such a way as to keep the transistor in strong inversion would have required impractical inductor values for the input matching network.

6.3 On Chip Rx/Tx Antenna Switch

As explained in Section 4.2.2 the transceiver has to include an on-chip Rx/Tx antenna switch. Therefore, the input of the LNA has to share the same pin with the output of the transmitter power-amplifier (PA).[2]

Figure 6.4 shows the LNA, the output stage of the power-amplifier, and the switches used to power down either circuit. Ideally, the impedance of the inactive circuit should be purely reactive. Any resistive component in fact degrades the performance of the other circuit by introducing losses and noise. This, to some extent, is achieved with the help of the four switches S_1–S_4:

- When the LNA is active (switches position as shown in the figure), M_3 is powered down and inductor L_M is turned into an open circuit. The resulting Z_{TX} impedance is high, slightly capacitive. Its influence on the input matching network of the LNA is readily compensated by adjusting the value of L_g.

[2] For details concerning the design of the PA see Section 7.2.

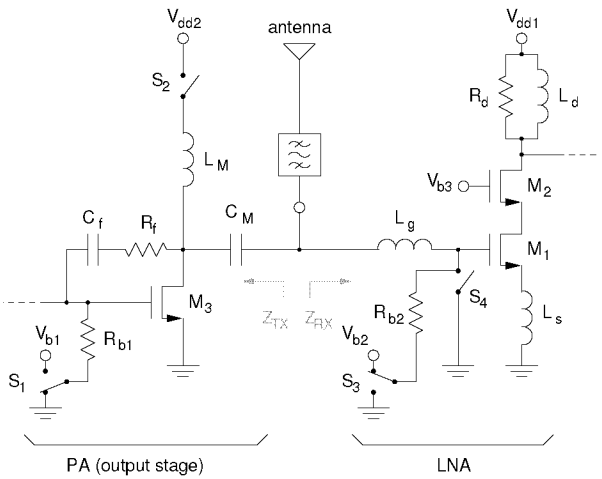


Figure 6.4: *"Distributed" Rx/Tx antenna switch.*

- In transmit mode (switches position opposite to what is shown in the figure), the LNA is powered down by grounding its gate. The impedance Z_{RX} is essentially defined by the large gate inductor L_g, and its influence on the output impedance of the PA can easily be corrected by fine-tuning L_M and C_M.

The main disadvantage of the proposed "distributed" Rx/Tx switch is constituted by the reduction of the quality factor of L_M and L_g in transmit mode, determined by the on resistance of the switches S_2 and S_4. To limit the degradation, the transistor with which the switch are implemented, have to be made short and large. An upper limit to the width of the transistors is set by their parasitic capacitances, most of which are proportional to the transistor width.

The design values of the LNA given in table 6.1 already take into account the influence of the antenna switch.

6.4 Image-Reject Mixer

The RF image-reject mixer must down-convert the RF signal to the 2 MHz IF. In addition to the requirements listed in Fig. 4.5 the mixer must provide a minimal image-reject ratio of 20 dB, and must work with a relatively low local oscillator signal. The generation of a high level LO signal is in fact very expensive in terms of power.

The implemented image-reject mixer is constituted by two mixers, a digital divide-by-two frequency divider LO phase shifter, and a sequence asymmetric polyphase filter (or simply polyphase filter). Single-balanced mixers are used as they require half the current of fully-balanced ones for the same g_m. A disadvantage of the single-balanced structure with respect to the double-balanced one is the lack of isolation between the LO and the IF port. The strong LO signal present on the IF-path, if not properly suppressed, could saturate the active channel filter and desensitize the receiver. As the LO frequency is three decades higher than the IF, the LO signal can be filtered with a non-critical passive RC low-pass filter. To minimize coupling through the substrate we use a differential LO signal which is the strongest on-chip high frequency signal. For the following reasons, we also make use of a differential IF signal:

- By using a differential signal, the maximal usable signal level is increased by 6 dB.
- The use of differential signals results in circuits which are less sensitive to common-mode noise and coupling through the power lines.
- Differential circuits are essentially free from even-order harmonic distortion.

6.4.1 Single Balanced Mixer

Although many mixer structures exist, only few can guarantee all of the requirements mentioned above simultaneously. The most convenient one for a monolithic implementation is the so-called Gilbert mixer, whose simplified schematic diagram is shown in Fig. 6.5.

A Gilbert mixer is essentially a transconductance stage followed by current commutating switches. Assuming ideal switches the conversion

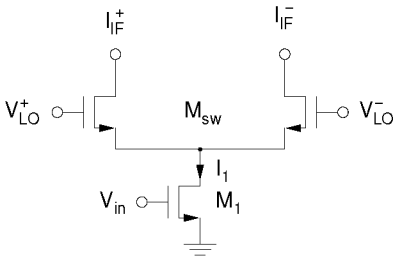


Figure 6.5: *Single-balanced mixer.*

transconductance $G_{SBM} = (I_{IF}^{+} - I_{IF}^{-})/V_{in}$ can be calculated by noting that the current I_1 of M_1 is switched between I_{IF}^{+} and I_{IF}^{-} at the local oscillator frequency f_{LO}. This corresponds to a multiplication of I_1 with a rectangular square-wave function $h(t)$ switching between 1 and -1, whose Fourier series is

$$h(t) = \frac{4}{\pi} \cdot \sum_{n=0}^{\infty} \frac{(-1)^n}{2n+1} \cdot \sin[(2n+1)\omega_{LO}t] \tag{6.11}$$

The ideal conversion transconductance results thus in

$$G_{SBM} = \frac{I_o}{V_{in}} = \frac{2}{\pi} \cdot g_{m1} \tag{6.12}$$

where $I_o = I_{IF}^{+} - I_{IF}^{-}$, and g_{m1} is the transconductance of M_1.[3] The conversion gain observed in simulations with the full transistor models is around 75 % the theoretical value.

To evaluate the noise performance of a Gilbert mixer we separately estimate the noise contributed by the two main noise sources, namely

- the input transconductor M_1, and
- the switching transistors M_{sw}.

An approximate value for the output noise contributed by the input transconductor can be calculated by summing all of those parts of the

[3]The factor 1/2 comes from the following trigonometric relation: $\sin\alpha \cdot \sin\beta = 1/2[\cos(\alpha - \beta) - \cos(\alpha + \beta)]$

white thermal noise $\overline{i_{dn}^2} = 4kT\gamma g_m$ of M_1 which are folded to IF by the switching process.[4] By noting that noise is present at both sides of every harmonic of $h(t)$, the output noise current can be calculated as

$$\begin{aligned}\overline{i_{on}^2} &= 2 \cdot \left(\frac{4}{\pi} \cdot \frac{1}{2}\right)^2 \cdot \left[\sum_{n=0}^{\infty} \frac{1}{(2n+1)^2}\right] \cdot \overline{i_{dn}^2} \\ &= 2 \cdot \left(\frac{4}{\pi} \cdot \frac{1}{2}\right)^2 \cdot \frac{\pi^2}{8} \cdot \overline{i_{dn}^2} \\ &= \overline{i_{dn}^2} \end{aligned} \tag{6.13}$$

From the above equation and (6.12) it appears that even infinitely fast switches degrade the signal-to-noise ratio (SNR) by $(\pi/2)^2$ or 3.9 dB.

To characterize the noise contributed by the switching transistors M_{sw}, the detailed switching transient must be analyzed. As previously noted, the amplitude, and the rise and fall time constants of the LO signal are limited by power consumption considerations to values around 300–400 mV, and 15–20% of the LO period, respectively. Thus, whereas during most of the time the switching transistors are either conducting the whole current I_1 or completely off, thereby contributing very little noise, there are two time slots τ per period T_{LO} during which both transistors are simultaneously on. During these time slots the switching transistors form a differential amplifier contributing thermal and flicker noise to the output. A detailed analysis is rather complicated since during switching the transistors pass through weak, moderate, and strong inversion. To simplify the analysis and gain some insight useful for the design of the transistors, we assume a constant transconductance $g_{m_{sw}}$ during τ, and a quadratic model. The average noise contribution of each transistor is then [32]

$$\overline{i_{dn_{sw}}^2} = \frac{2\tau}{T_{LO}} \left(4kT\gamma g_{m_{sw}} + \frac{K_F \cdot g_{m_{sw}}^2}{WLC'_{ox}f^{AF}}\right) \cdot \Delta f \tag{6.14}$$

By further assuming that τ is proportional to the overdrive voltage v_{ov}, for a fixed bias current and a given LO signal the noise results related to the geometry of the transistor in the following way:

$$\overline{i_{dn_{sw}}^2} \propto \left(4kT\gamma + \frac{K_F}{L^2C'_{ox}f^{AF}} \cdot \sqrt{\frac{L}{W}}\right) \cdot \Delta f \tag{6.15}$$

[4] Flicker noise from M_1 is up-converted to f_{LO} and does not appears at IF.

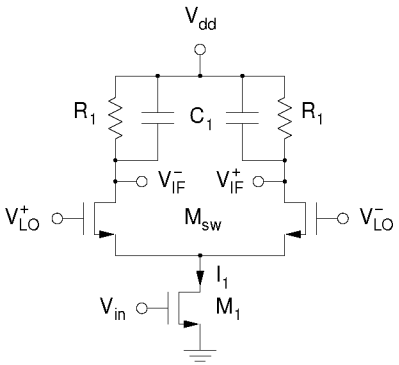


Figure 6.6: *Simplified schematic of the implemented SBM.*

This means that, to a first order approximation, the thermal noise introduced by the switching transistors does not depend on their size, and that flicker noise can be reduced either by an increase of the width or, more efficiently, by an increase of the length of the transistors.

Fig. 6.6 shows the simplified schematic of the implemented SBM. The mixer output current is converted to a voltage by the R_1C_1 load which also forms a first order low-pass filter. The filter has a -3 dB cutoff frequency of 16 MHz and is used to remove the LO feedthrough and the unwanted mixing products.

To realize a total conversion gain of 10 dB, each SBM has to provide a gain of 10 dB minus the gain of the IF phase shifter which in our case is around 0 dB (see below). On the one side, the use of large load resistors R_1 results in small filter capacitors C_1 and in a low G_{SBM} which can readily be realized at low current levels. On the other side, large load resistors are noisy and results in a large output impedance and thus in limited drive capabilities. In addition, the choice of R_1 is also constrained by the -1 dB compression point specification. The maximum output signal swing is in fact determined by the $I_1 \cdot R_1$ product. As a balance we have chosen load resistors R_1 of 600 Ω and a bias current I_1 of 1.67 mA.

To maximize the conversion gain, the switching transients have to be made as short as possible. The transients can be shortened by

biasing the switching transistors at a low overdrive voltage v_{od}. Since the bias current is imposed by other requirements, the only way to reduce v_{od} is to make the transistors as large as practical. From (6.15) large transistors are also helpful to reduce flicker noise. The maximum size is thus only limited by the drive capabilities of the stage driving the LO port, and by the increasing stray capacitances which tend to deteriorate the performance. The design values chosen are summarized in Table 6.2.

R, C		nMOS	W (μm)	L (μm)	I_{d0} (mA)
R_1 (Ω)	600	M_1	16x2.5	0.18	1.67
C_1 (pF)	16.5	M_{sw}	24x2.5	0.18	0.84

Table 6.2: *SBM design values.*

6.4.2 LO Phase Shifter

There are several ways to implement a 90° phase shifter. Here, before going into the details of the chosen implementation, we briefly discuss the four predominant methods used within integrated-circuits:

- *$RC - CR$ Network:* A 90° phase shifter can be realized with

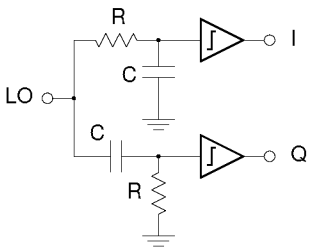


Figure 6.7: *$RC - CR$ phase shifter.*

an RC low-pass and a CR high-pass filter as shown in Fig. 6.7. Provided the resistors and the capacitors are matched, the phase difference is independent from frequency. If the two filters are

loaded by matched loads, the phase difference results also independent from the load. On the other hand, the amplitude is the same only at the -3 dB frequency which is set by an RC product, and, due to process variations, in a worst-case scenario can vary as much as $\pm 40\%$. To restore equal amplitudes limiting amplifiers following the phase-shifter are needed. To be effective such limiting amplifiers requires a quite high power consumption. A further disadvantage of this type of phase-shifter is the need for an LO buffer. The lossy input impedance of the network can not be directly driven by an LC oscillator.

- *Sequence Asymmetric Polyphase Network:* A 90° phase shifter which also introduces only small amplitude errors can be implemented with the help of sequence asymmetric polyphase networks, often called polyphase filters. A two stage polyphase phase-shifter is shown in Fig. 6.8. The RC time constant of each

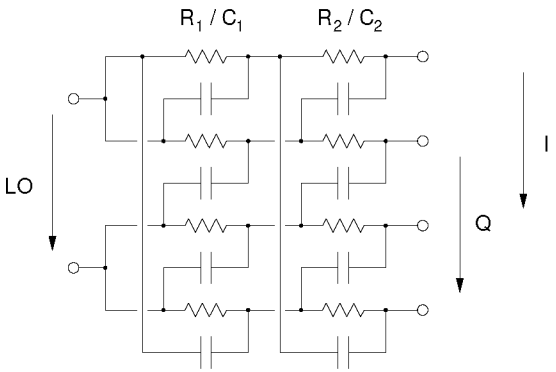


Figure 6.8: *Polyphase phase shifter.*

section determines the frequency at which the amplitude and the phase errors are zero. By cascading several sections a broadband phase-shifter can be realized. Due to the cyclical connection of the components, a polyphase phase-shifter is less sensitive to component mismatch than an $RC - CR$ one. A disadvantage of this structure is the attenuation introduced by the network. A two stage phase-shifter which has been successfully used in a proto-

type during this project [33] shows an attenuation of 3.2 dB and is thus comparable to the attenuation introduced by an $RC-CR$ phase-shifter. Also, similarly to an $RC-CR$ phase-shifter, the low and lossy input impedance of the network dictates the use of an LO buffer amplifier.

- *Coupled VCOs:* A further method which can be used to generate quadrature I and Q LO signals is by coupling two oscillators with the same nominal oscillation frequency as proposed in [34]. If the oscillators are coupled too loosely, the oscillators do not synchronize. If the coupling is too strong the phase-noise degrades. Therefore the quadrature oscillator performs as expected only over a limited range of the coupling coefficient [35]. Since this solution does not require buffer amplifiers, it shows a slight advantage in terms of power. This advantage is however partially lost due to the need for two oscillators.

- *Digital Divider:* A digital divide-by-two frequency divider constituted by two latches clocked on the opposite edges of the clock generates two signals with a phase difference of 90° which can be used as I and Q LO signals (Fig. 6.9). This kind of phase-shifter

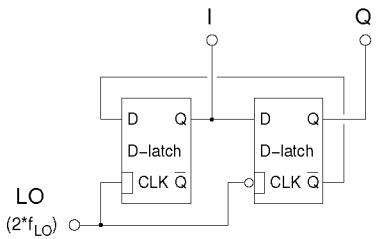


Figure 6.9: *Digital divide-by-two phase shifter.*

is very wideband (ideally from DC to an upper limit determined by the latches), very compact, and very precise. The main drawback is the need for an oscillator running at twice the required frequency. This disadvantage in a transceiver can be turned into an advantage by considering that, due to the different frequencies, no interaction between the output of the PA and the LO

signal can occur. At GHz frequencies the power consumption of frequency dividers becomes relatively high, but, considering the buffers or limiting amplifiers required by other solutions, the power consumption penalty is not very severe.

Due to its many advantages we have decided to implement a digital divide-by-two frequency divider phase-shifter. The main factor limiting the achievable quadrature accuracy using this kind of phase-shifter is the even-harmonics content of the VCO signal driving the circuit, as even-harmonics cause the duty cycle of the signal to deviate from the ideal 50% value. We analyze the phase error generated by the second-harmonic alone, since higher even-harmonics are always significantly lower than the second one. Fig. 6.10 shows the phase-error α generated by the signal

$$A[\sin(\omega t) + K\sin(2\omega t + \phi)] \tag{6.16}$$

driving an ideal master-slave D–flip-flop as a function of the relative amplitude of the second-harmonic component with respect to the fundamental K, for three phases ϕ. The phase-error α is amplitude and phase dependent: if the second harmonic component is in-phase with the fundamental ($\phi = 0$), no error is produced; the maximum error is caused by a phase difference ϕ of 90°. As usually it is not possible to control the relative phase ϕ, the only mean to minimize the phase-error α is to keep the second-harmonic and all higher even-harmonic components as low as possible. For this reason it is very important to use a VCO with a differential topology.

The implemented divide-by-two frequency divider (Fig. 6.11) has been designed in enhancement source coupled logic (ESCL) with resistive loads. The circuit is composed by a couple of latches clocked in anti-phase. Having a fully differential structure ESCL gates inject very little noise into the power supply and the substrate, and are immune to common-mode noise. Furthermore, working with low level signals they are much more power efficient than other logic families. The static power consumption of this logic family is of no concern here since the divider is always working at full speed.

The predominant RC time constant limiting the speed of the circuit is constituted by the load resistors and the total capacitance loading the output nodes. Thus, knowing the load capacitance, the required

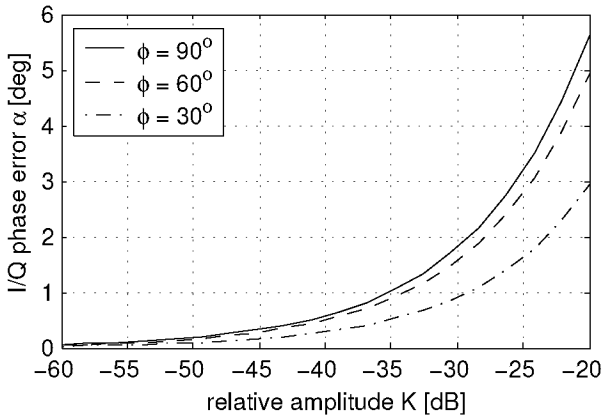


Figure 6.10: *Relative phase-error between the I and Q signals as a function of the relative amplitude of the second-harmonic with respect of the fundamental component of the signal driving an ideal master-slave D–flip-flop.*

load resistor value can be calculated. Knowing the value of the load resistors, the current I_0 required to produce the desired output signal level can be determined. The aspect ratio of the transistors is then sized according to the required input sensitivity (overdrive voltage) and stage gain which must be higher than unity. This is not a straightforward design process, since the capacitances of the latches themselves constitute a considerable part of the total capacitance loading the output nodes. More iterations are necessary to find the optimum configuration.

In order to ensure good mixer-core switching, a signal level of 400 mV has been chosen. Using the iterative procedure outlined above we found that load resistors of 170 Ω, a bias current I_0 of 2.35 mA and transistors with an aspect ratio of 45 μm/0.18 μm form the optimum configuration to drive the capacitive input impedance of the mixers of approximatively 80 fF. The design values are summarized in Table 6.3.

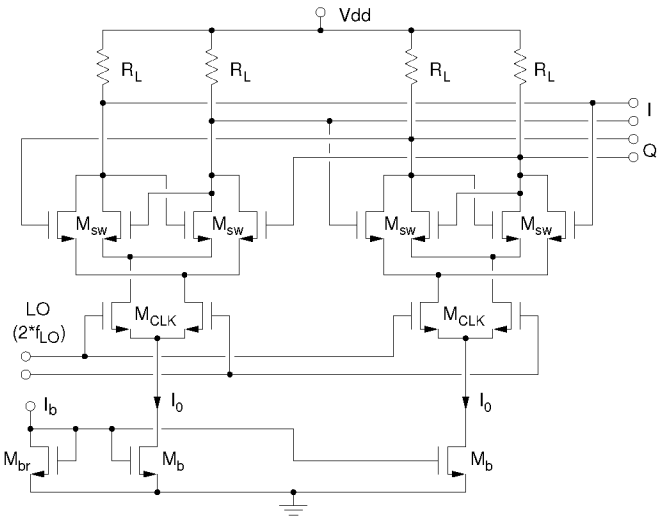


Figure 6.11: *Schematic of the divide-by-two frequency divider generating the I and Q signals.*

6.4.3 IF Polyphase Filter

Differently from the LO phase-shifter, the IF phase-shifter has to preserve the exact waveform of the input signal, and requires a much wider relative bandwidth. A phase-shifter with these characteristics can be implemented with the help of all-pass filters. As noted in section 3.1.2, however, this solution rely on the subtraction of two large signals at the output of the phase-shifter and is very sensitive to amplitude and phase errors.

A better solution is to use a polyphase filter like the two stage filter shown in Fig. 6.12. The key difference with respect to the all-pass phase-shifter is that in a polyphase network the unwanted sideband is canceled within the network itself and not outside it. This makes the polyphase filter an order of magnitude less sensitive to component mismatch.

It can be shown [36] that the chain matrix of a single stage polyphase

MOS	W (μm)	L (μm)	I (mA)		R (Ω)	
M_b	16x2.5	0.18	I_0	2.35	R_L	170
M_{CLK}	18x2.5	0.18				
M_{sw}	18x2.5	0.18				

Table 6.3: *Digital divide-by-two frequency divider design values.*

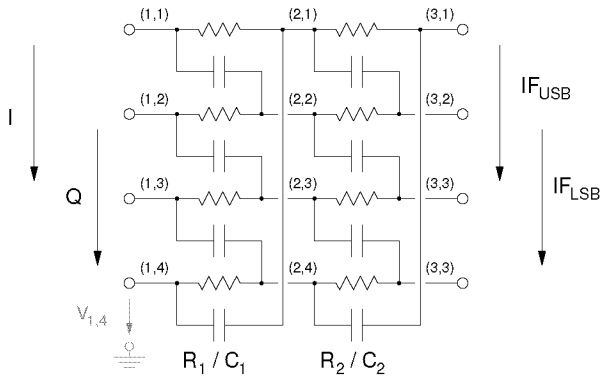


Figure 6.12: *Sequence asymmetric polyphase filter used to combine the I and Q receiver path suppressing the image signal.*

filter of the type shown in Fig. 6.12 is

$$\begin{pmatrix} V_{i,k} \\ I_{i,k} \end{pmatrix} = \begin{pmatrix} \frac{1+sC_iR_i}{1-jsC_iR_i} & \frac{R_i}{1-jsC_iR_i} \\ \frac{2sC_i}{1-jsC_iR_i} & \frac{1+sC_iR_i}{1-jsC_iR_i} \end{pmatrix} \cdot \begin{pmatrix} V_{i+1,k} \\ I_{i+1,k} \end{pmatrix} \tag{6.17}$$

Each section has zero gain at $\omega = -1/R_iC_i$ and maximum gain at approximatively $\omega = 1/R_iC_i$. By cascading several sections with different zeros, the bandwidth over which the image signal gets suppressed by the required amount can be increased.

A two sections polyphase filter with zeros at 1.4 MHz and 2.9 MHz guarantees an image-reject ratio of 20 dB over process variations. The choice of the component values is a tradeoff between noise and area. Low resistor values require big capacitors and thus a large area; high

R (kΩ)		C (pF)	
R_1	10	C_1	5.5
R_2	10	C_2	11.4

Table 6.4: *Design values for the IF polyphase network.*

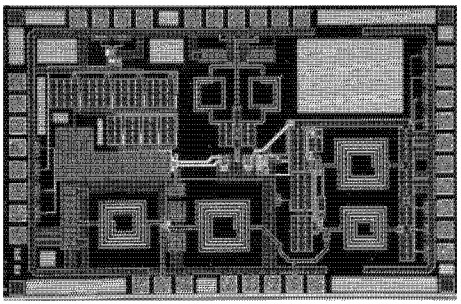


Figure 6.13: *Photomicrograph of the front-end test IC.*

resistor values require small capacitors, but are noisy. Table 6.4 summarize the values chosen for our implementation.

6.5 Front-End Measurements

In this section we present the measurements performed on the LNA/image-reject mixer front-end test IC. To include the effects of the antenna switch, the chip also includes the transmitter power amplifier, but its performance will not be discussed here. The LO port of the image-reject mixer is driven by the on-chip VCO described in the next section. The prototype IC also includes the 10 dB IF amplifier described in Sec. 6.7 and, to enable characterization, its IF output port has been buffered by source-followers with a simulated gain of -1.9 dB. A photomicrograph of the chip is shown in Fig. 6.13.

The measurements have been performed at the nominal supply voltage of 1.8 V on unpackaged chips directly bonded on a PCB. Fig. 6.14 shows the conversion gain of both sidebands. The voltage conversion

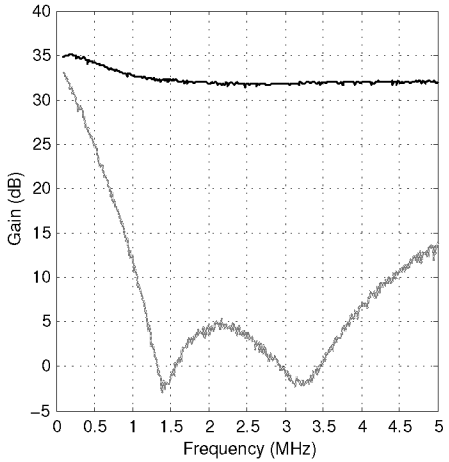


Figure 6.14: *Measured front-end Conversion Gain of wanted- (black line) and image-signal (gray line).*

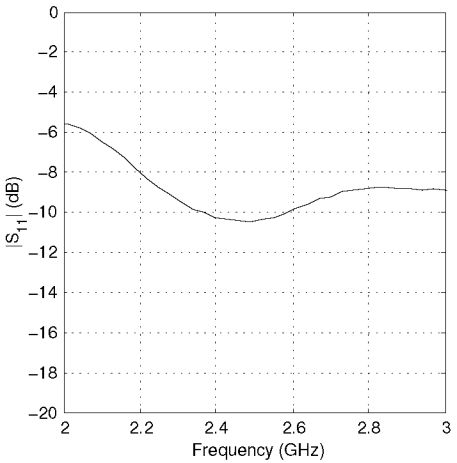


Figure 6.15: *Measured front-end* S_{11}.

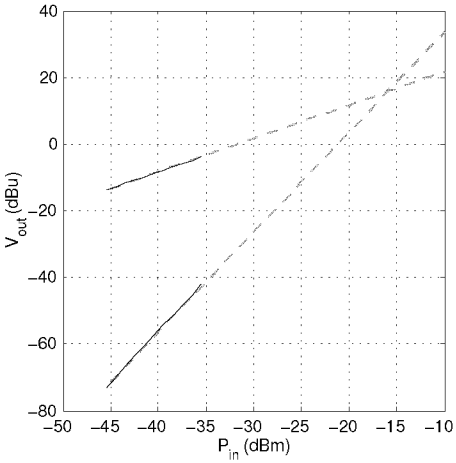


Figure 6.16: *Front-end IP3 based on measurements.*

gain experienced by the upper sideband signal is 29.9 dB (including the output buffer). The image rejection at 2 MHz is 28 dB and is greater than 20 dB between 1 and 4.5 MHz. The well defined zeros at 1.4 MHz and 3.2 MHz indicate a very small LO quadrature error. Both, the gain and the image-rejection are very close to the simulated values.

The input matching of the front-end is shown in Fig.6.15. Due to the low quality factor Q of the input matching network, a sufficiently good matching to the preselection filter is achieved over a large bandwidth. In the band of interest, S_{11} is slightly better than -10 dB.

The third order intermodulation characteristic of the front-end is shown in Fig. 6.16. The iIP3 is -15.9 dBm and meets specifications. Nevertheless, it's important to point out that the linearity of the measured circuit is limited by the 10 dB IF amplifier which actually constitute the first stage of the IF channel filter. Measurements on a similar prototype without this amplifier show an iIP3 of -10 dBm [33].

The noise figure of the front-end is 12.5 dB.

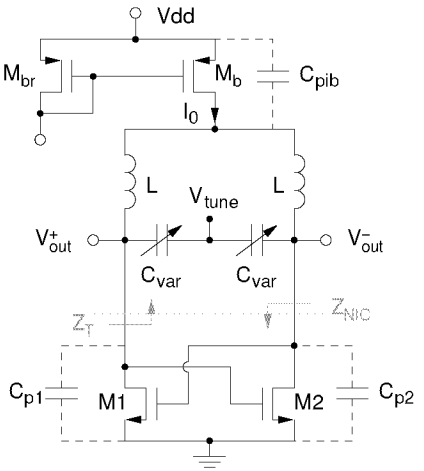


Figure 6.17: *Schematic of the VCO.*

6.6 Voltage Controlled Oscillator

Due to the chosen LO phase-shifter, the voltage controlled oscillator has to generate a frequency which is twice the frequency of the desired channel. This means that the VCO has to run at a center frequency of 4.9 GHz. Moreover, as seen in section 6.4.2, the oscillator must have low even harmonic distortion.

Fig. 6.17 depicts the simplified schematic of the implemented VCO. It is a cross-coupled oscillator and has been chosen mainly because of its differential topology. Several variations of this basic topology have been proposed. In particular a complementary topology making use of pMOS besides of nMOS transistors as feedback elements is very popular [37]. We have chosen to use a topology with only nMOS transistors as the effective mobility of electrons in modern deep submicron technologies is a factor around 4 higher than the effective mobility of holes. Thus, for the same transconductance g_m, nMOS transistors are considerably smaller than pMOS transistors. Smaller transistors have smaller parasitic drain junction capacitances which do not only reduce the achievable tuning range, but are also notoriously lossy.

The choice to use a pMOS biasing current source is dictated by the need to cover the whole tuning range with a controlling voltage comprised between 0 V and the 1.8 V power supply, and by the fact that pMOS transistors have a lower flicker noise spectral density than nMOS transistors. A large pMOS transistor here is advantageous, as the flicker noise spectral density is inversely proportional to the active area and a large capacitance C_{pib} ideally tends to increase the oscillation amplitude by reducing the duty cycle of the current pulses flowing through the transistors.

The cross-connected transistors M_1 and M_2 form a positive feedback loop generating a negative impedance $Z_{NIC} = -2/g_m$. A basic condition for oscillation is that the magnitude of this impedance must be lower than the effective load resistance of the tank at resonance R_T ($= Z_T(\omega_0)$). This results in the following condition for the transistor transconductance g_m

$$g_m \geq g_{mc} = \frac{2}{R_T} \tag{6.18}$$

A rough estimation of the steady state amplitude of oscillation $\hat{V}_{VCO}$ can be calculated by noting that if $\hat{V}_{VCO}$ is considerably larger than the overdrive voltage of the transistors, the transistors work essentially as switches synchronized with the oscillation frequency (Fig. 6.18). In this idealized scenario the current through each transistor is a square wave with 50% duty-cycle and amplitude I_0. The voltage across the tank generated by this current is

$$\hat{V}_{VCO} = \frac{4}{\pi}\frac{I_0}{g_{mc}} \tag{6.19}$$

As with every LC-VCO, the characteristics of the oscillator are determined to a great extent by the tank. As pointed out by Leeson's equation for the single-sideband noise spectral density [38]

$$L(\Delta\omega) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\left(1+\frac{\omega_{1/f}}{|\Delta\omega|}\right)\right\} \tag{6.20}$$

and also by more accurate theories [39], in order to obtain a low phase noise, the quality factor Q of the tank has to be maximized. The tuning

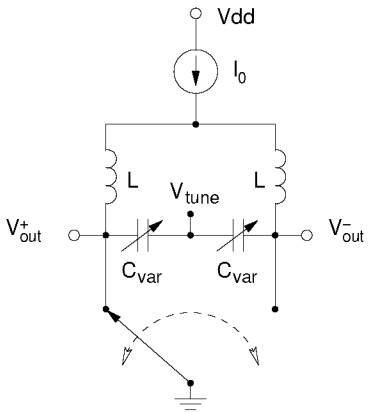


Figure 6.18: *Idealization for the calculation of the amplitude of oscillation.*

range is also determined by the tank: as it is not possible to realize on-chip variable inductors, given the required tuning range, the minimal required varactor capacitance ratio C_{max}/C_{min} can be expressed as follows:

$$\frac{C_{max}}{C_{min}} = \left(\frac{f_{max}}{f_{min}}\right)^2 = \left(\frac{1+\chi/2}{1-\chi/2}\right)^2 \tag{6.21}$$

where χ represents the relative tuning range. To achieve a tuning range of 25% assuming parasitic plus load capacitances $C_{p1} = C_{p2} = C_{min}/4$ a capacitance ratio of 1.8 is required. This large ratio can only be realized by means of accumulation mode MOS varactors which usually have a lower quality factor than *pn*-junction varactors [40]. The capacitance ratio of the p^+–N-well junctions available in the used technology is limited to 1.46 ($-2\ V < V_d < 0.3\ V$).

The process documentation included just a single MOS varactor example, but no scalable model. Therefore an equivalent circuit with an approximate value of the components had to be developed. The cross section of an accumulation mode nMOS varactor together with the elements of the used equivalent circuit is depicted in Fig. 6.19. An approximate value for the maximum and minimum capacitance as a

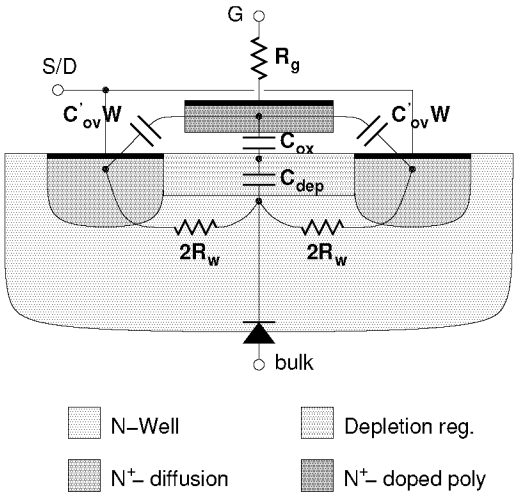


Figure 6.19: *Schematic cross section of an accumulation mode nMOS varactor.*

function of geometry can be calculated with the help of the following equations [41]:

$$C_{max} = C_{ox} + 2C'_{ov}NW \tag{6.22}$$

$$C_{min} = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} + 2C'_{ov}NW \tag{6.23}$$

$$C_{ox} = \frac{\varepsilon_{SiO_2}}{t_{ox}}NWL \tag{6.24}$$

$$C_{dep} = \frac{\varepsilon_{Si}}{t_{dmax}}NWL \tag{6.25}$$

$$t_{dmax} = \sqrt{\frac{2\varepsilon_{Si}}{qN_D}2\phi_f} \tag{6.26}$$

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N_D}{n_i}\right) \tag{6.27}$$

where L is the effective length, W the effective width and N the number of fingers; n_i is the Silicon intrinsic carrier density, C'_{ov} the gate-diffusions overlap capacitance per unit width, t_{ox} the gate dielectric

thickness, and N_D the N-well donor density. Although the last three parameters are technology parameters which are rarely explicitly specified, their value can be extracted from the transistor model parameters. Due to the complex 3D structure geometry, it is not possible to give an analytical expression for the parasitic resistor R_w, but it is intuitively clear that its value is proportional to L, inversely proportional to $N \cdot W$ and gate–N-well voltage dependent. An approximate value for R_g is given by $R_g = R_{shp}\frac{W}{3LN}$, where R_{shp} is the poly sheet resistance. The N-well–bulk junction impedance to a first order approximation does not influence the signal as the N-well lies at differential-mode ground.

R_w is the dominant parasitic resistor, therefore short varactors have a higher quality factor, but a lower C_{max}/C_{min} ratio (since the overlap capacitance $2C'_{ox}NW$ becomes a significant part of C_{min}) than long ones. As a balance between tuning range and quality-factor, we have chosen to use varactors with a length of 0.5 μm.

The impedance level of the tank influences several characteristics of the oscillator. On the one side, a high impedance reduces the power consumption and increase the amplitude of oscillation, but, on the other side, it requires a large area inductor with a high parasitic capacitance to the lossy substrate, and a small varactor with capacitance values comparable to the parasitic capacitances of the transistors and of the spiral inductors. Therefore, a high tank impedance also limit the achievable tuning range. To obtain the required tuning range, the varactor has been designed to have a mean capacitance value of 0.62 pF. The layout of the varactor is composed by 42 fingers, each of 5x0.5 μm^2.

The oscillator includes a second couple of varactors C_{mod} (not shown in Fig. 6.17) connected in parallel to the first one. The purpose of these varactors is to provide a second tuning port used as modulation port during transmission. During reception this port is not used and has to be grounded. The nominal value of the two varactors is 5 fF, their size is 2x0.5 μm^2.

The spiral inductors of the tank have been designed with the help of an electromagnetic-field simulator. Their nominal value (excluding the parasitic inductance of the lines connecting the spiral inductors to the rest of the circuit) is 0.87 nH, and is made of a single metal layer of thickness 1 μm and 15 μm width. The number of turns, the inner radius, and the distance between adjacent metal lines are 1.5, 55 μm, and 1.5 μm respectively. Its equivalent circuit model is depicted in

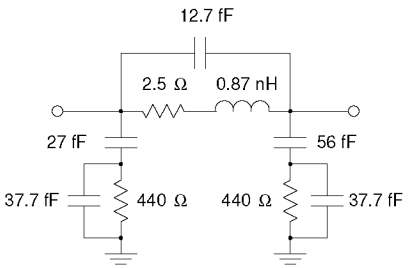


Figure 6.20: *Equivalent circuit of the VCO spiral inductors.*

nMOS	W (μm)	L (μm)	I (mA)		tank	
M_1	24x2.5	0.18	I_1	3	L	0.87 nH
M_2	24x2.5	0.18			C_{var}	0.62 pF
M_b	40x8.5	1				
M_{br}	4x8.5	1				

Table 6.5: *VCO design values.*

Fig. 6.20.

To ensure startup the transconductance g_m of M_1 and M_2 has to be 3–4 times the critical transconductance g_{mc} given by (6.18), and the bias current must be chosen according to the desired amplitude of oscillation. Due to process variations and the absence of an active amplitude regulation loop, some margin to guarantee an amplitude adequate to drive the LO phase-shifter under worst-case conditions is needed. The design values for the implemented VCO are summarized in Table 6.5.

6.6.1 Measured Performance

To enable an accurate characterization of the phase-noise, the VCO has also been realized as a stand-alone circuit. A micrograph of the oscillator is shown in Fig. 6.21. The measurements have been performed on unpackaged dies bonded on a printed circuit board (PCB) at the nominal supply voltage of 1.8 V. The two tuning ports of the free

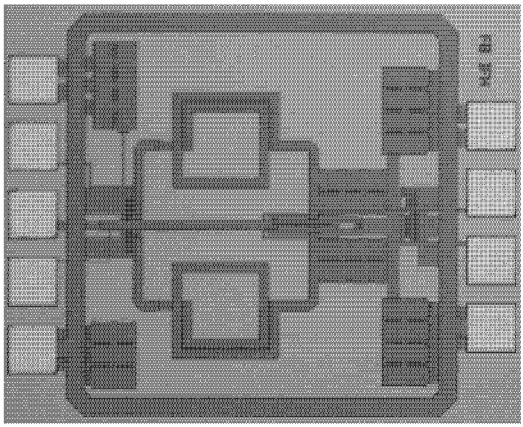


Figure 6.21: *Photomicrograph of the VCO.*

running oscillator have been shorted together and were driven by a voltage source.

Fig. 6.22 shows the VCO oscillation frequency and gain as a function of the controlling voltage V_{tune}. The gain has been obtained numerically computing the derivative of the measured oscillation frequency with respect to the controlling voltage. The maximum relative frequency tuning range is 27%, while the center oscillation frequency is 4.924 GHz.

The phase-noise of the free running VCO for a carrier frequency of 4.9 GHz is shown in Fig. 6.23. The most stringent Bluetooth phase-noise requirement is specified at an offset frequency of 3 MHz from the carrier. Due to the divide-by-two frequency divider, the VCO has (ideally) to satisfy the same specification at twice the offset frequency. The VCO phase-noise at an offset frequency of 6 MHz is -126 dBc/Hz.

6.7 Channel Filter

Several techniques can be used to implement integrated filters. Among the best known are MOSFET-C and g_m-C filters. MOSFET-C filters are actually active-RC filters where, to make the filter tunable, the

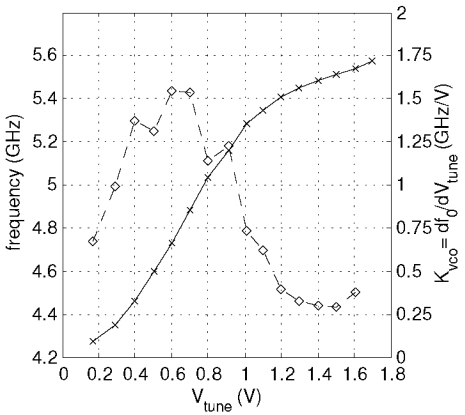


Figure 6.22: *Measured VCO tuning range (solid line) and gain (dashed line).*

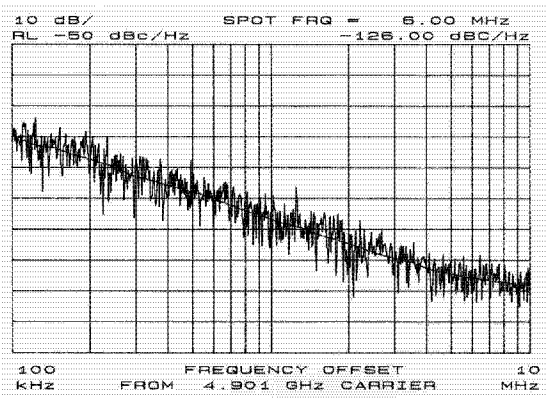


Figure 6.23: *Measured VCO phase-noise.*

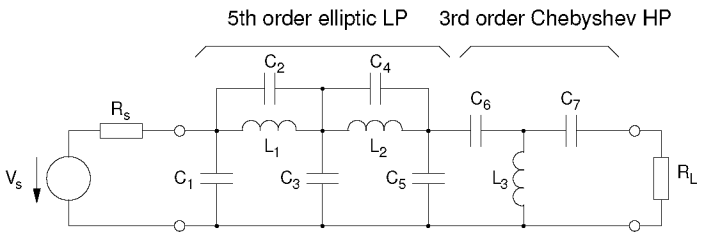


Figure 6.24: *LC ladder filter prototype.*

resistors are replaced with MOS transistors which are then used as voltage-controlled resistors. This kind of filters have good linearity and noise characteristics, but, to realize the filtering function with a small error, they require fast OpAmps with a gain-bandwidth product of around one hundred times the cutoff frequency of the filter, and capable of driving resistive loads. g_m-C filters, on the other hand, are implemented with capacitors and linearized MOS transconductors. The achievable linearity is inferior to that of MOSFET-C filter, but, by using simple transconductors, they can be profitably used to implement higher-frequency or lower-power filters.

Due to the limited dynamic range requirements of Bluetooth and to the high weight given to power consumption, we opted for a g_m-C filter implementation derived from the doubly terminated LC ladder prototype shown in Fig. 6.24. The schematic of the implemented fully differential channel filter is shown in Fig. 6.25. The terminating resistors are implemented with transconductors connected in unity gain configuration; the inductors are simulated with gyrators and capacitors. Each gyrator is implemented with two transconductors as shown in Fig. 6.26.

Since the shape of the filter response depends on the *ratio* of the component values, to improve repeatability and reduce the impact of process variations, each capacitor is made of an integer number of unit capacitors C_u, and each transconductor is made of an integer multiple of unit transconductors G_m. The center frequency of the filter can be adjusted by changing the transconductance of the unit transconductor.

The choice of the filter impedance level involves a trade-off between dynamic range, power consumption, and costs. A high impedance level

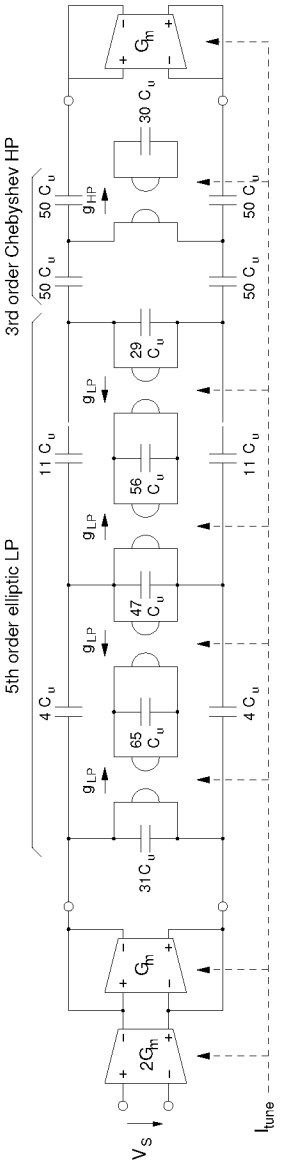


Figure 6.25: *Simplified schematic of the fully differential g_m-C filter.*

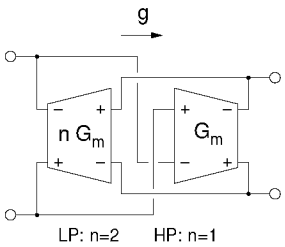


Figure 6.26: *Gyrator implemented with two transconductors.*

allows the use of small transconductors and capacitors (and therefore a small silicon area and a small current), but results in a noisy filter. Since the upper end of the dynamic range is indirectly limited by the supply voltage, a high noise floor results in a small dynamic range. For this reason, the highest usable impedance level is limited by dynamic range requirements. To satisfy the requirements stated in our plan, we use G_m=140 μS and C_u=363 fF.

To balance the margin at the upper- and at the lower-end of the dynamic range, the g_m-C filter is preceded by the amplifier shown in Fig. 6.27. The fully differential amplifier has a gain of 10 dB, and, in order to guarantee an adequate linearity, it has been heavily degenerated with resistor R_E. Each branch is biased with a current of 80 μA.

6.7.1 Linearized Transconductor

Figure 6.28a shows the schematic of the transconductor used in our implementation [42]. The core of the circuit is constituted by M_1–M_4. Transistors M_{b1}–M_{b3} form a current mirror degenerated by M_{CM1}–M_{CM3}, which operate in the triode region. Their purpose is to stabilize the common-mode output voltage at V_{ref}. M_1 and M_2 form a differential pair, the transfer characteristic of which is linearized by M_3 and M_4. These last two transistors, for small input signal amplitudes, operate in the triode region and play the role of degenerating resistors. By connecting their gates to the input of the stage, the effective degeneration resistance is made signal dependent, thus improving the linearity of the resulting $I_{out}(V_{in})$ characteristic. For large input signal

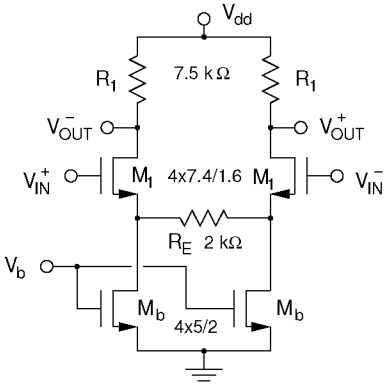


Figure 6.27: *10 dB amplifier preceding the channel filter. Transistor dimensions W/L are in μm.*

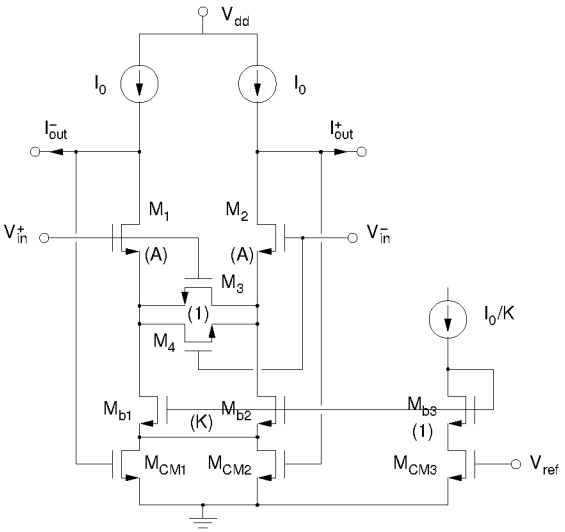
amplitudes, depending on the sign, M_3 or M_4 enters saturation, further extending the range where the effective transconductance of the stage is held (nearly) constant. The shape of the characteristic is a function of the transistor width ratio $A{=}W_1/W_3{=}W_2/W_4$. The optimum ratio concerning linearity is $A{=}6$. The transconductance G_m of the stage can be adjusted by changing the bias current I_0.

The low supply voltage of 1.8 V introduces several drawbacks in the design of the transconductor. The most important ones are:

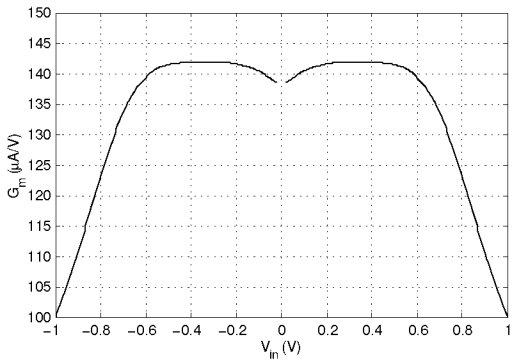
- since no cascode structure can be used to implement the current sources I_0, and the drain-source voltage of M_1 and M_2 is constrained to relatively low values, the resulting transconductor output impedance is rather limited.

- the small overdrive voltage allowed to bias M_{b1} and M_{b2} demands large and therefore noisy transistors.

The current I_0 used in our implementation is 100 μA. The sizes of the transistors are shown in Table 6.6; the simulated effective transconductance G_m as a function of the input signal V_{in} appears in Figure 6.28b.



(a) Simplified schematic.



(b) Simulated $G_m(V_{in})$ characteristic.

Figure 6.28: *Fully differential linearized transconductor.*

nMOS	W (μm)	L (μm)	nMOS	W (μm)	L (μm)
M_1	6x2.8	1.6	M_2	6x2.8	1.6
M_3	2.8	1.6	M_2	2.8	1.6
M_{b1}	4x10	1.6	M_{b2}	4x10	1.6
M_{CM1}	2x3.3	2	M_{CM2}	2x3.3	2
M_{b3}	2x10	1.6	M_{CM2}	3.3	2

Table 6.6: *Size of the transconductor transistors.*

6.7.2 Bandgap Reference

To maximize the dynamic range of the filter, its common-mode voltage has to be set at 1.2 V. A temperature stable 1.2 V reference voltage can conveniently be generated with a bandgap reference [11].

The schematic diagram of the implemented bandgap reference is shown in Fig. 6.29. The core of the circuit is constituted by Q_1, Q_2, and R_1. The single stage OpAmp composed by M_1–M_3, M_{10}, M_{11}, R_3, and C_c forces points A and B to the same potential, while the current-mirror M_{b3}/M_{bc3}, M_{b4}/M_{bc4} forces equal currents into the emitters of Q_1 and Q_2. These two constrains are simultaneously satisfied when the voltage across R_1 is

$$\Delta V_{be} = \frac{kT}{q} \ln K \ , \tag{6.28}$$

where K is the ratio of the emitter areas of Q_1 and Q_2, which in our implementation is 8. The current I_1 is thus proportional to the absolute temperature (PTAT), and its value is set by R_1. By mirroring this current to R_2 and summing the resulting voltage with the V_{be} voltage of Q_3 we obtain the required 1.2 V temperature stable reference voltage [11]. Q_1–Q_3 are parasitic pnp vertical bipolar transistors available to every CMOS technology [43]. Q_1 has a common-centroid layout with Q_2 at its center. All emitters have a square shape with an area of 25 μm^2.

Since the circuit is also stable for I_1=0,[5] to guarantee correct operation, a start up circuit has been added.

[5] Actually leakage currents ensure start up also without a start up circuit, but, since there currents are extremely small, the start up transient is very slow.

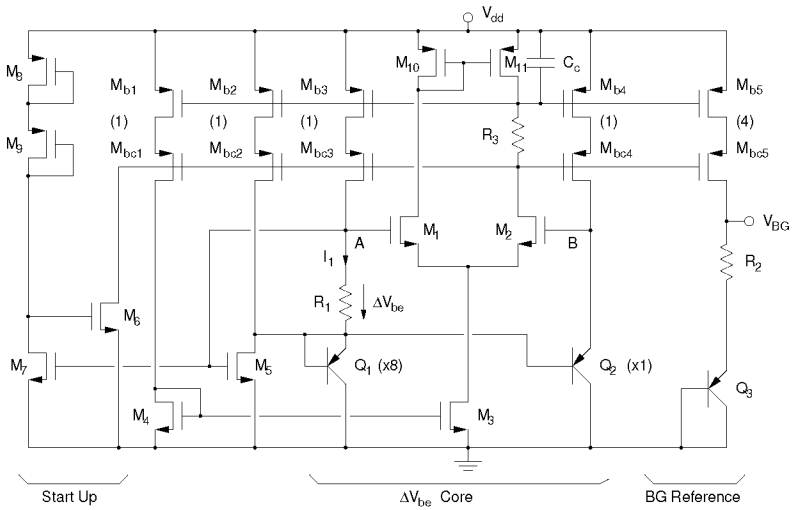


Figure 6.29: *Schematic diagram of the bandgap reference.*

6.7.3 Automatic Tuning

Due to process, temperature, and supply voltage variations, the center frequency of the channel filter can vary as much as ±20%. To guarantee the correct operation of the receiver an automatic frequency tuning control loop is therefore essential. Such a circuit is conveniently implemented by means of a phase-locked loop using a voltage-controlled oscillator realized with the same unit elements as the ones used to implement the filter [44]. By locking the frequency of the VCO to a reference frequency, and by using the same tuning current for the main filter, the center frequency of the filter is tuned to the nominal value. The accuracy of this scheme is limited by mismatch between the master (filter) and the slave (VCO) to 1–2%.

The simplified schematic of the implemented VCO is depicted in Fig. 6.30. It is a simple second-order oscillator where the inductor is simulated by a gyrator and a capacitor. To avoid using too small capacitor values its nominal oscillation frequency has been set to half the frequency of the crystal oscillator, i.e. 6.5 MHz. The nonlinear resistor

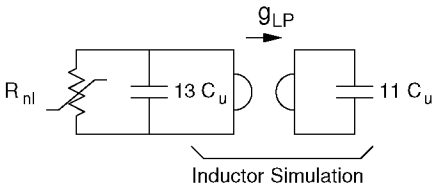


Figure 6.30: *Voltage-controlled oscillator used to implement the filter automatic frequency tuning control loop.*

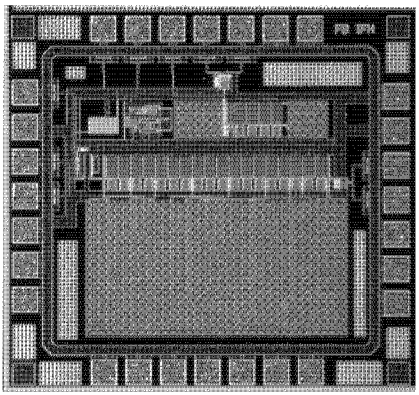


Figure 6.31: *Photomicrograph of the channel filter.*

R_{nl} has two functions: first, having a negative value for small amplitudes, it starts oscillations, and second, to limit the harmonics content of the generated signal, it limits the amplitude of oscillation to about 70% of the linear portion of the transconductor $I_{out}(V_{in})$ characteristic. Its design is based on [42].

6.7.4 Measured Performance

The channel filter test IC has been integrated without the 10 dB amplifier (this has been integrated and tested together with the front-end test IC), and for measurement purposes its output has been buffered with

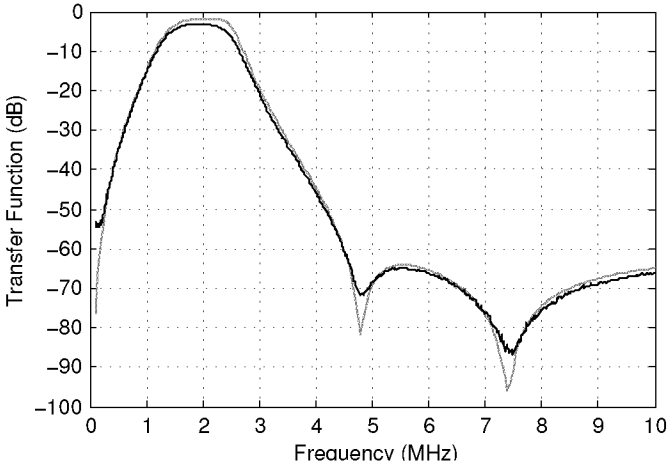


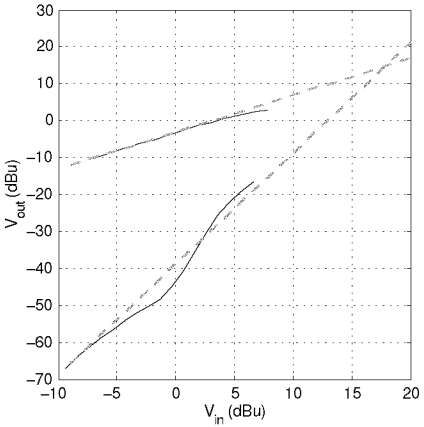
Figure 6.32: *Measured filter transfer function.*

source followers with a simulated gain of -1.9 dB. Figure 6.31 shows a photomicrograph of the IC. The lower half of the IC is occupied by the filter capacitors. The VCO is located in the upper right part of the die, while the circuit in the upper left part is the voltage reference.

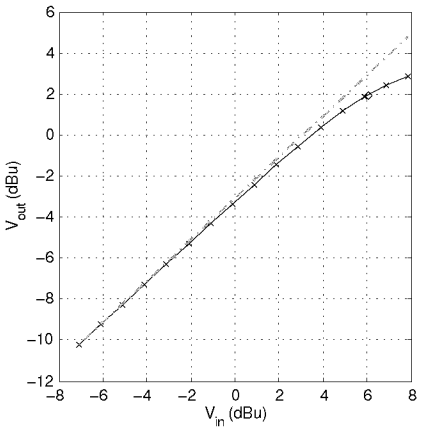
The filter has been tested at the nominal supply voltage of 1.8 V, and tuned with the help of an external potentiometer in such a way as to precisely set the VCO oscillation frequency at the nominal oscillation frequency of 6.5 MHz. The common-mode voltage of the filter has been set with the help of the on-chip bandgap reference. The voltage generated by the reference is 1.191 V. The measured transfer function (black line) is shown in Fig. 6.32 together with the simulated one (gray line). The frequency of the lowest transmission zero z_1 is 1.6% higher than the design value.

The intermodulation and compression characteristics of the circuit are shown in Fig. 6.33. The third order intermodulation has been measured with the two test tones at f_1=5 MHz and f_2=8 MHz, as specified by the Bluetooth standard. The iIP3 and iCP are 17.8 dBu and 6.1 dBu respectively.

The integrated noise (60 kHz–24 MHz) at the output of the fil-



(a) Third order intermodulation.



(b) Compression.

Figure 6.33: *Nonlinear behavior of the filter.*

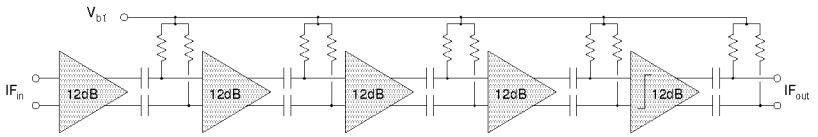


Figure 6.34: *60 dB limiting amplifier built with AC coupled amplifier cells.*

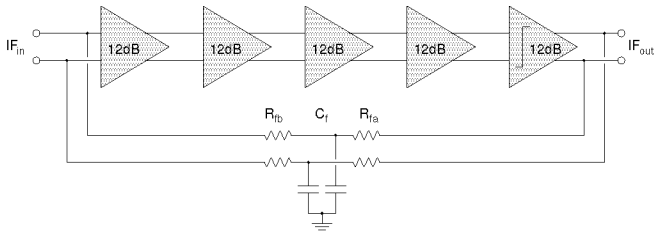


Figure 6.35: *60 dB limiting amplifier built with DC coupled amplifier cells.*

ter is 114 μVrms; no, spurious signal at the VCO frequency could be measured. The input voltage noise spectral density around 2 MHz is 76 nV/$\sqrt{\text{Hz}}$.

6.8 IF Limiting Amplifier

The principal purpose of the amplifier following channel selection is to increase the signal level to a level adequate for demodulation. In FM systems like Bluetooth, to suppress AM noise, it is customary to use limiting amplifiers. To amplify the smallest input signal to the limiting level of 6 dBu with some margin, 60 dB of gain are required. This large gain can easily be implemented by cascading several lower gain amplifiers.

The chain of low gain amplifiers can be AC or DC coupled. AC coupling the amplifiers (see Fig. 6.34) eliminate any problem having to do with the progressive build-up of offset voltages along the high

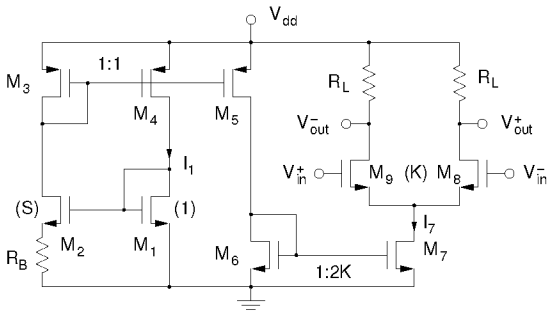


Figure 6.36: *Process, temperature, and supply voltage stable 12 dB gain amplifying cell.*

gain chain. However, due to the low IF frequency, several large coupling capacitors are needed. DC coupled stages do not require large capacitors and, as simulations have shown, generate less AM to PM conversion, but, the unavoidable DC input offset voltage of the amplifiers, if not corrected, can prevent correct operation of the amplifier. One way to remedy to this problem is shown in Fig. 6.35 [45]. The network constituted by R_{fa}, R_{fb}, and C_f reduces the low-frequency gain of the amplifier to 1, eliminating thus any problem related to offset voltages. By setting the pole of the feedback network to a sufficiently low frequency, in the band of interest the feedback network shows a high attenuation, and the amplifier provides the full open-loop gain.

For our implementation we use an hybrid solution: to avoid loading the channel filter with the feedback resistors R_{fb}, thus slightly changing its terminating impedance, we use DC coupled stages with its corresponding low-frequency feedback loop only for the last four stages. The first stage is coupled to the rest of the amplifier by 12.5 pF coupling capacitors. The four feedback resistors are 100 kΩ poly resistors, the two feedback capacitors need to be external, since their value has to be at least 1 nF.

The schematic diagram of the basic 12 dB amplifying cell together with its bias network is shown in Fig. 6.36. It is a simple differential amplifier whose gain is given by the transconductance of M_9 (g_{m9}) times R_L, and the limiting level by the tail current I_7 times R_L. The

gain of the amplifier is made process, temperature, and supply voltage stable by the constant-g_m bias network constituted by M_1–M_4. A simple analysis assuming a quadratic characteristic reveals in fact that the transconductance g_{m1} of M_1 is given by

$$g_{m1} = \frac{1}{R_B} \cdot \frac{2(\sqrt{S}-1)}{\sqrt{S}} \tag{6.29}$$

and depends only from R_B and the ratio S of the widths of M_1 and M_2. By mirroring current I_1 to the amplifying devices, and making M_8 and M_9 carry the same current *density* as M_1, the gain of the amplifier is given by the following expression

$$\frac{V_{out}}{V_{in}} = K \cdot \frac{2(\sqrt{S}-1)}{\sqrt{S}} \cdot \frac{R_L}{R_B} \tag{6.30}$$

which is only defined by *ratios*. For maximum accuracy R_B has to be of the same type as the load resistors R_L. The body effect and the drain-source impedance of the transistors introduce a small gain error, but the stability of the gain is not severely affected. The bandwidth of the amplifier is limited by the RC pole formed by the load resistors R_L and the gate-source capacitance of M_8 and M_9. The geometry of the transistors has been chosen in such a way as to obtain a bandwidth 2–3 time the IF frequency.

To ensure proper operation, a start-up circuit like the one used for the bandgap reference has been added. The design values used in our implementation are listed in Table 6.7. The simulated gain of the limiting amplifier vary between 59 dB at 80°C and 62 dB at -20°C.

Although the constant-g_m bias network has only been used in conjunction with the limiting amplifier described in this section, it can also be used to stabilize the gain of every circuit whose gain is defined by the product of a transconductance and a resistor.

6.8.1 Measured Performance

The amplifier is very compact. Its size is 200x300 μm^2, where two third of the area are occupied by the capacitors coupling the first stage of the amplifier to the following stages.

Figure 6.37 shows the gain of the amplifier measured with an input signal of -70 dBu. The output begins to saturate at an input level V_{in}

nMOS	W (μm)	L (μm)	R, I	
M_1	2x7.5	1.6	R_B	3.18 kΩ
M_2	8x7.5	1.6	R_L	7.5 kΩ
$M_{3,4,5}$	2x2.5	2	I_1	20 μA
M_6	2x2.05	1.6	I_7	80 μA
M_7	8x2.05	1.6	S	4
$M_{8,9}$	4x7.5	1.6	K	2

Table 6.7: *Design values for the 12 dB amplifying cell.*

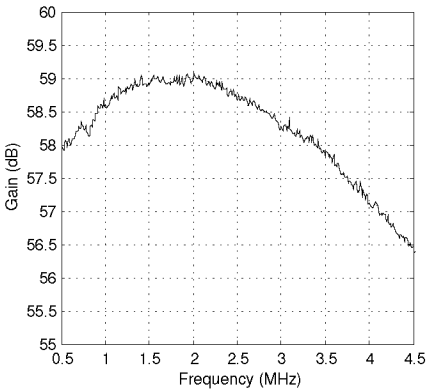


Figure 6.37: *Measured gain of the limiting amplifier.*

of -58 dBu reaching a level of 4 dBu at V_{in}=-52 dBu and 6 dBu at V_{in}=-42 dBu. The input voltage noise spectral density around 2 MHz is 7.9 nV/$\sqrt{\text{Hz}}$. All of the measurements have been performed with external feedback capacitors of 1 nF, and at the nominal supply voltage of 1.8 V.

6.9 Demodulator

Since the first practical use of frequency modulation in the thirties, many different FM demodulators have been developed [46]. A very

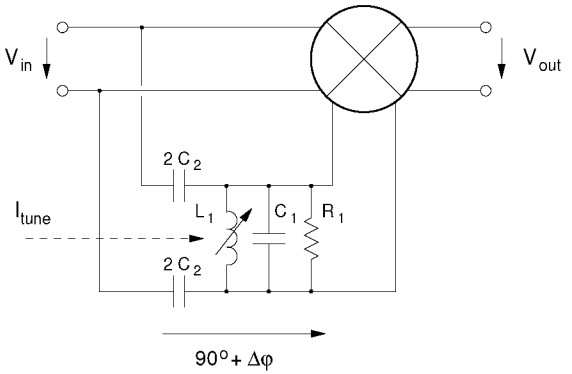


Figure 6.38: *Schematic representation of the quadrature frequency discriminator.*

simple frequency discriminator, allowing a low-voltage, low-power implementation is the so called quadrature (or delay line) discriminator depicted in Fig. 6.38. It is composed by a multiplier and by a resonator acting as a phase-shift network. The purpose of the phase-shift network is to convert the frequency modulation of the input signal to a phase modulation with a nominal phase-shift of 90° at the nominal IF frequency f_{IF}. The transmitted information can then be recovered by multiplying the input signal with the phase-shifted signal:

$$\begin{aligned} V_{out} &= K\cos(\omega_0 t)\cdot\sin(\omega_0 t+\Delta\varphi) \\ &= \frac{K}{2}\Big(\sin(\Delta\varphi)+\sin(2\omega_0 t+\Delta\varphi)\Big) \\ &\approx \frac{K}{2}\Delta\varphi \end{aligned} \tag{6.31}$$

The output signal contains, besides the demodulated signal, a component at $2f_{\mathrm{IF}}$ which has to be suppressed.

6.9.1 Phase-Shift Network

The transfer function of the phase-shift network constituted by R_1, L_1, C_1, and C_2 is

$$H(s) = \alpha \cdot \frac{\left(\frac{s}{\omega_0}\right)^2 \frac{1}{Q}}{\left(\frac{s}{\omega_0}\right)^2 + \left(\frac{s}{\omega_0}\right)\frac{1}{Q} + 1} \quad , \tag{6.32}$$

where

$$\omega_0^2 = \frac{1}{L_1(C_1 + C_2)} \tag{6.33}$$

$$Q = R_1\sqrt{\frac{C_1 + C_2}{L_1}} \tag{6.34}$$

$$\alpha = \omega_0 C_2 R_1 \tag{6.35}$$

The quality factor Q of the resonator is essentially determined by $f_{\mathrm{IF}}/2f_d$, where f_d is the frequency range for which sufficiently linear operation is required. The exact value of Q is then adjusted according to the linearity and the sensitivity requirements of the application at hand: a resonator with a low quality factor Q results in a very linear demodulator characteristic, but producing a small output signal. The use of a high Q resonator results in a higher, but more distorted output signal. Since the transmitted information is of digital nature, Bluetooth does not require a particularly linear demodulator characteristic. The maximum frequency deviation from the carrier under worst-case conditions is ±290 kHz.

The IF frequency of 2 MHz used in our receiver, calls for a resonator with a low quality factor in the range of 1–2, and opens the way to the integration of the whole demodulator, including the phase-shift network. The low Q inductor required to implement the resonator can in fact be readily simulated with the help of a gyrator and a capacitor, much in the same way as it was done to implement the channel filter. Moreover, by implementing the gyrator and the capacitors with the same unit elements as the ones used to implement the filter, the same frequency tuning loop used to tune the channel filter can also be used to tune the demodulator. The gyrator constant and the values of the components used to implement our prototype are given in Table 6.8.

C_1	$18C_u$	L_1	$C_{\text{gyr}}/g_{\text{gyr}}^2$
R_1	7.5 kΩ	C_{gyr}	$22C_u$
C_2	$29C_u$	g_{gyr}	140 μA/V
C_u	363 fF		

Table 6.8: *Components values of the demodulator phase-shift network.*

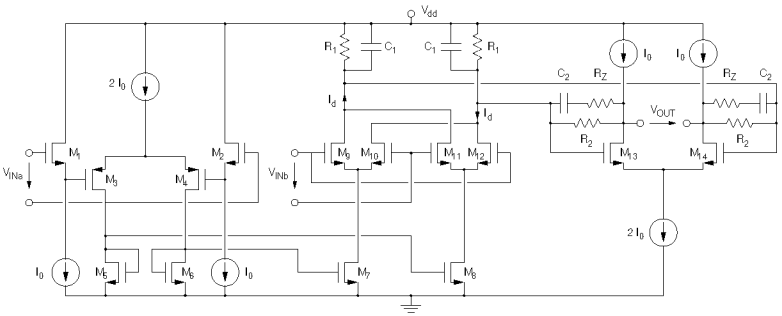


Figure 6.39: *Demodulator multiplier.*

Due to the fast transients of the input signal, and to the fact that the impedance level of the resonator is of the same order of magnitude as the output impedance of the limiting amplifier, the latter is not able to directly drive the phase-shift network. For this reason, the input impedance of the network has been increased with the help of source followers biased with a current of 400 μA.

6.9.2 Multiplier

The simplified schematic of the multiplier appears in Fig. 6.39, and consists of a modified double-balanced Gilbert cell driving a transimpedance amplifier.

The Gilbert cell is constituted by the differential pair formed by the leftmost $2I_0$ current source, M_3 and M_4, and by the switching transistors M_9–M_{12}. Due to the low supply voltage and to the high signal levels in the range of 6 dBu, instead of the usual stacked configura-

nMOS	W (μm)	L (μm)	C, R, I	
$M_{1,2}$	2.2	0.6	R_1	25 kΩ
$M_{3,4}$	8x6	0.3	R_2	40 kΩ
$M_{5,6,7,8}$	2.2	0.6	R_Z	8.1 kΩ
$M_{9,10,11,12}$	4x6	0.18	C_1	14.2 pF
$M_{13,14}$	2.2	0.6	C_2	4.72 pF
$g_{m13,14}$	0.2 mS		I_0	20 μA

Table 6.9: *Sizes of the transistors used to implement the demodulator multiplier.*

tion, the two stages have been cascaded. The output currents of the differential pair are mirrored to the switching transistors by the current mirrors M_6/M_7 and M_5/M_8. The common-mode safe operating region of input a is raised by the source-followers M_1 and M_2 to a level adequate to allow direct DC coupling of the input signal. In order to suppress any residual AM noise superimposed to the input signal, M_3 and M_4, as well as the switching transistors M_9–M_{12} are biased near weak inversion.

The demodulated output current from the multiplier is then fed to the transimpedance stage composed by M_{13}, M_{14}, R_1, R_2, R_Z, C_1, and C_2. Its transfer characteristic is given by

$$\frac{V_{out}}{I_d} = R_1 \left(\frac{1 - g_m R_2}{1 + g_m R_1} \right) \frac{1 + sC_2 \frac{R_2 + R_Z(1 - g_m R_2)}{1 - g_m R_2}}{(1 + \frac{sC_1 R_1}{1 + g_m R_1})(1 + sC_2(R_2 + R_Z))} \quad (6.36)$$

where g_m is the transconductance of M_{13} (and M_{14}). The actual core of the transimpedance is constituted by transistors M_{13} and M_{14}, and by the resistor R_2. Capacitor C_2 together with R_2 introduce a pole in the transfer function of the stage, providing some attenuation to the $2f_{\mathrm{IF}}$ by-product signal generated by the multiplier, while R_Z shifts the parasitic zero (also introduced by C_2) to a frequency much higher than the pole frequency. Resistor R_1 sets the DC operating point, and, together with C_1 provides a second pole used to further attenuate the $2f_{\mathrm{IF}}$ signal. The design values used in out prototype implementation are given in Table 6.9.

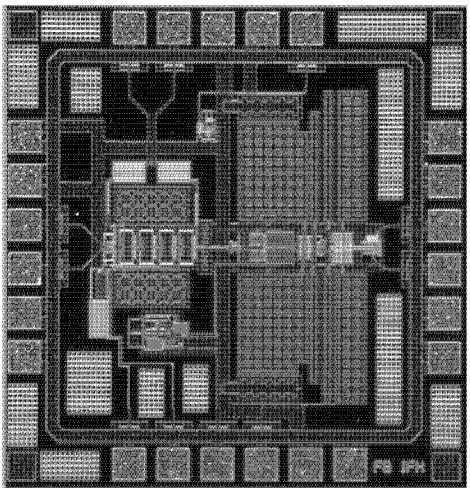


Figure 6.40: *Photomicrograph of the limiting amplifier and of the demodulator.*

6.9.3 Measured Performance

The demodulator has been integrated together with the IF limiting amplifier on a test IC. A microphotograph of the chip is shown in Fig. 6.40. The demodulator is located in the right half side of the IC, the limiting amplifier in the left half side. The circuit below the latter is a bandgap reference used to set the common-mode voltage of the gyrator.

The chip has been directly bonded on a small test PCB, and tested at the nominal supply voltage of 1.8 V. The demodulator center frequency has been tuned near to its nominal value with the help of a potentiometer. The measured characteristic appears in Figure 6.41.

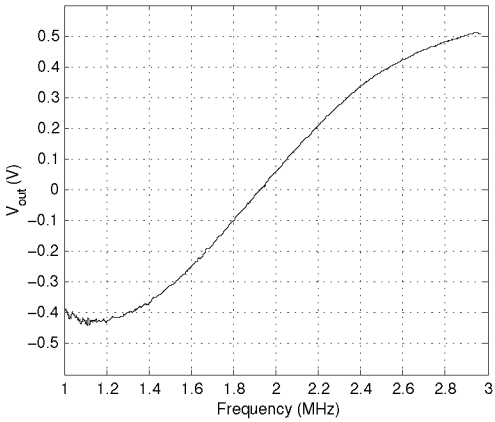


Figure 6.41: *Measured limiter/discriminator characteristic.*

Chapter 7

Design of the Transmitter

7.1 Dual-Modulus Prescaler

The dual modulus prescaler is a key component of the frequency synthesizer which is used for both, the receiver and the transmitter, and has to divide the LO frequency by 32/33. Even though it could be driven by the I or the Q signal generated by the receiver's LO phase-shifter, a second identical divide-by-two frequency divider[1] connected to the VCO has been implemented, as any asymmetry between the quadrature LO signals degrades the accuracy of the quadrature.

The block diagram of the prescaler is shown in Fig. 7.1. Like the digital LO phase-shifter, it is implemented in ESCL logic. The prescaler consists of a synchronous divide-by-4/5, followed by an asynchronous divide-by-8 divider. To reduce power consumption, the two parts have been optimized separately following the design procedure described in section 6.4.2. To ensure a high production yield, the prescaler has been designed to work at a frequency 40% higher than required at nominal conditions. FF_1–FF_3 utilize a switching current I_0 of 180 μA and resistive loads; Flip-Flops FF_4–FF_6 and gates G_1 and G_2 a switching

[1] This divide-by-two frequency divider can thus be considered the first stage of a 64/66 dual modulus prescaler

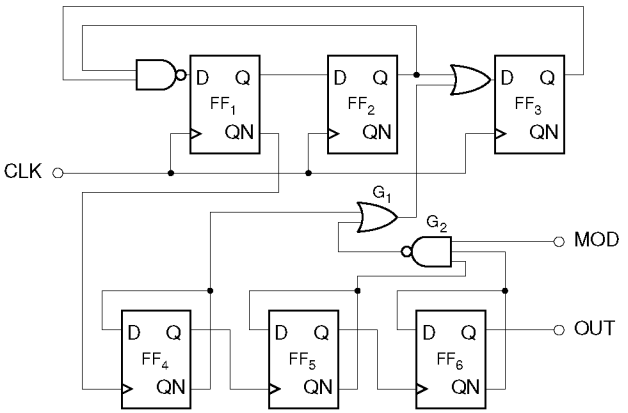


Figure 7.1: *Block diagram of the dual modulus prescaler.*

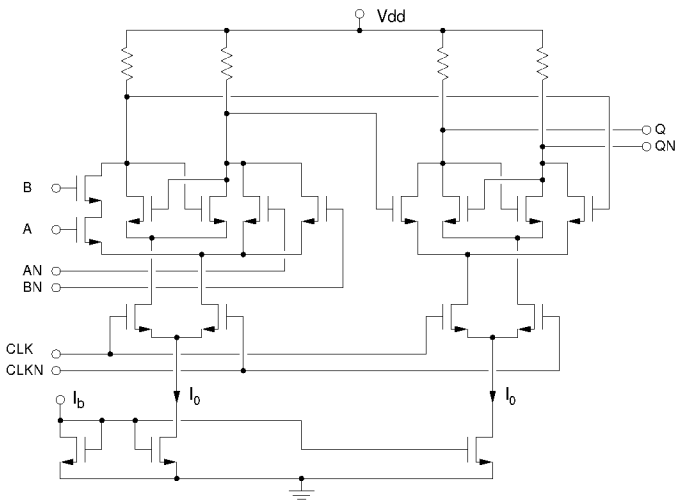


Figure 7.2: *Schematic of an ESCL Flip-Flop with embedded input gate.*

current of 90 μA and pMOS transistors operated in the triode region as loads. To reduce further the total current consumption, the NAND and OR gates driving Flip-Flop FF_1 and FF_3 have been embedded into the input stage of the Flip-Flop themselves (Fig. 7.2). The total current required by the 32/33 dual-modulus prescaler is 1.8 mA.

7.1.1 Measured Performance

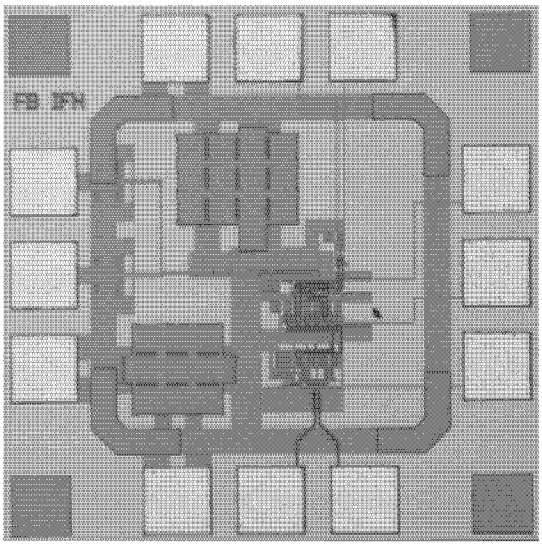


Figure 7.3: *Photomicrograph of the prescaler (including divide-by-two frequency divider).*

A photomicrograph of the prescaler also including the divide-by-two frequency divider is shown in Fig. 7.3. The measurements have been made on an unpackaged chip directly bonded on a printed circuit board at the nominal supply voltage of 1.8 V. The input port is resistively terminated to 50 Ω and driven differentially (with the help of a 3 dB/180° power splitter).

The maximum operating frequency with $P = 33$ and an input signal of 0 dBu is 8.4 GHz. The minimum required input signal as a function

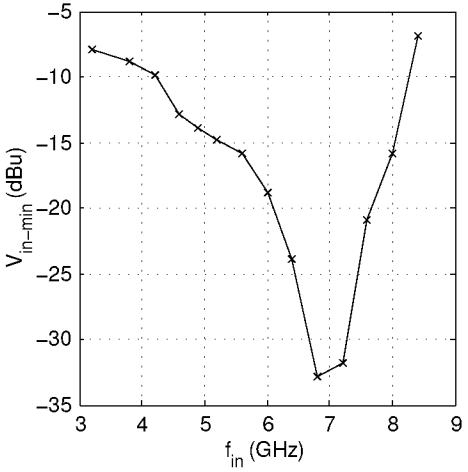


Figure 7.4: *Measured prescaler's minimum input amplitude as a function of frequency.*

of frequency is shown in Fig. 7.4. At the frequency band of interest around 4.9 GHz, the minimum required input signal is -13 dBu. The same figure also shows the self oscillating frequency of 7 GHz of the prescaler. In fact, with no input signal, every prescaler together with its stray capacitances form a relaxation oscillator.

7.2 Power Amplifier

The nominal power to be delivered by the amplifier is 2 dBm. The amplifier is driven by the second output port of the divide-by-two frequency divider also driving the prescaler. The input signal is therefore differential with a relatively high amplitude of about 350 mV. However, to avoid overloading the divider, the input impedance of the amplifier must be sufficiently high. The output of the amplifier on the contrary has to be single-ended with an output impedance of 50 Ω.

On the one hand, it would be convenient to perform the differential to single-ended conversion at the output node of the amplifier since

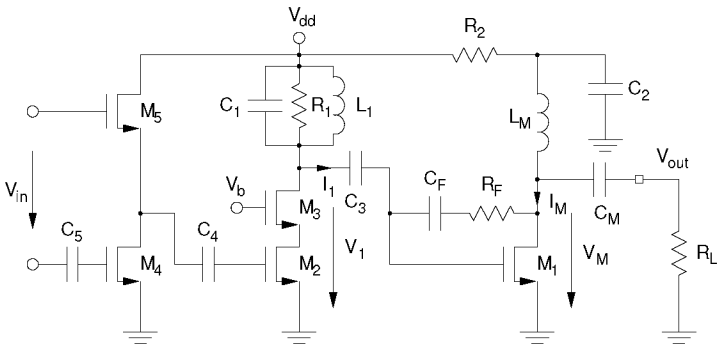


Figure 7.5: *Simplified schematic of the power amplifier.*

this would result in an amplifier injecting little noise into the power lines and the substrate, insensitive to noise generated by other circuits, and generating only odd order harmonics. On the other hand, to implement an efficient differential output stage exploiting the maximal possible voltage swing, a matching network (or transformer) with large and lossy spiral inductors and therefore having a large insertion loss would be needed. Since during transmission the receiver is inactive, and due to the stringent power consumption requirements, we have decided to implement a single-ended output stage requiring smaller and therefore better inductors, and to implement the differential to single-ended conversion right at the input of the amplifier.

The implemented amplifier is class-AB. Although more efficient, a class-C approach has been discarded since it provides less gain, and the realization of a well controlled 50 Ω output impedance without an output resistor is quite problematic.

The simplified schematic of the implemented amplifier (without bias network) is shown in Fig. 7.5. For maximal flexibility, the three stages of the amplifier are AC coupled with high quality MIM capacitors. The purpose of the input stage is to convert the differential input signal to a single-ended signal and to realize the required high input impedance. The stage is composed by a non-inverting source-follower (M_5) connected to the positive pole of the input port, and stacked on top of an inverting common-source amplifier (M_4) connected to the negative

pole of the input port. Due to the body-effect, the gain of the source-follower is slightly less than one, while the gain of the common-source is given by the transconductance of M_4 divided by the transconductance of M_5 and has been set to -1. The transistors have a transconductance of 6 mS, and draw 1 mA.

The second stage is constituted by M_2, M_3, L_1, C_1, and R_1 and provides part of the amplification. Cascode transistor M_3 is used to reduce the effect of the Miller capacitance and therefore increase the bandwidth of the first stage. L_1 tunes out the parasitic drain-bulk capacitance of the cascode stage and the gate-source capacitance of M_1. The purpose of C_1 is twofold. First, it is used to precisely set the resonance center frequency which otherwise would be set by parasitic capacitances, and second, it is used to reduce the value of L_1.

The gain of the stage is given by the transconductance of M_2 times the parallel connection of R_1, the input impedance of the third stage Z_{in}^T (see below), and the drain-source impedance of the cascode stage. The nominal bias current is 3 mA, and, at the nominal output power level, the stage works in class-AB and provides 8 dB of gain. If needed, the gain of the whole amplifier can be adjusted without affecting the input and output impedances by changing the gate bias voltage of M_2.

The last stage is a transimpedance amplifier and, besides contributing the rest of the gain, defines the output impedance of the amplifier. The stage is composed by M_1, R_F, and C_F. C_F is a coupling capacitor used to increase the flexibility by the choice of overdrive voltage, transconductance, and bias current of M_1. An important point to remark is that since the used technology has been developed to work with a supply voltage of 1.8 V, to avoid damaging the device, the maximal drain-source voltage of a transistor should not exceed this value by a too large amount. For this reason the DC potential at the drain of M_1 is lowered to 1.3 V using resistor R_2. C_2 is a decoupling capacitor used to short R_2 at signal frequencies.

To minimize the current required by the stage to deliver the nominal power, the 50 Ω load impedance R_L is raised to 130 Ω (R_L^M) by the matching network formed by C_M and L_M. At this impedance level, the voltage swing at the drain of M_1 is 720 mV optimally exploiting the safe operating region of the transistor, while always keeping M_1 in saturation. The design equations for the voltage gain, the input, and

the output impedance of the stage derived by linear analysis are:

$$A_V^T = \frac{V_M}{V_1} = \frac{R_L^M(1 - g_{m1}R_F)}{R_F + R_L^M} \tag{7.1}$$

$$Z_{in}^T = \frac{V_1}{I_1} = \frac{R_F + R_L^M}{1 + g_{m1}R_L^M} \tag{7.2}$$

$$Z_{out}^T = \frac{V_M}{I_M} = \frac{R_F + R_1}{1 + g_{m1}R_1} \tag{7.3}$$

where g_{m1} is the transconductance of M_1. Since at the nominal output power the stage operates in class-AB, Eq. (7.1) overestimate somewhat the actual gain. Due to the reciprocity of the output matching network, to realize the 50 Ω output impedance, Z_{out}^T has to be set to 130 Ω. The output matching is also slightly worsened by the class-AB operation of the device. The nominal bias current of the stage is 4 mA.

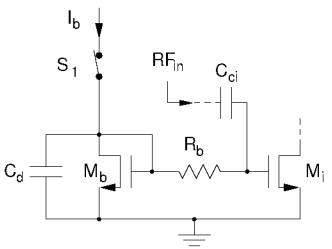


Figure 7.6: *Power amplifier bias network.*

The topology of the bias network used to set the operating point of the three stages is depicted in Fig. 7.6. It is a simple current mirror where M_i represents the amplifying transistor (M_1, M_2, or M_4), and R_b is used to decouple the bias from the signal path while causing minimal loading. By opening switch S_1, the transistors are shutdown thus deactivating the amplifier. The purpose of C_d is twofold. First, it filters any noise coming from the bias network, and second, it slows down the turn-on transient thus reducing the emission of spurious signals during ramp-up. To improve the signal attenuation in the off state, we use two further switches implemented with two relatively small pMOS transistors (W=12.5 μm, L=0.18 μm) connected in series with the gates of

nMOS	W (μm)	L (μm)	g_m (mS)	I_d (mA)
M_1	32x2.5	0.18	31	4
M_2	192x2.5	0.18	42	3
M_3	192x2.5	0.18	42	3
M_4	6x2.5	0.18	6	1
M_5	6x2.5	0.18	6	1

(a) Transistor parameters.

R, L, C			
R_F	1 kΩ	C_F	0.69 pF
R_1	390 Ω	C_1	0.1 pF
R_2	80 Ω	C_2	10 pF
L_M	5.2 nH	C_M	0.8 pF
L_1	5.6 nH	C_3	1.38 pF
C_5	0.69 pF	C_4	2.76 pF

(b) Passive component values.

Table 7.1: *PA design values.*

M_4 and M_5 (Fig. 7.5).

The values of the components and the sizes of the transistors are summarized in Table 7.1. When the output of the amplifier is connected to the input of the LNA as described in Section 6.3, besides adding a switch in series with L_M (as shown in Fig. 6.4), the value of L_M has to be reduced from 5.2 nH to 3.9 nH.

7.2.1 Measured Performance

For test purposes the amplifier has been integrated as a stand-alone circuit (without antenna switch). A photomicrograph of the chip is shown in Fig. 7.7. The input of the amplifier has been resistively matched to 50 Ω, and driven differentially with the help of an RF transmission line transformer (M/A-COM ETC1-1-13).

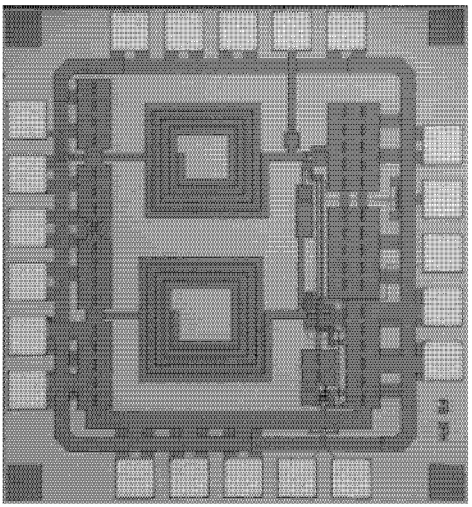


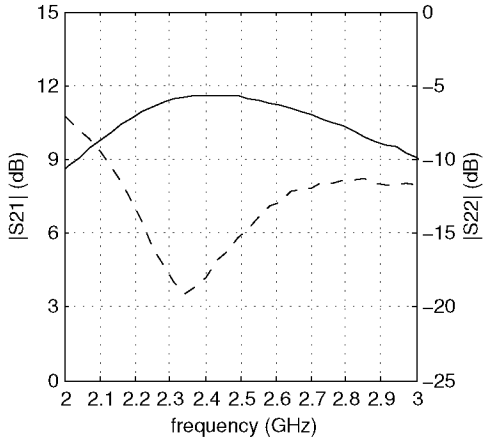
Figure 7.7: *Photomicrograph of the power amplifier.*

Figure 7.8a shows the gain and the output matching as a function of frequency. In the band of interest the amplifier shows good output matching with an $|S_{22}|$ better than -15 dB.

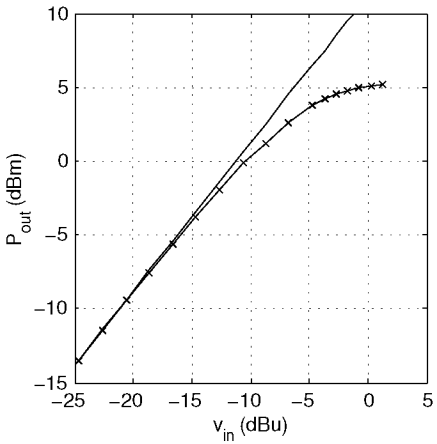
The compression characteristic of the amplifier is shown in Fig. 7.8b. The output 1 dB compression point is 1.48 dBm (-9.75 dBm at the input). At the nominal input signal level of about 0 dBu the amplifier is working in class-AB as expected, delivering 5 dBm into a 50 Ω load. By turning off the amplifier, the output power is reduced to -64.4 dBm. This low power level does not cause any saturation problem to the receiver. In addition, since part of this power is due to the parasitic coupling between input and output bond wires, this power level can be considered a worst case value.

7.3 Crystal Oscillator

The voltage controlled crystal oscillator (VCXO) generates the 13 MHz reference frequency for the PLL, and provides the low-frequency mod-



(a) Gain and output matching.



(b) Compression characteristic.

Figure 7.8: *Measured power amplifier performance.*

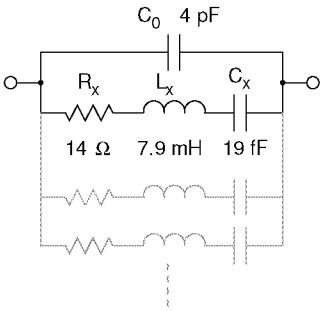


Figure 7.9: *Equivalent circuit of a crystal unit.*

ulation path for the two-point modulator.

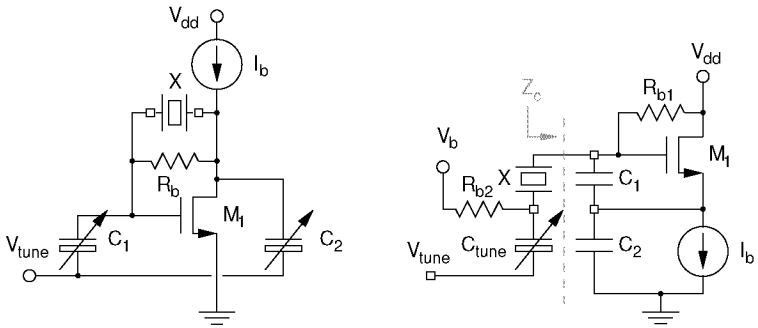
Figure 7.9 shows the equivalent circuit of a crystal unit and the parameters of the used device. C_x, L_x and R_x are the so-called motional capacitance, motional inductance and equivalent series resistance, and their values are determined by the mechanical characteristics of the crystal. C_0 is the so-called parallel capacitance and is determined by the parasitic capacitances of the crystal electrodes and of the package. The other elements drawn in gray represent higher order modes and spurious resonances of the crystal. These resonances can not be completely suppressed, but their quality factor is usually made much lower than the quality factor of the fundamental mode by the manufacturer.[2]

The oscillation frequency of a parallel mode crystal oscillator is a function of the capacitance C_L loading the crystal, and can be calculated with the following formula:

$$f_p = \frac{1}{2\pi\sqrt{L_x C_x}} \left(1 + \frac{C_x}{2(C_0 + C_L)}\right) \tag{7.4}$$

The load capacitance C_L required to obtain the nominal oscillation frequency is specified by the manufacturer. From (7.4) it is apparent that to implement a VCXO with wide tuning range, the crystal should have a large C_x, a small C_0, and requires a small load capacitance C_L. Since the maximum achievable C_x/C_0 ratio is limited by physics, the only

[2]This is obviously not true for overtone crystal units which are designed to be used at an higher order mode.



(a) Pierce oscillator.

(b) Colpitts oscillator.

Figure 7.10: *Simplifier schematic of the implemented VCXO.*

way to increase the tuning rage is by choosing a crystal requiring a small C_L.[3] For our design we use an AT cut fundamental mode crystal for telecom applications requiring a load capacitance C_L of 10 pF. To cover the tuning range necessary to properly modulate the oscillator, C_L must vary between 8.3 pF and 11.5 pF. This change in capacitance can readily be realized with integrated accumulation mode nMOS varactors.

7.3.1 Implemented Oscillators

Figure 7.10 shows the simplified schematic of the two voltage controlled crystal oscillators realized for this project: a Pierce and a Colpitts oscillator. Both are variations of the so-called three-point oscillator [47]; their design is therefore very similar. To minimize the critical transconductance g_{mc} required to start oscillation (and thus minimize current) of a three-point oscillator C_1 and C_2 should have the same value $C_1 = C_2 = C_{opt}$.

[3]The tuning range of a crystal oscillator can be further increased by resonating C_0 with an inductor. This, besides requiring a large external inductor, introduces other spurious resonances.

Pierce Oscillator

The heart of a Pierce oscillator pumping the power necessary to start and maintain oscillations is transistor M_1. In the steady-state oscillation regime, the voltage amplitude of the oscillation at the gate and the drain of this transistor (to first order) have the same amplitude and opposite sign. Node V_{tune} is therefore an AC ground, and the effective capacitance in parallel to the crystal is $C_{opt}/2$. The nominal value of the varactors C_1 and C_2 must therefore be twice C_L, i.e. 20 pF.

Resistor R_b has two functions. First, it is used to bias the gate of M_1, and second, it lowers the gain of the "parasitic" amplifier formed by the circuit at low frequencies: since the modulating signal is applied to V_{tune}, the same signal is coupled to the gate of M_1 by varactor C_1. At the modulation frequency the crystal has a very high impedance, and the circuit forms a common source amplifier boosting the modulating signal. If the gain is too large, the drain of M_1 clips to ground or the supply voltage, corrupting the 13 MHz oscillation. The choice of R_b is therefore a compromise between low gain and high resonator quality factor. The value used in our design is 8 kΩ.

Since the transconductance g_m for a given bias current is maximum in weak inversion, M_1 has been made large. In addition, to raise the drain-source impedance its gate is longer than the minimum design rule (W=56x2.5 μm, L=0.5 μm). The bias current I_b of the oscillator is regulated by a detector in such a way as to keep the oscillation across the varactors 240 mV_{pp}. Under nominal conditions the current stabilizes at 83 μA.

Colpitts Oscillator

The effective capacitance loading the crystal in a Colpitts oscillator is given by the series connection of C_1, C_2 and C_{tune}. Therefore, to realize a wide tuning range with a reasonably small varactor capacitance variation, C_1 and C_2 should be much larger than C_{tune}. On the other hand, since the real part of the impedance provided by the Colpitts configuration Z_c is

$$\Re(Z_c) = -\frac{g_m}{\omega_0^2 C_1 C_2} \tag{7.5}$$

large capacitors C_1 and C_2 require a large transistor transconductance g_m and therefore a higher current. As a compromise we have chosen a value of 100 pF. The varactor has then to provide a capacitance between 10.1 pF and 14.7 pF with a nominal value of 12.5 pF. Due to their large value, C_1 and C_2 are external to the chip.

Here the modulating signal applied to V_{tune} is also coupled to the gate of the M_1, but, with C_{tune} in series with the crystal, the signal reaching the gate is very small. In addition, since at the modulating frequency the Colpitts configuration forms a source-follower, there is no risk of clipping. For this reason, when modulated, we expect the Colpitts oscillator to perform better than the Pierce oscillator.

M_1 has a size of W=20x10 μm, L=0.18 μm. Resistor R_{b1} is used to bias the gate of M_1, and has a nominal value of 40 kΩ, while resistor R_{b2} sets the center of the tuning voltage at 0.7 V. To avoid limiting the modulation bandwidth of the oscillator with the input network constituted by C_{tune} and R_{b2}, the value of the latter has been set to 17 kΩ. The bias current I_b is regulated by a detector like the one used for the Pierce oscillator in such a way as to keep the swing across the varactor 240 mV_{pp}. Under nominal conditions the required current is 790 μA.

7.3.2 Varactors

As mentioned before, the varactors required to modulated the frequency of the oscillators have been implemented as on-chip accumulation mode nMOS varactors similar to the ones used for the VCO. Here, however, each varactor has been split into a principal varactor C_p, and a weighted array of smaller varactors C_1–C_N where the capacitance of element k is given by

$$C_k = C_1 \cdot 2^{k-1} \tag{7.6}$$

Each one of the elements of this array can be connected to or isolated from C_p with the help of an nMOS switch S_k (see Fig. 7.11). The center frequency of the oscillator can thus be tuned without having to change the DC potential of the modulating signal by switching in or out elements from the array. Since the initial center frequency of the transmitter has to be within $\pm$75 kHz from the nominal channel frequency, the reference frequency generated by the crystal oscillator

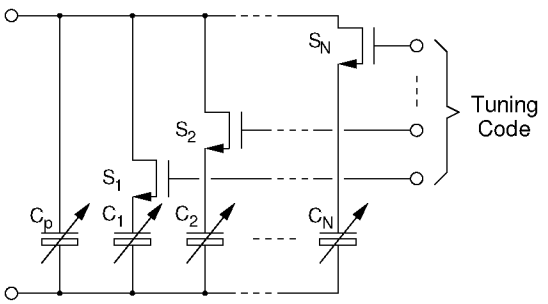


Figure 7.11: *Weighted array of nMOS varactors used to set the center frequency of the crystal oscillators.*

has to be accurate to at least ±30 ppm. The frequency step caused by switching element C_1 must be smaller than this.

The varactors used for the Pierce oscillator are characterized by C_p=16 pF, N=4, and C_1=0.53 pF. The array allows to change the mean varactor capacitance from 16 pF to 24 pF. The sizes of C_p and C_1 are W=2400x2 μm, L=0.5 μm, and W=80x2 μm, L=0.5 μm respectively. The frequency step caused by switching C_1 is about 16 ppm. For the Colpitts oscillator C_p=9 pF (W=1320x2 μm, L=0.5 μm), N=4, and C_1=0.4 pF (W=60x2 μm, L=0.5 μm). The mean varactor capacitance ranges from 9 pF to 15 pF. The smallest frequency step is about 21.8 ppm.

7.3.3 Amplitude Detector

The simplified schematic of the detector used to regulate the amplitude of the crystal oscillators is shown in Fig. 7.12. The core of the circuit is constituted by the two identical *asymmetric* differential stages M_1-M_2 and M_3-M_4, and by the current mirror M_5-M_6. Suppose for a moment $\alpha = 0$ (i.e. $I_{set} = 0$), then when $V_{in} = 0$ transistors M_1 and M_3, being A times narrower than transistors M_2 and M_4, conduct $1/(A+1)$ of the respective tail currents. These currents are summed and mirrored to the drain of M_6 where they are subtracted from the rest of tail currents flowing through M_2 and M_4. The net difference current I_{det} with no

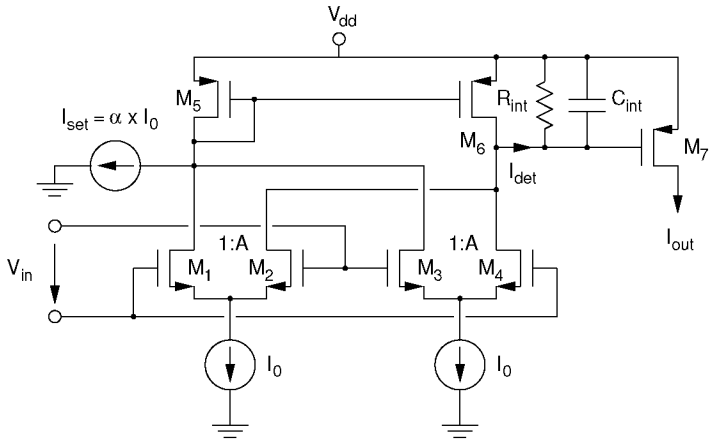


Figure 7.12: *Simplified schematic of the detector.*

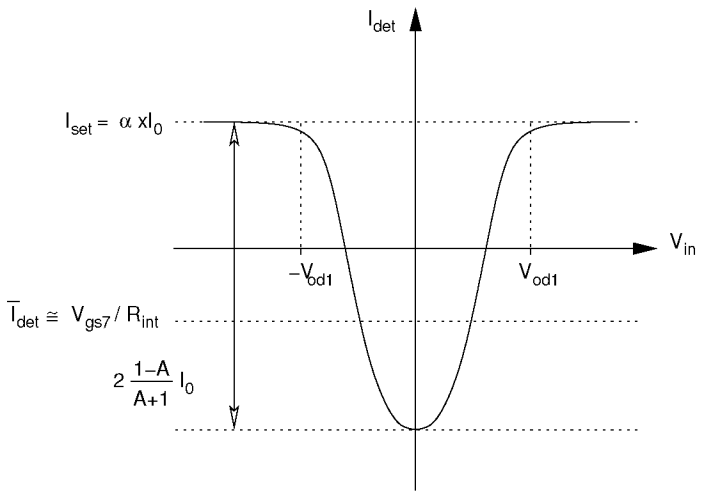


Figure 7.13: $I_{det}(V_{in})$ *detector characteristic.*

MOS	W (μm)	L (μm)	I, R, C	
M_1	2x10	0.18	C_{int}	100 pF
M_2	16x10	0.18	R_{int}	100 kΩ
M_3	2x10	0.18	I_0	20 μA
M_4	16x10	0.18	α	0.7
M_5	6.6	0.5	A	8
M_6	6.6	0.5		
M_7	4x6.6	0.5		

Table 7.2: *Detector design values.*

input signal is thus

$$I_{det}(V_{in} = 0) \quad = \quad 2 \cdot \frac{1 - A}{A + 1} \cdot I_0 \tag{7.7}$$

By applying a positive input signal, the drain current of M_1 is reduced from an already small fraction of I_0 to nearly zero, but M_3 begins to conduct a considerable part of the tail current resulting in a net increase of I_{det}. At large input signals, the tail currents flow entirely through M_2 and M_3 resulting in a difference current I_{det} of zero. For negative input signals the circuit behaves in a similar way, resulting in a symmetric $I_{det}(V_{in})$ characteristic. The slope of the characteristic is determined by the overdrive voltage of M_1 and M_3.

The current source I_{set} does not change the fundamental behavior of the circuit, it simply shifts the whole characteristic by I_{set}, allowing I_{det} to assume positive values (see Fig. 7.13).

The filter constituted by R_{int} and C_{int} averages I_{det}, provides the gate-source voltage for the output transistor M_7, and determines the dynamics of the detector. I_{out} is the current used to bias the oscillators.

The differential signal of the Pierce oscillator is coupled to the detector by a capacitive voltage divider attenuating the signal by a factor of two (C_{div} = 1.25 pF). The Colpitts signal is capacitively coupled to the positive input pole of the detector, while the negative pole lie at AC ground.

Table 7.2 summarizes the values of the components and the sizes of the transistors used in our prototype.

7.3.4 Amplitude Dynamics

In applications where the frequency of the crystal oscillator gets modulated (like in a two-point modulator), it is important to study the details of the dynamics of the amplitude of oscillation. The varactor capacitance change necessary to frequency modulate the oscillator signal cause in fact also an unwanted amplitude modulation. The response of the circuit to this perturbation has to be overcritically damped.

On the one hand the nonlinear operation of oscillators makes linear analysis methods useless for the analysis of the amplitude transient; on the other hand the very high quality factor of quartz resonators is responsible for a very slow oscillation build up and makes its numerical computation a difficult task. In particular, a direct SPICE-like transient simulation requires the calculation of tenth of thousand periods of oscillation and is therefore very time consuming, precluding the possibility of a "study by simulation" approach using a circuit simulation program.

An approximate method allowing the analysis of nonlinear systems having a slowly varying periodic solution in a short computer time is the so-called Method of Averaging, sometimes also called Slowly Varying Function Method [48, 49]. This method is applicable to systems described by an integro-differential equation of the following form:

$$\frac{d^2}{dt^2}v_1(t) + \omega_0^2 \cdot v_1(t) = \epsilon \cdot f(v_1, dv_1/dt, \int v_1 dt, \ldots) \tag{7.8}$$

By transforming this equation into a system of first order differential equations we obtain

$$\begin{cases} \frac{d}{dt}v_1(t) = v_2(t) \\ \frac{d}{dt}v_2(t) + \omega_0^2 \cdot v_1(t) = \epsilon \cdot f(v_1, v_2, \ldots) \end{cases} \tag{7.9}$$

For $\epsilon = 0$ this system describes a harmonic oscillator, and $v_1(t) = V_p \cos(\omega_0 t + \Phi)$ where V_p and Φ are constants. Therefore, if ϵ is small, we might expect a similar looking solution, and we assume that the solution to (7.9) is given by

$$\begin{cases} v_1(t) = v_p(t)\cos(\omega_0 t + \phi(t)) \\ v_2(t) = -\omega_0 v_p(t)\sin(\omega_0 t + \phi(t)) \end{cases} \tag{7.10}$$

where $v_p(t)$ and $\phi(t)$ are slowly varying functions. By applying this variable transformation, (7.9) can be transformed into the following equivalent system

$$\begin{cases} \frac{d}{dt}v_p(t) = -\frac{\epsilon}{\omega_0} f(v_p, \phi, \ldots) \sin(\omega_0 t + \phi(t)) \\ \frac{d}{dt}\phi(t) = -\frac{\epsilon}{\omega_0} f(v_p, \phi, \ldots) \cos(\omega_0 t + \phi(t)) \end{cases} \tag{7.11}$$

Now, to simply the solution of the system, we make the following assumption: if $v_p(t)$ and $\phi(t)$ are slowly varying functions, then their value does not change much over a period of the solution $T = 2\pi/\omega_0$; therefore we replace the right hand sides of (7.11) with their averages over one period

$$\begin{cases} \frac{d}{dt}v_p(t) \approx -\frac{\epsilon}{\omega_0 T} \int_t^{t+T} f(v_p(t), \phi(t), \ldots) \sin(\omega_0 \tau + \phi(t)) d\tau \\ \frac{d}{dt}\phi(t) \approx -\frac{\epsilon}{\omega_0 T} \int_t^{t+T} f(v_p(t), \phi(t), \ldots) \cos(\omega_0 \tau + \phi(t)) d\tau \end{cases} \tag{7.12}$$

The advantage of (7.12) over (7.11) is constituted by the fact that fast variations have been eliminated from the system of differential equations, and therefore the system can be solved in a short computer time with standard numerical methods.

Application of this method to the integro-differential equation describing the Pierce oscillator (neglecting the parallel capacitance C_0 of the crystal) results in the following system

$$\begin{cases} \frac{d}{dt}v_p(t) = -\frac{1}{2L_x}[R_x - \frac{g_{m1}(v_p(t))}{\omega_0^2 C_1 C_2}]v_p(t) \\ \frac{d}{dt}\phi(t) = 0 \end{cases} \tag{7.13}$$

where $g_{m1}(v_p)$ is the large signal transconductance of the transistor which, for a device having an exponential characteristic like a MOSFET in weak-inversion or a bipolar transistor, is given by [50]

$$g_{m1}(v_p) = \frac{I_d}{nU_T} \cdot \frac{I_0(v_p/(nU_T))}{v_p/(nU_T) I_1(v_p/(nU_T))} \tag{7.14}$$

Here $I_k(\cdot)$ are the modified Bessel functions of the first kind of order k, n is the transistor slope factor, I_d is its bias current, and U_T stands for kT/q.

Since the detector is driven by the slowly varying oscillator signal, the same averaging method can also be applied to the equation describ-

ing its behavior (assuming $\frac{1}{R_{int}C_{int}} \ll \omega_0$):

$$\begin{aligned} \frac{d}{dt}v_{gs7} \quad \approx \quad & -\frac{v_{gs7}}{R_{int}C_{int}} \\ & -\frac{R_{int}}{R_{int}C_{int}}\frac{1}{T}\int_t^{t+T} i_{det}(v_p(t)\cos(\omega_0\tau+\phi(t)))d\tau \end{aligned} \tag{7.15}$$

To complete the description of the servo system we have assumed a quadratic characteristic for M_7 of the detector, and its $I_{det}(V_{in})$ characteristic has been described with the help of the following approximation

$$I_{det}(V_{in}) = I_0[\alpha + \tanh(V_{in}/V_r - V_{os}) + \tanh(-V_{in}/V_r - V_{os}) \tag{7.16}$$

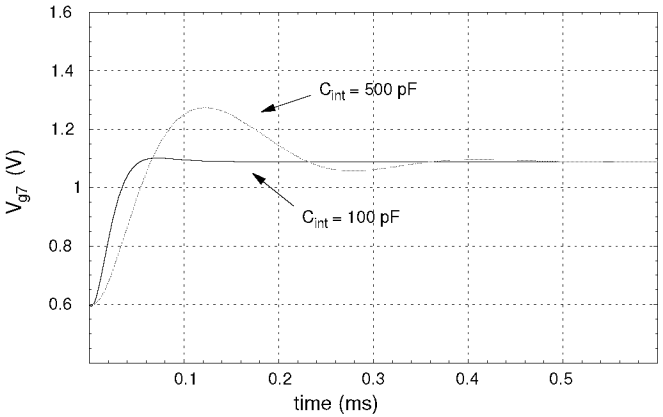
where V_{os} and V_r are fitting parameters depending from the transistor ratio A and the overdrive voltage of M_1.

Figure 7.14a shows the gate voltage of M_7 during the start-up transient for two values of C_{int}. The curve in black shows the transient for $C_{int} = 100$ pF, while the curve in gray represents the transient for $C_{int} = 500$ pF (in both cases $R_{int} = 100$ kΩ). From this figure its apparent that a large time constant for the filter of the detector cause an underdamped transient. By reducing this time constant the overshooting can be eliminated, with $C_{int} = 100$ pF being the critical case.[4]

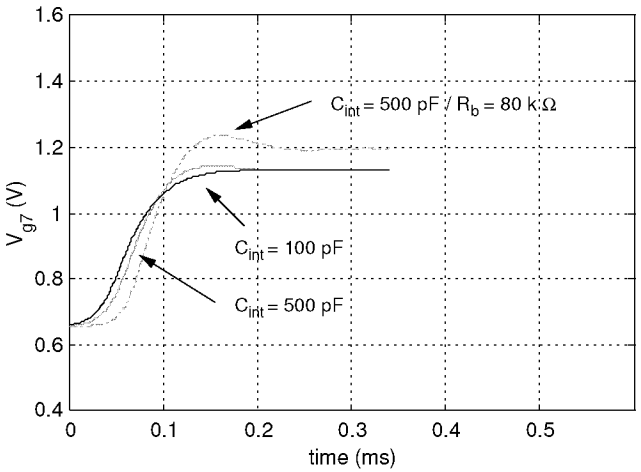
Figure 7.14b shows the transient simulation of the amplitude regulated oscillator calculated with Spectre and the full transistor models. The curves in black and gray are the counterparts of the curves represented in Fig. 7.14a. The dot-dashed curve has also been calculated with $C_{int} = 500$ pF, but the bias resistor R_b has been raised from 8 kΩ to 80 kΩ. These curves suggest that, despite the use of a rough approximation to represent the characteristic of the detector and a very simple transistor model, the Method of Averaging gives a good approximation of the dynamic behavior of the system, most of the error being introduced by the fact that the losses introduced by R_b and the output impedance of the transistor have been neglected.

Whereas the simulation of a transient time of 0.6 ms with the Method of Averaging requires a couple of seconds, the simulation of

[4]Since we are analyzing a nonlinear system, the terms underdamped, overdamped, and critically damped are used somewhat improperly. Their meaning is anyway representative for the responses observed.



(a) Method of Averaging.



(b) Spectre.

Figure 7.14: *Simulated start-up transient of the Pierce oscillator.*

0.4 ms with Spectre on the same machine (a Sun Ultra 60 workstation with 1 GB of RAM) requires about 40 minutes.

7.3.5 Modulation Bandwidth of the VCXOs

Differently from non-crystal controlled VCOs, which can be modulated at very high rates, the modulation bandwidth of VCXOs is restricted to relatively low values by the physical characteristics of the crystal. The spectrum of the signal generated by a modulated voltage controlled oscillator includes in fact several components. In case of a parallel resonant VCXO, the phase and the amplitude of those components around the series and the spurious resonances of the crystal are changed by the electrical characteristics of the crystal itself, resulting in a distorted output signal. Similarly, the spectrum of a series resonant VCXO is modified by the parallel and the spurious resonances of the crystal. Consequently a very rough estimation of the modulation bandwidth can be made by computing the difference between series and parallel resonance of the crystal, which for the used crystal is 9 kHz.

7.3.6 Measured Performance

Figure 7.15 shows a photomicrograph of the oscillators. The Pierce oscillator is located on the left half side of the picture, while the Colpitts oscillator lies on the right half side. The three varactor arrays are clearly visible on the top half side of the figure.

The tuning characteristic of the two oscillators is shown in Fig. 7.16. Whereas the tuning code necessary to set the oscillation frequency as close as possible to 13 MHz at the central tuning voltage for the Pierce oscillator is 0101,[5] near to the central value; the tuning code necessary for the Colpitts oscillator is 0000, suggesting the presence of a somewhat higher than expected parasitic capacitance. The oscillation frequency of the Colpitts oscillator as a function of the tuning code, and at a fixed tuning voltage of 0.7 V is shown in Fig. 7.17.

The amplitude of oscillation at the gate and at the drain of the Pierce oscillator are 280 mV_{pp} and 225 mV_{pp} respectively. The amplitude of oscillation across the varactor of the Colpitts oscillator is 231 mV_{pp}.

[5] 0: switch open; 1: switch closed.

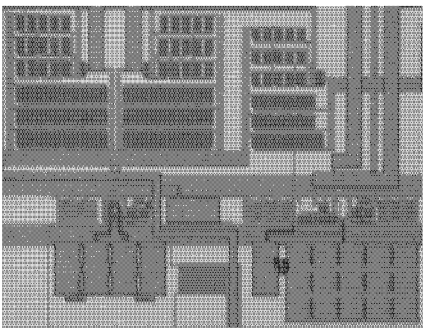


Figure 7.15: *Photomicrograph of the amplitude regulated crystal oscillators.*

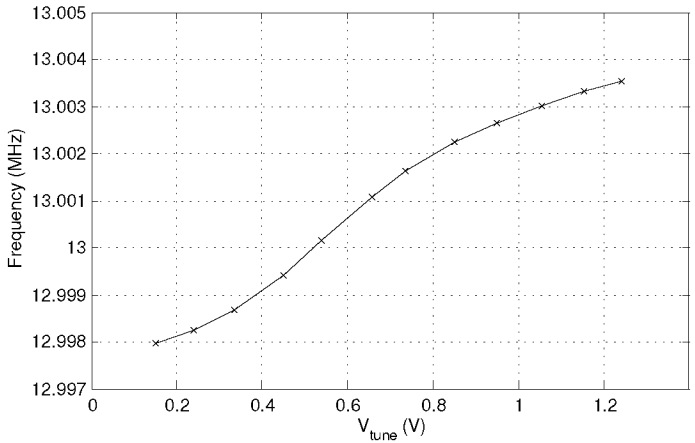
The amplitude build-up transient of the Pierce oscillator is shown in Fig. 7.18. The figure illustrates the gate voltage of M_7 of the detector, and has been measured by first stopping oscillations by shorting the crystal, and then removing the short circuit. The transient is very similar to the simulated one, and does not show any overshooting.

To evaluate their modulation characteristics, the two crystal oscillators have been modulated with a sinusoidal signal of frequency f_m. The amplitude of the signal has been adjusted to produce a frequency deviation of $\Delta f_{pp} = 1.7$ kHz (at $f_m = 100$ Hz). The oscillator instantaneous frequency has then been measured with a modulation domain analyzer (HP53310A). The observed behavior of the two VCXOs is summarized hereafter:

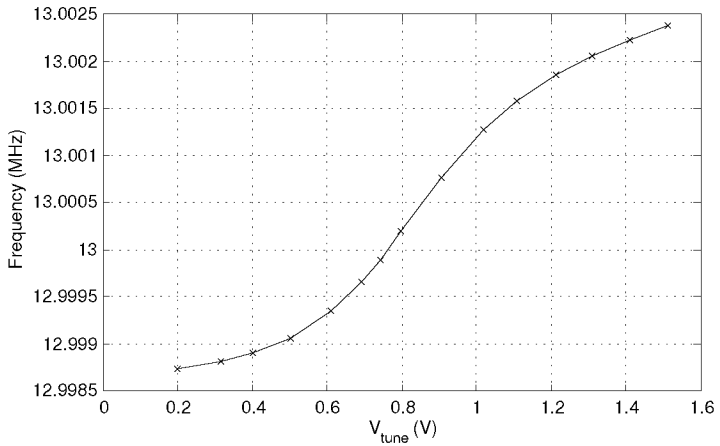
- *Pierce Oscillator*: up to a modulation frequency of 1 kHz, the waveform of the signal is practically undistorted, with only a slight amplitude reduction. At $f_m = 4$ kHz the frequency deviation is as low as $\Delta f_{pp} = 1.07$ kHz, and its waveform results slightly distorted. At higher frequencies the waveform distortion increases very rapidly, becoming rectangular-like with $\Delta f_{pp} = 1.19$ kHz at 6 kHz, and triangular-like with $\Delta f_{pp} = 1.78$ kHz at 8kHz. Above this frequency the frequency deviation increases up to about $\Delta f_{pp} = 2.8$ kHz at 10 kHz with a waveform similar to a sequence of short pulses.

- *Colpitts Oscillator*: the signal is undistorted up to a frequency of 2 kHz. Above this frequency the frequency deviation Δf_{pp} begins to decrease with a minimum of 1.26 kHz at f_m=6 kHz. The waveform of the signal results only slightly distorted. Above 6 kHz, the frequency deviation Δf_{pp} begins to increase reaching 2.4 kHz at 25 kHz. At this frequency the signal results strongly distorted.

The poorer performance of the Pierce oscillator is very probably caused by the unwanted amplification of the modulating signal described in Sec. 7.3.1.



(a) Pierce oscillator.



(b) Colpitts oscillator.

Figure 7.16: *Measured VCXO tuning range.*

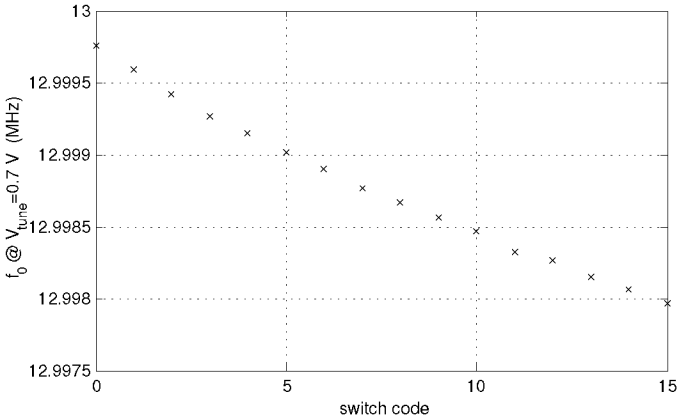


Figure 7.17: *Measured oscillation frequency of the Colpitts oscillator with internal varactor at the various switches positions.*

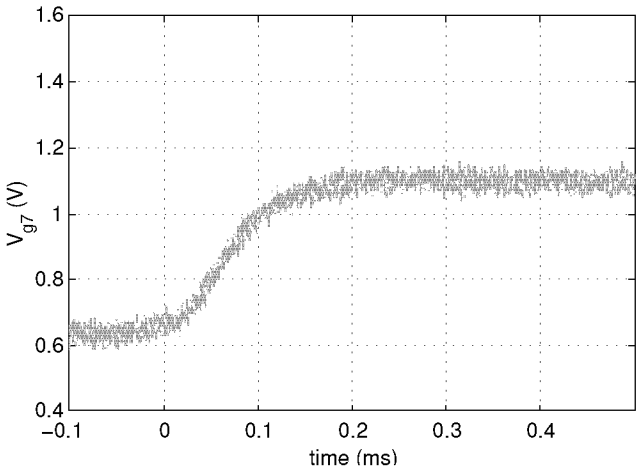


Figure 7.18: *Start-up transient of the Pierce oscillator. Voltage V_{g7} is the measured detector gate voltage (Fig. 7.12).*

Chapter 8

Characterization of the Transceiver

Most of the circuits discussed in the previous two chapters have been combined on a single chip to realize a complete Bluetooth transceiver. The IC includes LNA, image-reject mixer, channel filter, IF limiting amplifier, demodulator, VCO, prescaler, power amplifier, and antenna switch. The two crystal oscillators have been integrated on a separate IC to enable characterization of the two point modulator with various reference oscillators. A photomicrograph of the transceiver is shown in Fig. 8.1.

8.1 The Receiver

The unpackaged transceiver test IC has been glued and bonded on a printed circuit board. The channel filter and the demodulator have been tuned with the help of an external potentiometer in such a way as to precisely set the oscillation frequency of the filter auxiliary VCO at its nominal oscillation frequency of 6.5 MHz. The common-mode voltage of the filter has been set with the help of the on-chip bandgap reference.

Figure 8.2 shows $|S_{11}|$ in receive (black line) and transmit mode (gray line). The minimum of the curve in receive mode is set, among

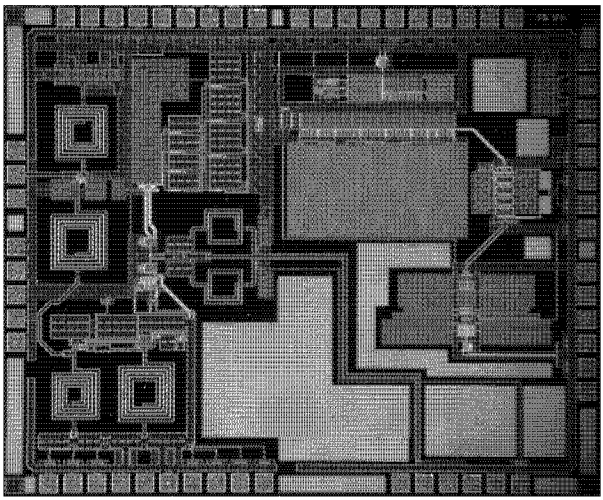


Figure 8.1: *Photomicrograph of the transceiver.*

other things, by the length of a bond wire. No attempt was made to optimize its length, but it should be possible to shift the minimum of the curve to the center of the band by slightly increasing the length of the bond wire. The peaks appearing in transmit mode are bogus, and are due to the fact that during measurement the transmitter was sending a signal.

The static demodulation characteristic of the receiver appears in Fig. 8.3. The curve is well centered at 2 MHz, proving good matching between demodulator, channel filter, and auxiliary 6.5 MHz VCO. The dynamic demodulation characteristic has been tested with a sinusoidally modulated carrier with a frequency of 2.434 GHz, a modulation index of 0.32, and modulated at 50 kHz. The spectrum of the receiver output signal measured with an input power of -50 dBm is shown in Fig. 8.4. The 50 kHz signal and odd harmonics of the signal are clearly visible. The spectrum shown corresponds to the maximal SNR of the receiver, which, as in every FM receiver, is limited by the *phase noise* of the local oscillator.[1]

[1]The noise floor peaking around 10 kHz is caused by the particular PLL loop

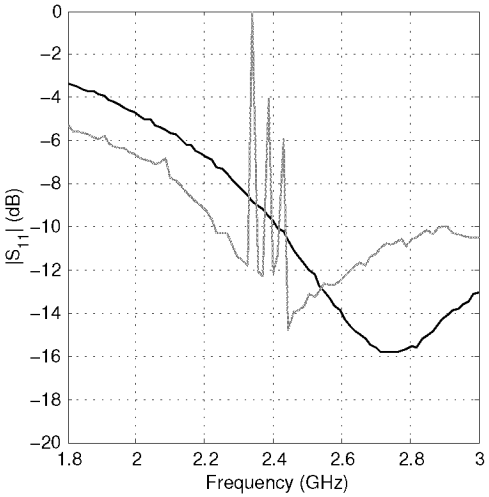


Figure 8.2: *Measured S_{11} in Rx (black line) and Tx (gray line) mode.*

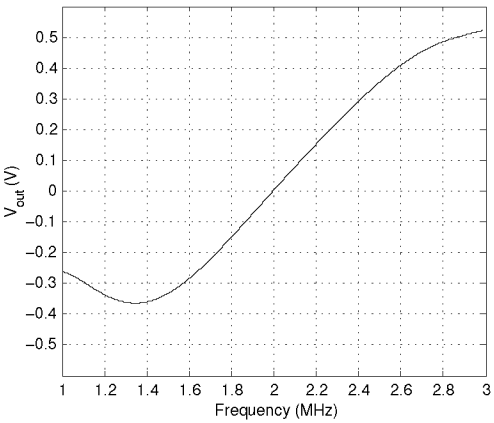


Figure 8.3: *Receiver demodulation characteristic.*

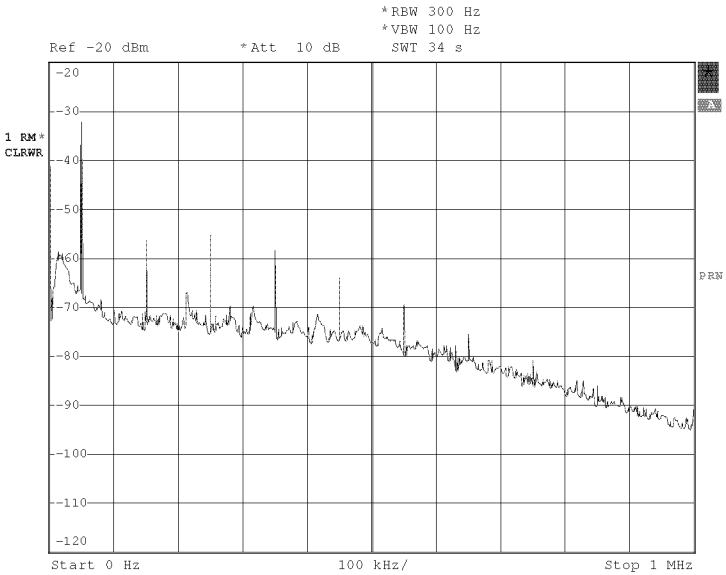


Figure 8.4: *Demodulated output signal.*

Since no data slicer has been implemented, we estimate the sensitivity and the iIP3 of the receiver by adding the noise and the intermodulation products generated by the various blocks, and obtain a sensitivity of -74.9 dBm and an iIP3 of -18.1 dBm (at the input of the chip).

The blocking characteristic of the receiver has been tested by noting at which power of the interfering signal I the SNR of the wanted signal S begins to degrade. The measured values are summarized in Table 8.1. The specifications are satisfied at all but one frequency: with an interfering signal 2 MHz below the wanted signal, the SNR of the wanted signal begins to degrade with a blocking signal 3 dB below the

filter used to test the receiver. The filter has a bandwidth of 10 kHz, and the phase margin of the loop is 55°.

S (dBm)	Δf (MHz)	I/S (dB)	Note
-60	+1	8	
-60	-1	11	
-60	+2	31	
-60	-2	27	LO frequency
-67	+3	41	
-67	-3	30	1 ch. above image freq.
-67	+4	43	
-67	-4	23	image freq.
-67	+5	46	
-67	-5	40	1 ch. below image freq.
-67	+6	48	
-67	-6	50	

Table 8.1: *Measured blocking characteristic. The signal power S has been chosen according to the test conditions specified by the Bluetooth standard.*

value specified by the standard. Therefore this frequency has to be considered one of the five spurious responses (with relaxed specifications) allowed by the standard.

8.2 The Transmitter

The prototype ICs have been combined with a commercial PLL frequency synthesizer (ADF4110) and two variable gain amplifiers to form a complete two-point modulator whose block diagram is shown in Fig. 8.5. In Section 3.2.3 we have seen that the transfer function of a two-point modulator, in theory and if properly calibrated, is independent from the loop filter. In spite of this, the loop filter determines which part of the spectrum of the modulating signal contributes to the modulation of the output signal through the low-frequency path P_{LF}, and which part contributes through the high-frequency path P_{HF}. An upper limit to the loop bandwidth of a two-point modulator is therefore constituted by the modulation bandwidth of its reference oscillator. Unfortunately, as noted in Section 7.3.5, the modulation bandwidth of

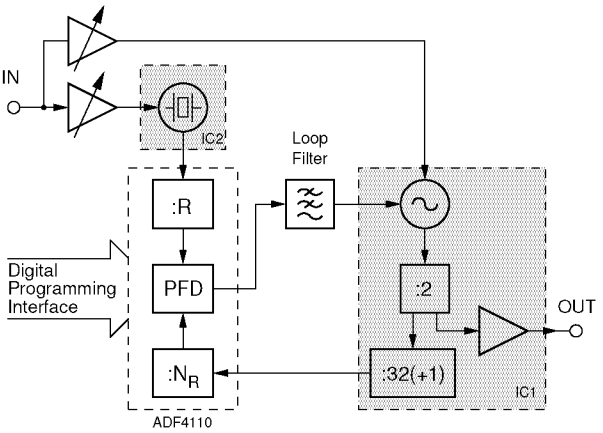


Figure 8.5: *Block diagram of the two-point modulator prototype.*

crystal oscillators is rather limited, and in the particular case considered here it is not large enough to guarantee the required lock time.

One way to solve this problem is by changing the loop bandwidth of the synthesizer during operation: during the transition from one channel to another, we set the bandwidth of the loop wide enough to satisfy the lock time specification, while during modulation we set the loop bandwidth narrow enough to ensure good modulation properties with little distortion.

Figure 8.6 shows the classic second order filter configuration used to implement a third order PLL, together with two second order filter configurations suitable to change the bandwidth of the synthesizer during operation. The transfer function of configuration (a) is

$$\frac{V_o}{I_{CP}} = \frac{1}{s(C_0+C_1)} \cdot \frac{sC_1R_1+1}{s\frac{C_0C_1}{C_0+C_1}R_1+1} \tag{8.1}$$

From this equation it is apparent that the zero and the highest pole of the transfer function can be simultaneously shifted by changing the value of resistor R_1. The value of the latter can be changed by using two parallel connected resistors and one switch as shown in configuration (b). Since the position of the switch also defines the impedance level of

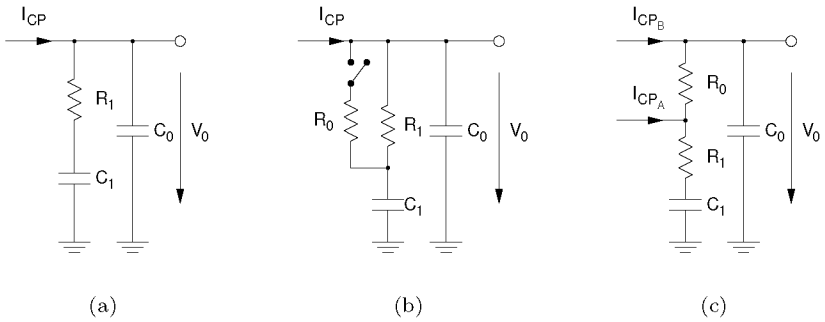


Figure 8.6: *PLL loop filters.*

the filter, the charge pump current I_{CP} has to be adjusted according to its position.

Configuration (c) shows a filter with the help of which it is possible to shift only the zero of the transfer function. Its location is changed by injecting the charge pump current either in A or in B:

$$\frac{V_o}{I_{CP_A}} = \frac{1}{s(C_0+C_1)} \cdot \frac{sC_1R_1+1}{s\frac{C_0C_1}{C_0+C_1}(R_0+R_1)+1} \tag{8.2}$$

$$\frac{V_o}{I_{CP_B}} = \frac{1}{s(C_0+C_1)} \cdot \frac{sC_1(R_1+R_0)+1}{s\frac{C_0C_1}{C_0+C_1}(R_0+R_1)+1} \tag{8.3}$$

This can be implemented without using any switch by integrating two charge pumps. The ratio between the currents of the two charge pumps I_{CP_A}/I_{CP_B} is determined by the amount by which the zero has to be shifted. Shifting only the zero of the transfer function has the advantage that, by doing so, it is possible to simultaneously change the bandwidth and the phase margin of the loop. Differently from what is suggested by the results of a linear analysis, practical experimentation shows in fact that the modulation distortion of a two-point modulator is a function of the phase margin: a small phase margin causes a large distortion.

Figure 8.7 shows the peak-to-peak frequency deviation normalized to 320 kHz as a function of modulation frequency measured on the prototype with the Colpitts crystal oscillator, for two filter configurations:

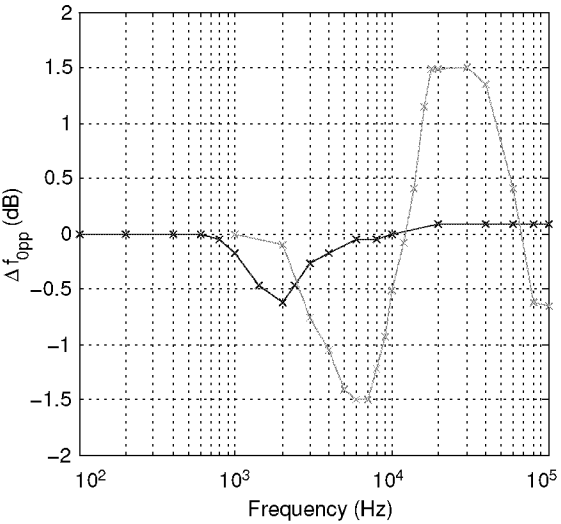


Figure 8.7: *Frequency response of the two-point modulator.*

the gray curve has been measured with a loop bandwidth of 15 kHz and a phase margin of 52°, the black curve with a loop bandwidth of 2 kHz and a phase margin of 76°. The transfer function of the two-point modulator could be made perfectly flat by replacing the crystal oscillator with a signal generator (HP ESG-3000A), confirming that the crystal oscillator is effectively by far the most important source of distortion.

The distortion observed on the prototype employing the Pierce oscillator is much larger than the one observed on the prototype employing the Colpitts oscillator.

The power emitted by the transmitter is -0.5 dBm.

Chapter 9

Conclusions

In this thesis we have presented the top-down design of a low-power, highly integrated transceiver for the Bluetooth short-range wireless technology, developed in a 0.18 μm CMOS technology. The design has started with a careful study of the specifications, followed by an analysis of various transceiver architectures, and concluded with the design and implementation of appropriate circuits.

The applications targeted by the project are wrist-watches and smart-cards, which have very tight power consumption requirements. For this reason, power consumption was given a high priority throughout all of the phases of the design. In addition, in the attempt to go as close as possible to the ultimate power consumption (for the chosen technology), it was decided at the beginning of the project to satisfy the specifications imposed by the standard with only a small margin.

A second very important constraint dictated by the targeted applications is the small space into which the whole system has to fit. The fulfillment of this constraint dictates the implementation of a highly integrated solution. The developed transceiver, besides making use of a low-IF receiver architecture to allow integration of the channel filter, has a single-ended RF interface and includes an on-chip antenna switch, simplifying its use and avoiding the need for external baluns and switches.

Although the RF performance required by Bluetooth is not very demanding if compared with other technologies, the implementation

of a highly integrated, low power transceiver is quite challenging as shown by the power consumption of most commercial products which is around 40 mA at 3 V in receive mode, and slightly lower in transmit mode. Only recently Texas Instruments Inc. has made a step in direction low power, introducing on the market a 0.13 μm CMOS Bluetooth unit (including baseband processor[1]) with a power consumption of 37 mA at 2 V in receive mode, and 25 mA in transmit mode. To our knowledge, up to now the Bluetooth transceiver with the lowest power consumption published in the open literature consumes 34 mA at 1.8 V in receive mode, and 26 mA in transmit mode [51]. Our design requires 26 mA at 1.8 V in receive mode, and 23 mA in transmit mode, however, with a slightly inferior performance.

The bottleneck of the dynamic range of the receiver presented in this work is constituted by the active channel filter. By improving its dynamic range, it is possible to greatly ameliorate sensitivity, intermodulation, and blocking performance of the whole receiver. Unfortunately, an improvement of the dynamic range of an analog active filter goes along with a substantial increase of the power consumption. One approach which deserves consideration and which becomes more and more attractive as the minimum feature size of technologies is reduced, is to implement only part of the filtering in the analog domain, and perform the rest of the channel selection (and demodulation) in the digital domain.

Concerning power consumption, the blocks of the receiver consuming most of the power are the two divide-by-two frequency dividers used to generate the quadrature LO signals, and to drive the power amplifier and the prescaler. Due to the good measured image-rejection, we believe that there is some margin for power reduction. The image-rejection is in fact almost completely set by the polyphase filter used to recombine the I and Q signal paths. It is therefore advantageous to use only one (slightly stronger) divider, and balance the loads connected to its I and Q output ports with dummy structures. Furthermore, it would be interesting to investigate the use of ESCL logic with resonant loads.

On the transmitter side, we have adopted an architecture requiring very little extra circuitry over what is needed to implement the receiver,

[1]The lowest power Bluetooth baseband processor on the market consumes 2 mA at 1.8 V.

and have found a way to solve the restrictions related to the limited modulation bandwidth of crystal oscillators. The main power consuming block of the transmitter is the power amplifier. This is mainly due to the low quality factor of the spiral inductor used to implement the output matching network, and to the attenuation introduced by the on-chip antenna switch.

Whereas the introduction of deep submicron CMOS technologies and the continuing trend toward always smaller minimum feature sizes can be claimed to have only positive effects on digital systems, the same can not be said for analog systems. The geometry of the transistors and the current required for analog designs is in fact dictated more by linearity and noise requirements than by technology dependent factors.[2] In addition, the reduced supply voltage accompanying modern deep submicron CMOS technologies makes the fulfillment of linearity and compression requirements an even more difficult task. To implement a low power transceiver it is therefore not enough to use a technology with fast transistors, but it is indispensable to have an intimate knowledge of all of the requirements of the system to be implemented, and to optimally exploit the strengths and the new possibilities offered by modern, deeply scaled technologies. This work shows that with a careful top-down design procedure it is possible to implement a highly integrated transceiver in a cost effective technology with a very modest power consumption.

[2] Unless working very close to the maximum cutoff frequency f_T of the technology.

Appendix A

Bluetooth Specifications Summary

Parameter	Value	Comment
Connection		
Access	TDMA	
Duplex	TDD	
TDD guard time	220 μs	
Frequency		
Band	2.40-2.4835 GHz	
Channel spacing	1 MHz	
Accuracy	$\pm$ 75 kHz 400 Hz/μs	initial center frequency max. drift rate
Hopping	1.6 kHops/s	
Modulation		
Type	GFSK (BT=0.5)	
Freq. deviation	$\pm$ 140-175 kHz	mod. index 0.28...0.35
Burst bit rate	1 Mbit/s	
Minimum freq. deviation	115 kHz	
Accuracy	$\pm$20 ppm ($\pm$10μs) $< 1/8\mu$s	symbol timing zero crossing

Parameter	Value	Comment
Receiver		
Sensitivity	-70 dBm	BER = 0.1 % (71 μV rms on 50 Ω)
Max. input level	-20 dBm	(23 mV rms on 50 Ω)
iIP3	-17 dBm	SNR_{dem}=19
Noise figure	25 dB	SNR_{dem}=19
Blocking (S=-67 dBm)	-27 dBm -10 dBm	2.0-2.399 GHz 2.498-3.0 GHz 30-2000 MHz 3.0-12.75 GHz
Image rejection	20 dB	in-band
Interference C/I	11 dB 0 dB -30 dB -40 dB	co-channel; S=-60 dBm 1st adjacent channel; S=-60 dBm 2nd adjacent channel; S=-60 dBm $\geq$ 3rd adjacent channel; S=-67 dBm
Spurious emission	-57 dBm -47 dBm	30-1000 MHz 1-12.75 GHz (out-of-band)
1st Local Oscillator (Tx and Rx)		
Phase noise	-80 dBc/Hz -101 dBc/Hz -111 dBc/Hz	@ 550 kHz @ 2 MHz @ 3 MHz
Transmitter		
Oputput power	1mW	class 2, 3
Spurious emission In-band Out-of-band 	 FCC Part 15.247c -20 dBc -20 dBm -40 dBm -36 dBm -30 dBm -47 dBm -47 dBm	 @ $\pm$ 550 kHz |N-M|=2 |N-M| $\geq$3 30-1000 MHz 1-12.75 GHz 1.8-1.9 GHz 5.15-5.3 GHz

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