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Characterisation of High Density Substrates for Use at Millimetre-Wave Frequencies

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Didier Cottet
Dipl. El.-Ing. ETH
born 22nd February 1971
citizen of Bossonnens FR

accepted on the recommendation of

Prof. Dr. Gerhard Tröster, examiner
Dr. David J. Pedder, co-examiner

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Contents

Abstract

In this dissertation we present a quantitative performance metric and benchmark methodology for high density substrate technologies used at millimetre-wave frequencies. The proposed method is based on the fact that next to the dielectric permittivity and the dielectric loss tangent, the determining factors for millimetre-wave system performance are mainly topology parameters related to the technology build-up, the process accuracy and the achievable minimum structure definition. This means that for a specified technology high frequency performance estimations and comparisons can be done at an early stage of product development and without use of dedicated high frequency simulation tools or measurement equipment and with no need for complete system designs. This thesis relies on the following three basic performance factors:

- Quality of design and layout
- Intrinsic material properties
- Quality of underlying manufacturing technology

The *quality of design and layout* is a matter of solid design engineering according to the laws of electromagnetic theory. The *material properties* are very important in the sense that they must be thoroughly characterised at the target frequencies. But once they are known, the values remain stable with only marginal variations and can be regarded as fixed. Hence, it is the *underlying manufacturing technology* that distinguishes between high performance and low performance systems, between expensive and low cost manufacturing and between low volume and high volume compatible processes. The quality of the underlying technology is on one hand defined by its topology build-up and on the other hand by the build-up parameters and their variations.

An important aspect to consider when characterising technology build-ups are the physical constraints occurring at millimetre-wave frequencies. Dielectric and conductor thickness, wavelength, skin depth and parasitic mode excitation as well as mechanical reliability are but a few of the issues that demand for thorough trade-off analysis. To determine if a technology suits the system specifications at millimetre-wave frequencies an effective, well-defined characterisation procedure is

required. The procedure must consist of a quantitative metric to measure the technology performance, a tool that facilitates the comparison and an acquisition technique for technology parameter data.

In this dissertation such a characterisation procedure is developed and its concept proven by means of a case study comparing 17 different high density substrate technology alternatives. The investigated technologies comprise thin film, laminate and thin film on laminate build-ups and were developed and manufactured within the European research projects LAP[1] and LIPS[2].

[1]LAP, Low Cost Large Area Panel Processing of MCM-D Substrates and Packages, Esprit Project no. 26261, BBW no. 97.0286

[2]LIPS, Low Cost Interconnect, Packaging and Sub-system Integration Technologies for Millimetre-wave Applications, IST Project no. 30128, BBW no. 01.0301

Zusammenfassung

Diese Dissertation präsentiert eine quantitative Leistungsmetrik und Vergleichsmethodik für High-Density Substrattechnologien und deren Anwendung im Millimeterwellen-Frequenzbereich. Als Grundlage dient die Tatsache, dass neben der dielektrischen Permittivität und dem dielektrischen Verlustfaktor der Materialien, vor allem auch rein topologische Grössen wie der Substratlagenaufbau, die Prozessiergenauigkeit und die minimale Strukturauflösung einen bedeutenden Einfluss auf die Gesamtleistung haben. Damit können die Hochfrequenzeigenschaften verschiedener Technologien bereits zu einem frühen Zeitpunkt und ohne komplexes Systemdesign und Hochfrequenzsimulationen abgeschätzt und verglichen werden. Folgende drei Leistungsfaktoren werden dabei unterschieden:

- Qualität von Design and Layout
- Intrinsische Materialeigenschaften
- Qualität der zugrunde liegenden Technologie

Die *Qualität von Design and Layout* wird im wesentlichen durch solides Handwerk des Designers bestimmt, basierend auf den Gesetzen der Elektromagnetischen Theorien. Die *intrinsischen Materialeigenschaften* spielen eine bedeutende Rolle und müssen vor allem im Frequenzbereich der Zielapplikation präzise charakterisiert werden. Einmal bekannt, ändern sich diese Eigenschaften nur noch unwesentlich und können als feste Werte betrachtet werden. Die *zugrunde liegende Technologie* ist somit die entscheidende Komponente welche teure Hochleistungssysteme von Billiggeräten unterscheidet und welche kleine oder grosse Stückzahlen ermöglicht. Die Qualität der Technologie ist einerseits durch den Topologieaufbau und andererseits durch die geometrischen Grössen und ihren Variationen bestimmt.

Ein wichtiger Aspekt, welcher bei Technologie-Charakterisierung in Betracht gezogen werden muss, sind die bei Millimeterwellen geltenden physikalischen Einschränkungen. Die Dicken der Dielektrikums- und Metalllagen, die Wellenlängen, die Tiefe des Skin-Effektes und die Anregung parasitärer Modi aber auch Zuverlässigkeitsaspekte müssen sorgfälltig aufeinander abgestimmt werden. Um genau ermitteln zu

können, ob eine Technologie den Systemanforderungen entspricht wird eine klar definierte Prozedur benötig. Diese Prozedur muss zu diesem Zweck eine quantitative Metrik für Technologieleistung, ein flexibles Vergleichswerkzeug und eine effiziente Parametermessmethodik zur Verfügung stellen.

Die vorliegende Arbeit beschreibt den Entwurf einer entsprechenden Prozedur und prüft deren Konzept mittels einer Fallstudie. Dabei werden 17 verschiedene Substrattechnologien aus den bereichen Dünnfilm, Laminate und Dünnfilm auf Laminat untersucht, welche im Rahmen der europäischen Forschunsprojekte LAP[3] und LIPS[4] entwickelt und hergestellt wurden.

[3]LAP, Low Cost Large Area Panel Processing of MCM-D Substrates and Packages, Esprit Project no. 26261, BBW no. 97.0286

[4]LIPS, Low Cost Interconnect, Packaging and Sub-system Integration Technologies for Millimetre-wave Applications, IST Project no. 30128, BBW no. 01.0301

1

Introduction

System integration of millimetre-wave applications is currently experiencing a paradigm change. It is expanding from pure military and space applications with high budgets and low volumes towards emerging applications aiming at low costs and high volumes such as, for example, wireless telecommunication, intelligent transportation systems and (tele-)medical electronics [1]. This new paradigm demands a different approach for realising such products: new methods for developing and characterising the required technologies and new concepts for designing systems are needed. Many research activities are taking advantage of available low cost technologies for use at millimetre-wave frequencies. However, they are not yet oriented towards characterisation and optimisation for high volume compatibility and low cost production. New methods are required to measure and quantify technology performance and their suitability for millimetre-wave system integration.

This first chapter starts with a general overview of today's millimetre-wave packaging markets and trends. This will lead to the motivation underlying this work and give a brief overview of other research and commercial activities performed in these fields. Novel contributions presented in this thesis are summarised and the structure of the thesis is explained.

1.1. Millimetre-Wave – Markets and Trends

Today, new telecommunication systems and services such as RF radio links and multimedia distribution systems (LMDS, local multipoint distribution system and MVDS, microwave video distribution systems) are already generating growing market segments for microwave monolithic integrated circuits (MMIC) above 6 GHz [2]. It is even estimated that in a few years more wireless than fixed line terminals will access the internet [3]. Two important application trends are observed for upcoming markets: point-to-point broadband radio links operating at 60 GHz [4, 5, 6] and intelligent adaptive cruise control (ACC) systems for automotive applications working at 77 GHz [7], not to forget the ongoing activities in the well established millimetre-wave markets space, defence and medical which are also shifting more and more towards low cost solutions [8, 9].

From a technological view, the different opinions existing in the controversy of system-on-chip (SoC) vs. system-on-package (SoP) [10] also apply to millimetre-wave system integration. Many new RF module technology architectures are proclaimed in publications, namely sub unit based systems vs. common substrate architectures, and since 1999 also single packaged MMICs [2]. For all these technologies cost effective substrates remain a challenge [3]. Hence, the big advantage of high density substrate technologies is the added value gained through their possibilities of integrated passives (IP) [3].

These trends have in consequence a strong influence on the education of millimetre-wave application engineers. The knowledge of high frequency theory is of course important but also other disciplines such as photonics, bioengineering, signal processing, communication technology and *packaging* are required [1]. Furthermore, the critically short 'development-to-market' cycles demand engineers with more generalised skills to cope with the various technologies and also with the production, quality assurance, marketing and sales staff [11].

1.2. Motivation and Objectives

Two reasons why millimetre-wave products fail to enter the consumer markets are the high costs of the necessary technologies for realising such systems and their incompatibility to fully automated mass production. The goal of this work is therefore to investigate cost effective packaging alternatives for use in millimetre-wave applications allowing

the reduction of size and cost and the improvement of high-volume production compatibility. This is done by using low cost materials in conjunction with existing technologies (MCM-D, MCM-L, MCM-L/D). Further cost reduction is achieved by increasing the integration level using single-substrate multi-MMIC modules and integrated passive components. The integration can go as far as including the system antennas or antenna arrays onto the same substrates for further size and cost reduction.

The instrument that will allow us to reach this goal is an effective method for evaluation and optimisation of existing substrate technologies in terms of RF performance. In contrast to the existing RF design and simulation tools, the proposed method aims at being used by process engineers with minimal knowledge of millimetre-wave theory. The challenge is therefore to formulate and model the relation between RF parameter performance and substrate manufacturing. Based on these models a technology performance measurement, comparison and benchmarking methodology is developed. The objectives underlying this thesis are therefore formulated as follows:

Objective I: To provide a technology RF performance metric and benchmark tool allowing for quantitative comparison of technology alternatives.

Objective II: To design test vehicles and methods capable of measuring the technology parameters responsible for the RF performance.

Objective III: To investigate today's high density substrate technologies and to compare their suitability for RF applications, using the previously mentioned test methods and benchmark tools.

1.3. Related Work

Technology evaluation is a necessary task when performance is being improved or production costs have to be reduced. A comparative analysis of PWB technologies for use in portable electronic devices was presented in [12] and in [13] various LTCC tapes were benchmarked up to 40 GHz. On a larger scale the Interconnection Technology Research Institute (ITRI) conducted a technology comparison where the RF performance of 18 MCM-L technologies from 16 manufacturers worldwide were tested [14].

On the software side, companies like Ansoft and Agilent offer design and analysis tools with complete performance optimisation capabilities. *Ansoft Designer* provides system simulation, circuit simulation and layout and manufacturing support with links to layout tools from companies such as Cadence, Mentor, Synopsys and Zuken. The optional *Optimetrics* extension provides sensitivity analysis with regard to manufacturing tolerances and material properties [15].

For the widely used *ADS* design tool from Agilent a *Statistical Design* extension is available for automatic sensitivity and yield analysis based on Design of Experiment (DOE) and Monte Carlo (MC) methods [16, 17].

Both tools aim at layout optimisation and design centring during product development. The statistical functions are applicable to entire designs resulting in accurate yield estimations. For technology development however, the needs are different as it is not the complexity of the investigated designs that counts but the flexibility of the compared technologies. And the final target is not a system yield but a technology performance ranking.

1.4. Novel Contributions

This section summaries the tasks and novelties that have been accomplished in order to reach the three objectives.

1. The *system realisation path* model as unique relation between process manufacturing and RF system design was developed to formulate the system's RF performance as a function of technology parameters.

2. A *technology capability and performance metric* is presented based on existing methods known from process development and process control.

3. A *technology benchmark tool* composed of generic RF component models was implemented for early technology performance and yield estimations. The benchmark tool is used for virtual processing and comparison of technology alternatives.

4. A method describing *technology variations* in the *spatial frequency domain* was developed. The general idea is to take the local occurrence of process variations into account and therefore to realise RF designs with tighter tolerances.

5. *Test vehicles* for characterisation of material properties and build-up topologies of millimetre-wave technologies were designed and implemented.

6. A novel, *zone based process monitoring* method is presented allowing for optimised process monitor placement, thus minimising area consumption and guaranteeing full panel coverage. The method is application oriented meaning that the extend of included monitoring is scalable with the demands of the application complexity.

7. An evaluation and benchmarking of *17 high density substrate alternatives* for millimetre-wave frequencies was performed with regard to their suitability for integration of a 77 GHz adaptive cruise control radar for automotive applications.

1.5. Structure

Chapter 2 reviews the typical requirements of millimetre-wave applications. This serves as a basis to understand the technology constraints applying at these frequencies. Chapter 3 develops a metric that allows to measure technology performance. It is based on existing process capability and process performance measures, adapted to the needs of substrate technologies. Chapter 4 describes the implementation of a technology benchmark tool using the technology performance metric introduced in Chapter 3. In Chapter 5 parameter description methods and test structures are proposed to effectively characterise the investigated technologies. Seventeen different high density substrate alternatives are discussed and compared in Chapter 6, using the characterisation methods and the benchmarking tool presented in the previous chapters. A 77 GHz adaptive cruise control transceiver module serves as benchmark reference application. Chapter 7 draws the conclusions and gives a short outlook.

2

Millimetre-Wave System Constraints

As radio frequency (RF) and wireless applications are moving towards millimetre-wave frequencies several physical constraints apply to the system components involved. This chapter shows the component's close relation to dimensional and material properties and the trade-offs between RF performance and mechanical reliability as encountered in high density packaging.

One aspect is the fact that compared to the system wavelength most elements in a millimetre-wave layout must be treated as distributed components. Hence, the functional or parasitic characteristics of such elements are proportional to physical dimensions of the technology. A second aspect is the unfortunate, often reciprocally proportional relation between the electrical performance and the mechanical reliability of the involved system components. Finally, also external and discrete millimetre-wave components (e.g. MMICs) must be taken into account from the beginning as their final performance strongly depends on the way they are connected to the packaging substrate.

2.1. Physical Constraints

First, theoretical performance limitations defined by geometrical and physical material properties and system package requirements are investigated. Typically these limitations are related to *electrical* factors such as wavelengths, target characteristic impedance, losses, higher order modes and surface waves, *mechanical* factors such as thermal coefficients, adhesion and power dissipation [18, 19] and finally *environmental* factors such as temperature and moisture (especially in automotive applications [20]). These constraints become even more relevant when passive components [21] or antennas [22] are being integrated.

Millimetre-wave systems have clearly defined *high level* system parameters such as target frequency, bandwidth and gain as well as *low level* component parameters such as insertion loss, return loss, characteristic impedance and port isolation. Typically, the high level parameters are determined by the performance of the low level parameters, which in turn are influenced and predefined by physical constraints.

2.1.1. Dielectric Permittivity

The dielectric permittivity ϵ is the most important material property in RF systems. It determines the propagation velocity as function of frequency and therefore also the wavelength. This relation is defined in Equation 2.1 where $c_0 = 2.998 \cdot 10^8$ m/s is the light speed, f the frequency and $\epsilon_{r_{eff}}$ the effective relative permittivity [1].

$$\lambda = \frac{c_0}{f \cdot \sqrt{\epsilon_{r_{eff}}}} \tag{2.1}$$

Table 2.1 shows the calculated wavelengths for different permittivities and frequencies. As expected for *millimetre-wave* frequencies, at $f = 58$ GHz and $f = 77$ GHz, the wavelength λ is of the order of a few millimetres. Any dimension larger than about $\lambda/10$ is treated as electrically distributed.

The second elementary component parameter which is determined by the dielectric permittivity is the characteristic impedance of transmission lines. Besides the dielectric permittivity it is also a function of topological dimensions. Depending on the used substrate technology the dielectric permittivity and the build-up topology dimensions are

[1] The effective relative permittivity is a function of substrate topology, relative permittivities and frequency.

Table 2.1: *Wavelength for different permittivities and frequencies.*

$\epsilon_{r_{eff}}$	$f = 1$ GHz	$f = 10$ GHz	$f = 58$ GHz	$f = 77$ GHz
2.0	$\lambda = 212$ mm	$\lambda = 21.2$ mm	$\lambda = 3.65$ mm	$\lambda = 2.75$ mm
3.0	$\lambda = 173$ mm	$\lambda = 17.3$ mm	$\lambda = 2.98$ mm	$\lambda = 2.25$ mm
10.0	$\lambda = 94.5$ mm	$\lambda = 9.45$ mm	$\lambda = 1.63$ mm	$\lambda = 1.23$ mm

fixed within certain limits. These are thus determining the range of realisable impedances for each feasible transmission line configuration.

2.1.2. Dielectric Thickness

The thickness of the dielectric layers in a substrate build-up plays an important role for many RF parameters. As already mentioned above, the realisable range of line impedances depends on substrate topology parameters such as the dielectric thickness. Also the ohmic losses in the conductors are reciprocally proportional to the thickness. Table 2.2 shows the computed total insertion losses of 50Ω microstrip lines for three different thicknesses. But with increasing thickness the lines are getting wider at constant impedance and at a certain point the line widths or any other interconnect element dimension such as the via diameters (see Table 2.2) are approaching the wavelength. With this, unwanted parasitic effects get large and deteriorate performance.

Table 2.2: *Transmission losses for different dielectric thicknesses.*

dielectric layer thickness	microstrip line width for $Z_0 = 50\Omega$	losses @ 60 GHz	via diameter
$h = 15$ μm	$w = 30$ μm	$\alpha = 1.8$ dB/cm	$v \approx 30$ μm
$h = 30$ μm	$w = 70$ μm	$\alpha = 1.0$ dB/cm	$v \approx 50$ μm
$h = 45$ μm	$w = 112$ μm	$\alpha = 0.67$ dB/cm	$v \approx 70$ μm

In the case of patch antennas, thick dielectrics are preferred and reach the optimum in the range of several 100μm depending on the frequency and the dielectric permittivity [22, 23]. Too thick dielectrics however are not recommended as higher order modes and surface waves are getting excited above a certain limit, also depending on the frequency and the dielectric permittivity [24].

From a mechanical viewpoint, thick dielectric layers can be critical when the build-up material's coefficients of thermal expansion (CTE) are not matched. This means that during processing or operation at

different temperatures the layers expand unequally. The thicker the individual layer are the stronger is the mechanical stress induced between the layers. This can rapidly lead to warpage, cracking or delamination effects [25, 26, 27].

2.1.3. Conductor Thickness

For the thickness of the conductor layers one important rule exists: the total thickness must be at least three times the skin depth to avoid increased ohmic losses as result of a reduced current flow surface area (Equations 2.2 and 2.3).

$$\delta = \sqrt{\frac{1}{\pi \mu_0 \sigma f}} \tag{2.2}$$

$$R_s = \frac{1}{\sigma \delta} \tag{2.3}$$

At 77 GHz for example the skin depth in copper conductors is $\delta = 0.265\mu$m. To be on the safe side, the metallisation thickness should therefore be at least $t = 1\mu$m or thicker.

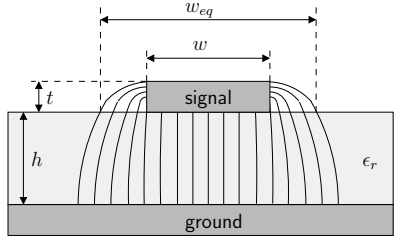


Figure 2.1: *Equivalent line width extension in microstrip lines.*

In Figure 2.1 the effect of the *equivalent line width extension* is illustrated, an effect which is directly related and proportional to the thickness of the metallisation. On 50 Ω microstrip lines with 15 μm thick copper and 60 μm dielectrics, the extended equivalent line width w_{eq} can be up to 10% wider than the actual line width w [28]. Therefore it is necessary to consider this effect during design, simulation and layout. w_{eq} is calculated using Wheelers Equations 2.4 and 2.5 [29].

$$w_{eq0} = w + \frac{t}{\pi} \cdot \ln\left(1 + \frac{4 \cdot \exp(1)}{\frac{t}{h} \cdot \coth^2\left(\sqrt{6.517 \cdot \frac{w}{h}}\right)}\right) \tag{2.4}$$

$$w_{eq} = w + \frac{w_{eq0} - w}{2} \cdot \left(1 + \frac{1}{\cosh(\sqrt{\epsilon_r - 1})}\right) \tag{2.5}$$

A relevant factor of the conductor metallisation quality is the cross section profile. As a result of the skin effect the current density distribution tends to concentrate towards the conductor extremities [30]. It is therefore advantageous to avoid conductor profiles with narrow edges such as depicted in Figure 2.2. The drawback of thick conductors as encountered on laminate dielectric build-ups is the difficulty to process well defined conductor side walls with smooth surfaces and ideally rectangular profiles.

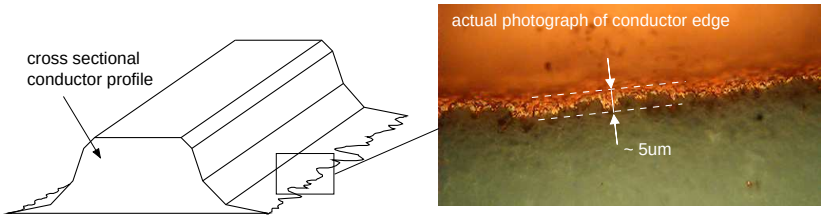


Figure 2.2: *Drawing and actual photograph of a conductor profile with poor definition producing very rough and narrow edges.*

2.1.4. Conductor Surface Roughness

The metallisation quality was already mentioned before as being an important factor for high RF performance. As a consequence of the skin effect, the current flow is concentrated in the conductor's surface, hence the quality of the surface becomes a technology parameter to consider. If the surface roughness (specified as root-mean-square (RMS) value R_q [31]) gets close to the skin depth, the effective surface resistance is increased and therewith the ohmic losses α_c become larger. The increased conductor losses α_c' are considered in simulations using the correction coefficient c_{R_q} (Equation 2.6) which is calculated with Equation 2.7 [32].

$$\alpha_c' = \alpha_c \cdot c_{R_q} \tag{2.6}$$

$$c_{R_q} = 1 + \frac{2}{\pi} \cdot \tan^{-1}\left(1.4 \cdot \left(\frac{R_q}{\delta}\right)^2\right) \tag{2.7}$$

Also important when considering surface roughness is the use of ferro magnetic metals such as nickel. Equation 2.2 shows that the skin depth is reciprocally proportional to the square root of the relative permeability μ_r [33]. Magnetic materials therefore accentuate the skin effect and increase the conductors surface resistivity R_s (Equation 2.3) and therefore also the ohmic losses.

2.2. Reliability Trade-offs

After the considerations made in the previous section it is clear that a single, optimum substrate technology does not exist. Moreover a trade-off needs to be evaluated for each situation. This section is therefore addressing the three-fold trade-off between mechanical reliability, RF performance and cost. As illustrated in Figure 2.3, RF performance and mechanical reliability can have opposing demands to common parameters.

Most trade-offs originate from physical technology constraints such as presented above. In order to illustrate the issues of competing demands four typical examples are presented.

1. From a mechanical point of view, the surface roughness promotes adhesion between build-up layers. Some manufacturers therefore use special techniques (e.g. plasma etching) to artificially increase the roughness. However, as presented earlier, at millimetre-wave frequencies where the skin depth is of the same order as the RMS value of the roughness, the ohmic losses are dramatically increased.

2. Copper metallisation tends to chemically react with polymers or to diffuse into other metals (electron migration) [34]. To prevent such effects nickel layers are often used as barriers to protect the copper. Nickel, unfortunately, is a ferro magnetic material with a relative magnetic permeability larger than 1. In magnetic materials the skin depth is reduced with the square root of μ_r

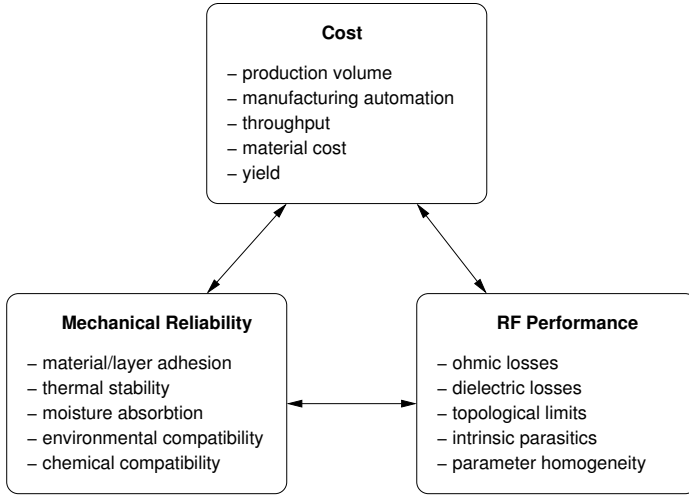


Figure 2.3: *The cost-reliability-performance three-fold trade-off points out the discrepancy of either optimising the process reliability or the RF performance*

thus increasing the ohmic losses by the same factor. The relative permeability of nickel is $\mu_{r_{Ni}} = 100 - 600\frac{H}{m}$ as initial, maximum values, $\mu_{r_{Ni}} = 5 - 20\frac{H}{m}$ at 1 GHz and further decreasing for higher frequencies. At millimetre-wave frequencies $\mu_{r_{Ni}}$ is expected to be close to unity but still to have a non-negligible effect on the conductor losses.

3. As many laminate materials have high CTE values in z-direction a minimal conductor thickness is needed to guarantee mechanical reliable metallisation of the via side walls. Thick copper layers however are more difficult to define and can result in trapezoidal profiles with large line width variations and poor edge definition. These effects are not tolerable at millimetre-wave frequencies where high quality metallisation is mandatory.

4. Metallic base or core materials are often used for mechanical stability, ease of handling, and power dissipation. In such cases the conductive base or core layers act as ground plane on the entire substrate area hence prohibiting the use of pure coplanar configurations.

2.3. System Components

Typically, millimetre-wave systems are composed of active components, passive components, interconnect elements and a module packaging or housing. The availability of components, the compatibility between component technologies and the mounting and usage recommendations of certain active components can represent severe constraints for the entire system [35]. This section briefly describes the individual component types and discusses their typical characteristics and functions [36, 37] and their influence on performance and cost [38, 39].

2.3.1. Active Components

Low noise amplifiers, power amplifiers, oscillators, frequency multipliers and mixers are but a few examples of active elements used in RF systems. These devices are manufactured as monolithic microwave integrated circuits (MMIC) and available in many different variations. Some MMICs are built in microstrip configuration with the chip bottom acting as ground and being connected to the substrate using conductive adhesives. Other MMICs use pure coplanar configurations rendering the use of flip chip attachment techniques easier. Inputs and outputs of MMICs are mostly designed with 50Ω input impedance. This means that any external interconnection must match the same impedance or provide a matching network.

2.3.2. Passive Components

Passive elements can be implemented *on-chip* or *off-chip*, both having advantages and drawbacks. The main drawback of on-chip inductors and capacitors is that they use valuable real estate on expensive active materials for passive purposes only. But with increasing application frequency the values of lumped elements get smaller and with this also their area usage. Higher application frequencies also shorten the signal wavelengths and therefore the layout dimensions of distributed elements. Furthermore, it might be more advantageous to keep some passives on-chip in order to avoid too many chip-to-substrate transitions deteriorating the signal quality.

Resistors, high-Q inductors and decoupling capacitors requiring large nominal values are not efficiently realisable on-chip. For this, some interconnect substrate technologies provide dedicated high resistivity and high permittivity layers for integration of large resistors

and capacitors, respectively. If such dedicated layers are not available, external SMD passives must be used.

Distributed passives such as couplers, baluns, Wilkinson power dividers, resonators and filters are for two reasons preferably integrated off-chip. The first is their large dimension and the second is their higher achievable performance on thick profile, low loss substrates.

2.3.3. Interconnect Elements

At millimetre-wave frequencies any interconnect element such as a transmission line connecting two MMICs must be taken into account during system design. Microstrip lines, striplines, coplanar waveguides, rigid waveguides, coaxial cables and connectors are all considered as interconnect elements. For each of these elements a variety of design components exist which need to be separately characterised. Typical interconnect design components are bends, junctions, tapers, vias and underpasses.

Interconnect elements are physically constrained to the used substrate technology. Configuration, size and shape are dictated by the technology's design rules and differ from one technology to the other. Nevertheless, they all need thorough characterisation and modelling for accurate RF system design [40]. Design tools supporting complete design flows often support component design kits (libraries) containing all required interconnect elements. Technology manufacturers are then able to provide dedicated tool kits for their technologies [41].

2.3.4. Chip Attachment

Wire bonding is a versatile interconnect technique to connect separate entities such as substrate-to-substrate, MMIC-to-MMIC or MMIC-to-substrate. In RF systems primarily ball-wedge bonding techniques with 25 – 33 μm diameter gold wires and 100 – 300 μm wire length are used. The wire inductance is typically in the order of 0.1 – 0.2 nH per wire. A widely used technique to reduce the inductance is to use two parallel wires per bond connection. A special type of wire bonding uses ribbons instead of wires (Figure 2.4). Ribbon bonding allows through its microstrip-like profile much better impedance control and lower ohmic losses.

Flip chip mounting has, compared to wire bond technologies, lower parasitic inductance and lower ohmic losses because of the shorter interconnect distance. And a big advantage of soldered flip chip mounting

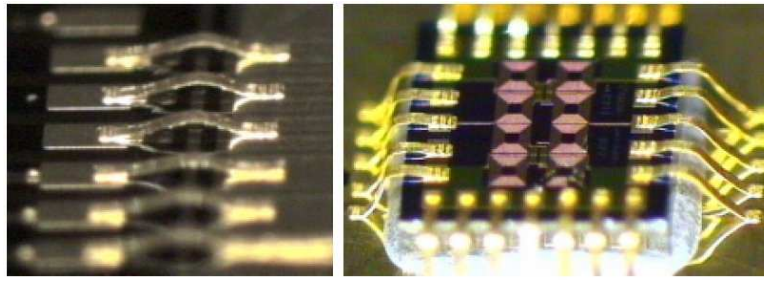


Figure 2.4: *Ribbon bonding for low profile, low loss substrate-to-substrate and MMIC-to-substrate chip attach.* *(Courtesy of Kitron Development)*

in general is the self-aligning with high repeatability. However, it also has some disadvantages: the MMICs must be designed in coplanar configuration to allow direct bonding of signal and ground pads. MMICs usually have a low number of I/Os and therefore only few bumps to handle mechanical stress. Underfill materials for stress relief have typically high dielectric losses and affect the functionality of the MMICs as a consequence of the modified effective dielectric permittivity. Flip chip mounting is also critical as the backside of coplanar chips remain unshielded and the proximity of the carrier substrate and housing can excite parasitic effects.

2.3.5. Module Housing

LTCC (low temperature cofired ceramics), HTCC (high temperature cofired ceramics), thin-film on ceramic, glass, silicon or laminates, milled bulk metals or ceramics and plastic injection molding are but a few of today's available packaging technologies, each with its advantages and disadvantages. To guarantee performance and reliability, millimetre-wave modules found in military and space applications combine the best fitting substrate technologies for each of their components, resulting in complex hybrid substrates. Mixed technologies are also used e.g in wireless baseband transceiver modules, where performance and reliability is more important than form factor and low cost. Figure 2.5 shows an example for a mixed technology transceiver module published in [42]. A 38 GHz transceiver module combining LTCC, flex and FR4 substrates and a metal case, assembled with chip & wire and SMD technologies.

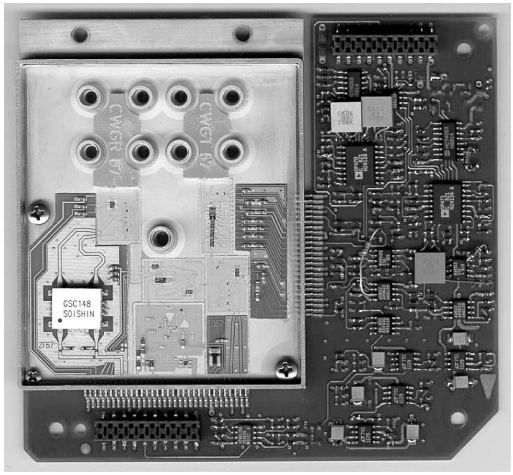


Figure 2.5: *Millimetre-wave transceiver board (65 mm × 61 mm) using mixed technology substrates.* *(Courtesy of EADS)*

In order to avoid performance degradation caused by lossy connectors or impedance mismatches at inputs and outputs, all high frequency signals should be processed as close as possible to the source. If possible only intermediate frequency (IF) signals at few hundred MHz or in the lower GHz frequencies should leave the module. For measurement or test purposes or to offer some minimal modularity various connector standards are available. SMA, V-connectors, W-connectors, waveguides exist today but still with non-negligible losses. And finally, transceiver modules with integrated antennas need to provide antenna access without distorting the radiation pattern.

2.4. Summary

Typical technology constraints occurring at millimetre-wave frequencies and requirements to the substrate technologies in terms of RF performance and mechanical reliability have been presented. Different trade-off assessments were identified as the main reason for the many types of millimetre-wave packaging alternatives existing today. Optimising the technology means therefore to take into account all constraints and to find the appropriate trade-offs which best suit the targeted application.

3

Measuring Technology Performance

While today's software implementations for yield estimation and design optimisation focus on *design centring* for a given technology, the work presented emphasises the improvement of existing technologies and the comparison of technology options. For that purpose a technology benchmark methodology is required which, besides the RF performance, also accounts for high volume production compatibility and typical commercialisation procedures. Hence, it must also include cost and yield trade-off analysis. For this it is important that benchmark results are based on a robust metric considering both absolute and relative performance values.

The first section analyses the relation between the design and the manufacturing of millimetre-wave systems. The main performance determining factors are identified and the *system realisation path* is pre-

sented as interface between technology users and technology suppliers. The second section describes the required benchmark models and parameters. Then, sensitivity analysis and performance measures are introduced to finally propose a consistent and effective method for comparing technologies or technology options. These investigations are motivated by three factors describing a benchmark [43]:

- A benchmark is generally defined as the comparison of one or more candidates (*others*) to a reference (*standard*).
- The comparisons done within a benchmark look for similarities, differences and the quantification of differences.
- Benchmarks are commonly performed to make a decision based on the benchmark results.

3.1. Describing the Design-Manufacturing Relation

3.1.1. System Performance Factors

Before measuring any performance it is necessary to identify the factors that are affecting a system's performance. In the case of millimetre-wave systems we distinguish three elementary performance factors:

1. Quality of design and layout
2. Intrinsic raw material properties
3. Quality of underlying manufacturing technology.

These factors are closely related in the sense that the design and layout strongly depend on the used materials, the choices of materials are connected to the chosen technology topologies and the technologies are chosen to match certain design criteria. To assess the total performance, all three factors must be considered and analysed with the appropriate method. This demands for a mathematical model describing these relations.

3.1.2. The System Realisation Path

A tentative block diagram is depicted in Figure 3.1 and illustrates the above mentioned relations. The following terms are used in the diagram:

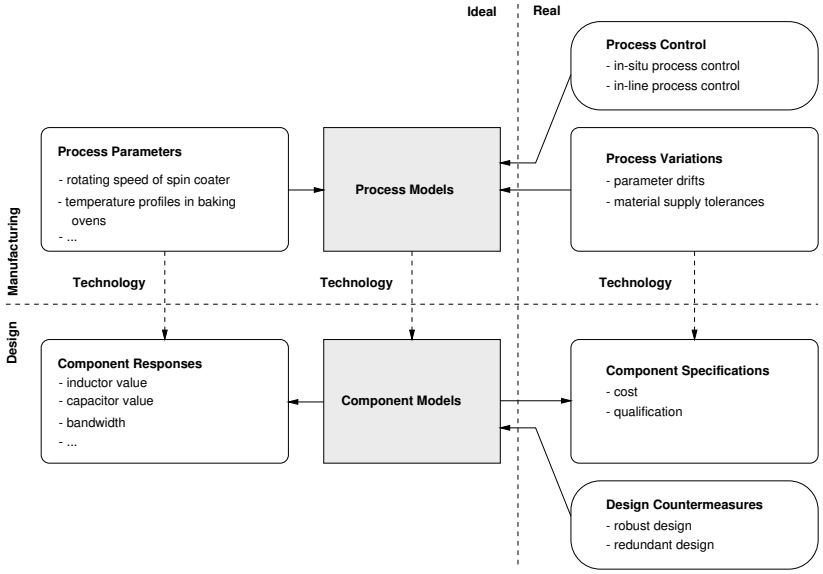


Figure 3.1: *Typical relation between the design and manufacturing as well as the ideal and real domains.*

Process Parameters are the actual control values which confront the process engineers when operating a piece of equipment. Examples are the rotation speed of a spin coater or the temperature profile of a curing oven. These parameters determine the output of a process step such as the thickness of a spin coated layer.

Process Models are describing the effect of changing process parameters and their impact on the process outputs. To find process models, process engineers typically use design of experiments [44] or statistical methods [45]. Process models enable systematic optimisation of process parameters to reach and control the target process outputs.

Process Variations are the distributions of the *real* values around the targeted *ideal* value. Every process step in a manufacturing line is susceptible to process variations. External factors such as humidity or temperature but also internal factors such as tooling inaccuracy can cause process variations. They can be systematic or stochastic and controllable or not.

Process Control is the general term for dealing with process variations. A process parameter can be controlled in-situ for immediate intervention when it starts getting out of target, or in-line when non-conforming process output is recognised to activate any required intervention preventing subsequent incorrect outputs.

Component Responses are the desired component[1] functions, required to make the millimetre-wave system work. Component responses can range from simple interconnection to complex high gain, narrow beam antenna functionality.

Component Models are defining the relation between the topology and the material characteristics of a component and its functional behaviour. RF-system designers have an immense choice of component models available in literature and commercial computer programs. These models range from purely analytical equations up to full-wave finite element methods.

Component Specifications describe the system specific requirements of a certain component. Specifications can include parameters such as cost, reliability, tolerances, maximum losses or size.

Design Countermeasures are dedicated design or layout features aiming at reducing the impact of process variations on component responses. Several methods exist to make components immune to parameter changes such as the inclusion of redundant elements compensating for failing parts.

Figure 3.1 clearly shows that a duality between the design and the manufacturing sides exists but nonetheless the connection remains unclear, especially when the distinction of the *ideal* and the *real* environments of both sides is made. In this context the term *technology* is often used without clarity. To fill this gap a consistent definition is required for what the term *technology* includes and how it is best inserted into the system realisation path.

[1] The model presented uses the term *component* rather than *system*, as the term system also represents a group of components but can also comprise external components such as MMICs and connectors which are not included in the following investigations.

3.1.3. Technology Model

In Figure 3.2 we introduce the *technology model* as unique path between the process model on the manufacturing side and the component model on the design side, covering both the ideal *and* the real environments. The technology model includes for example the topology of dielectric, conductor and special purpose layers, layer profiles and planarities and the used material properties based on the process model outputs. Dimensional and physical properties are defined (or adapted) by the technology model in order to be used in design and simulation tools. Process related parameter variations are also part of the technology model.

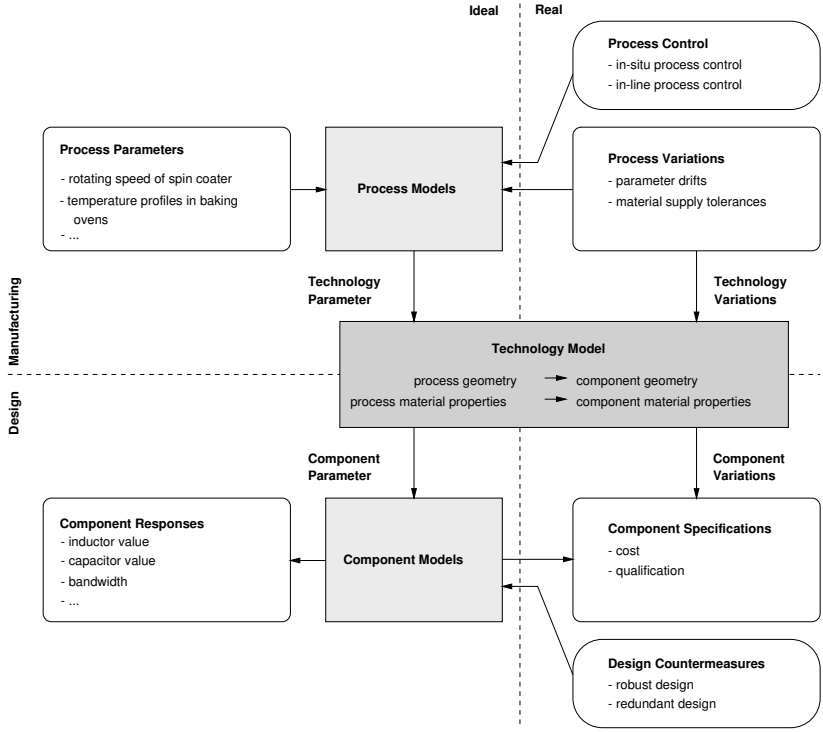


Figure 3.2: *The system realisation path introduces the technology model as unique interface between the technology processing and the component design.*

The system realisation path shown in Figure 3.2 represents the design-manufacturing relation which will serve as reference throughout this work. The theoretical technology performance measures as well as the benchmark tool implementation in the following chapter are both based on the diagram presented above.

3.2. Systematic Approach to the Benchmark Model

3.2.1. Defining Terms

The previous section introduced the system realisation path, separating process models, technology models and component models. For practical use we need to further define these models:

Definition 3.1 – Process Model. $\mathcal{M}_{process}$ *is represented in Figure 3.3(a) and defines the relation between process parameters* $\mathbf{p}$ *and technology parameters* $\mathbf{t}$.

$$\mathbf{t} = \mathcal{M}_{process}(\mathbf{p}) \qquad \text{with } \mathbf{p} = \{p_1, p_2, ...p_n\} \text{ and } \mathbf{t} = \{t_1, t_2, ...t_n\} \tag{3.1}$$

Definition 3.2 – Technology Model. $\mathcal{M}_{technology}$ *is represented in Figure 3.3(b) and defines the relation between technology parameters* $\mathbf{t}$ *and component parameters* $\mathbf{c}$.

$$\mathbf{c} = \mathcal{M}_{technology}(\mathbf{t}) \qquad \text{with } \mathbf{t} = \{t_1, t_2, ...t_n\} \text{ and } \mathbf{c} = \{c_1, c_2, ...c_n\} \tag{3.2}$$

Definition 3.3 – Component Model. $\mathcal{M}_{component}$ *is represented in Figure 3.3(c) and defines the relation between component parameters* $\mathbf{c}$ *and component response parameters* $\mathbf{r}$.

$$\mathbf{r} = \mathcal{M}_{component}(\mathbf{c}) \qquad \text{with } \mathbf{c} = \{c_1, c_2, ...c_n\} \text{ and } \mathbf{r} = \{r_1, r_2, ...r_n\} \tag{3.3}$$

Cascading the three models as represented in Equation 3.4 combines the process parameters, the technology parameters and the final component responses, thus describing the entire system realisation path.

$$\mathbf{r} = \mathcal{M}_{component}\Big(\mathcal{M}_{technology}\Big(\mathcal{M}_{process}(\mathbf{p})\Big)\Big) \tag{3.4}$$

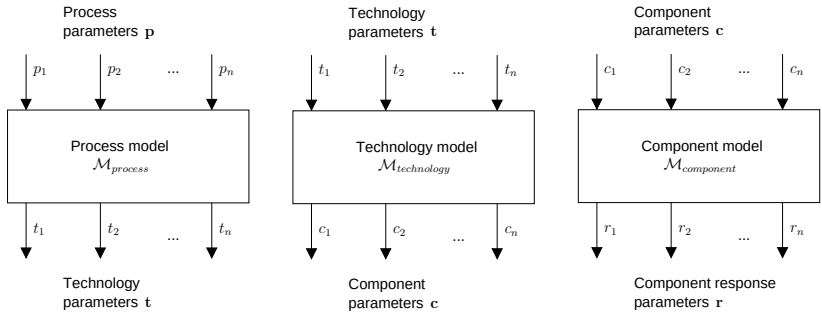


Figure 3.3: *General relation of input and output parameters for the process, the technology and the component models, respectively.*

3.2.2. Technology Benchmark Model

At this point we must remember that the goal of this work is not to characterise processes but to compare and benchmark technologies and their suitability for millimetre-wave system integration. For this it is assumed that the manufacturers supplying the investigated technologies use their own process models or have other methods to set up their process parameters. They should be able to provide technology parameters or at least technology samples which allow measurement and extraction of the required parameters. In this case the benchmark starts with the technology parameters $\mathbf{t}$ and the required benchmark model defined as follows:

Definition 3.4 – Benchmark Model. *The following benchmark model $\mathcal{M}_{benchmark}$ results from cascading $M_{technology}$ and $M_{component}$ and with $\mathbf{t}$ as input parameters and $\mathbf{r}$ as output response parameters:*

$$\mathbf{r} = \mathcal{M}_{benchmark}(\mathbf{t}) = \mathcal{M}_{component}\Big(\mathcal{M}_{technology}(\mathbf{t})\Big) \tag{3.5}$$

Of course, process models must qualitatively be considered in order to analyse and understand the behaviour and the variation distributions of the technology parameters.

3.2.3. Parameter Variations

The system realisation path has mentioned that process parameters are exposed to process variations which then propagate through the cascaded models to finally affect the component responses. More variations also occur at the technology level and add to the process variations to further affect the component responses. The sources of variations are manifold and in general characteristic for the affected parameters.

The ideal values without variations are the targets T_{p_i}, T_{t_i}, T_{c_i} and T_{r_i} while p_i, t_i, c_i and r_i denote those parameters exposed to variations. We distinguish four cases depending on the occurrence and distribution of the variations:

Definition 3.5 – Statistically distributed, based on SPC data. *These data are collected during processing with a significant high number of measurements for statistical relevance. These parameters are marked with a dot:* $\dot{p}_i$, $\dot{t}_i$, $\dot{c}_i$ *and* $\dot{r}_i$.

Definition 3.6 – Statistically distributed, based on estimated data. *These data are estimated values for a process under development but based on a similar, statistically controlled process. These parameters are marked with a hat:* $\hat{p}_i$, $\hat{t}_i$, $\hat{c}_i$ *and* $\hat{r}_i$.

Definition 3.7 – Distributed because of uncertainties. *Some input values differ depending on the source providing these data such as different suppliers, data sheets or publications. These parameters are marked with a tilde:* $\tilde{p}_i$, $\tilde{t}_i$, $\tilde{c}_i$ *and* $\tilde{r}_i$.

Definition 3.8 – Distributed based on sampled data. *These data are collected during process tests with a reduced number where statistical significance is not guaranteed. These parameters are marked with a check:* $\check{p}_i$, $\check{t}_i$, $\check{c}_i$ *and* $\check{r}_i$.

The underlying distribution functions strongly depend on the nature of the variations. From a mathematical point of view, normal distribution is preferred and fortunately applicable in most situations (how to treat non-normally distributed data is described in Section 3.3.4). Parameter variations are commonly expressed using the concept of *accuracy* and *precision* [45]. As illustrated in Figure 3.4, the accuracy denotes the offset of the distribution mean from the target T and the precision is a measure for the spread of the variation around its mean value.

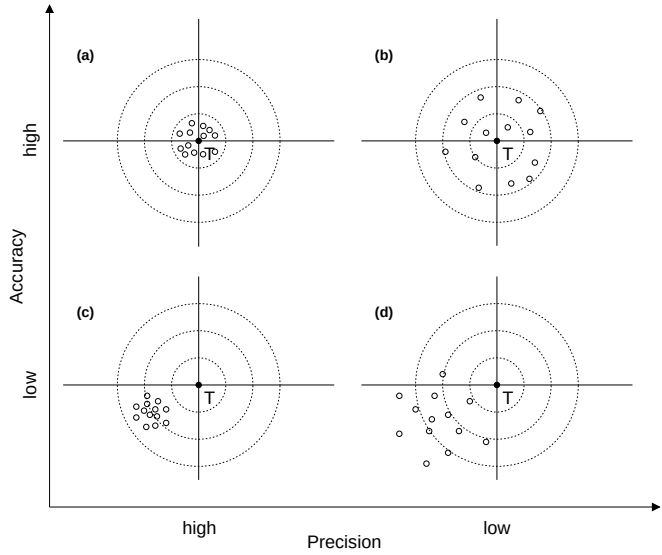


Figure 3.4: *Concept of accuracy and precision: (a) the distribution is accurate and precise, (b) the distribution is accurate but not precise, (c) the distribution is not accurate but precise and (d) the distribution is neither accurate nor precise (*T *= target).*

3.2.4. Model Accuracy

Every model has its inaccuracies as it is only an abstract representation of the reality. But inaccuracies are not necessarily to be a disadvantage, it is however important to know where they may occur. Figure 3.5 shows the cascaded diagram of the system realisation path including the individual sources of errors.

3.3. Performance Analysis Methods

3.3.1. Sensitivity Analysis

Sensitivity analysis tells us how much each technology parameter variation contributes to the component response variations. The simplest and most effective way to do this is the one-parameter-at-a-time (OPAT) approach where all component responses in $\mathbf{r}$ are determined for one technology parameter t_i varying while all other parameters re-

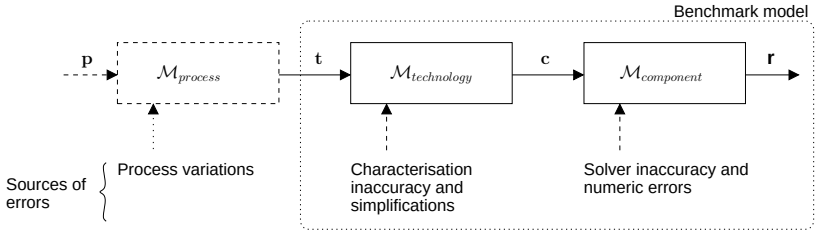


Figure 3.5: *Cascaded process, technology and component models showing the potential sources of errors. The dotted rectangle represents the* benchmark model.

main on their target values $T_{t_{\tilde{i}}}$. This gives us an $n \times n$ input matrix $\mathbf{t}_{OPAT}$ (Equation 3.6) where n is the size of $\mathbf{t}$, for which we get the sensitivity vectors $\mathbf{r}'$ (Equation 3.7). Another popular method to analyse interactions of input and output parameters are *design of experiment* (DOE) and fractional DOE [44]. But the goal and the strength of DOE is to optimise input parameters with minimised effort. DOE does not however provide full sensitivity information and it becomes a complex procedure with more than four input parameters [45].

$$\mathbf{t}_{OPAT} = \begin{pmatrix} t_1 & T_{t_2} & T_{t_3} & \dots & T_{t_n} \\ T_{t_1} & t_2 & T_{t_3} & \dots & T_{t_n} \\ T_{t_1} & T_{t_2} & t_3 & \dots & T_{t_n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ T_{t_1} & T_{t_2} & T_{t_3} & \dots & t_n \end{pmatrix} \tag{3.6}$$

$$\mathbf{r}' = \mathcal{M}_{benchmark}(\mathbf{t}_{OPAT}) \tag{3.7}$$

It is important at this point to remember that all model parameters are in fact distributions according to the Definitions 3.5 to 3.8. When varying t_i while doing the OPAT analysis it is therefore very important how the variation values are chosen. If the variation of t_i is a continuous distribution function then its $\mathbf{r}'$ response vector elements are also continuously distributed. For the sensitivity analysis, however, two variation values are sufficient: a *lower variation value* (L) and an *upper variation value* (U). Depending on the goal of the analysis and on how the parameter distributions are defined, several options exist to choose these values:

- For normally distributed $\dot{t}_i$: L_{t_i} and U_{t_i} are $\pm 3\sigma$.
  (σ = standard deviation)
- For normally distributed $\hat{t}_i$: L_{t_i} and U_{t_i} are $\pm 3\hat{\sigma}$.
- Uncertain $\tilde{t}_i$ can be regarded as uniform distribution between the minimum and the maximum known values. In this case L_{t_i} and U_{t_i} are $\min(\tilde{t}_i)$ and $\max(\tilde{t}_i)$.
- For sampled $\check{t}_i$: L_{t_i} and U_{t_i} are $\pm 3s$.
  (s = sample standard deviation)

Using L_{t_i}, T_{t_i} and U_{t_i} for each technology parameter we get for each response vector element $r'_i \in \mathbf{r'}$ three values $L_{r'}$, $T_{r'}$ and $U_{r'}$ forming the response *sensitivity vector* r' represented with the *sensitivity graph* (Figure 3.6). The different line end types denote the polarity L_{t_i} and U_{t_i} of the technology parameter variations (see also graph legend).

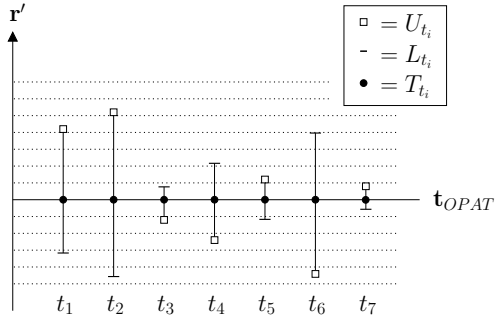


Figure 3.6: *The sensitivity graph shows for each input parameter t_i and its lower variation limit L_{t_i}, upper variation limit U_{t_i} and target T_{t_i} the corresponding values of r' – the sensitivity vector.*

3.3.2. Parameter Interaction

The OPAT sensitivity analysis treats each parameter individually to suppress any parameter interaction. Interaction means that the influence of one parameter variation depends on the actual value of another parameter. To fully account for all interactions of n parameters, all combinations of fixed and varied parameters would be necessary, thus generating a very large $n \times (2^n - 1)$ matrix. Technology vectors

$\mathbf{t}$ with up to ten parameters t_i are quite common and would yield a matrix of 10×1023 parameters. In practical use however, the OPAT shows that only few technology parameters significantly affect a single component response $r \in \mathbf{r}$. Hence, the few dominating technology parameters of each r are selected and their interaction is analysed in all combinations of two parameters each. This method is introduced as the *two-parameter-at-a-time* (STPAT) analysis providing interaction information of any two parameters. For this the selected parameters are combined in the STPAT matrix $\mathbf{t}_{STPAT}$ for which the two-parameter sensitivity vectors $\mathbf{r}''$ is generated. An example with three dominant technology parameters t_1, t_2 and t_6 in the sensitivity graph in Figure 3.6 is shown in the Equations 3.8 and 3.9.

$$\mathbf{t}_{STPAT} = \begin{pmatrix} t_1 & t_2 & T_{t_6} \\ t_1 & T_{t_2} & t_6 \\ T_{t_1} & t_2 & t_6 \end{pmatrix} \tag{3.8}$$

$$\mathbf{r}'' = \mathcal{M}_{benchmark}(\mathbf{t}_{STPAT}) \tag{3.9}$$

If we consider continuous variations of two parameters t_i and t_j for an STPAT analysis, each response vector element of $\mathbf{r}''$ would span a variation surface. To reduce this large amount of information, the same two variation values $L_{t_{i/j}}$ and $U_{t_{i/j}}$ are used in all four possible combinations. For each response vector element of $\mathbf{r}''$ we get the five values $UU_{\mathbf{r}''}$, $UL_{\mathbf{r}''}$, $LU_{\mathbf{r}''}$, $LL_{\mathbf{r}''}$ and $TT_{\mathbf{r}''}$. These response vectors can be represented with the *interaction graph* depicted in Figure 3.7. The different line end types denote the polarity combinations UU_{t_i}, UL_{t_i}, LU_{t_i} and LL_{t_i} for each technology parameter variation (see also graph legend).

For each parameter pair t_i and t_j an interaction ratio I_{ij} can now be calculated. The interaction ratio is defined in Equation 3.10 and represents the proportional response parameter change for a one-parameter and a two-parameter variation analysis.

$$I_{ij} = \frac{\mathbf{r}''(t_i, t_j)}{\mathbf{r}'(t_i) + \mathbf{r}'(t_j)} \tag{3.10}$$

An interaction ratio $I_{ij} = 1$ means no interaction, $I_{ij} < 1.0$ represents positive interaction and $I_{ij} > 1.0$ compensating interaction. The interaction ratio denotes if varying one parameter increases or decreases the sensitivity of another parameter. A ratio of for example $I_{ij} = 1.03$ means that the two parameters are increasing the sensitivity of each other by 3% within the variation range.

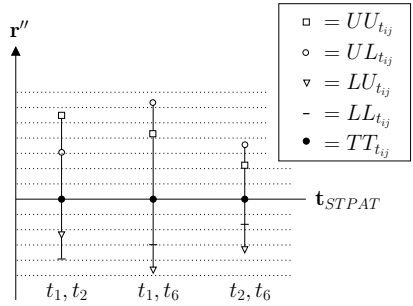


Figure 3.7: *The interaction graph shows the values of r'' for the four possible combinations upper and lower variations for two input parameters t_i and t_j plus its target values.*

3.3.3. Capability and Performance Measures

Capability and performance measures are widely used in the fields of process development and process control. While the process capability is a common evaluation metric, the term *capability* implies that a statistical significance is demonstrated. This is per definition the case in fabrication environments following the 6σ strategy [46]. To cope with process data before statistical control, the metric of process performance was introduced. It provides information concerning how well the process is performing and how it may be employed before being statistically controlled [47].

Performance measurement requires two prerequisites: first, a metric that quantifies a certain response and secondly, a reference to which the performance of the measured response can be rated. In a manufacturing process this is done by assigning a target T_i and specification limits USL_i (upper specification limit) and LSL_i (lower specification limit) to each technology parameter t_i. The process capabilities or process performances are then quantified with the difference of the measured parameter t_i and its target T_i and the measured parameter distribution (standard deviation σ) within the upper and lower specification limits.

Existing Measures for Process Control

In statistical process control a large variety of capability and performance measures exist. The definitions listed below give a brief overview of the most popular ones used today. Capability measures are based on

statistical values represented by the mean μ and the standard deviation σ while the performance measures are typically based on sampled data represented by the sample mean $\bar{X}$ and the sample variance s^2. These measures are however restricted to process data which are reasonably normally distributed [48].

Two-sided[2] process capability ratio:

$$C_p = \frac{USL - LSL}{6\sigma} \tag{3.11}$$

Estimated process capability ratio:

$$\hat{C}_p = \frac{USL - LSL}{6\hat{\sigma}} \tag{3.12}$$

One-sided[3] process capability ratio:

$$C_{pU} = \frac{USL - \mu}{3\sigma} \qquad \text{and} \qquad C_{pL} = \frac{\mu - LSL}{3\sigma} \tag{3.13}$$

Process capability ratio for off-centre process:

$$C_{pk} = min(C_{pU}, C_{pL}) \tag{3.14}$$

Extended process capability ratio accounting for off-centre process:

$$C_{pm} = \frac{USL - LSL}{6\tau} = \frac{USL - LSL}{6\sqrt{\sigma^2 + (\mu - T)^2}} \tag{3.15}$$

with

$$\tau = \sqrt{\sigma^2 + (\mu - T)^2} \tag{3.16}$$

where τ is the square root of the expected squared deviation from target T.

Process performance ratio:

$$P_p = \frac{USL - LSL}{6s} \tag{3.17}$$

[2]Two-sided = double-sided = bilateral
[3]One-sided = single-sided = unilateral

Estimated process performance ratio:

$$\hat{P}_p = \frac{USL - LSL}{6\hat{s}} \tag{3.18}$$

Extended process performance ratio accounting for off-centre process:

$$P_{pm} = \frac{USL - LSL}{6\sqrt{s^2 + \frac{n}{n-1}(\bar{X} - T)^2}} \tag{3.19}$$

Measures for Technology Benchmarks

All the above listed measures for process capability and process performance can be translated to *technology* capability and performance. We get C_{tU} (Equation 3.20), C_{tL} (Equation 3.21), C_{tm} (Equation 3.22), P_{tU} (Equation 3.23), P_{tL} (Equation 3.24) and P_{tm} (Equation 3.25). General terms for technology capability or performance are C_t and P_t, respectively.

$$C_{tU} = \frac{USL - \mu}{3\sigma} \tag{3.20}$$

$$C_{tL} = \frac{\mu - LSL}{3\sigma} \tag{3.21}$$

$$C_{tm} = \frac{USL - LSL}{6\sqrt{\sigma^2 + (\mu - T)^2}} \qquad \text{with } USL, LSL, T, \sigma, \mu \text{ from } r_i \tag{3.22}$$

$$P_{tU} = \frac{USL - \bar{X}}{3s} \tag{3.23}$$

$$P_{tL} = \frac{\bar{X} - LSL}{3s} \tag{3.24}$$

$$P_{tm} = \frac{USL - LSL}{6\sqrt{s^2 + \frac{n}{n-1}(\bar{X} - T)^2}} \qquad \text{with } USL, LSL, T, s, X \text{ from } r_i \tag{3.25}$$

The one-sided capability and performance ratios are used for technology parameters which do not have a fixed target value but must be as low or as high as necessary beyond a specified limit. Typical examples

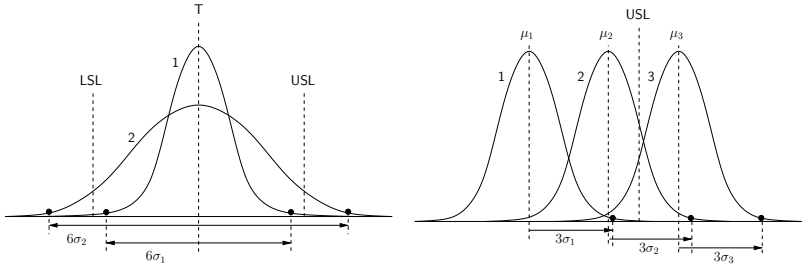
are the transmission losses per unit length of interconnect transmission lines.

Compared to C_p and P_p, the goals of C_t and P_t are to benchmark the potential performance of existing or new technologies, where centred designs can be assumed. For two-sided parameters this means that the *precision* is decisive rather than the *accuracy*. For C_{tm} and P_{tm} we therefore expect following values (see Figure 3.8(a)):

$$\begin{array}{lcl} 1 \leq \{C_{tm},\, P_{tm}\} & : & 6\sigma \text{ is within specifications limits.} \\ 0 < \{C_{tm},\, P_{tm}\} < 1 & : & 6\sigma \text{ is outside specifications limits.} \end{array}$$

For one-sided parameters the value ranges for $C_{tU/L}$ and $P_{tU/L}$ are different as the technologies are not centred around a target (see Figure 3.8(b)):

$$\begin{array}{lcl} 1 \leq \{C_{tU/L},\, P_{tU/L}\} & : & 3\sigma \text{ is within specifications limits.} \\ 0 \leq \{C_{tU/L},\, P_{tU/L}\} < 1 & : & 3\sigma \text{ is outside, but parameter mean } \mu \\ & & \text{within specifications limits.} \\ 0 > \{C_{tU/L},\, P_{tU/L}\} & : & 3\sigma \text{ and parameter mean } \mu \text{ are outside} \\ & & \text{specifications limits.} \end{array}$$



(a) two-sided (b) one-sided

Figure 3.8: *Parameter distribution ranges for calculation of C_{tm} and P_{tm} for two-sided (a) and one-sided (b) parameters.*

C_t and P_t can now be determined for any response parameter r_i, so the question arises about the total capability or performance of $\mathbf{r}$. The individual values of $C_t(r_i)$ or $P_t(r_i)$ must be combined to form

one single value for $C_t(\mathbf{r})$ or $P_t(\mathbf{r})$ respectively. Here, two cases are differentiated:

Case A: All $C_t(r_i)$ or $P_t(r_i)$ values are greater than 1, therefore the technology passes the 6σ requirements. Each $C_t(r_i)$ or $P_t(r_i)$ is then regarded as an individual chain link and the weakest link determines the capability or performance of the total chain. We get $C_t(\mathbf{r}) = min(C_t(r_i))$ and $P_t(\mathbf{r}) = min(P_t(r_i))$ and call it *least capable response* or *least performing response*.

Case B: If at least one $C_t(r_i)$ or $P_t(r_i)$ value is smaller than 1, the technology fails the 6σ requirements. Therefore we must consider all responses which do not contribute to the 6σ quality and take all $C_t(r_i)$ or $P_t(r_i)$ into account which are smaller than 1. These values are then multiplied to get the single-number capability $C_t(\mathbf{r})$ (*product of non-capable responses*)

$$C_t(\mathbf{r}) = \prod_{i \forall C_t(r_i) < 1} C_t(r_i) \tag{3.26}$$

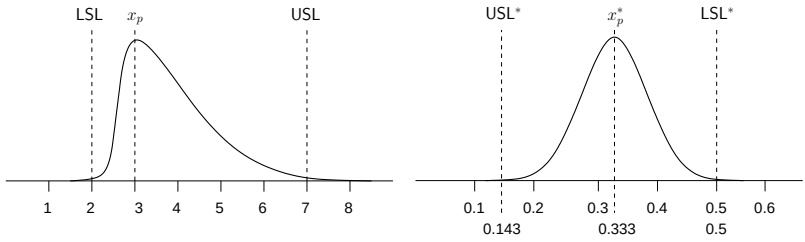
and performance $P_t(\mathbf{r})$ (*product of non-performing responses*)

$$P_t(\mathbf{r}) = \prod_{i \forall P_t(r_i) < 1} P_t(r_i). \tag{3.27}$$

3.3.4. C_t and P_t with Non-normal Distributions

It was mentioned in the beginning that the capability and performance ratios are valid under the assumption of normally distributed data. A common method to dealing with skewed (non-normal) distributions is the use of *reciprocal transformation* illustrated in Figure 3.9 [45]. The example in Figure 3.9(a) has specification limits $LSL = 2$, $USL = 7$ and a distribution with skewed peak at $x_p = 3$. With the reciprocal transformation $x^* = 1/x$ the specification limits become $LSL^* = 0.5$ and $USL^* = 0.143$ and the distribution gets a normal appearance with peak $x_p^* = 0.333$ (Figure 3.9(b)). The transformed data and specification limits allow calculation of technology capability and performance ratios giving realistic results.

For highly non-normal distributions where the mean value and the standard deviation are not reflecting the parameter performance, the best method is to run a Monte Carlo simulation using the parameter's



(a) non-normal (b) transformed

Figure 3.9: *Reciprocal transformation applied to skewed distribution (a) resulting in distribution with normal appearance (b).*

benchmark models. The generated simulation data can then be statistically analysed to compute the technology performance ratios. The values within which 99.73% of the best performing (closest to T) generated data lie are delimiting the 6σ range and the distribution frequency peak is used instead of the distribution mean μ.

3.3.5. Calculating the Parameter Yields

All statistical values and performance measures used in the previous sections are in fact very similar to *yield calculation*. Instead of comparing the specification limits with the 6σ limits of the technology response distribution, we calculate the total probability within the specification limits and get the individual component parameter yields Y. The yield value is an important factor when comparing technologies as it affects the technology's total manufacturing costs. For normally distributed parameters the yields are calculated using P_t and the Equations 3.28 or 3.29 for two-sided or one-sided cases respectively.

$$Y_{two-sided} = P_t \cdot 99.73\% \tag{3.28}$$

$$Y_{one-sided} = \frac{(1 + P_t)}{2} \cdot 99.73\% \tag{3.29}$$

Yield with Correlated Parameters

Simplified, the total component yield Y_{total} is the product of the individual component parameter yields. But in the case of correlated component parameters this would lead to over-pessimistic yield numbers. For correct total yield calculation the parameter correlation needs to be extracted from the sensitivity graphs and its sensitivity vectors $\mathbf{r}'$. For every component response parameter r_i, r'_i reveals how much each parameter contributes to the total variation of r_i. These contributions are then set in relation with each other to form the *relative variation contribution vector* $\mathbf{cr}_i$. This vector has the length n corresponding to the number of technology parameters and the sum of all vector elements is 1 (Equation 3.30).

$$\mathbf{cr}_i = \left[\begin{array}{cccccc} cr_{i_1} & cr_{i_2} & cr_{i_3} & \dots & cr_{i_n} \end{array} \right] \qquad \text{with} \qquad \sum_n cr_{i_n} = 1 \tag{3.30}$$

For every component response parameter r_i a correlation factor K_i is then computed, representing its correlation with all other response parameters $r_{\bar{i}}$ (Equation 3.31).

$$K_i = \sum_{j=1}^{n} \left(\frac{\min\left(cr_{i_j}, \text{mean}(cr_{\bar{i}_j})\right)}{\max\left(cr_{i_j}, \text{mean}(cr_{\bar{i}_j})\right)} cr_{i_j} \right) \tag{3.31}$$

The total mutual correlation factor K_{total} is the arithmetic mean of the individual factors (Equation 3.32).

$$K_{total} = \sum_{i=1}^{m} \frac{K_i}{m} \tag{3.32}$$

where cr_{i_j} *are the elements of the relative variation contribution vectors* $\mathbf{cr}_i$,
$\mathbf{cr}_{\bar{i}}$ *is the set of vectors* $\mathbf{cr}$ *minus* $\mathbf{cr}_i$,
n *is the length of each vector* cr_i, *and*
m *is the number of response parameters for which exist a vector* $\mathbf{cr}_i$ *and a correlation factor* K_i.

With the total mutual correlation factor K_{total} and the individual component parameter yields Y_i the total component yield Y_{total} is calculated according to Equation 3.33.

$$Y_{total} = \prod_i Y_i + \left(\min(Y_i) - \prod_i Y_i \right) K_{total} \tag{3.33}$$

Example for Parameter Correlation

To demonstrate correlated parameters we take an example consisting of an arbitrary component with three response parameters $\mathbf{r} = \{r_1, r_2, r_3\}$ and an underlying technology with also three parameters $\mathbf{t} = \{t_1, t_2, t_3\}$. The three individual component parameter yields are Y_1, Y_2 and Y_3. The OPAT analysis gives the three sensitivity vectors r'_i and from them we get the relative variation contribution vectors cr_i with the arbitrary values listed below. To demonstrate different correlations between r'_1, r'_2 and r'_3, we define five different values for cr_3 and combine them in an array of vectors.

$$\mathbf{cr}_1 = [cr_{1_1}\, cr_{1_2}\, cr_{1_3}] = \begin{bmatrix} 1.0 & 0.0 & 0.0 \end{bmatrix} \tag{3.34}$$

$$\mathbf{cr}_2 = [cr_{2_1}\, cr_{2_2}\, cr_{2_3}] = \begin{bmatrix} 1.0 & 0.0 & 0.0 \end{bmatrix} \tag{3.35}$$

$$\mathbf{cr}_3 = [cr_{3_1}\, cr_{3_2}\, cr_{3_3}] = \begin{bmatrix} 0.0 & 0.0 & 1.0 \\ 0.2 & 0.2 & 0.6 \\ 0.5 & 0.5 & 0.0 \\ 0.9 & 0.9 & 0.0 \\ 0.97 & 0.01 & 0.02 \end{bmatrix} \tag{3.36}$$

Figure 3.10 shows the three example response yields Y_1, Y_2 and Y_3. Y_1 and Y_2 are kept constant at 80% and 40% while Y_3 is varied from 0% to 100%. In the resulting graphs we can observe how the total component yield is moving towards the minimum yield with increasing correlation. The total mutual correlation factor K_{total} of the technology parameters is calculated for the sensitivity vectors $\mathbf{r}'_i$ using the relative variation contribution vectors $\mathbf{cr}_i$ and the Equations 3.31 and 3.32. K_{total} varies from 0.0 to 0.99.

3.3.6. The Cost Performance-Pareto Graph

With each component's total yield Y_{total} we are now able to calculate the total component costs for all compared technologies. The total costs versus the corresponding total technology performance ratios P_t form a pareto front as illustrated in Figure 3.11. The pareto graph

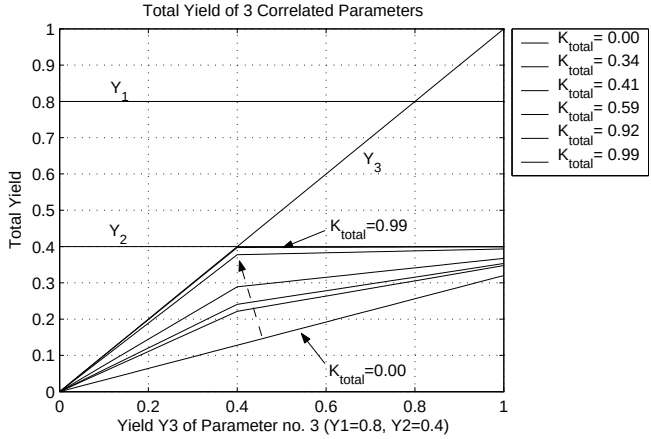


Figure 3.10: *Total yield for three correlated input variables with total mutual correlation factor K_{total} increasing from 0.00 to 0.99 and one component's parameter yield varying from 0% to 100%.*

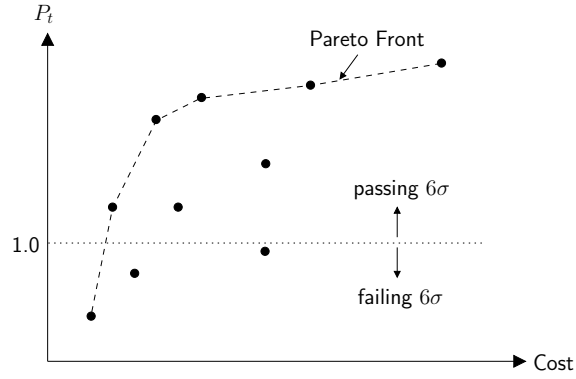


Figure 3.11: *Pareto graph for 10 different technology alternatives with their total cost ranges versus the technology performance ratio P_t.*

is a widely used visualisation method that helps to identify the best cost-performance trade-offs. It is most useful when many, not clearly distinguishable options exist or when other external parameters need to be taken into consideration. The pareto graph for technology performance benchmarking also shows the separation of those technologies failing the 6σ limits from those passing it which is the case when the performance ratio drops below 1.

3.4. Summary

In this chapter a technology performance metric was developed based on the *benchmark model* introduced with the *system realisation path*. The basic idea behind the performance metric is already known from process capability and performance characterisation and was adapted here for technology benchmarking. It calculates a value that represents the distribution of the technology parameters within specified limits. This value also allows the computation of yield estimations and therefore to quantitatively compare technology alternatives.

4

Benchmark Tool Implementation

This chapter describes the software implementation of the technology performance measures introduced in the previous chapter. A set of Matlab® functions is presented, representing a *virtual processing* environment for fast and flexible comparison of different technologies in terms of millimetre-wave performance. This *benchmark tool* is based on the benchmark model defined in Chapter 3 and consists of a set of generic RF component models and a custom set of technology models. The use of generic RF components has the advantage that quantitative performance comparisons can be done with no need for completed system designs. This means that the optimum technology can be found before the target system is fully specified or without disclosure of confidential design informations.

In the first section, the software structure is explained then the individual software elements are described and exemplified by means of an arbitrary microstrip line and an arbitrary technology. The chapter concludes with the description of benchmark assessment functions and

the interpretation of results.

4.1. Software Structure

The software of the benchmark tool consists of a set of dedicated functions for virtual processing of millimetre-wave components, technology performance comparison and benchmark result assessment. The functions are separated in three blocks and organised in five groups:

- Block 1: *Benchmark Project Description* (`projects`)
- Block 2: *Virtual Processing* (`components`, `functions`, `process`)
- Block 3: *Benchmark Result Assessment* (`visualize`)

The first block (*Benchmark Project Description*) contains the specifications of the investigated technologies, a choice of generic RF components, the assignment of these components to the technologies and the component specifications according to a benchmark reference application. This separation corresponds to the *technology model* and the *component specifications* in the product realisation path presented in Chapter 3.

The second block (*Virtual Processing*) contains the most important building blocks: the parameterised models for the supported generic RF components. These blocks are in fact not visible to the user but can, if necessary, be completed with new component models.

The third block (*Benchmark Result Assessment*) finally computes the technology performance and capability ratios and generates all graphical outputs. Parameter monitors can be displayed for each component to show its characteristics and performance independently from given specifications. These monitors are mainly used to set up the benchmark components, to check parameter dependencies and sensitivities and to trace back causes for performance losses. Finally, the comparison windows line up the technologies' component performances and summarise the total technology performance ratios and yields.

The strength of these graphical outputs is the visualisation of the relations between process parameters and RF component performance. The resulting graphs point out the process variation sensitivities of performance and cost relevant parameters.

4.2. Component Models

We remember that the main goal of the component models is focused on performance estimations for technology alternatives rather than optimisation of RF designs and layouts. This focus allows us to reduce the complexity of the models making them easier and faster to use, especially compared to 3-dimensional full-wave EM simulation tools. Many components can therefore be reduced to their key parameters and some can be combined into groups of components having the same performance defining parameters.

Component models are provided for generic RF components which build the core of the benchmarking tool and are part of the software block 2: *Virtual Processing and Monitoring*. These components are stored in the `components/` folder. Any performance calculation is done for a user-defined selection of one or several of these components. The individual models do not necessarily consist of one single function, they usually access other simple functions which in turn are used for other models. One example is the parameterised equation to calculate the increase of ohmic losses caused by surface roughness.

General mathematical functions for result computations are found in the `functions/` folder. One example is the reflection calculation function for cascaded transmission lines. For the virtual processing of the generic components each model is provided with a `_process.m` function stored in the `process/` folder. The virtual processing consists of performing a one-parameter-at-a-time (OPAT) and a selective two-parameter-at-a-time (STPAT) simulation with every input parameter for every output parameter (see Chapter 3).

The generic RF components are divided into three distinctive categories: interconnect transmission lines, lumped passives and distributed passives. The available components and their underlying models are described in the following subsections.

4.2.1. Transmission Line Models

The relevant transmission line parameters are the characteristic impedance, transmission losses, resonance frequency and minimum design rules. Complete and accurate closed form expressions and equations for microstrip lines and coplanar waveguides (CPW) can be found in the literature. For striplines and grounded coplanar waveguides (GCPW) equations exist but with less accuracy and flexibility. The following paragraphs are elaborating on microstrip and CPW lines

providing accurate models for use in the benchmark tool. Striplines and GCPW are not included in these investigations but remain the subject of future work.

Microstrip Lines

Many closed form equations for calculating the relevant microstrip parameters have been proposed in various publications [49, 50, 51, 52, 53], some claiming an accuracy with errors below 1%. The model used for this work supports the parameters listed in Table 4.1. *Note: The target frequency f is the frequency for which the response parameters are calculated. The resonance frequency f_{res} is calculated independently of f and depends on the specified microstrip conductor length l.*

Table 4.1: *Microstrip component input parameters* $\mathbf{c}$ *and response parameters* $\mathbf{r}$.

component parameters	$\mathbf{c}$	response parameters	$\mathbf{r}$
conductor width	$c_1 = w$	characteristic impedance	$r_1 = Z_0$
conductor thickness	$c_2 = t$	line width extension	$r_2 = w_{ext}$
conductor length	$c_3 = l$	effective diel. permittivity	$r_3 = \epsilon_{r_{eff}}$
dielectric thickness	$c_4 = h$	skin depth	$r_4 = \delta$
dielectric permittivity	$c_5 = \epsilon_r$	total insertion losses	$r_5 = \alpha$
dielectric loss tangent	$c_6 = \tan\delta$	dielectric losses	$r_6 = \alpha_d$
metal conductivity	$c_7 = \sigma$	conductor losses	$r_7 = \alpha_c$
metal surface roughness	$c_8 = R_q$	surface roughness losses	$r_8 = \alpha_{R_q}$
target frequency	$c_9 = f$	resonance frequency	$r_9 = f_{res}$

The model starts with checking the conductor thickness t. If it is non-zero the equivalent line width extension $w_{eq} = w + w_{ext}$ must be calculated using Wheelers Equations 4.1 and 4.2 [29].

$$w_{eq0} = w + \frac{t}{\pi} \cdot \ln\left(1 + \frac{4 \cdot \exp(1)}{\frac{t}{h} \cdot \coth^2\left(\sqrt{6.517 \cdot \frac{w}{h}}\right)}\right) \tag{4.1}$$

$$w_{ext} = \frac{w_{eq0} - w}{2} \cdot \left(1 + \frac{1}{\cosh(\sqrt{\epsilon_r - 1})}\right) \tag{4.2}$$

The next step is to calculate the effective relative permittivity $\epsilon_{r_{eff}}$ and the characteristic impedance Z_0. For this we use the accurate derivations described in Schnieder et al. [54] based on the formulas of Hammerstad and Jensen [49].

With $\epsilon_{r_{eff}}$ and the light speed c_0 we get the propagation velocity

$$v_p = \frac{c_0}{\sqrt{\epsilon_{r_{eff}} \cdot \mu_r}} \tag{4.3}$$

and the dielectric losses

$$\alpha_d = \frac{\pi \cdot f}{v_p} \cdot \frac{\epsilon_r}{\epsilon_{r_{eff}}} \cdot \frac{\epsilon_{r_{eff}} - 1}{\epsilon_r - 1} \cdot \tan(\delta) \qquad \text{[neper/m]} \tag{4.4}$$

and

$$\alpha_d = \frac{\pi \cdot f}{v_p} \cdot \frac{\epsilon_r}{\epsilon_{r_{eff}}} \cdot \frac{\epsilon_{r_{eff}} - 1}{\epsilon_r - 1} \cdot \tan(\delta) \cdot \frac{20}{\ln(10)} \qquad \text{[dB/m].} \tag{4.5}$$

For the conductor loss calculation we first determine the skin depth δ at target frequency f:

$$\delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \tag{4.6}$$

Here we must distinguish three cases depending on δ and the conductor thickness t. Case 1: If $t = 0$, perfect electric conductor is assumed, hence the conductor losses are set to zero. Case 2: If $0 < t < \delta$, Equation 4.7 based on the DC resistance value is used while Z_L stands for the microstrip line's characteristic impedance for the lossless case (see also Schnieder et al. [54]).

$$\alpha_c = \frac{1}{w_{eq} t \sigma} \cdot \frac{1}{2 Z_L} \tag{4.7}$$

Case 3: If $t \geq \delta$, the skin effect starts reducing the cross-sectional area for the current flow, thus increasing the ohmic losses. For this case the full derivation of α_c is found in Schnieder et al. [54]. A warning is given if $t < 3\delta$, as this is the transition range between pure DC resistance (Case 2) and the well developed skin effect resistance. The applied loss calculation formulas tend to give inaccurate results within this transition, the same as with many commercial EM-tools.

The conductor's surface roughness is taken into account with Equation 4.8 which calculates the increase of α_c as a function of the RMS surface roughness R_q and the skin depth δ.

$$\alpha_r = \alpha_c \cdot \frac{2}{\pi} \cdot \tan^{-1}\left(1.4 \cdot \left(\frac{R_q}{\delta}\right)^2\right) \tag{4.8}$$

The total insertion loss is now given with Equation 4.9.

$$\alpha = \alpha_d + \alpha_c + \alpha_r \tag{4.9}$$

The half wavelength resonance frequency $f_{res_{\lambda/2}}$ of a microstrip line is given with Equation 4.10 using the microstrip line length l and the effective dielectric permittivity $\epsilon_{r_{eff}}$. To account for the frequency dependency of $\epsilon_{r_{eff}}$ Equation 4.10 is iteratively repeated, until the iteration difference is smaller than 0.1%. Therewith $f_{res_{\lambda/2}}$ is calculated with $\epsilon_{r_{eff}}$ at $f_{res_{\lambda/2}}$.

$$f_{res_{\frac{\lambda}{2}}} = \frac{c_0}{2l} \cdot \frac{1}{\sqrt{\epsilon_{r_{eff}}}} \tag{4.10}$$

Coplanar Waveguides (CPW)

Many closed form expressions for CPW transmission lines are available in the literature, but unfortunately they are less advanced than those existing for microstrip lines. Most of them have limited ranges of validity and depending on the dimensional relations some equations are more accurate than others. Comparisons with full-wave EM simulations have shown that some formulas provide better results for the characteristic line impedances while others are more accurate for loss estimations. The models presented here are based on the expressions presented in [55, 56, 57, 58, 59, 60] and support the CPW line parameters listed in Table 4.2.

Table 4.2: *Coplanar waveguide component input parameters* **c** *and response parameters* **r**.

component parameters	**c**	response parameters	**r**
line width	$c_1 = w$	characteristic impedance	$r_1 = Z_0$
line-to-ground space	$c_2 = s$	effective diel. permittivity	$r_2 = \epsilon_{r_{eff}}$
conductor thickness	$c_3 = t$	skin depth	$r_3 = \delta$
angle of side walls	$c_4 = \gamma$	total insertion losses	$r_4 = \alpha$
conductor length	$c_5 = l$	dielectric losses	$r_5 = \alpha_d$
dielectric thickness	$c_6 = h$	conductor losses	$r_6 = \alpha_c$
dielectric permittivity	$c_7 = \epsilon_r$	surface roughness losses	$r_7 = \alpha_{R_q}$
dielectric loss tangent	$c_8 = \tan\delta$	resonance frequency	$r_8 = f_{res}$
metal conductivity	$c_9 = \sigma$		
metal surface roughness	$c_{10} = R_q$		
target frequency	$c_{11} = f$		

First, we calculate the effective dielectric permittivity according to Holloway and Kuester [58]:

$$\epsilon_{r_{eff}} = 1 + \frac{\epsilon_r - 1}{2} \frac{K(k')K(k_1)}{K(k)K(k_1')} \tag{4.11}$$

with

$$k = \frac{w}{w+2s}, \quad k_1 = \frac{\sinh(\frac{\pi w}{2h})}{\sinh(\frac{\pi(w+2s)}{2h})}, \quad \text{and} \quad k' = \sqrt{1-k^2} \tag{4.12}$$

and where $K(k)$ is the elliptic integral defined as

$$K(k) = \int_0^1 \frac{dx}{\sqrt{(1-x^2)(1-k^2x^2)}}. \tag{4.13}$$

The elliptic integral exists in Matlab® as predefined function `ellipke`. With $\epsilon_{r_{eff}}$ we are now able to calculate the CPW's characteristic impedance Z_0 with

$$Z_0 = \frac{30\pi}{\sqrt{\epsilon_{r_{eff}}}} \frac{K(k')}{K(k)}, \tag{4.14}$$

as well as the dielectric losses α_d using the Equations 4.4 or 4.5 presented earlier for the microstrip model.

The conductor losses α_c are modelled with the method presented [58] which has the advantage of taking the conductor side wall angles into account. The method uses a quasi-closed form expression based on look-up tables with empirical data for the *stopping distance* Δ[1] for $\gamma = 90°$ and $\gamma = 45°$ side wall angles.

For the conductor losses α_c we then get

$$\alpha_c = \frac{R_s b^2}{16 Z_0 K^2(k)(b^2-a^2)} \cdot \left(\frac{1}{a} \ln\left(\frac{2a}{\Delta} \frac{b-a}{b+a} \right) + \frac{1}{b} \ln\left(\frac{2b}{\Delta} \frac{b-a}{b+a} \right) \right) \tag{4.15}$$

where $a = \frac{w}{2}$, $b = a + s$, $k = \frac{a}{b}$, $K(k)$ = elliptic integral of k and R_s is the surface resistance which is best approximated with Equation 4.16 as presented in [55, 56].

$$R_s = Re\left(\frac{\sqrt{\frac{\pi f \mu_0}{\sigma}}(1+j)}{2\tanh\left(\sqrt{\pi f \mu_0 \sigma}(\frac{t}{2})(1+j)\right)} \right), \tag{4.16}$$

[1] The stopping distance is a mathematical artifact for field integration and is described in [58]

The CPW conductor's surface roughness is also considered with Equation 4.8 presented earlier for the microstrip line model. With this we get the total insertion loss as sum of dielectric, conductor and surface roughness losses (Equation 4.17).

$$\alpha = \alpha_d + \alpha_c + \alpha_r \tag{4.17}$$

4.2.2. Lumped Passive Component Models

The important parameters of lumped passives are the target values of the components: the resistance R, the capacitance C and the inductance L as well as the corresponding quality factors Q, the frequency at which Q reaches the maximum and the self resonance frequency. The geometry is also relevant for calculating the area consumption, yield and cost. The literature offers a variety of more or less accurate models and closed form equations for lumped passives [61, 62, 63, 64].

At millimetre-wave frequencies however, lumped passives such as e.g. spiral inductors play a minor role. A first reasons is that typical component values for use in millimetre-wave circuits are very small and therefore difficult to realise in lumped configurations. Second, their dimension is often of the same order as the wavelength of the target frequency, hence they must be considered as distributed. Nevertheless, since resistors are widely used in RF circuits and special high resistivity materials allow their integration with very small dimensions, they are further investigated here.

Resistors

The need for resistors in millimetre-wave systems is manifold. An important use is the 50Ω load resistor for port termination. And as part of the RF circuits they are used for example in integrated Wilkinson power dividers.

In terms of overall resistor performance the sheet resistance, the resistor geometry and the resistor material parameters interact in opposed directions:

- Higher R_{sheet} values yield shorter resistors which are less inductive but often require very thin layers which are more sensitive to thickness variations.
- Smaller R_{sheet} values provide more accurate thickness control but require larger resistors with higher parasitic inductance requiring

compensation elements.

- Long resistors can be avoided with narrower geometry, this however makes them more sensitive to process variations.

The main difficulty when designing high frequency resistors (e.g. matched load at millimetre-wave frequency) is that because of the dimensions of the resistors and the required short cut-vias to ground, their reactance becomes very large and compensation networks are needed. Such compensated resistor designs are only possible with the help of full-wave EM simulation tools. The parasitic reactance however is mainly a matter of design and layout and for general technology performance comparison the basic parameters are sufficient. The investigated parameters are listed in Table 4.3.

Table 4.3: *Resistor input parameters* **c** *and response parameters* **r**.

component parameters	**c**	response parameters	**r**
sheet resistance	$c_1 = R_{sheet}$	DC resistance value	$r_1 = R_{DC}$
resistor length	$c_2 = l_{res}$	size (area)	$r_2 = A_{res}$
resistor width	$c_3 = w_{res}$		

The DC resistance value R_{DC} is a simple function of the sheet resistance R_{sheet} and the resistor length l_{res} and width w_{res}:

$$R_{DC} = R_{sheet}\frac{l_{res}}{w_{res}} \tag{4.18}$$

The total resistor area is

$$A_{res} = l_{res} \cdot w_{res}. \tag{4.19}$$

Capacitors

In RF systems operating at lower microwave frequencies (e.g. bluetooth at 2.45 GHz and cell phones at 1.8 – 1.9 GHz) capacitors are used with values ranging over six orders of magnitude from about 1 pF to 1 μF [65]. Their functions range from decoupling and energy storage with values of about 1 nF – 1 μF to filtering with values of about 1 pF – 100 pF. Considering a 1 pF thin film capacitor integrated as parallel plate capacitor with 5 μm BCB dielectric ($\epsilon_r = 2.65$), according to Equation 4.20 the plates would have a size of about $A_{plate} =$ 460 μm $\times$ 460 μm. At millimetre-waves this corresponds to about a

quarter wavelength, hence the capacitor must be treated as distributed.

$$C = \frac{A_{plate}}{h} \cdot (\epsilon_0 \epsilon_r) \tag{4.20}$$

In order to reduce the size of integrated capacitors and to use them as lumped elements at millimetre-waves, special high-permittivity materials are required. High frequency performance studies of such materials are today still the object of investigations [66]. Therefore as a comparative performance factor for technology benchmarking, integrated capacitors are not well suited.

Inductors

Inductors used in millimetre-wave frequency circuits have typical values below 1 nH. Such small values are very difficult to achieve using lumped inductors. Examples are presented in [67] where two bandpass filters have been integrated for 15 GHz and 30 GHz, respectively. The required inductance values in the 15 GHz design is realised by shunt shorted transmission lines and in the 30 GHz design by capacitive coupled transmission line section. Above 30 GHz distributed solutions using $\lambda/4$ elements are more adequate for passives integration [68]. Hence, the benchmark tool components do not include inductor models.

4.2.3. Distributed Passive Component Models

Typical distributed components are microstrip bandpass filters, patch antennas, couplers or Wilkinson power dividers, to mention a few. Depending on the component's functionality the important parameters are the input reflections, insertion losses, the frequency bandwidth or the quality factor.

For the technology benchmark purposes the basic performance parameters can be extracted without complete component models. Distributed passives are typically designed in microstrip or coplanar waveguide configuration and most performance parameters such as the insertion losses are directly related to their transmission line equivalents. Therefore the transmission line comparisons allow us to draw conclusions on the performance of distributed passives. Other performance parameters need to be addressed separately and require dedicated models. Such parameters are the coupling coefficient of coupled lines and the input impedance of distributed components. Both parameters depend more on the interaction of transmission line sections than on the

single lines itself. Two examples of distributed component models are therefore presented in the following subsections: the *Wilkinson power divider* and the *coupled microstrip lines*.

Wilkinson Power Dividers

The Wilkinson power divider is a widely used passive element providing power splitting with matched and isolated output ports. The concept of the *equal* divider is to divide power into two equal paths, also called 3 dB power divider. Figure 4.1 shows the corresponding schematic with the input and output ports, the five transmission line sections (input line, output lines and quarter-wave transformers) and the isolation or shunt resistor. For equal power division the quarter-wave transformers have an impedance $Z_{qw} = \sqrt{2} \cdot Z_0$ and the shunt resistor has a value of $R_{shunt} = 2 \cdot Z_0$ [69].

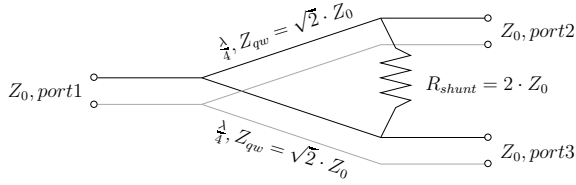


Figure 4.1: *Wilkinson power divider with input and output ports, quarter-wave transformers, and shunt resistor.*

Table 4.4 lists all supported component and response parameters. Microstrip parameters must be specified for the input line, the two output lines, the two quarter-wave transformer lines and resistor parameters for the shunt resistor. The component model for the Wilkinson power divider is based on the analysis methods presented in [69]. The input impedance Z_{in} is then

$$Z_{in} = \frac{Z_{qw}^2}{R_{shunt}} \tag{4.21}$$

with Z_{qw} being the characteristic impedance of the $\lambda/4$ segment and R_{shunt} the resistance of the shunt resistor. Both parameters are calculated with their corresponding component models presented earlier. The input reflection losses S_{11} are computed as cascaded transmission lines of impedance Z_0 and Z_{in}. The transmission S_{21} is the sum

Table 4.4: *Wilkinson power divider component input parameters* **c** *and response parameters* **r**.

component parameters	**c**	response parameters	**r**
line width Z_0	$c_1 = w_1$	input impedance	$r_1 = Z_{in}$
line width Z_{qw}	$c_2 = w_2$	Z_0 line impedance	$r_2 = Z_0$
line width resistor	$c_3 = w_{res}$	Z_{qw} line impedance	$r_3 = Z_{qw}$
in/out length	$c_4 = l_1$	shunt resistor value	$r_4 = R_{shunt}$
branch length	$c_5 = l_2$	S_{11} input match	$r_5 = S_{11}$
resistor length	$c_6 = l_{res}$	S_{21} transmission	$r_6 = S_{21}$
conductor thickness	$c_7 = t$		
dielectric thickness	$c_8 = h$		
dielectric permittivity	$c_9 = \epsilon_r$		
dielectric loss tangent	$c_{10} = \tan\delta$		
metal conductivity	$c_{11} = \sigma$		
metal surface roughness	$c_{12} = R_A$		
sheet resistance	$c_{13} = R_{sheet}$		
target frequency	$c_{14} = f$		

of the individual transmission line losses of the three segments of the Wilkinson power divider plus the -3 dB power division. The used model assumes perfect symmetry.

Coupled Lines

A short time after their well known closed form microstrip equations, Kirschning and Jansen have also published accurate equations for the characteristics of parallel coupled microstrip lines [70]. These equations are today still used in many commercial analysis tools as their error is below 1% within a broad range of topologies. The supported parameters are listed in Table 4.5.

The expressions (which are not further detailed here) allow rapid analytical calculation of the even and odd mode effective permittivities ϵ_{eff_e} and ϵ_{eff_o} and corresponding impedances Z_{even} and Z_{odd}. With

$$C = 20 \cdot \log\left(\frac{Z_{even} - Z_{odd}}{Z_{even} + Z_{odd}}\right) \tag{4.22}$$

and

$$Z_{in} = \sqrt{Z_{even} \cdot Z_{odd}} \tag{4.23}$$

we then get the coupling coefficient C in dB and the input impedance

Table 4.5: *Coupled microstrip lines input parameters* **c** *and response parameters* **r**.

component parameters	**c**	response parameters	**r**
line width	$c_1 = w$	input impedance	$r_1 = Z_{in}$
line space	$c_2 = s$	even mode impedance	$r_2 = Z_{even}$
line length	$c_3 = l$	odd mode impedance	$r_3 = Z_{odd}$
conductor thickness	$c_4 = t$	even mode effect. perm.	$r_4 = \epsilon_{eff_e}$
dielectric thickness	$c_5 = h$	odd mode effect. perm.	$r_5 = \epsilon_{eff_o}$
dielectric permittivity	$c_6 = \epsilon_r$	coupling coefficient	$r_6 = C$
dielectric loss tangent	$c_7 = \tan\delta$	S_{11} input reflection	$r_7 = S_{11}$
metal conductivity	$c_8 = \sigma$		
metal surface roughness	$c_9 = R_A$		
target frequency	$c_{10} = f$		

Z_{in}. The input reflection losses S_{11} are again computed as cascaded transmission lines of impedance Z_0 and Z_{in}.

4.2.4. Other Components

Accurate and robust analytical models for wire bonds are available and have been implemented for basic performance analysis. The basic idea presented in [71, 72, 73, 74, 75] is to partition the bond wire into separate sections modelled as transmission lines with mixed air-polymer dielectrics. The sections are then cascaded and the total input impedance Z_{in} and input reflection S_{11} are computed. For the technology benchmarking in Chapter 6 the wire bond model is not included and therefore not further elaborated at this point.

For the modelling of patch antennas, two basic approaches are found in the literature. The *transmission line model* was first presented in [76] for rectangular patches and generalised for arbitrary shapes in [77]. The second approach is the *cavity model* presented in [78, 79]. Both models provide high accuracy and flexibility but have not been implemented within this work. Instead, we will use the existing microstrip model to account for resonance frequencies of microstrip patch antennas.

4.3. Technology Models

Technology models are required because today no such complex component model exists, that could directly use the raw technology parameters without any adaptation. 3D finite element methods (FEM) with complex geometric models can approximate the real technology

quite well. But these models also fail when it comes to modelling the surface roughness, the inner behaviour of conductors with mixed metal stacks or the inhomogeneous dielectric parameters of coarse fibre reinforced resins. The technology model plays therefore the important role of matching the technology parameters **t** to the equivalent system component parameters **c** and providing empirical values for parameters which change when the materials are not used in their natural bulk form. Technology models must also be adapted to the later use as 3D FEM simulations for example use different parameters than planar Method of Moments (MoM) solver or transmission line calculators based on closed form equations.

The presented technology models consist of two parts: The first is the technology description defining 3D topology and material parameters including all parameter variations. The second is the assignment of technology parameters t_i to component input parameters c_i.

4.3.1. Example: Microstrip Line on MCM-D

The best way to illustrate the functionality and the necessity of the technology models is to use an arbitrary microstrip line and an arbitrary MCM-D technology as example.

The Tables 4.6 and 4.7 list the input and response parameters **c** and **r** of the microstrip component model. Following assumptions are made: the microstrip line has an infinite ground plane on the lowest metal layer and its line on the top metal layer. It is completely isolated from other elements and has an infinite height of air covering the line.

Table 4.6: *Example: microstrip line input parameters*

Parameter	Description	**c**
w	line width	c_1
t	line thickness	c_2
l	line length	c_3
h	dielectric thickness	c_4
ϵ_r	relative dielectric permittivity	c_5
$\tan\delta$	dielectric dissipation factor	c_6
σ	line conductivity	c_7

The technology parameters **t** of the MCM-D technology model are listed in Table 4.8. Following assumptions are made: The conductors have rectangular profiles with medium surface roughness, no barrier or passivation layers are used, and the dielectric layers provide perfect

Table 4.7: *Example: microstrip line response parameters*

Parameter	Description	**r**
Z_0	characteristic impedance	r_1
α	attenuation constant	r_2
$\epsilon_{r_{eff}}$	effective permittivity	r_3

planarisation. Technology parameter variations and their distributions are included for every t_i

Table 4.8: *Example: 3-layer MCM-D technology description*

Parameter	Description	**t**
$t1$	thickness of bottom metal 1	t_1
$t2$	thickness of metal 2	t_2
$t3$	thickness of top metal 3	t_3
$u1$	nominal undercut on bottom metal 1	t_4
$u2$	nominal undercut on metal 2	t_5
$u3$	nominal undercut on top metal 3	t_6
σ	metal conductivity	t_7
R_q	metal surface roughness	t_8
$h1$	thickness of lower dielectric 1	t_9
$h2$	thickness of upper dielectric 2	t_{10}
ϵ_r	dielectric permittivity	t_{11}
$\tan\delta$	dielectric dissipation factor	t_{12}

The technology models have now the important function of assigning the technology parameters t_i (Figure 4.2(b)) to the microstrip component parameters c_i (Figure 4.2(a)).

4.3.2. Defining the Technology Parameters

The first part of the technology model is to define all relevant technology parameters. This is done with the Matlab® function `define_technology.m` which declares all investigated technologies in a subsequent way. Every technology gets a unique identification number and new technologies can be added any time. Table 4.9 shows the parameter definition of the example MCM-D technology. The definition is divided in geometrical, electrical and cost parameters which together form the technology vector **t**. For the electrical and geometric parameters the lower variation L_{t_i}, the nominal target value T_{t_i} and the upper variation U_{t_i} are declared as vector. It is important at this point to know if the parameter variation values are specified as $\pm 1 \times \sigma$, $\pm 3 \times \sigma$

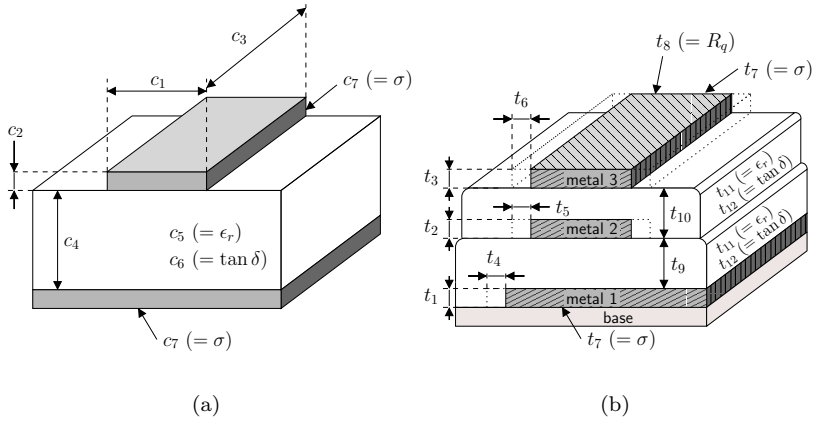


Figure 4.2: *Schematic substrate build-ups illustrating the microstrip component parameters c_i (a) and the technology parameters t_i (b).*

or even otherwise. This is especially relevant for the *component specifications* shown later in this section. The example below declares $\pm 3 \times \sigma$ parameter variations and uncertainty ranges.

4.3.3. Assigning Components to Technologies

The second part is the assignment of the technology parameters t_i to the component parameters c_i for each selected RF components. The microstrip line example with the line on the top layer (= metal layer 3) and ground on the bottom (= metal layer 1) is assigned to the MCM-D technology parameters with the Equations 4.26 to 4.29.

$$c_1 = w_{layout} + 2 \cdot t_6 \tag{4.24}$$

$$c_2 = t_3 \tag{4.25}$$

$$c_3 = l_{layout} + 2 \cdot t_6 \tag{4.26}$$

$$c_4 = t_9 + t_{10} \tag{4.27}$$

Table 4.9: *Technology parameter definition*

```
% --- Technology #1: MCM-D
tech = 1;
% --- geometric      LOWER        TARGET        UPPER
t_1(tech,:)    = [   2.5*1e-6,    3.0*1e-6,    3.5*1e-6];
t_2(tech,:)    = [   1.8*1e-6,    2.0*1e-6,    2.2*1e-6];
t_3(tech,:)    = [   1.8*1e-6,    2.0*1e-6,    2.2*1e-6];
u_1(tech,:)    = [  -1.0*1e-6,    0.0*1e-6,    1.0*1e-6];
u_2(tech,:)    = [  -1.0*1e-6,    0.0*1e-6,    1.0*1e-6];
u_3(tech,:)    = [  -2.0*1e-6,    0.0*1e-6,    2.0*1e-6];
h_1(tech,:)    = [   6.2*1e-6,    6.5*1e-6,    6.7*1e-6];
h_2(tech,:)    = [   6.2*1e-6,    6.5*1e-6,    6.7*1e-6];
rough(tech,:)  = [   100*1e-9,    150*1e-9,    200*1e-9];
% --- electrical/dielectric
sigma(tech,:)  = [     5.80e7,      5.88e7,      5.96e7];
er(tech,:)     = [       2.63,        2.65,        2.68];
tand(tech,:)   = [     0.0008,      0.0010,      0.0012];
% --- design rules
dr_l(tech,:)   = 20*1e-6;
dr_s(tech,:)   = 20*1e-6;
% --- cost
cost(tech,:)   = [       1.00,        1.05,        1.10];
```

$$c_5 = t_{11} \tag{4.28}$$

$$c_6 = t_{12} \tag{4.29}$$

The microstrip model used for this example does not provide an input parameter for the surface roughness (see Table 4.6), the technology however has a non-negligible roughness. At this point the benefits of the technology model become clear. In Equation 4.30 we use the microstrip conductivity parameter to include the surface roughness as a modified equivalent metal conductivity. The exact procedure for calculating the correction coefficient C_{corr} as function of the surface roughness R_q $(= t_8)$ and the target frequency f is described in [28].

$$c_7 = t_7 \cdot C_{corr}\,(t_8, f) \tag{4.30}$$

The corresponding benchmark tool function implemented in Matlab® is `assign_microstrip_technology.m` where the variable `tech` is the technology identification number. The assignment function for our mi-

crostrip on MCM-D example is shown in Table 4.10. The function contains the vector **c** of all microstrip component parameters supported by the corresponding model.

Table 4.10: *Component technology assignment*

```
% --- Component #1: microstrip line
ms_tech(ms)  = tech;
% --- geometric
ms_l(ms,:)     = 10000*1e-6  + (2*u_3(tech,:));
ms_w(ms,:)     = 46*1e-6     + (2*u_3(tech,:));
ms_t(ms,:)     = t_3(tech,:);
ms_h(ms,:)     = h_1(tech,:) + h_2(tech,:);
% --- electrical
ms_sigma(ms,:) = s_3(tech,:) * c_corr_rough;
ms_e(ms,:)     = er_1(tech,:);
ms_tand(ms,:)  = tand_1(tech,:);
ms_f(ms,:)     = 59*1e9;
```

4.4. Benchmark Description

A benchmark project is described in the *Benchmark Project Description* block where the user specifies the technologies, assigns generic RF components, sets the component specifications and calls the benchmark functions computing the technology yield and performance ratios and generating the graphical outputs. All necessary files are stored in an individual project folder located in the `projects/` directory.

4.4.1. Specification of Generic Components

In order to compare the technologies, generic RF components are chosen and specification limits defined. The components and the specifications can be arbitrary but it is more realistic to choose them in accordance with a *reference application*. This will not only compare the individual technologies to each other but will also provide information on how the reference application performs using different technologies.

The microstrip line example presented in the previous section is now considered as the relevant component of a reference application working at 59 GHz. For this system the component's response parameter specifications are the maximum characteristic impedance variations, the maximum loss per unit length and a resonance frequency bandwidth

for the case where the line is used as microstrip resonator. Here again it is important to be sure how the upper and lower values are specified. In the current example we have $\pm 3 \times \sigma$ specification limits (USL, LSL) for process yield estimations.

The reference application and the component specifications are declared in the Matlab® file `define_specifications.m` as depicted in Table 4.11.

Table 4.11: *Component specifications*

```
% --- Specification #1
spec = 1;
% --- specifications     LSL    TARGET       USL
% --- (+/- 3s)
% --- microstrip/cpw
z_spec(spec,:)    = [   48.0,     50.0,     52.0]; % two-sided
loss_spec(spec,:) = [                        1.0]; % one-sided
fres_spec(spec,:) = [ 76.2e9,   76.5e9,   76.8e9]; % two-sided
```

4.4.2. Selection of Benchmark Functions

Depending on the reference application and the chosen RF components the technology performance measures that can be computed and compared are different. Also the overall goal of the benchmark project can have different scopes. For this many technology benchmark functions have been developed based on the technology performance measures introduced in Chapter 3. From these functions a selection is made for each benchmark project.

4.5. Result Evaluation and Comparison

All results of the computed technology performance measures and the comparisons of the investigated technologies are visualised in the *Benchmark Result Assessment* block. The available benchmark assessment functions offer two types of information: the individual component monitoring outputs and the technology comparison charts which line up and compare the performance measures for all investigated technologies. An important aspect is the visualisation of parameter relations

which would be more difficult to identify by just comparing individual numbers.

4.5.1. Evaluation of Basic Decision Criteria

Before comparing the individual RF performances each technology undergoes a go/no-go test to evaluate the basic criteria. The most important questions to answer are:

1. Are integrated resistors required and is the technology providing them?
2. Are multilayer integrated passives planned and does the technology have sufficient layers?
3. Do design rule constraints exist and does the technology fulfil them?

The last criteria which play a decisive role are the choice of transmission line configuration and the range of impedance values that can be achieved.

4.5.2. Choice of Transmission Line Configuration

The transmission line configuration used must be fixed very early in a design project as it influences the choice of usable MMICs. The relevant impedances in a millimetre-wave system are

- 50 Ω for general interconnect transmission lines,
- 50, 71 (and 100) Ω for power dividers,
- 50, 100 and 200 Ω for feed networks of antenna arrays and
- 25 - 150 Ω (or even more) for coupled line based components.

These are only a few examples but they clearly show that depending on the benchmark reference application, some impedance values are more important than others. The range of impedances realisable with a technology is determined by the minimum design rules and the wavelength of the target application frequency. These limits are determined by the smallest possible design rules and by 1/10 of the wavelength. Figure 4.3 shows examples of five different technologies, for microstrip lines and CPW lines, respectively. These graphs are automatically generated for every benchmarked technology and left blank for those technologies for which certain configurations are not realisable.

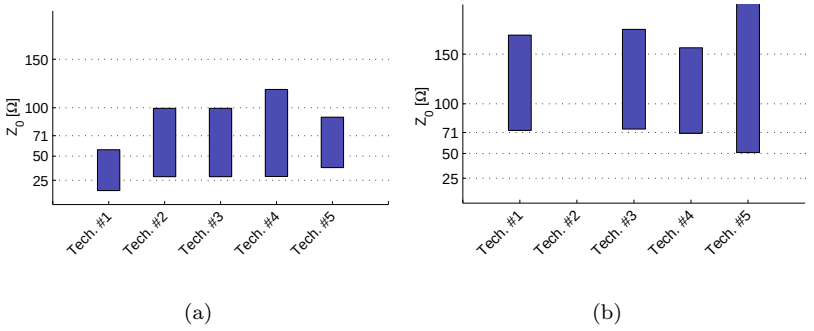


Figure 4.3: *Realisable impedance ranges for microstrip line (a) and CPW (b) examples.*

4.5.3. Transmission Line Parameter Outputs

Two types of transmission line parameter visualisation functions are included. The first are the monitoring outputs providing detailed charts to control and analyse each transmission line individually. The second are the parameter analysis charts which include the OPAT and STPAT sensitivity and interaction charts and line up all performance measures.

Parameter Monitoring

The individual component monitoring outputs provide details about the characteristics and the performance of each component parameter for each technology. These detailed informations are mainly used to set up and fine tune a benchmark project.

In the case of microstrip lines the first monitoring window shows the component's characteristic parameters which are the impedance and the resonance frequency. Characteristic parameters are those which must meet a certain value within a certain tolerance. Key information are component parameter variations related to technology parameter variations, fragmented into all its contributors (see upper Figure 4.4).

The second monitoring window shows the component performances parameters which have no specified target but must be as large or small as possible beyond a certain limit. Typical parameters are the insertion losses, separated into dielectric, conductor and roughness losses. Not

only the variation contributors are important but also the absolute performance loss contributors. Both parameters are individually displayed (see lower Figure 4.4).

Parameter Analysis

Very similar to the monitoring outputs are the sensitivity analysis outputs showing the results of the OPAT and STPAT analysis described in Chapter 3 (see Figure 4.5). The STPAT analysis function also computes and lists the interaction ratios I_{ij} for a custom selection of parameters.

4.5.4. Passive Component Outputs

Transmission lines represent the basic performance of a technology. Passive components on their part are more related to the specific reference applications. Two passive component models have been presented earlier and now included in the benchmark tool, the Wilkinson power divider and the coupled microstrip lines. The following paragraphs discuss their parameter performance analysis functions.

Basic Component Performance

The component's basic performance are closely related to their underlying transmission lines. Both, the Wilkinson power divider and the coupled lines, are implemented in microstrip configuration. The microstrip line performance results are therefore giving an impression of what can be expected from the passive components. The component's specific performance is based on the component models presented earlier in this chapter.

Coupled Microstrip Lines

For the coupled microstrip lines the OPAT sensitivity chart and the maximum achievable coupling coefficient can be displayed (Figure 4.6). The latter is first computed for any input impedance where the only limits are the minimum design rules, then it is also computed with the constraint of matched input impedance $Z_{in} = 50\ \Omega$.

Wilkinson Power Divider

A comparison line up of all response parameter variations (errorbars) for every technology allowing integration of a Wilkinson power divider

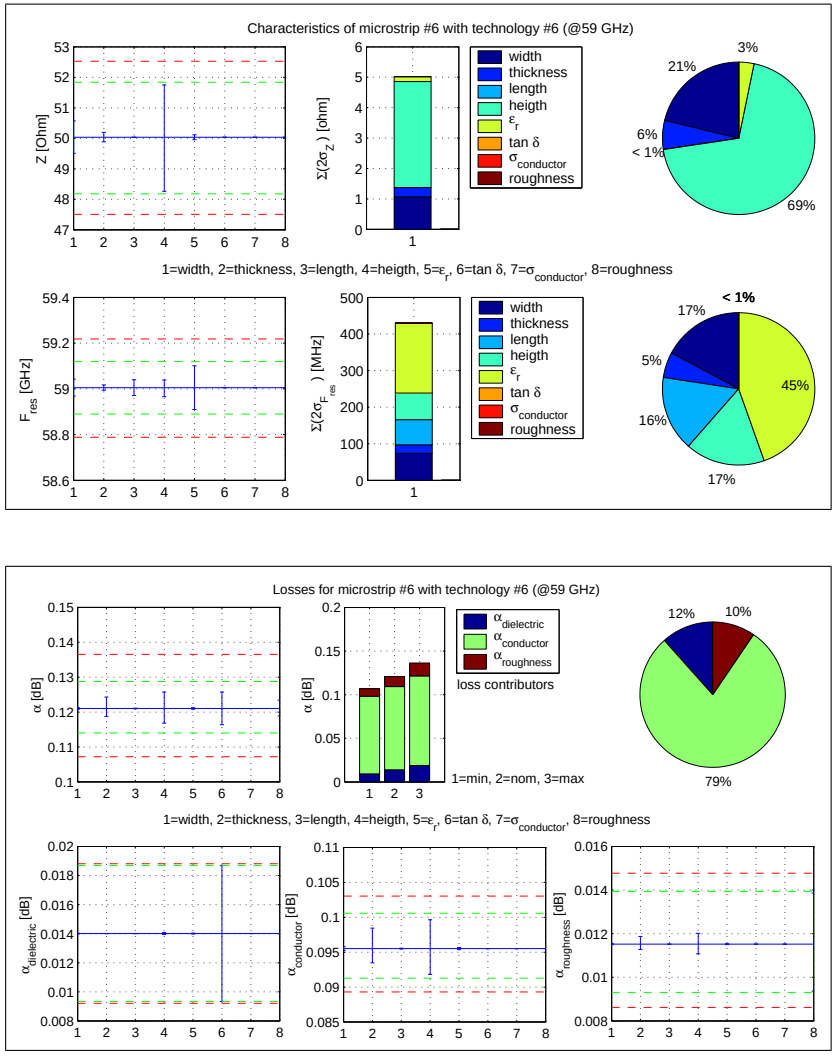
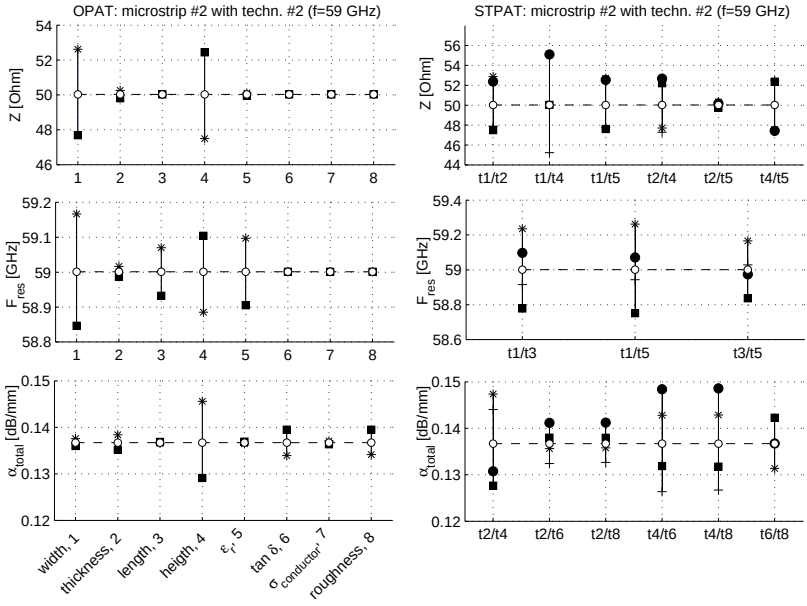


Figure 4.4: *Monitoring window for microstrip line characteristic parameters: impedance Z_0 and resonance frequency f_{res} (upper figure) and performance parameters: insertion losses α (lower figure).*



(a) (b)

Figure 4.5: *OPAT sensitivity graphs (a) and STPAT interaction graphs (b) for arbitrary characteristic impedance, resonance frequency and total insertion losses parameters. (OPAT:* $\circ = T_{t_i}$, $* = L_{t_i}$, $\blacksquare = U_{t_i}$, *STPAT:* $\circ = TT_{t_i}$, $\blacksquare = LL_{t_i}$, $\bullet = LU_{t_i}$, $+ = UL_{t_i}$, $* = UU_{t_i}$*)*

(integration of 100 Ω resistor possible) is shown in Figure 4.7. The OPAT sensitivity analysis in Figure 4.8 shows that the power divider's response parameters S_{11} and S_{21} are nonlinear functions of the input parameters. To get a picture of the total variation distributions, a Monte Carlo simulation function is implemented. Figure 4.9 shows the Monte Carlo results after 10'000 runs with variations of all input parameters.

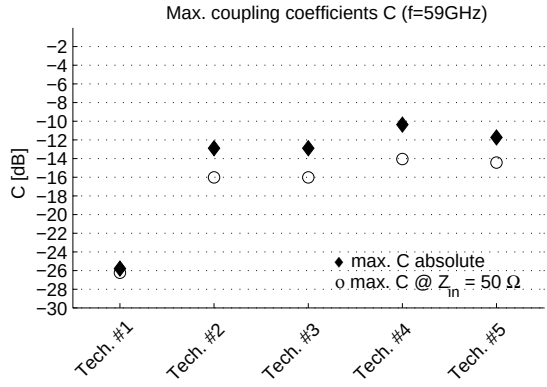


Figure 4.6: *Comparison of the maximum coupling coefficient of parallel coupled microstrip lines for five investigated technologies.*

4.5.5. Technology Comparison Line Ups

The final technology comparison outputs line up the technologies' total performance ratios and total yields according to the reference application specifications defined at the beginning. The final costs (incl. yield losses) versus the total performance ratios are plotted for all investigated technologies thus forming the cost performance-pareto graph.

4.6. Benchmark Assessment

When the benchmark results are compared to each other and conclusions drawn, it is crucial to remember the benchmark description's accuracy and the initial goal. The result *validation* and *exploitation* are the concluding actions of any technology benchmark.

4.6.1. Benchmark Validation

The presented benchmark system is based on a set of generic RF elements representing real applications. Several rules must be followed in order to provide best possible agreement:

- The computed parameters of each individual RF element must be as accurate as possible and in compliance with the validity range of the used models.

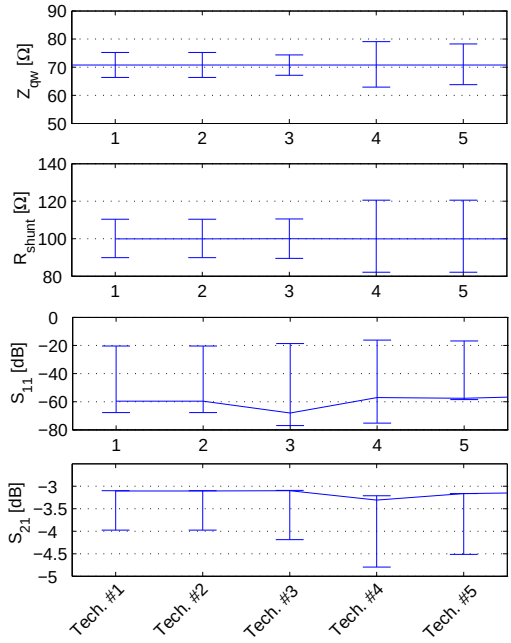


Figure 4.7: *Comparison of the Wilkinson divider's Z_{qw} branch impedances, R_{shunt} shunt resistors, S_{11} input reflection and S_{21} transmission losses of all investigated technologies. The errorbars show the $\pm 3 \times \sigma$ variations.*

- Technology parameter variations are specified with three values, a target value, a minimum value and a maximum value. Any yield estimation assumes a linear behaviour between these three points. For large process variations the user must keep in mind that this linearity might be inaccurate.
- In order to best represent the target application the used generic RF components must be selected carefully. The type and number of each component as well as its specifications are very important parameters.
- Intuitively, process engineers and RF designer with some practical experience should always question the plausibility of the results.

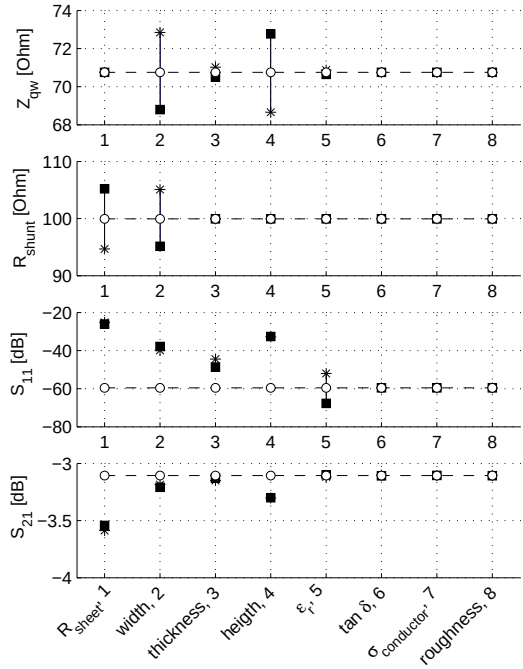


Figure 4.8: *Arbitrary OPAT sensitivity graphs of the Z_{qw} branch impedance, R_{shunt} shunt resistor, S_{11} input reflection and S_{21} transmission losses for a Wilkinson power divider. ($\circ = T_{t_i}$, $* = L_{t_i}$, $\blacksquare = U_{t_i}$)*

4.6.2. Exploiting the Benchmark Results

The goal of a technology benchmark is to allow early performance estimations and therefore to be able to make decisions on material selection and investments for process enhancement. This demands for a careful assessment of benchmark results. The benchmark tool offers the following assessment methods:

- The sensitivity charts show which technology parameters contribute most to yield losses. Depending on the underlying technology and the manufacturer's capabilities one parameter might be much easier to improve than another. This could be determining for choosing a technology.

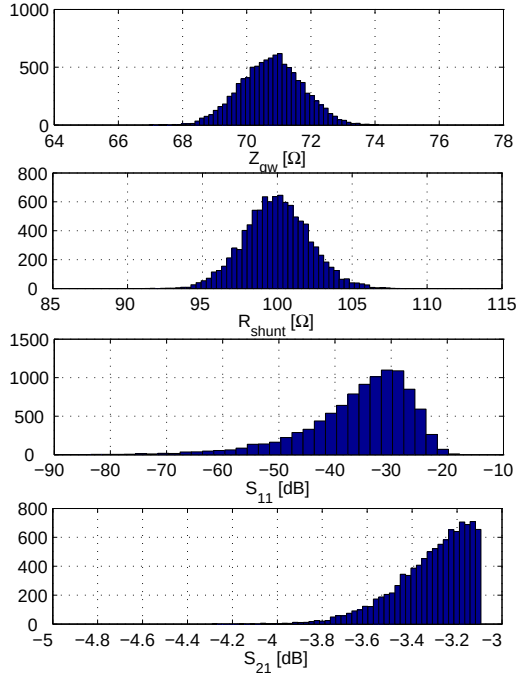


Figure 4.9: *Monte Carlo analysis of the Z_{qw} branch impedance, R_{shunt} shunt resistor, S_{11} input reflection and S_{21} transmission losses for a Wilkinson power divider.*

- Although all technologies may have 100% yield the performance ratios tell how close to 100% the technologies are. For minimising risks, the performance ratio is therefore more significant than the total yield.
- In many cases the performance must at minimum fulfil the specifications and everything above is not required. Here the total costs play the more important role.
- The benchmark can also show whether for one technology the yield is better using microstrip configuration while for another technology coplanar waveguides perform better. This might influence fundamental decisions when choosing the MMIC chip set.

4.7. Summary

An efficient technology benchmark tool was presented in this chapter. Besides its functionality and flexibility in terms of analysis and comparison functions provided, its underlying models are kept as simple as necessary thus capable of performing complete Monte Carlo simulations. They are necessary to compute the performance ratios and technology yields of components with highly non-linear parameter variation distributions.

5

Technology Characterisation

The previous chapters have shown that technology performance estimation demands precise characterisation of the investigated technologies. Especially for use at millimetre-wave frequencies some technology properties must be known very accurately. Unfortunately data sheets and manufacturers are often not capable of providing all required information, thus rendering own measurements indispensable. In this context two types of technology parameters are distinguished, the high frequency material characteristics and the 3-dimensional (3D) topology parameters. Measurement and extraction of material characteristics such as the dielectric constant and the dissipation factor at millimetre-wave frequencies are reported in great detail in Grzyb et al. [80, 81, 82]. This chapter therefore focuses on the characterisation of the 3D topology introducing new test structures and methods to effectively describe and specify technology parameters. These methods account for manufacturing tolerances, statistical variations and estimations, spatial distribution of parameter variations and inter-panel variability.

The first section identifies the technology parameters which are relevant for determining the technology performance. In Section 2 a method describing technology parameters in the spatial frequency domain is introduced. It is not only important to know how large process variations are but also to know where they occur. Benefits are demonstrated by means of theoretical background and practical examples. In Section 3 a technology characterisation test vehicle (TCTV) is presented, providing dedicated test structures for measuring the 3D topology parameters. These test structures are laid out such as to preserve the spatial information of the measured parameters. Once a technology is fully characterised it is important to keep all parameters on target during production. To do so, Section 4 introduces a process control method based on process related panel zones.

5.1. Technology Build-Up Parameters

The technologies covered in this section include thin film and laminate build-ups with photo lithographically defined or laser drilled microvias, both having similar topologies and therefore being described with the same set of technology parameters. These include three dimensional topology build-up parameters, physical material properties and technology design rules.

5.1.1. 3D Build-Up Topology Parameters

Figure 5.1 depicts a cross-sectional view of a generic 4 metal-layer build-up showing all relevant parameters. The layer thicknesses, alignment and torsion as well as the surface roughness are well known standard parameters. The *undercut* u is described as half the difference between the layout metal dimensions (w_{layout}) and the resulting real dimensions (w_{real}). The value therefore represents the difference for one edge and is positive if w_{layout} is larger than w_{real}. The conductor *profiles* can exhibit many different shapes depending on the used process. Simplified, rectangular and trapezoid profiles with positive or negative slopes g are distinguished (the profile in Figure 5.1 shows a positive slope). The *degree of planarisation* (DOP) describes the ability of the dielectric layers to planarise an uneven underground. It strongly depends on the used dielectric materials, the layer thicknesses and the size of the uneven parts underneath [83].

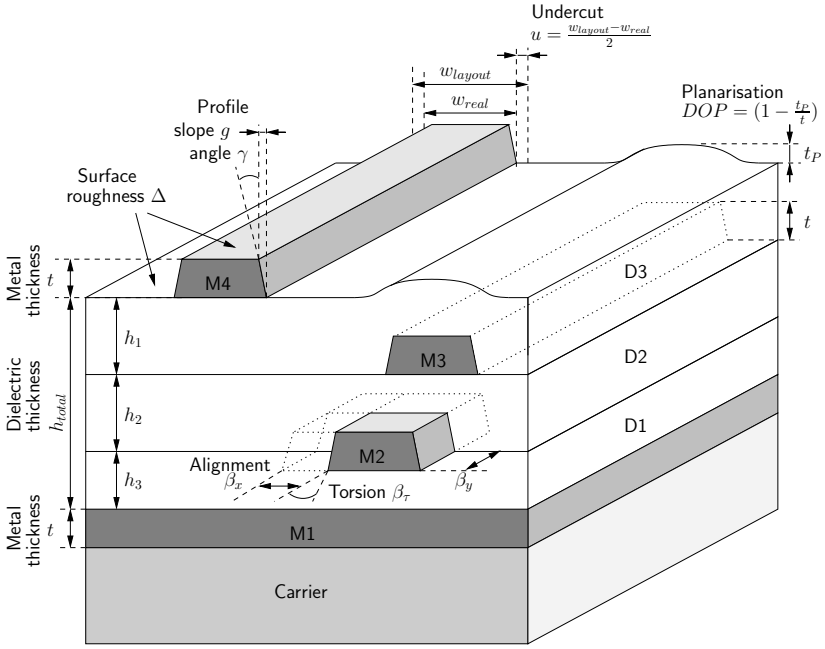


Figure 5.1: *Three dimensional build-up topology parameters for complete geometrical description of the investigated thin film and laminate substrate technologies.*

5.1.2. Material Properties

Table 5.1 lists the physical material properties that determine the design of integrated passives at millimetre-wave frequencies. The list separates conductive and non-conductive materials. For every parameter there exists a specific value which is valid for the raw material in bulk form under specific environmental conditions. Such values are available in reference books and datasheets. After processing, however, the material properties are most likely subject to change. It is therefore imperative to know the material properties at the final stage of processing and also at the stage of operating.

Table 5.1: *Electrically relevant material properties*

Types	Functions	Parameters and symbols
conductive materials	conductor layers barrier layers adhesion layers metallic carriers	resistivity ρ [Ωm], relative magnetic permeability μ_r
isolating materials	isolation layers passivation layers adhesion layers non-metallic carriers	relative dielectric permittivity ϵ_r, dielectric dissipation factor $\tan\delta$

5.1.3. Technology Design Rules

The minimum feasible design rules are one of the most limiting factors for a technology's total performance. The design rules set the limits for the achievable component parameter ranges such as characteristic impedances or the coupling of parallel lines. Figure 5.2 and Table 5.2 show the most important design rules used in this work.

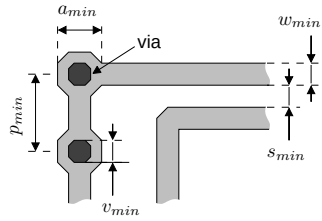


Figure 5.2: *Technology design rule parameters.*

Table 5.2: *Technology design rules.*

Design rule parameters	Symbols
smallest line width	w_{min}
narrowest line space	s_{min}
smallest via diameter	v_{min}
minimum via landing area	a_{min}
minimum via pitch	p_{min}

5.2. Spatial Frequency Description of Parameter Variations

In a typical high budget, low volume millimetre-wave application (e.g. space and military), the fabrication costs are dominated by product development efforts, prototyping and initial tooling costs. The costs of manufacturing yield losses and system tuning play a minor role. For low cost, high volume consumer applications these relations change: the development effort must be compensated by low cost manufacturing thus requiring high yield and a minimum of system tuning [84]. Many attempts to reduce the manufacturing costs of high density substrates have been presented in the literature. However, one conclusion common to these trials investigating cheaper materials and processing methods is the increasing difficulty to control process accuracy. Especially when using laminate based large area processing, the process variations become very important [85, 86].

The main idea of introducing spatial frequency for parameter variations is therefore to keep as much information as possible about their spatial occurrence and to assess the correlation of local parameter variations to total technology performance. With this information it is possible to take technology variations into account during the design phase and to optimise process control actions during manufacturing. The resulting benefit is that millimetre-wave designs can be realised with tighter tolerances [87, 88].

5.2.1. Background

A common way to describe process variations is to specify a nominal value with an upper and a lower tolerance limit, typically related to the standard deviation of the process. However, this does rather reflect the worst case eventuality than the real process capabilities. Further it contains no information about *where* (location) and *how often* (frequency) variations occur. But this is an important factor that can make the decisive difference between two technology alternatives.

Important differences between copper deposition using subtractive etching and additive electroplating were reported in [89]. The terms *large ripples* and *small ripples* were used to describe the different spatial distributions of the line width variations. Similar observations were first presented in [90] and later in [91], where the terms *roughness*, *waviness* and *flatness* were introduced to characterise different types of

non-uniformities in thin film substrates. In the semiconductor industry, process variations are commonly described as *wafer-to-wafer*, *across-wafer*, *macro* and *micro non-uniformities* [92].

5.2.2. Defining the Spatial Frequency

The approach presented here is to combine all the terms listed previously into one single expression – the spatial frequency description (SFD). We define the spatial wavelength λ_v and the spatial frequency f_v to describe the spatial occurrence of process variation according to Equation 5.1 and Figure 5.3 [1].

$$f_v = \frac{1}{\lambda_v} \tag{5.1}$$

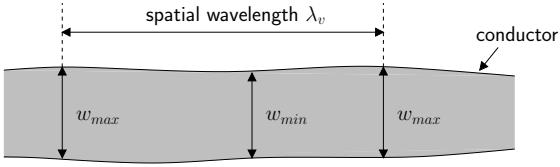


Figure 5.3: *Definition of spatial wavelength λ_v and frequency f_v for parameter variations, illustrated for a conductor line width variation.*

The SFD model separates three spatial frequency bands as shown in Table 5.3. The band definition is closely related to the target frequency wavelength of the application.

Table 5.3: *Definition of the three spatial frequency bands.*

Frequency band	Description	Spatial range
high	*Roughness* and *Micro non-uniformities*	$\lambda_v < \lambda_{features}$ $\lambda_v < \lambda_{system}$
mid	*Macro non-uniformities* and *Across-wafer non-uniformities*	$\lambda_v > \lambda_{system}$ $\lambda_v \approx wafersize$
low	*Wafer-to-wafer* and *Batch-to-batch non-uniformities*	$\lambda_v >$ wafer size $\lambda_v >$ batch size

[1] The definitions introduced here are applied to electronic packaging substrates. However, this general method can be adopted to any other technology, where parameter variations occur at different spatial frequencies.

Table 5.3 uses several terms describing spatial quantities such as e.g. *wafer* and *batch*. At this point it is therefore appropriate to define the terms used within this work in order to avoid misunderstandings. Figure 5.4 illustrates these relations.

Feature A feature is an element of the technology build-ups such as, for example, the conductor widths the via diameters or the dielectric layer thicknesses.

Component For distributed integrated components, the spatial quantity is the length of the resonating sections up to the total component dimensions. For lumped components such as a spiral inductor the quantity relates to its spiral diameter.

System This is the system's target frequency wavelength.

Module The diced substrate used for one system.

Wafer/Panel The largest single manufacturing unit. Both terms are used as some technologies have been manufactured on square panels and others on circular wafers.

Batch A batch comprises all wafers that are manufactured within the same environment. This can be a single wafer or several cassettes full of wafers. Another term which is often used in the same context is *lot*.

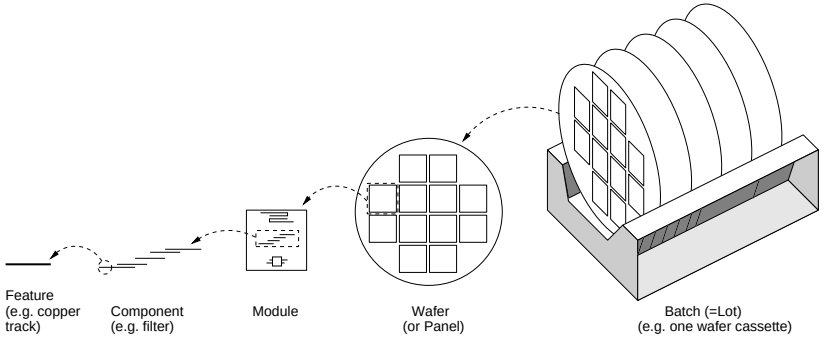
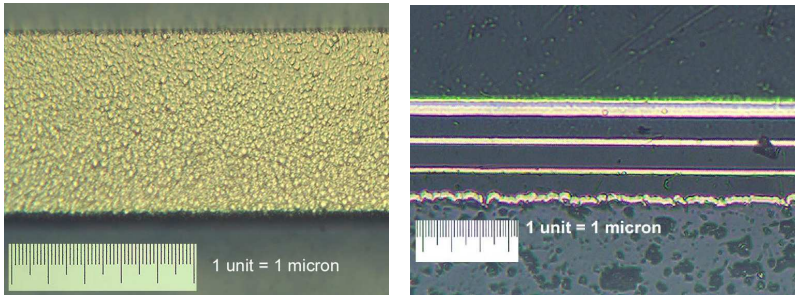


Figure 5.4: *Relation of the spatial quantities* batch, wafer, module, component *and* feature.

5.2.3. Examples for Spatial Frequency Bands

The simplest way to illustrate the spatial frequency bands is to show examples where typical process variations occur at different frequencies.

Roughness The roughness R_q describing surface texture is specified as the root-mean-square (RMS) value of repetitive or random deviations from the normal surface [93, 94, 95]. A material's surface roughness is either predetermined by its chemical consistence or a result of its deposition or treatment process. Figure 5.5(a) shows the surface roughness of an electroplated gold layer with $\lambda_v \approx 2 - 4\mu$m. Figure 5.5(b) shows the cross section of a 4-layer thin film build-up on alumina substrate. The roughness of the alumina surface directly affects the roughness of the first deposited (sputtered) copper layer with $\lambda_v \approx 3 - 6\mu$m.



(a) (b)

Figure 5.5: *Photographs of surface roughness on a gold track (a) and on the bottom copper layer sputtered on a rough alumina carrier (b).*

Micro non-uniformity Micro non-uniformities are caused by material inhomogeneities, material residues through insufficient cleaning, roughness of laminate reinforcement fibres or other types of irregularities. The term micro non-uniformity is used when λ_v is of the same order as layout feature dimensions. In Figure 5.6 the reinforcement fibres of a laminate carrier have diameters and spaces of about 10μm. Both may cause non-uniformities with $\lambda_v \approx 20 - 30\mu$m which are of the same order as the conductor line widths.

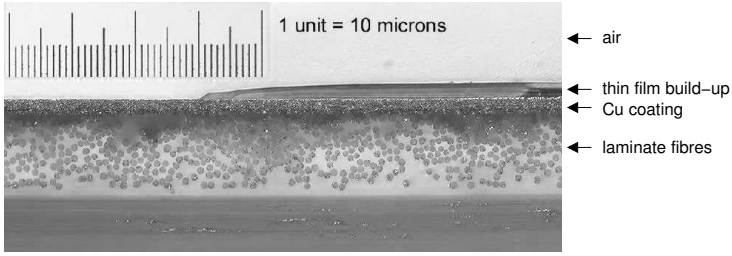
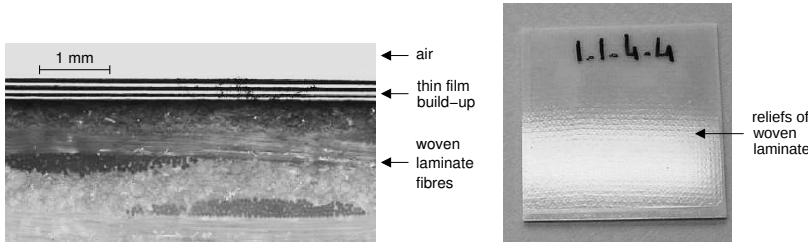


Figure 5.6: *Cross section photograph of single laminate fibres causing micro non-uniformities in the bottom metal layer.*

Systematic macro non-uniformities also exist and often they are partly avoidable. Examples are out-of-focus photo-lithography as effect of non-planarities caused by underlying metal layers or warpage and unequal deposition rates of an electroplating process caused by unequal current densities in different metal structure densities.

Macro non-uniformities The woven structures of laminate carriers such as illustrated in Figure 5.7(a) can produce a bumpy topography visible throughout the entire build-up. The flat illumination of the modules in Figure 5.7(b) renders this waviness visible. Another reason for uneven dielectric thickness is inhomogeneous spin coating caused by large metal obstacles such as test pads, bond pads, plate capacitors or large vias.

Across-wafer non-uniformities Across-wafer or across-panel non-uniformities can be a result of out-of-focus photo-lithography on bowed substrates or inaccurate step-and-repeat lithography on large panels . The panel handling (vertical vs. horizontal) as well as the panel agitation in wet benches are also very critical process steps. Often these variations can be distinguished into typical zones related to specific process steps. Such zones are for example panel edges vs. panel corners or wafer centre vs. wafer borders [96]. Figure 5.8 shows a 12"×12" (30 cm×30 cm) large area panel with the corresponding measured top layer sheet resistance. The example shows a typical across-panel non-uniformity with $\lambda/2 \approx 30$ cm.



(a) (b)

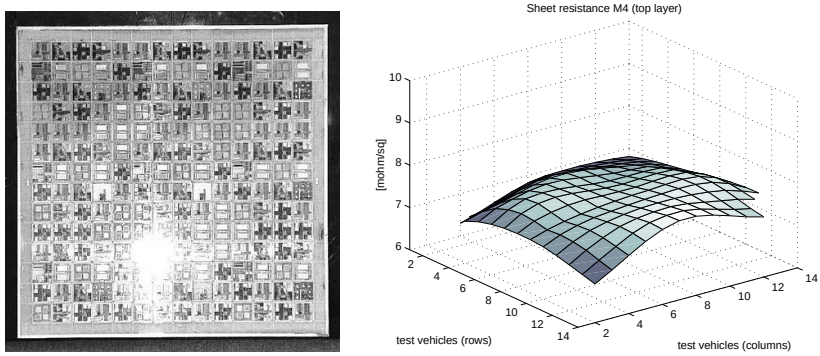
Figure 5.7: *Cross section photograph of a macro non-uniformity caused by the woven laminate fibres (a) and the same effect visualised with flat light reflection showing the reliefs on a 20 mm × 20 mm module (b).*

Wafer-to-wafer non-uniformities Wafer-to-wafer or panel-to-panel non-uniformities can result from different wafer handling or varying process parameters depending on the location of the wafer inside the cassette or from drifting process conditions. Typical examples are degrading etchant concentrations with increasing wafer numbers or age and temperature of liquid polymers such as benzocyclobutene (BCB) [97].

Batch-to-batch non-uniformities Between two batches of the same product the process environment can change. This could be due to installation of new equipment, calibration of some equipment parts or a new batch of raw material. Depending on the exactitude of restoring the process, some parameters might therefore be different from batch to batch.

5.2.4. Measuring Spatial Parameter Variations

Measuring technology parameters in a way that preserves the spatial information of variations requires some important considerations. First of all is the fact that when we measure parameter values with a broad variation frequency spectrum the sampling theorem of Nyquist applies. That means no matter which measurement or extraction technique we use, we have to consider the effects of higher variation frequencies.



(a) (b)

Figure 5.8: *Example for across-panel non-uniformity: a) 12"×12" panel and b) measured sheet resistance across the panel.*

Depending on the measurement method different types of 'low pass-filtering' and 'band pass-filtering' exist to separate the frequency bands of interest. Continuous and discrete data acquisition are differentiated.

Continuous Data

Methods to measure continuous parameter values are mechanical or optical profilometres, contour detection using digital image processing or time domain reflectometry (TDR) to extract the dielectric thickness, the line width and the dielectric permittivity [98]. These methods often have the advantage of providing natural low pass filtering effects and the standard deviations can be extracted using signal processing methods such as numerical bandpass filtering. To exemplify this method we use an arbitrary conductor line of length $l = 10$mm and width $w = 20\mu$m including random line width variations (see upper graph in Figure 5.9). The line width variations are then separated into four spatial frequency bands (see lower graph in Figure 5.9) using the Butterworth filters shown in Figure 5.10. (Note that for better visualisation the bands chosen for this example differ from the band definition in Table 5.3.) The standard deviation is extracted for the four separated bands individually. The experiment shows that the cumulation of the

four extracted standard deviations corresponds to the total standard deviation of the original data with an error smaller than 1%.

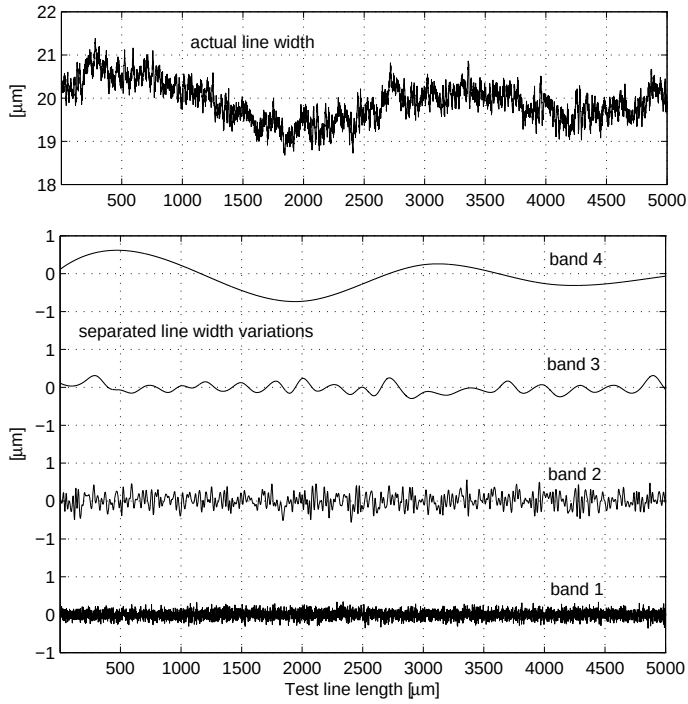


Figure 5.9: *Line width variations separated into four spatial frequency bands using Butterworth filters.*

Discrete Data

When continuous measurements are not possible the spatial information is gathered by performing discrete measurements along chains of adjacent test structures. Small parallel plate capacitors arranged as a chain are for example used to extract the dielectric thickness along these chains. With this method the sampling theorem plays again an important role. It says that the sampling frequency (in our case the pitch of the adjacent test structures) must be twice the highest occurring frequency (or half the shortest wavelength λ_{crit}). The smallest

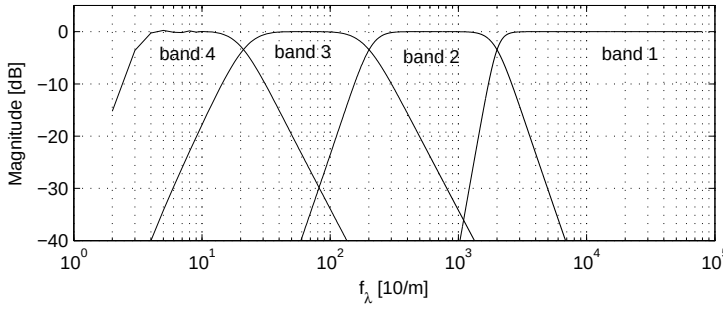


Figure 5.10: *Matlab® implementation of Butterworth filters for separation of four spatial frequency bands.*

occurring wavelength is the surface roughness which is very short compared to the size of the smallest useful test structure thus requiring low pass-filtering.

The advantage of some test structures is that they automatically measure parameters averaged over the length l_{ts} of the structure itself. A parallel plate capacitor for example gives the dielectric thickness h averaged along the side length l_{ts} of its plates (Figure 5.11). In a chain this behaves like a *stepped* median filter providing the spatial frequency attenuation described by Equation 5.2 and shown in Figure 5.12.

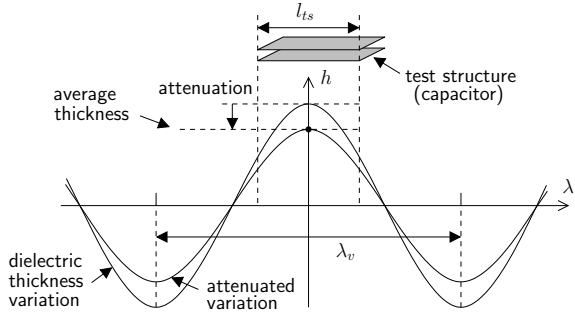


Figure 5.11: *Averaging scheme of dielectric thickness measurement using parallel plate capacitor with length l_{ts}.*

$$attenuation = \int_{-\frac{l_{ts}}{2}}^{\frac{l_{ts}}{2}} \cos(\lambda) d\lambda \frac{1}{l_{ts}} \tag{5.2}$$

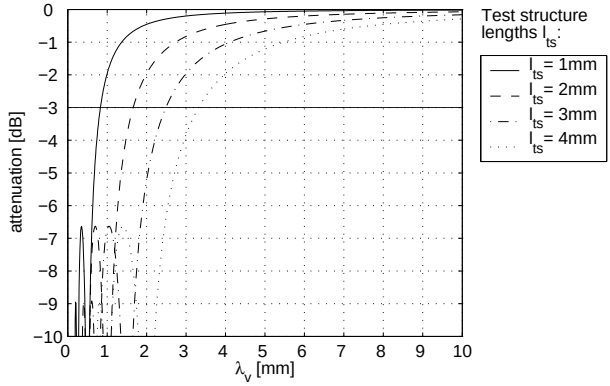


Figure 5.12: *Spatial frequency attenuation with stepped median filtering for four different test structure lengths* l_{ts}.

With the -3dB point defined as the smallest critical wavelength λ_{crit}, Figure 5.12 shows that the sampling theorem cannot completely be fulfilled. According to Equation 5.2 the adjacent structures need to be $1.1701 \times \frac{\lambda_v}{2}$ wide with a pitch $1 \times \frac{\lambda_v}{2}$, thus overlapping by $0.1701 \times l_{ts}$. The only solution is therefore to choose the distance between adjacent test structures to be as small as possible.

5.2.5. Benefits

The benefits of describing parameter variations in spatial frequency bands are manifold and applicable at different stages of design and manufacturing. Few examples are given here, but more specific advantages are given later in this chapter, when presenting the dedicated test structures.

- Microwave designers can perform sensitivity analysis of circuit layouts and compute yield estimations with relation to the different process variation frequencies. This is very important when large structures (e.g. antenna arrays) are integrated and the homogeneity within the entire structure must be guaranteed.

- Process control engineers observing unexpected parameter variations in a certain frequency band can use that specific spatial information to isolate possible failure causes.
- Considering the process variations in the frequency bands with wavelengths close to the feature size of integrated passives (e.g. line width and space of spiral inductors), RF system designers can estimate system yields in an early design stage [63].
- The gathered spatial information allows distinguishing and separating those variations that affect RF performance and those which do not affect RF performance. With this knowledge the design tolerances become tighter and the RF designs can be optimised for tighter tolerances.

5.3. Characterisation Methods

This section describes the implementation of test vehicles[2] (TV) dedicated to substrate technology characterisation (TCTV). Special attention is given to the spatial description of parameter variations presented in the previous section. The TCTVs described here were developed and manufactured within the EU research projects LAP [99] and LIPS [100] and adapted to the various build-ups and design rules of the investigated technologies. In this section we will focus on a TCTV implementation designed for four-layer thin-film substrates (Figure 5.13). Modifications for other technologies are mentioned if required.

Note: Within the frame of the above mentioned research projects mainly two types of test vehicles were used: the RF Test Vehicles *(RFTV) and the* Technology Characterisation Test Vehicles *(TCTV), both having clearly defined scopes within the characterisation task. The RFTVs' main objectives are the high frequency properties of the materials and build-ups according to Table 5.1. The TCTVs are responsible for all other parameters according to Figure 5.1 and Table 5.2. The test structures and measurement methods used to extract the dielectric permittivities and dissipation factors up to millimetre-wave frequencies using the RFTVs are described in great detail in [80, 81, 82]. This section is therefore focusing on the TCTVs and its test structures.*

[2] In the literature the terms *test coupons* and *test cells* are also found in this context.

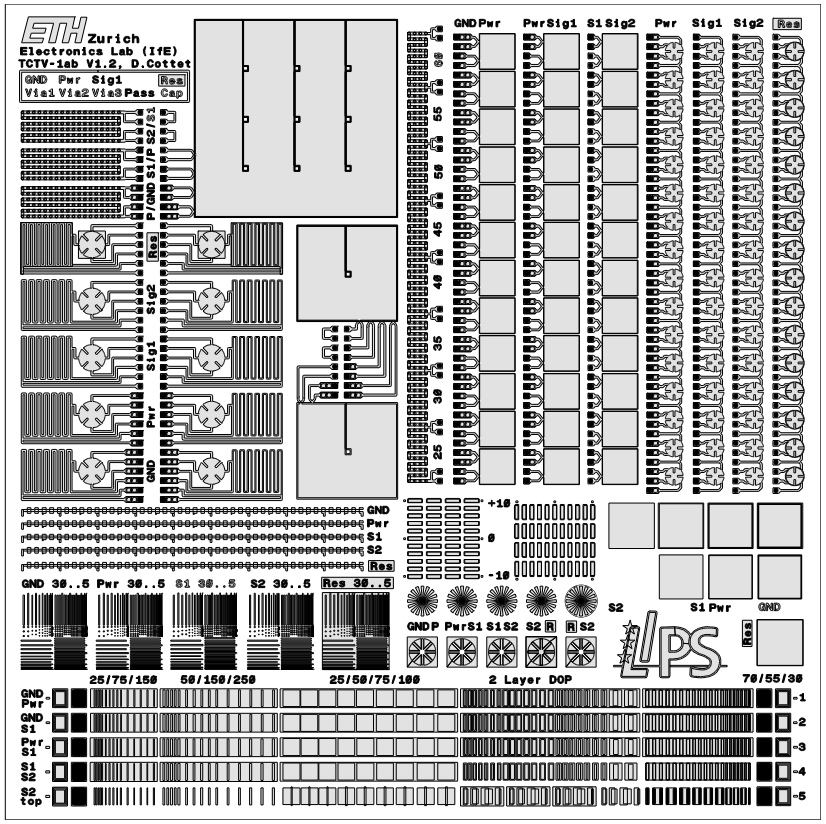


Figure 5.13: *Technology characterisation test vehicle (TCTV) for four-layer thin film build-ups realised within the LIPS project. The TCTV outline is 21.6 mm × 21.6 mm.*

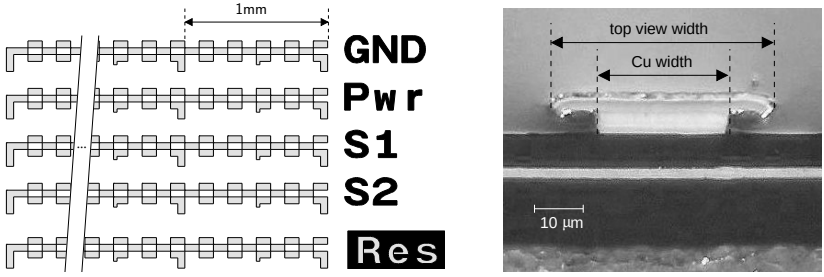
5.3.1. Test Structures and Measurement Methods for Conductor Layers

This first group of test structures measures the accuracy of the conductor dimensions, profiles, surface roughness and conductivity. Dedicated test patterns aim at determining the minimum design rules.

Conductor Line Width

The simplest way to measure the conductor dimension variations is to use a microscope to measure the conductor width of any known structure. For that special purpose the patterned lines shown in Figure 5.14(a) were designed providing 100 μm units as spatial reference. This simplifies the procedure of doing equidistant discrete measurements along the line. The small units of $l_{ts_1} = 100\mu$m and the total line length of $l_{ts_2} = 9$mm provide spatial information in the wide range of micro and macro non-uniformities.

Top-view measurements are however very treacherous as only the highest visible features are measured. In the case of a pronounced mushroom effect as shown in Figure 5.14(b) (conductor cross-section of a Cu/Ni/Au metallisation stack) this leads to incorrect results and other methods must therefore be applied.

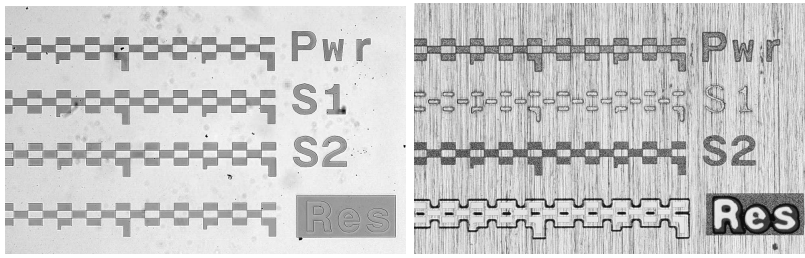


(a) (b)

Figure 5.14: *Patterned line structures (a) and conductor cross section (b) for line width measurements.*

The long line test patterns are capable of revealing many interesting metallisation process characteristics. Figure 5.15(a) shows almost perfect metallisation with correct dimensions, straight edges and sharp corners on all layers including the resistor layer. The example in Figure 5.15(b) shows heavy undercut with rounded corners on signal layer 1 (S1) and a similar undercut but with sharp corners on the resistor layer (Res). The other two layers (Pwr and S2) look much better but with slightly different edge definitions.

Another method also included on the TCTV uses track resistance



(a) (b)

Figure 5.15: *Examples of patterned long line structures on high resolution, high accuracy MCM-D technology(a) and on a second, less accurate MCM-D technology (b).*

measurements of at least two long (meander) lines with known line width differences Δw and length l. The proximity of the two measured lines must guarantee that they have the same undercut, and hence Δw remains unaffected. With the two measured track resistances R_{meas1} and R_{meas2} the Equations 5.3 and 5.4 can be solved giving the sheet resistance R_{sheet} and the line widths w_1 and $w_2 = w_1 + \Delta w$.

$$R_{meas1} = R_{sheet} \cdot \frac{l}{w_1} \tag{5.3}$$

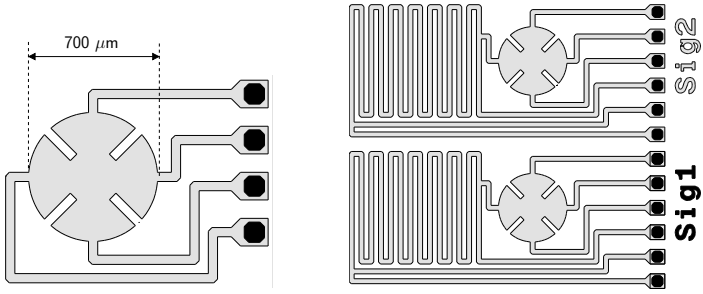
$$R_{meas2} = R_{sheet} \cdot \frac{l}{w_1 + \Delta w} \tag{5.4}$$

This method only provides an average line width and an equivalent sheet resistance assuming rectangular homogeneous profiles. In all cases, conductor cross sections as in Figure 5.14(b) are necessary to exclude any doubts about the exact conductor dimensions.

Conductor Thickness and Sheet Resistance

In the previous paragraph we have already mentioned the resistance measurement methods and cross sections which as a side-effect also provide the conductor thickness and sheet resistance. A third, and widely used method, is the *van der Pauw* technique, based on the Hall effect

and the Lorentz force [101, 102]. Figure 5.16(a) shows a van der Pauw test structure as proposed by the National Institute of Standards and Technology (NIST) in [103]. A space-saving combination of the meander lines and van der Pauw structures (Figure 5.16(b)) is included on the TCTV for each layer.



(a) (b)

Figure 5.16: *Van der Pauw test structure (a) and combination of van der Pauw and meander lines (b) for sheet resistance, thickness and conductor width measurements.*

The measured resistance R_{meas} and Equation 5.5 are then used to get the sheet resistance R_{sheet}.

$$R_{sheet} = R_{meas} \cdot \frac{\pi}{\ln 2} \tag{5.5}$$

For gathering the spatial distribution of thickness variations in the band of macro non-uniformities, the TCTV contains for every layer 12 mm long chains of 16 small van der Pauw structures with $l_{ts} = 500\mu$m each. To demonstrate the amount of information that is gained through this test structure a quick example is given. In Figure 5.17 the measured sheet resistance R_{sheet} of resistor layers on two different panels and three TVs (#1, #3 and #6) each are plotted. While panel 1 exhibits very uniform distribution along the chains and within the panel, on panel 2 several problems are identified. The first is a general offset of R_{sheet} as consequence of an overall too thin film deposition (low SFD band variation). Second is that the TVs on the panel edges (#1 and #6) have much higher sheet resistivity than TV#3 in the centre (mid SFD band variation). And third, the uniformity within the TVs

(along the van der Pauw chains) is very poor at the panel edges but much better in the centre. The latter shows that with such dedicated test structures we can easily detect parameter variations which vary with their actual location.

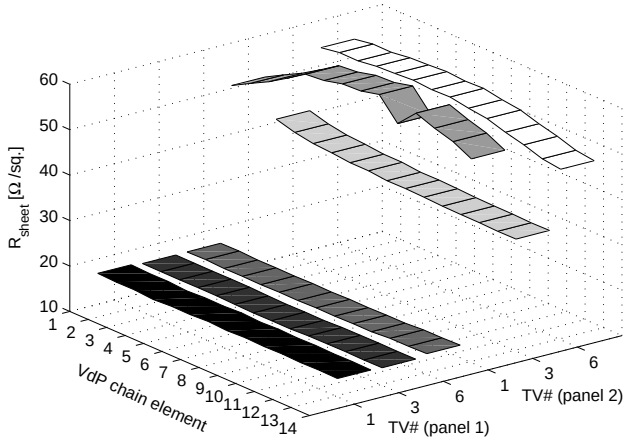
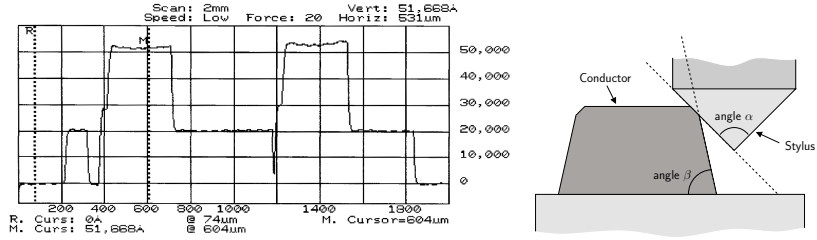


Figure 5.17: *Spatial distribution of sheet resistance measurements performed on two panels and three TVs each.*

The limitation of the van der Pauw method is again complex metallisation such as the Cu/Ni/Au stack shown in Figure 5.14(b). In such cases the extracted sheet resistance represents the equivalent value of a parallel resistor circuit of the single stack layers. Again, only cross sections can reveal the last details about the metallisation stack.

The fourth method for conductor thickness measurements is the use of a profilometre. Such measurements provide continuous thickness profiles with very high accuracy (depending on the equipment used) and no need for special test structures. Figure 5.18(a) shows the measured profile of partially Ni/Au plated Cu conductors. This technique has two main drawbacks: first, the measured profiles must be mechanically accessible. This means that for measuring inner layers or passivated layers the fabrication process must be interrupted. Second, because of the obtuse angle of the stylus head (typically $\alpha = 45° - 60°$), steep conductor side walls with $\beta > 90° - \alpha/2$ are not measured correctly (see Figure 5.18(b)).



(a) (b)

Figure 5.18: *Profilometre measurement of the thickness contour of 2 µm Cu with 3.5 µm Ni/Au (a), and illustration of stylus head (b).*

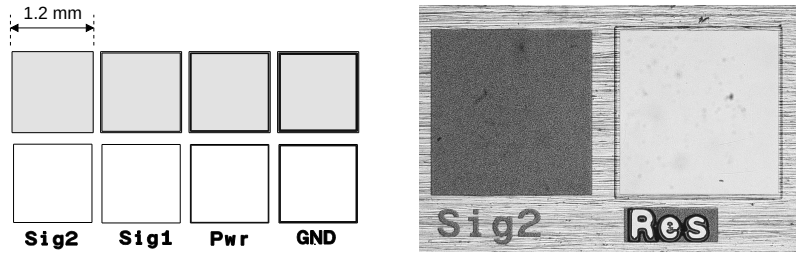
Conductor Surface Roughness

Previous chapters have shown that the conductor surface roughness can have a significant impact on the ohmic losses at millimetre-wave frequencies. Two definitions exist for the surface roughness, R_q or R_{RMS} is the root-mean-square (RMS) roughness value and R_a represents the arithmetic mean roughness value [31]. Unfortunately, R_q and R_a are often confused in publications where R_a is wrongly referenced as the RMS value.

Qualitative roughness analysis can be performed with optical microscopes or scanning electron microscopes (SEM). For quantitative roughness measurements the most common methods are mechanical and optical profilometres or, for sub-nanometer resolutions, atomic force microscopes (AFM). Independently of the used technique, the TCTV designs provide on each layer and for each type of surface (metals, dielectrics and resistors) dedicated measurement areas (see Figure 5.19). To access inner layers, in many cases, but depending on the process, the fabrication flow of a wafer must be interrupted to perform the measurements.

Design Rules

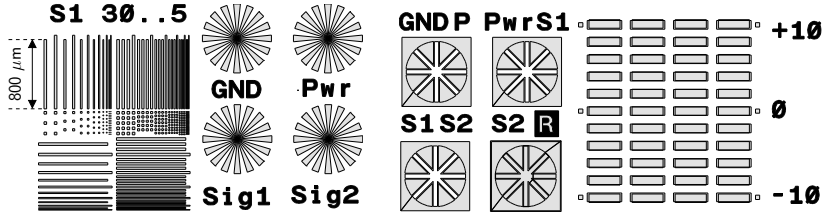
The first experiment when analysing the process' definition and resolution limits is to observe the effects when going beyond these limits. The second is to test the interlayer resolution defined by the layer align-



(a) (b)

Figure 5.19: *Layout example (a) and actual photograph (b) of test areas for surface roughness measurements.* Sig2 = *top metal layer,* Res = *resistor layer.*

ment (β_x and β_y) and torsion (β_τ). For that purpose many test patterns have been developed and implemented on the TCTV. This includes sets of parallel lines with varying line spaces and widths and Agfa flowers (Figure 5.20(a)) for the within-layer parameters, nonius lines and overlapping star patterns (Figure 5.20(b)) for the inter-layer parameters.

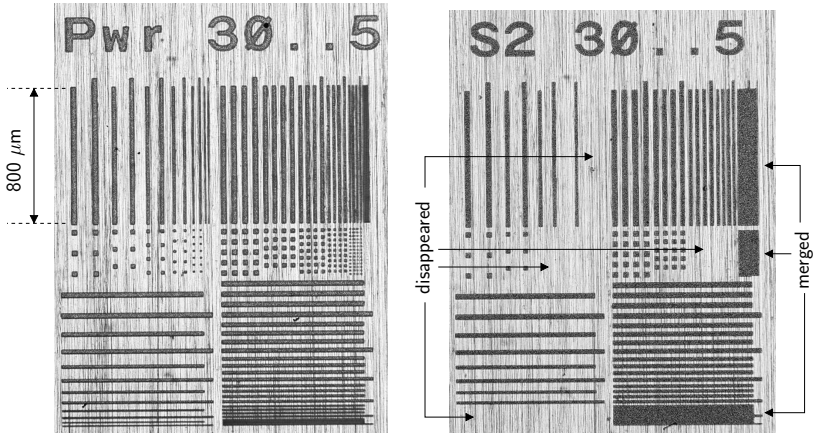


(a) (b)

Figure 5.20: *Layout examples of test structures for conductor resolution (a) and layer alignment (b).*

A pronounced effect of an unstable process is illustrated in Figure 5.21 showing the parallel line patterns on two different layers. In Figure 5.21(a) even the smallest lines and spaces ($l = s = 5\mu$m) are

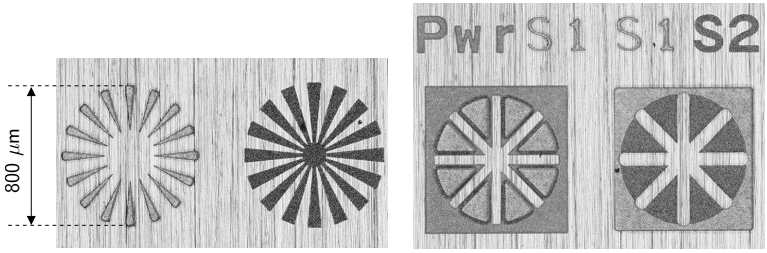
well resolved while in Figure 5.21(b) the isolated small lines have completely disappeared and the same small lines lying close to each other have merged to form one big metal surface. In this special case, different design rules apply for the different layers.



(a) (b)

Figure 5.21: *Photographs of resolution test structure showing well resolved lines and spaces (a), compared to low resolution lines where small structures disappeared and small spaces merged (b).*

The Agfa flowers depicted in Figure 5.22(a) show the different metallisation characteristics on two different metal layers. For the interpretation of these patterns it is important to consider the target application and its potential metallisation layouts and resolution requirements. If only transmission lines are planned, the edges, corners and small space resolutions are not as critical as for integrated passives with close coupled lines requiring very small spaces. The overlapping star patterns in Figure 5.22(b) show precise layer alignment. This will for example allow reduction of the minimum diameter a_{min} of via landing pads, thus reducing the minimum via pitch p_{min}.



(a) (b)

Figure 5.22: *Photographs of Agfa flowers showing the line space and width resolutions on different layers (a) and overlapping stars showing interlayer alignment (b).*

The TDR Alternative

Time domain reflectometry (TDR) is typically used to determine the transmission line parameters in communication systems. TDR has also the advantage of providing results in the time domain which can easily be transformed into the spatial domain using the signal propagation velocity. This feature was investigated in [104] where the line width and dielectric thickness variations along transmission lines were extracted from measured impedance profiles. This method however exhibits some disadvantages: The first is that TDR requires dedicated equipment with fine pitch connectors or probes and sensitive calibration procedures which render the measurement more cumbersome than necessary. Secondly, the separation of the two parameters line width and dielectric thickness requires more elaborate measurement and numerical extraction methods. And thirdly, to achieve high spatial resolution, fast pulse rise times are necessary which are only available in high end TDR devices.

5.3.2. Test Structures and Measurement Methods for Dielectric Layers

The second group of test structures measures the dielectric layer parameters thickness, degree of planarisation, via definition and via design rules.

Dielectric Thickness

Parallel plate capacitors with well defined plate dimensions are included on all TCTVs. If we assume known dielectric permittivity, the capacitors allow extraction of the dielectric thickness between any two metal layers. The thickness h is found with Equation 5.6 where A is the plate area, C_{meas} the measured plate capacitance, ϵ_0 ($= 8.85419 \cdot 10^{-12}$ As/Vm) the free space permittivity and ϵ_r the material's relative permittivity.

$$h = \frac{A}{C_{meas}}(\epsilon_0 \cdot \epsilon_r) \tag{5.6}$$

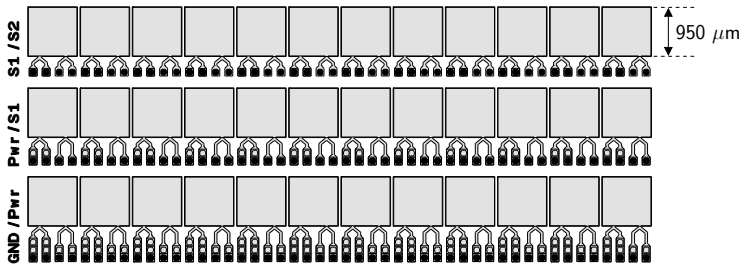
Figure 5.23(a) shows the chains of 12 adjacent capacitors with 950 μm plate length and 50 μm space each. They determine the dielectric thickness variations along a 12 mm distance with discrete measurement locations each separated by 1 mm. This gives information about thickness variations in the spatial range of $2\text{mm} < \lambda_v < 12\text{mm}$ – the macro non-uniformities in the mid SFD band.

If the permittivity is not exactly known, we must use cross sections (see Figure 5.23(b)) to measure the exact thickness and as consequence also to extract the dielectric permittivity with Equation 5.6. As a side effect, and if overlapping structures are available with cross sections, we can also determine the degree of planarisation (DOP) of the investigated material.

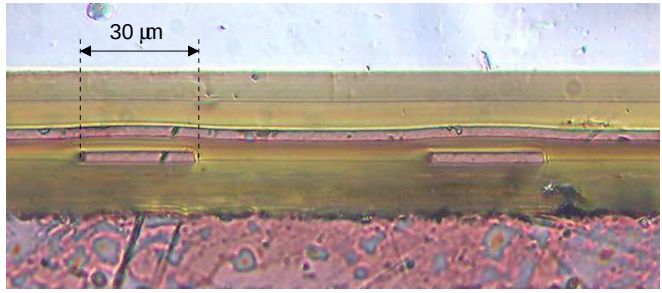
Just as for the conductor thickness, if the measured dielectric layers are mechanically accessible profilometres can be used as exact method of also providing spatial variation information.

Dielectric Surface Roughness

The surface roughness of a dielectric layer is very important as it determines the roughness of a conductor deposited on its surface. Depending on the deposition process the bottom surface of the metal more or less adopts the roughness of the underlying material. In the case of microstrip line configuration it is the bottom surface of the conductors that affect the ohmic losses. The measurement methods are the same as presented earlier for the conductor surface roughness using profilometres or AFM.



(a)



(b)

Figure 5.23: *Layout example of capacitor chains (a) and photograph of cross section (b) for spatial distributed dielectric thickness measurements.*

Via Size, Opening and Resistance

Four point Kelvin style resistance measurements of long via chains allow extraction of the resistance of single vias (Figure 5.24(a)). The best way to design via chains is to use one line-square equivalent per via and one line-square per via connection line (Figure 5.24(b)). The via chains included on the TCTVs consist of 108 vias (with one line square equivalent each) and 109 connection line squares. The 109 connection line squares are divided in 55 upper layer lines and 54 lower layer lines. With this the total chain resistance R_{meas} adds up to 108 via squares R_{via}, 55 upper layers squares $R_{sheet_{upper}}$ and 54 lower layer

squares $R_{sheet_{lower}}$. The single via resistance is then calculated with Equation 5.7.

$$R_{via} = \frac{(R_{meas} - 55 \cdot R_{sheet_{upper}} - 54 \cdot R_{sheet_{lower}})}{108} \tag{5.7}$$

Topological via parameters are measured optically. Top view microscope measurements as shown in Figure 5.24(b) are used for the top and bottom edge diameter. Cross sections on their side can provide much information about the via profiles (aspect ratio and angle), the side wall metallisation and the mask alignment. For quantitative measurements of via cross section as shown in Figure 5.24(c), it must be guaranteed that the section is going through the centre of the via.

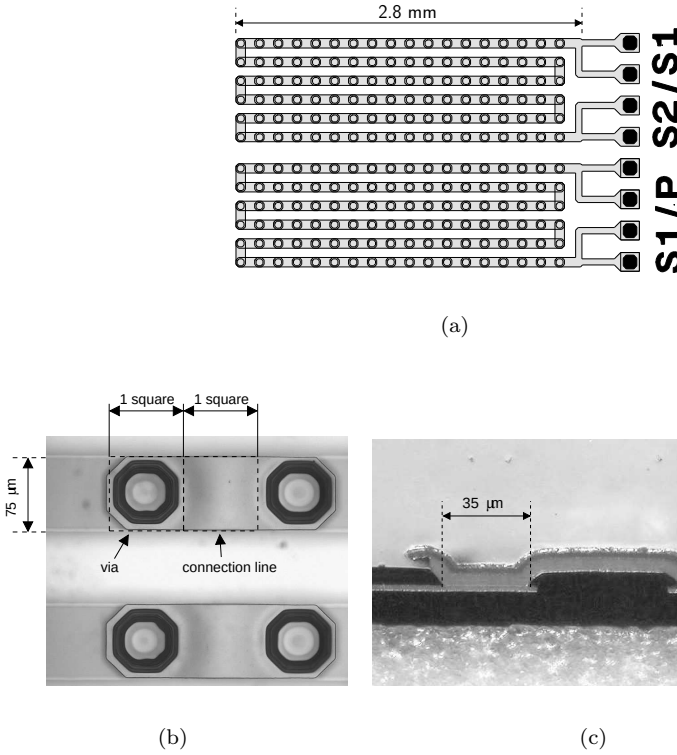
The TDR Alternative

As mentioned in the previous section on conductor parameter measurements, the TDR technique also provides data about the dielectric parameters.

5.3.3. Assessing Measurement Results

The most important factor when performing measurements is the correct interpretation of the measured values. Some aspects are repeated briefly here for the sake of completeness.

- Every measurement equipment used has its well specified measurement ranges and measurement noise figures. Especially when aiming at technology parameter variations, the variations induced by the test equipment must be characterised in advance and its standard deviation declared as uncertainty caused by measurement noise.
- The influence of the environment while measuring is also very important. Again technology parameter variations and room temperature variations must clearly be separated.
- Some equipment or techniques require calibration of the test fixture. It might be a cumbersome procedure but if the calibration starts drifting as the equipment heats up, it is very likely that the drift is misinterpreted as technology parameter change.



(a)

(b)

(c)

Figure 5.24: *Layout of long via chain for via contact and resistance measurements (a) and photographs of via chain elements for optical analysis and measurement of via opening (b) and via profiles (c).*

5.4. Process Control

It was mentioned in Chapter 3 that one of the three performance factors is the process accuracy. Therefore it is very important to make use of effective process control methods in order to keep a constant process performance during manufacturing. The previous section introduced a range of test structures aiming at full characterisation of technology material and 3D topology parameters. These structures can also be used for monitoring purposes in process control. But here, two more factors must be considered: first, the substrate area used by the monitoring

structures is to be minimised and second, the structures must be placed at representative locations covering the wafer areas according to the spatial occurrence of parameter variations.

Introductions on statistical process control and definitions of terms can be found in [45, 105, 106]. This section is emphasising a new approach first presented in [96] and [107] which accounts for the spatial variation distribution by dividing the manufacturing panels into process related zones.

5.4.1. Introducing the Zone Based Process Control

Large area panel processing was in the past often the object of investigations as a solution for reducing the manufacturing costs of thin film substrates. First attempts were presented by the CILAP consortium [91, 108, 109] and later by the European LAP consortium [99, 110]. The essential conclusion of the two projects was that the within-panel non-uniformity become very important while in order to achieve any cost reduction the yield on large panels must reach the same values as with small panels.

A major problem when monitoring a large area process is its (non-) uniformity as parameters can drift at one end of the panel and remain constant at the other end. Correct monitoring of such a process must recognise this difference and provide information on local process parameters. When this is the case full panel coverage is achieved. In [111] Ross and Atchison describe the wafer-zone methods for process monitoring and yield analysis of semiconductor wafers. A similar approach is proposed in [112] where spatial yield modelling for semiconductor wafers is used to separate zero yield regions and non-zero yield regions.

5.4.2. Defining the Panel Zones

Dividing the production panels into zones allows the handling of large panels as several small panels and the application of process monitoring on a smaller scale. The method we propose in this work adopts this strategy and presents a zone-based process monitoring technique for large area thin film production providing full panel coverage. To find appropriate shapes for these zones, we must identify the critical process steps and describe their geometric behaviour. Column A of Figure 5.25 lists three groups of critical process steps and column B shows their geometric s. Local distribution of potential process failures and the resulting zones on a rectangular panel are given in column C.

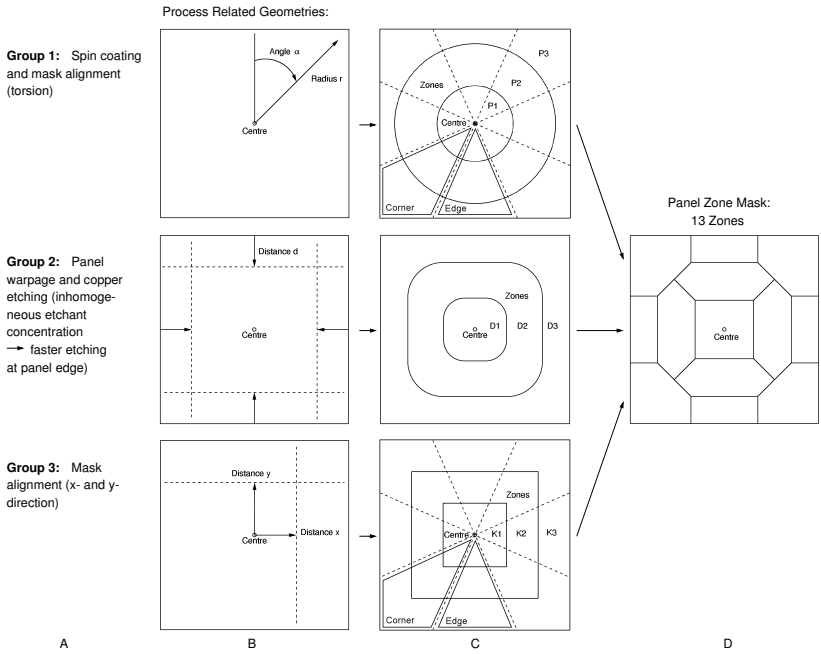


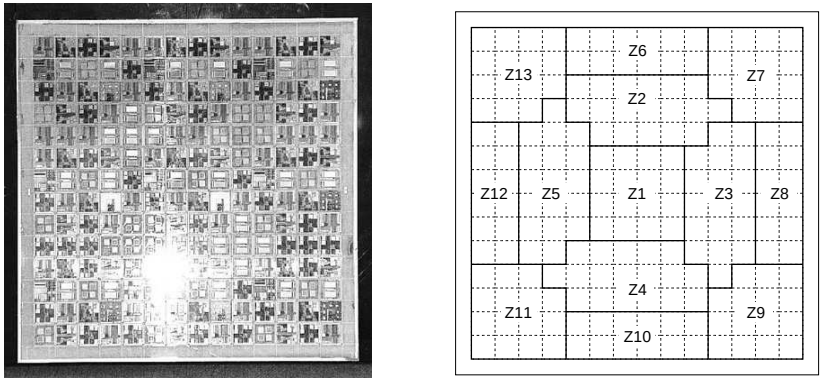
Figure 5.25: *Three groups of critical process steps and their characteristic geometries dividing the panel into zones. Merging the zones of the three groups results in the panel zone mask.*

Spin coating the dielectric layers and the torsion of mask alignment (group 1) are functions of radius r from the panel centre and angle α. This divides the panel into concentric circular zones P1 (centre), P2 (intermediate) and P3 (border), distinguishing corners and edges. Copper etching, which is sensitive to inhomogeneous etchant concentration, is a function of the distance d from the panel border. This and the panel warpage [25] (group 2) divides the panel into zones D1 (centre), D2 (intermediate) and D3 (border). The misalignment of masks in x- and y-direction (group 3) is a function of the distance x and the distance y from the centre and divides the panel into concentric rectangular zones K1 (centre), K2 (intermediate) and K3 (border), again distinguishing corners and edges. Merging the zones of the three groups finally results in the *panel zone mask* depicted in column D of Figure 5.25.

A panel now consists of 13 zones and within each zone similar process parameter values and parameter variations can be expected. In order to handle the zones individually like one small panel each, every zone must contain its own process monitoring structures.

5.4.3. Mapping the Panel Zones

The example in Figure 5.26(a) shows a 12" × 12" panel manufactured within the frame of the LAP project. Figure 5.26(b) shows the resulting panel map when applying the panel zone map onto the example panel, dividing it into 13 zones (Z1 – Z13).



(a) (b)

Figure 5.26: *Photo of a 12" × 12" panel (a) and the resulting panel zone map when the panel zone mask is applied (b).*

We present two methods to place process monitors with minimised area consumption. The first method (P1) is to include one process monitor in each zone as illustrated in Figure 5.27(a). The second method (P2) proposes cross-like process monitor lines plus four monitor cells in the corner zones (Z7, Z9, Z11 and Z13) as depicted in Figure 5.27(b).

The cross-like process monitor line proposed for placement method P2 has a width PW which depends on the number and size of used structures and is in the range of 2–4 mm. Figure 5.28 shows a detailed view of a 3.9 mm wide example monitor line.

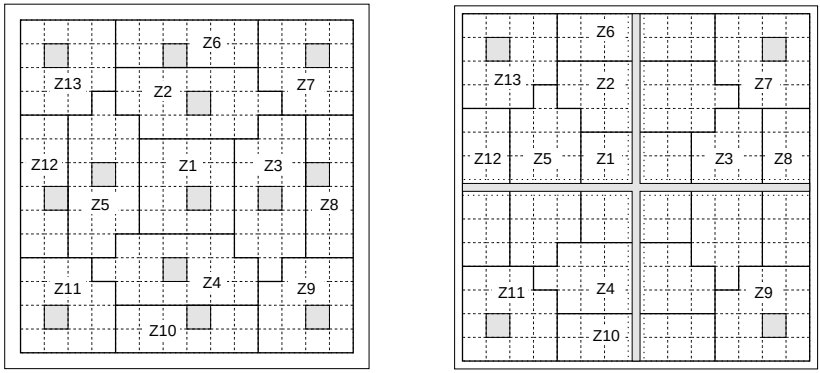


Figure 5.27: *Two possible placement methods P1 (a) and P2 (b) for monitoring structures, both ensuring coverage of each zone.*

We can express the total relative area consumption AC for the two methods with the Equations 5.8 and 5.9 where PM is the number of process monitors ($PM = 13$ in the case of 13 panel zones), S the number of substrates along one side of the panel, and PW the absolute width of the monitor lines.

$$AC_{P1} = \frac{PM}{S^2} \cdot 100 \tag{5.8}$$

$$AC_{P2} = \left(2PW - PW^2 + \frac{4}{S^2}\right) \cdot 100 \tag{5.9}$$

The area consumption calculation determines which placement method is to be used. Figure 5.29 shows that in the case of $PW = 3.9$ mm the break-even is at $S = 18$. The 12" × 12" panel presented earlier contains 14 × 14 substrates ($S = 14$), therefore method P2 is preferred.

5.4.4. Benefits

The benefits of the panel zone approach are twofold. First, test time and yield losses can be minimised during production. If, for example,

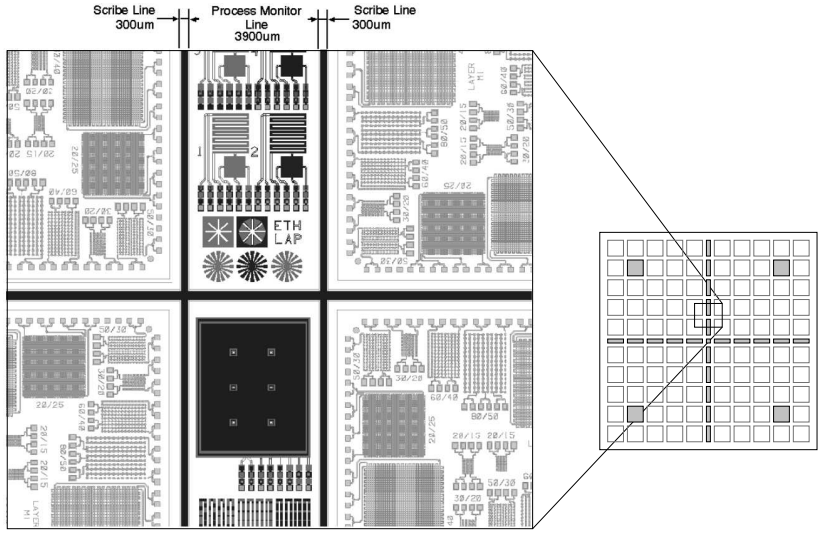


Figure 5.28: *Detail view of a 3.9 mm wide monitor line with 0.3 mm scribe lines. The figure shows examples of monitoring structures such as van der Pauw structures, meanders, Agfa flowers and a plate capacitor.*

the process monitor of one zone shows measurement out of specification limits while all others are correct, only the substrates within this zone are declared as non-conforming and scrapped, thus reducing the time for final testing. Second, the monitor measurement results provide spatial information of within-panel process variations. According to the definition of panel zones presented in the previous paragraph, the locations of the outliers give information on potential causes for process failures.

5.5. Summary

In this chapter all relevant technology parameters in terms of millimetre-wave system integration have been identified. Then the *spatial frequency description* (SFD) was introduced proposing a new method to describe the local distribution of parameter variations. In order to acquire this information a dedicated test vehicle for technology characterisation (TCTV) was implemented. The TCTV provides test structures capable of preserving the spatial distribution of measured pa-

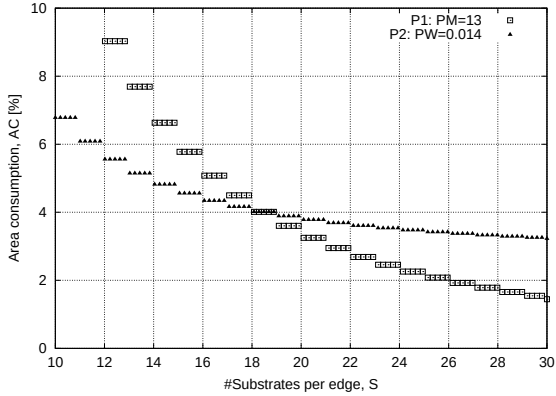


Figure 5.29: *Area consumption for the placement methods P1 and P2 compared for different numbers of substrates S along the panel sides.*

rameter variations. The benefits of using the SFD were demonstrated and an adaptation for use in process monitoring applications was proposed with the panel zone based process control approach. Taking advantage of the spatial distribution of process variations this method divides the panel into process related zones and treats them as individual small panel. As a consequence test time and yield losses are reduced.

6

Technology Alternatives

This chapter investigates thin film and laminate technologies with regard to their millimetre-wave suitability. For each technology typical physical and electrical material parameters are discussed and illustrated by means of actual photographs or measurements. Important aspects are the compatibility of the various materials and process options as well as unwanted effects of some process steps affecting the electrical performance at target frequency (see also Chapter 2). The proposed alternatives are compared in a case study, using the benchmark tool presented in Chapter 4 and a 77 GHz transceiver module acting as benchmark reference application. Seventeen representative technology examples were chosen, covering the categories of thin film (MCM-D), laminate (MCM-L) and thin film on laminate (MCM-L/D). The investigated examples were manufactured for technology characterisation purposes within the European research projects LAP [99] and LIPS [100].

6.1. Material and Process Alternatives

Chapter 3 states that the overall performance of a millimetre-wave system depends on three aspects, the intrinsic material properties, the technology build-up quality and the RF design and layout optimisation. For the material properties and technology build-ups many alternatives exist offering a wide range of technology enhancement options with regard to physical and electrical aspects, availability and cost. In order to identify potential problems in high volume production it is imperative to remember the origins of these technologies. While MCM-D is often manufactured on lower end VLSI or flat panel display (FPD) equipment, MCM-L processes use high-end PCB equipment. This means that the two technologies are operating at opposite risk levels.

Processing alternatives are presented without going into the details of each process step. Instead, their relevant technological and electrical issues in term of RF performances of integrated systems are discussed. More literature on processing of thin film and laminate substrates can be found in [34, 113].

6.1.1. Conductor Layers

The conductors for RF signal transmission are the primary elements of technology build-up and discussed in this section. Table 6.1 lists the most common materials with their deposition and patterning methods used today.

Table 6.1: *Conductor technology alternatives*

Materials	Copper (Cu), aluminium (Al), gold (Au), silver (Ag)
Deposition	Sputtering in vacuum chamber, electroplating with sputtered seed layer, electroless plating.
Patterning	Wet etching with deposited and photo-lithographically defined mask, spray etching with resist mask, dry etching, electroplating inside patterned resist mask.

Thickness

Laminated dielectric layers typically need thick copper layers for two main reasons. The first is that thin (1–2 μm) layers are not able to planarise the rough laminate surface. Secondly, in order to withstand

the vertical elongations as a result of the high CTE values in z-direction, the via side walls need a minimum metal thickness of 5–10 μm [114].

In terms of insertion losses the thickness becomes important when the skin depth is larger than about 1/3 of the track thickness. On the other hand, if the metal thickness is too large, the equivalent line width extension starts affecting the effective line width. In between these two limits the metallisation process itself determines the performance. Wet etching processes for conductor patterning are preferably used on thin metal layers. One reason for this is the inevitable undercut which is equal to the metal thickness and therefore smaller on thin layers. Secondly, the within-wafer homogeneity of the etch process depends on the local etch rate which in turn depends on the local etchant concentration. On thin layers the etch rate differences are smaller than on thick layers. Typically, on a 5"wafer with 2 μm copper, the undercut along the edges is 1–2 μm larger than in the centre.

The total thickness of electroplated metals depends on the local current density which itself depends on the local metal pattern density. The electroplated metallisation quality is influenced by the applied currents. Low quality metallisation is evident for example when the deposited copper shows large grains and voids.

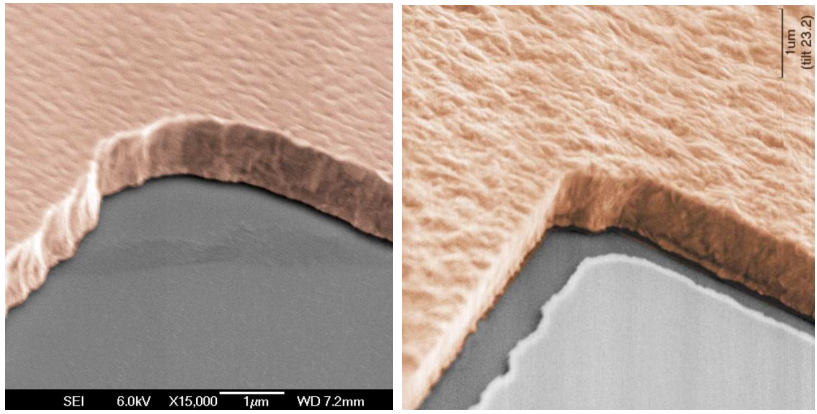
Surface Roughness

Chapter 2 showed that at millimetre-wave frequencies the surface roughness has strong influence on the ohmic losses. Typically, electroplating processes yield much rougher surfaces than sputtering processes. On the other hand, etched conductors show rougher side walls than traces that have been plated inside resist masks (see Figure 6.1).

Thick metal layers use mainly electroplating processes as they have much faster deposition rates compared to sputtering. But with increasing thickness, the conductor surface roughness becomes more accentuated. Figure 6.2 shows AFM measurements of 10μm thick copper on laminate substrates. The RMS surface roughness is $R_q = 740n$m on Espanex (NSC) [115] and $R_q = 650n$m on Biac LCP [116].

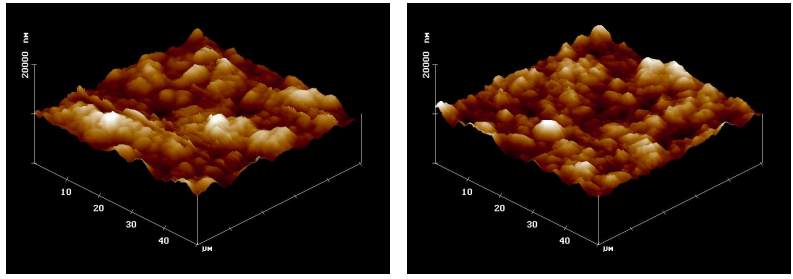
Conductor Profiles

With electroplated conductors, undercut problems occur when the seed layer is removed by a wet etching process. Technically, the seed layer is very thin ($\ll 1\mu$m) and therefore the undercut should remain negligible. However, operators tend to purposely overetch in order to eliminate all



(a) (b)

Figure 6.1: *SEM photographs of sputtered (a) and electroplated (b) copper metallisation.* *(Courtesy of Acreo)*



(a) (b)

Figure 6.2: *AFM measurements of electroplated copper on laminates: Cu on Espanex (a), Cu on Biac LCP (b).*

risks of seed layer residues provoking short cuts [117]. Unfortunately this is all too often done carelessly and causes ugly mushroom-like conductor profiles as depicted in Figure 6.3.

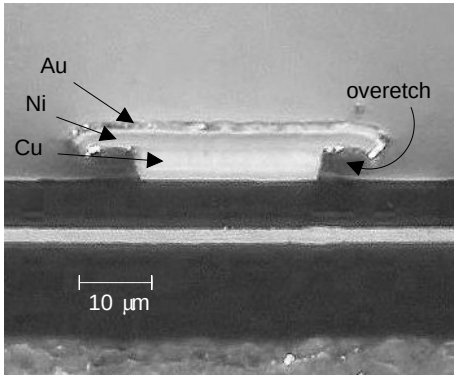


Figure 6.3: *Cross section photograph of mushroom-like conductor profile as the results of an uncontrolled seed layer etch process.*

Etched conductors have typically trapezoidal profiles with positive slopes which, in the worst case have very narrow edges along the bottom. This can lead to increased ohmic losses as the skin effect tends to squeeze the current density along these edges (see also Chapter 2). Electroplated conductors have more rectangular profiles with straight side walls. The side walls however are mainly determined by the resist mask development process.

6.1.2. Dielectric Layers

The dielectric layers accomplish important functions such as electrical isolation of conductor layers, determination of RF characteristics and mechanical protection in the form of top layer passivation. Table 6.2 lists the most common materials with their deposition and patterning methods used today.

Table 6.2: *Dielectric technology alternatives*

Materials	Polyimide (PI), benzocyclobutene (BCB) and diverse laminate materials.
Deposition	Spincoating, Meniscus coating and lamination of prepregs or resin coated copper foils (RCC).
Patterning	Photo-lithography, plasma etching (reactive ion etching, RIE) and laser drilling.

Materials

Polyimide was for a long time the quasi-standard for thin film dielectrics, despite its high moisture absorption ratio and high dielectric loss tangent ($\tan\delta = 0.002$ @ 1 kHz). Benzocyclobetene (BCB) is best known from the Cyclotene product line from Dow Chemical, which provides much better dielectric properties ($\tan\delta = 0.0008$ @ 1 GHz) and very low moisture absorption. Since several years BCB is more and more replacing Polyimide in many applications, especially where high frequency performance is demanded. Polyimide remains a popular material for medical implants for its biocompatibility [118].

For laminate technologies great progress was made in recent years and many low loss polymer materials are available today. Very promising are the *liquid crystal polymers* (LCP) with low dielectric losses ($\tan\delta = 0.002$ @ 3–45 GHz) and low thermal expansion coefficient ($CTE_Z = 16$ ppm/°C) [116, 119].

Thickness

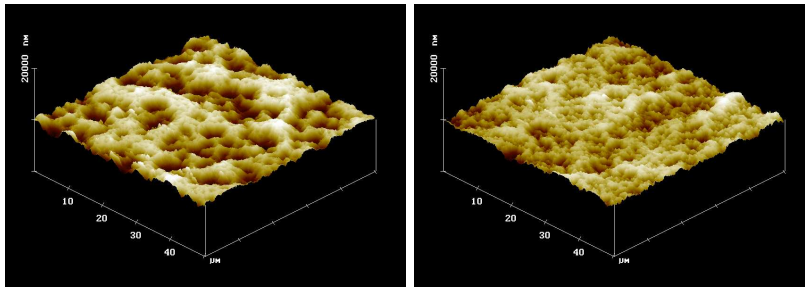
In Chapter 2 the dielectric thickness was described as an important topology parameter for integrated passives. It has a considerable impact on the choice of transmission line configurations and on component performance.

Until recently, BCB dielectrics were recommended for single layer thicknesses up to maximal 14 μm. However, newly developed BCB formulas will soon allow thicknesses up to 25 μm per layer. The overall thickness tolerance of typical dielectrics is in the range of 5–10%. These values are mainly wafer-to-wafer and batch-to-batch variations rather than within-wafer variations which are significantly smaller.

Note that the specified thickness tolerances do not include the planarisation capabilities of the materials. This effect is separately referred as the degree of planarisation (DOP) and is an important factor to consider when measuring or specifying the local thickness of multilayer integrated structures or structures requiring underpasses. The DOP is strongly dependent on the dimensions and spaces of the materials being covered or planarised. Laminate materials have usually DOP values close to 100%, BCB is in the range of 75–85% and Polyimide has much lower DOP values, around 50% [83].

Surface Roughness

Most laminate materials have compared to thin film dielectrics a very pronounced surface roughness. New materials such as liquid crystalline polymers provide a much smoother surface, but are still not comparable to BCB (see Figure 6.4). Measured RMS values are in the range of R_q = 0.4–0.7μm. AFM measurements of BCB exhibit a surface roughness in the nanometer range up to few nanometers after plasma etching for increased adhesion (see Figure 6.5).



(a) (b)

Figure 6.4: *AFM measurements showing the surface roughness of Espanex (a) and Biac LCP (b) laminates.*

6.1.3. Base Materials

The base materials have either a pure carrier function for supporting subsequent interconnect build-ups or they also provide re-routing or interconnect functionalities. Table 6.3 lists some common base materials and packaging functionalities.

Table 6.3: *Carrier technology alternatives*

Materials	Metals (Cu, Al, Si), metal alloys (F45), ceramics (Al_2O_3 96% or 99.6%, AlN) and laminates.
Packaging	Mechanical carrier, redistribution, interconnection and RF functionality in combination with build-up layers.

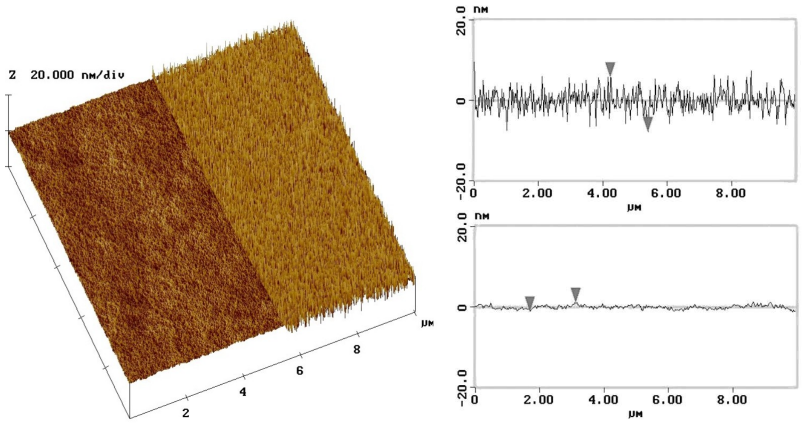


Figure 6.5: *AFM measurements showing the roughness of BCB before and after RIE (in the left figure the two measured profiles are superimposed).* *(Courtesy of Acreo)*

Conductive Materials

With conductive base materials (metals, metal alloys, low resistivity silicon) the use of pure CPW transmission line configurations is not possible. Instead microstrip or GCPW should be used. The choice of base material plays therefore an important role for the overall RF system design.

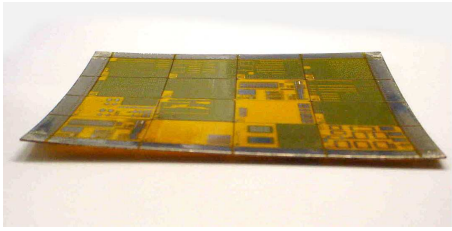
Dielectric Material

Non-conductive base materials (ceramics, laminates) allow the use of pure CPW transmission line configurations. This however requires low loss dielectric properties as the EM-fields will penetrate the base materials.

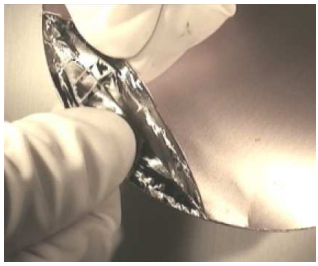
Thermal and Thermo-mechanical Properties

High power amplifiers used in transceiver systems need efficient thermal heat dissipation paths. High thermal conductivity is achieved with metallic base materials (e.g. Cu: 395 W/mK) followed by ceramics (e.g. Al_2O_3: 15–35 W/mK) and laminates with poor conductivity values (0.1–0.6 W/mK).

Another aspect is the material's coefficient of thermal expansion (CTE) which should be matched for different materials attached to each other. CTE differences produce mechanical stress when layers expand differently with temperature changes e.g. during processing or operation. On large panels this effect gets even worse [27]. In this context the elasticity of the materials is important; while elastic materials (laminates, thin metals) tend to bow (Figure 6.6(a)), stiff materials (thick metals, ceramics) produce cracks or delamination in the build-up layers (Figure 6.6(b)).



(a) panel warpage (Courtesy of Thales Microwave)



(b) cracked Si wafer (Courtesy of Thales RT)

Figure 6.6: *Two consequences of thermo-mechanical stress: substrate bow of a small 4" × 4" panel (a) and cracked 5" silicon wafer (b).*

6.1.4. Die Attach

The usable die attach methods mainly depend on the MMIC configurations and the substrate technologies. Alternatives are discussed here in terms of suitability for millimetre-wave applications but are not further investigated nor used for the technology benchmarking in the following sections.

Flip-chip: Flip chip mounting is available with bumps or stubs, both with different solder materials. A problem with flip chipping MMICs is the use of underfills for stress relief. Underfill epoxy materials available today are not conceived for RF applications and have high dissipation factors. Furthermore, MMICs are not designed to be covered with other dielectrics. A method to avoid

underfills is to use CTE-matched materials, bigger bumps or stubs and materials containing Au for higher elasticity.

Wire-bond: Many commercial MMICs today are built in microstrip configuration requiring face-up chip attach for reliable ground contact. In this case only wire or ribbon bonding can be used. Typical MMICs have thicknesses of about 100 μm so that the total wire length gets large and produces inductive interconnects. Several techniques for building cavities can be used, thus allowing chip embedding and reduction of the wire length.

Ribbon-bond: Compared to the circular wires used for wire bonding, the ribbon bonds provide well defined, wide and flat geometries which allow design optimisation with controlled impedance.

TAB: Chip face-up or chip face-down TAB is available today with the advantage of providing a one step-die attach process for high pin count chips. But typical MMICs have a dozen pins, often placed at quite odd locations rendering TAB mounting inefficient. The advantage of having ribbon-like connections can be achieved with ribbon bonding.

Collective wiring: A very interesting die attach and bonding method for RF system integration is the collective wiring as presented in [120]. The MMICs are embedded into cavities inside the base materials *before* deposition of the build-up layers.

6.1.5. Special Purpose Materials

High resistivity and high permittivity materials are often used to extend the functionality of the technology. The materials listed below represent a small assortment of today's alternatives being used or under investigations.

Resistors: For integrated resistors at millimetre-wave frequencies (e.g. for Wilkinson power dividers or 50 Ω loads) high accuracy and low parasitics are required. Meander resistors using the sheet resistivity of copper cannot meet these requirements. Therefore, Ti, $NiCr$, $CrSi$ and other materials with sheet resistivity values in the range of $R_{sheet} = 15 - 50\Omega/\square$ are deposited as thin film resistor layers. For laminate technologies other materials such as Ohmega-Ply® are available [121].

Capacitors: Thin layers of high permittivity materials allow integration of large capacitance values on small areas. Examples are Si_3Ni_4 ($\epsilon_r = 7$), Ta_2O_5 ($\epsilon_r = 25$) and $BaTiO_3$ ($\epsilon_r = 5000$). With these materials, large capacitors for energy storage and decoupling purposes are realisable. Capacitors for use at millimetre-wave frequencies have very small values such that the normal dielectric layers are sufficient for integrating parallel plate or interdigital capacitors.

6.2. Case Study Technologies

The investigated case study technologies include thin film, laminate and thin film on laminate. In the following section we will describe 17 different alternatives, focusing on the material and build-up parameters and giving the necessary technology cost data at the end.

The technology parameters were measured on different quantities of test vehicles ranging from only 3 TVs for MCM-L #1a, 1b and 1d to several dozens for MCM-D #1 and 2. These numbers obviously provide no statistical relevance, but all measurements were discussed with the corresponding manufacturers and completed with statistical production data. Furthermore, those technologies produced by the same manufacturers were cross-compared as they were processed on the same equipment.

6.2.1. Thin Film Technologies

Six different thin film technologies (MCM-D) are investigated. Three of them were developed within the LAP project and three within the LIPS project. The LIPS technologies are expected to provide much better performance as the dielectric thickness was increased to 45μm.

MCM-D #1

The first example is a thin film technology with $3 \times 6.5\mu$m BCB dielectrics on a Rogers RO4003 [122] laminate carrier (500μm for MCM-D #1a and 800μm for MCM-D #1b). A Cu metallisation is electroplated using a sputtered TiW adhesion and Cu seed layer. The top metallisation provides an electroplated Ni/Au finish serving as barrier and passivation layer and providing wire bond compatible pads. The manufacturing panel size is 4" $\times$ 4".

Comments:

- MCM-D #1 is a standard thin film technology with qualified manufacturability and reliability. These circumstances keep the manufacturing costs low (see Section 6.2.4).
- A high process accuracy and precision is achieved through its optimised process flow (undercut $u = \pm 2\mu$m).
- The thin dielectric build-up combined with the low dielectric permittivity is a disadvantage for millimetre-wave frequencies.
- For microstrip configuration the thin dielectric build-up implies narrow lines and therefore high ohmic losses.
- The Ni/Au finish on the entire top metallisation accentuates the skin effect and renders poor defined conductor profiles such as the mushroom-like undercut effect.

MCM-D #2

This thin film technology again uses $3 \times 6.5\mu$m BCB dielectrics but on a large area Rogers RO4003 laminate carrier with 800μm thickness. The Cu metallisation is electroplated using a sputtered TiW adhesion and Cu seed layer. A Ni/Au finish is electroplated on the top metallisation as barrier and passivation layer and for wire bond compatible pads. The manufacturing panel size is 12" × 12".

Comments:

- The same considerations as above also apply to this technology, except for lowered costs achieved with large area processing (see Section 6.2.4).
- A big disadvantage of using large manufacturing panels is the much higher across-panel non-uniformities compared to small panels. This will become manifest in the parameter variations (undercut $u = \pm 4\mu$m) and component yields.

MCM-D #3

The third technology is an enhanced thin film providing $3 \times 15\mu$m thick BCB layers on a 800μm thick Rogers RO4003 laminate carrier. The inner layers have electroplated Cu metallisation with sputtered TiW

adhesion and Cu seed layer. The top metallisation is electroplated Au to avoid complex metal stacks and BCB passivation layers but still providing bondable pads. A NiCr resistor layer with $R_{sheet} = 38\Omega/\square$ is sputtered underneath the top Au metallisation allowing integrated resistors. The manufacturing panel size is 4" × 4".

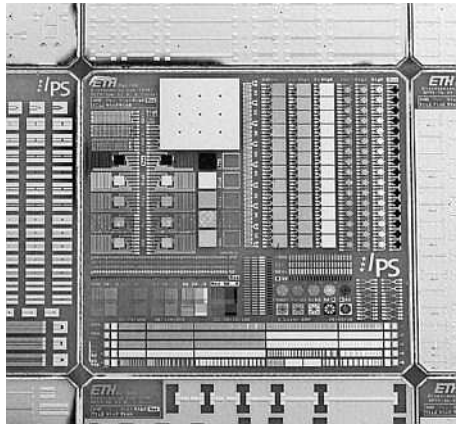


Figure 6.7: *Actual photograph of 21.6 mm × 21.6 mm TCTV manufactured on MCM-D #3.*

Comments:

- The main technology enhancement is the 45μm thick dielectrics allowing for very low ohmic losses and higher flexibility for transmission line impedances.
- The wider conductors of microstrip lines make the impedances less sensitive to process variations (The metal edge accuracy is $u = \pm 1.8\mu$m).
- Pure Au is used for the top layer with slightly lower conductivity, but this avoids the ferro magnetic Ni layer, the mushroom-like undercut effect and the passivation layer.
- The goal of using a low loss RO4003 laminate carrier ($\tan\delta = 0.0027$) is to realise high performance CPW structures.

MCM-D #4

This technology has the same enhanced thin film build-up with $3 \times 15\mu$m BCB dielectrics on a 800μm thick aluminium carrier. The inner layers have electroplated Cu metallisation with sputtered TiW adhesion and Cu seed layer. The top metallisation is electroplated Au to avoid complex metal stacks and BCB passivation layers but still providing bondable pads. A NiCr resistor layer with $R_{sheet} = 38\Omega/\square$ is sputtered underneath the top Au metallisation allowing integrated resistors. The manufacturing panel size is 4" $\times$ 4".

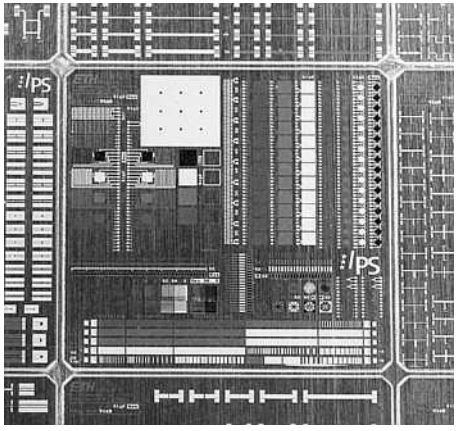


Figure 6.8: *Actual photograph of 21.6 mm $\times$ 21.6 mm TCTV manufactured on MCM-D #4.*

Comments:

- Same considerations and advantages as above also apply to this technology, except for the stiff aluminium base preventing substrate warpage. The rough aluminium surface avoids delamination that could be caused by the remaining mechanical stress.
- The conductive base material also prohibits the use of pure coplanar structures.

MCM-D #5

Another MCM-D technology providing $3 \times 15\mu$m thick BCB dielectrics is proposed, using a high resistivity Si carrier with 800μm thickness. Cu conductors are sputtered with a Ti adhesion layer. The top metallisation is passivated with 8μm BCB while all bond and test pads have an electroplated Ni/Au finish. The Ti layer underneath the top metallisation is also used as resistive layer with $R_{sheet} = 25\Omega/\square$ for integrated resistors. The manufacturing is done on 5" diameter wafers.

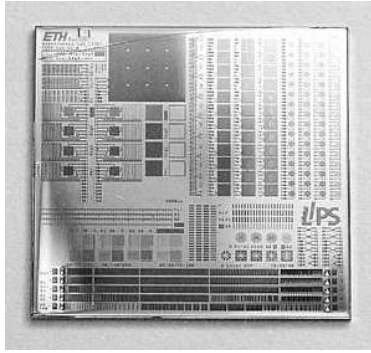


Figure 6.9: *Actual photograph of 21.6 mm × 21.6 mm TCTV manufactured on MCM-D #5.*

Comments:

- The main technology enhancement is the 45μm thick dielectric for low ohmic losses and high range of transmission line impedances.
- The wider conductors of microstrip lines make the impedances less sensitive to process variations.
- Pure Cu metallisation is employed for high conductivity and no profile artifacts caused by Ni or Au deposition. This is possible with a thin BCB passivation layer and locally Au plated test and bond pads.
- The silicon wafers used have very planar surfaces, allowing for very precise definition of conductors (undercut $u = \pm 1\mu$m).

- Mechanical stress caused by the thick BCB stack can cause delamination on the smooth silicon surface.

6.2.2. Laminate Technologies

Ten different laminate technologies (MCM-L) are investigated here; all of them were developed within the LIPS project. The first six technologies have thin film-like metallisation while the other four use the initial copper coating supplied with the laminate materials. The use of thin film-like conductors allows much smaller design rules compared to copper coated laminates.

MCM-L #1

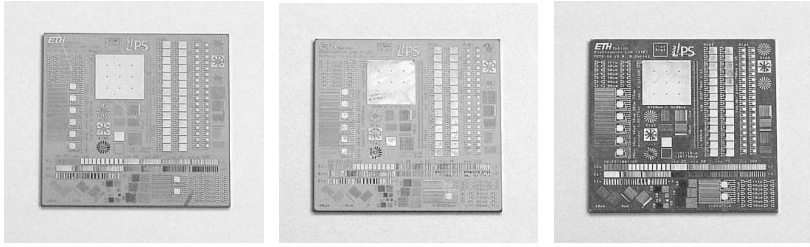
The first MCM-L technology consists of one laminated dielectric layer on a high resistivity Si carrier. Six different combinations of adhesion and laminate materials are investigated. The metallisation consist of an electroplated Cu layer covering the silicon carrier and acting as ground plane plus one electroplated Cu signal layer on top of the laminate dielectric. The initial Cu coating of the laminates is used as via mask for laser ablation. No passivation is used on these substrates, except for a plated Au layer on the test pads. The manufacturing is done on 4" diameter wafers.

Although it has not been practically investigated, all MCM-L #1 technologies will be benchmarked with the possibility of using a resistive layer with $R_{sheet} = 38\Omega/\square$. These layers are assumed to have the same structure definition as the top layer metallisation which is $u = \pm 5\mu$m.

Investigated laminate build-ups are 1) Pyralux & Arlon 85NT, 2) Speedboard C & Espanex, 3) Speedboard C & Biac LCP, 4) Microlam 410 & Espanex, 5) Microlam 410 & Biac LCP and 6) Microlam 410.

Comments:

- The main goal of this technology is to keep the build-up as simple as possible, thus maintaining the manufacturing costs low.
- As a result of the thin film-like metallisation process, the conductor definition is very accurate for a laminate based technology (undercut $u = \pm 5\mu$m).
- The very basic, two-layer topology and the low dielectric permittivities limit this technology to microstrip transmission line



(a) MCM-L #1a (b) MCM-L #1c (c) MCM-L #1d

Figure 6.10: *Actual photographs of 21.6 mm × 21.6 mm TCTVs manufactured on MCM-L #1 technologies (#1b, #1e and #1f are not displayed). The colour differences result from the different laminate materials.*

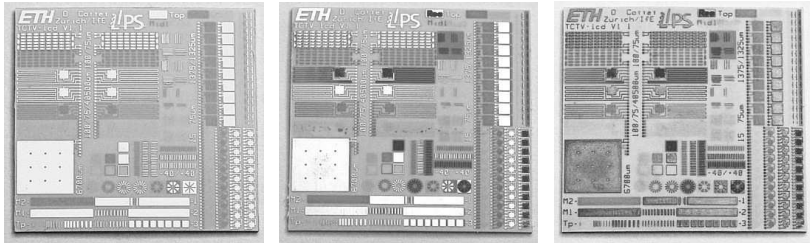
configurations. Furthermore, any kind of multilayer structure is not feasible with this technology.

- The laminate materials used have considerable surface roughness ranging from $R_q = 0.44 - 0.63\mu$m and contribute to the total insertion losses.
- Laminated dielectrics require thicker metallisation for high via reliability. This is minimised when using laminates with lower CTE values in z-direction such as Espanex ($CTE_Z = 32$ ppm/°C), Microlam ($CTE_Z = 19$ ppm/°C) or Biac LCP ($CTE_Z = 16$ ppm/°C).
- Thick metallisations defined with subtractive etching processes imply controllable but high undercut and define the lower limits for the smallest possible line spaces.

MCM-L #2

In contrast to the previous MCM-L, this technology uses a conventional laminate build-up. It consists of four symmetric dielectric layers on each side of a Rogers RO4003 core with through hole vias in the core and laser ablated microvias in the build-up layers. Four different combinations of adhesion and laminate materials are investigated.

The metallisation uses the initial Cu coating supplied with the laminates covered with an electroplated Cu layer for via metallisation. Two different top metallisations have been investigated: pure copper with electroplated copper test pads and all structures with an electroplated Ni/Au finish. For the technology benchmark only the pure copper version is considered. The manufacturing is done on 9" × 12" panels.



(a) MCM-L #2a (b) MCM-L #2b (c) MCM-L #2d

Figure 6.11: *Actual photographs of 28.1 mm × 28.1 mm TCTVs manufactured on MCM-L #2 technologies (#2c is not displayed). The colour differences result from the different laminate materials.*

Investigated laminate build-ups are 1) Speedboard C & Biac LCP, 2) Microlam 410 & Biac LCP 3) Microlam 410 and 4) Speedboard C.

Comments:

- This technology corresponds to the widely used symmetric PWB technology with well optimised materials and reliability and very low manufacturing costs. The achieved metal edge accuracy is $u = \pm 8\mu$m.
- New laminate materials available today provide millimetre-wave compatible low loss dielectrics.
- The laminate materials used have non-negligible surface roughness ranging from $R_q = 0.44 - 0.63\mu$m and contribute to the total insertion losses.
- Typical laminate substrate design rules are coarse and not accurate enough and unlikely to meet the requirements for integrated passives at millimetre-wave frequency.

- Large manufacturing panels cannot provide high enough across-panel accuracy. Using smaller panels would however increase the manufacturing costs.

6.2.3. Mixed Build-Up Technology

Finally, a thin film on laminate mixed build-up technology (MCM-L/D) is investigated.

MCM-L/D

A symmetric laminate carrier with two dielectric layers serves as base for a thin film build-up. The MCM-L carrier consists of a Rogers RO4003 core with through hole vias, laser ablated microvias in the build-up layers and a thin laminated and ground planarisation layer on top. The laminate materials are Speedboard C and Biac LCP. The MCM-D build-up has $3 \times 15\mu$m BCB dielectric layers with sputtered Cu metallisation, Ti adhesion layer and top metallisation passivated with 8μm BCB. Bond and test pads have electroplated Ni/Au finish. The Ti adhesion layer underneath the top metallisation is also used as a resistive layer for integrated resistors. The manufacturing is done on 5" diameter wafers.

Comments:

- The stack of laminate materials plus the thin film build-up allow very thick dielectrics for minimised ohmic losses and increased IP bandwidths combined with the accuracy of thin film metallisation.
- 45μm BCB induce a mechanical stress affecting the planarity of the laminate base thus reducing the accuracy of the thin film layers (undercut $u = \pm 1.5\mu$m).
- The via transitions connecting the upper thin film layers to the inner laminate layers require long staggered via chains.

6.2.4. Technology Costs

It is generally very difficult and delicate to give cost figures for technologies originating from different sources and calculated at different stages of development, ramp up or product life. One reason is that cost

models and figures are often not accessible or must remain confidential. Furthermore, cost models used at different companies can vary so much that similar technologies can have different cost numbers. Finally cost figures available in publications must be treated with care as they might be embellished.

The cost figures utilised here are based on cost modelling techniques developed within the LAP and LIPS projects. In order to preserve confidentiality the numbers given in Table 6.4 have been anonymised and are specified with arbitrary cost units [a.u.] per surface area.

Table 6.4: *Technology cost figures*

technologies	a.u./area
MCM-D#1a, #1b	4.0
MCM-D#2	3.0
MCM-D#3, #4, #5	5.0
MCM-L#1a	3.0
MCM-L#1b, #1c, #1d, #1e, #1f	2.0
MCM-L#2a, #2b, #2c, #2d	0.5
MCM-L/D	6.0

6.3. Case Study Reference System

In this section we introduce the reference application to which the technology alternatives are benchmarked. A transceiver module for adaptive cruise control (ACC) in automotive applications will serve for the case study as it best represents a cost sensitive millimetre-wave frequency consumer product manufactured in high volumes. It operates at 76.5 ± 0.5 GHz as a frequency-modulated continuous-wave (FMCW) radar system. Examples of such systems are described in [7, 36, 123, 124] and a general overview on automotive cruise control sensors is given in [125].

6.3.1. System Components

Different transceiver architectures have been published in the literature, most of them using similar components (some even the same chip sets). Figure 6.12 shows a block diagram of the system used as the benchmark reference. It consists of three wire or ribbon bonded MMICs (voltage controlled oscillator (VCO), medium power amplifier (MPA) and mixer), 50 Ω impedance transmission lines for the 77 GHz

RF signals, passive RF components (one band pass filter (BPF) and two power splitters), a 77 GHz antenna and some IF/DC components which are not further investigated here (low pass filter (LPF), biasing and matching networks).

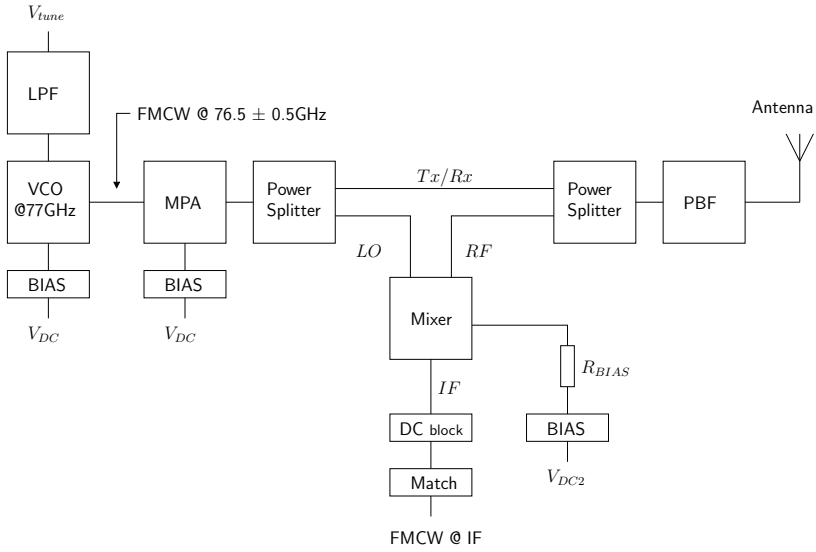


Figure 6.12: *Block diagram of 77 GHz transceiver system.*

Table 6.5 lists the important RF components and describes their implementation and specifications for the technology benchmarking.

6.3.2. System Cost Contributors

The total system costs for typical millimetre-wave transceiver modules are determined by the following cost contributors [2]:

- MMICs and external components
- packaging and assembly
- testing and tuning

The substrate technologies benchmarked here contribute to the packaging and assembly costs and have been cost calculated using the manufacturer's process and material data and dedicated cost models

Table 6.5: *Components of 77 GHz benchmark reference system*

Components	Description	Benchmark specifications
3 × MMIC	Mixer, voltage controlled oscillator (VCO), medium power amplifier (MPA),	-
transmission lines	50 Ω lines for 77 GHz RF signals	$45\Omega < Z_0 < 55\Omega$ $\alpha_{max} < 1.5$ dB/mm
power splitter	Wilkinson power divider with 100 Ω resistor	$S_{21} > -4$ dB $S_{11} < -20$ dB
band pass filter	represented with coupled microstrip lines	$C > -20$ dB $S_{11} < -20$ dB
antenna	represented with resonance frequency of microstrip component	76.5 GHz $< f_{res} <$ 77.5 GHz

[126, 127]. The relative contribution to the system cost varies as with integrated passives the substrate functionality increases and other external components may become obsolete. When comparing different technologies it is therefore important that similar functionality is provided. For the 77 GHz benchmark reference system, the critical components in that sense are the Wilkinson power divider requiring integrated resistors and the antenna with high demands on the technology to achieve the required efficiency and bandwidth.

Table 6.6: *Overview of investigated technologies*

#	label	conductor/dielectrics	carrier	size
1	MCM-D#1a	Cu/3 × 6.5μm BCB	RO4003	4”×4”
2	MCM-D#1b	Cu/3 × 6.5μm BCB	RO4003	4”×4”
3	MCM-D#2	Cu/3 × 6.5μm BCB	RO4003	12”×12”
4	MCM-D#3	Au/3 × 15μm BCB	RO4003	4”×4”
5	MCM-D#4	Au/3 × 15μm BCB	Al	4”×4”
6	MCM-D#5	Cu/3 × 15μm BCB	Si	5” wafer
7	MCM-L#1a	Cu/72μm Pyralux/Arlon 85NT	Si	5” wafer
8	MCM-L#1b	Cu/63μm Speedboard C/Espanex	Si	5” wafer
9	MCM-L#1c	Cu/63μm Speedboard C/Biac LCP	Si	5” wafer
10	MCM-L#1d	Cu/63μm Microlam 410/Espanex	Si	5” wafer
11	MCM-L#1e	Cu/63μm Microlam 410/Biac LCP	Si	5” wafer
12	MCM-L#1f	Cu/62μm Microlam 410	Si	5” wafer
13	MCM-L#2a	Cu/63μm Speedboard C/Biac LCP	RO4003	9”×12”
14	MCM-L#2b	Cu/63μm Microlam 410/Biac LCP	RO4003	9”×12”
15	MCM-L#2c	Cu/57μm Speedboard C	RO4003	9”×12”
16	MCM-L#2d	Cu/62μm Microlam 410	RO4003	9”×12”
17	MCM-L/D	Cu/3 × 15μm BCB & 63μm Speedboard C/Biac LCP	RO4003	5” wafer

6.4. Technology Benchmark Results

In this section we will analyse and discuss the benchmark results of the 17 case study technologies, using the benchmark tool developed in Chapter 4. A summary of the benchmark technologies is listed in Table 6.6 (see previous page).

6.4.1. Transmission Line Configurations

In Figure 6.13 we can see that CPW lines are of no use as the realisable impedance ranges are very limited. Either the important 50 Ω lines are not feasible or the technologies use metallic carriers thus prohibiting pure CPW lines. The resulting grounded CPW (GCPW) configurations are not recommended here as considerable effort is required to suppress the excited parallel plate modes between the coplanar and the underlying ground planes. Different via positioning techniques are investigated in [128] to avoid resonances and bulk modes in GCPW. They all cause RF structure design to become very complicated in terms of via placement and structure simulations requiring much more computing power because of the more complex 3D topologies. The realisable impedance ranges with microstrip configuration are shown in Figure 6.14.

6.4.2. Transmission Line Performance

In Figure 6.15 the microstrip parameters Z_0, f_{res} and α are lined up for all investigated technologies. We can observe interesting results for MCM-D #2 which shows large impedance variation, MCM-D #5 with the best overall performance (smallest variations and lowest losses) and MCM-L #1c as the best performing pure laminate based technology.

For further analysis we take a closer look at the OPAT sensitivity vectors of the three mentioned technologies, depicted in Figure 6.16. We see that the MCM-D #2 impedance variations are mainly caused by the line width variations, what is indeed not surprising for the large area 12" × 12" panel. The main advantage of the MCM-D #5 technology compared to the MCM-L #1c technology is the overall better process precision in terms of line width and dielectric thickness control. Problematic for the MCM-L #1c is the uncertainty about the exact dielectric material properties – the permittivity ϵ_r and the dissipation factor $\tan\delta$. This uncertainty produces important variations of the resonance frequency and the dielectric losses.

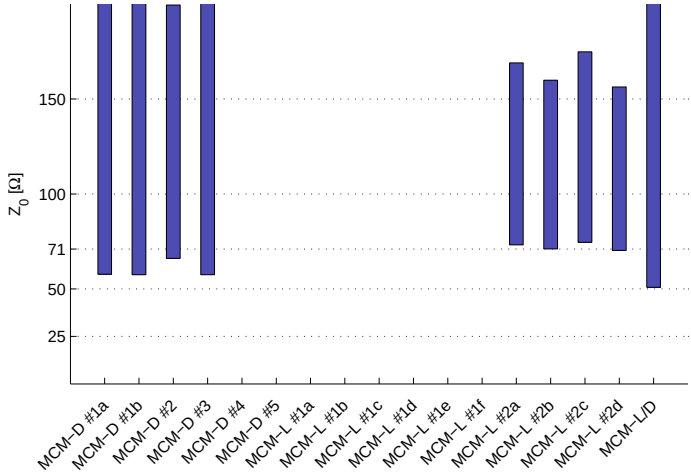


Figure 6.13: *Realisable impedance ranges for CPW configurations at 77 GHz.*

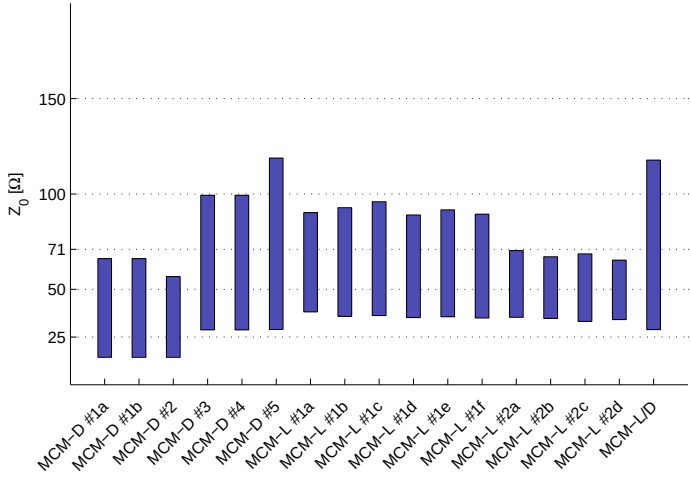


Figure 6.14: *Realisable impedance ranges for microstrip configurations at 77 GHz.*

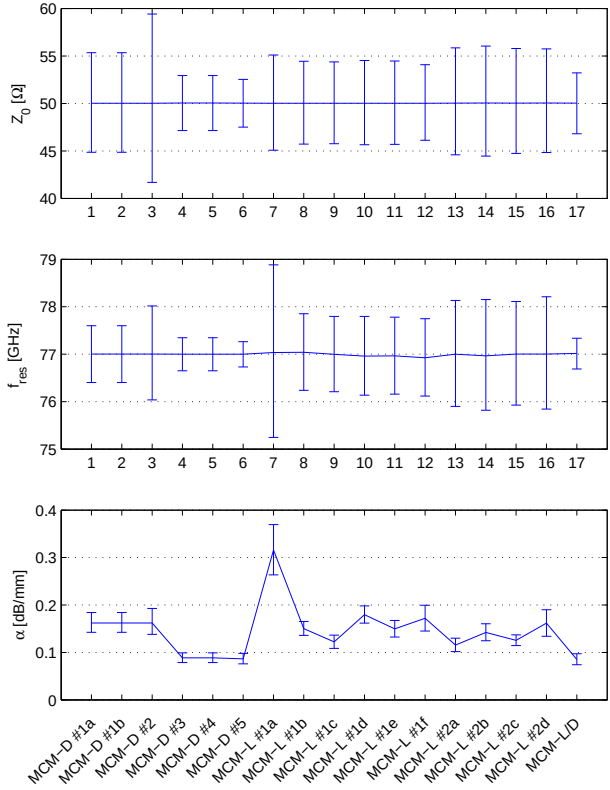
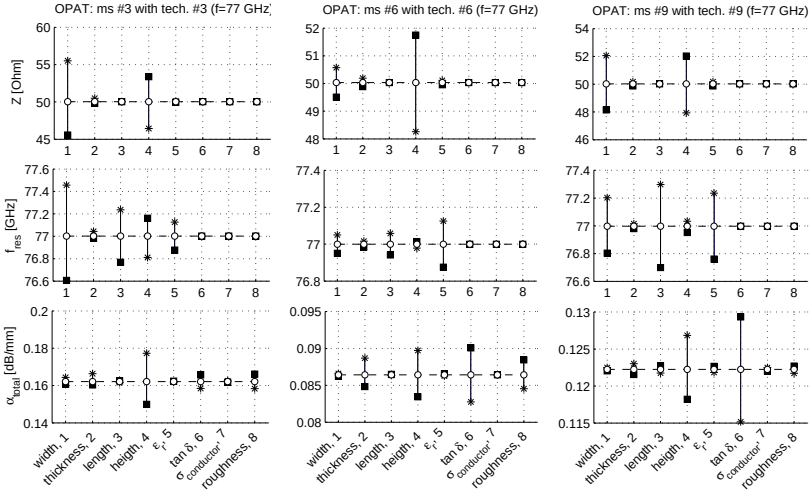


Figure 6.15: *Comparison of microstrip parameters at 77 GHz.*

No surprising results are observed with the STPAT analysis depicted in Figure 6.17, with all corresponding interaction ratios close to $I = 1.0$ (= no interaction). This linear behaviour and the symmetric interaction and sensitivity graphs allow direct calculation of the technology performance ratios assuming normal distribution of the component response parameters.

The calculated technology performance ratios P_t and yields Y for impedance and loss are listed in Table 6.7, showing the best performing technologies bold faced. In terms of transmission performance the MCM-D technologies with thick dielectric layers, the MCM-L alternatives with low loss materials and thick layers and the MCM-L/D mixed



(a) MCM-D #2 (b) MCM-D #5 (c) MCM-L #1c

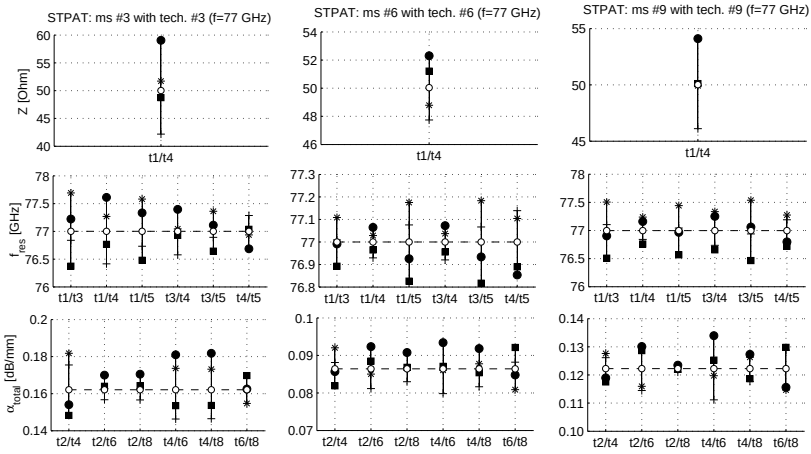
Figure 6.16: *OPAT analysis of microstrip parameters for three selected technologies. ($\circ = T_{t_i}$, $* = L_{t_i}$, $\blacksquare = U_{t_i}$)*

build up also with low loss materials and thick dielectrics come up to expectations.

6.4.3. Basic Component Performance

The basic performance of integrated passives is closely related to their equivalent transmission line parameters: The insertion losses (S_{21}) of passive components depend (among other effects) on the sum of its partial transmission line element losses. The reflection losses (S_{11}) adding up to the inevitable design conditioned reflections are caused by the impedance variations of the individual transmission line elements. Finally, the component's operation frequencies depend on the resonance frequency of the resonating transmission line sections used in the component.

Based on this, we will use the resonance frequency f_{res} of the microstrip component model to represent the reference system's integrated antenna. This simplification may appear quite risky, but the



(a) MCM-D #2 (b) MCM-D #5 (c) MCM-L #1c

Figure 6.17: *STPAT analysis of microstrip parameters for selected technologies. ($\circ = TT_{t_i}$, $\blacksquare = LL_{t_i}$, $\bullet = LU_{t_i}$, $+ = UL_{t_i}$, $* = UU_{t_i}$)*

Table 6.7: *Microstrip technology performance ratios and yields*

#	technology	$P_{tm_{Z_0}}$	$P_{tU_{loss}}$	$P_{t_{total}}$	Y_{Z_0}	Y_{loss}	Y_{total}
1	MCM-D#1a	0.9526	-0.5494	-0.5767	94.97	22.46	21.33
2	MCM-D#1b	0.9526	-0.5494	-0.5767	94.97	22.46	21.33
3	MCM-D#2	0.5547	-0.3969	-0.7155	55.31	30.06	16.63
4	**MCM-D#3**	**1.7239**	**5.8621**	**1.7239**	**100**	**100**	**100**
5	**MCM-D#4**	**1.7239**	**5.8621**	**1.7239**	**100**	**100**	**100**
6	**MCM-D#5**	**1.9894**	**5.4506**	**1.9894**	**100**	**100**	**100**
7	MCM-L#1a	0.9962	-3.1088	-3.1207	99.32	0	0
8	MCM-L#1b	1.1451	-0.0159	-0.0159	100	49.05	49.05
9	**MCM-L#1c**	**1.1604**	**1.9389**	**1.1604**	**100**	**100**	**100**
10	MCM-L#1d	1.1244	-1.5861	-1.5861	100	0	0
11	MCM-L#1e	1.1390	0.0170	0.0170	100	50.70	50.70
12	MCM-L#1f	1.2535	-0.8052	-0.8052	100	9.709	9.709
13	**MCM-L#2a**	**0.8819**	**2.3817**	**0.8819**	**87.92**	**100**	**87.92**
14	**MCM-L#2b**	**0.8561**	**0.4302**	**0.3683**	**85.35**	**71.30**	**60.85**
15	**MCM-L#2c**	**0.8960**	**2.1174**	**0.8960**	**89.33**	**100**	**89.33**
16	MCM-L#2d	0.9055	-0.4174	-0.4610	90.28	29.04	26.22
17	**MCM-L/D**	**1.5604**	**5.3660**	**1.5604**	**100**	**100**	**100**

frequency offset obtained from the microstrip line variations correspond precisely to the frequency shift of a microstrip patch antenna.

Table 6.8 adds the performance ratios and yields of the resonance frequency f_{res} to the previously computed ratios for the impedance and losses. The results show that the thick conductors and the poor line width accuracy of the MCM-L technologies drastically reduce their performance. MCM-L #1c is again marked (bold faced) as best performing laminate based technology but with unacceptable performance and yield values.

Table 6.8: *Microstrip equivalent performance ratios and yields*

#	technology	$P_{tm_{f_{res}}}$	$P_{t_{total}}$	$Y_{f_{res}}$	Y_{total}
1	MCM-D#1a	0.8357	-0.6901	83.32	17.78
2	MCM-D#1b	0.8357	-0.6901	83.32	17.78
3	MCM-D#2	0.5033	-1.4216	50.18	8.342
4	**MCM-D#3**	**1.4352**	**1.4352**	**100**	**100**
5	**MCM-D#4**	**1.4352**	**1.4352**	**100**	**100**
6	**MCM-D#5**	**1.8731**	**1.8731**	**100**	**100**
7	MCM-L#1a	0.2736	-11.406	27.28	0
8	MCM-L#1b	0.6106	-0.0260	60.87	29.86
9	**MCM-L#1c**	**0.6301**	**0.6301**	**62.82**	**62.82**
10	MCM-L#1d	0.5989	-2.6480	59.71	0
11	MCM-L#1e	0.6118	0.0104	60.99	30.92
12	MCM-L#1f	0.5963	-1.3503	59.45	5.772
13	MCM-L#2a	0.4472	0.3944	44.59	39.20
14	MCM-L#2b	0.4284	0.1578	42.71	25.99
15	MCM-L#2c	0.4572	0.4096	45.58	40.72
16	MCM-L#2d	0.4217	-1.0932	42.04	11.02
17	**MCM-L/D**	**1.5322**	**1.5322**	**100**	**100**

6.4.4. Wilkinson Power Divider

We know from Chapter 4 that the Wilkinson power divider circuit contains a 100 Ω shunt resistor for output port isolation. Only the technologies MCM-D #3 – #5 and MCM-L/D were developed with dedicated resistive layers for resistor integration, but as already mentioned in the technology introduction section, we will also benchmark the technologies MCM-L #1a – #1f with the supposed possibility of integrated resistors. In Figure 6.18 we see the component response parameters Z_{qw}, R_{shunt}, S_{11} and S_{21} lined up for performance comparison (for those technologies without resistive layer the graphs are left blank).

In this comparison line up we pick out three technologies and perform further analysis using the OPAT sensitivity chart (see Fig-

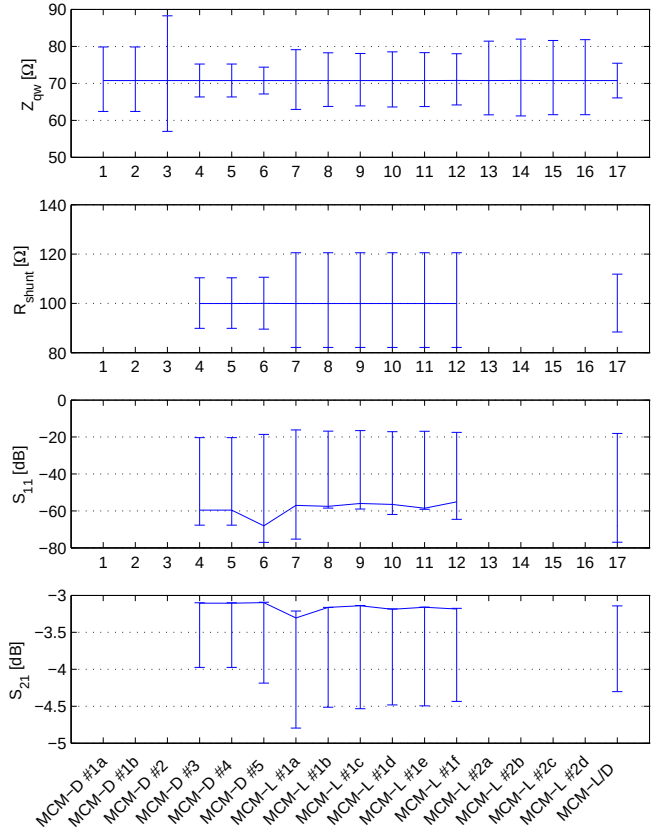
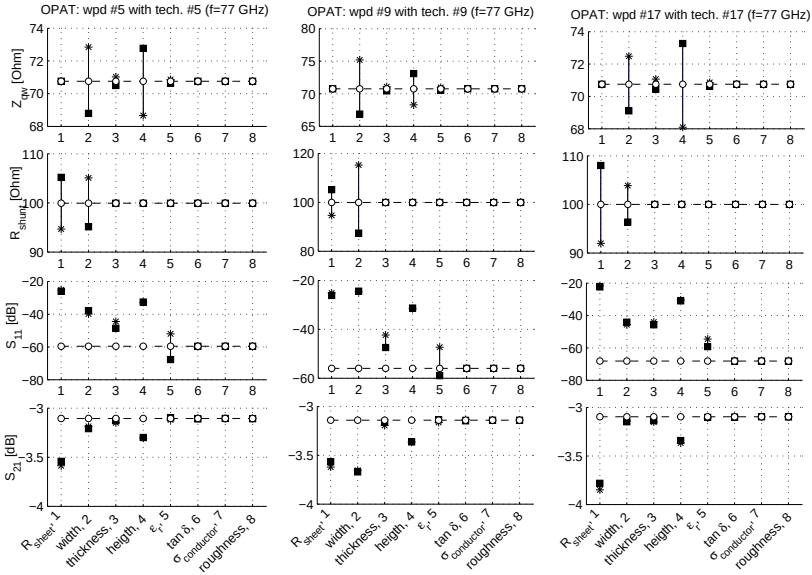


Figure 6.18: *Comparison of Wilkinson power divider parameters at 77 GHz.*

ure 6.19): MCM-D #4 shows (together with MCM-D #3) the best input match S_{11}, MCM-L #1c is the best performing laminate based technology and the mixed build-up MCM-L/D is chosen as generally interesting technology. In the parameter sensitivity charts we see that the sheet resistance R_{sheet} of the resistive layers has the largest influence on the input reflection S_{11} and the total transmission losses S_{21} (together with the structure width accuracy on MCM-L #1c).

However, from the asymmetric OPAT charts in Figure 6.19 we can tell that the parameter variations for S_{11} and S_{21} are unlikely to be



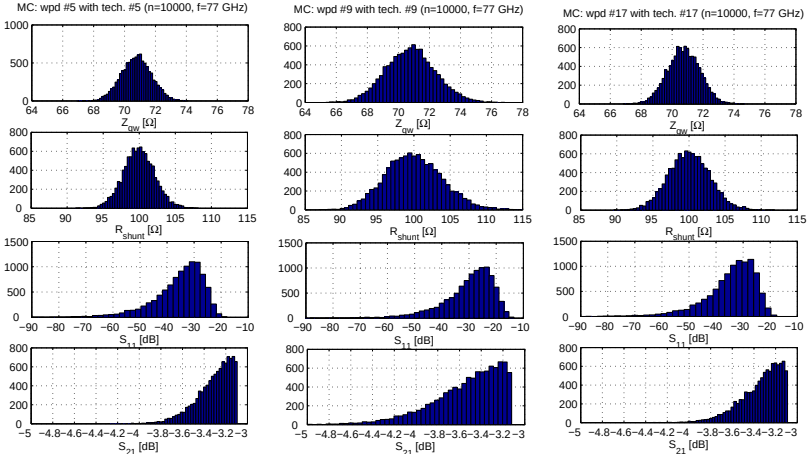
(a) MCM-D #4 (b) MCM-L #1c (c) MCM-L/D

Figure 6.19: *OPAT analysis of Wilkinson power divider parameter for three selected technologies. ($\circ = T_{t_i}$, $* = L_{t_i}$, $\blacksquare = U_{t_i}$)*

normally distributed. To determine the exact distributions for the ten remaining technologies, we have performed Monte Carlo simulations. In Figure 6.20 the response parameter distributions after 10'000 simulations each are shown for the three technologies selected above. S_{11} exhibits a log-normal like distribution while S_{21} appears as a half-sided normal distribution.

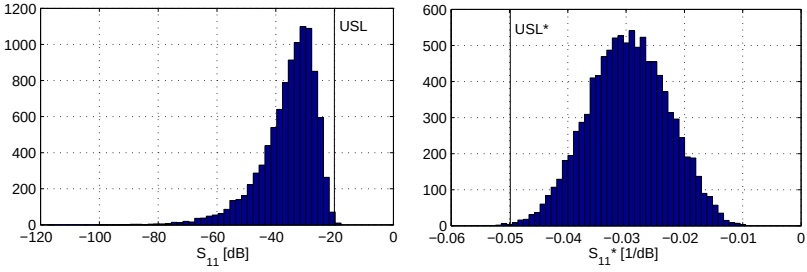
The Monte Carlo simulation data are further used to calculate the individual parameter performance ratios $P_{t_{S_{11}}}$ and $P_{t_{S_{21}}}$ and yields $Y_{S_{11}}$ and $Y_{S_{21}}$. The distribution of S_{11} is predestined for the reciprocal transformation presented in Chapter 3. Figure 6.21 shows the result of the $S_{11}^* = 1/S_{11}$ transformation, with $USL = -20$ dB becoming $USL^* = -0.05$ dB[1].

[1]Through reciprocal transformation upper specification limits are becoming lower specification limits and vice versa.



(a) MCM-D #4 (b) MCM-L #1c (c) MCM-L/D

Figure 6.20: *Monte Carlo analysis of Wilkinson power divider parameter for three selected technologies.*



(a) non-normal (b) transformed

Figure 6.21: *Reciprocal transformation of non-normal S_{11} distribution for MCM-D #4 technology.*

The distribution of S_{21} does not allow such a transformation; however its half-sided normal appearance allows easy handling of the Monte Carlo simulation data. We must therefore determine the upper 99.73% of the simulation data to specify the distorted 6σ data range. Then we use the S_{21} distribution peak near the top end of the curve to replace the distribution mean μ. With these two values we get much more realistic performance ratios.

The performance ratios and yields of the specified Wilkinson power divider parameter are both listed in Table 6.9. Although the three MCM-D technologies have performance ratios larger than 1, the yields are slightly below 100%. The MCM-L/D technology also reaches a quite acceptable yield ($Y = 93.57\%$) but all MCM-L technologies are clearly dissociated. MCM-L #1c is again highlighted (bold faced) as the best performing MCM-L technology.

Table 6.9: *Wilkinson power divider performance ratios and yields*

#	technology	$P_{tU_{S_{11}}}$	$P_{tL_{S_{21}}}$	$P_{t_{total}}$	$Y_{S_{11}}$	$Y_{S_{21}}$	Y_{total}
1	MCM-D#1a	n/a	n/a	n/a	n/a	n/a	n/a
2	MCM-D#1b	n/a	n/a	n/a	n/a	n/a	n/a
3	MCM-D#2	n/a	n/a	n/a	n/a	n/a	n/a
4	**MCM-D#3**	**1.0018**	**1.1469**	**1.0018**	**99.79**	**99.88**	**99.67**
5	**MCM-D#4**	**0.9913**	**1.1041**	**0.9913**	**99.26**	**99.87**	**99.13**
6	**MCM-D#5**	**0.9850**	**1.0921**	**0.9850**	**98.95**	**99.88**	**98.83**
7	MCM-L#1a	0.4633	0.3970	0.1839	72.95	81.55	59.49
8	MCM-L#1b	0.4694	0.4941	0.2319	73.25	88.54	65.86
9	**MCM-L#1c**	**0.4837**	**0.5018**	**0.2427**	**73.96**	**90.47**	**66.91**
10	MCM-L#1d	0.4437	0.4579	0.2032	71.97	86.49	62.25
11	MCM-L#1e	0.4599	0.4696	0.2160	72.78	88.37	64.32
12	MCM-L#1f	0.4532	0.4581	0.2076	72.44	87.01	63.03
13	MCM-L#2a	n/a	n/a	n/a	n/a	n/a	n/a
14	MCM-L#2b	n/a	n/a	n/a	n/a	n/a	n/a
15	MCM-L#2c	n/a	n/a	n/a	n/a	n/a	n/a
16	MCM-L#2d	n/a	n/a	n/a	n/a	n/a	n/a
17	**MCM-L/D**	**0.8848**	**0.9521**	**0.8424**	**93.96**	**99.58**	**93.57**

6.4.5. Coupled Lines Parameters

Coupled lines are used here as representative elements for the case study system's band pass filter, implemented as a coupled microstrip filter. The most critical parameter here is the space between the two coupled lines, where small minimum space means high maximum coupling. Figure 6.22 shows for each technology the largest possible coupling coeffi-

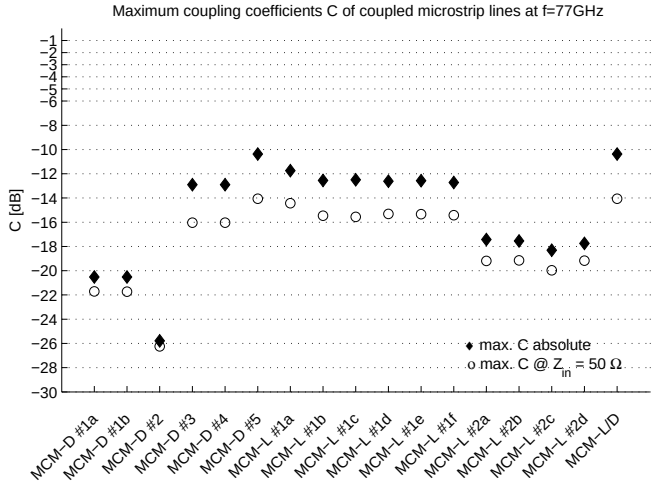
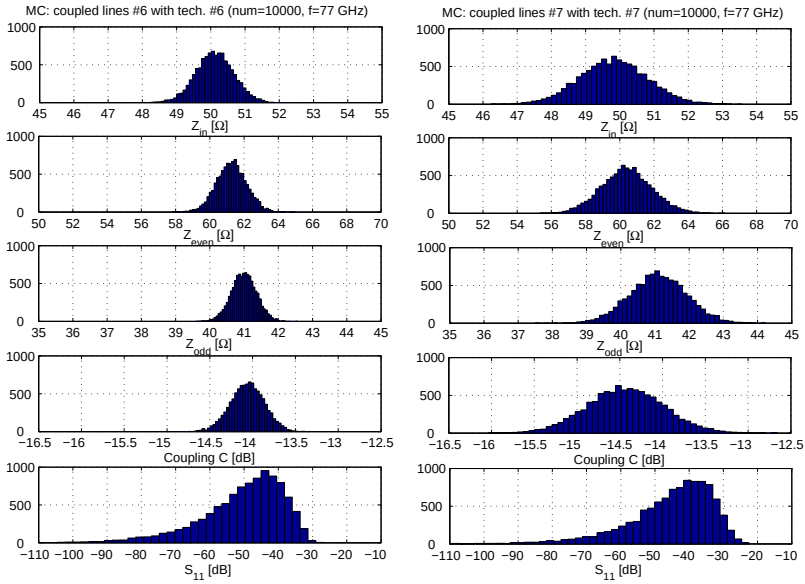


Figure 6.22: *Maximum coupling coefficients at 77 GHz.*

cients C. The absolute C value is the upper limit with no restrictions while C @ $Z_{in} = 50\ \Omega$ is limited through the constraint of providing 50 Ω matched input impedance.

In Figure 6.22 we notice that the MCM-L #1a technology provides a surprisingly high coupling coefficient, outperformed only by MCM-D #5 and MCM-L/D. The reason for this is the thicker dielectric ($d = 72\mu$m) of the Pyralux/Arlon build-up compared to the other MCM-L #1 technologies ($d = 63\mu$m and $d = 62\mu$m). This apparent high performance gets relativised when we compare the parameter distributions obtained with the Monte Carlo simulations depicted in Figure 6.23. The graphs clearly show that the variations of the even and odd mode impedances are much larger for the MCM-L #1a than for the MCM-D #5 technology. This in consequence strongly affects the variation of the coupling coefficient C.

The S_{11} parameter variation of the coupled lines component shows the same non-normal distribution as observed earlier for the Wilkinson power divider (Figure 6.23). Hence, the reciprocal transformation can also be applied here to get a normal distribution and thus to compute the technologies' performance ratios and yields. The transformed distributions for the two technologies MCM-D #5 and MCM-L #1a discussed above are shown in Figure 6.24.



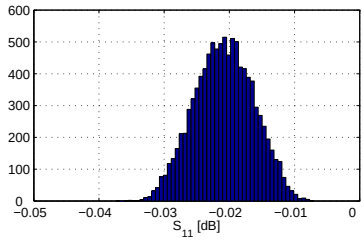
(a) MCM-D #5 (b) MCM-L #1a

Figure 6.23: *Comparison of Monte Carlo analysis of coupled microstrip line parameters for a thin film (a) and a laminate based (b) technology.*

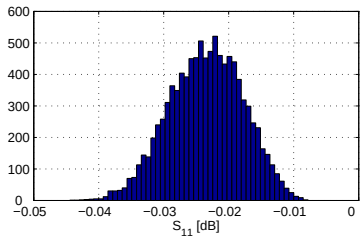
All performance ratios and yields for the specified coupled microstrip line response parameters are listed in Table 6.10. Now we can clearly see the difference between the MCM-D technologies #3 – #5 with performance ratios $P_t > 2$ and the MCM-L #1a technology, which in the beginning appeared quite promising, with $P_t = 1.5643$. In this case the thin film based technologies take advantage of their much smaller parameter variations.

6.4.6. Benchmark Result Discussion

If we look at the performance and yield tables computed for the individual components (Tables 6.7–6.10), the technologies MCM-D #1a, #1b and #2 are rapidly disqualified. Their poor results prove that thin



(a) MCM-D #5



(b) MCM-L #1a

Figure 6.24: *Reciprocal transformation of non-normal S_{11} distribution for two selected technologies.*

Table 6.10: *Coupled lines performance ratios and yields*

#	technology	$P_{tU_{S_{11}}}$	P_{tL_C}	$P_{t_{total}}$	$Y_{S_{11}}$	Y_C	Y_{total}
1	MCM-D#1a	1.3894	-1.2555	-1.2555	100	0	0
2	MCM-D#1b	1.4144	-1.2446	-1.2446	100	0	0
3	MCM-D#2	0.9272	-3.2218	-3.2218	99.07	0	0
4	**MCM-D#3**	**2.0211**	**5.0209**	**2.0211**	**100**	**100**	**100**
5	**MCM-D#4**	**2.0319**	**5.0874**	**2.0319**	**100**	**100**	**100**
6	**MCM-D#5**	**2.1516**	**10.021**	**2.1516**	**100**	**100**	**100**
7	**MCM-L#1a**	**1.5643**	**4.1228**	**1.5643**	**100**	**100**	**100**
8	**MCM-L#1b**	**1.6038**	**3.2746**	**1.6038**	**100**	**100**	**100**
9	**MCM-L#1c**	**1.5899**	**3.1984**	**1.5899**	**100**	**100**	**100**
10	**MCM-L#1d**	**1.6064**	**3.3425**	**1.6064**	**100**	**100**	**100**
11	**MCM-L#1e**	**1.3386**	**3.3177**	**1.3386**	**100**	**100**	**100**
12	**MCM-L#1f**	**1.6466**	**3.3497**	**1.6466**	**100**	**100**	**100**
13	MCM-L#2a	1.3021	0.5119	0.5119	100	75.37	75.37
14	MCM-L#2b	1.3226	0.5342	0.5342	100	76.48	76.48
15	MCM-L#2c	1.2558	0.0332	0.0332	100	51.51	51.51
16	MCM-L#2d	1.2467	0.5333	0.5333	100	76.44	76.44
17	**MCM-L/D**	**1.8909**	**7.3216**	**1.8909**	**100**	**100**	**100**

dielectric layers are a big disadvantage at millimetre-wave frequencies. The remaining technologies are lined up in the Figures 6.25 and 6.26 summarising all individual component performance ratios and yields. Best performing in all disciplines are the thin film technologies including the mixed MCM-L/D build-up. This is mainly a result of the high precision of conductor structure definition and the increased dielectric thickness which almost reaches the thickness of laminate technologies.

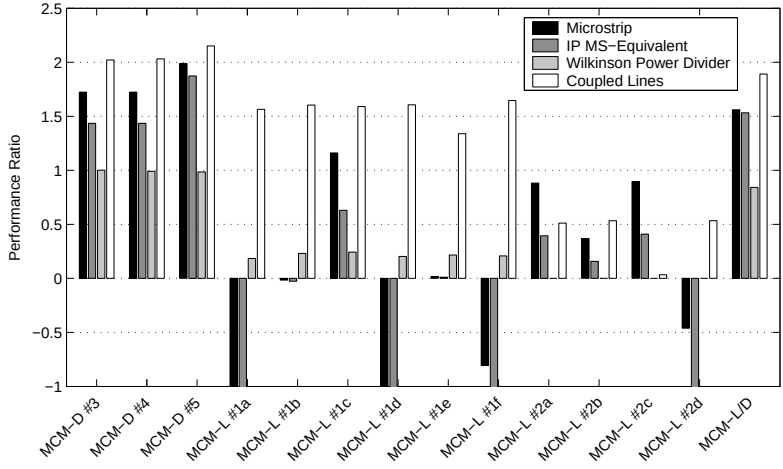


Figure 6.25: *Line up of all individual performance ratios for the investigated technologies (without MCM-D #1a, #1b and #2).*

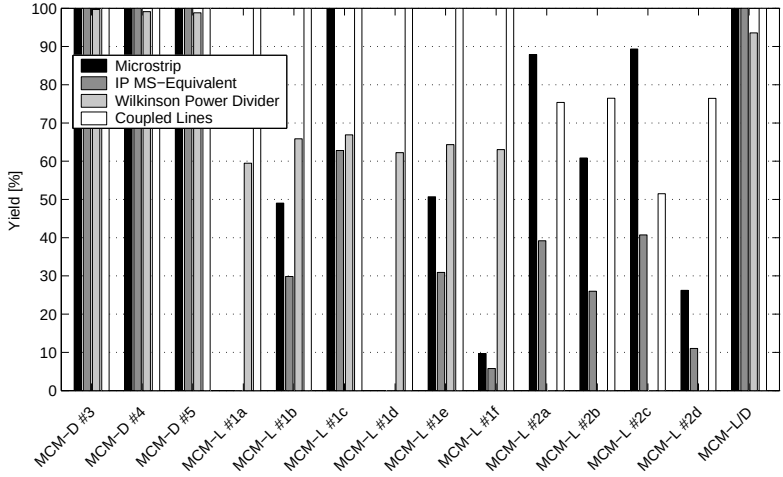


Figure 6.26: *Line up of all individual component yields for the investigated technologies (without MCM-D #1a, #1b and #2).*

In order to get a differentiated technology comparison the benchmark results will be evaluated in three steps. First, we only compare the transmission performances using the microstrip component performance results. Then, as some technologies do not provide integrated resistors, the Wilkinson power divider is omitted for the second step. For the third step, we finally combine the performance ratios of all benchmark components as described in Chapter 3. The resulting total performance ratio is valid for the generic component representation of our benchmark reference application. Figure 6.27 shows the resulting three pareto graphs computed using the cost data specified in Table 6.4.

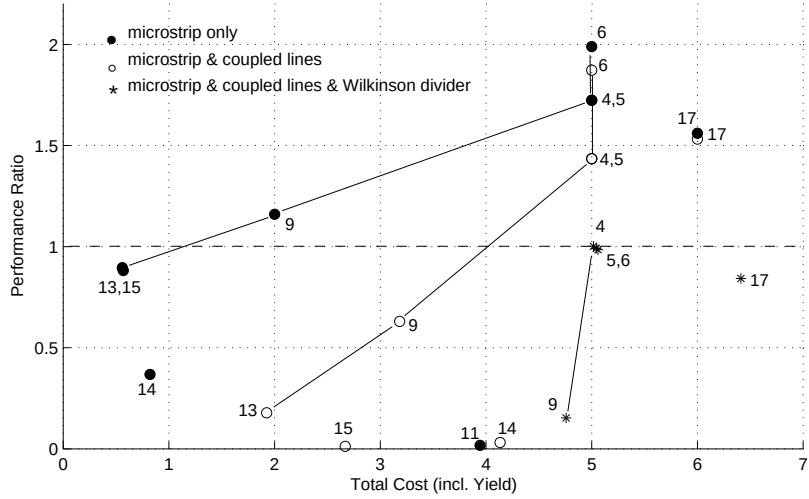


Figure 6.27: *Pareto graphs for the three benchmark steps.*

The pareto fronts show that for pure interconnect purposes the thin film technologies overshoot the performance demands at high costs. MCM-L #1c (no. 9) also reaches 100% yield with a comfortable performance ratio of $P_{t_{total}} = 1.1604$ but at much lower costs.

Introducing the coupled microstrip lines disqualifies all laminate technologies. Both yield and performance ratios drop below the 6σ limit. But the pareto front shows that despite the much lower yield, the technology MCM-L #1c (no. 9) is still less expensive than the thin film solutions. However, if we consider that this technology is very unstable in terms of performance ratio ($P_{t_{total}} = 0.6301$), the low costs become illusive and represent a higher risk. Here the thin film technologies are

the better choice. Among each other they are still separated by their total performance ratios.

The Wilkinson power divider finally reduces the choice of alternatives to only 3 remaining technologies. The three MCM-D technologies (no. 4, 5 and 6) still provide yields and performance ratios in the 6σ region but slightly below the limit. All laminate technologies have dropped in performance and yield and even the MCM-L/D technology (no. 17) exhibits considerable yield losses, thus becoming even more expensive. If we take a look back at its OPAT sensitivity chart in Figure 6.19, the reason for the low performance of MCM-L/D becomes clear. The variations of the total dielectric thickness and the sheet resistance strongly affect Z_{qw} and R_{shunt} and therefore both S_{11} and S_{21} are deteriorated. With this we can identify the deposition of the resistor film and the thickness control of the dielectric layers as the sensitive process parameters for effective technology enhancement.

For the 77 GHz reference transceiver module the benchmark results have several consequences. If we aim at a single substrate solution with all RF passives integrated, only the enhanced thin film technologies are to be considered. If we envisage to use laminate based technologies the antenna must be externally connected and the Wilkinson power dividers replaced by other passive components (which do not need integrated resistors) or included as external components. In that case the MCM-L #1c technology also becomes a feasible alternative but with the additional costs of external components.

6.5. Summary

A large variety of high density technology alternatives was presented and analysed for its use at millimetre-wave frequencies. Seventeen different alternatives were then proposed and compared based on technology parameters gained from test vehicle measurements and manufacturer data. The comparison was conducted as a case study using the benchmark tool presented in Chapter 4 and a 77 GHz transceiver module serving as the benchmark reference system. The concept of the technology performance measures was successfully used to provide a *quantitative* ranking of the proposed alternatives. In one example (MCM-L/D) the two most sensitive process parameters in terms of RF performance were identified thus reflecting a typical benefit of the presented technology benchmarking and analysis method.

7

Conclusions

Attracted by the emerging high volume consumer applications operating in the millimetre-wave frequency range (see Chapter 1), more and more technology manufacturers want to enter these markets by offering suitable packaging solutions. High density substrates based on high frequency materials and capable of providing high accuracy structure definition seem predestinated for that purpose. However, at millimetre-wave frequencies different rules reign and other technology constraints apply. Chapter 2 has reviewed these constraints and set the background for the novel results and achievements presented in this thesis.

7.1. Achievements

The main objectives of this thesis were motivated by the market prognoses demanding for high volume and low cost manufacturability and the requirements of millimetre-wave technologies. This section summarises the achievements as the outcome of the three main objectives formulated in the introduction of this work.

7.1.1. Benchmark Methodology

Objective I: *"To provide a technology RF performance metric and benchmark tool allowing for quantitative comparison of technology alternatives."*

The interface between technology manufacturers and RF designers was identified as a critical path during realisation of millimetre-wave systems. Chapter 3 introduces the *system realisation path* in order to specify clearly the relation between the technology alternatives and the system behaviour and to fully account for process variations and their impact on system performance. Its key elements are the *technology model* and the definitions for describing the relation between the process parameters **p**, the technology parameters **t**, the component parameters **c** and the component responses **r**.

Based on the technology and component models the *benchmark model* was derived to further define the methodology for quantitative performance analysis. The method consists of dedicated analysis tools such as the OPAT and STPAT sensitivity vectors and a set of technology capability and performance measures C_t and P_t. The issues of *non-normal* parameter variation distributions and *correlated* parameters were addressed and solutions presented.

The *benchmark tool* was then implemented as a set of Matlab® functions for analysis and comparison of substrate technologies. The tool is based on *generic* RF components used to represent a benchmark reference application. The advantage of using generic components is to be able to compare technology alternatives with no need for complete RF system designs. Component models for *microstrip lines*, *CPW lines*, *resistors*, *capacitors*, *Wilkinson power dividers* and *coupled microstrip lines* have been implemented.

7.1.2. Technology Characterisation

Objective II: *"To design test vehicles and methods capable of measuring the technology parameters responsible for the RF performance."*

First, a new method was presented for describing technology parameter variations in the *spatial frequency domain* thus preserving the local distribution of performance and yield losses. Examples were discussed to illustrate the *spatial frequency bands* and to demonstrate their benefits. In order to measure technology parameters including spatial

information of their variations, dedicated test structures are required. A *test vehicles* for technology characterisation is therefore developed in Chapter 5, providing test structures optimised for that purpose. The corresponding test and measurement techniques and different methods to extract spatial informations are described.

To keep the achieved performance of a technology on a constant level throughout the production, monitoring and control methods are mandatory. A novel, *zone based process monitoring* method was therefore developed for minimising area consumption while maximising panel coverage.

7.1.3. Technology Benchmarking

Objective III: *"To investigate today's high density substrate technologies and to compare their suitability for RF applications using the previously mentioned test methods and benchmark tools."*

Alternatives for high density substrates, based on thin film and laminate technologies were presented. The analysed options propose several processing methods for material deposition and definition. Considerations were made in terms of *materials*, *topologies* and *quality* and for use as *conductor*, *dielectric* or *special purpose* layers.

In the frame of a case study, *17 technology alternatives* were proposed and compared to each other using a 77 GHz transceiver module as reference application. The proposed alternatives cover a broad range of thin film, laminate and thin film on laminate technologies which were developed and characterised in the frame of the EU research projects LAP and LIPS. The *77 GHz reference system* used is a transceiver module for adaptive cruise control (ACC) in automotive systems and represents a typical cost sensitive, high volume application.

The benchmark tool introduced in Chapter 4 was used to benchmark the technology alternatives. The reference system was therefore described using generic RF component models for microstrip lines, Wilkinson power dividers and coupled microstrip lines. The benchmark analysis and comparison functions and the technology performance ratios exposed the advantages and drawbacks of each technology and permitted the rapid generation of quantitative performance rankings.

7.2. Conclusions

The results of the case study have shown that the performance metric, the benchmark tool and the technology characterisation test vehicles provide the expected benefits and therefore achieve the objectives. As an important outcome of the technology benchmarking, several factors have been identified as being relevant to achieve high RF performance. The absolute upper limits of achievable RF performance are generally defined by the *intrinsic material properties*, the *metallisation type* and the *thickness of the dielectric layers*. These are performance parameters which must be chosen and fixed during technology development. In order to get as close as possible to these upper performance limits the following two conditions are imperative:

1. The technologies must provide fine design rules to realise a wide range of impedances and therefore to enable the integration of required passive components.

2. Technology parameter variations must be minimised in order to get high yields, even at very fine design rules.

If either of these conditions is not fulfilled, the best materials and optimised topologies are useless. RF designers will not be able to reach the component specifications or the manufacturing costs will increase as a result of low design yield.

7.3. Outlook

Possible improvements regarding the acquisition of technology parameters and the implementation of the benchmark tool are proposed and an outlook to future work on technology comparison is given.

7.3.1. Technology Data Acquisition

The technology data acquisition path used during this work was a cumbersome procedure of measurement, extraction, interpretation and data typing. This acquisition path can easily be accelerated as all modern measurement and test equipment provide software interfaces to all kinds of data formats. When connected to the automated in-line or in-situ test equipment even more parameters such as temperature, time, equipment and shift identification and process parameters could be included. This would extend the benchmark model to also consider

process parameters **p** thus modelling the entire *system realisation path* presented in Chapter 3 and allow description of the RF component responses **r** as functions of process parameters **p**:

$$\mathbf{r} = \mathcal{M}_{benchmark}(\mathbf{p}) = \mathcal{M}_{component}\Big(\mathcal{M}_{technology}\big(\mathcal{M}_{process}(\mathbf{p})\big)\Big)$$

7.3.2. Benchmark Tool Implementation

The current implementation of the technology benchmark tool leaves many options for further improvements. In a short term a more friendly user interface is necessary to keep better overview of the many technology and component parameters accruing when 17 technologies are compared. For higher flexibility and more precise representation of the benchmark reference applications more generic RF component models may be included. In a longer term, the technology benchmark tool could also be offered as plug-in solution for existing RF design tools.

7.3.3. Technology Alternatives

Besides the 17 technologies compared in Chapter 6, many other alternatives exist today in terms of material selection, metallisation types and layer topologies. The comparisons could therefore be extended to technologies such as HTCC and LTCC but also mixed substrate technologies. Furthermore, the use of high volume statistical technology data gathered from actual production manufacturing lines could be considered and compared to results based on estimated parameters.

Glossary

Scalars

AC	Area consumption of process monitors
A_{plate}	Plate capacitor area
A_{res}	Resistor area
C	Capacitance / coupling coefficient / cost
C_{R_q}	Surface roughness loss correction coefficient
C_{tL}	One-sided technology capability ratio with lower limit
C_{tU}	One-sided technology capability ratio with upper limit
C_{tm}	Technology capability ratio
K	Mutual parameter correlation factor
LSL	Lower specification limit
L_{t_i}	Lower parameter variation value
PM	Number of process monitors per panel
PW	Absolute width of process monitor line
P_{tL}	One-sided technology performance ratio with lower limit
P_{tU}	One-sided technology performance ratio with upper limit
P_{tm}	Technology performance ratio
R_q	Surface roughness (RMS)
R_s	Surface resistance
R_{DC}	DC resistance
R_{sheet}	Sheet resistance
R_{shunt}	Shunt resistor
R_{via}	Single via resistance
S	Number of substrates along one panel side
T_{t_i}	Parameter target value
USL	Upper specification limit
U_{t_i}	Upper parameter variation value
$\bar{X}$	Sample mean value

Y	Yield
Z_0	Characteristic impedance
Z_{even}	Even mode impedance
Z_{in}	Input impedance
Z_{odd}	Odd mode impedance
Z_{qw}	Quarter wavelength section impedance
Δ_w	Meander line width difference
α	Total insertion losses
α_c	Conductor losses
α_d	Dielectric losses
α_r	Surface roughness losses
γ	Angle of conductor side walls
δ	Skin depth
ϵ_0	Free space permittivity ($= 8.85419 \cdot 10^{-12}$ F/m)
ϵ_r	Relative dielectric permittivity
$\epsilon_{r_{eff}}$	Effective relative dielectric permittivity
λ	Wavelength
λ_v	Spatial variation wavelength
$\lambda_{feature}$	Feature dimensions
λ_{system}	System dimensions
μ	Distribution mean value
μ_0	Free space permeability ($= 1.25663 \cdot 10^{-6}$ H/m)
μ_r	Relative permeability
σ	Metal conductivity
σ	Standard deviation
ω	Angular frequency
a_{min}	Minimum via landing pad diameter
$a.u.$	Arbitrary cost unit
c_0	Light speed ($= 2.99792 \cdot 10^8$ m/s)
c_i	Component parameter
f	Frequency
f_v	Spatial variation frequency
g	Slope of conductor side walls
h	Dielectric layer thickness

l	Transmission line length
l_{layout}	Transmission line length as specified in layout
l_{real}	Actual length of processed transmission line
l_{res}	Resistor length
l_{ts}	Length of test structures
p_i	Process parameter
p_{min}	Minimum via pitch
r_i	Response parameter
s	Line spaces / sample standard deviation
s_{min}	Minimum line spaces
t	Metal thickness
t_i	Technology parameter
u	Metal undercut
v_p	Propagation velocity
v_{min}	Smallest via diameter
w	Transmission line width
w_{layout}	Transmission line width as specified in layout
w_{min}	Minimum line width
w_{eq}	Extended equivalent line width
w_{ext}	Line width extension
w_{real}	Actual width of processed transmission line
w_{res}	Resistor width

Vectors

$\mathbf{cr}$	Variation contribution vector
$\mathbf{c}$	Component parameter vector
$\mathbf{p}$	Process parameter vector
$\mathbf{r}$	Response parameter vector
$\mathbf{r}'$	Sensitivity vector
$\mathbf{r}''$	Two-parameter sensitivity vector
$\mathbf{t}$	Technology parameter vector

Abbreviations

3D	3 Dimensional
ACC	Adaptive Cruise Control
AFM	Atomic Force Microscope
Ag	Silver
Al	Aluminium
Au	Gold
BCB	Benzocyclobutene
BPF	Band Pass Filter
CL	Coupled Lines
CPW	Coplanar Waveguide
CTE	Coefficient of Thermal Expansion
Cr	Chromium
Cu	Copper
DC	Direct Current
DOE	Design Of Experiment
DOP	Degree Of Planarisation
FC	Flip Chip
FEM	Finite Element Modelling
FPD	Flat Panel Display
FR4	Fire Retardant, Class 4
GCPW	Grounded Coplanar Waveguide
GaAs	Gallium Arsenide
HDP	High Density Packaging
HFSS	High Frequency Structure Simulator
HPA	High Power Amplifier
HTCC	High Temperature Co-fired Ceramics
IC	Integrated Circuit
IF	Intermediate Frequency
IP	Integrated Passives
ISO	International Organization for Standardization
LAP	Large Area Processing
LCP	Liquid Crystalline Polymere
LMDS	Local Multipoint Distributed Systems

LNA	Low Noise Amplifier
LPF	Low Pass Filter
LSL	Lower Specification Limits
LTCC	Low Temperature Co-fired Ceramics
MC	Monte Carlo
MCM	Multi Chip Module
MM	Millimetre-Wave
MMIC	Monolithic Microwave Integrated Circuit
MPA	Medium Power Amplifier
MVDS	Microwave Video Distribution System
MoM	Method of Moments
NIST	National Institute of Standards and Technology
Ni	Nickel
OPAT	One Parameter at a Time
PBO	Polybenzoxazole
PCB/PWB	Printed Circuit Board/Printed Wiring Board
PI	Polyimide
ppm	Parts per million ($= 10^{-6}$)
RF	Radio Frequency
RFTV	Radio Frequency Test Vehicle
RMS	Root-Mean-Square
SBU	Sequential Build-Up
SEM	Scanning Electron Microscope
SFD	Spatial Frequency Description
SMD	Surface Mount Devices
SOC	System-on-a-Chip
SOP/SIP	System-on/in-a-Package
SPC	Statistical Process Control
STPAT	Selective Two Parameter at a Time
Si	Silicon
TAB	Tape Automated Bonding
TCTV	Technology Characterisation Test Vehicle
TDR	Time Domain Reflectometry
TV	Test Vehicle

Ti	Titanium
USL	Upper Specification Limits
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyser
W	Tungsten
WB	Wire Bonding
WPD	Wilkinson Power Divider

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Curriculum Vitae

Personal Information

Didier Cottet
Born February 22, 1971
Zurich, Switzerland
Citizen of Bossonnens FR, Switzerland

Education

1998–2003:	Ph.D. student at Swiss Federal Institute of Technology (ETH) Zurich
1991–1997:	M.S. (Dipl. El.-Ing. ETH) in Electrical Engineering at Swiss Federal Institute of Technology (ETH) Zurich
1986–1990:	Mathematisch-Naturwissenschaftliches Gymnasium Rämibühl, Zurich, Switzerland
1978–1986:	Primary and secondary school in Adliswil ZH, Switzerland

Work

1998–2003:	Teaching and research assistant, Electronics Laboratory, ETH Zurich
2002:	Internship at HiDEC, Fayetteville, AR, USA: Thin film processing
1995:	Internship at Faselec AG, Zurich, Switzerland: Analogue-IC test software design