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Large-Area Photosensing in CMOS

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And there's blue sky breaking
Through the edge of the night
I can see the light
Oh, I can feel the light

(Mike Oldfield)

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ABSTRACT

The demand for highly developed photosensors to replace and automate information sensing and processing of the human eye is steadily increasing in every domain of modern life. Beside classical imaging, the wide range of applications with large photosensing area is continuously expanding and numerous specific applications are becoming more and more important, e.g. optical spectrometry applications such as environmental control. Photodetectors in CMOS technology with on-chip analog and digital signal processing circuitry provide high functionality and offer cost efficient miniaturized system-on-a-chip solutions.
In this work large-area photosensing in CMOS technology is addressed. Large photosensing area generally implies high photodetector capacitance and is a challenge for high speed and noise performance. Therefore different photodetector types, system architectures and operating modes are investigated with respect to speed, dynamic range, resolution, sensitivity, chip area and power consumption.
First, a generic model for integrating sampled-data photosensing is introduced and implemented in a corresponding software tool, thus providing noise and performance analysis. Various signal processing techniques are considered, such as the use of a bias current, a bandwidth limiting filter, ramp analog-to-digital converters (ramp ADCs), correlated double sampling (CDS) and averaging. Different ramp ADC concepts are distinguished and the noise transfer characteristic of a ramp ADC using a comparator with fixed level is investigated, which is known in the literature as the level-crossing problem or the first passage time problem. The effect of CDS on 1/f noise is analyzed and a simple approximation for first-order low-pass filtered 1/f noise after correlated double sampling is found. The noise performance of integrating sampled-data photosensing systems is determined with respect to the model parameters. The derived relations show that high performance with respect to thermal noise and 1/f noise requires low photodetector capacitance.

Next, the basic photodetectors and architectures for large-area photosensing in CMOS technology are classified, realized and characterized. The basic photodetectors are the different types of photodiodes and the photogate. The basic photosensing architectures are the combinations of these photodetectors with the different types of integrators, which are the passive and the active integrator. Further array arrangements of the basic architectures such as active pixel sensors (APS) and photodiode arrays are investigated. Charge-coupled devices (CCDs) are discussed, but they are not realizable in the current CMOS technology. The realizable architectures are implemented in a modern $0.6\ \mu$m CMOS process and compared with respect to the different performance parameters.
Then, advanced photodetectors and architectures for large-area photosensing in CMOS technology are developed. After investigating the charge transport in photogates, the sweep photogate concept is presented, which combines the low photodetector capacitance of photogates with fast charge transport and yields low noise and high speed. Different improved photogates are realized and characterized confirming the sweep photogate concept. The realized $500\ \mu$m long shifted sweep photogate is about two decades faster than the standard photogate of the same length. Further current-mode architectures for low-voltage operation and speed and noise improvement are discussed and the photodiode current source and the current-mode transintegrator are introduced. The photodiode current source provides separation of the photodetector capacitance and the integration capacitance resulting in high speed. The current-mode transintegrator is a low-noise integrating amplifier stage with adjustable gain that yields high speed and improved noise performance. Cascode configurations such as the proposed improved regulated cascode circuit are used to improve precision, chip area and power consumption. The realized photodiode current source with current-mode transintegrator achieves noise-equivalent optical power densities in the range of 10 nW/m^2 at measurement times of 10 s with a photodetector area of $30\ \mu\text{m} \times 500\ \mu$m.
The integrating sampled-data photosensing model and the corresponding software are powerful tools for the design of future advanced large-area photosensing systems. The sweep photogate concept is a promising approach for improved noise performance of applications with moderate speed requirements, e.g. in optical spectrometry. Current-mode architectures are superior in different concerns, e.g. in very high speed applications such as in fiber optic transmission systems. The low-noise current-mode transintegrator with its high transfer coefficient is particularly suitable to low-level applications that do not require high resolution, e.g. for IR remote control applications.

KURZFASSUNG

Der Bedarf an hochentwickelten Photosensoren, um die Aufnahme und Verarbeitung von Informationen durch das menschliche Auge zu ersetzen und zu automatisieren, nimmt täglich in allen Lebensbereichen stetig zu. Neben herkömmlicher Bildaufnahme vergrössert sich der breite Bereich von Anwendungen mit grosser photoempfindlicher Fläche fortlaufend, und zahlreiche spezifische Anwendungen werden immer wichtiger, wie zum Beispiel Anwendungen optischer Spektrometrie in der Umgebungsüberwachung. Photodetektoren in CMOS-Technologie mit auf dem gleichen Chip integrierter analoger und digitaler Signalverarbeitung bieten hohe Funktionalität und ermöglichen kostengünstige miniaturisierte "system-on-a-chip"-Lösungen.
In dieser Arbeit wird grossflächige Photosensorik in CMOS-Technologie behandelt. Grosse photoempfindliche Fläche bedeutet üblicherweise hohe Photodetektorkapazität und stellt eine Herausforderung an gutes Geschwindigkeits- und Rauschverhalten dar. Deshalb werden verschiedene Arten von Photodetektoren, Systemarchitekturen und Betriebsarten hinsichtlich Geschwindigkeit, Dynamik, Auflösung, Empfindlichkeit, Chip-Fläche und Leistungsverbrauch untersucht.
Zuerst wird ein generisches Modell für integrierende abgetastete Photosensorik eingeführt und in einem entsprechenden Anwendungsprogramm implementiert, was Rausch- und Leistungsauswertungen ermöglicht. Berücksichtigt werden verschiedenartige Signalverarbeitungsmethoden wie die Verwendung eines Grundstromes, ein bandbegrenzendes Filter, Rampen-Analog-Digital-Wandler (Rampen-"analog-to-digital converters", Rampen-ADCs), korrelierte Doppelabtastung ("correlated double sampling", CDS) und Mittelwertbildung. Verschiedene Konzepte von Rampen-ADCs werden unterschieden und das Rauschübertragungsverhalten eines Rampen-ADCs mit einem Komparator mit fester Vergleichsschwelle wird beleuchtet, was in der Literatur als "level-crossing"- oder "first passage time"-Problem bekannt ist. Die Auswirkung von

CDS auf 1/f-Rauschen wird untersucht und eine einfache Näherung für mit einem Tiefpass erster Ordnung gefiltertes 1/f-Rauschen nach CDS wird gefunden. Das Rauschverhalten integrierender abgetasteter Photosensoriksysteme mit Bezug auf die Modellparameter wird bestimmt. Die hergeleiteten Beziehungen zeigen, dass günstiges Verhalten hinsichtlich thermischem und 1/f-Rauschen tiefe Photodetektorkapazität erfordert.
In der Folge werden die grundlegenden Photodetektoren und Architekturen für grossflächige Photosensorik in CMOS-Technologie klassifiziert, realisiert und charakterisiert. Die grundlegenden Photodetektoren sind die verschiedenen Arten von Photodioden und das Photogate. Die grundlegenden Photosensorikarchitekturen sind die Kombinationen dieser Photodetektoren mit den verschiedenen Arten von Integratoren, welche der passive und der aktive Integrator sind. Weiter werden Array-Anordnungen der grundlegenden Architekturen wie Aktiv-Pixel-Sensoren ("active pixel sensors", APS) und Photodioden-Arrays untersucht. Ladungsgekoppelte Elemente ("charge-coupled devices", CCDs) werden behandelt, aber sie sind nicht realisierbar in der aktuellen CMOS-Technologie. Die realisierbaren Architekturen sind in einem modernen $0.6\ \mu$m-CMOS-Prozess implementiert und werden hinsichtlich der verschiedenen Leistungsmerkmale verglichen.
Dann werden fortgeschrittene Photodetektoren und Architekturen für grossflächige Photosensorik in CMOS-Technologie entwickelt. Nach der Untersuchung des Ladungstransports in Photogates wird das Konzept des Sweep-Photogates vorgestellt, welches die tiefe Photodetektorkapazität von Photogates mit schnellem Ladungstransport vereint und somit tiefes Rauschen und hohe Geschwindigkeit ergibt. Das realisierte $500\ \mu$m lange Schieberegister-Sweep-Photogate ist etwa zwei Dekaden schneller als das gleich lange einfache Photogate. Weiter werden Architekturen im Strombereich für tiefe Versorgungsspannungen und verbessertes Geschwindigkeits- und Rauschverhalten behandelt und die Photostromquelle und der Strombereich-Transintegrator werden eingeführt. Die Photostromquelle ermöglicht eine Trennung der Photodetektorkapazität und der Integrationskapazität, was hohe Geschwindigkeit bringt. Der Strombereich-Transintegrator ist eine rauscharme integrierende Verstärkerstufe mit einstellbarer Verstärkung, was hohe Geschwindigkeit und verbessertes Rauschverhalten ergibt. Kaskoden-Schaltungen wie die verbesserte regulierte Kaskode werden zur Verbesserung von Genauigkeit, Chip-Fläche und Leistungsverbrauch verwendet. Die realisierte Photostromquelle mit Strombereich-Transintegrator erreicht rauschäquivalente optische Leistungsdichten im Bereich von $10\ \mathrm{nW/m^2}$ bei Messzeiten von $10\ \mathrm{s}$ mit einer

Photodetektorfläche von $30\ \mu\text{m} \times 500\ \mu\text{m}$.
Das Modell für integrierende abgetastete Photosensorik und das entsprechende Anwendungsprogramm sind leistungsfähige Werkzeuge für den Entwurf von zukünftigen fortgeschrittenen grossflächigen Photosensoriksystemen. Das Konzept des Sweep-Photogates ist ein vielversprechender Ansatz für verbessertes Rauschverhalten bei Anwendungen mit mässigen Geschwindigkeitsanforderungen, wie zum Beispiel in optischer Spektrometrie. Architekturen im Strombereich sind in verschiedener Hinsicht überlegen, zum Beispiel in sehr schnellen Anwendungen wie in faseroptischen Übertragungssystemen. Der rauscharme Strombereich-Transintegrator mit seinem hohen Übertragungsmass ist besonders geeignet für Kleinstsignalanwendungen, welche keine hohe Auflösung benötigen, wie zum Beispiel für Infrarot-Fernbedienungen.

1. INTRODUCTION

Motivation

Progress in technology and productivity enhancement in industry as well as in everyday life shows an ever increasing demand for automation. Reliable and efficient automation is based on regulation processes requiring a high level of online information about the environment. Automated information acquisition makes use of highly developed sensors and demands systems that can replace human information sensing and processing. One of the most important human sensors is the eye, which represents a photosensing system with high resolution and very high dynamic range as well as a high degree of specific integrated information pre-processing. There exists a large effort in developing more and more powerful photosensors extending from smart optical sensors [1] to artificial retinas [2][3] and seeing chips [4].

The objective of this work is to investigate photodetector types, system architectures and operating modes of large-area photosensors in complementary metal-oxide-semiconductor (CMOS) technology with the aim of optimizing performance parameters such as speed, dynamic range, resolution, sensitivity, chip area and power consumption.

Very important fields of large-area photosensing applications are infrared (IR) remote controls, fiber optic transmission systems and optical spectrometry. Large-area photosensors with increased sensitivity enhance range and facilitate alignment of IR remote controls or could provide novel wireless networks. High-speed large-area photosensors in CMOS allow to build low-cost single-chip fiber optic receivers in pure CMOS technology for use in fiber optic transmission systems. Completely integrated photosensors with large sensitive area and very high dynamic range are used to develop miniaturized sensor heads for optical spectrometry, e.g. for environmental control or biomedical diagnostics.

This work shall contribute in the particular field of photosensing with large sensitive area to further approach the skills of the human eye, to see the light in its

various intensities and appearances.

Analog versus Digital

Whereas most signals in nature fundamentally behave in a continuous way and therefore nature mostly represents an analog domain, any kind of images of nature nowadays are usually represented and processed by electronic circuitry in the digital domain offering high performance and flexibility. Thus interfacing with nature requires sensors and actuators working in the analog domain for compatibility reasons. Conversions between nature's analog domain and the domain of the digital circuitry are performed by analog-to-digital converters (ADC) and digital-to-analog converters (DAC). Signal processing can be performed in the analog as well as in the digital domain. Thus electronic circuits and systems generally consist of sensors, analog signal processing circuitry, analog-to-digital converters, digital signal processing circuitry, digital-to-analog converters and actuators.
Before digital circuits were available, signal processing had been fully analog and no conversion and digital circuitry had been present. Later these parts were introduced and nowadays there is an ongoing shift from analog to digital signal processing due to the availability of continuously increasing computing performance at decreasing dimensions [5][6]. The reduction in classical analog signal processing circuitry increases the need for smart sensors with a high level of integrated functionality for close and simple connection to analog-to-digital converters. While the analog signal processing part may fully disappear in the future, the sensors will always be present and be of great importance.

Imaging versus Large-Area Photosensing

A photodetector can be defined as an element whose output signal represents the intensity of the incident light integrated over a certain area. A large number of photosensing applications require more than one such single photosensing element or photodetector in order to achieve spatial resolution. Photosensing elements or photodetectors are usually arranged in one- or two-dimensional arrays in order to obtain a one- or two-dimensional picture. A single element of that array or picture is called "picture element" or "pixel".
A very large field of photosensing is imaging using large arrays of small pixels with sizes down to a square of some μm edge length [7]. Typical applications are

video and electronic still cameras, scientific imaging or guidance and navigation sensors. There has been a lot of work in the field of imaging where parasitic effects and technology dependence have high influence.
There is a wide range of specific photosensing applications with large pixel sizes [8][9], e.g. in optical metrology such as spectrometry or densitometry, industrial process control, biomedical applications or optical telecommunications such as infrared (IR) remote control or fiber optic transmission systems. Large-area requirements may result from geometry reasons as well as from speed, resolution or sensitivity requirements. In this work large-area photosensing is addressed. Since large photosensing area makes the photodetectors robust to parasitic effects, a comparative analysis of different large-area photosensing concepts seems practicable. Large-area photosensing in this work refers to pixel sizes larger than about $100\ \mu\text{m} \times 100\ \mu\text{m}$.

CCD versus CMOS

Charge-coupled devices (CCD) [10] had an enormous impact on imaging applications in the past and rapidly supplanted traditional metal-oxide-semiconductor (MOS) technology based photosensors which suffered from limited noise performance due to high parasitic capacitances [11]. CCDs have been evolved for a very long time and their benefits are very high performance as well as high density. But there are several drawbacks due to their sophisticated level of development. They are fabricated in a highly specialized technology resulting in high costs. Their operation principle requires high supply voltages and makes it difficult to achieve very large array sizes.
There have been intensive efforts in the last few years to develop photosensors in CMOS technology with comparable performance and there is a continuous discussion on whether CMOS photosensors will supplant CCDs in the future [12]. CMOS is the mainstream technology in digital electronics and benefits from good availability and high cost efficiency due to its high market share. It is compatible with analog and digital circuitry as well as with photosensors and therefore offers increased functionality and an exceptional level of miniaturization. It is suitable for low-voltage and low-power applications and its architectures provide random access to the individual pixels. However, compared to CCDs these systems basically have limited performance mainly due to fixed-pattern noise [13] unless suitable signal processing techniques for fixed-pattern noise reduction are applied.

System-on-a-Chip

The compatibility of CMOS technology with analog and digital circuitry as well as with photodetectors combined with the continuously increasing level of circuit integration push the development of system-on-a-chip solutions in photosensing applications [14]. Single-chip photosensing systems offer cost reductions and open new applications due to the enhanced miniaturization. They support the simple and powerful implementation of drastically increased functionality and the entire on-chip signal processing circuitry yields potential for improved performance.

CMOS Scaling

CMOS technology is continuously being scaled down driven by high performance and low power requirements of digital circuits [15][16]. Scaling down the dimensions in digital circuits results in smaller chip area or higher density and therefore reduced costs. In addition, capacitances are reduced and speed performance is improved. Doping concentrations have to be increased to reduce the size of depletion regions and thus to preserve node separation. Voltages are scaled down along with dimensions in order to preserve the electric fields. Reduced voltages in combination with decreased currents yield drastically reduced power consumption per circuit. Nevertheless, even with the reduction of the voltages, total power consumption increases due to the increased density and performance, and because leakage currents are increased by scaling down threshold voltages.
In analog circuits CMOS scaling generally results in improved transistors and in combination with decreasing voltages reduces power consumption. But at given performance, decreasing voltage considerably increases power consumption. The overall effect is that power consumption decreases with scaling down to minimum feature sizes of about $0.35\ \mu$m or $0.25\ \mu$m and increases for smaller minimum feature sizes or circuit performance decreases [17]. In addition, in deep submicron CMOS technology device characteristics become more sensitive to variations in channel length, thus magnifying the effects of process variations and device mismatch [18].
Although a lot of parameters relevant to photosensing are affected by CMOS scaling, e.g. the available voltage swing, standard CMOS technology seems to be suitable for photosensing applications down to minimum feature sizes of about $0.35\ \mu$m or $0.25\ \mu$m [19].

Chip-Level versus Pixel-Level Analog-to-Digital Conversion

There are different multiplexing approaches in analog-to-digital conversion of pixel arrays [20][14]. The traditional chip-level analog-to-digital conversion sequentially uses a single analog-to-digital converter (ADC) for all pixels [21]. The chip-level ADC is not area-critical, but it has to be fast due to its serial operation. Driven by the increasing level of circuit integration there are approaches towards column-level analog-to-digital conversion of two-dimensional arrays corresponding to pixel-level analog-to-digital conversion of one-dimensional arrays. There are true column-level ADCs that serve one column of a two-dimensional array [22] as well as interleaved column-level ADCs that are shared among several columns [20][23]. Column-level ADCs can be slower than chip-level ADCs but their area is more critical as a whole one-dimensional array of ADCs has to be implemented. Further decreases in multiplexing in two-dimensional arrays are realized in interleaved pixel-level ADCs [24] and true pixel-level ADCs [25][26]. They have even more relaxed speed requirements but their area is strongly limited. Whereas in chip-level ADCs various analog-to-digital conversion techniques are used, towards pixel-level architectures mainly oversampling $\Sigma\Delta$ converters or any kind of ramp analog-to-digital conversion technique [27] are utilized for area reasons.

Voltage-Mode versus Current-Mode

Traditional signal processing circuits operate in the voltage-mode, i.e. the signals are represented by voltages. The supply voltage has strong impact on circuit performance, since the available voltage swing determines the maximum dynamic range and resolution. Speed performance is mainly limited by parasitic capacitances that have to be charged according to their voltage swings. As voltages are scaled down, analog circuit performance with respect to dynamic range and resolution is generally reduced. In contrast, current-mode circuits, i.e. circuits where signals are represented by currents, can achieve high dynamic range and resolution even at low supply voltages [28]. In addition, speed performance can be very high since no significant voltage swings have to be applied to the parasitic capacitances. Thus for high performance analog circuits at low supply voltages current-mode circuits are often preferable to traditional voltage-mode circuits.

Outline of this Work

The fundamentals of photosensing such as the basic properties of light and the conversion of light into an electrical value in a semiconductor are briefly reviewed in Chapter 2. In Chapter 3 a generic model for integrating sampled-data photosensing is presented and the basic parameters and relations with respect to noise and performance as well as different signal processing techniques are discussed. The effect of photodetector capacitance on performance is investigated. Guidelines for the realized circuits and the corresponding measurements are given. Chapter 4 analyzes, characterizes and compares the basic photodetectors in standard CMOS technology. The correspondence between photosensing area and photodetector capacitance is analyzed. In Chapter 5 the basic photosensing architectures employing the basic photodetectors are analyzed and realized. The architectures are basically determined by the photodetector, the type of integrator and the use of a single detector or an array of detectors. The realizations are characterized and compared and a synopsis is presented. Chapter 6 explores advanced photodetectors for large-area photosensing in CMOS technology with emphasis on photodetector capacitance. The charge transport in photogates is treated and two improved photogate concepts are presented, realized and characterized. In Chapter 7 a photodetector circuit and an integrator in the current-mode are introduced and two advanced architectures for large-area photosensing are proposed and realized. These architectures are less critical with respect to photodetector capacitance. They are characterized and compared and a synopsis is presented. Chapter 8 concludes the work.

2. PHOTOSENSING FUNDAMENTALS

This chapter briefly reviews the basic properties of light and discusses the conversion of light into an electrical value in a semiconductor. The different steps associated with the photodetection process in CMOS technology are identified and the characteristic parameters are discussed. Further the general structure of a photosensing system is introduced and the signal acquisition process is treated from a signal theory point of view.

2.1 Light

Light is an electromagnetic wave phenomenon described by the same theoretical principles that govern all forms of electromagnetic radiation [29]. Optical frequencies occupy a band of the electromagnetic spectrum that extends from the infrared through the visible to the ultraviolet with wavelengths from 1 mm to 10 nm. The wavelengths of visible light range from 390 nm to 760 nm.
The intensity of the incident light is characterized by the optical power density per unit area P''_{opt}. A complete uniform light beam with light spot size A_{opt} supplies the optical power

$$P_{opt} = A_{opt} P''_{opt}. \tag{2.1}$$

The optical energy E_{opt} transferred during the time t is

$$E_{opt} = P_{opt} t. \tag{2.2}$$

This refers to a number of photons

$$n_{photon} = \frac{E_{opt}}{E_{photon}}, \tag{2.3}$$

where the photon energy E_{photon} is

$$E_{photon} = hf = \frac{hc}{\lambda}. \tag{2.4}$$

h is the Planck constant

$$h = 6.63 \cdot 10^{-34} \text{ Js} \tag{2.5}$$

and f is the frequency

$$f = \frac{c}{\lambda}. \tag{2.6}$$

c is the speed of light in vacuum

$$c = 3.00 \cdot 10^{8} \text{ m/s} \tag{2.7}$$

and λ is the wavelength.

2.2 Optics

Most of the photosensing applications need optical components to produce some picture of the environment on the photodetector. These optical systems may be very complex and can perform various operations in the optical domain, but they generally suffer from very high costs. Therefore if admissible the optical systems are usually reduced to the minimum and signal processing is performed in the electronic domain. Often the optical system consists of an objective with one or several lenses such as in camera applications. Due to the near diffraction limit of these camera lenses it is generally acknowledged that pixel sizes much below $5\ \mu\text{m} \times 5\ \mu\text{m}$ are not needed [19].
Integrated on-chip optics provide potential for advanced optical signal processing and highly enhanced miniaturization. There has been a lot of work in on-chip color filters for color imaging applications and monolithic lens arrays to increase the responsivity of pixels [30]. However these techniques are not available in standard CMOS technology and need further processing steps thus producing additional costs.

2.3 Photodetection in CMOS

Photodetection in CMOS technology means the conversion of incident light with optical power P_{opt} into an electrical value, which is primary a current and even-

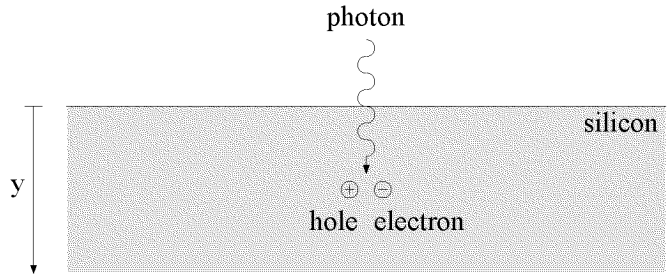


Fig. 2.1: Charge generation. An impinging photon generates an electron-hole pair.

tually a voltage. This whole process consists of charge generation, charge transport, charge detection or charge collection and finally charge conversion.
Charge generation means that impinging photons are absorbed in the semiconductor and generate electron-hole pairs by the supplied photon energy as illustrated in Fig. 2.1. The quantum efficiency η represents the relation between the number of photons and the number of photogenerated charge carriers n_{ph}:

$$n_{ph} = \eta n_{photon}. \tag{2.8}$$

Photon absorption depends on the wavelength and the material. As photons are absorbed the optical power density within the semiconductor decreases according to

$$P''_{opt}(y) = P''_{opt} e^{-\alpha_{opt} y}, \tag{2.9}$$

where α_{opt} is the absorption coefficient and y is the depth in the semiconductor. The light penetration depth y_{opt} is defined as the depth at which the optical power density has fallen to the $1/e$ part of the surface optical power density:

$$y_{opt} = \frac{1}{\alpha_{opt}}. \tag{2.10}$$

The absorption coefficient and the light penetration depth are wavelength dependent. The shorter the wavelength the higher the absorption coefficient and the lower the light penetration depth. In silicon the light penetration depth varies from 0.055 μm to 6.7 μm for wavelengths from 390 nm to 760 nm [31].
Charge transport is necessary to separate the electrons and holes to avoid recombination of these charge carriers and to capture and transport them to a detection node in order to measure the amount of generated charge. The charges are

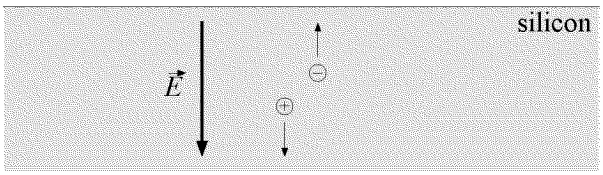


Fig. 2.2: Charge transport. The electric field $\vec{E}$ separates the electrons and holes and captures the charge.

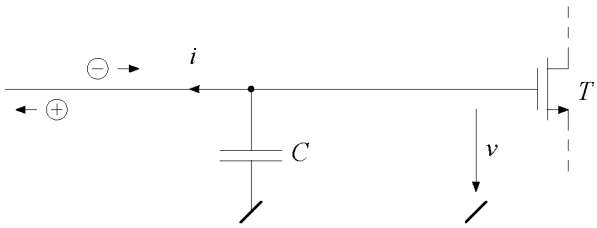


Fig. 2.3: Charge detection. Equivalent circuit of the detection node with capacitance C and transistor T.

transported by an electric field in the semiconductor as shown in Fig. 2.2. This produces a photocurrent

$$i_{ph} = R_\lambda P_{opt}, \tag{2.11}$$

where R_λ is the responsivity

$$R_\lambda = \frac{e}{hc}\lambda\eta \tag{2.12}$$

with the elementary charge

$$e = 1.60 \cdot 10^{-19}\ \mathrm{C}. \tag{2.13}$$

Charge detection or charge collection refers to collecting the transported charge at a detection node with a certain capacitance thus producing a detection voltage. This node is connected to the gate of a transistor for detection as illustrated in Fig. 2.3. Instead of collecting the charge on the capacitance, the detection voltage could be produced by the charge flowing through a resistor at the detection node.
Charge conversion is accomplished by the transistor in Fig. 2.3 and subsequent circuit elements thus yielding an electrical value that represents the photogenerated charge.

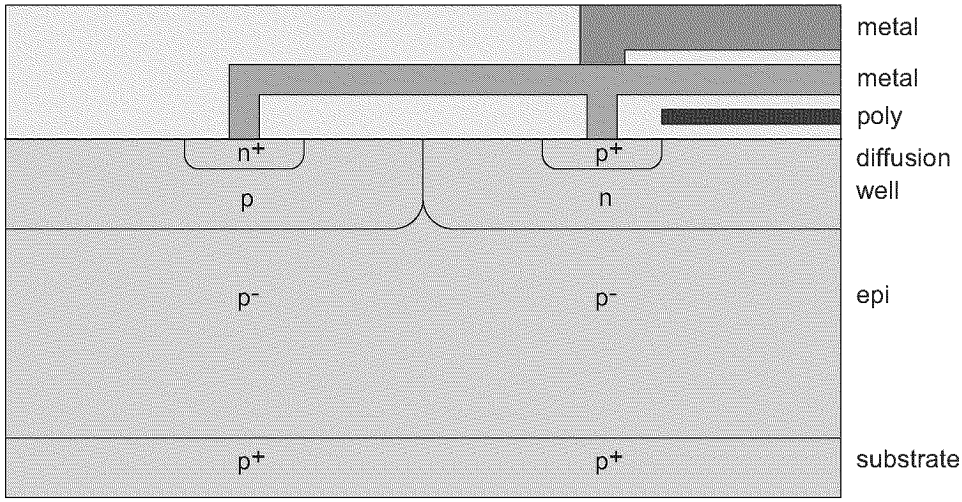


Fig. 2.4: AMS 0.6 μm CMOS process CUX.

In this work the CMOS process CUX with a minimum feature size of 0.6 μm provided by Austria Mikrosysteme (AMS) is used exclusively. The cross section of this technology with the typical layers is shown in Fig. 2.4. It provides several semiconductor regions which could be suitable for charge generation and different space charge regions for charge transport as well as versatile circuits for charge collection and detection. The AMS 0.6 μm CMOS process CUX is a twin-well p-substrate epi-layer process with one poly and two metal layers in its basic configuration. A second poly layer for linear capacitors as well as a third metal layer are available optionally. There is further a high-resistance option for the first poly layer in order to integrate high resistor values. Despite of these partly analog options the basic configuration of this process is fully digital and the whole technology including the options is widely used and can be considered as standard CMOS technology.

2.4 Photosensing Area

In this work photosensing area is referenced as an area of homogeneous illumination whose optical power density is to be measured. Systems with spatial resolution, e.g. imaging systems, are considered as arrays of many such photosensing areas, each of them showing approximately homogeneous illumination in its area.
In a lot of applications the size of the photosensing area can be chosen in a cer-

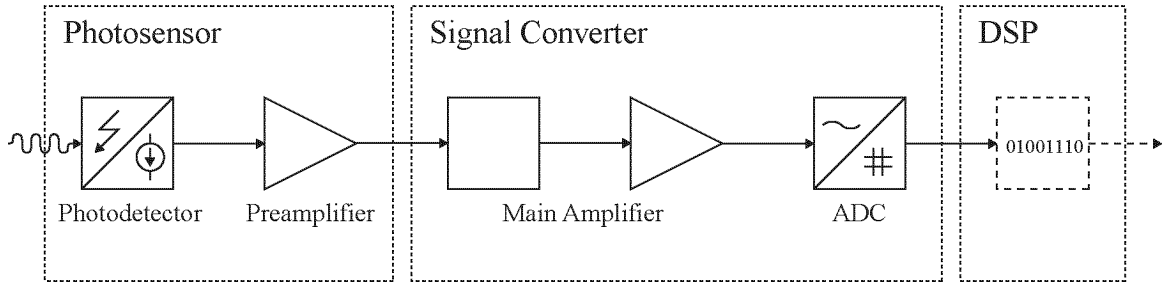


Fig. 2.5: Photosensing system.

tain range although having consequences on the optical system. But there are many systems where optical or geometrical requirements exactly determine the photosensing area.
Photodetector area does not have to be equal to the photosensing area. It may cover only a part of the photosensing area still yielding the correct optical power density as it is equal in every spot of the photosensing area. Although small photodetector area produces small absolute signal values to be measured and requires more sensitive electronics.

2.5 Photosensing Systems

A photosensing system basically consists of a photosensor, a signal converter and a digital signal processor (DSP) as shown in Fig. 2.5. The photosensor fundamentally contains a photodetector and a preamplifier, although the preamplifier does not necessarily have to exist. The signal converter consists of a main amplifier and an analog-to-digital converter (ADC). The digital signal processor may be any digital system that further processes the digital data delivered by the ADC.

2.6 Signal Acquisition

The sampling theorem implies that the signal bandwidth B_{signal} has to be lower than the sampling-limited signal bandwidth B_{ss}:

$$B_{signal} < B_{ss}. \tag{2.14}$$

The sampling-limited signal bandwidth B_{ss} is equal to

$$B_{ss} = \frac{f_s}{2}, \tag{2.15}$$

where f_s is the sampling frequency

$$f_s = \frac{1}{T_s} \tag{2.16}$$

with the sampling period T_s.
If the signal bandwidth is higher than the sampling-limited signal bandwidth the signals are distorted by the sampling process due to aliasing and the samples do not precisely represent the complete signal shape before the sampling process any more. Therefore signal bandwidth usually has to be limited by an anti-aliasing filter prior to sampling.
As an alternative, aliasing can be overcome by oversampling. This means that the sampling frequency is chosen much higher than the rate measurement values are required. This automatically increases the sampling-limited signal bandwidth and allows much higher signal bandwidths according to (2.14). However this requires much higher speeds and the digital samples with high data rate have to be processed additionally to obtain the measurement values at reduced rate.
A lot of analog-to-digital conversion schemes require sample-and-hold technique at their input to guarantee proper operation. But if measurement time or signal bandwidth are low enough the signal is approximately constant during the measurement and sample-and-hold is not required. Integrating analog-to-digital conversion techniques with direct integration of the signal do not need sample-and-hold stages as well.
For ideal signal acquisition sampling times have to be equally spaced. Sampling time variations or time jitter generally change the signal and introduce some kind of noise. Its effect can be minimized using oversampling or precise sample-and-hold technique. Sampling time variations are particularly effective in analog-to-digital conversion techniques with signal-dependent measurement times such as in direct integration analog-to-digital converters. If integration starts at equally spaced times and lasts a signal-dependent period the effective sampling times are approximately half the periods after start of integrations and may vary very much. In this work signal bandwidths are assumed to be always low enough that the signals are approximately constant (quasi-static) during the whole measurement time, thus removing sampling time variation effects.

2.7 Conclusions

A general photosensing system basically consists of a photosensor, a signal converter and a digital signal processor, where the photosensor includes the photodetector and the signal converter includes the analog-to-digital converter.
The electrical signal level at the output of a photodetector is a function of optical power density, light spot size, wavelength, and quantum efficiency of the photodetector. The quantum efficiency of a photodetector depends on its structure, as its geometry and electrical properties determine the charge generation and transport processes. CMOS processes offer different layers in the semiconductor that can serve as space charge region to build an electric field for charge transport.
High oversampling allows to omit sample-and-hold and reduces aliasing and the influence of sampling time variations.

3. INTEGRATING SAMPLED-DATA PHOTOSENSING (ISDPS)

This chapter analyzes integrating sampled-data photosensing. Non-integrating sampled-data photosensing has minor significance in CMOS technology and is not considered here. This chapter first identifies all the different fundamental functional blocks of a general integrating sampled-data photosensing system. A generic model for integrating sampled-data photosensing is developed that provides noise and performance analysis for any integrating sampled-data photosensing system. The basic parameters and relations of this model are derived and different signal processing techniques for enhanced performance are discussed. After introducing the principal noise sources of this model, the expressions for the overall noise performance of the system are derived and key performance issues with regard to different performance challenges are discussed. Finally the qualitative and quantitative noise behavior of the voltage ramp analog-to-digital converter in the measurement setup is experimentally verified.

3.1 Generic Model

Fig. 3.1 shows the generic integrating sampled-data photosensing (ISDPS) model. It basically consists of the photocurrent source, the integrating analog-to-digital converter (integrating ADC) and the digital signal processor (DSP).
The photocurrent source contains the photodetector and the preamplifier. In addition a potential bias current is provided.
The integrating analog-to-digital converter consists of the integrator, the amplifier and the ramp analog-to-digital converter (ramp ADC). The amplifier either is the voltage amplifier or the transconductor in combination with the resistor if necessary. The ramp ADC can be the voltage or the current ramp ADC. There

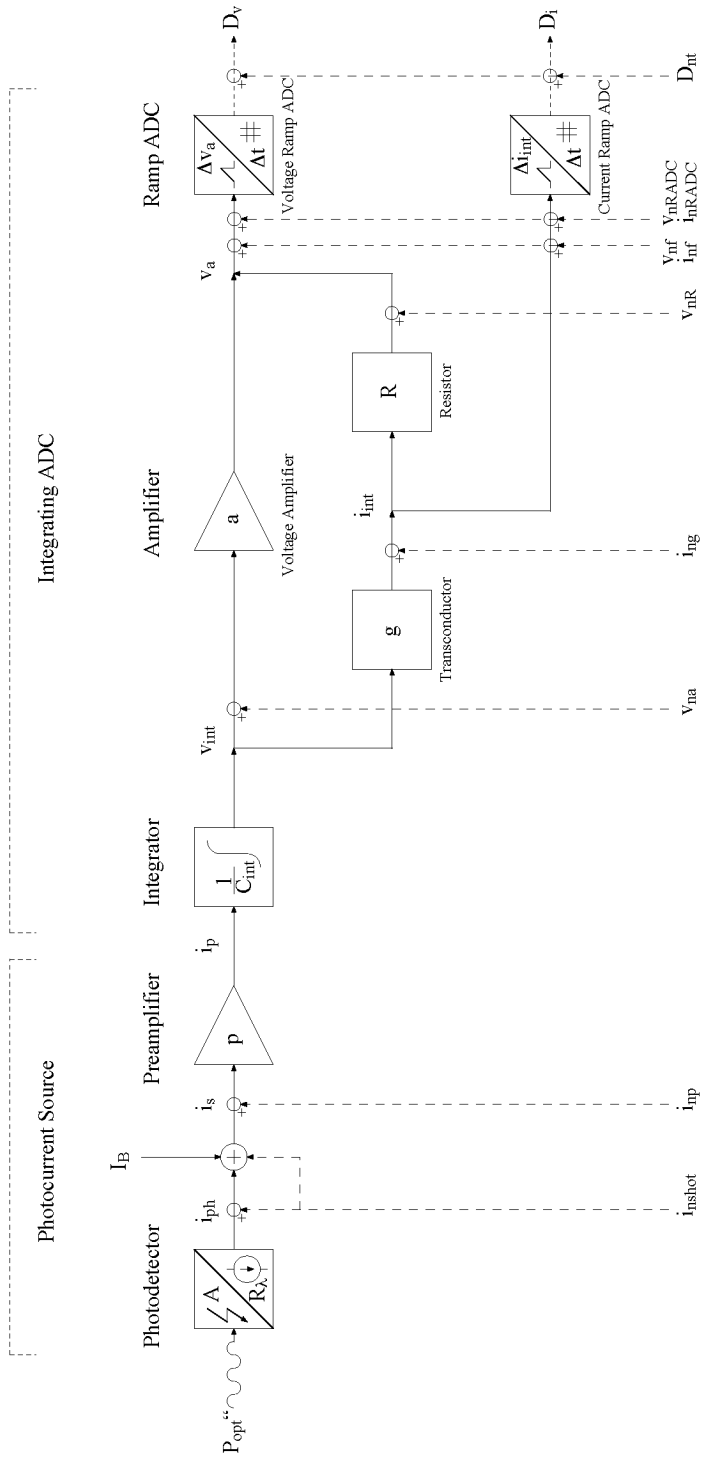


Fig. 3.1: Integrating sampled-data photosensing (ISDPS) model with bias current I_B and noise contributions i_n, v_n and D_n. The digital signal processor at the end of the diagram is not shown.

are principally three possible arrangements: the voltage amplifier in combination with the voltage ramp ADC, the transconductor with the resistor in combination with the voltage ramp ADC, or the transconductor in combination with the current ramp ADC.
The digital signal processor is the digital system that further processes the digital data delivered by the ADC.
Fig. 3.1 includes the different noise contributions as described later in this chapter.

3.1.1 Photodetector

The incident light has the optical power density per unit area P''_{opt}. The photodetector converts the light into the photocurrent

$$i_{ph} = R_\lambda A P''_{opt}, \tag{3.1}$$

where A is the photodetector area and R_λ is the responsivity. The signal current i_s is

$$i_s = i_{ph} \tag{3.2}$$

provided no bias current is present.

Bias

The bias is a constant value superimposed to the photogenerated signal providing a non-zero output signal even at zero photogenerated signal.
The bias current I_B causes a signal current

$$i_s = I_B + i_{phb}, \tag{3.3}$$

where i_{phb} is the photocurrent if a bias current is provided.

3.1.2 Preamplifier

The preamplifier amplifies the signal current with the preamplifier gain p and yields the preamplified current

$$i_p = p i_s. \tag{3.4}$$

3.1.3 Integrator

The integrator integrates the preamplified current and converts it to the integration voltage

$$v_{int} = \frac{1}{C_{int}} \int i_p dt \tag{3.5}$$

using the integration capacitance C_{int}. Provided the preamplified current is constant during the integration, this simplifies to

$$v_{int} = \frac{i_p}{C_{int}} t \tag{3.6}$$

and represents a linear voltage ramp.

3.1.4 Amplifier

The amplifier is either the voltage amplifier or the transconductor in combination with the resistor if necessary and amplifies the integration voltage yielding an amplified signal ramp.

Voltage Amplifier

The voltage amplifier with voltage amplifier gain a directly produces the amplified voltage

$$v_a = a v_{int}. \tag{3.7}$$

Transconductor

The transconductor with transconductor value g generates the integration current

$$i_{int} = g v_{int}. \tag{3.8}$$

Resistor

The resistor with resistor value R converts the integration current to the amplified voltage

$$v_a = R i_{int}. \tag{3.9}$$

As the two possible amplifier paths in Fig. 3.1 for voltage ramp analog-to-digital conversion are equivalent, the voltage amplifier gain has to be equal to the gain of the transconductor in combination with the resistor:

$$a = gR. \tag{3.10}$$

3.1.5 Ramp Analog-to-Digital Converter (Ramp ADC)

The ramp analog-to-digital converter converts the signal ramp into an integration sample, which is a digital value representing the slope of the ramp. The signal ramp is sampled at two different times to get two ramp samples. The time between these two ramp samples is the integration time Δt and together with the difference between the two ramp samples forms the integration sample, which represents the slope of the signal ramp.

Voltage Ramp ADC

The voltage ramp ADC converts the voltage ramp into the digital output sample D_v. The difference between the two ramp samples is the amplified voltage drop Δv_a.

Current Ramp ADC

Analogous to the voltage ramp ADC the current ramp ADC converts the current ramp into the digital output sample D_i. The difference between the two ramp samples is the integration current drop Δi_{int}.

3.1.6 Digital Signal Processor (DSP)

The digital signal processor is the digital system that further processes the digital data delivered by the ramp ADC and is assumed not to introduce additional noise.

3.2 Derived Parameters

In addition to the primary parameters of the integrating sampled-data photosensing model introduced in Section 3.1, several parameters useful in later discussions can be defined. Different charges referring to different nodes in the model, virtual integration parameters describing signal integration, transfer functions, signal limits and noise-equivalent signals can be derived.

3.2.1 Charge

The photogenerated charge q_{ph} is equal to

$$q_{ph} = \int i_{ph} dt. \tag{3.11}$$

Assuming constant photocurrent this totals to

$$Q_{ph} = i_{ph} \Delta t. \tag{3.12}$$

The number of photogenerated charge carriers n_{ph} is

$$n_{ph} = \frac{q_{ph}}{e} \tag{3.13}$$

and

$$N_{ph} = \frac{Q_{ph}}{e} \tag{3.14}$$

respectively.
The collected charge q_{int} is

$$q_{int} = \int i_p dt \tag{3.15}$$

and totals to

$$Q_{int} = i_p \Delta t. \tag{3.16}$$

The number of collected charge carriers n_{int} is

$$n_{int} = \frac{q_{int}}{e} \tag{3.17}$$

and

$$N_{int} = \frac{Q_{int}}{e} \tag{3.18}$$

respectively. The integration voltage drop Δv_{int} is

$$\Delta v_{int} = \frac{Q_{int}}{C_{int}} = \frac{i_p}{C_{int}} \Delta t. \tag{3.19}$$

3.2.2 Virtual Integration

The conversion of the signal current into the signal ramp at the input of the ramp ADC can be virtually considered as direct integration although it includes several functions. The virtual integration function depends on whether the voltage or the current ramp ADC is used.

Voltage Ramp ADC

For the voltage ramp ADC the virtual integration capacitance C_{virt} can be defined as

$$C_{virt} = \frac{C_{int}}{pa}. \tag{3.20}$$

This yields

$$v_a = \frac{1}{C_{virt}} \int i_s dt \tag{3.21}$$

and assuming the signal current to be constant results in a linear ramp

$$v_a = \frac{i_s}{C_{virt}} t. \tag{3.22}$$

The integration sample then refers to

$$\Delta v_a = \frac{i_s}{C_{virt}} \Delta t. \tag{3.23}$$

Current Ramp ADC

For the current ramp ADC the virtual integration coefficient h_{virt} defined by

$$h_{virt} = \frac{C_{int}}{pg} \tag{3.24}$$

yields

$$i_{int} = \frac{1}{h_{virt}} \int i_s dt \tag{3.25}$$

and for constant signal current results in a linear ramp

$$i_{int} = \frac{i_s}{h_{virt}} t. \tag{3.26}$$

The integration sample refers to

$$\Delta i_{int} = \frac{i_s}{h_{virt}} \Delta t. \tag{3.27}$$

3.2.3 Transfer Functions

The conversion of light into a photocurrent can be directly expressed by the specific responsivity R_A:

$$i_{ph} = R_A P''_{opt}. \tag{3.28}$$

The specific responsivity is defined by

$$R_A = R_\lambda A, \tag{3.29}$$

where A is the photodetector area.
The transfer function from the incident light to the signal ramp depends on the type of ramp ADC.

Voltage Ramp ADC

For the voltage ramp ADC the transfer function from the incident light to the amplified voltage is determined by the transfer factor T_A. This yields for the integration samples

$$\frac{\Delta v_a}{\Delta t} = T_A P''_{opt} \qquad , I_B = 0. \tag{3.30}$$

The transfer factor is defined by

$$T_A = \frac{R_A}{C_{virt}}. \tag{3.31}$$

Current Ramp ADC

For the current ramp ADC the transfer is determined by the transfer coefficient H_A, which yields for the integration sample

$$\frac{\Delta i_{int}}{\Delta t} = H_A P''_{opt} \qquad , I_B = 0. \tag{3.32}$$

The transfer coefficient is defined by

$$H_A = \frac{R_A}{h_{virt}}. \tag{3.33}$$

3.2.4 Limits

In this work minimum values are generally characterized by the subscript suffix $_{min}$ and maximum values by the subscript suffix $_{max}$.
According to the specifications and circuit topology there is a maximum integration time Δt_{max} and a minimum integration time Δt_{min}. The minimum integration time limits the photocurrent to the maximum photocurrent

$$i_{phmax} = C_{virt} \frac{\Delta v_a}{\Delta t_{min}}. \tag{3.34}$$

The maximum integration time analogously determines the minimum photocurrent

$$i_{phmin} = C_{virt} \frac{\Delta v_a}{\Delta t_{max}}. \tag{3.35}$$

The corresponding maximum optical power density P''_{optmax} is

$$P''_{optmax} = \frac{1}{R_A} i_{phmax} = \frac{1}{T_A} \frac{\Delta v_a}{\Delta t_{min}} \tag{3.36}$$

and the minimum optical power density P''_{optmin} is

$$P''_{optmin} = \frac{1}{R_A} i_{phmin} = \frac{1}{T_A} \frac{\Delta v_a}{\Delta t_{max}} \tag{3.37}$$

respectively.

3.2.5 Noise-equivalent Signals

Noise-equivalent signals are characterized by the subscript suffix $_{neq}$. They represent signal values equal to the effective noise signal. This is treated more detailed later in this chapter.

3.3 Signal Processing Techniques

3.3.1 Bias Current

A bias current as shown in Fig. 3.1 has an impact on most of the signal-related characteristics. The characteristics referring to the use of a bias current are characterized by the subscript suffix $_b$. Generally $I_B = 0$ is assumed unless indicated by the suffix.
When a bias current I_B is being used, it is added to the photocurrent i_{phb} according to (3.3). The effect on subsequent stages is the same as that of a photocurrent i_{ph} without bias current where i_{ph} is

$$i_{ph} = I_B + i_{phb}. \tag{3.38}$$

This relation is particularly useful in systems that require a minimum signal current to work properly, as the resulting signal current is non-zero due to the bias current even for zero photocurrent. It is explained in detail for the ramp ADC with fixed integration voltage drop later in this chapter.
However, although the effect on subsequent stages is in principle the same with a bias current, in the photodetector and particularly concerning the incident light the signal characteristics are different. In order to use the results without bias current to determine the characteristics when a bias current is applied, the following expressions can be derived. The photocurrent i_{phb} is defined by (3.1) and can be expressed as the photocurrent i_{ph} multiplied by a conversion function:

$$i_{phb} = R_\lambda A P''_{optb} = i_{ph} \frac{i_{phb}}{I_B + i_{phb}}. \tag{3.39}$$

Consequently this yields for the photogenerated charge Q_{ph}

$$Q_{ph} = Q_{phbias} + Q_{phb}, \tag{3.40}$$

$$Q_{phbias} = I_B \Delta t, \tag{3.41}$$

$$Q_{phb} = i_{phb}\Delta t = Q_{ph}\frac{i_{phb}}{I_B + i_{phb}}, \tag{3.42}$$

for the number of photogenerated charge carriers N_{ph}

$$N_{ph} = N_{phbias} + N_{phb}, \tag{3.43}$$

$$N_{phbias} = \frac{Q_{phbias}}{e}, \tag{3.44}$$

$$N_{phb} = \frac{Q_{phb}}{e} = N_{ph}\frac{i_{phb}}{I_B + i_{phb}}, \tag{3.45}$$

for the collected charge Q_{int}

$$Q_{int} = Q_{intbias} + Q_{intb}, \tag{3.46}$$

$$Q_{intbias} = pI_B\Delta t, \tag{3.47}$$

$$Q_{intb} = pi_{phb}\Delta t = Q_{int}\frac{i_{phb}}{I_B + i_{phb}}, \tag{3.48}$$

for the number of collected charge carriers N_{int}

$$N_{int} = N_{intbias} + N_{intb}, \tag{3.49}$$

$$N_{intbias} = \frac{Q_{intbias}}{e}, \tag{3.50}$$

$$N_{intb} = \frac{Q_{intb}}{e} = N_{int}\frac{i_{phb}}{I_B + i_{phb}}, \tag{3.51}$$

and for the integration voltage drop Δv_{int}

$$\Delta v_{int} = \Delta v_{intbias} + \Delta v_{intb}, \tag{3.52}$$

$$\Delta v_{intbias} = \frac{Q_{intbias}}{C_{int}} = \frac{pI_B}{C_{int}}\Delta t, \tag{3.53}$$

$$\Delta v_{intb} = \frac{Q_{intb}}{C_{int}} = \frac{pi_{phb}}{C_{int}}\Delta t = \Delta v_{int}\frac{i_{phb}}{I_B + i_{phb}}. \tag{3.54}$$

This allows to use the results without bias current to determine the characteristics when a bias current is applied. In this work it is always assumed that a photocurrent can be potentially partitioned into a bias current and a lower photocurrent.

3.3.2 Bandwidth Limiting Filter

In order to minimize noise for high performance, the bandwidth of the system has to be limited to the minimum possible still meeting the signal requirements. The input signal of the ramp ADC is a ramp signal with periodical reset resulting in a saw-tooth shape. The minimum length of a single saw-tooth is the minimum integration time. Thus a ramp-related bandwidth $1/\Delta t_{min}$ can be defined referring to the highest saw-tooth rate.
Simulations indicate that an analog bandwidth B of approximately four times the ramp-related bandwidth is required to guarantee proper ramp signals with a tolerable level of distortion to be processed by the ramp ADC:

$$B \approx \frac{4}{\Delta t_{min}}. \tag{3.55}$$

A saw-tooth shape filtered by a first-order low-pass with this bandwidth yields a distorted saw-tooth shape with a peak-to-peak value of more than 80 % of the original value. This provides reasonable signal drop, but the distorted ramp signal produces non-linearity in the signal conversion that could be corrected in the digital domain. Distortion of the filtered saw-tooth shape is mainly generated at the steep falling edge. The error in the gradient is less than 1 % over a length of 68 % of the period. Filtering a saw-tooth shape with an ideal low-pass thus removing all frequency components beyond four times the ramp-related bandwidth would yield much higher errors in the gradient over the whole period and would result in 18 % distortion if the dc component of the signal was taken into consideration.
Assuming a bandwidth limiting filter of first-order low-pass type with analog bandwidth B the noise-effective bandwidth B_n is

$$B_n = \frac{\pi}{2} B \tag{3.56}$$

according to Appendix C.6. This is the bandwidth of ideally band-limited white noise yielding the same effective noise signal as the first-order low-pass filtered white noise [32].
In this work it is assumed that the analog bandwidth is always limited according to (3.55) by a first-order low-pass filter.

3.3.3 Ramp ADC

There is a variety of analog-to-digital conversion architectures that are associated with the expression "ramp analog-to-digital converter (ramp ADC)". In this work ramp ADCs are defined as analog-to-digital converters that measure the slope of their input signal, which is a ramp signal [33]. Such ramp ADCs are very suitable for use in integrating ADCs. ADCs that convert the input signal by comparing it to a separately generated constant ramp are not primarily addressed here, although their operating principle is very similar [34].
In order to measure the slope of the ramp, ramp ADCs have to acquire a corresponding pair of integration time and signal drop that build the integration sample. In general this pair can be generated by random signal access, which means that there are no strong restrictions to either the integration time or the signal drop. But most architectures work with either a fixed integration time or a fixed signal drop. Fixed signal drop refers to fixed integration voltage drop for both voltage and current ramp ADC.

Random Signal Access

Random signal access in slope measurement of the ramp means that any algorithm or strategy can be employed to acquire the integration sample as a pair of integration time and signal drop as shown in Fig. 3.2. This may give high flexibility to the ramp ADC architecture and in general does not restrict the ramp, but it affords costly control logic. The performance of such ADCs can be very high as they allow to use the dynamic range and resolution of both the integration time domain and the signal drop domain. Multiple sampling is a dynamic range enhancement scheme that makes use of these random signal access advantages [35][36].

Fixed Integration Time

The straightforward approach for a ramp ADC is to measure the signal drop after a fixed integration time as shown in Fig. 3.3. This technique allows to employ any kind of standard ADC architecture. The signal drop during the integration time may range from zero to the full-scale input signal of the ADC, and the performance of the complete ramp ADC is limited by the signal drop

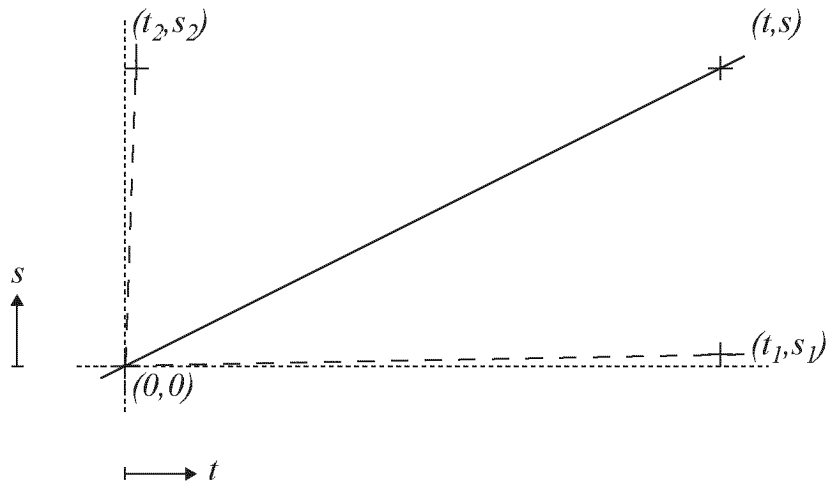


Fig. 3.2: Principle of the ramp ADC with random signal access. The integration sample is measured as a pair of integration time t and signal drop s.

domain measurement. This technique does not directly allow measuring very steep ramps unless the integration time is decreased.

Fixed Integration Voltage Drop

Ramp ADCs with fixed integration voltage drop measure the slope of the ramp by determining the integration time the signal ramp needs to attain a fixed signal drop as shown in Fig. 3.4. They permanently compare the ramp to a fixed comparator level thus obtaining the signal-dependent time. This structure is very similar to ADCs that convert the input signal by comparing it to a separately generated constant ramp. They principally consist of a comparator, a counter and a latch and are well-suited for multichannel implementation due to their simple and area-efficient architecture [33][34][27]. Instead of generating digital output data the converter could be used in a feedback arrangement without counter and latch to form an analog-to-frequency converter [37]. However the frequency would have to be measured by some means anyway.
There are single slope [33] as well as multiple slope approaches [38] to ramp ADCs. In order to be independent of reset effects of the ramp two comparators can be used. They have different comparator levels differing by the integration voltage drop and build a window comparator.
Ramp ADCs with fixed integration voltage drop do generally need high-speed

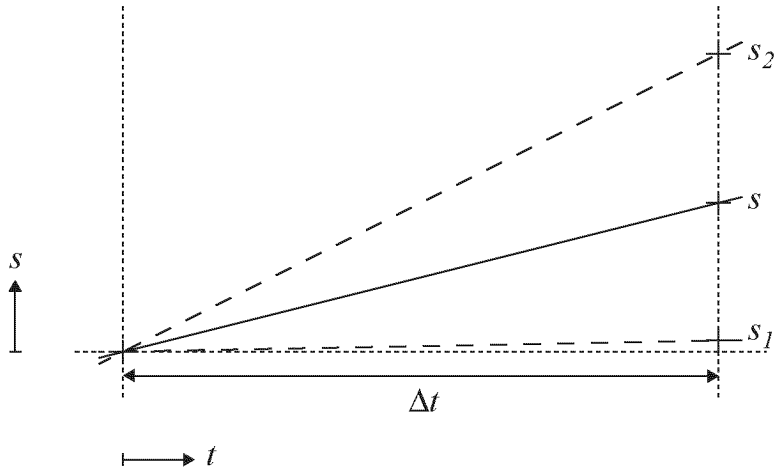


Fig. 3.3: Principle of the ramp ADC with fixed integration time. The signal drop s is measured for a fixed integration time Δt.

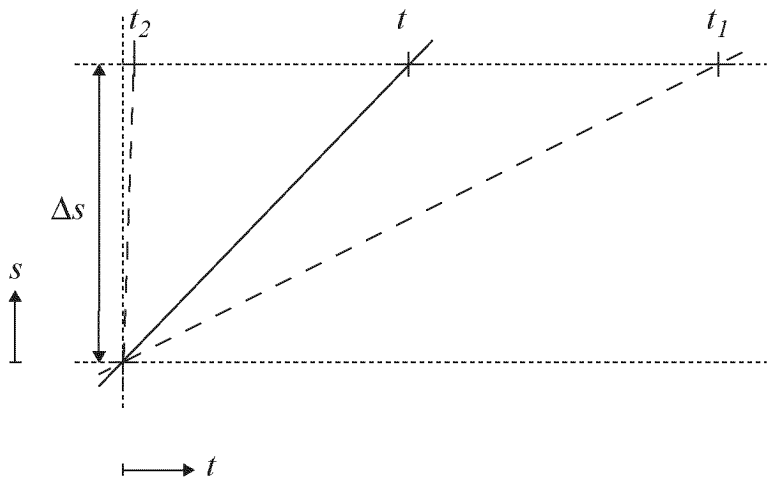


Fig. 3.4: Principle of the ramp ADC with fixed integration voltage drop. The integration time t is measured for a fixed signal drop Δs.

counters as their performance is achieved in the integration time domain. And since the integration voltage drop is fixed, the ramp has to guarantee a minimum slope to perform the measurements in a given maximum integration time. However a bias superimposed to the signal as described earlier in this chapter can be used to extend the signal range down to zero.
The fixed integration voltage drop corresponds to a fixed amount of collected charge for all integration samples. This is true for any integration transfer characteristic, even if it is completely non-linear. Since the integration time is measured for this fixed amount of collected charge, the integration samples depend on the signal current in a well defined way independent of any non-linearities in the signal path. The integration samples are exactly inversely proportional to the signal current and the signal measurements corresponding to the signal current can be calculated from the integration samples. Therefore the ramp ADC with fixed integration voltage drop is inherently linear. This is particularly useful in CMOS circuits if junction capacitances or MOS capacitors with voltage-dependent capacitance are used for integration. The non-linearities due to the voltage dependence of the capacitances do not affect the linearity of this ramp ADC.
In this work ramp ADCs with fixed integration voltage drop are used exclusively, although, in general, results can be extended to the other types accordingly.

3.3.4 Correlated Double Sampling (CDS)

As the signal ramp is periodically reset to generate the saw-tooth shape required for ramp analog-to-digital conversion, residual offsets are introduced by the reset operation generating variable starting points of the signal ramps. There are four main contributions to these residual offsets sometimes referred to as reset noise or fixed-pattern noise in arrays: Clock feedthrough of the reset switch; channel charge injection by the reset switch; sampled noise or kTC noise, which is Nyquist or thermal noise across the holding capacitor sampled at the end of reset; and leakage current [39]. To remove these residual offsets correlated double sampling (CDS) can be used [40]. CDS is an autozeroing technique that first samples the reset value and then the signal value. As the reset value is subtracted from the signal value to get the effective sample residual offsets are cancelled. In addition low-frequency noise such as 1/f noise is reduced due to the high-pass filter characteristics of CDS.
The transfer characteristics of CDS have been diversely investigated [41][42][43][44][45] and different advanced CDS methods have

been proposed [46][47][48]. The basic transfer characteristics of CDS are investigated in Appendix C.
Ramp analog-to-digital conversion with fixed integration voltage drop is well-suited for simple implementation of CDS by the use of a window comparator as mentioned earlier. In this work CDS is used exclusively for ramp analog-to-digital conversion and residual offsets are completely cancelled thus removing reset noise.

3.3.5 Averaging

In the ramp ADC with fixed integration voltage drop the integration time may be much shorter than the measurement time, which is the maximum integration time referring to the minimum input signal. Thus multiple integration samples can be taken during the measurement time and can be averaged to a final sample representing the measurement sample. This represents some kind of oversampling and provides noise reduction. Characteristics referring to this averaging technique are characterized by the subscript suffix $_{avg}$.
The number of integration samples per signal measurement m depends on the measurement time and the signal-dependent integration time and has to be an integer. For simplicity reasons boundary effects are neglected and the number of integration samples per signal measurement is defined as

$$m = \frac{\Delta t_{max}}{\Delta t} = \frac{pa\Delta t_{max}}{C_{int}\Delta v_a} i_{ph} \tag{3.57}$$

even though this is not an integer in general. With unchanged photocurrent

$$i_{phavg} = i_{ph} \tag{3.58}$$

or

$$i_{phbavg} = i_{phb} = i_{ph}\frac{i_{phb}}{I_B + i_{phb}} \tag{3.59}$$

respectively, the number of photogenerated charge carriers N_{phavg} increases to

$$N_{phavg} = mN_{ph} = \frac{\Delta t_{max}}{e} i_{ph} \tag{3.60}$$

or

$$N_{phbavg} = mN_{phb} = \frac{\Delta t_{max}}{e} i_{phb} \tag{3.61}$$

and the integration voltage drop Δv_{intavg} to

$$\Delta v_{intavg} = m\Delta v_{int} = \frac{p\Delta t_{max}}{C_{int}} i_{ph} \tag{3.62}$$

or

$$\Delta v_{intbavg} = m\Delta v_{intb} = \frac{p\Delta t_{max}}{C_{int}} i_{phb} \tag{3.63}$$

respectively. Thus averaging in ramp analog-to-digital conversion represents a measurement technique with virtually increased integration voltage drop for high signal levels. This consequently achieves enhanced dynamic range compared to the fixed integration time case and improved resolution compared to the fixed integration voltage drop case with single integration sample.

3.4 Noise

A noisy voltage $s_n(t)$ can be expressed as

$$s_n(t) = v + v_n(t), \tag{3.64}$$

where the signal voltage s is

$$s = \overline{s_n(t)} = v \tag{3.65}$$

and the noise voltage $v_n(t)$ results from

$$v_n(t) = s_n(t) - \overline{s_n(t)}. \tag{3.66}$$

According to Appendix C the mean square noise voltage v_{neff}^2 is

$$v_{neff}^2 = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} [v_n(t)]^2 \, dt \tag{3.67}$$

and the root mean square (rms) noise voltage v_{neff} or effective noise voltage is given by

$$v_{neff} = \sqrt{v_{neff}^2}. \tag{3.68}$$

The noise voltage power spectral density v_n^2 is a single-sided expression and is defined as

$$v_n^2 = \frac{\partial \left(v_{neff}^2\right)}{\partial f} = 2S(\omega), \tag{3.69}$$

where the power spectral density $S(\omega)$ is a double-sided expression defined in (C.9) with the angular frequency

$$\omega = 2\pi f. \tag{3.70}$$

The mean square noise voltage can be expressed as

$$v_{neff}^2 = \int_0^\infty v_n^2 df = S_{tot} \tag{3.71}$$

with the total power S_{tot} defined in (C.20). The noise voltage root power spectral density v_n is single-sided and results from

$$v_n = \sqrt{v_n^2}. \tag{3.72}$$

The noise-equivalent signal voltage s_{neq} is

$$s_{neq} = v_{neff}. \tag{3.73}$$

The general definition of the signal-to-noise ratio SNR_{gen} corresponds to the ratio of the signal power to the noise power and results to

$$SNR_{gen} = \frac{P_{signal}}{P_{noise}} = \frac{P_{signal}}{P_{signal\ neq}} \tag{3.74}$$

since

$$P_{noise} = P_{signal\ neq}. \tag{3.75}$$

The units of the signal-to-noise ratio are decibel:

$$\left[SNR_{gen}\big|_{\mathrm{dB}_{gen}}\right] = \mathrm{dB}_{gen}. \tag{3.76}$$

The signal-to-noise ratio in dB_{gen} is calculated by

$$SNR_{gen}\big|_{\mathrm{dB}_{gen}} = 10\log(SNR_{gen}). \tag{3.77}$$

The optical signal-to-noise ratio SNR_{opt} is defined as

$$SNR_{opt} = \frac{P_{opt}}{P_{optneq}} = \frac{s}{s_{neq}} \tag{3.78}$$

since according to (2.11), (3.30) and (2.1)

$$P_{opt} = \frac{i_{ph}}{R_\lambda} = \frac{A\Delta v_a}{T_A \Delta t} \sim s. \tag{3.79}$$

The units of the optical signal-to-noise ratio are dB_{opt}:

$$\left[SNR_{opt}\big|_{\mathrm{dB}_{opt}}\right] = \mathrm{dB}_{opt}. \tag{3.80}$$

The optical signal-to-noise ratio in dB_{opt} is calculated by

$$SNR_{opt}\big|_{\mathrm{dB}_{opt}} = 10\log(SNR_{opt}). \tag{3.81}$$

The electrical signal-to-noise ratio SNR_{el} is defined as

$$SNR_{el} = \frac{P_{el}}{P_{elneq}} = \frac{s^2}{s_{neq}^2} \tag{3.82}$$

since

$$P_{el} = vi = Ri^2 = \frac{v^2}{R} \sim s^2. \tag{3.83}$$

The units of the electrical signal-to-noise ratio are dB_{el}:

$$\left[SNR_{el}\big|_{\mathrm{dB}_{el}}\right] = \mathrm{dB}_{el}. \tag{3.84}$$

The electrical signal-to-noise ratio in dB_{el} results to

$$SNR_{el}\big|_{\mathrm{dB}_{el}} = 10\log(SNR_{el}) = 20\log(SNR_{opt}) = 2SNR_{opt}\big|_{\mathrm{dB}_{opt}} \tag{3.85}$$

[32].
The signal-to-noise ratio SNR in photosensing applications unless stated otherwise is usually the optical signal-to-noise ratio:

$$SNR = SNR_{opt} = \sqrt{SNR_{el}} = \frac{s}{s_{neq}} = \frac{v}{v_{neff}}. \tag{3.86}$$

However, the signal-to-noise ratio in dB is usually the electrical signal-to-noise ratio in dB_{el} and therefore

$$SNR\big|_{\mathrm{dB}} = SNR_{el}\big|_{\mathrm{dB}_{el}} = 2SNR_{opt}\big|_{\mathrm{dB}_{opt}} = 20\log(SNR). \tag{3.87}$$

The correspondence between the different signal-to-noise ratio units is

$$20\text{dB}\hat{=}20\text{dB}_{el}\hat{=}10\text{dB}_{opt}. \tag{3.88}$$

The fundamental noise contributions in integrating sampled-data photosensing as shown in Fig. 3.1 are shot noise, preamplifier thermal noise, voltage amplifier thermal noise, transconductor thermal noise, resistor thermal noise, 1/f noise, ramp ADC thermal noise and quantization noise. They are treated separately in the following paragraphs and then the total noise expressions are given. Due to correlated double sampling no reset noise is considered here, but modeling and estimation of fixed-pattern noise can be found elsewhere [49].

3.4.1 Shot Noise

The charge generation in the photodetector is a stochastic process with Poisson distributed arrival times of the charge carriers thus causing shot noise. Shot noise, sometimes referred to as Poisson or quantum noise, is in general generated by random diffusion of charge carriers through space charge regions and by random generation and recombination of electron-hole pairs. The rms noise in number of photogenerated charge carriers N_{neff} for shot noise is

$$N_{neff} = \sqrt{N_{ph}} = \sqrt{\frac{C_{int}\Delta v_a}{pae}}. \tag{3.89}$$

The noise current power spectral density of shot noise $i^2_{n_{shot}}$ is approximately constant for low frequencies and as single-sided expression is

$$i^2_{n_{shot}} \approx 2ei_{ph} \tag{3.90}$$

[29].
The noise-equivalent photocurrent i_{phneq} according to (3.89) is

$$i_{phneq} = \sqrt{\frac{pae}{C_{int}\Delta v_a}}i_{ph}. \tag{3.91}$$

The signal-to-noise ratio results to

$$SNR = \sqrt{\frac{C_{int}\Delta v_a}{pae}}. \tag{3.92}$$

3.4.2 Preamplifier Thermal Noise

The preamplifier thermal noise is assumed to be dominated by the thermal noise of the input transistors of the preamplifier. If this is not the case the preamplifier thermal noise can be referred to noise-equivalent transistors. The thermal noise or Johnson noise is frequency independent corresponding to white noise. The noise current power spectral density of the drain current of a single transistor $i^2_{n_{transistor}}$ in its single-sided expression is

$$i^2_{n_{transistor}} = 4\alpha kTg_m \tag{3.93}$$

with the transistor noise coefficient α, the Boltzmann constant

$$k = 1.38 \cdot 10^{-23}\ \text{J/K}, \tag{3.94}$$

the Temperature T usually $T = 300$ K and the transconductance of the transistor g_m [50]. The transistor noise coefficient is process and operating point dependent and usually about $\alpha = 1$ [51][52][53].
The noise current power spectral density of the preamplifier $i^2_{n_p}$ in its single-sided expression results to

$$i^2_{n_p} = \frac{n_{CDS}n_p 4\alpha kT}{g_{mp}} 4\pi^2 C^2_{ph} f^2, \tag{3.95}$$

where n_{CDS} is the number of ramp samples per integration measurement, n_p the number of preamplifier noise-equivalent transistors, g_{mp} the transconductance of preamplifier noise-equivalent transistors and C_{ph} the photodetector capacitance

$$C_{ph} = C''_{ph}A. \tag{3.96}$$

C''_{ph} is the specific photodetector capacitance per unit area. n_{CDS} is equal to 2 due to correlated double sampling. n_p is equal to 1 for single-ended and equal to 2 for differential input stages of the preamplifier.
The rms noise current i_{neff} is approximately

$$i_{neff} \approx \frac{2\pi C_{ph}B}{\sqrt{3}} \sqrt{\frac{n_{CDS}n_p 4\alpha kTB}{g_{mp}}} \tag{3.97}$$

according to Appendix C with (C.20) for band-limited white noise (C.26) of the preamplifier. The noise-equivalent photocurrent i_{phneq} is

$$i_{phneq} = \frac{paC_{ph}}{\Delta v_a C_{int}} \sqrt{\frac{n_{CDS}n_p 4\alpha kTB_n}{g_{mp}}} i_{ph} \tag{3.98}$$

and the signal-to-noise ratio results to

$$SNR = \frac{\Delta v_a C_{int}}{paC_{ph}} \sqrt{\frac{g_{mp}}{n_{CDS} n_p 4\alpha k T B_n}}. \tag{3.99}$$

3.4.3 Voltage Amplifier Thermal Noise

Using (3.93) the noise voltage power spectral density of the voltage amplifier $v_{n_a}^2$ yields the single-sided expression

$$v_{n_a}^2 = \frac{n_{CDS} n_a 4\alpha k T}{g_{ma}}, \tag{3.100}$$

where $n_a$is the number of voltage amplifier noise-equivalent transistors and g_{ma} is the transconductance of voltage amplifier noise-equivalent transistors. n_a is equal to 1 for single-ended and equal to 2 for differential input stages of the voltage amplifier.
The rms noise voltage v_{neff} is equal to

$$v_{neff} = \sqrt{\frac{n_{CDS} n_a 4\alpha k T B_n}{g_{ma}}}. \tag{3.101}$$

The noise-equivalent photocurrent i_{phneq} yields

$$i_{phneq} = \frac{a}{\Delta v_a} \sqrt{\frac{n_{CDS} n_a 4\alpha k T B_n}{g_{ma}}} i_{ph} \tag{3.102}$$

and the signal-to-noise ratio results to

$$SNR = \frac{\Delta v_a}{a} \sqrt{\frac{g_{ma}}{n_{CDS} n_a 4\alpha k T B_n}}. \tag{3.103}$$

3.4.4 Transconductor Thermal Noise

According to (3.93) the noise current power spectral density of the transconductor $i_{n_g}^2$ is the single-sided expression

$$i_{n_g}^2 = \frac{n_{CDS} n_g 4\alpha k T}{g_{mg}} g^2, \tag{3.104}$$

where n_g is the number of transconductor noise-equivalent transistors and g_{mg} is the transconductance of transconductor noise-equivalent transistors. n_g is equal to 1 for single-ended and equal to 2 for differential input stages of the transconductor.
The rms noise current i_{neff} is

$$i_{neff} = g\sqrt{\frac{n_{CDS} n_g 4\alpha kTB_n}{g_{mg}}} \tag{3.105}$$

and the noise-equivalent photocurrent i_{phneq} results to

$$i_{phneq} = \frac{a}{\Delta v_a}\sqrt{\frac{n_{CDS} n_g 4\alpha kTB_n}{g_{mg}}} i_{ph}. \tag{3.106}$$

This yields the signal-to-noise ratio

$$SNR = \frac{\Delta v_a}{a}\sqrt{\frac{g_{mg}}{n_{CDS} n_g 4\alpha kTB_n}}. \tag{3.107}$$

3.4.5 Resistor Thermal Noise

The resistor thermal noise or Johnson noise is frequency independent corresponding to white noise [32]. Similar to the transistor thermal noise in (3.93) the noise voltage power spectral density of a resistor $v^2_{n_{resistor}}$ in its single-sided expression is

$$v^2_{n_{resistor}} = 4kTR. \tag{3.108}$$

In this model this yields the noise voltage power spectral density of the resistor $v^2_{n_R}$ as single-sided expression

$$v^2_{n_R} = n_{CDS} 4kTR. \tag{3.109}$$

The rms noise voltage v_{neff} results to

$$v_{neff} = \sqrt{n_{CDS} 4kTRB_n} \tag{3.110}$$

and the noise-equivalent photocurrent i_{phneq} is

$$i_{phneq} = \frac{1}{\Delta v_a}\sqrt{n_{CDS} 4kTRB_n} i_{ph}. \tag{3.111}$$

This yields the signal-to-noise ratio

$$SNR = \Delta v_a \sqrt{\frac{1}{n_{CDS} 4kTRB_n}}. \tag{3.112}$$

3.4.6 1/f Noise

In electronic circuits low-frequency noise whose power spectral density is inversely proportional to the frequency can be observed. This noise is referred to as 1/f noise or flicker noise or contact noise. 1/f noise is a universal phenomenon prevalent in all electronic devices where different materials are in contact; the different "material" may be a vacuum, a different alloy, or a differently doped semiconductor. The number of carriers flowing through, or parallel to, such an interface usually fluctuates due to various mechanisms such as generation-recombination or trapping [54]. Many investigations have been performed on the 1/f noise in MOS transistors and it has been widely observed that the 1/f noise in MOS transistors depends on geometry and bias conditions and is related to the interface states and oxide traps, but the mechanisms involved have not yet been fully understood and no definite theory has been set to account for the diverse experimental results obtained for the different MOS technologies. This means that in order to characterize the 1/f noise, it is necessary to carry out some kind of noise measurements [55]. Therefore in this work a single 1/f noise signal coefficient that has to be experimentally determined is used.

Voltage Ramp ADC

For the voltage ramp ADC the noise voltage power spectral density of 1/f noise $v_{n_f}^2$ can be modeled as single-sided expression

$$v_{n_f}^2 = \frac{N_{vf}}{f} \tag{3.113}$$

with the 1/f noise voltage coefficient N_{vf}, which has to be determined experimentally or from experimental data of the devices. This expression corresponds to the total 1/f noise contribution of the system referred to the amplified voltage at the input of the voltage ramp ADC. For a single transistor the noise voltage power spectral density at its gate can be expressed with (3.113), where the 1/f

noise voltage coefficient of the single transistor $N_{vf_{transistor}}$ is

$$N_{vf_{transistor}} = \frac{K_f}{C''^2_{ox} W L} \tag{3.114}$$

with K_f typically $K_f \approx 10^{-28}$ C^2/m^2 [55][56][32][57]. C''_{ox} is the specific oxide capacitance per unit area of the transistor and W and L are the gate width and length.
This yields an rms noise voltage v_{neff} of

$$v_{neff} \approx \sqrt{N_{vf} \left[1 + 2 \ln \left(2\pi B \Delta t\right)\right]} \tag{3.115}$$

according to appendix C with (C.92) for 1/f noise (C.30) after a first-order low-pass filter and correlated double sampling. The corresponding noise-equivalent photocurrent i_{phneq} of

$$i_{phneq} \approx \frac{1}{\Delta v_a} \sqrt{N_{vf} \left[1 + 2 \ln \left(2\pi B \Delta t\right)\right]} i_{ph} \tag{3.116}$$

results in the signal-to-noise ratio

$$SNR \approx \frac{\Delta v_a}{\sqrt{N_{vf} \left[1 + 2 \ln \left(2\pi B \Delta t\right)\right]}}. \tag{3.117}$$

Current Ramp ADC

For the current ramp ADC the noise current power spectral density of 1/f noise $i^2_{n_f}$ analogous to (3.113) is

$$i^2_{n_f} = \frac{N_{if}}{f} \tag{3.118}$$

with the 1/f noise current coefficient N_{if}. This expression corresponds to the total 1/f noise contribution of the system referred to the integration current at the input of the current ramp ADC. For a single transistor the noise current power spectral density at its drain can be expressed with (3.118), where the 1/f noise current coefficient of the single transistor $N_{if_{transistor}}$ is

$$N_{if_{transistor}} = \frac{g^2_m K_f}{C''^2_{ox} W L} = \frac{2\mu I_D K_f}{C''_{ox} L^2} \tag{3.119}$$

according to (3.114) with the transconductance of the transistor g_m given by

$$g_m = \sqrt{2\mu C''_{ox} \frac{W}{L} I_D} \tag{3.120}$$

and with the mobility μ and the drain current I_D [55].
The rms noise current i_{neff} is

$$i_{neff} \approx \sqrt{N_{if} \left[1 + 2\ln\left(2\pi B \Delta t\right)\right]} \tag{3.121}$$

analogous to (3.115) and the noise-equivalent photocurrent i_{phneq} of

$$i_{phneq} \approx \frac{1}{\Delta i_{int}} \sqrt{N_{if} \left[1 + 2\ln\left(2\pi B \Delta t\right)\right]} i_{ph} \tag{3.122}$$

yields the signal-to-noise ratio

$$SNR \approx \frac{\Delta i_{int}}{\sqrt{N_{if} \left[1 + 2\ln\left(2\pi B \Delta t\right)\right]}}. \tag{3.123}$$

3.4.7 Ramp ADC Thermal Noise

The thermal noise of the ramp ADC in this model is given as an effective noise value since the ramp ADC internally processes the noise with constant bandwidth and therefore yields a constant effective noise.

Voltage Ramp ADC

For the voltage ramp ADC the rms noise voltage v_{neff} is equal to

$$v_{neff} = \sqrt{n_{CDS}} v_{nRADC\,eff} \tag{3.124}$$

where $v_{nRADC\,eff}$ is the ramp ADC input noise voltage.
Assuming first-order low-pass filtered white noise the noise voltage power spectral density $v^2_{n_{RADC}}$ can be determined from the single-sided expression

$$v^2_{n_{RADC}} = \frac{v^2_{nRADC\,eff}}{B_n}. \tag{3.125}$$

The noise-equivalent photocurrent i_{phneq} is given by

$$i_{phneq} = \frac{\sqrt{n_{CDS}} v_{nRADC\,eff}}{\Delta v_a} i_{ph} \tag{3.126}$$

and the signal-to-noise ratio results to

$$SNR = \frac{\Delta v_a}{\sqrt{n_{CDS}} v_{nRADC\,eff}}. \tag{3.127}$$

Current Ramp ADC

For the current ramp ADC the rms noise current $i_{n\,eff}$ analogous to (3.124) is

$$i_{n\,eff} = \sqrt{n_{CDS}} i_{nRADC\,eff} \tag{3.128}$$

with the ramp ADC input noise current $i_{nRADC\,eff}$.
Assuming first-order low-pass filtered white noise the noise current power spectral density $i^2_{n_{RADC}}$ can be determined from the single-sided expression

$$i^2_{n_{RADC}} = \frac{i^2_{nRADC\,eff}}{B_n}. \tag{3.129}$$

The noise-equivalent photocurrent i_{phneq} results to

$$i_{phneq} = \frac{\sqrt{n_{CDS}} i_{nRADC\,eff}}{\Delta i_{int}} i_{ph} \tag{3.130}$$

and the signal-to-noise ratio to

$$SNR = \frac{\Delta i_{int}}{\sqrt{n_{CDS}} i_{nRADC\,eff}}. \tag{3.131}$$

3.4.8 Quantization Noise

Transforming an analog signal into a digital signal with a limited number of discrete values generally changes the value of the initial analog signal since the

analog values are rounded to the closest discrete values thus introducing a quantization error. The quantization error has the character of a random signal and can be considered as quantization noise being added to the initial analog signal. Assuming a uniform distribution of the quantization error, the rms noise in time t_{neff} can be calculated to

$$t_{neff} = \frac{\sqrt{n_{CDS}} t_{res}}{\sqrt{12}}, \tag{3.132}$$

where t_{res} is the timing resolution. The noise-equivalent photocurrent i_{phneq} then is

$$i_{phneq} = \frac{pa\sqrt{n_{CDS}} t_{res}}{\sqrt{12} C_{int} \Delta v_a} i_{ph}^2 \tag{3.133}$$

and the signal-to-noise ratio results to

$$SNR = \frac{\sqrt{12} C_{int} \Delta v_a}{pa\sqrt{n_{CDS}} t_{res}} \frac{1}{i_{ph}}. \tag{3.134}$$

3.4.9 Total Noise

The total noise of the system in this model can be calculated from the single noise contributions introduced in the previous sections. The signal-to-noise ratio of the integration samples at the output of the ramp ADC is principally equal to the signal-to-noise ratio of the ramp signal, although the ramp ADC transfer function may be a non-linear but well defined function such as for the ramp ADC with fixed integration voltage drop. This is shown in detail later in Section 3.7. Assuming zero bias current and no averaging, for the voltage ramp ADC with voltage amplifier the noise-equivalent photocurrent $i_{phneq_{total}}$ totals to

$$i_{phneq_{total}} = \sqrt{\sum_n i_{phneq_n}^2} \qquad , n = shot, p, a, f, RADC, t \tag{3.135}$$

and the resulting signal-to-noise ratio SNR_{total} is

$$SNR_{total} = \frac{1}{\sqrt{\sum_n \frac{1}{SNR_n^2}}} \qquad , n = shot, p, a, f, RADC, t. \tag{3.136}$$

For the voltage ramp ADC with transconductor and resistor the noise-equivalent photocurrent $i_{phneq_{total}}$ totals to

$$i_{phneq_{total}} = \sqrt{\sum_n i^2_{phneq_n}} \qquad , n = shot, p, g, R, f, RADC, t \tag{3.137}$$

and the resulting signal-to-noise ratio SNR_{total} is

$$SNR_{total} = \frac{1}{\sqrt{\sum_n \frac{1}{SNR_n^2}}} \qquad , n = shot, p, g, R, f, RADC, t. \tag{3.138}$$

For the current ramp ADC the noise-equivalent photocurrent $i_{phneq_{total}}$ totals to

$$i_{phneq_{total}} = \sqrt{\sum_n i^2_{phneq_n}} \qquad , n = shot, p, g, f, RADC, t \tag{3.139}$$

and the resulting signal-to-noise ratio SNR_{total} is

$$SNR_{total} = \frac{1}{\sqrt{\sum_n \frac{1}{SNR_n^2}}} \qquad , n = shot, p, g, f, RADC, t. \tag{3.140}$$

Bias Current

In this model the bias current has the same noise behavior as the photocurrent, i.e. I_B shows shot noise. For the photocurrent i_{phb} according to (3.39) the noise-equivalent photocurrent i_{phbneq} then is

$$i_{phbneq} = i_{phneq}, \tag{3.141}$$

and the resulting signal-to-noise ratio SNR_b is determined by

$$SNR_b = SNR\frac{i_{phb}}{I_B + i_{phb}}. \tag{3.142}$$

Averaging

If averaging is applied, the photocurrent i_{phavg} is not changed according to (3.58) and (3.59). But the noise-equivalent photocurrent $i_{phavgneq}$ is reduced to

$$i_{phavgneq} = i_{phneq}\frac{1}{\sqrt{m}} \tag{3.143}$$

and

$$i_{phbavgneq} = i_{phavgneq} = i_{phbneq}\frac{1}{\sqrt{m}} = i_{phneq}\frac{1}{\sqrt{m}} \tag{3.144}$$

respectively. The resulting signal-to-noise ratio SNR_{avg} is

$$SNR_{avg} = SNR\sqrt{m} = SNR\sqrt{\frac{pa\Delta t_{max}}{C_{int}\Delta v_a}}\sqrt{i_{ph}} \tag{3.145}$$

and

$$SNR_{bavg} = SNR_b\sqrt{m} = SNR\sqrt{\frac{pa\Delta t_{max}}{C_{int}\Delta v_a}}\frac{i_{phb}}{\sqrt{I_B + i_{phb}}} \tag{3.146}$$

respectively.

3.5 Performance

The introduced integrating sampled-data photosensing model is implemented in the software tool "PhotoList" described in Appendix E. This tool is used to analyze and to design integrating sampled-data photosensing systems. It is based on parameter identification and provides noise and performance analysis for any integrating sampled-data photosensing system.
The basic performance parameters of a photosensing system are defined in the following sections.

3.5.1 Speed

The speed performance is determined by the measurement time, which is the maximum integration time Δt_{max}. This is the time required to take a measurement sample and therefore represents the sampling period of the incident light. The sampling-limited signal bandwidth B_{ss} according to (2.15) is

$$B_{ss} = \frac{1}{2\Delta t_{max}}. \tag{3.147}$$

Apart from signal bandwidth restrictions, there are spatial and temporal aspects affecting speed performance. If there are long and varying delay times from the incident light to the ADC, different measurement samples may superimpose and produce smear. This can limit the speed performance beyond the limit given in (2.14).

3.5.2 Dynamic Range

Dynamic range DR can be defined as the ratio of the maximum to the minimum signal. Since the optical power density represents the signal, this yields

$$DR = \frac{P''_{optmax}}{P''_{optmin}}. \tag{3.148}$$

The dynamic range in dB is defined as

$$DR\big|_{\mathrm{dB}} = 20\log(DR) \tag{3.149}$$

according to (3.87).

3.5.3 Resolution

Resolution corresponds to the precision a signal can be determined and is represented by the signal-to-noise ratio

$$SNR = \frac{P''_{opt}}{P''_{optneq}} \tag{3.150}$$

as long as absolute accuracy is not regarded. The signal-to-noise ratio in dB is defined in (3.87):

$$SNR\big|_{\mathrm{dB}} = 20\log(SNR). \tag{3.151}$$

3.5.4 Sensitivity

Sensitivity corresponds to the minimum signal change that can be recognized. This is represented by the noise-equivalent optical power density P''_{optneq}.

3.5.5 Chip Area

Chip area A_{chip} is the total area occupied by the circuit in the appropriate technology and can be a crucial factor concerning costs and size.

3.5.6 Power Consumption

Power consumption is characterized by the consumed static power P_{DD} defined as

$$P_{DD} = V_{DD} I_{DD}, \tag{3.152}$$

where V_{DD} is the supply voltage and I_{DD} is the supply current.

3.6 Realization

In this work the circuits are implemented using the AMS $0.6\ \mu$m CMOS process CUX. The supply voltage is $V_{DD} = 5$ V, although some circuits could be operated at much lower voltages. The photodetector area is $A = 30\ \mu\text{m} \times 500\ \mu\text{m}$ for all architectures. In order to gain an impartial comparative analysis of the different architectures, signal integration is performed on separate physical capacitances with a total value of $C_{physical} = 710$ fF for all circuits, independent of the number of integration capacitances. A voltage ramp ADC with fixed integration voltage drop is used exclusively. The amplified voltage drop is $\Delta v_a = 1$ V for all realizations.

3.7 Measurements

3.7.1 Measurement Setup

The setup for the noise measurements of the various realized architectures is shown in Fig. 3.5. The devices-under-test (DUT) are the integrated circuits including the photosensing architectures, which cover the signal conversion from the incident light to the amplified voltage. The integrated circuits are placed in a shielding metal box and adjusted by a microscope. A light emitting diode (LED) which emits at the wavelength $\lambda = 612$ nm is used for illumination through the microscope. The light beam is generated by a pin-hole and the light spot is focussed and adjusted by the microscope.
The control signals for the circuits are generated by a pulse generator. They are further used as trigger signals for the measurement instruments.
The amplified voltage of the integrated circuit is fed to a window comparator built of discrete elements and the time difference between their output pulses is

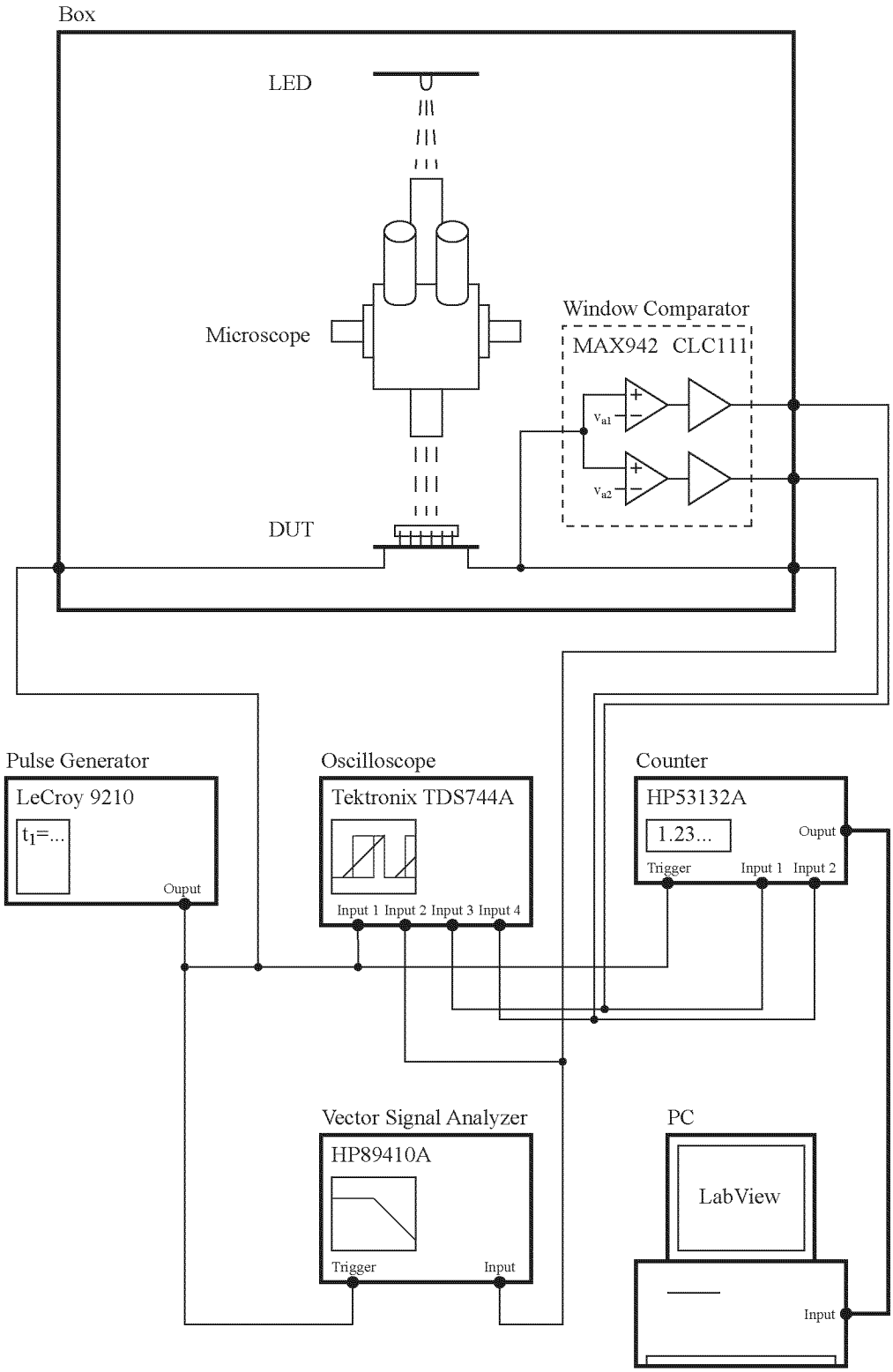


Fig. 3.5: Measurement setup.

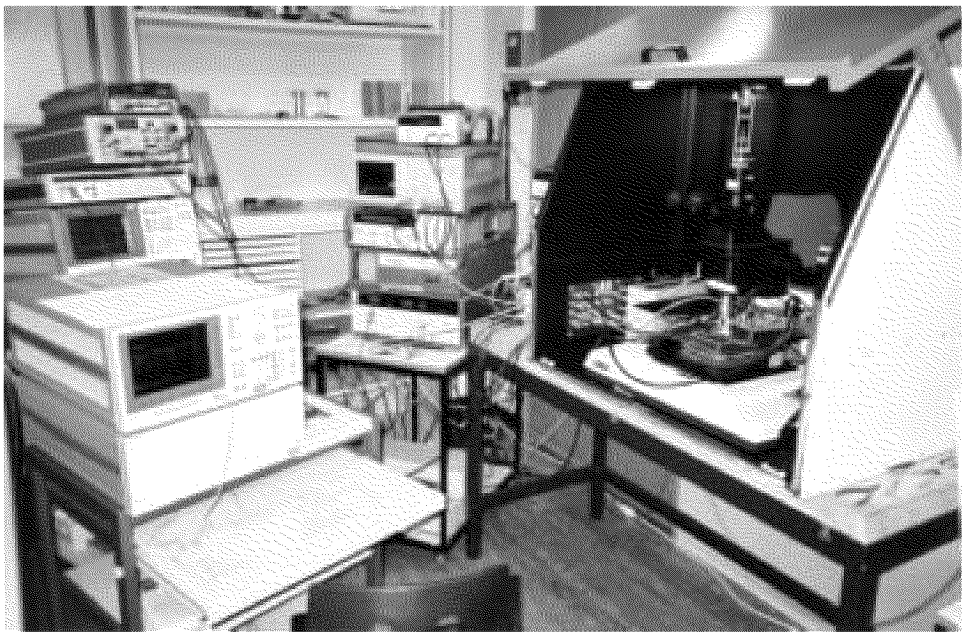


Fig. 3.6: Measurement setup.

measured by a counter. The window comparator circuit together with the counter represents the ramp ADC. The amplified voltage and the output pulses are analyzed by additional instruments, such as an oscilloscope and a vector signal analyzer.
The user interface is realized in LabView running on a PC. The LabView application controls the counter, acquires the data and generates the graphical output. A photograph of the measurement setup is shown in Fig. 3.6.

3.7.2 Performance Extraction

Noise performance of the integrated circuits has to be extracted from the experimental data, which are quantized values of the integration time Δt. Noise is determined from a set of a number N of some hundreds of integration samples Δt_i at constant illumination. The integration time Δt corresponds to the mean value of the set and is extracted by

$$\Delta t = \overline{\Delta t} = \frac{1}{N} \sum_{i=1}^{N} \Delta t_i \tag{3.153}$$

corresponding to (3.65) and (C.1) for the discrete time case. In principle, the rms noise value or effective noise value of the integration time Δt_{neff} is extracted by

$$\Delta t_{neff} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left(\Delta t_i - \overline{\Delta t}\right)^2} \tag{3.154}$$

corresponding to (3.66) and (C.4) for the discrete time case [58]. Instead of the constant mean value for the integration time $\overline{\Delta t}$, a linearly changing value for the integration time can be used corresponding to a line fitted to the set of integration samples according to mean square estimation [59]. This suppresses long-time drift and transients during the measurement.

The effect of a noisy signal on the distribution of the time when this signal first passes a certain level as in the window comparator of the ramp ADC is a very complex topic. It is known in the literature as the level-crossing problem or the first passage time problem and has been investigated intensively not yielding a general and simple expression to be used here [59][60][61]. The noise considerations of the integrating sampled-data photosensing model in Section 3.4 are based on the hypothesis that noise on the signal ramp is transferred into noise in the integration time measurement in the same way the signal itself is transferred. This means that the signal-to-noise ratio of the ramp signal is equal to the signal-to-noise ratio of the integration time measurement. In order to verify this hypothesis and to obtain the relation between the noise of the amplified voltage or voltage ramp and the noise of the integration time or integration sample, a ramp signal with noise in a voltage ramp ADC with fix integration voltage drop is investigated here. First shot noise is considered and a simplified relation is derived valid for high signal-to-noise ratios. Then the relation is simulated for various signal-to-noise ratios for shot noise as well as for first-order low-pass filtered white noise.

In the following a ramp signal with shot noise generated by charge carrier collection is considered and a simplified relation is derived in a way not yet described in the literature to our knowledge: The ramp signal is proportional to the number of collected charge carriers, and since the collected charge carriers are entirely conserved, their number can only increase as shown in Fig. 3.7. Therefore the ramp signal is a monotonously increasing function of time. As a result if the ramp signal at a certain time is lower than the fixed comparator level, it is assured that the ramp signal has not yet crossed the comparator level. On the other hand it is obvious that if the ramp signal at a certain time is higher than the fixed comparator level, it must have crossed the comparator level before. Therefore

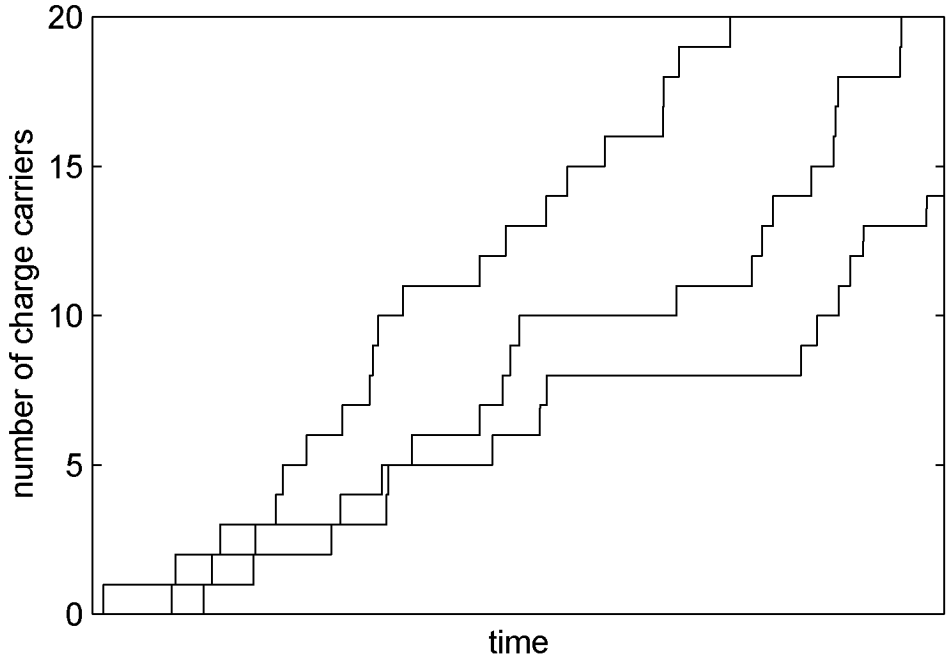


Fig. 3.7: Simulated ramp signals with shot noise generated by charge carrier collection: The number of photogenerated charge carriers n_{ph} is plotted versus the time for three different ramps.

the probability that the ramp signal has crossed the comparator level before a certain time is equal to the probability that the ramp signal at that time is higher than the comparator level. This yields a relation between the distribution and density function of the ramp signal and the level-crossing time. The calculation of the mean values and standard deviations allows to relate the corresponding signal-to-noise ratios.
The charge generation in the photodetector causes shot noise and the probability of the number of photogenerated charge carriers $P[n_{ph} = n]$ is given by the Poisson law [59] with

$$P[n_{ph} = n] = \frac{\mu_n^n e^{-\mu_n}}{n!}. \tag{3.155}$$

as illustrated in Fig. 3.8. μ_n is the mean number of photogenerated charge carriers

$$\mu_n = \lim_{n_t \to \infty} n_t p_n \tag{3.156}$$

resulting from a number of time slots n_t with the probability p_n that a charge carrier occurs in a single time slot. The standard deviation of the number of

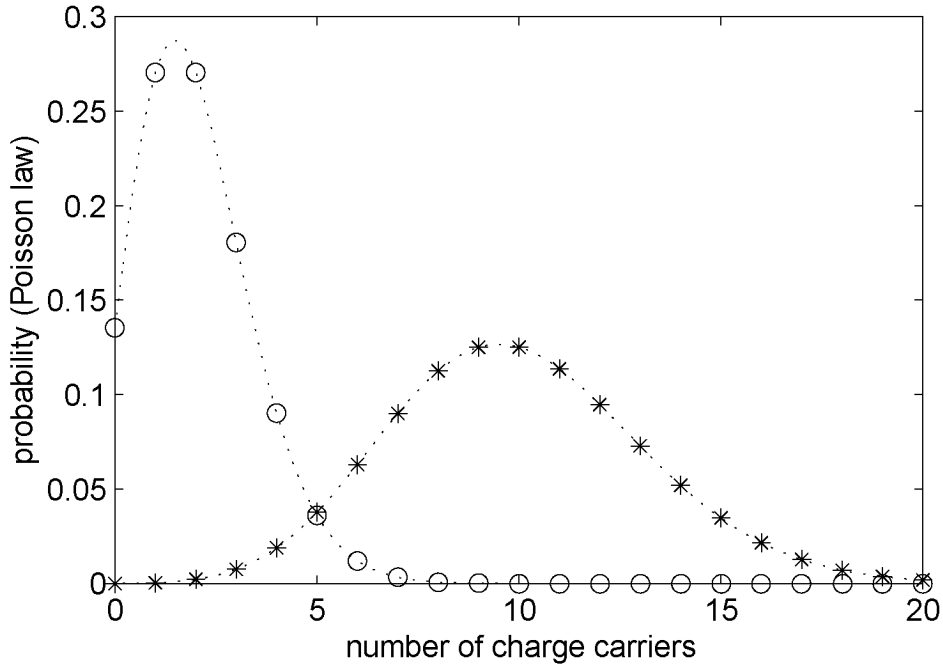


Fig. 3.8: Probability of the number of photogenerated charge carriers $P[n_{ph} = n]$ versus the number of charge carriers n for the Poisson law. The samples correspond to mean numbers of photogenerated charge carriers of 2 (o) and 10 (*).

photogenerated charge carriers σ_n is

$$\sigma_n = \sqrt{\mu_n} \tag{3.157}$$

and the signal-to-noise ratio of the number of photogenerated charge carriers SNR_n results to

$$SNR_n = \frac{\mu_n}{\sigma_n} = \sqrt{\mu_n}. \tag{3.158}$$

For high numbers of photogenerated charge carriers

$$\mu_n > 9 \tag{3.159}$$

the Poisson law can be approximated by the Gaussian law [62] yielding the probability of the number of photogenerated charge carriers

$$P[n_{ph} = n] = \frac{1}{\sqrt{2\pi\mu_n}} e^{-\frac{(n-\mu_n)^2}{2\mu_n}} \tag{3.160}$$

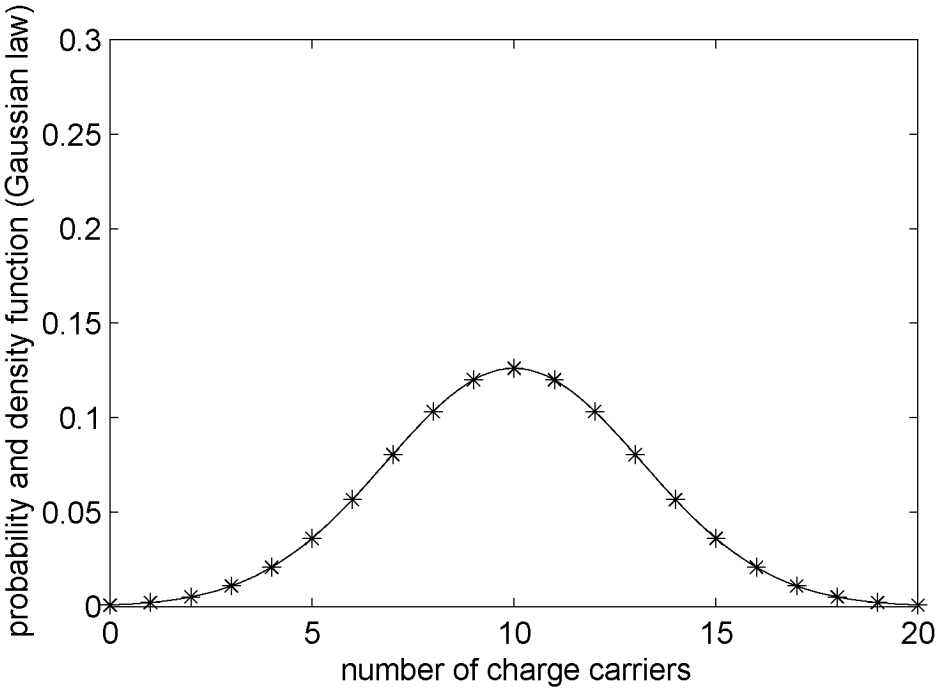


Fig. 3.9: Probability of the number of photogenerated charge carriers $P[n_{ph} = n]$ (*) and density function of the number of photogenerated charge carriers $f_n(n)$ (-) versus the number of charge carriers n for the Gaussian law. The data correspond to a mean number of photogenerated charge carriers of 10.

as illustrated in Fig. 3.9. Considering n to be a continuous variable yields the distribution function of the number of photogenerated charge carriers

$$P[n_{ph} \leq n] = \int_{-\infty}^{n} f_n(n')dn' \tag{3.161}$$

as shown in Fig. 3.10 with the density function of the number of photogenerated charge carriers

$$f_n(n) = \frac{1}{\sqrt{2\pi\mu_n}} e^{-\frac{(n-\mu_n)^2}{2\mu_n}} \tag{3.162}$$

according to Fig. 3.9.
For the corresponding integration voltage v_{int} with

$$v_{int} = \frac{pen_{ph}}{C_{int}} \tag{3.163}$$

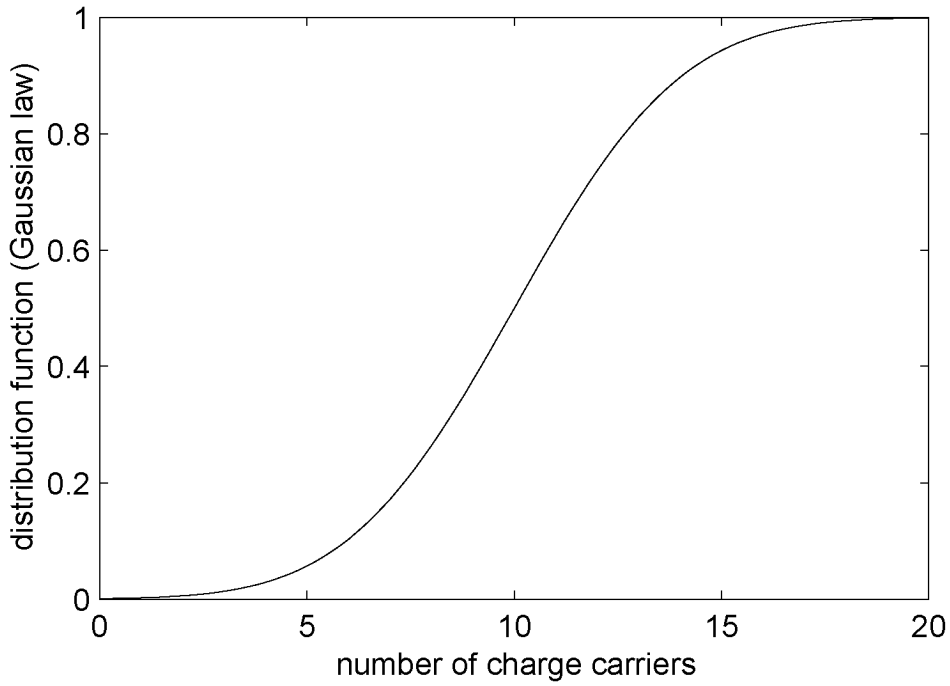


Fig. 3.10: Distribution function of the number of photogenerated charge carriers $P[n_{ph} \leq n]$ versus the number of charge carriers n for the Gaussian law. The curve corresponds to a mean number of photogenerated charge carriers of 10.

consequently the Normal law is valid and yields the distribution function of the integration voltage

$$P[v_{int} \leq v] = \int_{-\infty}^{v} f_v(v')dv' = P\left[n_{ph} \leq \frac{C_{int}v}{pe}\right] \tag{3.164}$$

with the density function of the integration voltage

$$f_v(v) = \frac{1}{\sqrt{2\pi\sigma_v^2}} e^{-\frac{(v-\mu_v)^2}{2\sigma_v^2}}. \tag{3.165}$$

The mean integration voltage μ_v is

$$\mu_v = \frac{pe}{C_{int}}\mu_n \tag{3.166}$$

and the standard deviation of the integration voltage σ_v is

$$\sigma_v = \sqrt{\frac{pe}{C_{int}}\mu_v} = \frac{pe}{C_{int}}\sqrt{\mu_n}. \tag{3.167}$$

According to (3.19) the mean integration voltage μ_v is a linear function of time:

$$\mu_v = \frac{i_p}{C_{int}}t. \tag{3.168}$$

This yields for the time dependent distribution function of the integration voltage

$$P[v_{int} \leq v] = \int_{-\infty}^{v} \frac{1}{\sqrt{2\pi\sigma_v^2}} e^{-\frac{(v'-\frac{i_p}{C_{int}}t)^2}{2\sigma_v^2}} dv'. \tag{3.169}$$

The standard deviation of the integration voltage σ_v is also time dependent and is a linear function of the square-root of time. But for high signal-to-noise ratio the noise on the integration voltage is low compared to the comparator level or integration voltage drop. Therefore the deviations of all the relevant level-crossing times from the integration time for a noise-free ramp signal are relatively small and the standard deviation of the integration voltage in the interesting range is approximately constant:

$$\sigma_v \approx \sqrt{\frac{pe\Delta v_{int}}{C_{int}}}. \tag{3.170}$$

This approximation and setting $v = \Delta v_{int}$ results in

$$\begin{aligned} P[v_{int} \leq \Delta v_{int}] &\approx \int_{-\infty}^{\Delta v_{int}} \frac{1}{\sqrt{2\pi \frac{pe\Delta v_{int}}{C_{int}}}} e^{-\frac{(v' - \frac{i_p}{C_{int}} t)^2}{2\frac{pe\Delta v_{int}}{C_{int}}}} dv' \\ &\approx \int_{t}^{\infty} \frac{1}{\sqrt{2\pi \frac{peC_{int}\Delta v_{int}}{i_p^2}}} e^{-\frac{(t' - \frac{C_{int}\Delta v_{int}}{i_p})^2}{2\frac{peC_{int}\Delta v_{int}}{i_p^2}}} dt'. \end{aligned} \tag{3.171}$$

As explained above the probability that the considered ramp signal has exceeded the integration voltage drop before a certain time is equal to the probability that the integration voltage at that time is higher than the integration voltage drop. Thus the distribution function $P[t_x \leq t]$ of the level-crossing time t_x is

$$P[t_x \leq t] = P[v_{int} > \Delta v_{int}] = 1 - P[v_{int} \leq \Delta v_{int}] \tag{3.172}$$

and the density function $f_t(t)$ of the level-crossing time is

$$f_t(t) = \frac{\partial}{\partial t} \left(P[t_x \leq t] \right) = -\frac{\partial}{\partial t} \left(P[v_{int} \leq \Delta v_{int}] \right). \tag{3.173}$$

Using (3.171) yields

$$f_t(t) \approx \frac{1}{\sqrt{2\pi\sigma_t^2}} e^{-\frac{(t-\mu_t)^2}{2\sigma_t^2}} \tag{3.174}$$

with the mean level-crossing time

$$\mu_t = \frac{C_{int}\Delta v_{int}}{i_p} = \Delta t \tag{3.175}$$

and the standard deviation of the level-crossing time

$$\sigma_t = \frac{\sqrt{peC_{int}\Delta v_{int}}}{i_p}. \tag{3.176}$$

This results in the signal-to-noise ratio of the level-crossing time

$$SNR_t = \frac{\mu_t}{\sigma_t} = \sqrt{\frac{C_{int}\Delta v_{int}}{pe}} = \sqrt{\mu_n} = SNR_n \tag{3.177}$$

according to (3.166), (3.168) at $t = \Delta t$ and (3.19). This means that for high signal-to-noise ratios the ramp ADC converts the ramp signal with shot noise causing a certain signal-to-noise ratio into noise in integration time with the same signal-to-noise ratio. This result supports the hypothesis that shot noise on the signal ramp is transferred into noise in the integration time measurement in the same way the signal itself is transferred.
Fig. 3.11 shows a simulation of the level-crossing problem for a ramp signal with shot noise with a signal-to-noise ratio of $SNR = 20$ dB. The upper diagram shows the distribution of the normalized ramp signal at fixed integration time for a number of photogenerated charge carriers $N_{ph} = 100$. The distribution represents the Poisson law. The corresponding standard deviation of 0.1 is 10 times smaller than the mean value according to the signal-to-noise ratio of shot noise, which is the square root of the number of photogenerated charge carriers. The lower diagram shows the normalized integration time at fixed integration voltage drop. The distribution is similar to the one in the upper diagram and it yields about the same standard deviation thus confirming the result obtained in (3.177).
Fig. 3.12 shows the simulated signal-to-noise ratio of the integration time at fixed integration voltage drop versus the signal-to-noise ratio of the ramp signal at fixed integration time for a ramp signal with shot noise. Fig. 3.13 shows the corresponding simulation for a ramp signal with first-order low-pass filtered white noise with a filter bandwidth of four times the ramp-related bandwidth according to (3.55). The signal-to-noise ratios of the integration time are all approximately equal to the corresponding signal-to-noise ratios of the ramp signal for both shot noise and first-order low-pass filtered white noise. These simulations confirm the hypothesis that noise on the signal ramp is transferred into noise in the integration time measurement in the same way the signal itself is transferred.
It is assumed here that the above hypothesis is valid for 1/f noise as well. 1/f noise can be approximated by a series of first-order low-pass filtered white noise, for which the hypothesis is verified and confirmed by simulations. The verification of the hypothesis for 1/f noise is not carried out here.

3.7.3 Reference Measurement

Fig. 3.14 shows a reference measurement of the measurement setup using a low-noise function generator. The signal-to-noise ratio is plotted for different integration times corresponding to different optical power densities. The different

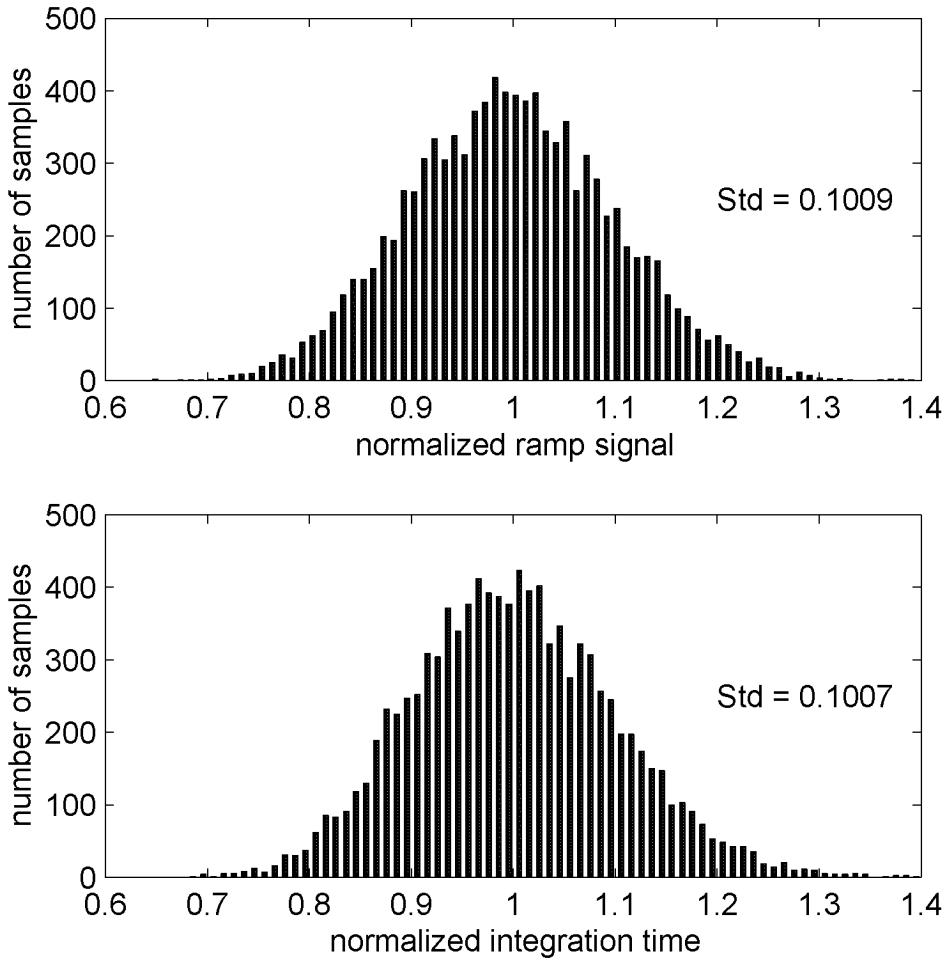


Fig. 3.11: Simulated distribution of the normalized ramp signal at fixed integration time and of the normalized integration time at fixed integration voltage drop for a ramp signal with shot noise. (Number of photogenerated charge carriers $N_{ph} = 100$.)

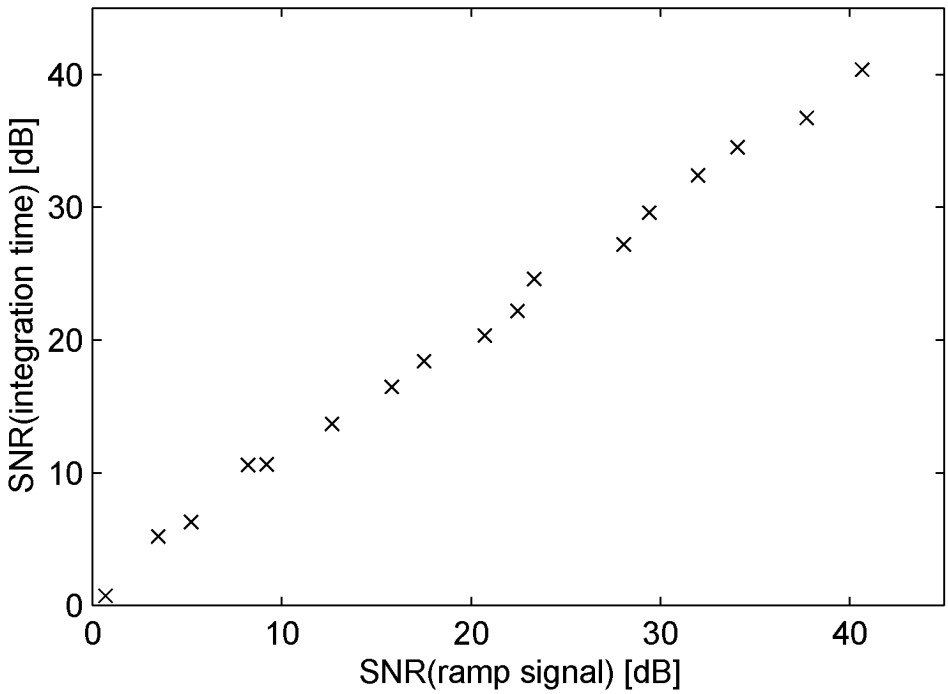


Fig. 3.12: Simulated signal-to-noise ratio of the integration time at fixed integration voltage drop versus the signal-to-noise ratio of the ramp signal at fixed integration time for a ramp signal with shot noise.

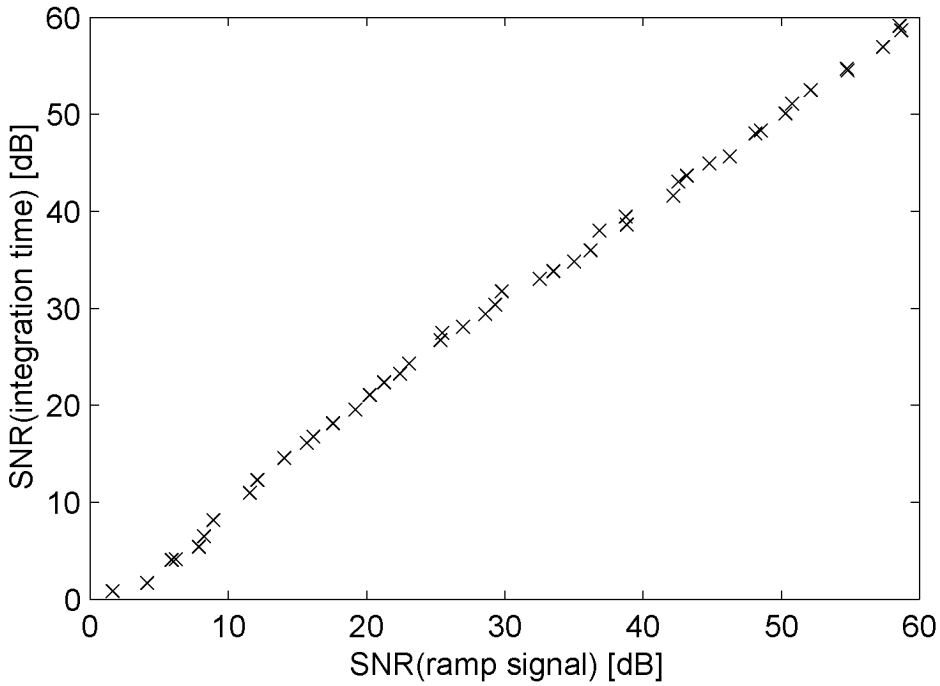


Fig. 3.13: Simulated signal-to-noise ratio of the integration time at fixed integration voltage drop versus the signal-to-noise ratio of the ramp signal at fixed integration time for a ramp signal with first-order low-pass filtered white noise. (The filter bandwidth is four times the ramp-related bandwidth according to (3.55).)

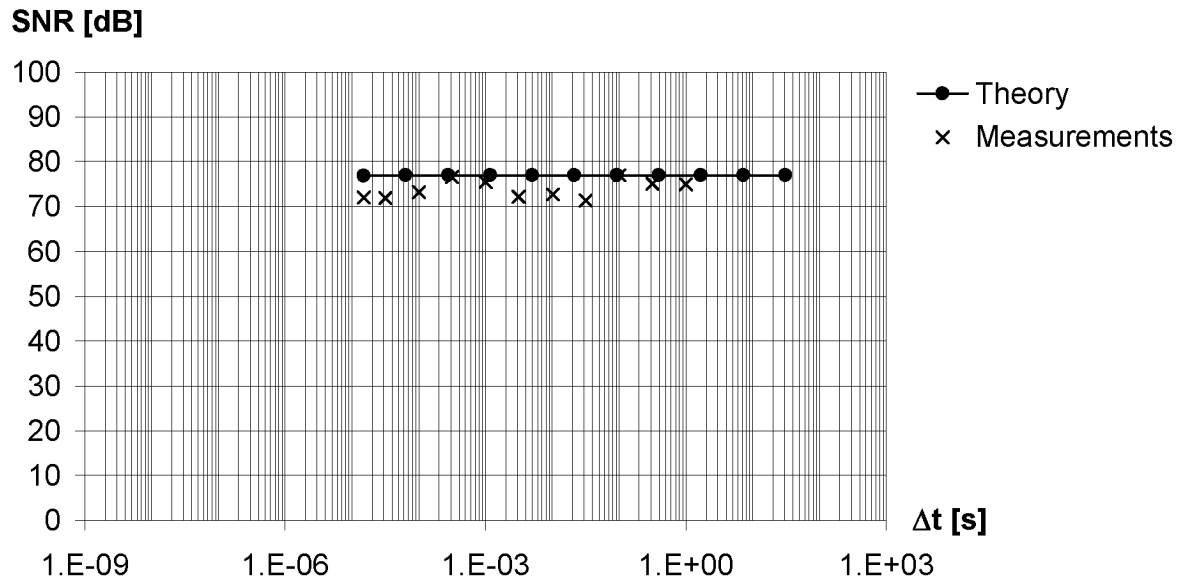


Fig. 3.14: Signal-to-noise ratio of the measurement setup for a low-noise voltage ramp generated by a function generator.

voltage ramps generated by the low-noise function generator yield a constant signal-to-noise ratio of $SNR = 77$ dB, which corresponds to the ramp ADC thermal noise with a ramp ADC input noise voltage of about $100\ \mu$V. This means that noise measurements up to a signal-to-noise ratio of 77 dB can be performed with this setup.

3.7.4 Line Interferences

Although the measurements are performed in a shielding metal box, they are disturbed by line interferences. These disturbances are fed into the circuits either via the power supplies due to insufficient suppression and blocking or via signal cables and through the air directly to critical high-impedance nodes. Fig. 3.15 shows SNR measurements of the photodiode with active integrator, which is discussed in the next chapter, with different levels of line interferences. The interference level is adjusted by a power cable that can be placed near the critical circuit part inside the shielding metal box. The theoretical signal-to-noise ratio of $SNR = 61$ dB for a photodetector capacitance of 20 pF is drastically reduced in certain regions due to the line interferences.

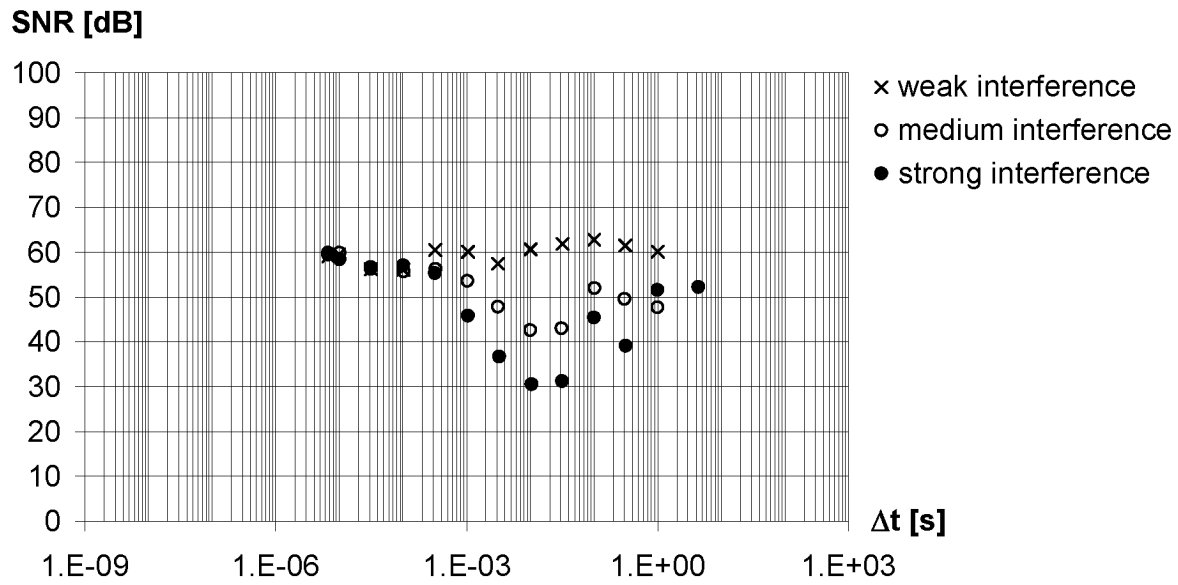


Fig. 3.15: Measured signal-to-noise ratio of a photodiode with active integrator (section 5.1) with different levels of line interference.

Line interferences are sinusoidal signals at 50 Hz frequency of the power line. They are particularly effective for integration times in the range of the period of the power line due to the window comparator measurement principle. For such integration times the line interference causes significant differences in the two ramp samples that yield an integration sample and thus introduces an error. For integration times much shorter than the period of the power line the line interferences represent some kind of offset and are cancelled by the window comparator. For very long integration times the window comparator just measures the envelope of the line interference, which is constant and therefore cancelled like an offset. This is confirmed by the simulation shown in Fig. 3.16. The signal-to-noise ratio for a ramp signal with constant noise level and superimposed line interference is plotted versus the integration time and results in a curve very similar to the measurements in Fig. 3.15.

3.8 Conclusions

The introduced generic model for integrating sampled-data photosensing fundamentally consists of a photocurrent source, an integrating analog-to-digital

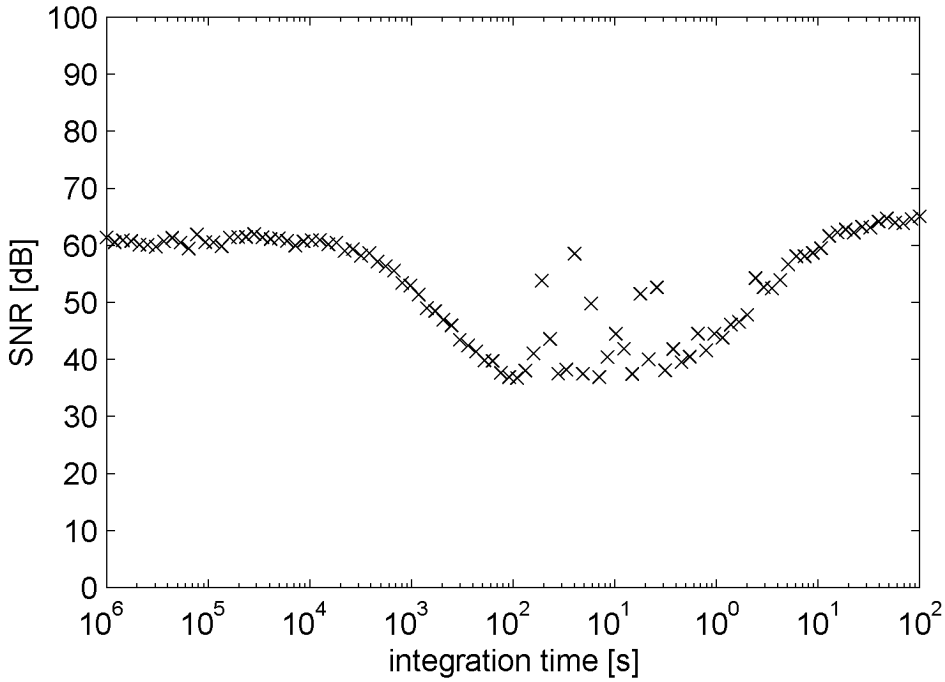


Fig. 3.16: Simulated signal-to-noise ratio for a ramp signal with constant noise level and superimposed line interference.

converter and a digital signal processor. It fits for any integrating sampled-data photosensing system and the developed software tool provides appropriate noise and performance analysis. Model fitting is based on parameter identification in the physical system for all the fundamental functional blocks of the model.
The proposed ramp ADC with fixed integration voltage drop is a simple and area-efficient technique for analog-to-digital conversion of ramp signals well-suited for photosensing applications. It provides simple implementation of correlated double sampling. Noise on the signal ramp is principally transferred into noise in the integration time measurement in the same way the signal itself is transferred. The suitability of this ramp ADC for high-speed applications is limited because the timing resolution of the appropriate counter basically determines the dynamic range and highly affects the signal resolution. Nevertheless, the resolution at high signal levels can be enhanced by averaging, as the integration time under these circumstances becomes much shorter than the measurement time.
The use of a bias current in the proposed circuit can expand the dynamic range by decades while still meeting specific timing constraints. If the bias current is set to the initial minimum photocurrent, the dynamic range is extended by ap-

proximately the signal-to-noise ratio of the bias current.
The analog bandwidth of the system must be limited by a low-pass filter to four times the ramp-related bandwidth in order to minimize the noise contributions and yet to guarantee proper ramp signals.
Correlated double sampling is mandatory for high-precision applications. It removes offsets introduced by switches as well as reset noise, and it reduces low-frequency noise such as 1/f noise. The effect of correlated double sampling on first-order low-pass filtered 1/f noise can be approximated by a simple expression.
For integration times much shorter than the measurement time, averaging can be applied to enhance the resolution by the square root of the number of integration samples per measurement sample.
High resolution basically requires low photodetector capacitance to reduce the contribution of the preamplifier thermal noise. High resolution without averaging requires high virtual integration capacitance to enhance the shot noise limit, as this yields long measurement time and therefore a high number of photogenerated charge carriers.
The transfer factor depends on the responsivity and the virtual integration capacitance and directly determines the speed of the system. Very high speed as well as very high sensitivity demand very high transfer factor, as the ramp signal always has to cover a full signal drop in the specified measurement time for detection. Very high transfer factor for a certain responsivity requires very low virtual integration capacitance, which can be achieved by very low integration capacitance or very high preamplifier or voltage amplifier gain.
The measurement setup basically provides signal-to-noise ratio measurements of 77 dB, but line interferences degrade the resolution for integration times in the range of the period of the power line.

4. BASIC PHOTODETECTORS

This chapter analyzes the basic photodetector structures realizable in CMOS technology. The different basic photodetectors in standard CMOS technology are realized and characterized. They are compared with respect to different key performance issues. Special emphasis is given on responsivity and photodetector capacitance.

4.1 Photodiode (PD)

The most common photodetector in CMOS technology is the photodiode as shown in Fig. 4.1. It is an ordinary pn junction operated in zero or reverse bias condition causing a space charge region with a built-in electric field as calculated in Appendix B. This electric field provides charge transport and a photocurrent results at the photodiode terminals. The anode is the terminal at the p-side and the cathode is the one at the n-side of the junction.
There are principally four types of photodiodes realizable in the AMS 0.6 μm CMOS process CUX as shown in Fig. 4.2. The p-diffusion/n-well diode with

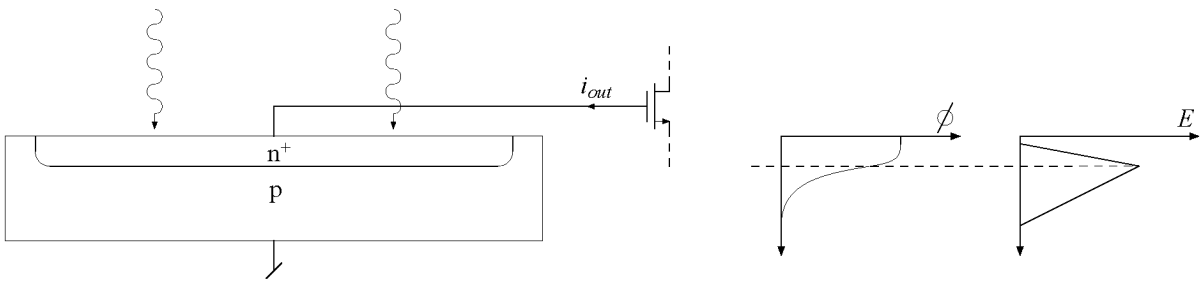
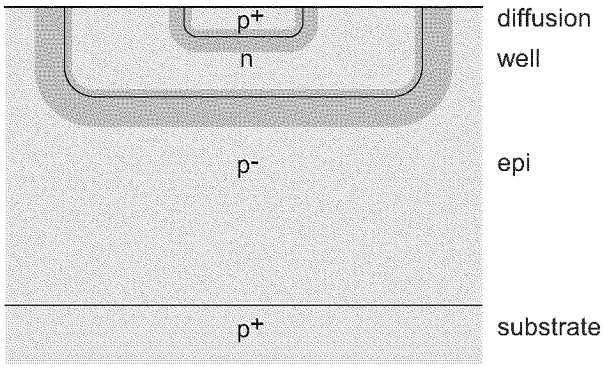


Fig. 4.1: Photodiode. Cross section and distribution of the potential ϕ and the electric field E in vertical direction.

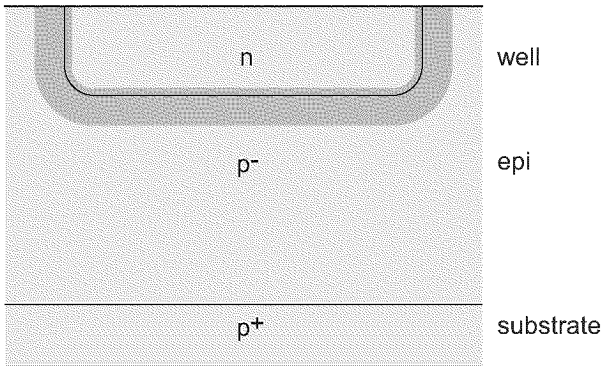
heavily doped p-side and moderately doped n-side is realized by contacting the p-diffusion and the n-well in Fig. 4.2a. The photodiode terminal voltages can be chosen freely, but the photocurrent is only available at the anode, since the current at the cathode includes the current flowing to the substrate. Fig. 4.2b shows the p-substrate/n-well diode with lightly doped p-side and moderately doped n-side. Since the anode is connected to ground the voltage applied to the cathode is directly the reverse voltage and the photocurrent is only available at this terminal. Another photodiode type is the combination of the p-diffusion/n-well diode and the p-substrate/n-well diode as shown in Fig. 4.2a. Here still the anode of the p-substrate/n-well diode is connected to ground though the voltage at the anode of the p-diffusion/n-well diode can be chosen freely. The photocurrent is available only at the cathode. The last photodiode type shown in Fig. 4.2c is the p-substrate/n-diffusion diode. It is a two-step junction with a lower junction of two lightly and moderately doped p-type layers and with an upper junction with moderately doped p-side and heavily doped n-side. The anode is connected to ground and the photocurrent is only available at the cathode, where the reverse voltage is applied.

The responsivity of a photodetector is directly related to its quantum efficiency according to (2.12). There are schemes that allow to determine the quantum efficiency as a function of the wavelength of the incident light and the structural parameters of the photodiode [31]. But because the quantum efficiency is a complex function of process technology and the physical layout of the photodiode, in general it cannot be determined accurately in an analytical way or using simulation, and it usually has to be measured [63]. Fig. 4.3 shows the measured spectral quantum efficiency of the p-diffusion/n-well photodiode (pw), the p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode (pw+sw), the p-substrate/n-well photodiode (sw) and the p-substrate/n-diffusion photodiode (sn). The additional curve at the bottom corresponds to the minimum value of the measurement current of 0.5 pA thus indicating the resolution of the measurement setup. Data below this curve are not reliable.

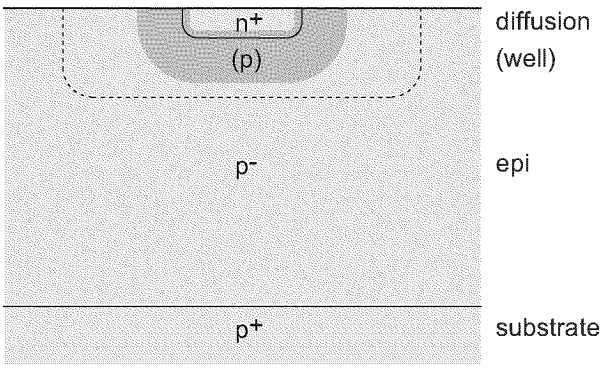
The diffusion lengths of the charge carriers in the different layers strongly vary due to the different doping levels. The p-diffusion and the n-diffusion have doping concentrations of about $4 \cdot 10^{20}$ cm^{-3} and yield diffusion lengths of less than 0.1 μm. The p-well and the n-well with doping concentrations of about $6 \cdot 10^{16}$ cm^{-3} achieve diffusion lengths in the range of 100 μm. In the epi-layer the doping concentration is about $7 \cdot 10^{14}$ cm^{-3} and the diffusion length is about 1000 μm. The substrate has a doping concentration of about $1 \cdot 10^{20}$ cm^{-3} and yields a diffusion length of less than 1 μm. In comparison the depth of the dif-



(a)



(b)



(c)

Fig. 4.2: Photodiode types in the AMS 0.6 μm CMOS process CUX. (a) p-diffusion/n-well diode in combination with p-substrate/n-well diode. (b) p-substrate/n-well diode. (c) p-substrate/n-diffusion diode.

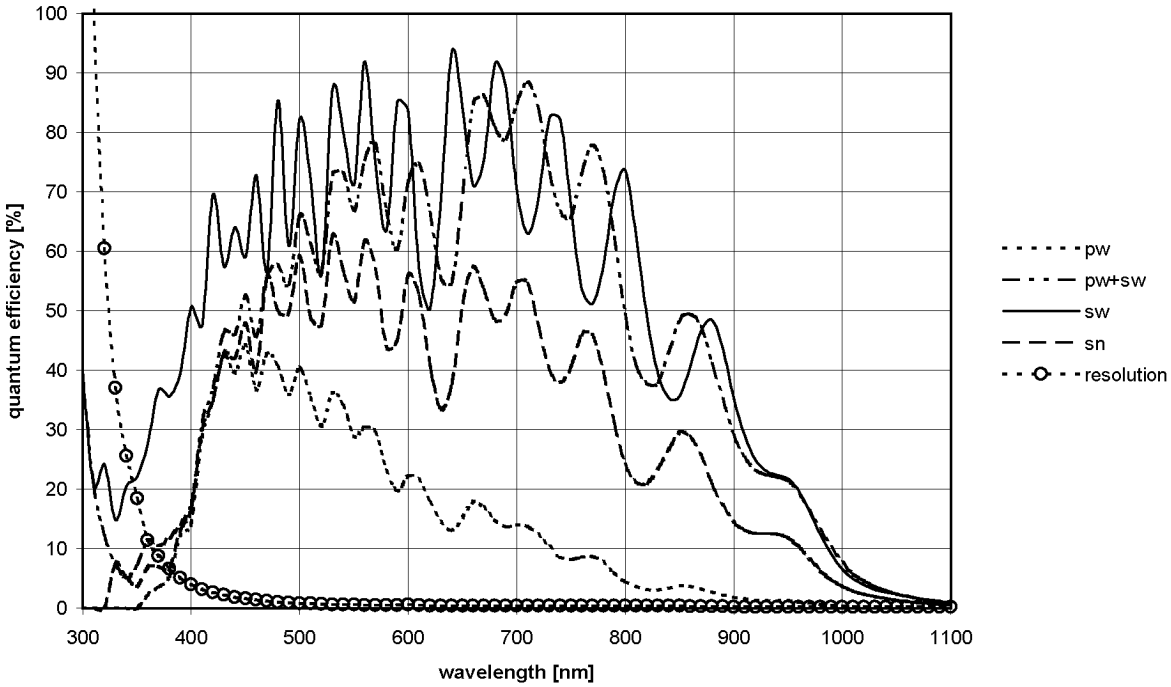


Fig. 4.3: Measured spectral quantum efficiency of the different photodiodes. (pw) p-diffusion/n-well photodiode. (pw+sw) p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode. (sw) p-substrate/n-well photodiode. (sn) p-substrate/n-diffusion photodiode. (o) resolution of the measurement setup.

fusions is about $0.3\ \mu$m and that of the wells about $2.5\ \mu$m. The thickness of the epi-layer below the wells is about $15\ \mu$m.
The p-substrate/n-well photodiode achieves the highest quantum efficiency over the whole wavelength range. This is because the junction is deep in the semiconductor due to the high n-well depth and because of the high space charge region width due to the low doping levels according to (B.30). In addition the diffusion lengths are high according to (B.26) due to the long carrier lifetimes resulting from the low doping levels.
The p-diffusion/n-well photodiode in combination with the p-substrate/n-well photodiode achieves about the same quantum efficiency as the p-substrate/n-well photodiode at long wavelengths. This is because for high light penetration depths corresponding to long wavelengths the p-substrate/n-well photodiode generates the photocurrent. At short wavelength the quantum efficiency is considerably lower than for the p-substrate/n-well photodiode because the diffusion length in the highly doped p-diffusion near the surface is very low.
The p-substrate/n-diffusion photodiode yields reduced quantum efficiency compared to the p-substrate/n-well photodiode over the whole wavelength range. This is because the junction is near the surface and because of the lower space charge region width as well as the lower diffusion lengths due to the higher doping levels.
The p-diffusion/n-well photodiode achieves the lowest quantum efficiency. For short wavelengths it yields about the same quantum efficiency as the p-diffusion/n-well photodiode in combination with the p-substrate/n-well photodiode and as the p-substrate/n-diffusion photodiode due to the equal structure and doping levels. For longer wavelengths it yields considerably reduced quantum efficiency since at high light penetration depth the photogenerated charge is captured by the p-diffusion/n-well diode that is not used for detection.
The oscillations in the quantum efficiency over the spectral range is caused by interferences in the different layers, particularly the oxide layers and the protection layers [64].
The photodetector capacitances and leakage currents of the different photodiodes are discussed in the next chapter.

4.2 Photogate (MOS Photodetector, PG)

Another basic photodetector in CMOS technology is the photogate or MOS photodetector as shown in Fig. 4.4. It is an MOS structure operated in inversion with

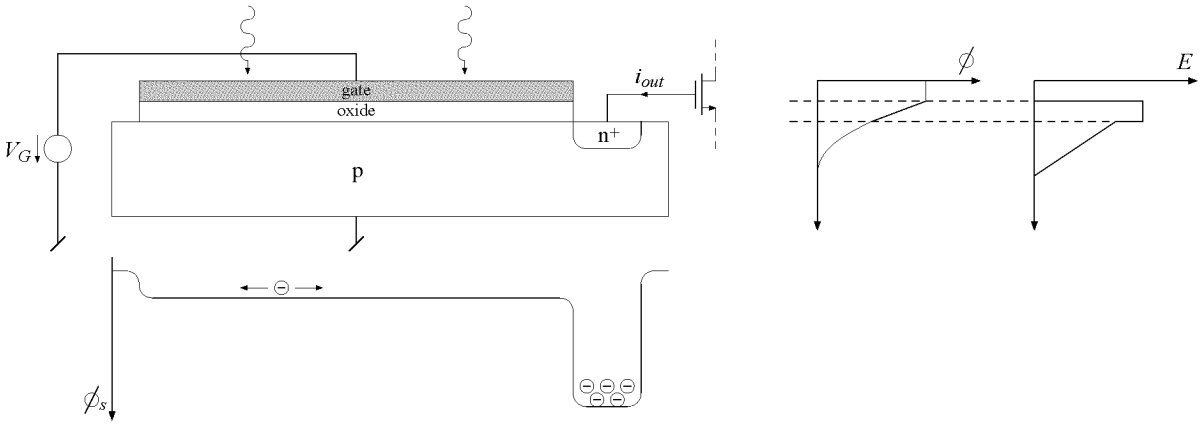


Fig. 4.4: Photogate (PG). Cross section, distribution of the potential ϕ and the electric field E, and surface potential profile ϕ_s.

an adjacent floating diffusion, which is a small p-substrate/n-diffusion diode. The MOS structure causes a depletion region or space charge region in the semiconductor with an electric field as calculated in Appendix B. This electric field provides charge transport in the semiconductor perpendicular to the surface and collects the charge in a thin inversion layer at the surface. The charge in the inversion layer is transported by diffusion to the p-substrate/n-diffusion diode and a photocurrent results at the cathode of the diode or floating diffusion. The surface potential profile in Fig. 4.4 illustrates that the MOS structure forms a potential well at the surface of the semiconductor according to the applied gate voltage. The potential well is a local maximum of surface potential and represents a local minimum of charge carrier energy. The adjacent floating diffusion is biased at high voltage and represents a very deep potential well. As a result the charge carriers at the surface in the MOS structure are transported only by diffusion and they are captured by the floating diffusion once they get there.
In the AMS $0.6\ \mu$m CMOS process CUX the semiconductor in the MOS structure is the moderately doped p-well. The floating diffusion is a p-substrate/n-diffusion diode with moderately doped p-side and heavily doped n-side. The anode is connected to ground and the photocurrent is only available at the cathode, where the reverse voltage of the diode is applied. The whole photogate is not a standard device in this technology, but it can be implemented without changes in the standard technology, although the common design rules may have to be violated.
Fig. 4.5 shows the measured spectral quantum efficiency of the photogate. The

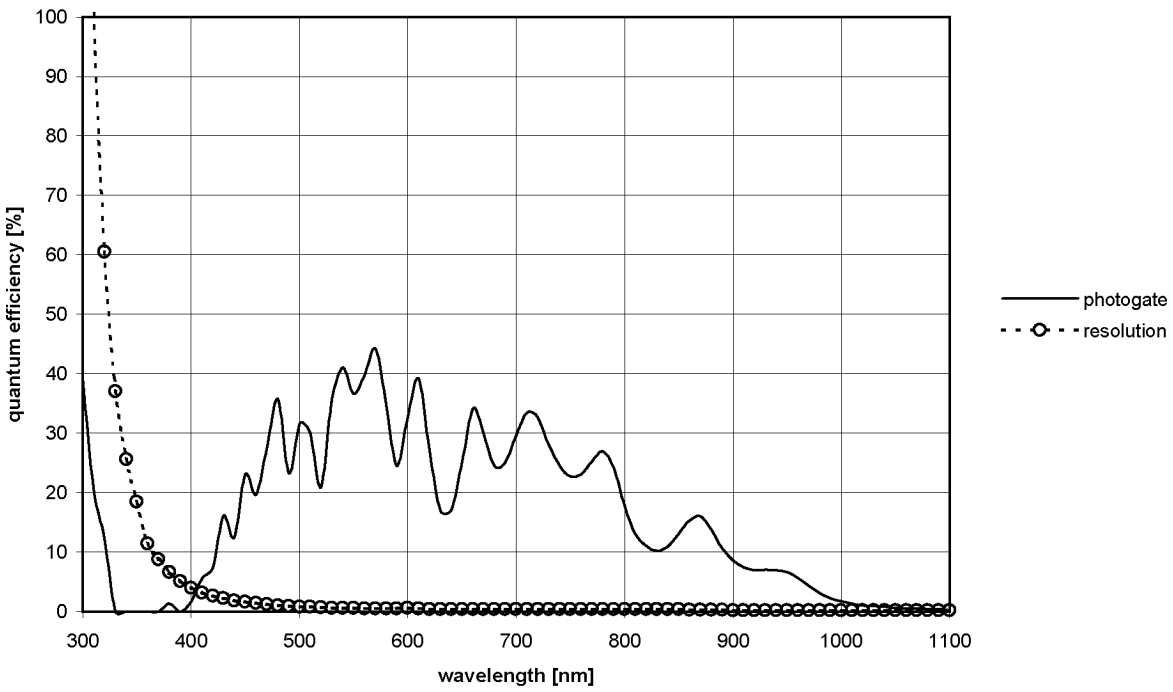


Fig. 4.5: Measured spectral quantum efficiency of the photogate (PG). (o) resolution of the measurement setup.

additional curve at the bottom corresponds to the minimum value of the measurement current of 0.5 pA thus indicating the resolution of the measurement setup. Data below this curve are not reliable.
The light penetration depths in the photogate are strongly affected by the overlaying polysilicon gate, which has a thickness of about 0.25 μm.
The photogate yields a quantum efficiency at small wavelengths lower than all the photodiodes due to the absorption in the overlaying gate. For longer wavelengths the quantum efficiency is higher than that of the p-diffusion/n-well photodiode but still lower than that of all the other photodiodes.
The photodetector capacitance depends on the area of the junction and the voltage across the junction used for detection. The photodetector capacitance of the different basic photodetectors versus the voltage across the sensing diode in reverse direction is plotted in Fig. 4.6. From the junctions with large area of 30 μm $\times$ 500 μm, the p-diffusion/n-well photodiode yields a higher and the p-substrate/n-well photodiode a lower photodetector capacitance than the p-substrate/n-diffusion photodiode. The photodetector capacitance of the p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode

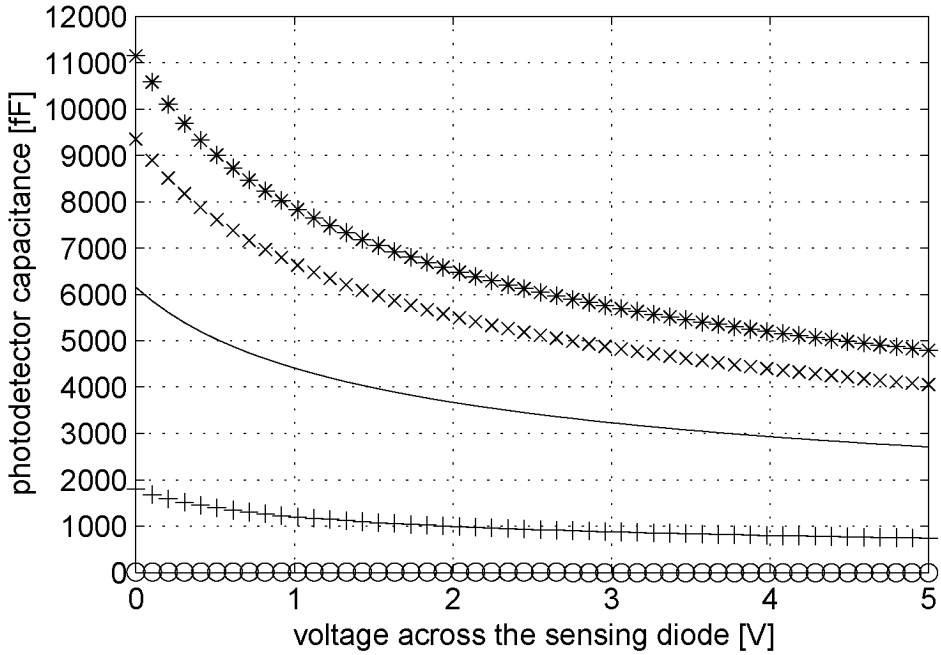


Fig. 4.6: Photodetector capacitance of the different basic photodetectors versus voltage across the sensing diode in reverse direction. (x) p-diffusion/n-well photodiode. (*) p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode. (+) p-substrate/n-well photodiode. (-) p-substrate/n-diffusion photodiode. (o) p-substrate/n-diffusion sensing diode of the photogate.

is about the sum of the two separate photodetector capacitances. The photogate with its very small p-substrate/n-diffusion sensing diode has very low photodetector capacitance. The dependence of the photodetector capacitances on the voltage across the sensing diode is clearly illustrated. The photodetector capacitance at a voltage of 5 V across the sensing diode may be less than half of that at zero voltage.

Fig. 4.7 shows the photodetector capacitance of the different basic photodetectors at zero voltage versus photodetector area. The photodetector area is expressed in the edge length of the photodetector assuming a square shape. The photodetector capacitances of the photodiodes increase about with the square of the edge length, whereas the photodetector capacitance of the photogate has very low constant value.

The photodetector leakage current as well depends on the area of the junction and the voltage across the junction used for detection. It is approximately zero at zero voltage and increases with increasing reverse voltage. The photodetec-

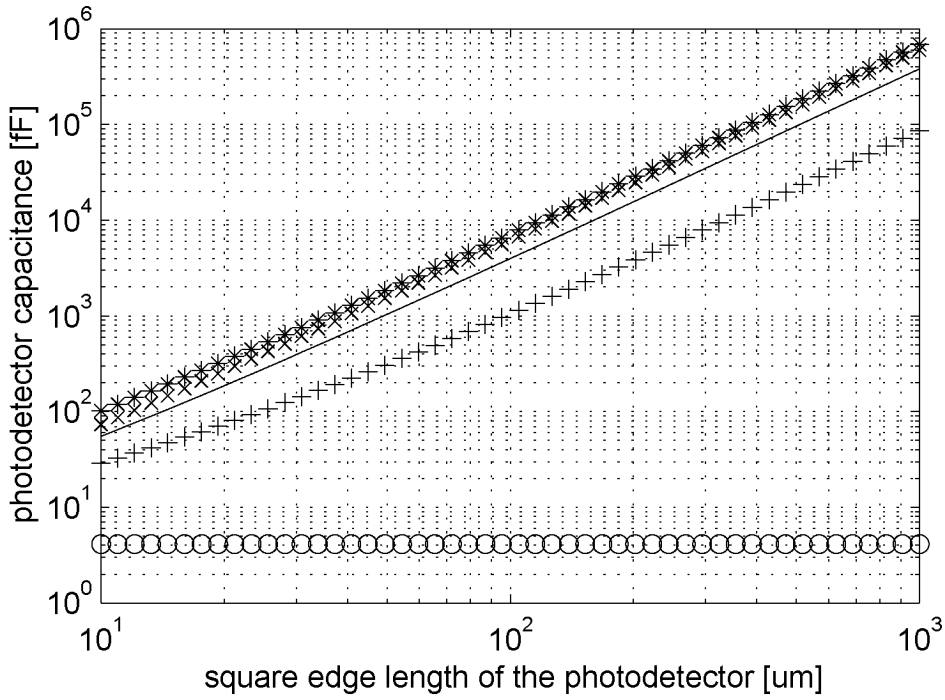


Fig. 4.7: Photodetector capacitance of the different basic photodetectors at zero voltage versus area expressed in square edge length of the photodetector. (x) p-diffusion/n-well photodiode. (*) p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode. (+) p-substrate/n-well photodiode. (-) p-substrate/n-diffusion photodiode. (o) p-substrate/n-diffusion sensing diode of the photogate.

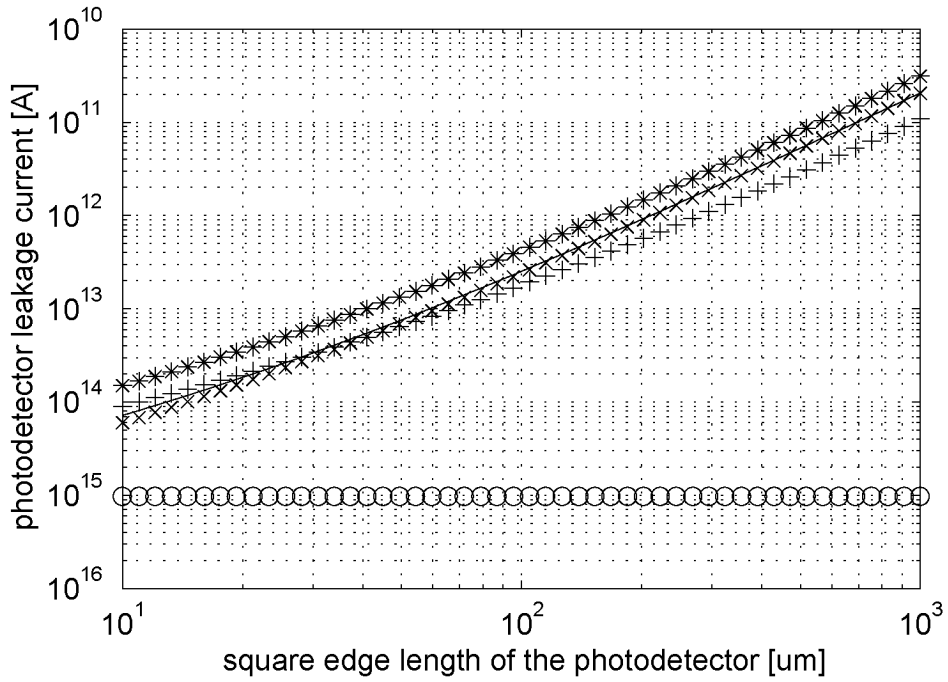


Fig. 4.8: Photodetector leakage current of the different basic photodetectors at 5 V reverse voltage versus area expressed in square edge length of the photodetector. (x) p-diffusion/n-well photodiode. (*) p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode. (+) p-substrate/n-well photodiode. (-) p-substrate/n-diffusion photodiode. (o) p-substrate/n-diffusion sensing diode of the photogate.

tor leakage current of the different basic photodetectors at 5 V reverse voltage versus photodetector area is plotted in Fig. 4.8. The photodetector area is expressed in the edge length of the photodetector assuming a square shape. Analogous to the photodetector capacitances, the photodetector leakage currents of the photodiodes increase about with the square of the edge length, whereas the photodetector leakage current of the photogate has very low constant value.

4.3 Conclusions

The basic photodetectors in standard CMOS technology are the photodiode and the photogate. There are principally three different pn junctions that can serve as photodiode individually or in combination.
The p-substrate/n-well photodiode achieves the highest responsivity over the

whole wavelength range, but it yields a high photodetector capacitance and the anode is inherently grounded.
The p-diffusion/n-well photodiode allows variable terminal voltages, but its responsivity is strongly reduced and it still yields a high photodetector capacitance.
The photogate yields a very low photodetector capacitance independent of its area, although it has reduced responsivity and is especially inefficient in the lower visible wavelength range corresponding to blue light. It is slower than the photodiodes and its speed depends on its area, as the dominant charge transport is driven by lateral diffusion.
Because of its low photodetector capacitance and despite of its reduced responsivity the photogate can be superior to the photodiodes in applications where preamplifier thermal noise is dominant.

5. BASIC PHOTOSENSING ARCHITECTURES

In this chapter the basic photosensing architectures realizable in CMOS technology are classified considering the basic photodetectors with respect to their area and their array arrangement. The various architectures are analyzed and their performance is derived using the integrating sampled-data photosensing model. The realizations of the different basic photosensing architectures in the same standard CMOS technology are characterized under equivalent conditions and all the relevant parameters of the integrating sampled-data photosensing model are measured for each architecture. The realizations are compared and the architectures with best performance with respect to speed, dynamic range, resolution, sensitivity, area and power consumption are determined. As a result of these characterizations the qualitative and quantitative noise behavior of the integrating sampled-data photosensing model is experimentally verified.

5.1 Single Detector Architectures

Single detector architectures in large-area photosensing have a single detector per photosensing area, which is a large area of homogeneous illumination. Arrangements with spatial resolution using an array of such photosensing areas each having large area and homogeneous illumination are still referred to as single detector architectures, since each pixel represents a large-area photosensing architecture by itself.

A traditional photosensing architecture is the photodiode with transimpedance amplifier. It is not an integrating architecture but it is included in this work for completeness and for comparison due to its wide use.

The basic single detector photosensing architectures for integrating sampled-

data photosensing are characterized by the type of photodetector and the type of integrator. The basic photodetectors are the photodiode and the photogate. The basic integrators are the passive and the active integrator [65][66]. The passive integrator is a simple capacitance that integrates the input current without any feedback thus affecting the input voltage [67]. The active integrator is a feedback circuit with a capacitance and an amplifier that integrates the input current and keeps the input voltage at a defined value. The combination of the two basic photodetectors and the two basic integrators yields four basic photosensing architectures.
The active integrator is often referred to as charge amplifier. It can be operated in the recharge mode, where the photocurrent is integrated on the photodetector capacitance. At the end of the integration time the photodetector capacitance is recharged and the recharge current is instantly integrated on the active integrator thus yielding an output voltage corresponding to the photogenerated charge [65].
The photodiode architectures are realized using the p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode. The photocurrent is taken from the cathode. Other photodiode types can be used accordingly. However for the p-diffusion/n-well photodiode the photocurrent has to be taken from the anode thus having reverse direction, but this can be realized analogously. The voltage across the photodiode in the actual realization is only zero for equal anode and cathode voltages of 0 V since the p-substrate/n-well diode with permanently grounded anode is part of the photodiode.
The parameters of the realized architectures according to the integrating sampled-data photosensing model are given in Appendix G.

5.1.1 Photodiode with Transimpedance Amplifier (PD+TIA)

The photodiode with transimpedance amplifier is shown in Fig. 5.1. The photocurrent of the photodiode D_1 is converted into the continuous-time voltage V_O by resistor R_1. This signal-dependent voltage has to be sampled and converted by a voltage analog-to-digital converter in order to get the measurement samples. This is a non-integrating sampled-data photosensing technique that is based on a continuous-time concept. It is often employed in discrete component circuits with either moderate resistor values requiring high photocurrents or with very high resistor values at very low analog bandwidth for noise reduction [68].
This architecture is not suitable for integration in CMOS technology because there are no structures available that offer appropriate resistors with the required

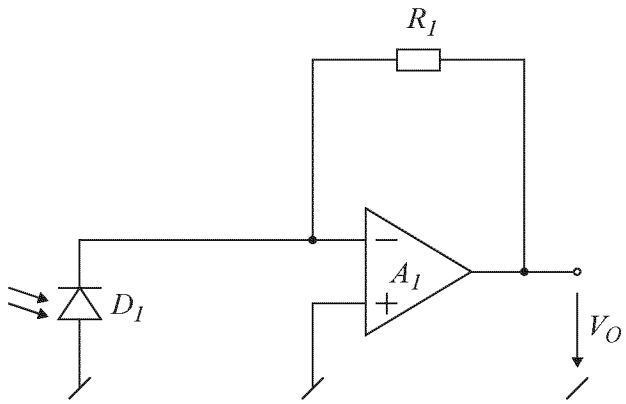


Fig. 5.1: Photodiode with transimpedance amplifier (PD+TIA).

very high values.
A related architecture that is realizable in CMOS technology uses a transistor in resistor configuration, i.e. a transistor with shorted gate and drain [69]. For low photocurrents the transistor operates in weak inversion and yields high resistor values with a logarithmic relation between current and voltage. This architecture is basically a continuous time circuit but differs from the standard configuration in Fig. 5.1 due to the logarithmic resistor transfer characteristics and because the voltage across the diode is not kept constant by a feedback circuit. It is a very non-linear architecture susceptible to fabrication and parameter variations and usually does not achieve high performance. And since again it is not an integrating photosensing architecture, it is not analyzed in detail in this work.

5.1.2 Photodiode with Passive Integrator (PD+PI)

The photodiode with passive integrator is shown in Fig. 5.2. It is basically a photodiode operated in integration mode with a source follower [67]. The photodiode D_1 together with the capacitance C_1 are first charged to the reset voltage V_R by closing switch S_1. After the reset phase the switch S_1 is opened and the photocurrent and the photodiode leakage current are integrated on the integration capacitance consisting of the photodiode capacitance, the capacitance C_1 and the gate-source capacitance of the transistor T_1 thus yielding a voltage ramp. The source follower stage consisting of transistor T_1 and current source I_R provides high impedance at the integration node and transfers the integration voltage to the amplified voltage V_O thus yielding a low impedance voltage ramp.

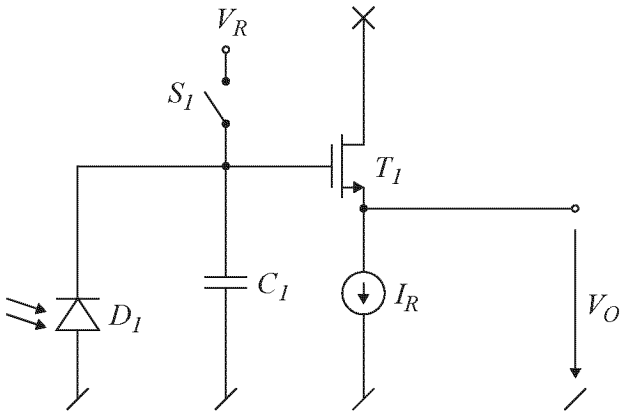


Fig. 5.2: Photodiode with passive integrator (PD+PI).

This architecture is very simple, but it is not wide-spread and can be typically found in particular circuits with variations of the source follower [70][71].
The chip layouts of the circuit realizations are shown in Appendix F. The parameters for the realized architectures according to the integrating sampled-data photosensing model of Chapter 3 are listed in Appendix G. To simplify matters the circuits are all operated at a supply voltage of 5 V. The size of transistor T_1 is $W/L = 1.6\mu\text{m}/1.2\mu\text{m}$. It is small to achieve small area, low bias current and low parasitic capacitance. However, it is not designed with minimum size of $W/L = 0.8\mu\text{m}/0.6\mu\text{m}$ to reduce short channel effects such as channel length modulation. The bias current I_R of 1 μA yields a gate-source voltage of about 1.7 V and a transconductance of 18 μS. The gate-source voltage modulation at changing source voltages due to the body effect yields a small-signal gain of about 0.82 from the input to the output of this source follower. The used range of the amplified voltage V_O from 2.5 V to 1.5 V with an amount of 1 V for the amplified voltage drop yields an integration voltage ranging from about 4.3 V to 3.1 V with an amount of about 1.2 V for the integration voltage drop. The reset voltage V_R is 5 V. The switch S_1 is a CMOS switch with an n-channel transistor of $W/L = 0.8\mu\text{m}/0.6\mu\text{m}$ and a p-channel transistor of $W/L = 2.4\mu\text{m}/0.6\mu\text{m}$. The switch is small to achieve low parasitic capacitance and low clock feedthrough to the high impedance integration node. The larger size of the p-channel transistor is due to the lower conductivity of these devices and to guarantee low resistance of about 4 kΩ of the closed switch over the whole voltage range. The integration capacitance of this architecture is equal to the photodetector capacitance. This is the capacitance of the integration node and includes the separate physical capacitance C_1 of 710 fF and the photodiode

capacitance, which depends on the integration voltage. Linearizing this function in the operating point yields a photodiode capacitance of about 5.9 pF and totals the integration capacitance and the photodetector capacitance to about 6.6 pF. D_1 is a p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode yielding a quantum efficiency of 70 % at a wavelength of 612 nm. The 1/f noise voltage coefficient of transistor T_1 is about 10^{-10} V^2. Using the voltage amplifier gain of about 0.82, this corresponds to a 1/f noise voltage coefficient of about $0.69 \cdot 10^{-10}$ V^2 referred to the amplified voltage at the input of the ramp ADC. The analog bandwidth of this architecture is determined by the output conductance of the source follower given by the transconductance of the transistor and by the load capacitance at this node that is connected to the ramp ADC. The load capacitance of slightly above 10 pF in the actual measurement setup yields an analog bandwidth of about 200 kHz.
The software tool "PhotoList" described in Appendix E provides noise and performance analysis for the realized architectures. Fig. 5.3 shows the signal-to-noise ratio contributions of the different noise sources of the realized photodiode with passive integrator versus the photocurrent. The curves indicate the signal-to-noise ratio if only the specified single noise source was present, which is either the shot noise, the preamplifier thermal noise, the voltage amplifier thermal noise, the transconductor thermal noise, the resistor thermal noise, the 1/f noise, the ramp ADC thermal noise, or the quantization noise resulting from limited timing resolution. The curve referring to the total noise indicates the resulting signal-to-noise ratio for the voltage ramp ADC with voltage amplifier if all noise contributions are taken into account according to (3.136). The figure also shows the resulting signal-to-noise ratio referring to the total noise if averaging is applied according to (3.145).
The dominant noise sources of this realization are shot noise with a corresponding SNR of 77 dB and ramp ADC thermal noise with an SNR of 77 dB. The total SNR results to 74 dB.
Fig. 5.4 shows the measured signal-to-noise ratio of the photodiode with passive integrator without averaging versus the integration time Δt. The theoretical curve corresponds to the total noise in Fig. 5.3. The reduction in measured SNR at short integration times is due to line interferences as investigated in Section 3.7. The reduced measured SNR at long integration times results from temperature drift due to long measurement times and from transients due to insufficient settlement prior to the noise measurement.

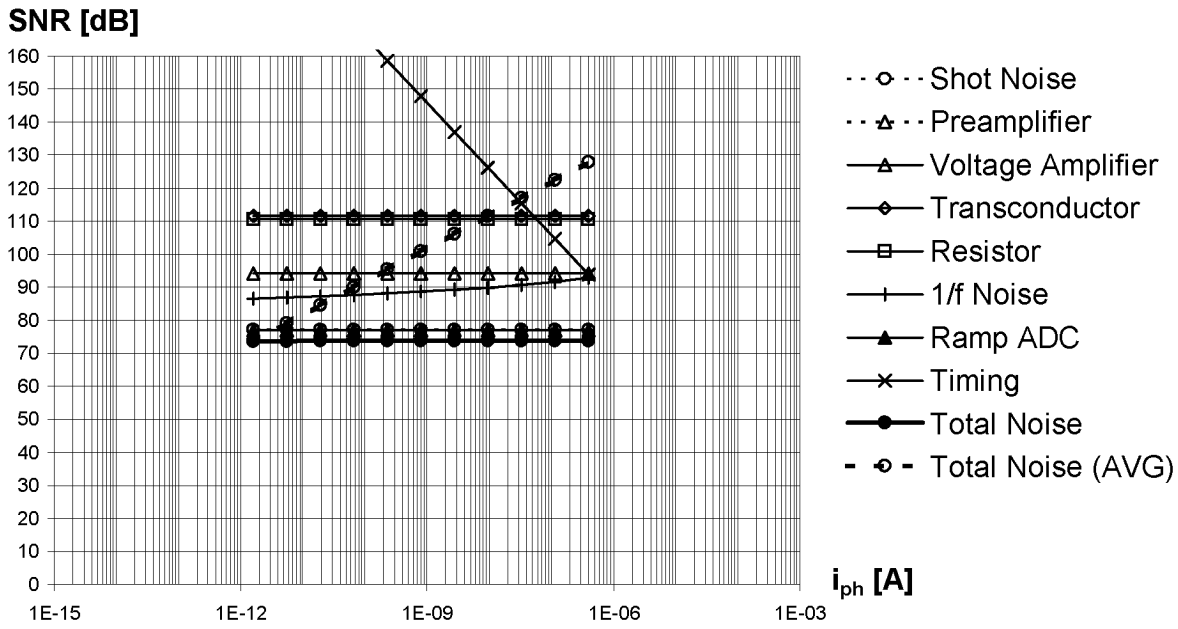


Fig. 5.3: Signal-to-noise ratio contributions of the different noise sources of the photodiode with passive integrator (PD+PI).

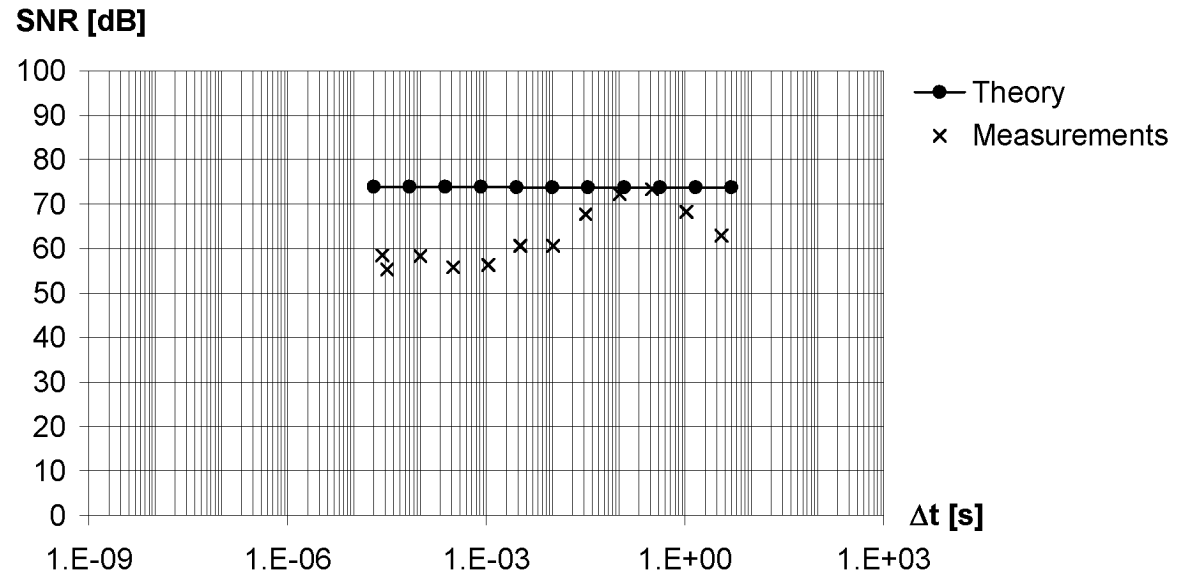


Fig. 5.4: Signal-to-noise ratio of the photodiode with passive integrator (PD+PI).

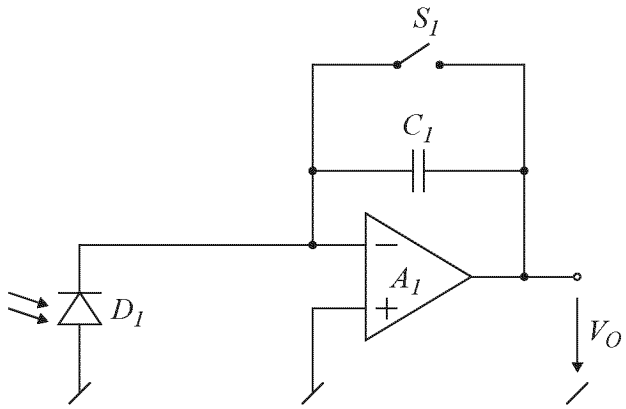


Fig. 5.5: Photodiode with active integrator (PD+AI).

5.1.3 Photodiode with Active Integrator (PD+AI)

The photodiode with active integrator is shown in Fig. 5.5. The photodiode is basically operated at constant voltage and the photodiode current or the recharge current in switched designs is integrated thus measuring the transferred charge [65]. The operational amplifier A_1 permanently provides virtual ground at its negative input due to the feedback and thus yields constant zero voltage across the photodiode D_1. The switch S_1 is first closed to decharge the capacitance C_1. After the reset phase the switch S_1 is opened and the photocurrent is integrated on the integration capacitance C_1 thus yielding the integration voltage V_O, which is equal to the amplified voltage.
This architecture is wide-spread and is typically used in linear photosensor arrays with large pixels [8].
The actual realization uses a standard operational amplifier from a library provided by the foundry. Due to the limited input voltage range the non-inverting input of the operational amplifier A_1 is connected to a constant voltage of 1 V representing signal ground. The integration voltage V_O is equal to the amplified voltage and ranges from 1.5 V to 2.5 V with an amplified voltage drop of 1 V. The switch S_1 is the same CMOS switch with an n-channel transistor of $W/L = 0.8\mu$m/0.6μm and a p-channel transistor of $W/L = 2.4\mu$m/0.6μm as in the photodiode with passive integrator. The integration capacitance of this architecture is the separate physical capacitance C_1 of 710 fF. The photodetector capacitance includes the photodiode capacitance of about 10.6 pF and the input capacitance of the operational amplifier of 800 fF and totals to about 11.4 pF. D_1 is a p-diffusion/n-well photodiode in combination with p-substrate/n-well pho-

todiode yielding a quantum efficiency of 70 % at a wavelength of 612 nm. The voltage across the p-diffusion/n-well photodiode is zero. The operational amplifier generates both preamplifier thermal noise and voltage amplifier thermal noise. Its input voltage noise of about 25 nV/$\sqrt{\text{Hz}}$ is equivalent to the thermal noise of two transistors with a transconductance of 50 μS at the input of a noise-free operational amplifier. The 1/f noise voltage coefficient of the operational amplifier is about $2.2 \cdot 10^{-12}$ V^2. Using the small-signal gain of about 17 of the non-inverting amplifier represented by operational amplifier A_1 and the photodetector capacitance and the integration capacitance, this corresponds to a 1/f noise voltage coefficient of about $6.4 \cdot 10^{-10}$ V^2 referred to the amplified voltage at the input of the ramp ADC. The analog bandwidth of this architecture is determined by the small-signal gain of the mentioned non-inverting amplifier. The operational amplifier has a unity gain bandwidth of about 10 MHz and the small-signal gain of about 17 yields an analog bandwidth of about 600 kHz.
Fig. 5.6 shows the signal-to-noise ratio contributions of the different noise sources of the realized photodiode with active integrator versus the photocurrent analogous to Fig. 5.3. The dominant noise sources of this realization are shot noise with a corresponding SNR of 66 dB and particularly preamplifier thermal noise with an SNR of 65 dB. The total SNR results to 62 dB.
Fig. 5.7 shows the measured signal-to-noise ratio of the photodiode with active integrator without averaging versus the integration time Δt analogous to Fig. 5.4. The reduction in measured SNR at short integration times is due to line interferences as investigated in Section 3.7.

Effect of Photodetector Capacitance

The effect of photodetector capacitance on preamplifier thermal noise according to (3.99) is illustrated in Fig. 5.8. It shows the measured signal-to-noise ratio of the realized photodiode with active integrator for different photodetector capacitances. The shot noise is constant with a corresponding SNR of 66 dB. The photodetector capacitance of 11.4 pF causes preamplifier thermal noise with a corresponding SNR of 65 dB and yields a total SNR of 62 dB according to Fig. 5.6. An increased photodetector capacitance of 100 pF causes increased preamplifier thermal noise with a corresponding SNR equal to the total SNR of theoretically 55 dB. A very high photodetector capacitance of 1 nF causes very high preamplifier thermal noise with a corresponding SNR equal to the total SNR of theoretically only 45 dB. The experimental results in Fig. 5.8 confirm the different photodetector capacitance dependent SNR levels.

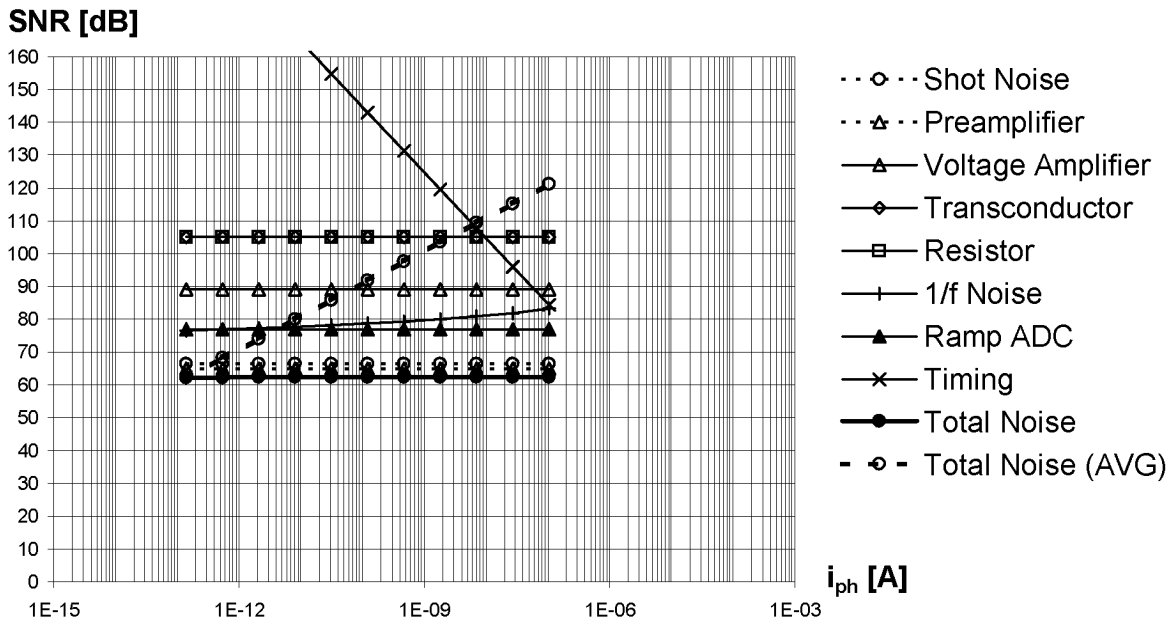


Fig. 5.6: Signal-to-noise ratio contributions of the different noise sources of the photodiode with active integrator (PD+AI).

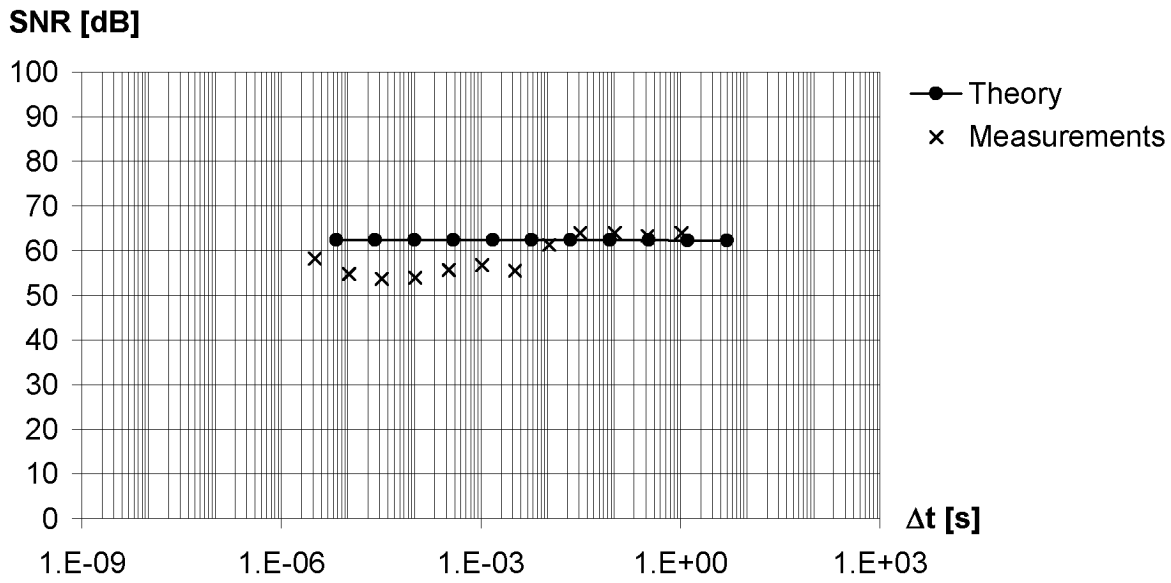


Fig. 5.7: Signal-to-noise ratio of the photodiode with active integrator (PD+AI).

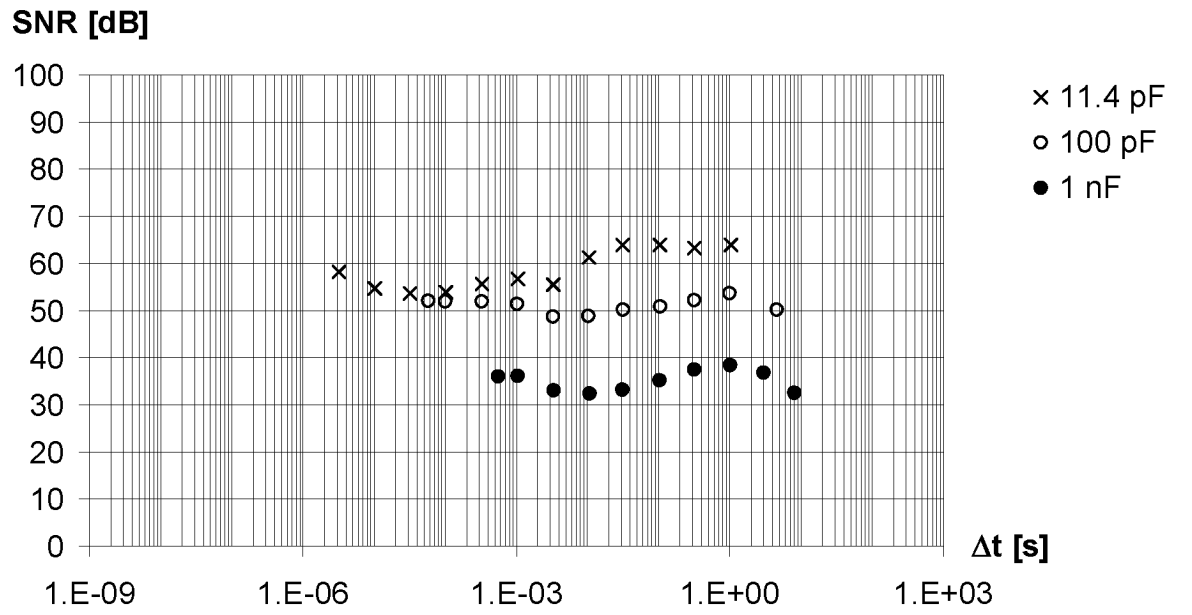


Fig. 5.8: Measured signal-to-noise ratio of the photodiode with active integrator (PD+AI) for different photodetector capacitances.

Effect of Timing Resolution

The effect of timing resolution on signal-to-noise ratio according to (3.134) with (3.23), (3.2) and (3.20) is illustrated in Fig. 5.9. It shows the measured signal-to-noise ratio of the realized photodiode with active integrator for a reduced timing resolution of 1 μs. The quantization noise increases with increasing photocurrent or decreasing integration time. Hence the total SNR of 62 dB according to Fig. 5.6 decreases for short integration times to the SNR corresponding to the quantization noise, which decreases by 20 dB per decade with decreasing integration time.

5.1.4 Photogate with Passive Integrator (PG+PI)

The photogate with passive integrator is shown in Fig. 5.10. It is basically the same architecture with almost exactly the same operating principle as the photodiode with passive integrator according to Fig. 5.2 except that the sensing diode D_1 has a much lower capacitance value.
In contrast to the photodiode with passive integrator, the integration capacitance

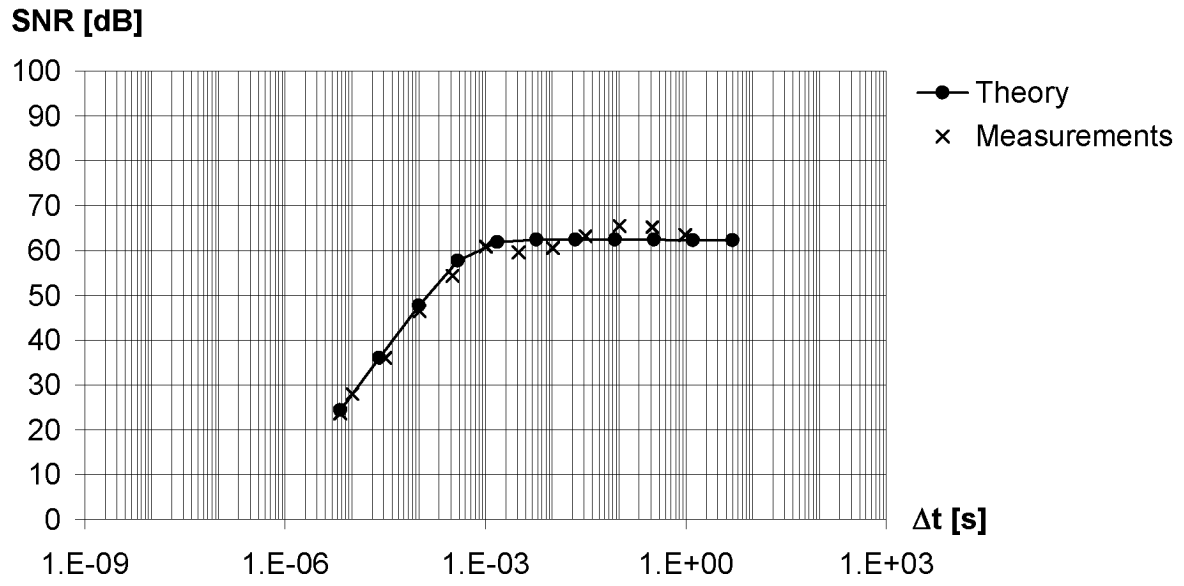


Fig. 5.9: Signal-to-noise ratio of the photodiode with active integrator (PD+AI) for a reduced timing resolution of 1 μs.

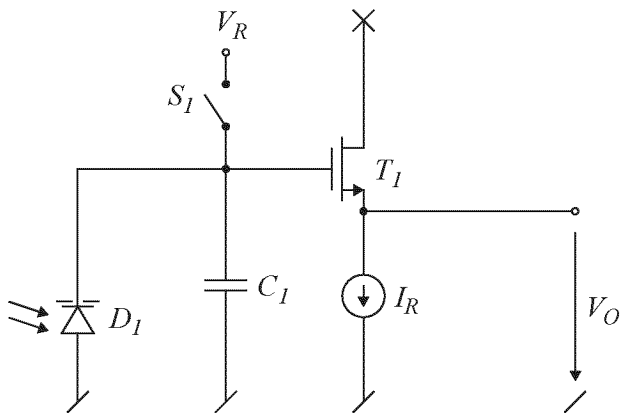


Fig. 5.10: Photogate with passive integrator (PG+PI).

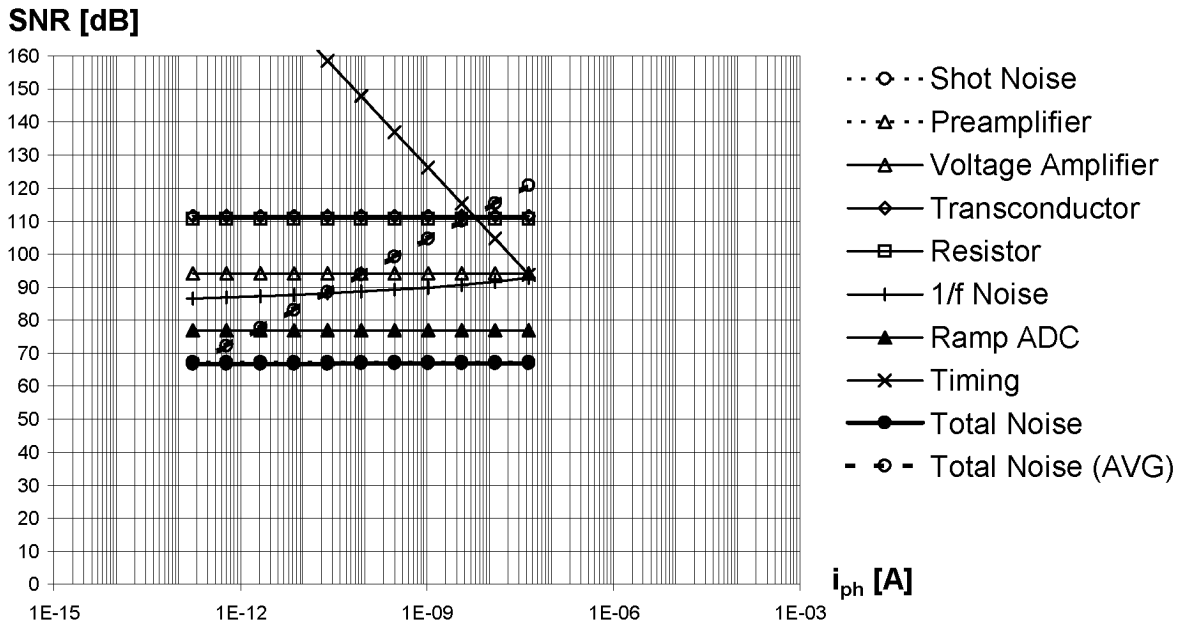


Fig. 5.11: Signal-to-noise ratio contributions of the different noise sources of the photogate with passive integrator (PG+PI).

and the photodetector capacitance of this realization are equal to the separate physical capacitance C_1 of 710 fF, since the capacitance of the very small sensing diode D_1 is only about 4 fF. The photogate yields a quantum efficiency of 30 % at a wavelength of 612 nm.

Fig. 5.11 shows the signal-to-noise ratio contributions of the different noise sources of the realized photogate with passive integrator versus the photocurrent analogous to Fig. 5.3. The dominant noise source of this realization is shot noise with a corresponding SNR equal to the total SNR of 67 dB. Compared to the photodiode with passive integrator the lower capacitance of the sensing diode results in a lower integration capacitance and therefore in lower photogenerated and collected charge. This yields higher shot noise with a lower corresponding SNR so that the ramp ADC thermal noise is not limiting here.

Fig. 5.12 shows the measured signal-to-noise ratio of the photogate with passive integrator without averaging versus the integration time Δt analogous to Fig. 5.4. The reduction in measured SNR at short integration times is due to line interferences as investigated in Section 3.7.

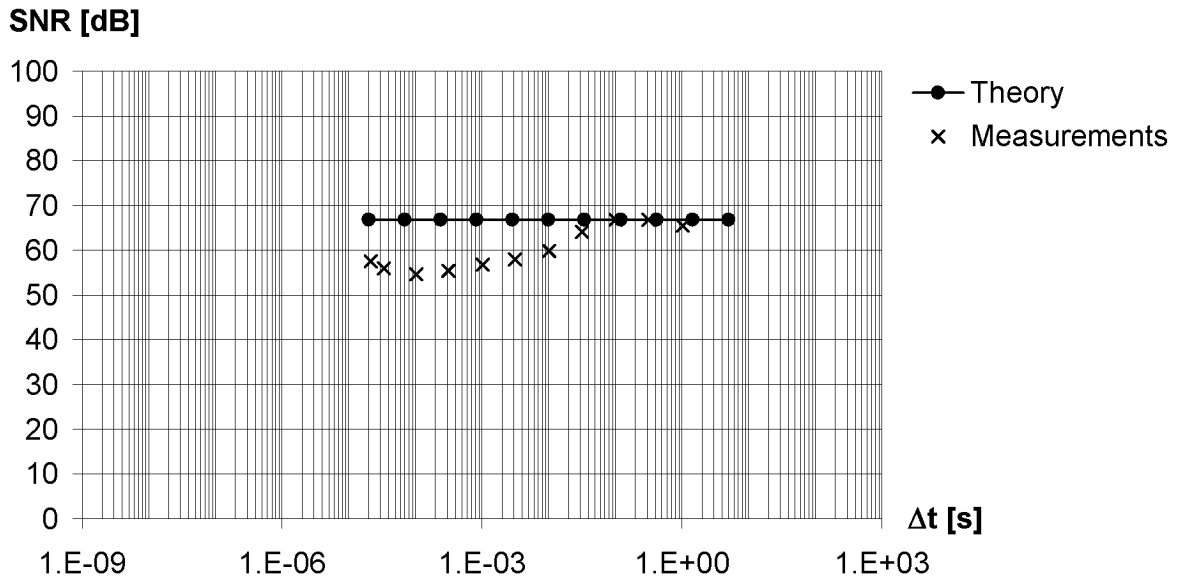


Fig. 5.12: Signal-to-noise ratio of the photogate with passive integrator (PG+PI).

5.1.5 Photogate with Active Integrator (PG+AI)

The photogate with active integrator is shown in Fig. 5.13. It is basically the same architecture with almost exactly the same operating principle as the photodiode with active integrator according to Fig. 5.5 except that the sensing diode D_1 has a much lower capacitance value.
In contrast to the photodiode with active integrator, the photodetector capacitance of this realization is equal to the input capacitance of the operational amplifier of about 800 fF, since the capacitance of the very small sensing diode D_1 is only about 4 fF. The photogate yields a quantum efficiency of 30 % at a wavelength of 612 nm. The small-signal gain of the non-inverting amplifier represented by operational amplifier A_1 and the photodetector capacitance and the integration capacitance is about 2.1. This yields a 1/f noise voltage coefficient of about $0.12 \cdot 10^{-10}$ V^2 referred to the amplified voltage at the input of the ramp ADC. The unity gain bandwidth of the operational amplifier of about 10 MHz and the small-signal gain of about 2.1 yield an analog bandwidth of about 5 MHz.
Fig. 5.14 shows the signal-to-noise ratio contributions of the different noise sources of the realized photogate with active integrator versus the photocurrent analogous to Fig. 5.3. The dominant noise source of this realization is shot

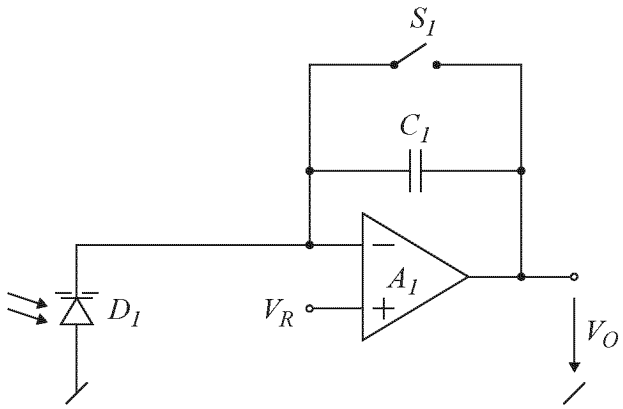


Fig. 5.13: Photogate with active integrator (PG+AI).

noise with a corresponding SNR equal to the total SNR of 66 dB. At high photocurrents quantization noise resulting from limited timing resolution becomes dominant and the total SNR begins to decrease by 20 dB per decade with increasing photocurrent. Compared to the photodiode with active integrator the lower capacitance of the sensing diode results in a lower photodetector capacitance. This yields lower preamplifier thermal noise and results in shot noise to be solely limiting.
Fig. 5.15 shows the measured signal-to-noise ratio of the photogate with active integrator without averaging versus the integration time Δt analogous to Fig. 5.4. The reduction in measured SNR at medium integration times is due to line interferences as investigated in Section 3.7.

5.2 Array Architectures

Array architectures in large-area photosensing have an array of detectors or pixels per photosensing area instead of only one single detector. The pixels of such an array architecture may have any area, but they have all the same homogeneous illumination and all together they represent a large-area photosensing architecture with one photosensing area that can be part of a larger array of photosensing areas with spatial resolution.
The basic array photosensing architectures for integrating sampled-data photosensing are characterized by the type of photodetector and the type of pixel determined by the amplifier arrangement. The basic photodetectors are the photodiode and the photogate. The basic pixel types are the active and the passive

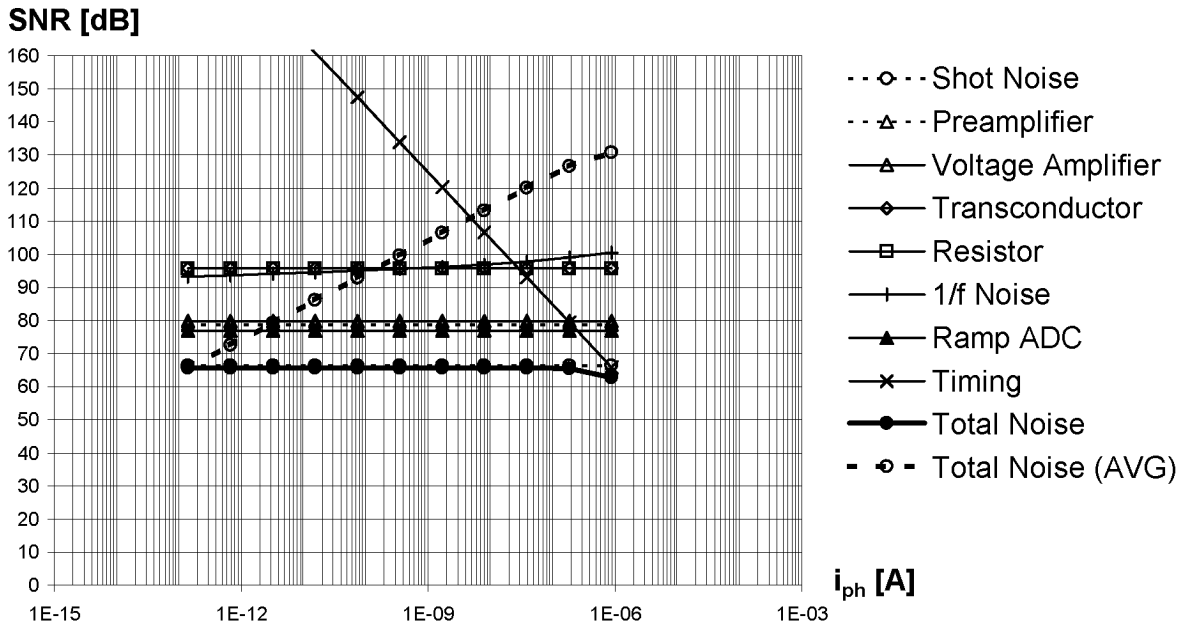


Fig. 5.14: Signal-to-noise ratio contributions of the different noise sources of the photogate with active integrator (PG+AI).

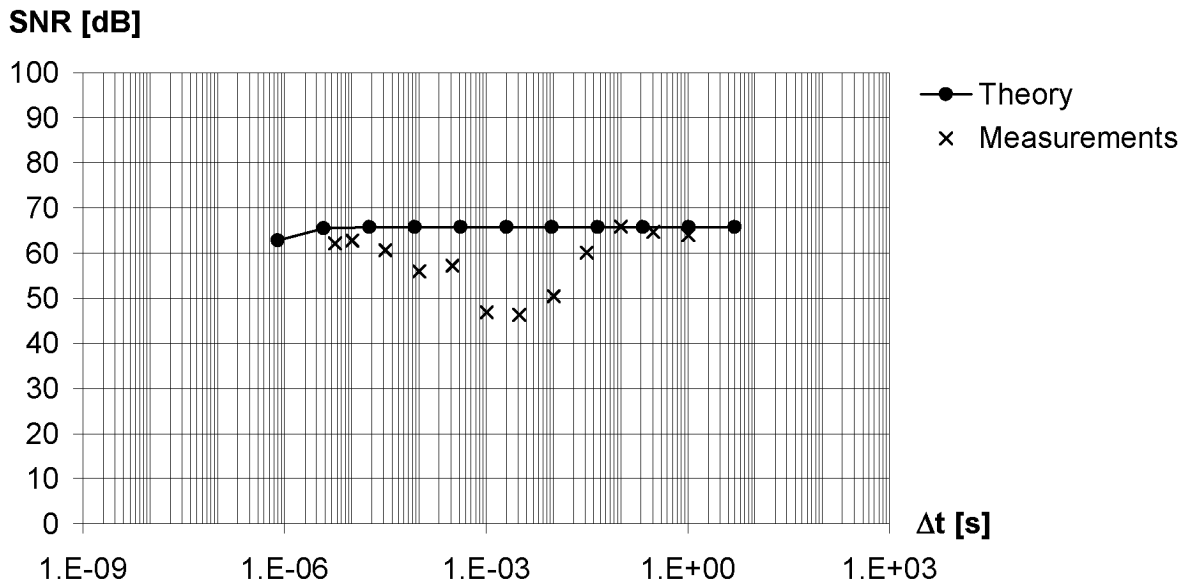


Fig. 5.15: Signal-to-noise ratio of the photogate with active integrator (PG+AI).

pixel [72][14]. The active pixel contains an active amplifier in each pixel [12]. The passive pixel just consists of passive components and switches, and amplifiers are located elsewhere and shared among several or all of the pixels. The combination of the two basic photodetectors and the two basic pixel types yields in principle four basic photosensing architectures, but the photogate in a passive pixel does not make sense and is not found in realizations and therefore not considered here. The photodiode in an active pixel is the standard active pixel sensor. The photodiode in a passive pixel is found in the photodiode array with active integrator. The photogate in an active pixel is referred to as photogate active pixel sensor.
Apart from the above classification there are basic array photosensing architectures that differ in the charge transport mechanism, known as charge-coupled devices [10]. Their photodetectors are always MOS structures building some kind of photogates, but they are characterized by using either the passive or the active integrator.
In this work array architectures are realized in 1 x 16 arrays. The photodetector area of the single pixels of this array is equal to the photodetector area of the single detector architectures divided by 16.

5.2.1 Standard Active Pixel Sensor (SAPS)

The standard active pixel sensor is shown in Fig. 5.16. It is basically the same architecture with almost exactly the same operating principle as the photodiode with passive integrator according to Fig. 5.2 except that the photodiode D_1 is much smaller and that there are select switches and a second source follower stage [14]. The first source follower stage consisting of transistor T_1 and current source I_{R1} provides high impedance at the integration node in the pixel and transfers the integration voltage to the bus. Readout of the pixels is controlled by the select switches. The switch S_{A1} selects the drawn pixel to drive the bus. The second source follower stage consisting of transistor T_2 and current source I_{R2} transfers the bus voltage to the amplified voltage V_O thus yielding a low impedance voltage ramp.
This architecture is wide-spread in image sensors with typically two-dimensional arrays of high numbers of small pixels [73][74]. There are circuits that provide a bias current in the pixels as discussed in Section 3.3 [75]. And the source follower section may slightly vary and consist of more than two stages or only a single stage [76].
Transistor T_1, bias current I_{R1} and switch S_1 of this realization match the photo-

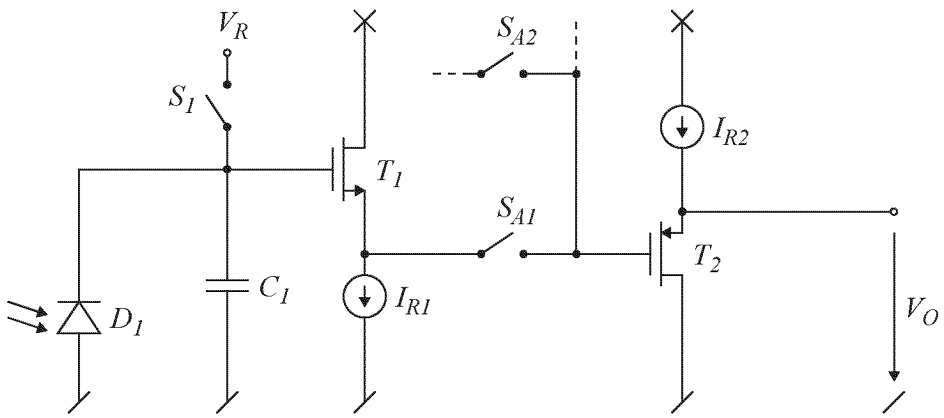


Fig. 5.16: Standard active pixel sensor (SAPS).

diode with passive integrator. The size of transistor T_2 is $W/L = 16\mu\text{m}/1.2\mu\text{m}$. It is larger than transistor T_1 since it is a p-channel device with lower conductivity and since parasitic capacitance is not critical for this stage. The bias current I_{R2} of 10 μA yields a gate-source voltage of about -1.1 V and a transconductance of 100 μS. The gate-source voltage modulation at changing source voltages due to the body effect is negligible for this second source follower. This yields a small-signal gain of about 0.82 from the input to the output of the complete two-stage source follower. The used range of the amplified voltage V_O from 3.6 V to 2.6 V with an amount of 1 V for the amplified voltage drop yields the same integration voltages as for the photodiode with passive integrator. The switches S_{Ai} are CMOS switches with an n-channel transistor of $W/L = 8\mu\text{m}/0.6\mu\text{m}$ and a p-channel transistor of $W/L = 24\mu\text{m}/0.6\mu\text{m}$ with a very low resistance of about 400 Ω of the closed switch over the whole voltage range. The integration capacitance and the photodetector capacitance are equal to the capacitance of the integration node, which includes the separate physical capacitance C_1 of about 46 fF and the photodiode capacitance, which depends on the integration voltage. Linearizing this function in the operating point yields a photodiode capacitance of about 390 fF and totals the integration capacitance and the photodetector capacitance to about 440 fF. The photodiode D_1 is 16 times smaller than the one of the photodiode with passive integrator. The thermal noise of transistor T_1 with a transconductance of 18 μS in sequence with transistor T_2 with a transconductance of 100 μS can be modeled by the thermal noise of a single transistor with a transconductance of 14 μS. The measured analog bandwidth of this architecture in the actual measurement setup is about 550 kHz.

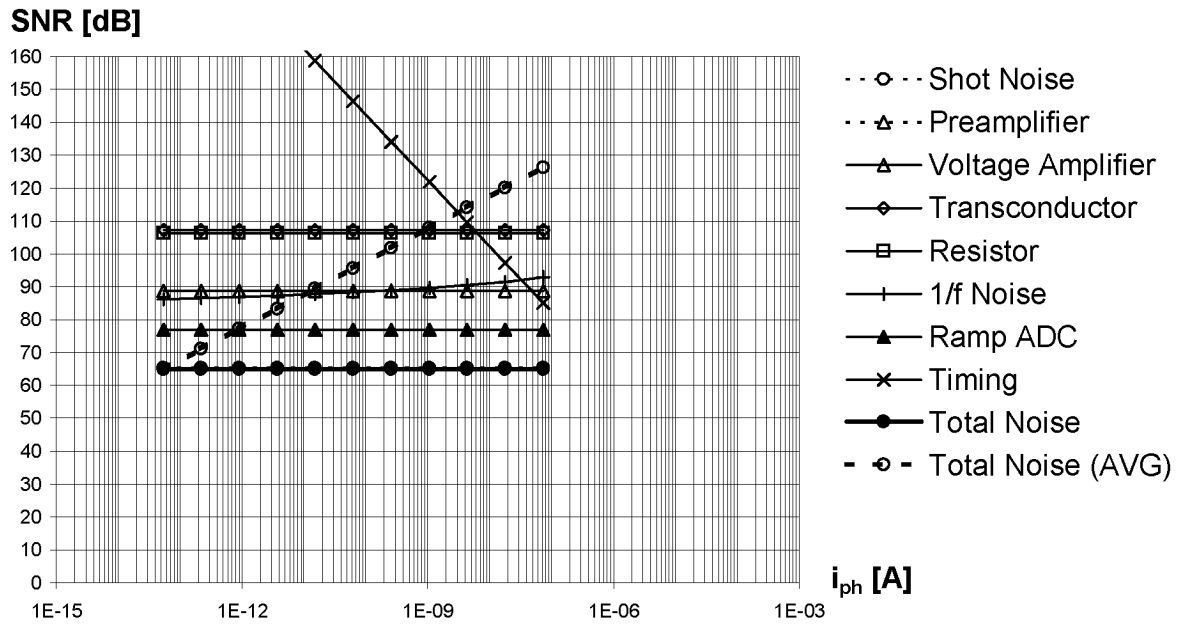


Fig. 5.17: Signal-to-noise ratio contributions of the different noise sources of a single pixel of the standard active pixel sensor (SAPS).

Fig. 5.17 shows the signal-to-noise ratio contributions of the different noise sources of a single pixel of the realized standard active pixel sensor versus the photocurrent analogous to Fig. 5.3. The dominant noise source of this realization is shot noise with a corresponding SNR of 65 dB for a single pixel. Compared to the photodiode with passive integrator the lower capacitance of the smaller photodiode results in a lower integration capacitance and therefore in lower photogenerated and collected charge. This yields higher shot noise with a lower corresponding SNR so that the ramp ADC thermal noise is not limiting here. The realized standard active pixel sensor has 16 pixels per photosensing area. The measurement samples of these pixels are averaged to get the final signal measurement, which is equivalent to averaging 16 integration samples per signal measurement as in (3.57). According to (3.145) this increases the SNR by a factor of 4 or by 12 dB and the total SNR results to 77 dB.
Fig. 5.18 shows the measured total signal-to-noise ratio of the standard active pixel sensor without temporal averaging versus the integration time Δt analogous to Fig. 5.4. The reduction in measured SNR at short integration times is due to line interferences as investigated in Section 3.7.

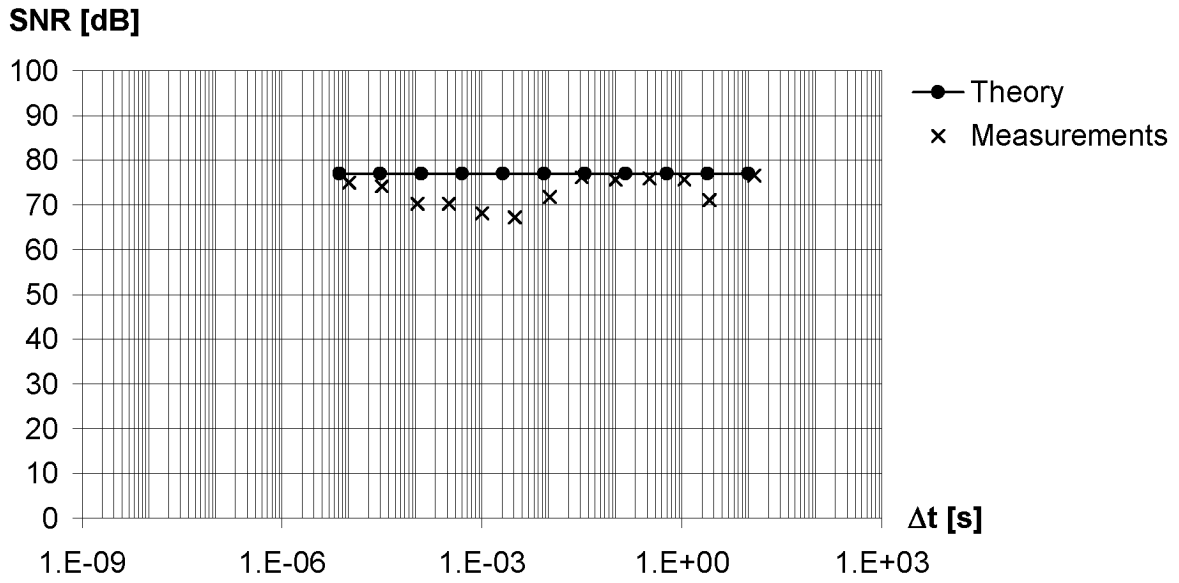


Fig. 5.18: Signal-to-noise ratio of the standard active pixel sensor (SAPS).

5.2.2 Photodiode Array with Active Integrator (PDA+AI)

The photodiode array with active integrator is shown in Fig. 5.19. It is basically the same architecture with almost exactly the same operating principle as the photodiode with active integrator according to Fig. 5.5 except that the photodiode D_1 is much smaller and that there are select switches [66]. The pixel consists only of the photodiode, which can be directly connected to the bus. Readout of the pixels is controlled by the select switches. The switch S_{A1} selects the drawn pixel and connects it to the bus and therefore to the active integrator.
This architecture is wide-spread and is often used in two-dimensional photosensor arrays [77].
Operational amplifier A_1, capacitance C_1 and switch S_1 of this realization match the photodiode with active integrator. The switches S_{Ai} are CMOS switches with an n-channel transistor of $W/L = 8\mu\text{m}/0.6\mu\text{m}$ and a p-channel transistor of $W/L = 24\mu\text{m}/0.6\mu\text{m}$ with a very low resistance of about $400\ \Omega$ of the closed switch over the whole voltage range. The photodetector capacitance includes the photodiode capacitance of about 690 fF, the input capacitance of the operational amplifier of 800 fF and the capacitance of the interconnect wires of about 110 fF. This totals to about 1.6 pF. The photodiode D_1 is 16 times smaller

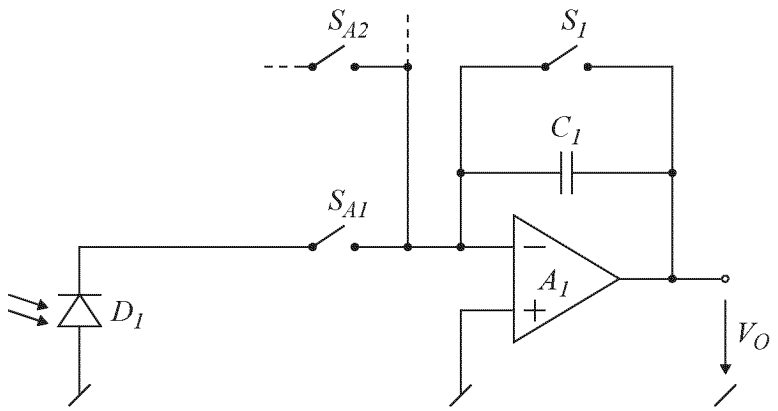


Fig. 5.19: Photodiode array with active integrator (PDA+AI).

than the one of the photodiode with active integrator. The small-signal gain of the non-inverting amplifier represented by operational amplifier A_1 and the photodetector capacitance and the integration capacitance is about 3.3. This yields a 1/f noise voltage coefficient of about $0.25 \cdot 10^{-10}$ V^2 referred to the amplified voltage at the input of the ramp ADC. The unity gain bandwidth of the operational amplifier of about 10 MHz and the small-signal gain of about 3.3 yield an analog bandwidth of about 3 MHz.

Fig. 5.20 shows the signal-to-noise ratio contributions of the different noise sources of a single pixel of the realized photodiode array with active integrator versus the photocurrent analogous to Fig. 5.3. The dominant noise source of this realization is shot noise with a corresponding SNR of 66 dB for a single pixel. This yields a total SNR of 65 dB for a single pixel. At high photocurrents quantization noise resulting from limited timing resolution becomes dominant and the SNR for a single pixel begins to decrease by 20 dB per decade with increasing photocurrent. Compared to the photodiode with active integrator the lower capacitance of the smaller photodiode results in a lower photodetector capacitance. This yields lower preamplifier thermal noise and results in shot noise to be solely limiting. The realized photodiode array with active integrator has 16 pixels per photosensing area. The measurement samples of these pixels are averaged to get the final signal measurement, which is equivalent to averaging 16 integration samples per signal measurement as in (3.57). According to (3.145) this increases the SNR by a factor of 4 or by 12 dB and the total SNR results to 77 dB.

Fig. 5.21 shows the measured total signal-to-noise ratio of the photodiode array with active integrator without temporal averaging versus the integration time Δt

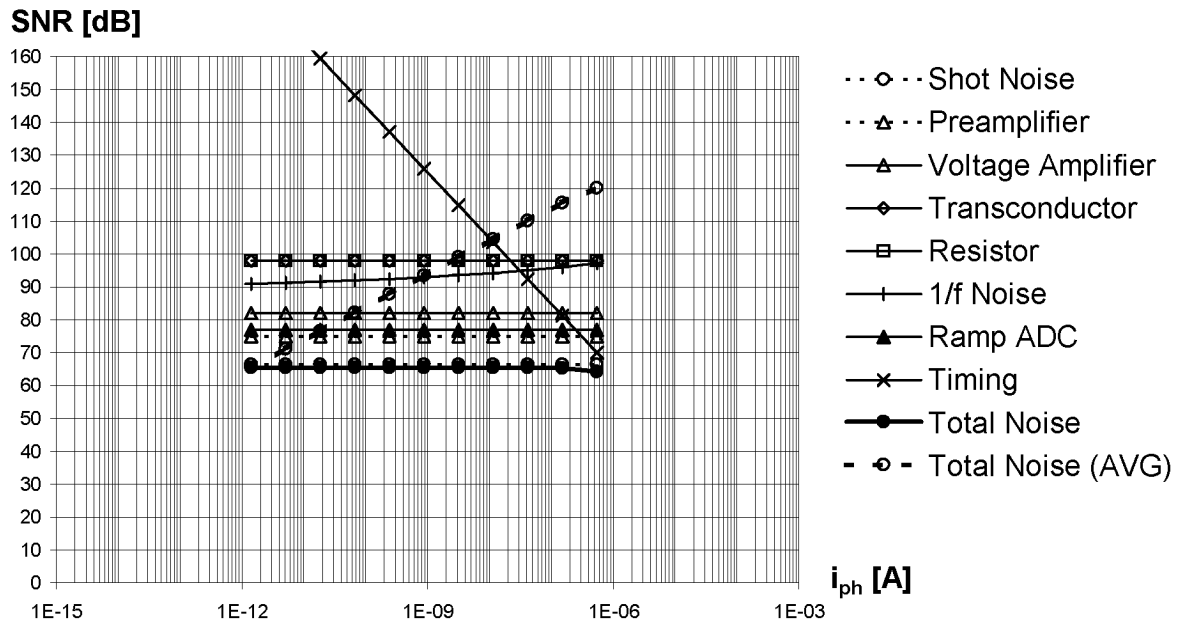


Fig. 5.20: Signal-to-noise ratio contributions of the different noise sources of a single pixel of the photodiode array with active integrator (PDA+AI).

analogous to Fig. 5.4. The reduction in measured SNR at medium integration times is due to line interferences as investigated in Section 3.7.

5.2.3 Photogate Active Pixel Sensor (PAPS)

The photogate active pixel sensor is shown in Fig. 5.22. It is basically the same architecture with almost exactly the same operating principle as the photogate with passive integrator according to Fig. 5.10 except that the sensing diode D_1 is much smaller and that there are select switches and a second source follower stage [14]. The first source follower stage consisting of transistor T_1 and current source I_{R1} provides high impedance at the integration node in the pixel and transfers the integration voltage to the bus. Readout of the pixels is controlled by the select switches. The switch S_{A1} selects the drawn pixel to drive the bus. The second source follower stage consisting of transistor T_2 and current source I_{R2} transfers the bus voltage to the amplified voltage V_O thus yielding a low impedance voltage ramp. The photogate active pixel sensor is almost the same architecture as the standard active pixel sensor according to Fig. 5.16 except that

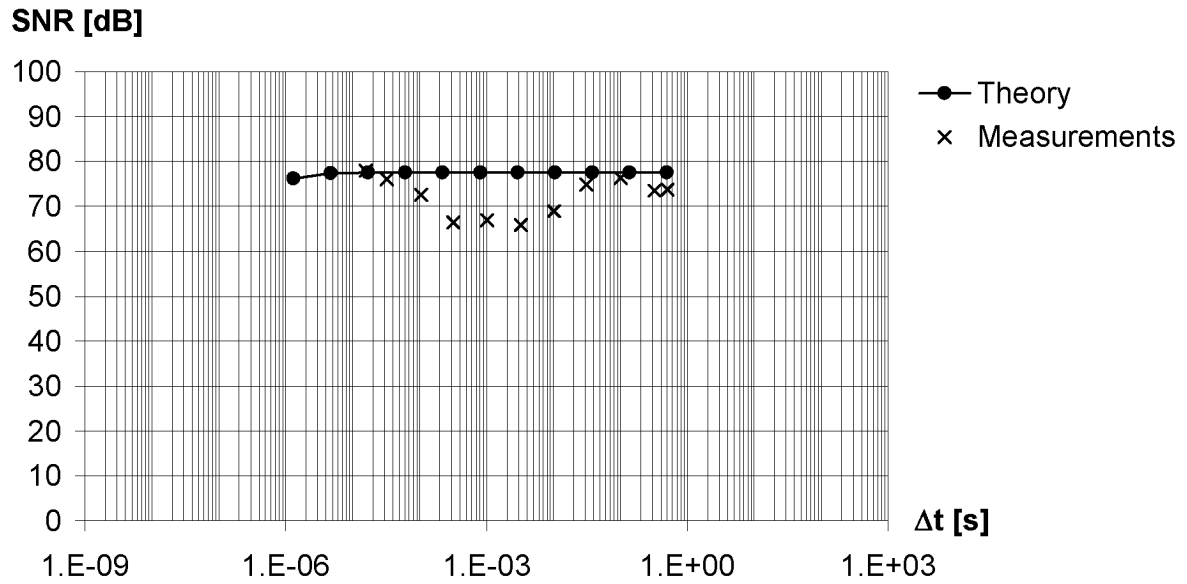


Fig. 5.21: Signal-to-noise ratio of the photodiode array with active integrator (PDA+AI).

the sensing diode D_1 has a much lower capacitance value.
This architecture like the standard active pixel sensor is wide-spread in image sensors with typically two-dimensional arrays of high numbers of small pixels [78][79].
In contrast to the standard active pixel sensor, the integration capacitance and the photodetector capacitance of this realization are much smaller. With the separate physical capacitance C_1 of about 46 fF and the capacitance of the very small sensing diode D_1 of about 4 fF, the measured integration capacitance and photodetector capacitance are about 75 fF. The photogate yields a quantum efficiency of 30 % at a wavelength of 612 nm.
Fig. 5.23 shows the signal-to-noise ratio contributions of the different noise sources of a single pixel of the realized photogate active pixel sensor versus the photocurrent analogous to Fig. 5.3. The dominant noise source of this realization is shot noise with a corresponding SNR of 58 dB for a single pixel. Compared to the photogate with passive integrator and the standard active pixel sensor the lower capacitance C_1 and the lower capacitance of the small sensing diode result in a lower integration capacitance and therefore in lower photogenerated and collected charge. This yields higher shot noise with a lower corresponding SNR so that the margin to the ramp ADC thermal noise is higher here. The realized

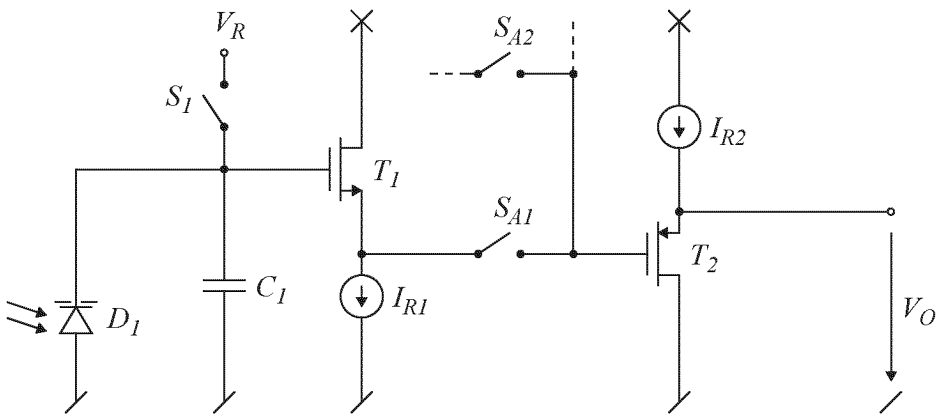


Fig. 5.22: Photogate active pixel sensor (PAPS).

photogate active pixel sensor has 16 pixels per photosensing area. The measurement samples of these pixels are averaged to get the final signal measurement, which is equivalent to averaging 16 integration samples per signal measurement as in (3.57). According to (3.145) this increases the SNR by a factor of 4 or by 12 dB and the total SNR results to 70 dB.
Fig. 5.24 shows the measured total signal-to-noise ratio of the photogate active pixel sensor without temporal averaging versus the integration time Δt analogous to Fig. 5.4.

5.2.4 Charge-Coupled Device with Passive Integrator (CCD+PI)

The charge-coupled device with passive integrator is shown in Fig. 5.25. It is basically the same architecture with almost exactly the same operating principle as the photogate with passive integrator according to Fig. 5.10 except that the charge transport to the sensing diode D_1 is different.
A charge-coupled device (CCD) is a linear array of closely spaced metal-oxide-semiconductor (MOS) structures operated in inversion [10][80]. The MOS structures as analyzed in Section B.9 form potential wells at the surface of the semiconductor according to the voltages applied to the electrodes. The potential wells under the electrodes are local minima of charge carrier energy. There are principally two types of CCDs, namely the surface-channel CCD where the energy minima are located at the surface of the semiconductor, and the buried-channel CCD where the energy minima are located below the surface due to an

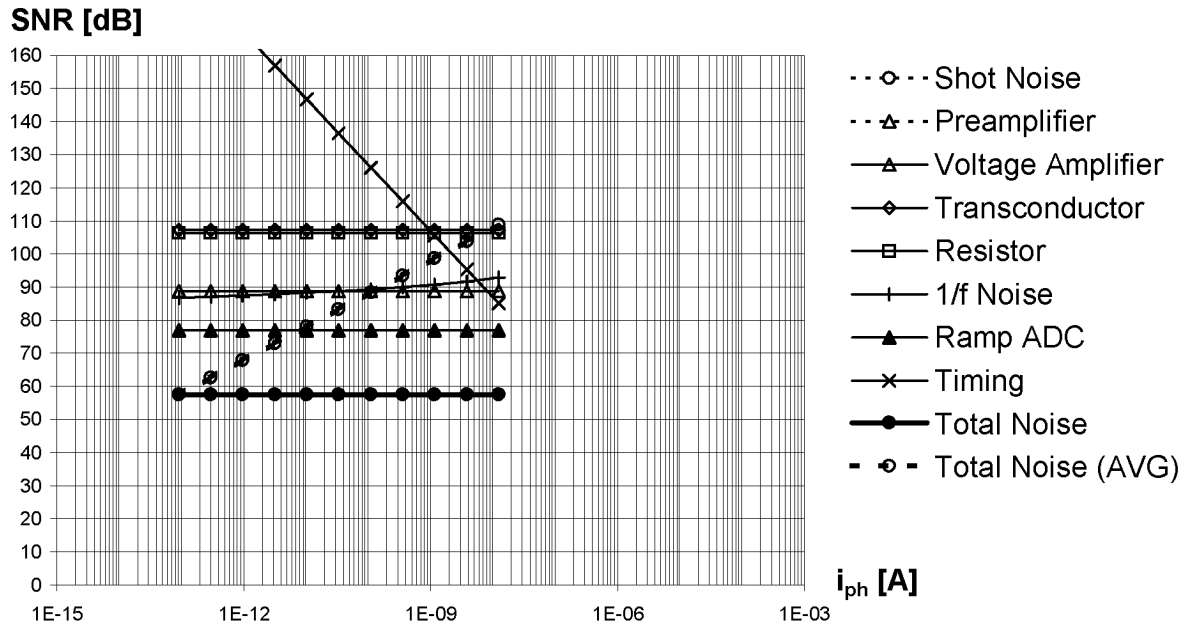


Fig. 5.23: Signal-to-noise ratio contributions of the different noise sources of a single pixel of the photogate active pixel sensor (PAPS).

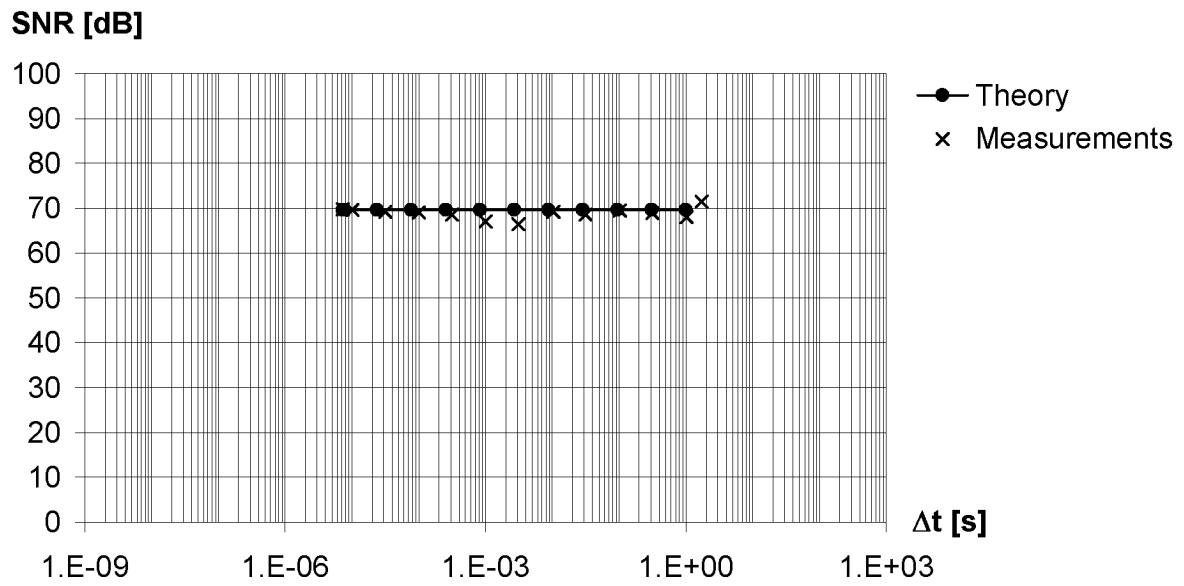


Fig. 5.24: Signal-to-noise ratio of the photogate active pixel sensor (PAPS).

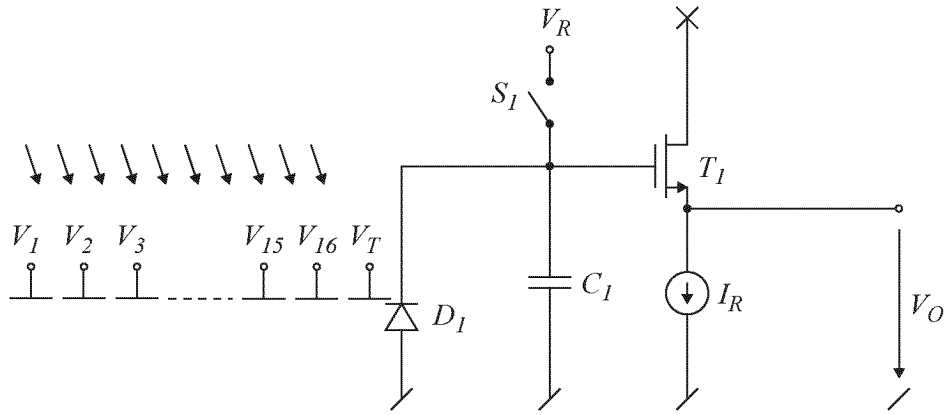


Fig. 5.25: Charge-coupled device with passive integrator (CCD+PI).

additional thin layer of opposite doping at the surface. Because the surface of the semiconductor is close to the electrode, the surface potential under a given electrode in the surface-channel CCD is determined almost totally by the voltage of that electrode as described by (B.71). The potential wells formed by the surface potential can be used to collect and store photogenerated charge. The charge can be transferred over the surface of the semiconductor by moving the surface potential extrema and therefore the energy minima by applying appropriate voltage patterns to the electrodes. The charge always flows towards the local energy minimum and can be easily transferred from one electrode to the next electrode. Charge transfer is achieved by diffusion, self-induced drift and externally induced drift due to fringing fields. The charge transfer efficiency is the fraction of charge transferred from one electrode to the next. Charge transfer efficiency is limited by incomplete charge transfer due to limited transfer time and by charge trapping due to interface states at the semiconductor-oxide interface. Charge transfer efficiencies typically achieve values larger than 0.999. Therefore the charge can be transferred to the sensing diode at the output of the CCD with almost no loss and almost free of noise.

In Fig. 5.25 photogenerated charge is collected in the 16 MOS structures forming the CCD. The charge is transferred to the sensing diode D_1 by applying appropriate voltage patterns V_1 to V_{16} to the 16 electrodes. An additional MOS structure builds a transfer gate that provides isolation of the photosensitive CCD elements from the sensing diode and reduces clock feedthrough from the clocked electrode voltage V_{16} to the sensing diode. The transfer gate is controlled by the voltage V_T.

The charge-coupled device with passive integrator is the standard architecture

for CCDs and is largely used in image sensing systems [40][81].
CCDs are fabricated in dedicated technologies with specific geometries and levels of doping concentrations. The MOS structure of a surface-channel CCD used to collect and store photogenerated charge can be implemented in standard CMOS technology, but charge transfer from one electrode to the next electrode is typically not achievable with modern CMOS technology due to high doping concentrations and referred to that high interelectrode spacings or gaps between the electrodes [82] [83]. The AMS 0.6 μm CMOS process CUX has a doping concentration of about $6 \cdot 10^{16}$ cm^{-3} in the semiconductor which is formed by either p-well or n-well. The minimum interelectrode spacing according to the design rules is 0.8 μm, but a drawn interelectrode spacing down to 0.6 μm can be fabricated still providing electrode isolation. Fig. 5.26 shows the simulated surface potential of two electrodes of a charge-coupled device in the AMS 0.6 μm CMOS process CUX with a drawn interelectrode spacing of 0.6 μm and with two floating diffusions on both sides. The structure with a p-type semiconductor is designed for electron collection and transport. Therefore the potential wells correspond to the surface potential maxima since they are the minima of charge carrier energy. The floating diffusions are externally biased at 5 V and represent very deep potential wells. The solid curve refers to 5 V on both electrodes and shows a very high potential barrier between the potential wells under the electrodes thus not allowing any charge transfer. The dashed curve refers to the maximum available potential difference for charge transport with 0 V on the left electrode and 5 V on the right electrode. There is still a high potential barrier between the electrodes thus prohibiting charge transfer from one electrode to the next with reasonable charge transfer efficiency. Therefore CCDs are generally not realizable in modern standard CMOS technology such as the AMS 0.6 μm CMOS process CUX.
Provided the charge-coupled device with passive integrator is realizable in a specific CMOS technology, it has about the same noise performance as the photogate with passive integrator due to its equivalent architecture.

5.2.5 Charge-Coupled Device with Active Integrator (CCD+AI)

The charge-coupled device with active integrator is shown in Fig. 5.27. It is basically the same architecture with almost exactly the same operating principle as the photogate with active integrator according to Fig. 5.13 except that the charge transport to the sensing diode D_1 is different and works like in the

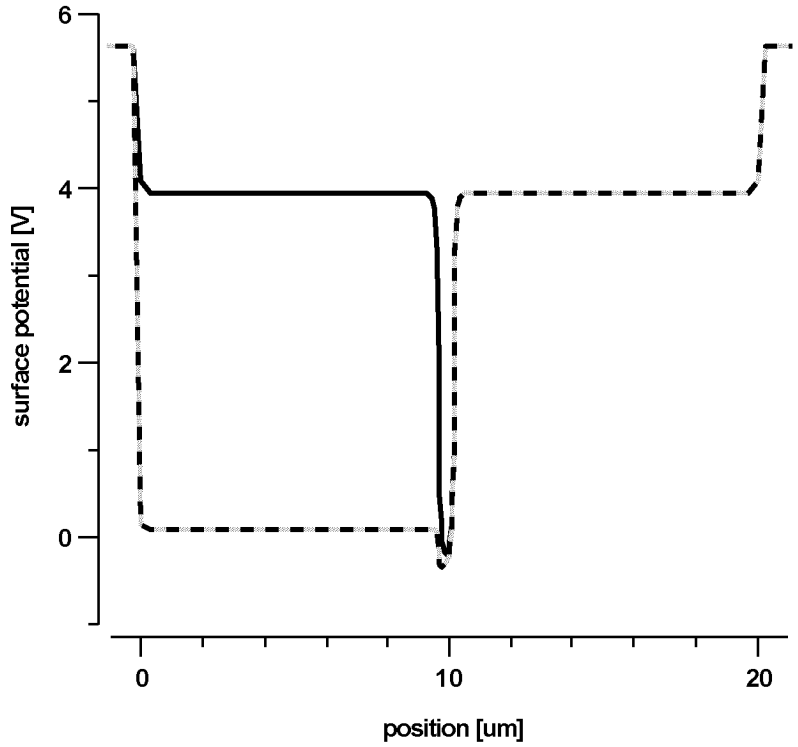


Fig. 5.26: Simulated surface potential of two electrodes of a charge-coupled device in CMOS with two floating diffusions on both sides. The solid curve refers to 5 V on both electrodes and the dashed curve refers to 0 V on the left electrode and 5 V on the right electrode.

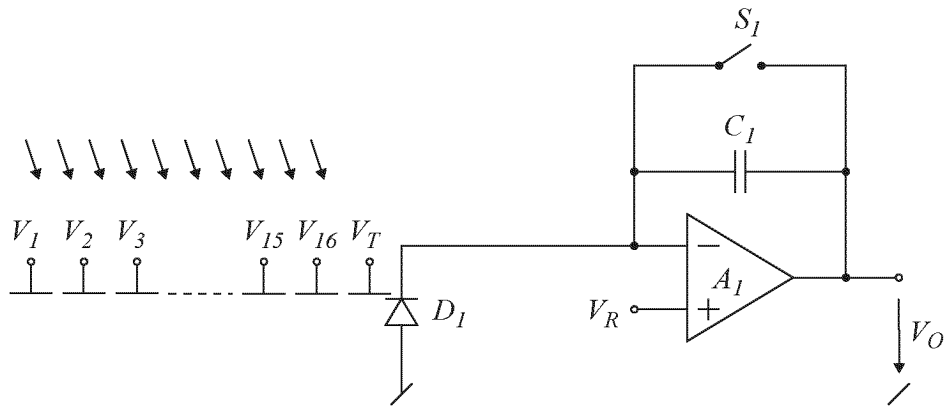


Fig. 5.27: Charge-coupled device with active integrator (CCD+AI).

charge-coupled device with passive integrator according to Fig. 5.25.
The charge-coupled device with active integrator is a not wide-spread alternative to the standard architecture with passive integrator [84].
According to the previous investigation of the charge-coupled device with passive integrator CCDs are generally not realizable in modern standard CMOS technology such as the AMS 0.6 μm CMOS process CUX.
Provided the charge-coupled device with active integrator is realizable in a specific CMOS technology, it has about the same noise performance as the photogate with active integrator due to its equivalent architecture.

5.3 Synopsis

Fig. 5.28 shows the dynamic range of the different realized basic photosensing architectures without bias current and without averaging versus the measurement time or maximum integration time Δt. The dynamic range is given by the relation of the maximum integration time to the minimum integration time according to (3.148), (3.36) and (3.37). The dynamic range for a certain measurement time depends on the analog bandwidth which determines the minimum integration time. The dynamic range without measurement time limit depends on the analog bandwidth as well, but also on the virtual integration capacitance and the minimum photocurrent or dark current which determine the maximum integration time.
The dynamic range of passive integrator architectures is basically limited by the transconductance of the source follower transistor stage and the correspond-

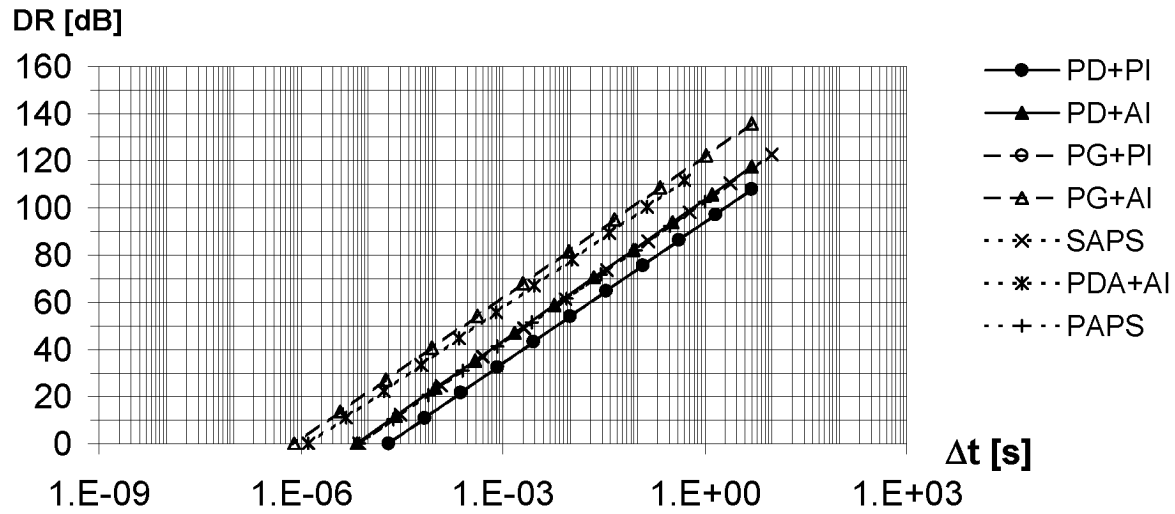


Fig. 5.28: Synopsis of the dynamic range of the realized basic photosensing architectures.

ing load capacitance, as this determines the analog bandwidth. Dynamic range improvement requires either lower load capacitance such as in completely integrated circuits or larger or multi-stage source follower transistor stages.
The dynamic range of active integrator architectures is basically limited by the bandwidth of the operational amplifier in combination with the respective small-signal gain of the integrator. This small-signal gain depends on the relation of the photodetector capacitance to the integration capacitance and high dynamic range is achieved by low photodetector capacitance.
For a certain measurement time the photogate with active integrator achieves the highest dynamic range due to the high analog bandwidth resulting from the low photodetector capacitance. The photodiode with active integrator has lower dynamic range due to the high photodetector capacitance, but it can be increased by dividing the photodetector, which yields the photodiode array with active integrator.
The photodiode array with active integrator has the lowest maximum integration time due to high leakage currents in the switches. The standard active pixel sensor achieves the highest maximum integration time due to the low dark current of the small photodiodes in combination with medium virtual integration capacitance.
The highest dynamic range without measurement time limit is achieved by the photogate with active integrator due to the high analog bandwidth and medium

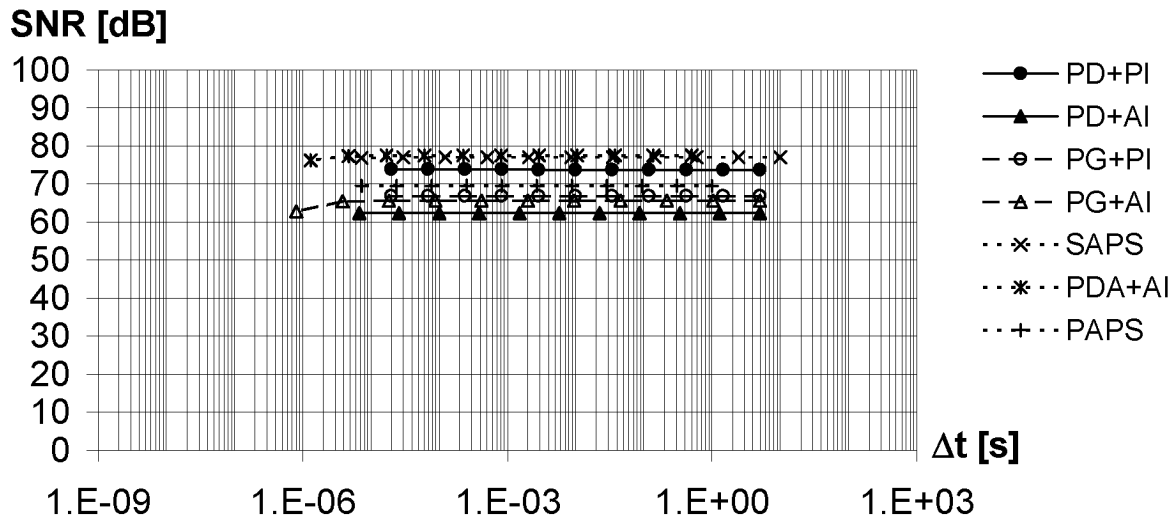


Fig. 5.29: Synopsis of the signal-to-noise ratio of the realized basic photosensing architectures.

maximum integration time. The photogate active pixel sensor yields the lowest dynamic range due to the low virtual integration capacitance in combination with medium analog bandwidth.

Fig. 5.29 shows the resolution or signal-to-noise ratio of the different realized basic photosensing architectures without averaging versus the integration time Δt. Tab. 5.1 indicates the dominant noise sources and shows that the resolution of all realized basic photosensing architectures is basically limited by shot noise, although for the photodiode with active integrator preamplifier thermal noise is slightly more dominant. The resolution limited by shot noise depends on the virtual integration capacitance and is independent of the integration time according to (3.92) with (3.20), but the resolution may decrease at low integration times due to quantization noise introduced by the limited timing resolution according to (3.134) with (3.23) and (3.2). Averaging would increase the resolution with increasing measurement time by 10 dB per decade for measurement times longer than the minimum integration time according to (3.145) with (3.57) and would yield approximately the same resolution at the same integration time for all architectures independent of their virtual integration capacitance.

Most of the single detector architectures have a virtual integration capacitance of around 800 fF which yields a resolution of around 65 dB. Only the photodiode with passive integrator has a virtual integration capacitance of 8000 fF and yields a 10 dB higher resolution of approximately 75 dB.

	Shot Noise	Preamplifier	1/f Noise	Ramp ADC	Timing
PD+PI	•			•	
PD+AI	(•)	•			
PG+PI	•				
PG+AI	•				(•)
SAPS	•				
PDA+AI	•				(•)
PAPS	•				

Tab. 5.1: Dominant noise sources of the realized basic photosensing architectures.

The array architectures provide spatial averaging and an improvement in resolution of a single array element by the square root of the number of array elements, which yields approximately 12 dB for the realized arrays with 16 elements. Thus the standard active pixel sensor and the photodiode array with active integrator with a virtual integration capacitance of around 800 fF yield a resolution between 75 dB and 80 dB. The photogate active pixel sensor with a virtual integration capacitance of around 80 fF yields a 10 dB lower resolution between 65 dB and 70 dB.

The photodiode array with active integrator achieves the highest resolution because it has the highest sum of virtual integration capacitances considering spatial averaging. The photodiode with active integrator yields the lowest resolution due to the lowest virtual integration capacitance and the influence of the preamplifier thermal noise.

Fig. 5.30 shows the sensitivity or noise-equivalent optical power density of the different realized basic photosensing architectures without bias current and without averaging versus the integration time Δt. The sensitivity is expressed by the noise-equivalent optical power density which is the optical power density divided by the resolution according to (3.150). High sensitivity means low noise-equivalent optical power density. The noise-equivalent optical power density increases with increasing square root of the virtual integration capacitance and decreases with increasing responsivity and integration time as long as shot noise is dominant according to (3.91) and (3.1) with (3.23) and (3.2).

Photodiode architectures yield a higher sensitivity than photogates approxi-

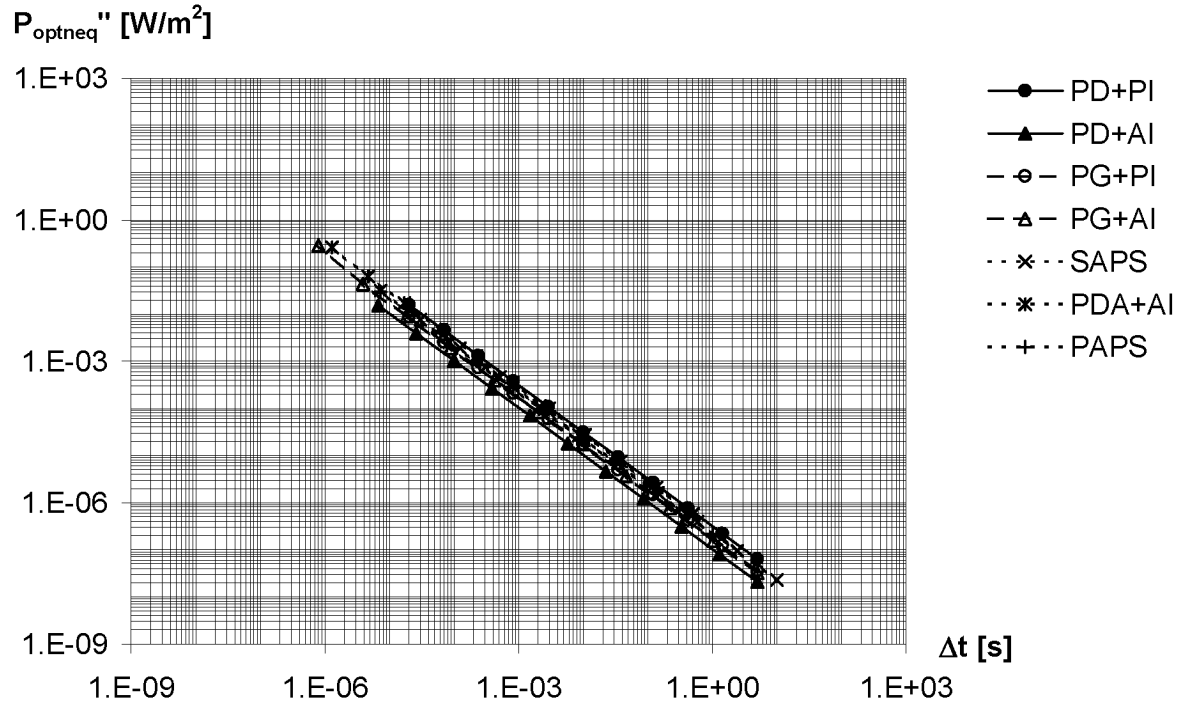


Fig. 5.30: Synopsis of the noise-equivalent optical power density of the realized basic photosensing architectures. ($\lambda = 612$ nm.)

mately by a factor of 2.3 due to the higher responsivity provided they have the same virtual integration capacitance. This is qualitatively demonstrated by the photodiode and photogate with active integrator.
Decreased virtual integration capacitances by a factor of 10 improve the sensitivity approximately by a factor of 3.2 provided the responsivity remains unchanged. This is well demonstrated by the photodiode with active and passive integrator.
Single detector architectures yield a higher sensitivity than array architectures approximately by a factor of 4 due to the lower square root of the sum of virtual integration capacitances provided they have the same responsivity and the same virtual integration capacitance per integrator and array element. This is qualitatively demonstrated by the photodiode and photodiode array with active integrator.
Overall variations in sensitivity of the basic photosensing architectures are less than a factor of 4 as the above effects diminish one another.
The photodiode with passive integrator yields the lowest sensitivity due to the high virtual integration capacitance. The photodiode with active integrator achieves the highest sensitivity due to the high responsivity in combination with medium virtual integration capacitance.
Tab. 5.2 shows the general performance of the realized basic photosensing architectures. It lists the integration time Δt at an optical power density of $P''_{opt0} = 0.1$ W/m^2, the dynamic range without measurement limit, the signal-to-noise ratio at the optical power density of $P''_{opt0} = 0.1$ W/m^2, and the signal-to-noise ratio with averaging at the same optical power density for a measurement time of $\Delta t_A = 10$ s. It shows further the noise-equivalent optical power density P''_{optneq} at an integration time of $\Delta t_0 = 1$ ms, the chip area A_{chip} and the consumed static power P_{DD}.
Tab. 5.3 shows the performance of the realized basic photosensing architectures in a typical application with an optical power density ranging from $P''_{optb1} = 0.1$ mW/m^2 to $P''_{optbmax} = 0.1$ W/m^2 and with a measurement time of $\Delta t_{max} = 1$ ms at a timing resolution of $t_{res} = 100$ ns. The short measurement time requires a bias current I_B as indicated in Tab. 5.3. The indicated minimum integration time Δt_{min} results from the maximum optical power density in combination with the bias current. Tab. 5.3 shows the dynamic range, the signal-to-noise ratio with averaging at the minimum and at the maximum optical power density, and the noise-equivalent optical power density $P''_{optbneq}$ at the minimum optical power density in this typical application with the bias current.

	Δt $@P''_{opt0}$ [ms]	DR [dB]	SNR $@P''_{opt0}$ [dB]	SNR_{avg} $@P''_{opt0}, \Delta t_A$ [dB]	P''_{optneq} $@\Delta t_0$ [μW/m^2]	A_{chip} [mm^2]	P_{DD} [mW]
PD+PI	15.3	108	74	102	310	0.029	0.005
PD+AI	1.35	117	62	101	100	0.057	2
PG+PI	3.85	108	67	101	170	0.024	0.005
PG+AI	3.16	136	66	101	160	0.052	2
SAPS	16.3	123	77	105	230	0.143	0.13
PDA+AI	21.6	112	77	104	290	0.113	2
PAPS	6.49	103	70	101	220	0.138	0.13

Tab. 5.2: General performance of the realized basic photosensing architectures. ($I_B = 0$, $P''_{opt0} = 0.1$ W/m^2, $\lambda = 612$ nm, $\Delta t_0 = 1$ ms, $\Delta t_A = 10$ s.)

	I_B [nA]	Δt_{min} [μs]	DR_b [dB]	SNR_{bavg} $@P''_{optb1}$ [dB]	SNR_{bavg} $@P''_{optbmax}$ [dB]	$P''_{optbneq}$ $@P''_{optbmin}$ [μW/m^2]
PD+PI	8.05	939	50	-10	50	310
PD+AI	0.710	575	63	3	61	68
PG+PI	0.866	794	55	-5	54	180
PG+AI	0.710	759	56	-4	55	160
SAPS	0.537	942	53	-7	52	230
PDA+AI	0.710	956	51	-9	51	270
PAPS	0.0915	866	53	-7	53	220

Tab. 5.3: Performance of the realized basic photosensing architectures in a typical application. ($P''_{optbmax} = 0.1$ W/m^2, $P''_{optb1} = 0.1$ mW/m^2, $\lambda = 612$ nm, $A = 1.5 \cdot 10^{-8}$ m^2, $\Delta t_{max} = 1$ ms, $t_{res} = 100$ ns.)

	I_B [pA]	Δt_{min} [μs]	DR_b [dB]	SNR_{avg} @$P''_{optmax}, \Delta t_A$ [dB]	$P''_{optbneq}$ @$P''_{optbmin}$ [nW/m^2]	$P''_{optbavgneq}$ @$P''_{optbmin}, \Delta t_A$ [nW/m^2]
PD+PI	1.7	20	181	131	67	47
PD+AI	0.15	6.7	179	124	22	16
PG+PI	0.18	20	174	124	36	26
PG+AI	0.15	0.8	201	134	35	24
SAPS	0.054	7.3	199	138	23	23
PDA+AI	1.5	1.3	189	145	610	140
PAPS	0.092	7.3	172	131	220	69

Tab. 5.4: Performance limits of the realized basic photosensing architectures. ($\lambda = 612$ nm, $\Delta t_A = 10$ s.)

Tab. 5.4 shows the performance limits of the realized basic photosensing architectures. The indicated bias current I_B is chosen slightly above the minimum photocurrent i_{phmin} without bias current. Tab. 5.4 lists the minimum integration time Δt_{min}, the maximum dynamic range, the signal-to-noise ratio with averaging at the maximum optical power density for a measurement time of $\Delta t_A = 10$ s, and the minimum noise-equivalent optical power densities $P''_{optbneq}$ without averaging and $P''_{optbavgneq}$ with averaging for a measurement time of $\Delta t_A = 10$ s.
Tab. 5.5 shows the dominant noise sources of the realized basic photosensing architectures with a large photodetector with a high photodetector capacitance of $C_{ph} = 600$ pF in contrast to Tab. 5.1. It confirms that photodetector capacitance has a strong impact on noise performance and shows that noise sources other than shot noise become limiting at high photodetector capacitances.

5.4 Conclusions

The basic photosensing architectures in standard CMOS technology are principally the combinations of the basic photodetectors, which are the photodiode and photogate, and the basic integrator circuits, which are the passive and the active integrator. In addition, the photodetector element can be built of a single

	Shot Noise	Preamplifier	1/f Noise	Ramp ADC	Timing
PD+PI				•	
PD+AI		(•)	•		
PG+PI				•	
PG+AI		(•)	•		
SAPS				•	
PDA+AI		•			
PAPS				•	

Tab. 5.5: Dominant noise sources of the realized basic photosensing architectures with a large photodetector ($C_{ph} = 600$ pF).

detector or an array of smaller detectors. CCDs are not realizable in modern standard CMOS technology.

Tab. 5.6 shows the typical properties of the basic photosensing architectures with respect to performance. "+"means advantageous and "++"very favorable value for high performance, whereas "−"means disadvantageous and "−−"very unsuitable value concerning performance. Tab. 5.6 characterizes the basic photosensing architectures with regard to high responsivity R_λ, zero voltage across the sensing diode v_D, low preamplifier thermal noise contribution i_{n_p}, independent integration capacitance C_{int}, variable virtual integration capacitance C_{virt}, low voltage amplifier thermal noise contribution v_{n_a} or transconductor thermal noise contribution i_{n_g}, stable voltage amplifier gain a or transconductor value g, and compatibility with current ramp analog-to-digital converter IRADC. The resulting performance of the different basic photosensing architectures is compared in Tab. 5.7. It characterizes speed, dynamic range, resolution, sensitivity, chip area and power consumption.

Speed performance is basically determined by the transfer factor which depends on the responsivity and the virtual integration capacitance. The virtual integration capacitance is approximately equal to the integration capacitance for all the basic photosensing architectures as their preamplifier and voltage amplifier have all approximately unity gain.

Dynamic range basically depends on the voltage across the sensing diode, which determines the dark current, and as well the virtual integration capacitance or the integration capacitance itself.

	R_λ	v_D	i_{n_p}	C_{int}	C_{virt}	v_{n_a}, i_{n_g}	a,g	**IRADC**
PD+PI	+	−−	++	−−	−	+	+	−
PD+AI	+	+	−	+	−	−	+	−
PG+PI	−	−−	++	−	−	+	+	−
PG+AI	−	−	−	+	−	−	+	−
SAPS	+	−−	++	−−	−	+	+	−
PDA+AI	+	+	−−	+	−	−	+	−
PAPS	−	−−	++	−	−	+	+	−

Tab. 5.6: Typical properties of the basic photosensing architectures (High responsivity R_λ, zero voltage across the sensing diode v_D, low preamplifier thermal noise contribution i_{n_p}, independent integration capacitance C_{int}, variable virtual integration capacitance C_{virt}, low voltage amplifier thermal noise contribution v_{n_a} or transconductor thermal noise contribution i_{n_g}, stable voltage amplifier gain a or transconductor value g, compatibility with current ramp analog-to-digital converter IRADC.

	Speed	**Dynamic Range**	**Resolution**	**Sensitivity**	**Chip Area**	**Power Consumption**
PD+PI	−−	−	+	−	++	++
PD+AI	+	+	−	+	−	−
PG+PI	−	−	+	−	++	++
PG+AI	−	−	−	−	−	−
SAPS	−−	−	+	−	−	+
PDA+AI	−	−	−	−	−	−
PAPS	−	−	+	−	−	+

Tab. 5.7: Synopsis of the performance of the basic photosensing architectures.

Resolution is basically limited by the preamplifier and amplifier thermal noise contributions provided the fundamental shot noise limit is not reached, which can be controlled by the measurement time.
Sensitivity is basically determined by the voltage across the sensing diode, the preamplifier and amplifier thermal noise contributions as well as the transfer factor, which depends on the responsivity and the virtual integration capacitance or the integration capacitance itself.
Photodiode architectures are principally faster than photogate architectures due to their higher responsivity, provided they have the same virtual integration capacitance. For architectures that yield the photodetector capacitance being part of the integration capacitance, the photogate solutions usually achieve significantly higher speeds due to their reduced photodetector capacitance. Therefore the photogate with passive integrator and the photogate active pixel sensor are much faster than the photodiode with passive integrator and the standard active pixel sensor. In addition, the photogate solutions can achieve higher resolution if preamplifier thermal noise is dominant, as they have reduced photodetector capacitance.
Active integrator architectures can principally achieve higher speed than passive integrator architectures, as the integration capacitance of active integrators can be chosen independent of the photodetector capacitance, which is very obvious for the photodiode with active or passive integrator. Passive integrator architectures generally achieve higher resolution, as the preamplifier and amplifier thermal noise contributions of active integrators are higher due to the use of complete operational amplifiers. But active integrators have potential for high sensitivity, as they can provide constant zero voltage across the sensing diode resulting in very low dark current. Passive integrators consume little chip area and power due to their simple transistor stages. Therefore the photodiode and photogate with passive integrator have smallest chip area and lowest power consumption.
The performance of array architectures is basically equivalent to that of single detector architectures, although the arrays consume more chip area and power and they require much more complex circuits for result evaluation. In addition, parasitic elements are more effective in arrays as the single elements are smaller.
From the realized architectures the photodiode with active integrator achieves the highest speed and therefore the highest dynamic range in a typical application due to its high transfer factor resulting from the high responsivity and low virtual integration capacitance. However, the photogate with active integrator

achieves the lowest limit in integration time and therefore generally the highest dynamic range due to its high analog bandwidth, provided the optical power density can be freely adjusted. The photodiode with passive integrator and the standard active pixel sensor are slow because they do not provide separation of their integration capacitance from their high photodetector capacitance and due to their low analog bandwidth.
The noise performance of all these realizations is basically limited by shot noise. Speed performance can be exchanged with resolution by changing the virtual integration capacitance if applicable to the circuit. This can result in other noise contributions to limit the performance.
The highest resolution of the realized architectures is achieved by the photodiode with passive integrator, the standard active pixel sensor and the photodiode array with active integrator resulting directly from their high virtual integration capacitance. The basic signal-to-noise ratio of approximately 75 dB can still be improved by averaging. In a typical application the photodiode with active integrator may achieve the highest resolution after averaging, as its high speed does not demand high bias currents, which introduce additional noise.
The photodiode with active integrator achieves the highest sensitivity due to its high transfer factor resulting from the high responsivity and low virtual integration capacitance. The lowest noise-equivalent optical power density for a measurement time of 10 s is approximately 10 nW/m^2.
The smallest chip area and the lowest power consumption are both achieved by the photodiode and photogate with passive integrator due to their simple structure.
All of the basic photosensing architectures provide high stability in transfer factor due to the feedback structure of the amplifiers. They are all based on voltage ramps and therefore not compatible with current ramp analog-to-digital converters such as in current-mode circuits.
Experimental results demonstrate a good agreement with the integrating sampled-data photosensing model. Measurement results are degraded by line interferences due to the "contaminated" environment and insufficient shielding. Line interferences are effective as long as the period of the power line is somewhere in the interval ranging from the integration time to the total measurement time.

6. ADVANCED PHOTODETECTORS FOR LARGE-AREA PHOTOSENSING

In this chapter advanced photodetectors for large-area photosensing in CMOS technology with low photodetector capacitance and sufficient speed performance are introduced. First the charge transport in photogates is investigated. Then a photogate with increased speed performance is discussed and an optimized photogate concept with very high speed performance is proposed. The introduced photodetectors are realized and characterized in standard CMOS technology.

6.1 Charge Transport in Photogates

The photogate as described in Section 4.2 causes a depletion region or space charge region in the semiconductor with an electric field as calculated in Appendix B. The normal component of the electric field provides charge transport in the semiconductor perpendicular to the surface and collects the charge in a thin inversion layer at the surface. The lateral charge transport in the inversion layer is characterized by the current density equation

$$j_x = \mu \left| q_s''' \right| E_x - D \frac{\partial q_s'''}{\partial x} \tag{6.1}$$

considering drift and diffusion according to (B.23) and (B.24). j_x is the surface current density in lateral direction per unit area, μ the mobility, q_s''' the surface charge density per unit volume, E_x the surface electric field in lateral direction, and D the diffusion constant. Using the continuity equation

$$\frac{\partial q_s'''}{\partial t} = -\frac{\partial j_x}{\partial x}, \tag{6.2}$$

where generation and recombination are not taken into account, the transport equation results to

$$\frac{\partial q_s'''}{\partial t} = \frac{\partial}{\partial x}\left[-\mu\left|q_s'''\right| E_x + D\frac{\partial q_s'''}{\partial x}\right]. \tag{6.3}$$

The surface electric field E_x is

$$E_x = -\frac{\partial \phi_s}{\partial x}, \tag{6.4}$$

where ϕ_s is the surface potential approximated by

$$\phi_s \approx \phi_{s0} + \gamma_s\left(v_G - V_{FB} + \frac{q_s''}{C_{ox}''}\right) \tag{6.5}$$

according to (B.72) with the surface potential approximation coefficient $\gamma_s \approx 0.8$ according to (B.73) and Fig. B.5. v_G is the gate voltage referred to the substrate contact, q_s'' is the surface charge density per unit area, C_{ox}'' is the specific oxide capacitance per unit area, and ϕ_{s0} and V_{FB} are constants. Using (6.4) and (6.5) the surface electric field results to

$$E_x \approx -\gamma_s\left(\frac{\partial v_G}{\partial x} + \frac{1}{C_{ox}''}\frac{\partial q_s''}{\partial x}\right). \tag{6.6}$$

The left part in this expression represents the external drift field or fringing field resulting from the gate voltage profile, and the right part represents the self-induced drift field of the charge carriers. Integrating (6.3) in vertical direction and using (6.6) yields the modified transport equation with the three contributions referring to externally induced drift, self-induced drift and diffusion [85][86][87][88][89]:

$$\frac{\partial q_s''}{\partial t} = \frac{\partial}{\partial x}\left[\mu\gamma_s\left|q_s''\right|\left(\frac{\partial v_G}{\partial x} + \frac{1}{C_{ox}''}\frac{\partial q_s''}{\partial x}\right) + D\frac{\partial q_s''}{\partial x}\right]. \tag{6.7}$$

The charge distribution in the photogate as a function of time can be evaluated in different ways each yielding the same result. Either the appropriate difference equation according to (6.7) can be solved numerically using a matrix computation software such as MATLAB [86][89]. Or an equivalent distributed electrical circuit model with lumped discrete elements that represents (6.7) can be simulated using a SPICE-like circuit simulator such as PSTAR [90][91][92]. Or the

physical photogate structure can be simulated by finite elements using a device simulator that includes the transport mechanisms according to (6.7) such as ISE-TCAD.
In the standard photogate as described in Section 4.2 the gate voltage has constant value along the whole photogate and the externally induced drift component in (6.7) is cancelled. The resulting charge distribution versus time caused only by self-induced drift and diffusion is qualitatively shown in Fig. 6.1 for an initial charge packet at the beginning of the photogate structure. The x-axis represents the location in the photogate, where the beginning is all to the right and the end all to the left. The t-axis represents the time proceeding from left behind to right in front. It illustrates the decay of the charge packet and that no useful net charge propagation is obtained due to the omnidirectional spreading. The charge transport to the output of the photogate is very slow due to these mechanisms.

6.2 Constant Lateral Field Photogate (CPG)

The constant lateral field photogate is a photogate with a constant lateral voltage V_L across the gate by applying different voltages to the beginning and the end of the gate as shown in Fig. 6.2 [93]. As the gate is fabricated in high-resistive polysilicon in order to minimize the lateral static current flowing through the gate, the constant lateral field photogate is also known as resistive-gate sensor [94][95]. The gate voltage is a linear function of the gate location and the resulting surface potential profile in Fig. 6.2 shows a surface potential gradient in the desired transport direction under the gate. This illustrates the presence of the externally induced drift component in (6.7) in contrast to the standard photogate as described in Section 4.2.
The charge distribution versus time for the constant lateral field photogate is qualitatively shown in Fig. 6.3 for an initial charge packet at the beginning of the photogate structure analogous to Fig. 6.1 [93][96]. It illustrates the decay of the charge packet according to Fig. 6.1 and in addition the propagation of the whole charge packet to the output due to the external drift field caused by the applied lateral voltage V_L. This large and unidirectional lateral drift field yields fast charge transport and therefore high speed.
The increased power consumption due to the static lateral gate current limits the benefit of this photodetector in low-power applications.

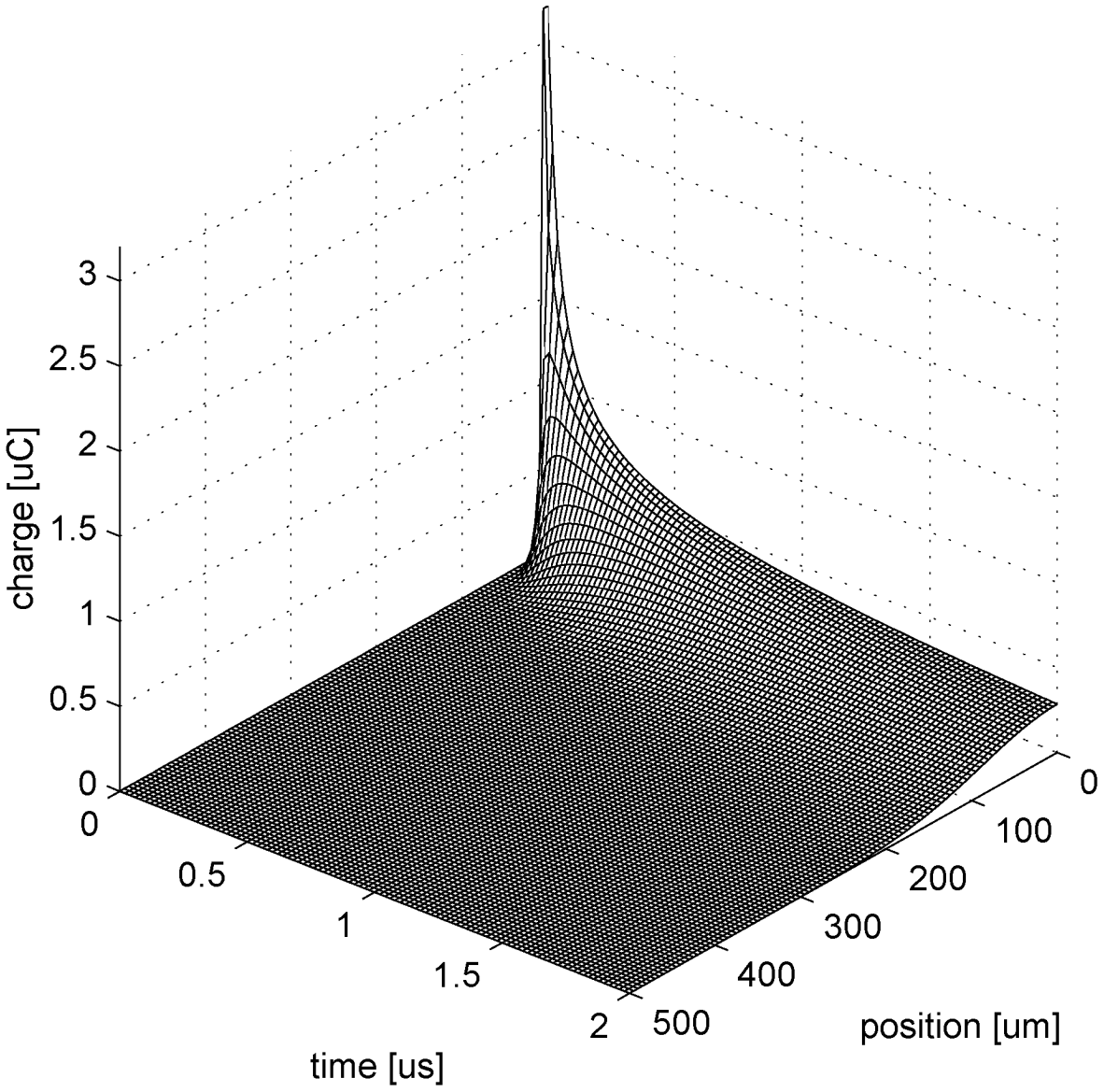


Fig. 6.1: Simulated charge distribution versus time of the standard photogate.

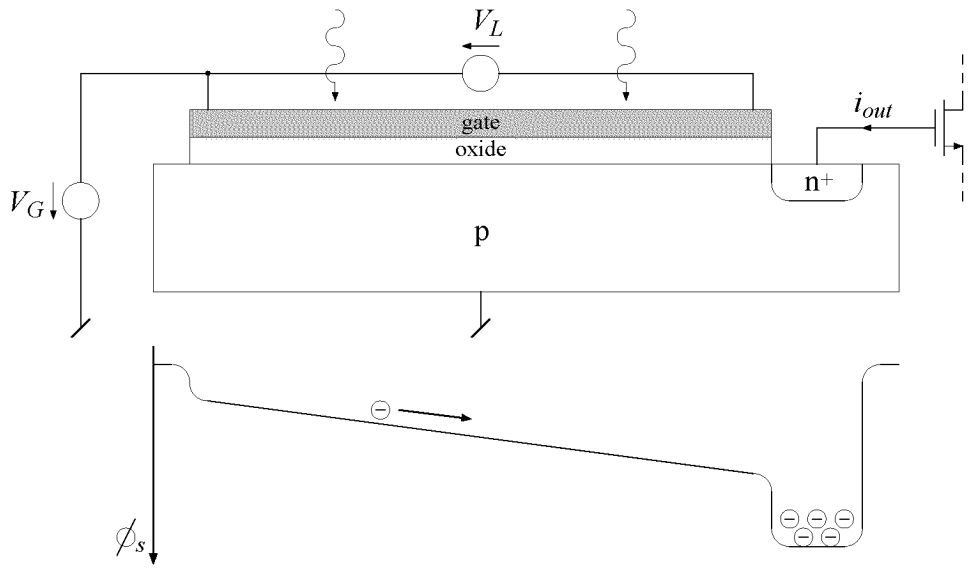


Fig. 6.2: Constant lateral field photogate (CPG). Cross section and surface potential profile ϕ_s.

6.2.1 Constant Lateral Field Photogate with Passive Integrator (CPG+PI)

The realized constant lateral field photogate with passive integrator is the same circuit as shown in Fig. 5.10 using the constant lateral field photogate as photodetector. Fig. 6.4 shows the measured output signal of the constant lateral field photogate with passive integrator for different lateral voltages V_L. After the reset phase governed by the reset control signal a 100 μs long light pulse is applied to the beginning of the photogate after a short delay of 100 μs as illustrated by the light pulse control signal. The photogenerated charge is then transported across the 500 μm long photogate with different speeds according to the different lateral voltages V_L. $V_L = 0$ V refers to the standard photogate as described in Section 4.2 and yields the slowest charge transfer and thus the largest decay of the charge packet resulting in a strongly delayed and deformed output signal. The output signals for $V_L = 0.2$ V, 0.4 V and 0.6 V illustrate the accelerated charge transport and the reduced decay of the charge packets resulting from the lateral voltage V_L. The output signal for $V_L = 0.6$ V shows a complete charge transfer to the output after some tens of microseconds shortly after the end of the light pulse, whereas $V_L = 0$ V needs more than a millisecond.

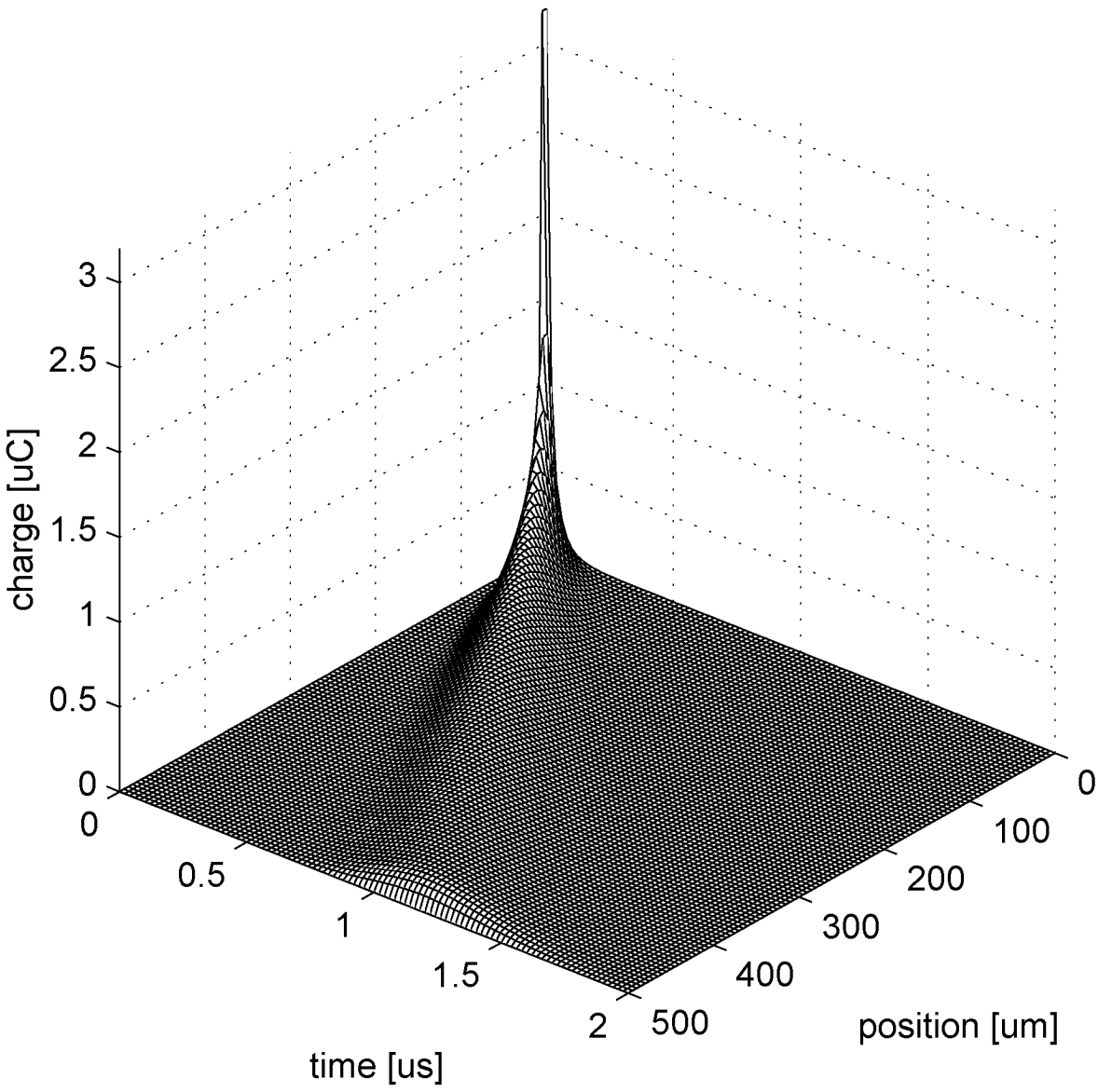


Fig. 6.3: Simulated charge distribution versus time of the constant lateral field photogate.

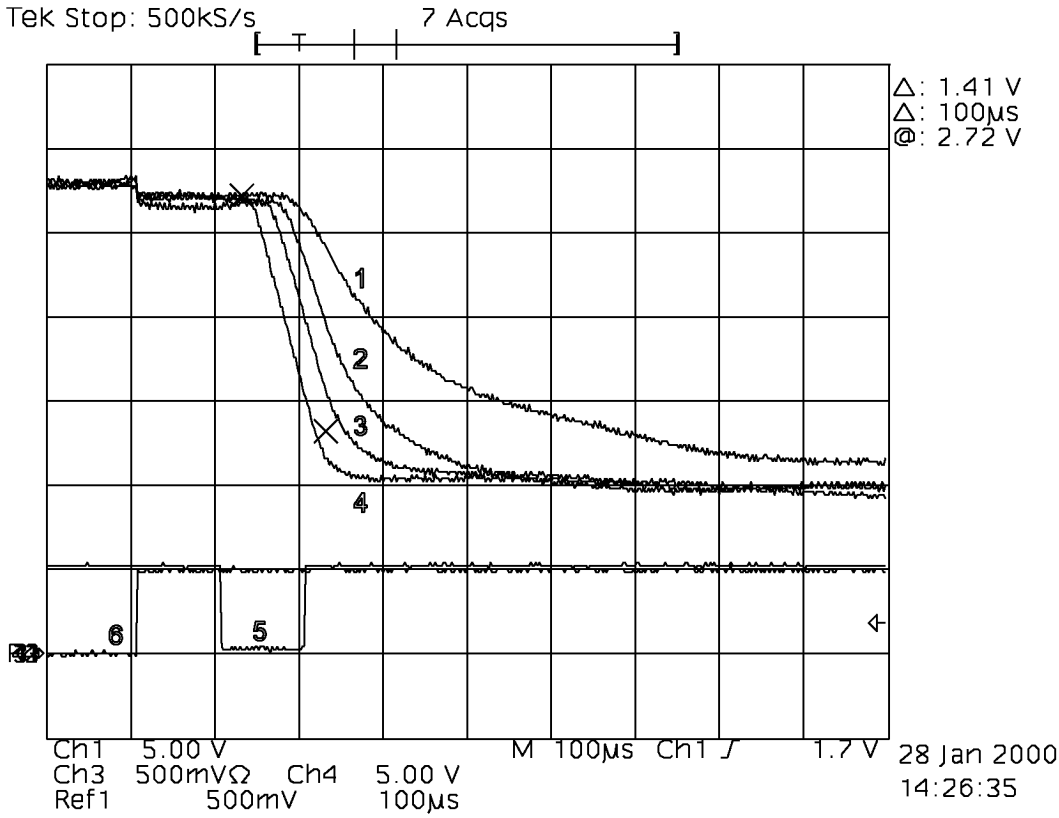


Fig. 6.4: Measured output signal of the constant lateral field photogate with passive integrator (CPG+PI) for different lateral voltages V_L. (1) $V_L = 0$ V, (2) $V_L = 0.2$ V, (3) $V_L = 0.4$ V, (4) $V_L = 0.6$ V. (5) Light pulse control signal. (6) Reset control signal.

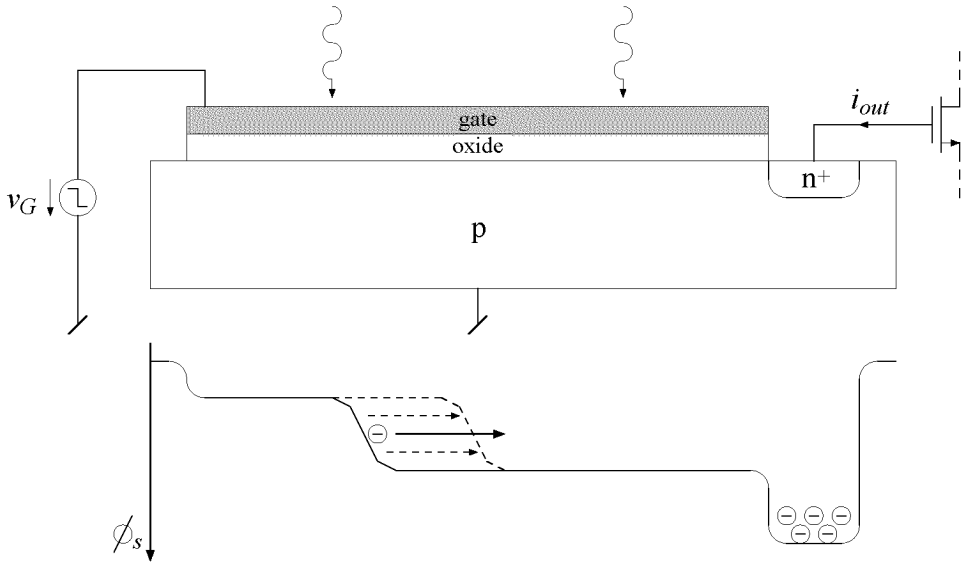


Fig. 6.5: Sweep photogate (SPG). Cross section and surface potential profile ϕ_s.

6.3 Sweep Photogate (SPG)

The sweep photogate concept is based on a fast traveling drift pulse with high lateral drift field that sweeps along the photogate as shown in Fig. 6.5 [97]. The idea is that initially the gate voltage is at constant potential. For readout a voltage step is applied to the beginning of the gate yielding a high local gate voltage gradient that rapidly propagates towards the end of the gate which forms a transmission line. Along with the local gate voltage gradient a high local surface potential gradient sweeps towards the end of the photogate and builds a fast traveling drift pulse that transports the photogenerated charge carriers and accumulates them in front of this sweeping gradient in the surface potential profile as shown in Fig. 6.5.
The sweeping readout using the fast traveling drift pulse with high lateral drift field yields very high speed and moderate power consumption as the lateral gate current is applied very locally and only during readout.
The MOS structure of the sweep photogate is a sort of microstrip line and forms a transmission line [98][99][100]. The transmission line is characterized by the following differential equations:

$$\begin{aligned} -\frac{\partial v_G}{\partial x} &= R'_G i_G + L'_G \frac{\partial i_G}{\partial t} \\ -\frac{\partial i_G}{\partial x} &= G'_G v_G + C'_G \frac{\partial v_G}{\partial t}. \end{aligned} \tag{6.8}$$

v_G is the gate voltage referred to the substrate contact and i_G is the gate current in lateral direction. R'_G, L'_G, G'_G and C'_G are the specific gate resistance, inductance, conductance and capacitance per unit length. Combining the above differential equations yields the Telegrapher's equations

$$\begin{aligned}\frac{\partial^2 v_G}{\partial x^2} &= R'_G G'_G v_G + (R'_G C'_G + L'_G G'_G)\frac{\partial v_G}{\partial t} + L'_G C'_G \frac{\partial^2 v_G}{\partial t^2} \\ \frac{\partial^2 i_G}{\partial x^2} &= R'_G G'_G i_G + (R'_G C'_G + L'_G G'_G)\frac{\partial i_G}{\partial t} + L'_G C'_G \frac{\partial^2 i_G}{\partial t^2}. \end{aligned} \quad (6.9)$$

For sinusoidal excitation the complex notation can be used and the Telegrapher's equations transform to the wave equations

$$\begin{aligned}\frac{\partial^2 \underline{V}_G}{\partial x^2} &= \underline{\gamma}_G^2 \underline{V}_G \\ \frac{\partial^2 \underline{I}_G}{\partial x^2} &= \underline{\gamma}_G^2 \underline{I}_G, \end{aligned} \quad (6.10)$$

where the propagation constant $\underline{\gamma}_G$ is

$$\underline{\gamma}_G = \sqrt{(R'_G + j\omega L'_G)(G'_G + j\omega C'_G)} = \alpha_G + j\beta_G \quad (6.11)$$

with the attenuation constant α_G and the phase constant β_G. The algebraic solution of the wave equations yields the transmission line equations as a superposition of incident and reflected waves:

$$\begin{aligned}\underline{V}_G(x) &= \frac{1}{2}(\underline{V}_1 + \underline{Z}_G \underline{I}_1)e^{-\underline{\gamma}_G x} + \frac{1}{2}(\underline{V}_1 - \underline{Z}_G \underline{I}_1)e^{\underline{\gamma}_G x} \\ \underline{I}_G(x) &= \frac{1}{2}\left(\frac{\underline{V}_1}{\underline{Z}_G} + \underline{I}_1\right)e^{-\underline{\gamma}_G x} - \frac{1}{2}\left(\frac{\underline{V}_1}{\underline{Z}_G} - \underline{I}_1\right)e^{\underline{\gamma}_G x}. \end{aligned} \quad (6.12)$$

$\underline{V}_1$ is the gate input voltage and $\underline{I}_1$ is the gate input current, and the characteristic impedance $\underline{Z}_G$ is

$$\underline{Z}_G = \sqrt{\frac{R'_G + j\omega L'_G}{G'_G + j\omega C'_G}}. \quad (6.13)$$

The wavelength λ_G is

$$\lambda_G = \frac{2\pi}{\beta_G} \quad (6.14)$$

and the phase velocity v_p is

$$v_p = \frac{\omega}{\beta_G} = \lambda_G f \quad (6.15)$$

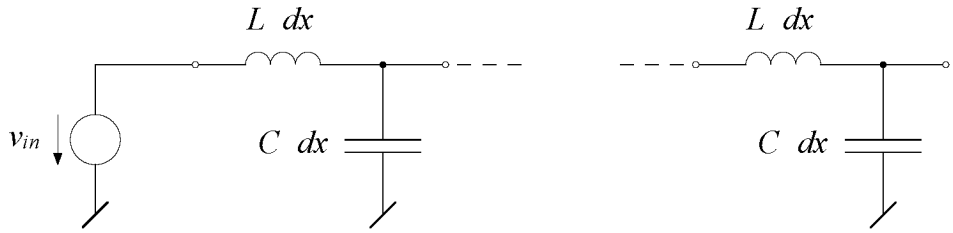


Fig. 6.6: Lossless transmission line model without load impedance.

where f is the frequency. The group velocity v_g is

$$v_g = \frac{\partial \omega}{\partial \beta_G}. \tag{6.16}$$

Ideal propagation of the traveling drift pulse in the sweep photogate would be achieved if the MOS structure was a lossless transmission line. The lossless transmission line is free of resistive elements and can be modeled as shown in Fig. 6.6. The propagation constant $\underline{\gamma}_G$ is

$$\underline{\gamma}_G = j\omega\sqrt{L'_G C'_G} \tag{6.17}$$

and the attenuation constant α_G is zero:

$$\alpha_G = 0. \tag{6.18}$$

The phase constant β_G is

$$\beta_G = \omega\sqrt{L'_G C'_G} \tag{6.19}$$

and the phase velocity v_p and the group velocity v_g result to

$$v_p = v_g = \frac{1}{\sqrt{L'_G C'_G}}. \tag{6.20}$$

This means that there is no attenuation of the traveling pulse along the transmission line and the pulse has a constant shape.
The gate voltage and charge distributions versus time for the ideal sweep photogate assuming a lossless transmission line are qualitatively shown in Fig. 6.7

and Fig. 6.8 for an initial charge packet at the beginning of the photogate structure analogous to Fig. 6.1. They illustrate the fast and constant propagation of the local gate voltage gradient and the fast and complete charge transport by the traveling drift pulse.

The specific gate conductance G'_G of a MOS structure is typically negligible compared to its specific gate capacitance C'_G. But resistive losses due to the specific gate resistance R'_G have to be taken into account and the specific gate inductance L'_G dominates the characteristics of the transmission line only at high frequencies, where

$$R'_G < \omega L'_G. \tag{6.21}$$

Using a typical sheet resistance of $0.1\ \Omega$ the specific gate resistance of a $10\ \mu$m wide metal line results to $R'_G \approx 10$ kΩ/m. For a minimum frequency of 100 MHz the specific gate inductance according to (6.21) has to be $L'_G > 16\ \mu$H/m. Transmission line inductances of metal lines are typically in the order of some 100 nH/m to about $1\ \mu$H/m and therefore at least about two orders of magnitude too low [101][102]. However spiral inductors using metal lines can be used to achieve increased inductance [103][102][104][105]. Their inductance is typically some nH for an inductor area of $100\ \mu\text{m} \times 100\ \mu$m. This yields some tens of μH/m in a linear dimension for a series of discrete spiral inductors, which is barely high enough to satisfy (6.21). Similar inductance values can be achieved using active inductors built of transistors [106].

Neglecting the specific gate resistance the group velocity is given by (6.20). This velocity determines the local gate voltage gradient caused by the voltage step applied to the beginning of the gate. For a voltage step applied in 10 ns with a desired maximum dimension of $10\ \mu$m the maximum group velocity results to $v_p = 10^3$ m/s. The maximum achievable specific gate capacitance for a specific capacitance per unit area of about $1\ \text{mF/m}^2$ with a maximum width of about 10 mm is $C'_G \approx 10\ \mu$F/m. This specific gate capacitance and the above group velocity applied to (6.20) yields a required specific gate inductance of $L'_G \approx 0.1$ H/m. This is many orders of magnitude higher than what is realizable according to the above discussion.

Real sweep photogate structures are lossy transmission lines in form of MOS transmission lines [91][107]. The specific gate inductance L'_G in that kind of lossy transmission lines is negligible compared to the specific gate resistance R'_G and the MOS transmission line can be modeled as shown in Fig. 6.9. The Telegrapher's equation for the gate voltage in (6.9) then reduces to the diffusion equation

$$\frac{\partial^2 v_G}{\partial x^2} = R'_G C'_G \frac{\partial v_G}{\partial t}. \tag{6.22}$$

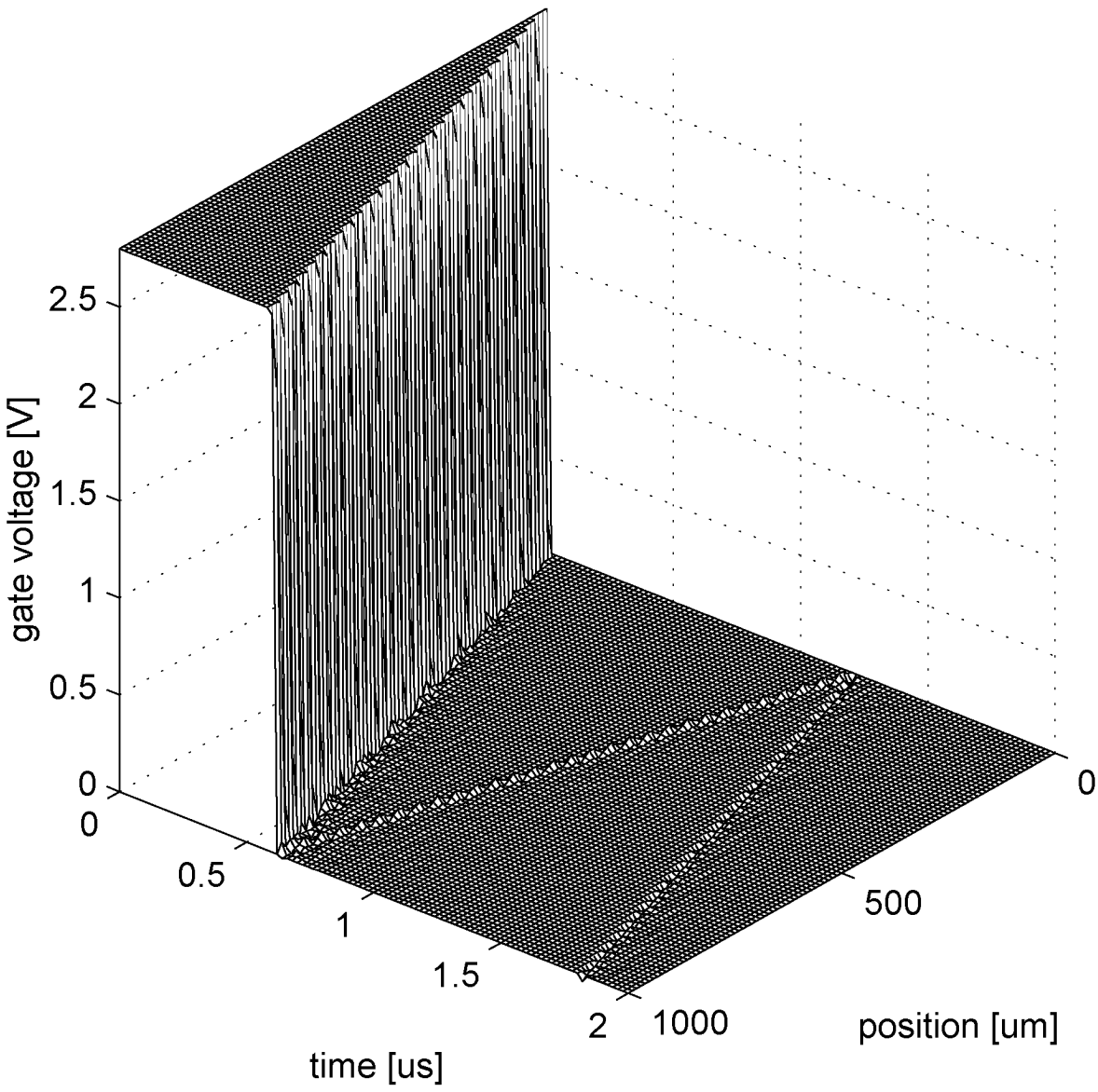


Fig. 6.7: Simulated gate voltage distribution versus time of the ideal sweep photogate.

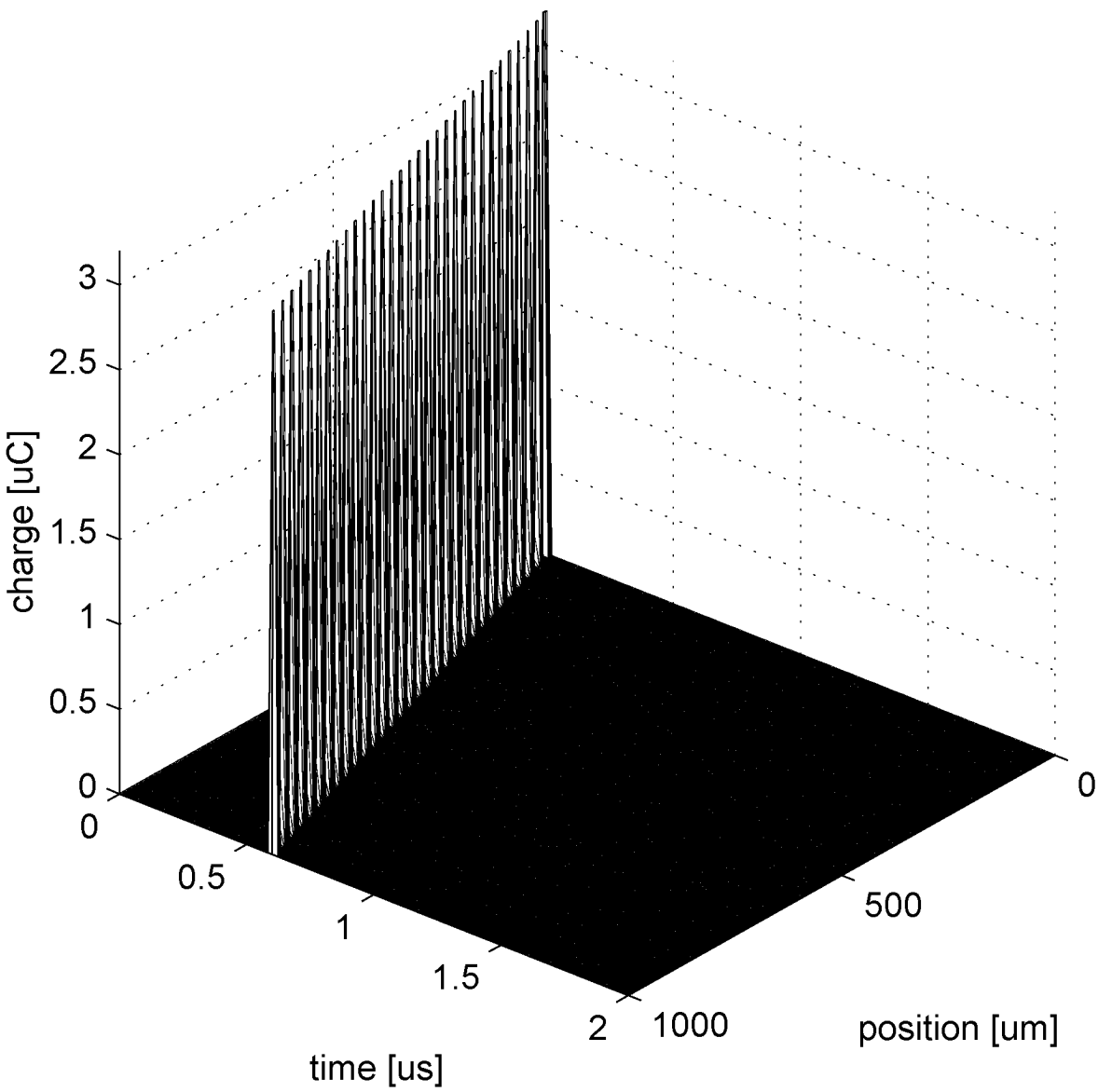


Fig. 6.8: Simulated charge distribution versus time of the ideal sweep photogate.

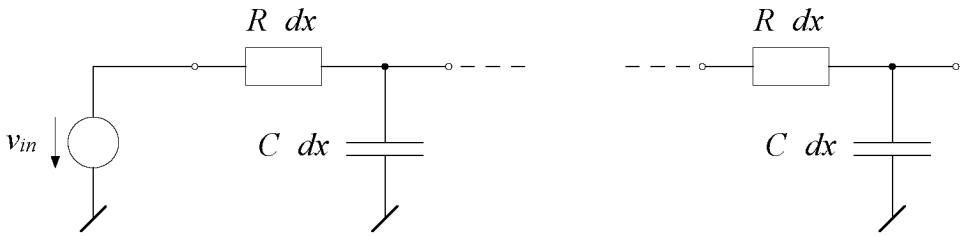


Fig. 6.9: MOS transmission line model without load impedance.

This means that the transient behavior of the gate voltage is characterized by strong attenuation and deformation due to the resistive losses, which decreases the charge transport speed towards the end of the gate.
The gate voltage and charge distributions versus time for the real sweep photogate assuming an MOS transmission line are qualitatively shown in Fig. 6.10 and Fig. 6.11 for an initial charge packet at the beginning of the photogate structure analogous to Fig. 6.1 [91][108]. They illustrate the diffusion-like spreading of the local gate voltage gradient and the attenuation of the traveling drift pulse resulting in decreasing charge transport speed towards the end of the gate.
The effect of speed attenuation along the photogate due to transmission line losses can be reduced by extending the gate beyond the floating diffusion at the output or by terminating the transmission line with an appropriate load impedance.

6.3.1 Shifted Sweep Photogate with Sensitive Passive Integrator (SSPG+SPI)

The shifted sweep photogate is an uncritical implementation of the sweep photogate concept where the local gate voltage is externally controlled through a high number of gate contacts by digital voltage and timing control circuitry [109][110]. The gate is subdivided in a high number of segments each having its own gate contact. The voltage applied to this gate contact is controlled by a storage cell allocated to the segment. In the shifted sweep photogate the series of the storage cells of all the successive segments builds a long shift register that passes values from cell to cell at each clock cycle. Thus variable gate voltage profiles can be swept along the photogate at variable speeds controlled by the clock signal. This scheme is similar to the charge-coupled devices (CCD) operation, but it overcomes the problem of insufficient charge transfer

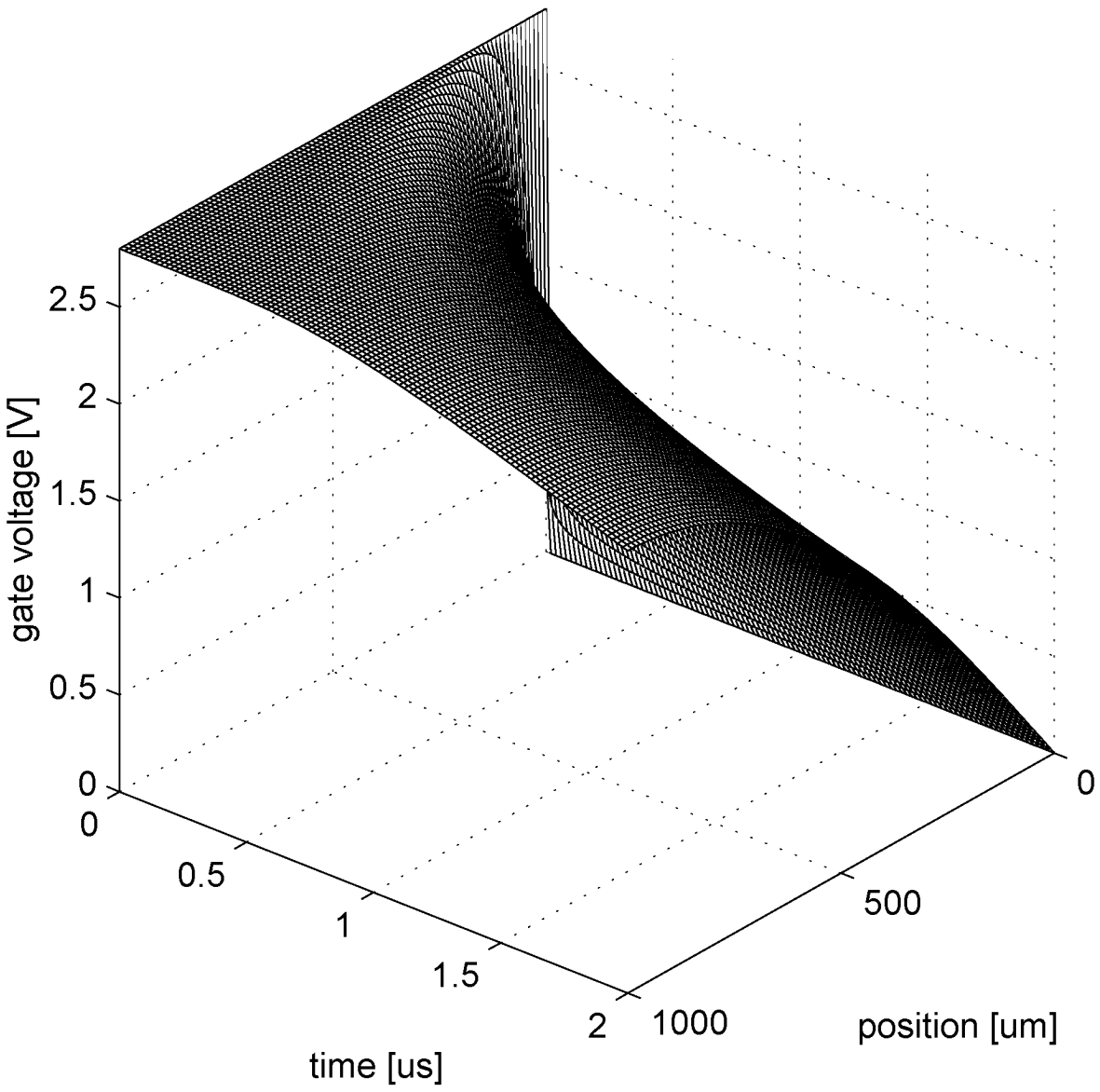


Fig. 6.10: Simulated gate voltage distribution versus time of the real sweep photogate.

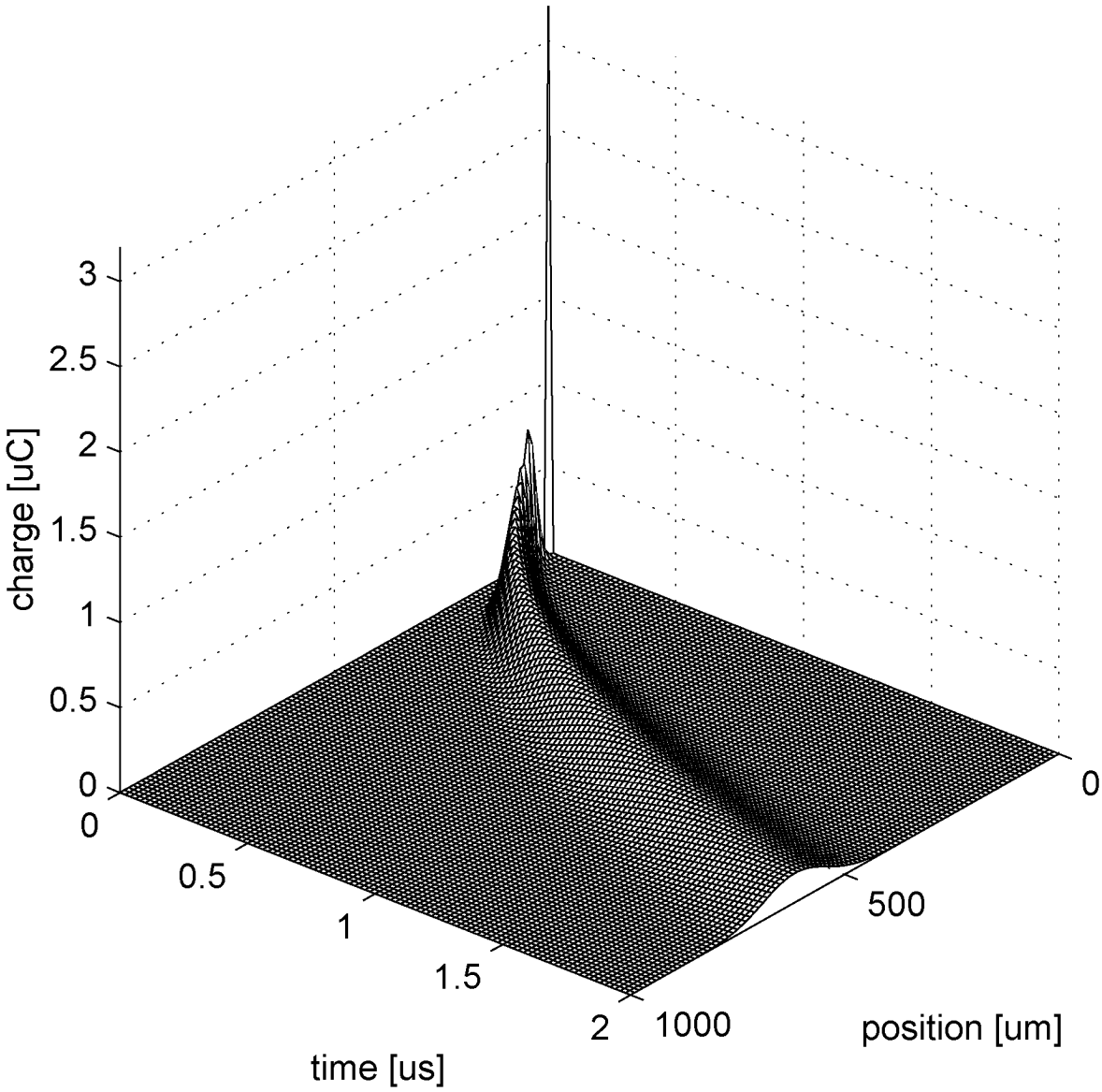


Fig. 6.11: Simulated charge distribution versus time of the real sweep photogate.

due to surface potential barriers caused by interelectrode spacings or gaps.
The realized shifted sweep photogate with sensitive passive integrator is the same circuit as shown in Fig. 5.10 but with a lower integration capacitance C_1 and using the shifted sweep photogate as photodetector. Fig. 6.12 shows the measured output signal of the shifted sweep photogate with sensitive passive integrator for different operating modes referring to different gate voltage profiles. Immediately after the reset phase governed by the reset control signal a 1.1 μs long light pulse is applied to the middle of the 500 μm long photogate. The photogenerated charge is then transported to the output of the photogate with different speeds according to the different operating modes. The transferred charge is represented by the difference between the output signal and the dark signal, which is the output signal caused by the dark current. The dark signal for the shifted sweep photogate mode is different from that for the standard photogate and constant lateral field photogate modes due to capacitive coupling from clock signals. But the difference between the output signal after complete charge transfer and the dark signal is constant for all modes since this difference represents the total photogenerated charge of the light pulse. The standard photogate mode yields the slowest charge transfer and thus the largest decay of the charge packet resulting in a strongly delayed and deformed output signal in accordance with Fig. 6.4. The constant lateral field photogate mode with a constant lateral voltage $V_L = 1$ V yields increased charge transport speed and reduced decay of the charge packet resulting from the lateral drift field. The shifted sweep photogate mode with a gate voltage gradient of 1 V achieves very fast charge transport and very compact transfer of the charge packet due to the high local lateral drift field that is swept across the whole photogate in 270 μs. The output signal for the shifted sweep photogate mode shows a complete charge transfer to the output after some hundreds of microseconds, whereas the constant lateral field photogate mode needs several miliseconds and the standard photogate mode some tens of miliseconds.

6.4 Conclusions

Charge transport in photogates is driven by diffusion and drift. Fast charge transport is achieved by high unidirectional drift fields, whereas diffusion is omnidirectional and slow.
The constant lateral field photogate is a simple photodetector with low photodetector capacitance and moderate speed. It is significantly faster than the standard

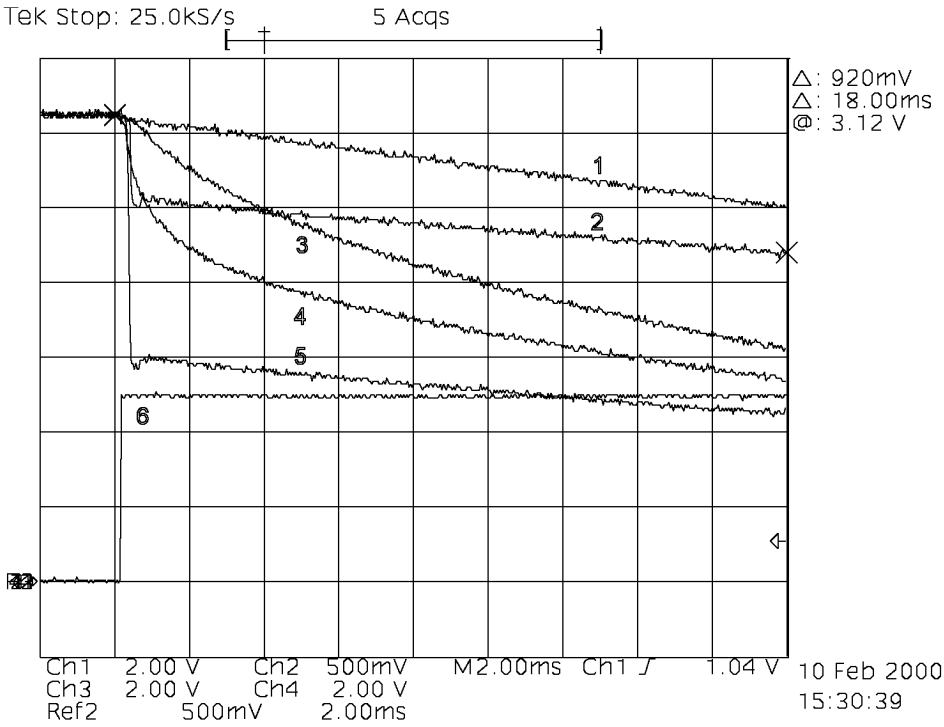


Fig. 6.12: Measured output signal of the shifted sweep photogate with sensitive passive integrator (SSPG+SPI) for different operating modes. (1) Dark signal for standard photogate and constant lateral field photogate mode, (2) dark signal for shifted sweep photogate mode. (3) Standard photogate mode, (4) constant lateral field photogate mode, (5) shifted sweep photogate mode. (6) Reset control signal.

photogate as its charge transport is dominated by drift instead of diffusion. The static lateral gate current results in increased power consumption.
The proposed sweep photogate concept yields fast large-area photodetectors with low photodetector capacitance at low power consumption. Its charge transport is based on fast traveling drift pulses with high local lateral drift fields that sweep across the whole photogate and are applied for only a short time period.
The shifted sweep photogate is a flexible implementation of the sweep photogate concept yielding low photodetector capacitance and high speed.
The photodetector capacitance of a 10'000 μm $\times$ 100 μm large standard, constant lateral field or shifted sweep photogate is about three decades smaller than that of a p-diffusion/n-well photodiode of the same area.
The realized 500 μm long shifted sweep photogate is approximately two decades and the constant lateral field photogate approximately one decade faster than the standard photogate of the same length.
The reduced responsivity of photogates compared to photodiodes can be improved by covering only a portion of the photodetector area with the gate layer instead of the whole area, although this influences the speed performance.

7. ADVANCED ARCHITECTURES FOR LARGE-AREA PHOTOSENSING

This chapter introduces a system architecture that can be implemented in the current-mode and suitable circuit techniques are investigated. An advanced architecture for large-area photosensing in CMOS technology that yields high resolution and simple analog-to-digital conversion is developed and its performance is derived using the integrating sampled-data photosensing model. This advanced architecture for large-area photosensing is realized and characterized in standard CMOS technology and compared to the realized basic photosensing architectures.

7.1 Current-Mode Architecture

A photocurrent measurement system for integrating sampled-data photosensing in the current-mode basically consists of a photocurrent source, a photocurrent converter and a digital signal processor (DSP) as shown in Fig. 7.1 [111]. The photocurrent source fundamentally contains a photodetector and some additional circuitry that provides current source characteristics at the output. The photocurrent converter consists of an integrator, an amplifier and a ramp analog-to-digital converter (ramp ADC). The digital signal processor (DSP) may be any digital system that further processes the digital data delivered by the ramp ADC.

7.2 Photodiode Current Source (PDCS)

The photodiode current source as shown in Fig. 7.2 represents a photocurrent source to be used in current-mode architectures [111]. Operational amplifier

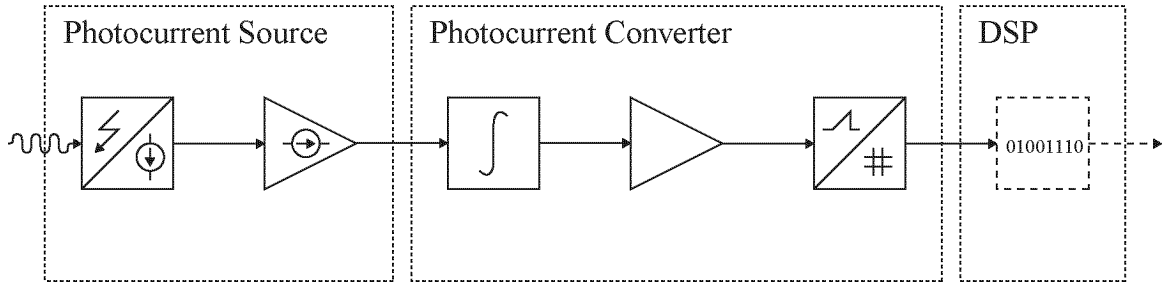


Fig. 7.1: Photocurrent measurement system.

A_3 and transistor T_6 build a feedback loop that keeps constant zero voltage across the photodiode D_1 and provides current source characteristics at the output. Hence the output current I_O is equal to the photocurrent independent of the output voltage V_O thus providing separation of the photodiode from the output. A simple variant of this circuit is achieved by removing the operational amplifier A_3 and by applying a constant voltage to the gate of transistor T_6, but this significantly affects the performance [112]. Various cascode circuits as discussed in Appendix D can be used for transistor T_6 in any case to achieve high precision even at low-voltage operation [113].

7.3 Current-Mode Transintegrator (CMTI)

The current-mode transintegrator as shown in Fig. 7.3 represents an integrator suitable for the photocurrent converter of current-mode architectures [114]. It is based on the basic memory cell of switched-current circuits [115][116]. The switched-current memory cell is properly a switched current copier cell for sampled-data circuits [117][118][119]. But here it is used in a continuous-time mode serving as a current-mode integrator with periodical reset. The current source I_R with the current mirror consisting of transistor T_3 and T_4 provides the bias current for transistor T_1. During reset the switch S_1 is closed while the switch S_2 is open and the bias current I_R slightly reduced by the low input current I_I is stored in transistor T_1. The resulting gate-source voltage of transistor T_1 is mainly determined by the bias current I_R and represents the integration voltage V_I at reset. After the reset phase the switch S_1 is opened and the switch S_2 is closed. Since immediately after switching the gate-source voltage of transistor T_1 or integration voltage V_I is unchanged, the drain current of transistor

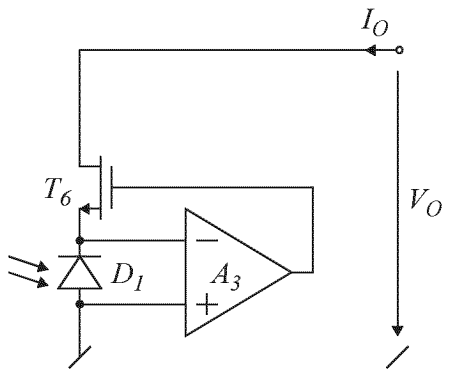


Fig. 7.2: Photodiode current source (PDCS).

T_1 is still about the bias current I_R and therefore the output current I_O is about zero. As the input current I_I is integrated on the integration capacitance C_1 the gate-source voltage of transistor T_1 or integration voltage V_I decreases and reduces the drain current of transistor T_1 according to the transistor transfer characteristic. For low integration voltage drops the transistor transfer characteristic can be linearized and the ratio of the current drop at the drain to the integration voltage drop is equal to the transistor transconductance. This reduced current at the drain causes an output current I_O equal to the current drop at the drain. Therefore the output current I_O is proportional to the integration voltage drop and represents the integral of the input current I_I thus yielding a current ramp at the output.

High precision requires very high output resistances of the output transistors which act as current sources. There are various cascode circuits as discussed in Appendix D that can be used for transistor T_1 and transistor T_4 to achieve very high output resistance for high precision even at low-voltage operation [113]. However the switched current copier configuration of transistor T_1 yields specific restrictions on the use of cascode circuits [120][121].

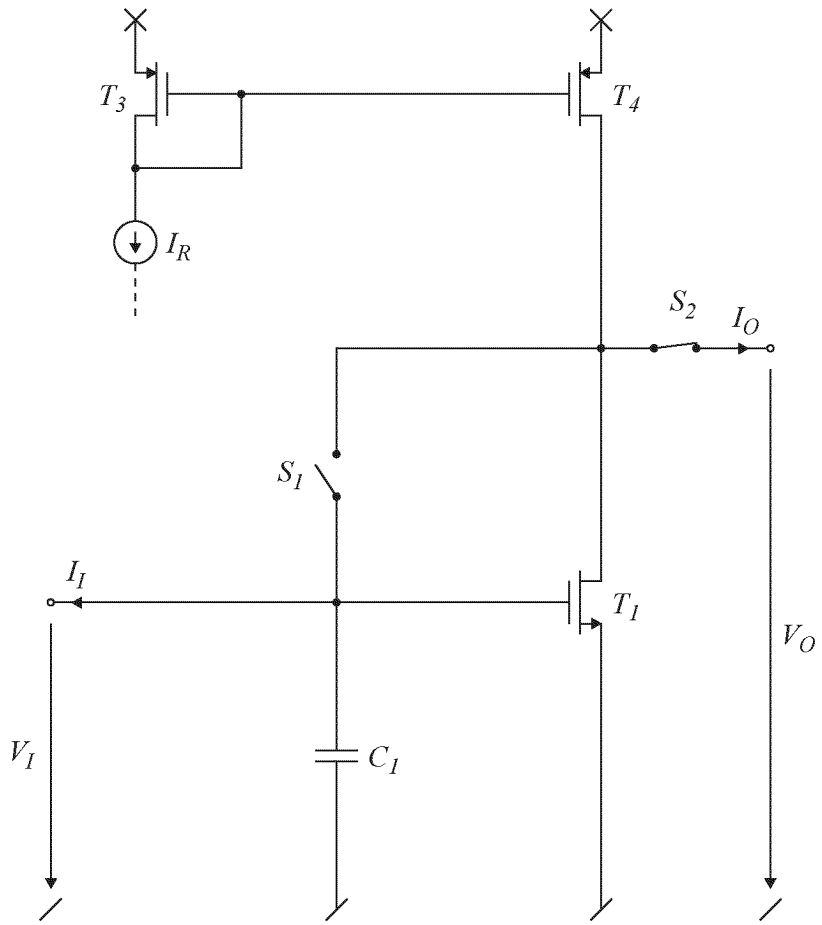


Fig. 7.3: Current-mode transintegrator (CMTI).

7.4 Photodiode with Current-Mode Transintegrator (PD+CMTI)

The photodiode with current-mode transintegrator is shown in Fig. 7.4. It is basically a photodiode operated in integration mode with a single transistor voltage-to-current amplifier stage. The current-mode transintegrator according to Fig. 7.3 is improved by cascode configurations for transistor T_1 and transistor T_4 using operational amplifier A_1 and transistor T_2 as well as operational amplifier A_2 and transistor T_5 respectively. During reset the switch S_1 is closed while the switch S_2 is open and the bias current I_R slightly reduced by the low photocurrent is stored in transistor T_1. Thus the photodiode D_1 together with the capacitance C_1 are charged to the integration voltage at reset which is the resulting gate-source voltage of transistor T_1 mainly determined by the bias current I_R. After the reset phase the switch S_1 is opened and the switch S_2 is closed. Since immediately after switching the gate-source voltage of transistor T_1 or integration voltage is unchanged, the drain current of transistor T_1 is still about the bias current I_R and therefore the output current I_O is about zero. Now the photocurrent and the photodiode leakage current are integrated on the integration capacitance consisting of the photodiode capacitance, the capacitance C_1 and the gate-source capacitance of the transistor T_1 thus yielding a voltage ramp. The transistor amplifier stage consisting of transistor T_1 with additional cascode circuitry and current source I_R with current mirror and additional cascode circuitry provides high impedance at the integration node and transfers the integration voltage to the integration current I_O thus yielding a high impedance current ramp suitable to a current ramp analog-to-digital converter. The integration current I_O can be converted to the amplified voltage V_O by connecting resistor R_1 between the output and the reference voltage V_{R2} thus yielding a voltage ramp suitable to a voltage ramp analog-to-digital converter.
This architecture provides different levels of precision corresponding to the complexity of the cascode configurations for the transistors. It is also suited for array implementation [122].
The chip layouts of the circuit realizations are shown in Appendix F. The parameters for the realized architectures according to the integrating sampled-data photosensing model of Chapter 3 are listed in Appendix G. The size of transistor T_1 is $W/L = 16\mu\text{m}/0.6\mu\text{m}$. It is designed to achieve high transconductance and low gate-source capacitance at the same time. The bias current I_R of $540\ \mu\text{A}$ yields a gate-source voltage of about 1.5 V and a transconductance of 1.3 mS. Operational amplifier A_1 and transistor T_2 regulate the drain of transistor T_1 to

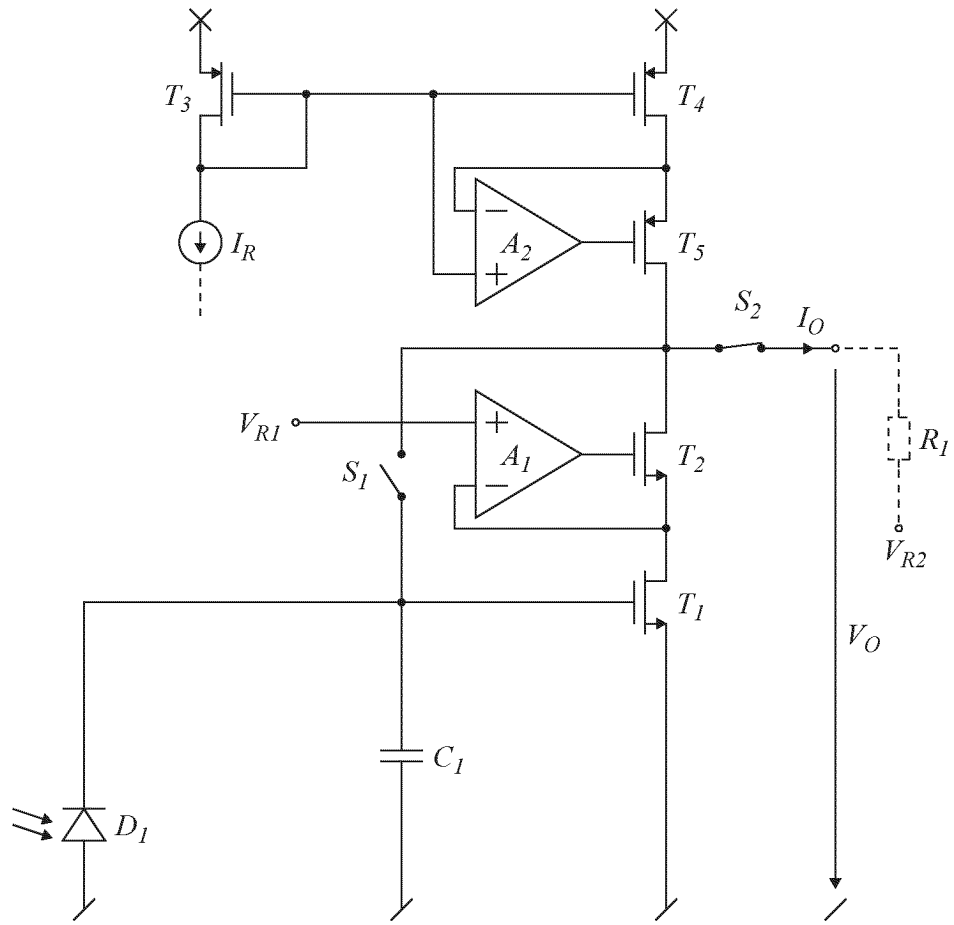


Fig. 7.4: Photodiode with current-mode transintegrator (PD+CMTI).

the reference voltage V_{R1} of 1 V. The size of transistor T_2 is $W/L = 8\mu$m/0.6μm to guarantee a drain current equal to the bias current I_R of 540 μA at reset with a source voltage of 1 V and a drain voltage of 1.5 V. The size of transistors T_3 and T_4 of the current mirror is $W/L = 32\mu$m/0.6μm to provide the bias current I_R of 540 μA at a low gate-source voltage of about -1.65 V. Operational amplifier A_2 and transistor T_5 regulate the drain of transistor T_4 to its gate voltage of about 3.35 V. The size of transistor T_5 is $W/L = 32\mu$m/0.6μm to achieve a low drain-source voltage at the drain current of 540 μA with a source voltage of 3.35 V and a gate voltage controlled by operational amplifier A_2. The achievable drain-source voltage is about -0.15 V. Therefore the complete bias current source works up to a voltage of about 3.2 V at the drain of transistor T_5. The switch S_2 is a CMOS switch with an n-channel transistor of $W/L = 8\mu$m/0.6μm and a p-channel transistor of $W/L = 24\mu$m/0.6μm with a very low resistance of about 400 Ω of the closed switch over the whole voltage range. The reference voltage V_{R2} is set to 1.5 V in order to be equal to the gate-source voltage of transistor T_1 at reset. The resistor R_1 is 10 kΩ. The usable range of the amplified voltage V_O is from the gate-source voltage of transistor T_1 at reset of 1.5 V to about 3.1 V, which is the maximum output voltage of the bias current source of about 3.2 V minus the voltage drop across the switch S_2. This voltage drop is about 65 mV for a full swing to the maximum output voltage of the bias current source with a resistor R_1 of 10 kΩ. Higher resistor values yield higher voltage amplifier gains but reduce the available bandwidth at the output. Lower resistor values increase the output current and limit the available output voltage range if the bias current I_R of 540 μA is reached. The transconductance of transistor T_1 of 1.3 mS and the resistor R_1 of 10 kΩ yield a voltage amplifier gain of 13. The used range of the amplified voltage V_O from 2 V to 3 V with an amount of 1 V for the amplified voltage drop yields an integration voltage ranging from about 1.4 V to 1.3 V with an amount of about 77 mV for the integration voltage drop. The switch S_1 is a CMOS switch with an n-channel transistor of $W/L = 0.8\mu$m/0.6μm and a p-channel transistor of $W/L = 2.4\mu$m/0.6μm. The switch is small to achieve low parasitic capacitance and low clock feedthrough to the high impedance integration node. The larger size of the p-channel transistor is due to the lower conductivity of these devices and to guarantee low resistance of about 4 kΩ of the closed switch over the whole voltage range. The integration capacitance of this architecture is equal to the photodetector capacitance. This is the capacitance of the integration node and includes the separate physical capacitance C_1 of 710 fF, the gate-source capacitance of transistor T_1 of about 30 fF and the photodiode capacitance, which depends on the integration voltage. Linearizing this function

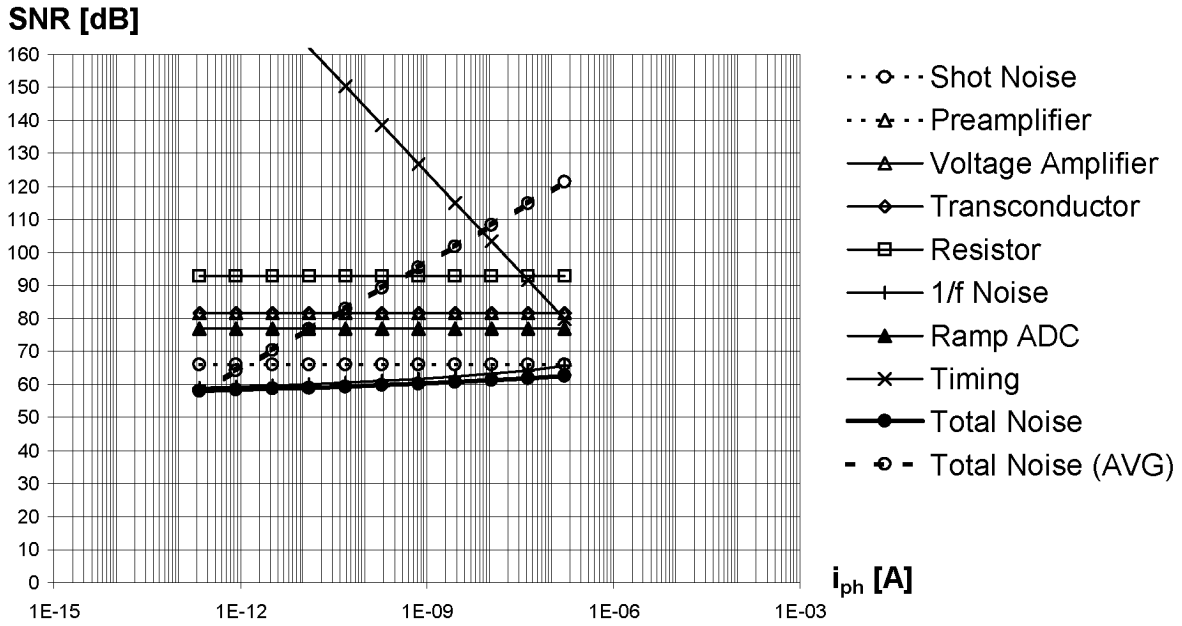


Fig. 7.5: Signal-to-noise ratio contributions of the different noise sources of the photodiode with current-mode transintegrator (PD+CMTI).

in the operating point yields a photodiode capacitance of about 7.8 pF and totals the integration capacitance and the photodetector capacitance to about 8.5 pF. D_1 is a p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode yielding a quantum efficiency of 70 % at a wavelength of 612 nm. The 1/f noise voltage coefficient of transistor T_1 is about $2.2 \cdot 10^{-10}$ V^2. Using the voltage amplifier gain of about 13, this corresponds to a 1/f noise voltage coefficient of about $370 \cdot 10^{-10}$ V^2 referred to the amplified voltage at the input of the ramp ADC. The analog bandwidth of this architecture is determined by the load resistor R_1 of 10 kΩ and by the load capacitance at this node that is connected to the ramp ADC. The load capacitance of slightly above 10 pF in the actual measurement setup yields an analog bandwidth of about 1 MHz.

Fig. 7.5 shows the signal-to-noise ratio contributions of the different noise sources of the realized photodiode with current-mode transintegrator versus the photocurrent analogous to Fig. 5.3. The dominant noise sources of this realization are shot noise with a corresponding SNR of 66 dB and particularly 1/f noise with an SNR of 59 dB to 66 dB depending on the photocurrent. The total SNR results to 58 dB to 63 dB depending on the photocurrent.

Fig. 7.6 shows the measured signal-to-noise ratio of the photodiode with current-

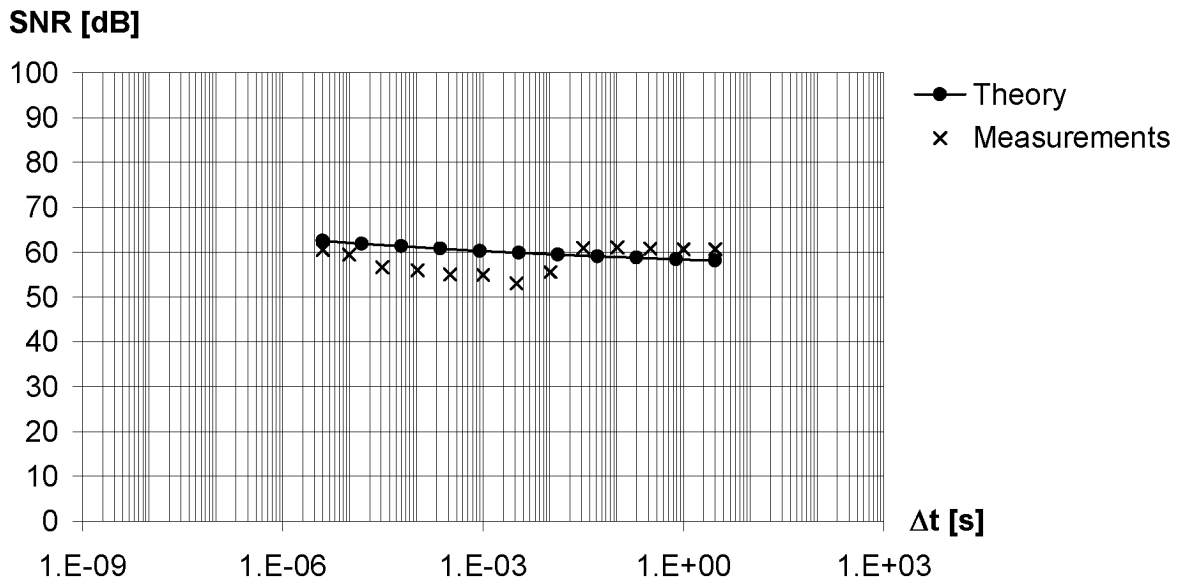


Fig. 7.6: Signal-to-noise ratio of the photodiode with current-mode transintegrator (PD+CMTI).

mode transintegrator without averaging versus the integration time Δt analogous to Fig. 5.4. The reduction in measured SNR at short integration times is due to line interferences as investigated in Section 3.7.

7.5 Photodiode Current Source with Current-Mode Transintegrator (PDCS+CMTI)

The photodiode current source with current-mode transintegrator is shown in Fig. 7.7. It is basically the same architecture with almost exactly the same operating principle as the photodiode with current-mode transintegrator according to Fig. 7.4 except that the photodiode D_1 is separated from the integration node [111][114]. Operational amplifier A_3 and transistor T_6 build a feedback loop that keeps constant zero voltage across the photodiode D_1 and provides current source characteristics at the output. Transistor T_6 is built as cascode circuit using transistor T_7 and reference voltage V_{R3}.
In contrast to all the other realized photosensing architectures the preamplifier bandwidth of the photodiode current source with current-mode transintegrator is not constant but depends on the signal current and therefore on the integra-

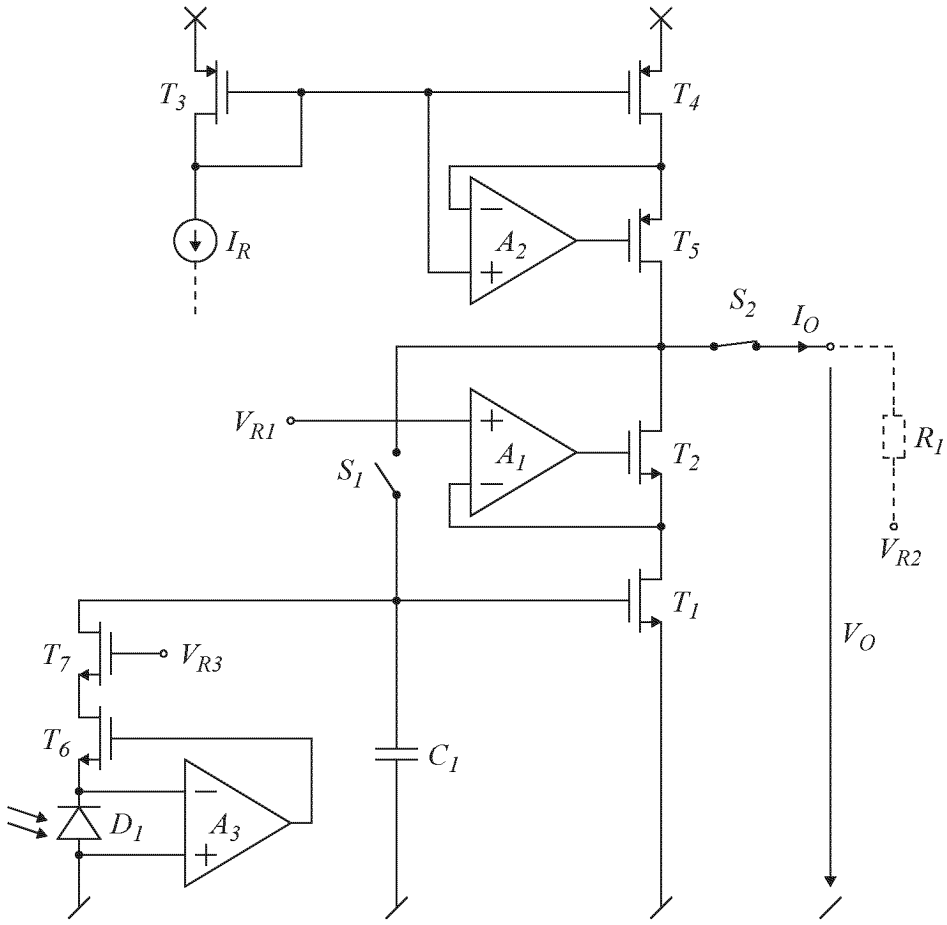


Fig. 7.7: Photodiode current source with current-mode transintegrator (PDCS+CMTI).

tion time Δt. The preamplifier bandwidth is the bandwidth of the photodiode current source in Fig. 7.7 and is a square root function of the unity gain bandwidth of the operational amplifier A_3, the transconductance of the transistor T_6 and the photodetector capacitance C_{ph}. Due to the low signal currents, transistor T_6 operates in weak inversion and therefore its transconductance is proportional to the signal current [123]. As a result the preamplifier bandwidth is proportional to the square root of the signal current. Fig. 7.8 shows the constant analog bandwidth referring to the photocurrent converter and the corresponding noise-effective bandwidth according to (3.56). It also shows the approximated signal dependent preamplifier bandwidth referring to the photocurrent source versus the integration time Δt. This illustrates that the preamplifier bandwidth decreases with the square root of the increasing integration time if no bias is applied. The preamplifier bandwidth can be separately adjusted by the bandwidth of the operational amplifier and by a bias current. Fig. 7.8 also shows the sampling-limited signal bandwidth according to (2.15). It illustrates that in the interesting range the adaptive low-pass filtering of the photodiode current source provides high enough bandwidth with respect to the sampling theorem but significantly reduces the bandwidth of the preamplifier for long integration times yielding improved noise performance.
The size of transistors T_6 and T_7 of this realization is $W/L = 1.6\mu\text{m}/1.2\mu\text{m}$. They are small to achieve small area and low parasitic capacitances. However, they are not designed with minimum size of $W/L = 0.8\mu\text{m}/0.6\mu\text{m}$ to reduce short channel effects such as channel length modulation. The reference voltage V_{R3} is 1.5 V to guarantee saturation operation of both transistors T_6 and T_7. In contrast to the photodiode with current-mode transintegrator, the integration capacitance of this architecture includes the separate physical capacitance C_1 of 710 fF, the gate-source capacitance of transistor T_1 of about 30 fF and the capacitance of the interconnect wires of about 140 fF. This totals to about 880 fF. The photodetector capacitance includes the photodiode capacitance of about 10.6 pF and the input capacitance of the operational amplifier of 800 fF and totals to about 11.4 pF. D_1 is a p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode yielding a quantum efficiency of 70 % at a wavelength of 612 nm. The voltage across the p-diffusion/n-well photodiode is zero. The operational amplifier A_3 generates preamplifier thermal noise. Its input voltage noise of about 25 nV/$\sqrt{\text{Hz}}$ is equivalent to the thermal noise of two transistors with a transconductance of 50 μS at the input of a noise-free operational amplifier. The 1/f noise voltage coefficient of the operational amplifier is about $2.2 \cdot 10^{-12}$ V^2. Using the small-signal gain of about 13 of the amplifier

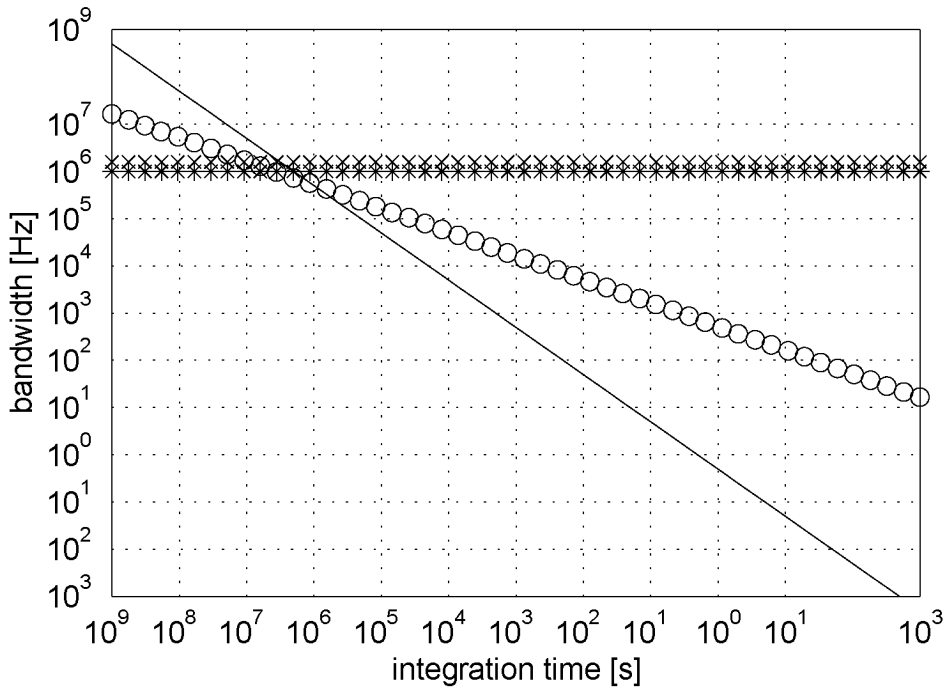


Fig. 7.8: Bandwidth of the photodiode current source with current-mode transintegrator (PDCS+CMTI) versus integration time Δt. (-) Sampling-limited signal bandwidth (for $\Delta t_{max} = \Delta t$). (o) Preamplifier bandwidth (photocurrent source bandwidth). (*) Analog bandwidth (photocurrent converter bandwidth). (x) Noise-effective bandwidth (according to the photocurrent converter bandwidth).

represented by operational amplifier A_1 and the photodetector capacitance and the integration capacitance, this corresponds to a 1/f noise voltage coefficient of about $3.7 \cdot 10^{-10}$ V^2 referred to the gate of transistor T_1. Together with the 1/f noise voltage coefficient of transistor T_1 of about $2.2 \cdot 10^{-10}$ V^2 and using the voltage amplifier gain of about 13, this corresponds to a 1/f noise voltage coefficient of about $1000 \cdot 10^{-10}$ V^2 referred to the amplified voltage at the input of the ramp ADC. The calculated preamplifier bandwidth of this realization with a unity gain bandwidth of operational amplifier A_3 of about 10 MHz and with transistor T_6 operating in weak inversion is shown in Fig. 7.8. The preamplifier bandwidth is plotted versus the integration time Δt.
The software tool "PhotoList" described in Appendix E has to be slightly modified to provide noise and performance analysis for this architecture. Fig. 7.9 shows the signal-to-noise ratio contributions of the different noise sources of the realized photodiode current source with current-mode transintegrator versus the photocurrent analogous to Fig. 5.3. The dominant noise sources of this realization are shot noise with a corresponding SNR of 56 dB and 1/f noise with an SNR of 55 dB to 61 dB depending on the photocurrent. The total SNR results to about 53 dB. At high photocurrents preamplifier thermal noise becomes dominant and the total SNR begins to decrease by 5 dB per decade with increasing photocurrent down to 49 dB. Compared to the photodiode with current-mode transintegrator the separation of the photodiode from the integration node results in a lower integration capacitance and therefore in lower photogenerated and collected charge. This yields higher shot noise with a lower corresponding SNR so that 1/f noise is not primarily dominant.
Fig. 7.10 shows the measured signal-to-noise ratio of the photodiode current source with current-mode transintegrator without averaging versus the integration time Δt analogous to Fig. 5.4. The reduction in measured SNR at short integration times is due to line interferences as investigated in Section 3.7.

7.6 Synopsis

Fig. 7.11 shows the dynamic range of the realized advanced architectures for large-area photosensing without bias current and without averaging versus the measurement time or maximum integration time Δt according to Fig. 5.28. The dynamic range of these architectures is basically limited by the resistor value and the corresponding load capacitance, as this determines the analog bandwidth. Dynamic range improvement requires either lower load capacitance such

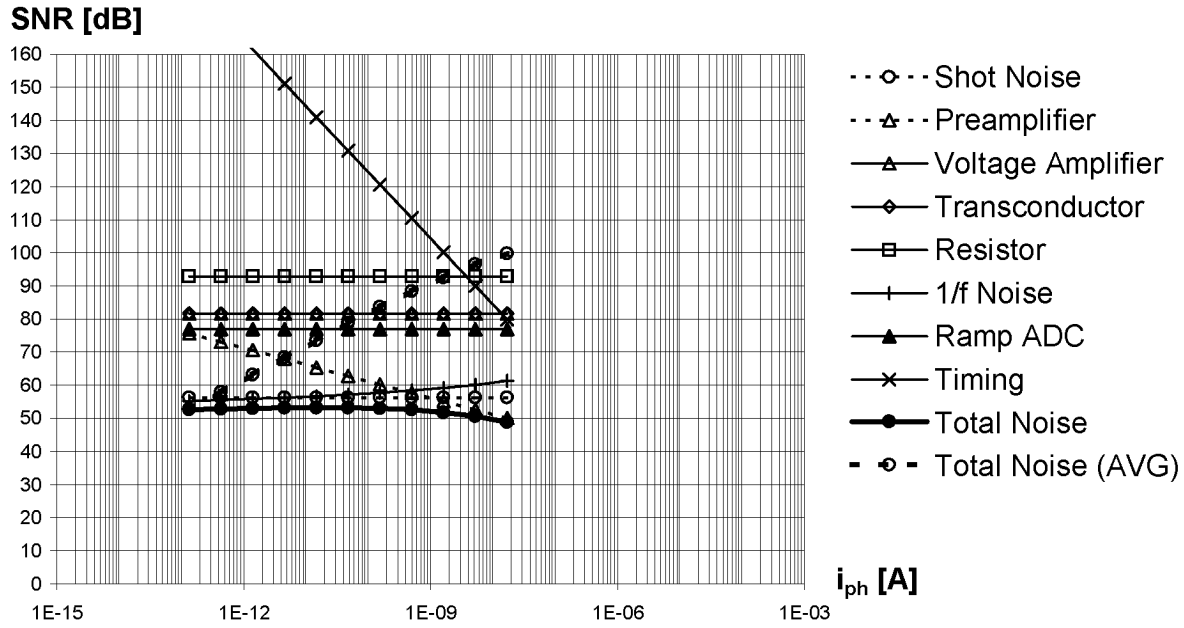


Fig. 7.9: Signal-to-noise ratio contributions of the different noise sources of the photodiode current source with current-mode transintegrator (PDCS+CMTI).

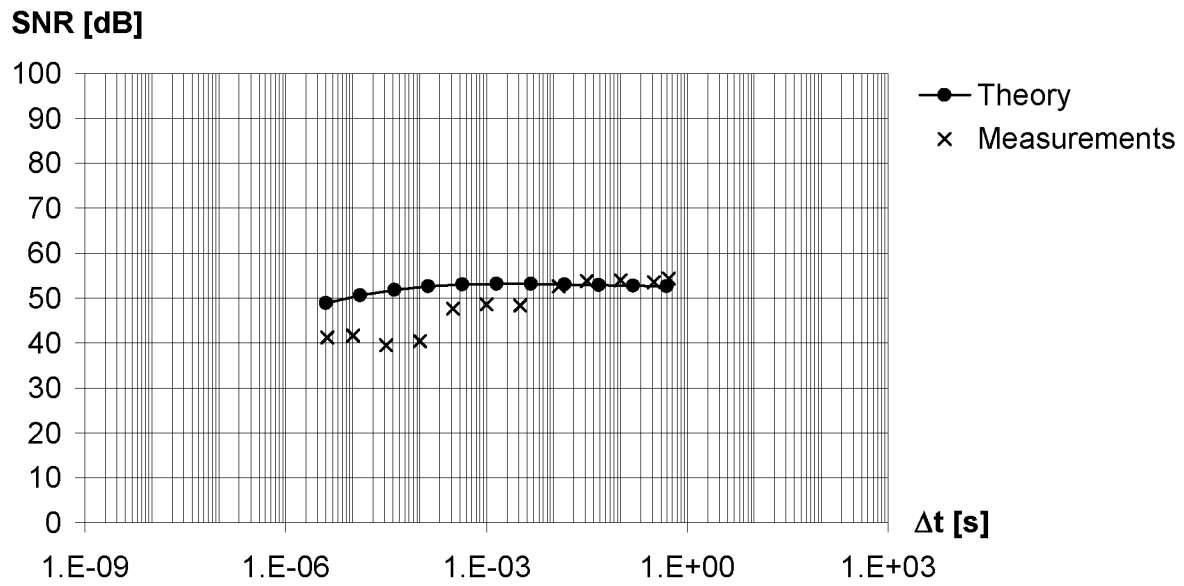


Fig. 7.10: Signal-to-noise ratio of the photodiode current source with current-mode transintegrator (PDCS+CMTI).

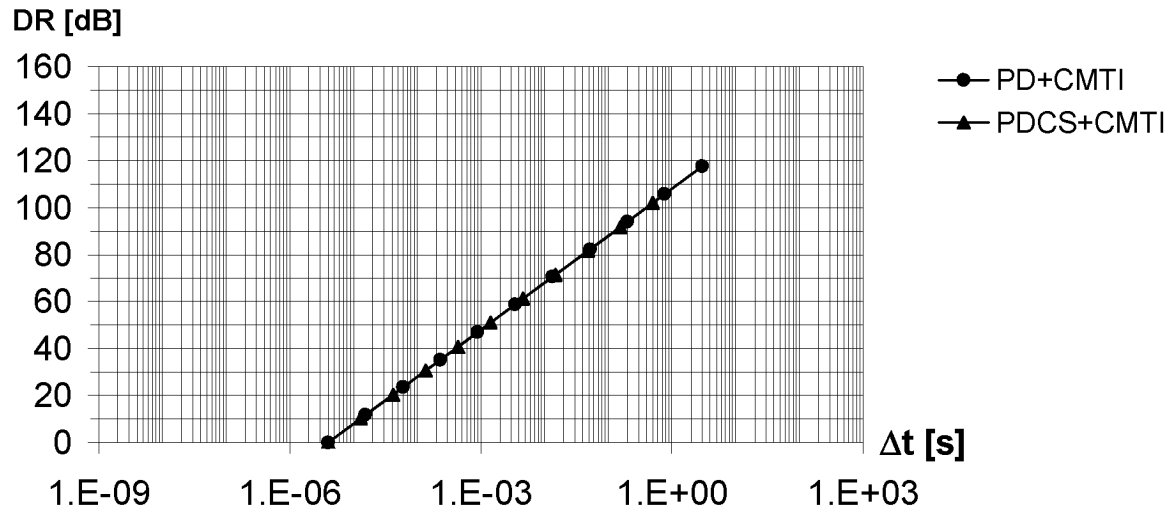


Fig. 7.11: Synopsis of the dynamic range of the realized advanced architectures for large-area photosensing.

as in completely integrated circuits or larger current-mode transintegrator with higher transconductor and lower resistor value.
These architectures generally achieve medium dynamic range, but the photodiode current source with current-mode transintegrator yields low dynamic range without measurement time limit due to the low virtual integration capacitance in combination with medium analog bandwidth.
Fig. 7.12 shows the resolution or signal-to-noise ratio of the realized advanced architectures for large-area photosensing without averaging versus the integration time Δt according to Fig. 5.29. Tab. 7.1 indicates the dominant noise sources and shows that the resolution of the realized advanced architectures for large-area photosensing is basically limited by shot noise and 1/f noise simultaneously, although for the photodiode with current-mode transintegrator 1/f noise is slightly more dominant.
The photodiode with current-mode transintegrator has a virtual integration capacitance of around 800 fF and yields a shot noise limited resolution of around 65 dB, while the photodiode current source with current-mode transintegrator has a virtual integration capacitance of around 80 fF and yields a resolution of around 55 dB.
The photodiode with current-mode transintegrator yields lower resolution than the photodiode with active integrator and decreasing resolution with increas-

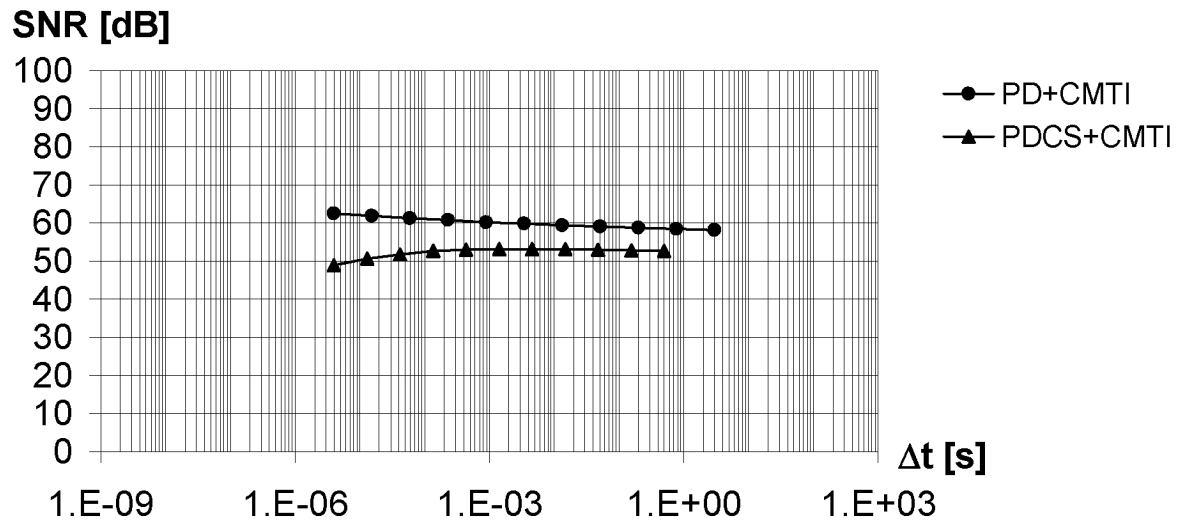


Fig. 7.12: Synopsis of the signal-to-noise ratio of the realized advanced architectures for large-area photosensing.

	Shot Noise	Preamplifier	1/f Noise	Ramp ADC	Timing
PD+CMTI	(•)		•		
PDCS+CMTI	•	(•)	•		

Tab. 7.1: Dominant noise sources of the realized advanced architectures for large-area photosensing.

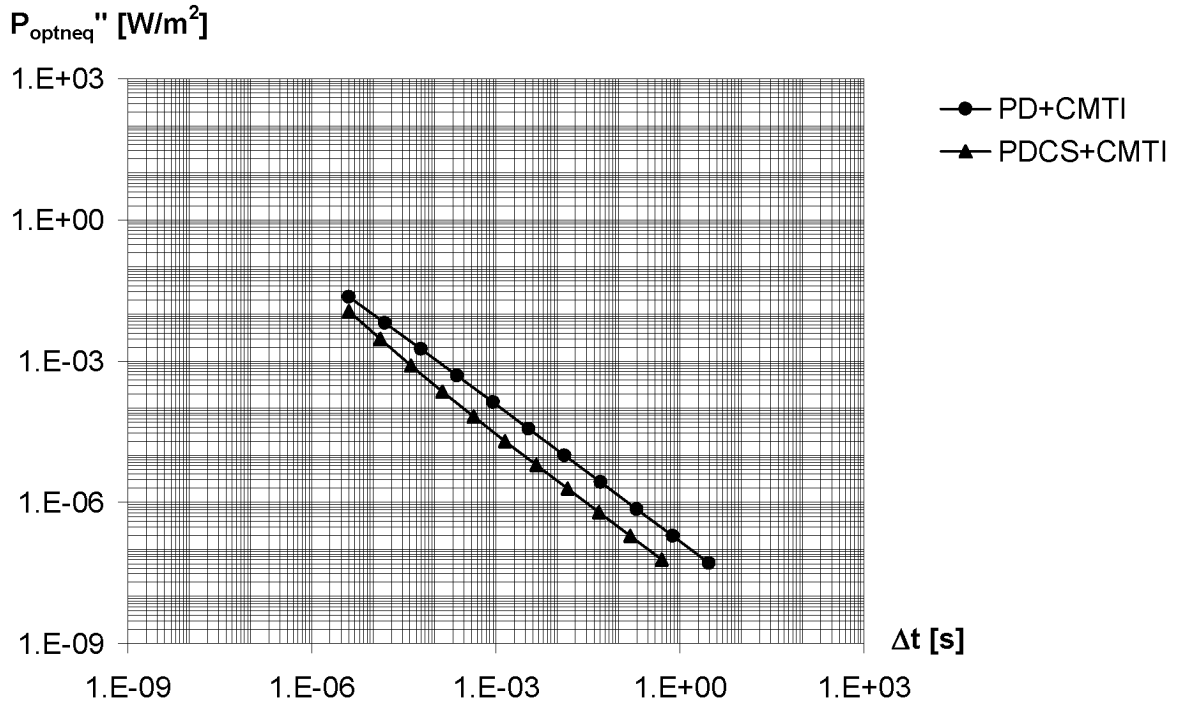


Fig. 7.13: Synopsis of the noise-equivalent optical power density of the realized advanced architectures for large-area photosensing. ($\lambda = 612$ nm.)

ing integration time both due to 1/f noise. The photodiode current source with current-mode transintegrator yields slightly decreasing resolution with decreasing integration time due to the preamplifier thermal noise with signal dependent preamplifier bandwidth.

Fig. 7.13 shows the sensitivity or noise-equivalent optical power density of the realized advanced architectures for large-area photosensing without bias current and without averaging versus the integration time Δt according to Fig. 5.30. The photodiode with current-mode transintegrator yields approximately the same sensitivity as the photodiode with active integrator as they have the same responsivity and approximately the same virtual integration capacitance. The photodiode current source with current-mode transintegrator achieves more than three times higher sensitivity than the photodiode with active integrator due to the very low virtual integration capacitance.

The maximum sensitivity without measurement time limit of the photodiode with active integrator in Fig. 5.30 is approximately equal to that of the photodiode current source with current-mode transintegrator after averaging for the

	Δt $@P''_{opt0}$ [ms]	DR [dB]	SNR $@P''_{opt0}$ [dB]	SNR_{avg} $@P''_{opt0}, \Delta t_A$ [dB]	P''_{optneq} $@\Delta t_0$ [μW/m^2]	A_{chip} [mm^2]	P_{DD} [mW]
PD+CMTI	1.25	118	60	99	120	0.088	6.5
PDCS+CMTI	0.129	102	53	101	28	0.116	8.5

Tab. 7.2: General performance of the realized advanced architectures for large-area photosensing. ($I_B = 0$, $P''_{opt0} = 0.1$ W/m^2, $\lambda = 612$ nm, $\Delta t_0 = 1$ ms, $\Delta t_A = 10$ s.)

	I_B [nA]	Δt_{min} [μs]	DR_b [dB]	SNR_{bavg} $@P''_{optb1}$ [dB]	SNR_{bavg} $@P''_{optbmax}$ [dB]	$P''_{optbneq}$ $@P''_{optbmin}$ [μW/m^2]
PD+CMTI	0.654	555	60	0	58	95
PDCS+CMTI	0.0677	114	72	12	62	26

Tab. 7.3: Performance of the realized advanced architectures for large-area photosensing in a typical application. ($P''_{optbmax} = 0.1$ W/m^2, $P''_{optb1} = 0.1$ mW/m^2, $\lambda = 612$ nm, $A = 1.5 \cdot 10^{-8}$ m^2, $\Delta t_{max} = 1$ ms, $t_{res} = 100$ ns.)

same measurement time.

Tab. 7.2 shows the general performance of the realized advanced architectures for large-area photosensing according to Tab. 5.2.

Tab. 7.3 shows the performance of the realized advanced architectures for large-area photosensing in a typical application with an optical power density ranging from $P''_{optb1} = 0.1$ mW/m^2 to $P''_{optbmax} = 0.1$ W/m^2 and with a measurement time of $\Delta t_{max} = 1$ ms at a timing resolution of $t_{res} = 100$ ns according to Tab. 5.3.

Tab. 7.4 shows the performance limits of the realized advanced architectures for large-area photosensing according to Tab. 5.4.

Tab. 7.5 shows the dominant noise sources of the realized advanced architectures for large-area photosensing with a large photodetector with a high photodetector capacitance of $C_{ph} = 600$ pF in contrast to Tab. 7.1. It confirms that

	I_B [pA]	Δt_{min} [μs]	DR_b [dB]	SNR_{avg} @$P''_{optmax}, \Delta t_A$ [dB]	$P''_{optbneq}$ @$P''_{optbmin}$ [nW/m^2]	$P''_{optbavgneq}$ @$P''_{optbmin}, \Delta t_A$ [nW/m^2]
PD+CMTI	0.22	4	175	127	52	29
PDCS+CMTI	0.14	4	154	113	63	14

Tab. 7.4: Performance limits of the realized advanced architectures for large-area photosensing. ($\lambda = 612$ nm, $\Delta t_A = 10$ s.)

	Shot Noise	**Preamplifier**	**1/f Noise**	**Ramp ADC**	**Timing**
PD+CMTI			•		
PDCS+CMTI		(•)	•		

Tab. 7.5: Dominant noise sources of the realized advanced architectures for large-area photosensing with a large photodetector ($C_{ph} = 600$ pF).

photodetector capacitance has a strong impact on noise performance and shows that noise sources other than shot noise become limiting at high photodetector capacitances.

7.7 Conclusions

A photocurrent measurement system basically consists of a photocurrent source, a photocurrent converter and a digital signal processor. It is suitable for current-mode implementation. Advanced architectures for large-area photosensing in standard CMOS technology are achieved using the photodiode or the photodiode current source in combination with the current-mode transintegrator.
Tab. 7.6 shows the typical properties of the advanced architectures for large-area photosensing with respect to performance according to Tab. 5.6. The resulting performance of the different advanced architectures for large-area photosensing is compared in Tab. 7.7 according to Tab. 5.7.
The proposed photodiode current source is well-suited for current-mode circuits and provides spatial separation of the charge generation and charge detection,

	R_λ	v_D	i_{n_p}	C_{int}	C_{virt}	v_{n_a}, i_{n_g}	a,g	**IRADC**
PD+CMTI	+	−−	++	−−	+	+	−	+
PDCS+CMTI	+	+	+	+	+	+	−	+

Tab. 7.6: Typical properties of the advanced architectures for large-area photosensing (High responsivity R_λ, zero voltage across the sensing diode v_D, low preamplifier thermal noise contribution i_{n_p}, independent integration capacitance C_{int}, variable virtual integration capacitance C_{virt}, low voltage amplifier thermal noise contribution v_{n_a} or transconductor thermal noise contribution i_{n_g}, stable voltage amplifier gain a or transconductor value g, compatibility with current ramp analog-to-digital converter IRADC.

	Speed	**Dynamic Range**	**Resolution**	**Sensitivity**	**Chip Area**	**Power Consumption**
PD+CMTI	+	−	+	−	+	−
PDCS+CMTI	++	++	+	++	−	−−

Tab. 7.7: Synopsis of the performance of the advanced architectures for large-area photosensing.

which yields high flexibility in choosing photodetector and integration capacitance independently. It can provide constant zero voltage across the sensing diode, which results in very low dark current and therefore high sensitivity. The photodiode current source provides adaptive low-pass filtering that depends on the signal level. This preamplifier bandwidth decreases by 10 dB per decade with increasing integration time if no bias current is applied. It can be separately adjusted by the bandwidth of the operational amplifier and by a bias current.
The proposed current-mode transintegrator provides adjustable voltage amplifier gain and achieves low virtual integration capacitance even for high integration capacitances resulting in high speed. It can achieve low preamplifier thermal noise, as a single transistor with high transconductance can be used as amplifier instead of an operational amplifier. However, the current-mode transintegrator does not achieve high stability of the transfer factor as the transconductor value is fabrication and temperature dependent.
The investigated cascode circuits provide various levels of precision and complexity for use in current-mode circuits. The proposed improved regulated cascode circuit is area-efficient and yields high precision even at low supply voltages. These cascode circuits can replace the operational amplifiers in the photodiode current source and the current-mode transintegrator to achieve small chip area, low power consumption and full current-mode compatibility.
Photodiodes as photodetectors in these architectures are superior to photogates as they achieve higher responsivity and as the current-mode transintegrator achieves low virtual integration capacitance even for high integration capacitances. However, an application limited by preamplifier thermal noise could require a photogate as photodetector in order to reduce the preamplifier thermal noise contribution.
The photodiode with current-mode transintegrator achieves the speed performance of the photodiode with active integrator and provides potential for high resolution and small chip area as it does not require operational amplifiers.
The photodiode current source with current-mode transintegrator is a simple architecture for advanced large-area photosensing. The actual realization is approximately one decade faster than the photogate with active integrator and achieves the highest dynamic range in a typical application due to its approximately one decade higher transfer factor resulting from the lower virtual integration capacitance. This higher speed by one decade results in an approximately 10 dB lower resolution as still shot noise is dominant and then speed performance exchanges with resolution. In a typical application the photodiode current source with current-mode transintegrator may achieve the highest resolu-

tion after averaging, as its high speed does not demand high bias currents, which introduce additional noise. This architecture achieves the highest sensitivity due to its highest transfer factor. The lowest noise-equivalent optical power density is approximately 10 nW/m^2 like that of the photodiode with active integrator. The required operational amplifier yields large chip area and together with the required bias current for the current-mode transintegrator high power consumption.

The photodiode current source with current-mode transintegrator is particularly suitable for large-area photosensing where preamplifier thermal noise is critical due to the high photodetector capacitance. The photodiode current source provides low-pass filtering of the preamplifier thermal noise while the current-mode transintegrator still achieves very high bandwidth, which yields a decoupling of the signal and preamplifier bandwidth from the analog bandwidth, the ramp-related bandwidth and the integration time. A preamplifier bandwidth much lower than the analog bandwidth of the current-mode transintegrator results in a significant reduction in preamplifier thermal noise and allows to reach the shot noise limit. The preamplifier bandwidth can be set to only the signal bandwidth while the analog bandwidth of the current-mode transintegrator is still four times the ramp-related bandwidth as required for proper ramp signals or even higher if shorter integration times are required. Thus low preamplifier bandwidth with high analog bandwidth is particularly suitable for serial measurement sequences in array architectures where the measurement times have to be very short although the signal bandwidth is quite low.

The photodiode with current-mode transintegrator and the photodiode current source with current-mode transintegrator may have problems in transfer factor stability since the transconductor values are fabrication and temperature dependent.

These architectures support both voltage and current ramp analog-to-digital converters.

8. CONCLUSIONS

The introduced generic model for integrating sampled-data photosensing provides noise modeling and performance analysis for any integrating sampled-data photosensing system.
The ramp analog-to-digital converter in the model determines the slope of the ramp signal which corresponds to the optical power density at the input of the system. The ramp signal is represented by either a voltage or a current and offers this technique to be implemented in the voltage-mode or in the current-mode. Determining the slope of the ramp signal is based on measuring two ramp samples on the same ramp yielding a certain signal drop and a certain integration time. Random signal access is a difficult technique and measuring the signal drop for a fixed integration time or measuring the integration time for a fixed signal drop are much simpler to implement. A bias current superimposed to the photocurrent provides finite integration times even for zero input signal but yields additional noise.
The analog bandwidth of the system has to be limited by a filter in order to achieve an optimum in noise reduction. The analog bandwidth has to be four times the ramp-related bandwidth to guarantee proper ramp signals and the ramp-related bandwidth has to be larger than two times the signal bandwidth in order to avoid aliasing according to the sampling theorem.
Measuring two ramp samples on the same ramp as explained above provides correlated double sampling and removes offsets and reduces reset noise as well as low-frequency noise. The effect of correlated double sampling on 1/f noise is implemented in the model by a simple approximation for first-order low-pass filtered 1/f noise after correlated double sampling.
For integration times much shorter than the measurement time, averaging can be applied to enhance the resolution.
Comparative analysis and experimental results are all based on voltage ramp analog-to-digital converters with fixed voltage drop providing correlated double sampling, optimum bandwidth limitation and ideal averaging. Noise on the

signal ramp is principally transferred into noise in the integration time measurement in the same way the signal itself is transferred.
The photodetector capacitance determines the preamplifier thermal noise and should be very low for high resolution.
The virtual integration capacitance determines the shot noise contribution and the transfer factor. High resolution without averaging requires high virtual integration capacitance to enhance the shot noise limit, whereas high speed as well as high sensitivity demand low virtual integration capacitance in order to achieve high transfer factor. Thus speed and sensitivity can basically be exchanged with resolution by adjusting the virtual integration capacitance. However, high speed and sensitivity as well as high resolution can be achieved by low virtual integration capacitance if averaging is used.
Photodiodes are simple photodetectors and offer different types to be implemented in CMOS technology. They achieve high responsivity and fast charge transport, but they have high photodetector capacitances particularly for large photodetector area.
The photogate is a basic photodetector in CMOS technology that yields low photodetector capacitance even for large photodetector area, but it has lower responsivity and the charge transport is slow because it is achieved only by diffusion across the whole photodetector area.
The basic photosensing architectures all yield a virtual integration capacitance approximately equal to the integration capacitance which is at least as high as the physical capacitance inserted for integration. In passive integrator architectures the integration capacitance is higher than the photodetector capacitance whereas active integrators provide separation of the photodetector capacitance and the integration capacitance and therefore achieve certain integration capacitance independent of the photodetector area.
Photodiode architectures generally achieve higher speed than photogate architectures due to the higher responsivity, but photogates can achieve significantly higher speeds than photodiodes in passive integrator architectures due to the low photodetector capacitance. In addition, photogate architectures can achieve higher resolution if preamplifier thermal noise is dominant.
Active integrator architectures generally achieve higher speed than passive integrator architectures due to the separation of photodetector capacitance and integration capacitance. But they generally yield lower resolution due to the high preamplifier and voltage amplifier thermal noise contributions of the operational amplifiers. Active integrators provide constant zero voltage across the sensing diode and thus can achieve higher sensitivity. Passive integrator architectures

yield smaller chip area and lower power consumption due to their simple transistor stages.
Array architectures do not improve performance of single detector architectures.
From the realized basic photosensing architectures the photodiode with active integrator generally achieves the highest speed due to the high transfer factor. For that reason it also yields the highest dynamic range in a typical application. However, the realized photogate with active integrator has potentially the highest dynamic range due to the high analog bandwidth and short minimum integration time.
The resolution of all the realized basic photosensing architectures is basically shot noise limited. The realized photodiode array with active integrator yields the highest resolution limit due to the high sum of virtual integration capacitances of all array elements.
The photodiode with active integrator achieves the highest sensitivity due to the high transfer factor.
The smallest chip area and the lowest power consumption are both achieved by the photodiode and photogate with passive integrator due to their simple structure.
All of the basic photosensing architectures provide high stability in transfer factor due to the feedback structure of the amplifiers. They are all based on voltage ramp analog-to-digital converters and therefore operate in the voltage-mode.
The measurement results are systematically degraded by line interferences, which has been verified in theory and experimentally.
The constant lateral field photogate is an advanced photodetector for large-area photosensing as it yields low photodetector capacitance and moderate speed in charge transport due to the applied drift field.
The proposed sweep photogate concept is very suitable for large-area photosensing due to the low photodetector capacitance and the very fast charge transport resulting from high local lateral drift fields.
The photodetector capacitance of these advanced photodetectors for large-area photosensing is equal to that of the standard photogate. But they achieve higher speed due to the improved charge transport.
The proposed photodiode current source is well-suited for current-mode circuits and provides separation of photodetector capacitance and integration capacitance for high speed as well as zero voltage across the sensing diode for high sensitivity. In addition the preamplifier noise is low-pass filtered resulting in improved resolution.
The introduced current-mode transintegrator is a current-mode circuit that pro-

vides low virtual integration capacitance and high transfer factor even for high integration capacitances due to the adjustable voltage amplifier gain, which yields high speed. It achieves low preamplifier thermal noise and therefore high resolution due to the low-noise amplifier stage.
Precision, chip area and power consumption of these circuits can be improved by cascodes such as the proposed improved regulated cascode circuit.
The photodiode with current-mode transintegrator is an advanced architecture for large-area photosensing that achieves the speed performance of the photodiode with active integrator and provides potential for high resolution and small chip area as it does not require operational amplifiers.
The photodiode current source with current-mode transintegrator is a simple architecture for large-area photosensing that achieves very high transfer factor resulting in very high speed, dynamic range and sensitivity. High speed yields low bias currents and therefore can result in higher resolution. Inherent low-pass filtering of the preamplifier thermal noise improves resolution as well and is very useful for array architectures.
These advanced architectures for large-area photosensing may have problems in transfer factor stability due to the non-feedback structure of the amplifier and therefore may need regular calibration. They are suitable for voltage-mode as well as current-mode circuits and can be used in combination with voltage as well as current ramp analog-to-digital converters.
Tab. 8.1 summarizes the typical performance of the different photosensing architectures.
The introduced integrating sampled-data photosensing model and the corresponding software tool "PhotoList" are very helpful in applying the above conclusions to the design and analysis of specific large-area photosensing applications, e.g. the ones mentioned in the introduction of this work.
In IR remote control applications the photodetector area is typically about 5 mm $\times$ 5 mm and the clock frequency of about 100 kHz yields measurement times of about 10 μs. In order to achieve highest sensitivity, the best architecture for this very large photosensing area at high speed is the photodiode with current-mode transintegrator using the current ramp ADC with fixed integration voltage drop. The best photodiode is the p-substrate/n-well diode yielding low photodiode capacitance of some nF and high responsivity at the typical wavelength of about 900 nm. Photogates with that large photosensing area would yield lower photodetector capacitance but would not achieve the required speed performance. The current-mode transintegrator achieves the highest sensitivity due to its low transconductor thermal noise and 1/f noise as well as its high

	Speed	Dynamic Range	Resolution	Sensitivity	Chip Area	Power Consumption
PD+PI	−−	−	+	−	++	++
PD+AI	+	+	−	+	−	−
PG+PI	−	−	+	−	++	++
PG+AI	−	−	−	−	−	−
SAPS	−−	−	+	−	−	+
PDA+AI	−	−	−	−	−	−
PAPS	−	−	+	−	−	+
PD+CMTI	+	−	+	−	+	−
PDCS+CMTI	++	++	+	++	−	−−

Tab. 8.1: Synopsis of the performance of the different photosensing architectures.

transfer coefficient. The transconductor thermal noise and the 1/f noise of the single transistor in the current-mode transintegrator can be optimized by its geometry and are lower than the preamplifier and voltage amplifier thermal noise and the 1/f noise contributions of an operational amplifier such as in the active integrator. Although the passive integrator can principally achieve the noise performance of the current-mode transintegrator, it does not achieve high transfer factor comparable to the transfer coefficient of the current-mode transintegrator. The current ramp ADC with fixed integration voltage drop suits well to the current-mode transintegrator, is very simple and does not require high timing resolution in this application where dynamic range and resolution can be low. If dynamic range or resolution is crucial, the current ramp ADC with fixed integration time or with random signal access can be used. The sensitivity of IR remote control applications is limited by transconductor thermal noise and 1/f noise and using the proposed architecture yields noise-equivalent optical power densities in the range of $100\ \mu\mathrm{W/m^2}$ with the actually realized transistors.
The best architecture for fiber optic transmission applications with a typical photosensing area of about $100\ \mu\mathrm{m} \times 100\ \mu\mathrm{m}$ operating at very high speed is the photodiode with current-mode transintegrator using the current ramp ADC with fixed integration time. The best photodiode is the p-substrate/n-well diode yielding low photodiode capacitance in the range of 1 pF and high responsivity at a wavelength of 500 nm. Photogates are too slow for these applications. And architectures including operational amplifiers are not practicable due to the very

high speed requirements. In the range of GSamples/s the ramp ADC thermal noise is dominant due to the input noise of about 10 mV of available voltage ADCs or about 1 μA of available current ADCs at such short measurement times. The current-mode transintegrator in combination with the current ADC yields an equivalent input voltage noise of about 1 mV and is superior to the architectures using the voltage ADC. The speed limit in fiber optic transmission applications in CMOS at optical power values of some μW using the proposed architecture corresponds to measurement times in the range of 1 ns.
In optical spectrometry applications photosensing areas are typically 30 μm $\times$ 500 μm with maximum optical power densities in the range of 100 mW/m^2 at measurement times of about 10 ms. The best architecture to achieve very high dynamic range is the photogate with active integrator using the sweep photogate concept and the voltage ramp ADC with random signal access. The sweep photogate yields very low photodetector capacitance of about 10 fF and can be easily operated down to integration times of about 100 μs. The low photodetector capacitance yields low noise-equivalent optical power densities for both thermal noise and 1/f noise of the operational amplifier. The dynamic range in the signal drop domain is limited by the 1/f noise of the operational amplifier in the active integrator and is in the range of 100 dB corresponding to about 16 bit. The voltage ramp ADC with random signal access using a 16 bit voltage ADC yields a dynamic range of about 100 dB in the signal drop domain and about 40 dB in the integration time domain according to minimum integration times of about 100 μs. Thus the proposed architecture for optical spectrometry applications yields a dynamic range of about 140 dB with maximum optical power densities of about 1 W/m^2 and noise-equivalent optical power densities in the range of 100 nW/m^2.

APPENDIX

A. PHYSICAL CONSTANTS

Planck constant	$h = 6.63 \cdot 10^{-34}$	Js
Speed of light	$c = 3.00 \cdot 10^{8}$	m/s
Elementary charge	$e = 1.60 \cdot 10^{-19}$	C
Boltzmann constant	$k = 1.38 \cdot 10^{-23}$	J/K
Permittivity of free space	$\epsilon_0 = 8.85 \cdot 10^{-12}$	F/m

B. SEMICONDUCTOR PROPERTIES

This appendix lists the basic properties of semiconductors. It includes the fundamental relations of the pn junction, the MOS structure in equilibrium and nonequilibrium as well as the MOS transistor. There is special emphasis on the surface potential of the MOS structure in nonequilibrium operating in inversion. The relation between the gate voltage, the surface potential and the inversion layer charge density and the corresponding surface potential approximation (B.72) are particularly useful in the discussion of charge transport in photogates. At the end of this appendix the most important parameters of the involved materials and the relevant simulation parameters of the used CMOS process are given.

B.1 Carrier Concentration

- Electron concentration n
- Hole concentration p
- Intrinsic carrier concentration $n_i = p_i$
- Carrier concentrations

$$np = n_i^2 = p_i^2 \tag{B.1}$$

- Electrostatic potential ϕ
- Electron concentrations at different points

$$\frac{n_1}{n_2} = e^{\frac{\phi_{12}}{\phi_t}} \tag{B.2}$$

Electrostatic potential difference between points 1 and 2 ϕ_{12}

$$\phi_{12} = \phi_1 - \phi_2 = -\phi_{21} \tag{B.3}$$

Thermal voltage ϕ_t

$$\phi_t = \frac{kT}{e} = 25.9 \text{ mV} \tag{B.4}$$

Boltzmann constant $k = 1.38 \cdot 10^{-23}$ J/K
Temperature $T = 300$ K
Elementary charge $e = 1.60 \cdot 10^{-19}$ C

B.1.1 n-Type Semiconductor

- Donor concentration N_D
- Majority carrier concentration in the absence of electric field n_0

$$n_0 \approx N_D \tag{B.5}$$

- Minority carrier concentration in the absence of electric field p_0

$$p_0 \approx \frac{n_i^2}{N_D} \tag{B.6}$$

B.1.2 p-Type Semiconductor

- Acceptor concentration N_A
- Minority carrier concentration in the absence of electric field n_0

$$n_0 \approx \frac{n_i^2}{N_A} \tag{B.7}$$

- Majority carrier concentration in the absence of electric field p_0

$$p_0 \approx N_A \tag{B.8}$$

B.2 Work Function

- The work function of material J W_J is the energy required to remove an electron from the material to the vacuum [123].

$$W_J = E_R - E_F \tag{B.9}$$

Vacuum energy level E_R
Fermi energy level E_F

B.3 Contact Potential

- The contact potential of material A to material B φ_{AB} is the electrostatic potential drop in going from A to B [123].

$$\varphi_{AB} = \varphi_A - \varphi_B = -\frac{W_A - W_B}{e} \tag{B.10}$$

Contact potential of material A to the intrinsic semiconductor φ_A
Contact potential of material B to the intrinsic semiconductor φ_B

- Contact potential of the extrinsic semiconductor J to the intrinsic semiconductor φ_J

$$\varphi_J = -\phi_F \tag{B.11}$$

- Fermi potential ϕ_F

$$\phi_F = -\frac{E_F - E_i}{e} = \phi_t \ln\left(\frac{n_i}{n_0}\right) = \phi_t \ln\left(\frac{p_0}{n_i}\right) \tag{B.12}$$

The intrinsic energy level E_i is the Fermi energy level of the intrinsic semiconductor.

- Electron concentration n

$$n = n_i e^{\frac{E_F - E_i}{kT}} = n_i e^{-\frac{\phi_F}{\phi_t}} \tag{B.13}$$

- Hole concentration n

$$p = n_i e^{\frac{E_i - E_F}{kT}} = n_i e^{\frac{\phi_F}{\phi_t}} \tag{B.14}$$

B.3.1 n-Type Semiconductor

- Fermi potential ϕ_F

$$\phi_F \approx -\phi_t \ln\left(\frac{N_D}{n_i}\right) \tag{B.15}$$

B.3.2 p-Type Semiconductor

- Fermi potential ϕ_F

$$\phi_F \approx +\phi_t \ln\left(\frac{N_A}{n_i}\right) \tag{B.16}$$

B.4 Electrostatics

- Charge density per unit volume Q'''
- Electric field $\underline{E}$

$$\underline{E} = \frac{1}{\epsilon} \int Q''' d\underline{x} \tag{B.17}$$

Permittivity ϵ

$$\epsilon = \epsilon_r \epsilon_0 \tag{B.18}$$

Relative permittivity ϵ_r
Permittivity of free space ϵ_0

$$\epsilon_0 = 8.85 \cdot 10^{-12} \text{ F/m} \tag{B.19}$$

- Electrostatic potential ϕ

$$\phi = -\int \underline{E} d\underline{x} \tag{B.20}$$

- Poisson equation

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{Q'''}{\epsilon} \tag{B.21}$$

B.5 Drift

- Drift velocity $\underline{v}_d$

$$\underline{v}_d = \pm \mu \underline{E} \tag{B.22}$$

Mobility μ
Saturation velocity v_s

- Current density $\underline{j}$

$$\underline{j} = Q''' \underline{v}_d = \pm \mu Q''' \underline{E} = \mu \left| Q''' \right| \underline{E} \tag{B.23}$$

B.6 Diffusion

- Current density $\underline{j}$

$$\underline{j} = -D \frac{\partial Q'''}{\partial \underline{x}} \tag{B.24}$$

Diffusion constant D

$$D = \mu \phi_t \tag{B.25}$$

- Diffusion length L

$$L = \sqrt{D\tau} \tag{B.26}$$

Carrier lifetime τ

B.7 pn Junction

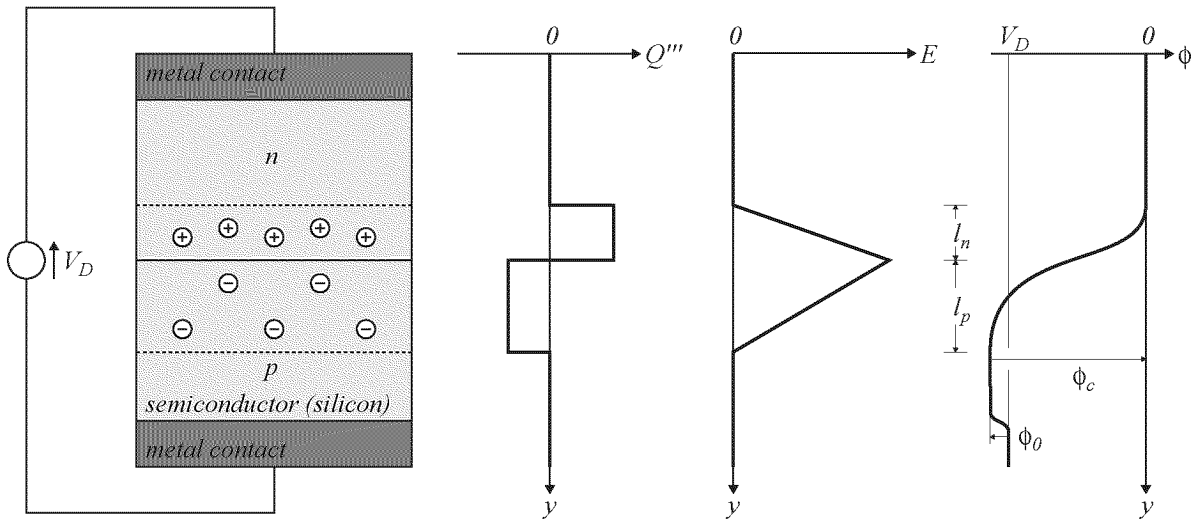


Fig. B.1: pn junction with external voltage source.

- Electrostatic potential across the depletion region ϕ_c

$$\phi_c = V_D - \phi_0 \tag{B.27}$$

External voltage across the pn junction V_D
Built-in potential ϕ_0

$$\phi_0 = \varphi_{np} = \phi_{Fp} - \phi_{Fn} \tag{B.28}$$

Fermi potential of the p-side ϕ_{Fp}
Fermi potential of the n-side ϕ_{Fn}

- Depletion region widths l_p, l_n

$$\frac{l_p}{l_n} = \frac{N_D}{N_A} \tag{B.29}$$

$$l_p + l_n = \sqrt{\frac{2\epsilon}{e}\frac{N_A + N_D}{N_A N_D}(\phi_0 - V_D)} \tag{B.30}$$

B.7.1 p^+n Junction

- Doping concentrations

$$N_A \gg N_D \tag{B.31}$$

- Depletion region widths l_p, l_n

$$l_p \ll l_n \tag{B.32}$$

$$l_n = \sqrt{\frac{2\epsilon}{eN_D}(\phi_0 - V_D)} \tag{B.33}$$

- Specific junction capacitance per unit area C_j''

$$C_j'' = \sqrt{\frac{\epsilon e N_D}{2(\phi_0 - V_D)}} \tag{B.34}$$

- Current I_D

$$I_D = I_R \left(e^{\frac{V_D}{\phi_t}} - 1 \right) \tag{B.35}$$

  Reverse current I_R

B.7.2 pn^+ Junction

- Doping concentrations

$$N_A \ll N_D \tag{B.36}$$

- Depletion region widths l_p, l_n

$$l_p \gg l_n \tag{B.37}$$

$$l_p = \sqrt{\frac{2\epsilon}{eN_A}(\phi_0 - V_D)} \tag{B.38}$$

- Specific junction capacitance per unit area C_j''

$$C_j'' = \sqrt{\frac{\epsilon e N_A}{2(\phi_0 - V_D)}} \tag{B.39}$$

- Current I_D according to (B.35)

B.8 MOS Structure in Equilibrium

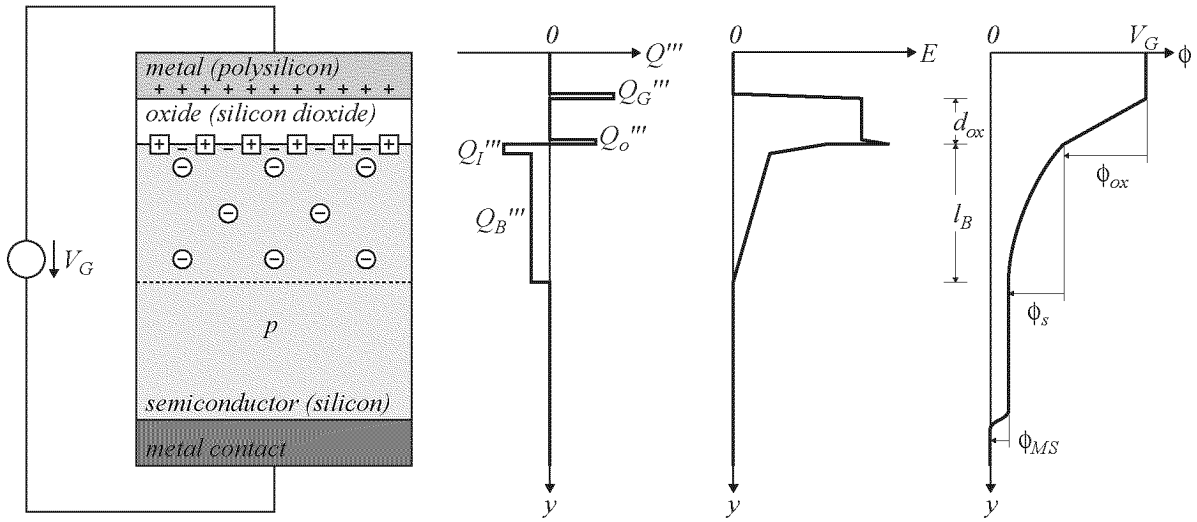


Fig. B.2: Two-terminal MOS structure in equilibrium (p-type substrate).

- Potential balance

$$V_G = \phi_{ox} + \phi_s + \phi_{MS} \tag{B.40}$$

Gate voltage V_G (referred to substrate contact)
Potential drop across the oxide ϕ_{ox}
Surface potential ϕ_s
Contact compensation potential ϕ_{MS}

$$\phi_{MS} = -\varphi_{GB} = -(\varphi_{gate} - \varphi_{bulk}) = \varphi_{bulk} - \varphi_{gate} \tag{B.41}$$

- Charge balance

$$Q''_G + Q''_o + Q''_I + Q''_B = 0 \tag{B.42}$$

Gate charge density per unit area Q''_G

$$Q''_G = C''_{ox}\phi_{ox} \tag{B.43}$$

Specific oxide capacitance per unit area C''_{ox}

$$C''_{ox} = \frac{\epsilon_{ox}}{d_{ox}} \tag{B.44}$$

Permittivity of the oxide ϵ_{ox}
Oxide thickness d_{ox}
Effective interface charge density per unit area Q''_o
Inversion layer charge density per unit area Q''_I
Depletion region charge density per unit area Q''_B
Semiconductor charge density per unit area $Q''_I + Q''_B$

$$Q''_I + Q''_B = \mp C''_{ox}\gamma\sqrt{\phi_t e^{-\frac{\phi_s}{\phi_t}} + \phi_s - \phi_t + e^{-\frac{2\phi_F}{\phi_t}}\left(\phi_t e^{\frac{\phi_s}{\phi_t}} - \phi_s - \phi_t\right)} \tag{B.45}$$

Body effect coefficient γ

$$\gamma = \frac{\sqrt{2e\epsilon_s N_A}}{C''_{ox}} \tag{B.46}$$

Permittivity of silicon ϵ_s

B.8.1 Flat-Band Condition

- Flat-band voltage V_{FB}

$$V_{FB} = \phi_{MS} - \frac{Q''_o}{C''_{ox}} \tag{B.47}$$

- Conditions

$$\boxed{\begin{aligned} V_G &= V_{FB} \\ Q_I'' + Q_B'' &= 0 \\ \phi_s &= 0 \end{aligned}} \tag{B.48}$$

B.8.2 Accumulation

- Conditions

$$\boxed{\begin{aligned} V_G &< V_{FB} \\ Q_I'' + Q_B'' &> 0 \\ \phi_s &< 0 \end{aligned}} \tag{B.49}$$

B.8.3 Depletion

- Conditions

$$\boxed{\begin{aligned} V_G &> V_{FB} \\ Q_I'' + Q_B'' &< 0 \\ 0 < \phi_s &< \phi_F \end{aligned}} \tag{B.50}$$

B.8.4 Inversion

- Conditions

$$\boxed{\begin{aligned} V_G &> V_{FB} \\ Q_I'' + Q_B'' &< 0 \\ \phi_s &> \phi_F \end{aligned}} \tag{B.51}$$

- Semiconductor charge density $Q''_I + Q''_B$

$$Q''_I + Q''_B \approx -C''_{ox}\gamma\sqrt{\phi_s + \phi_t e^{\frac{\phi_s - 2\phi_F}{\phi_t}}} \tag{B.52}$$

Depletion region charge density Q''_B

$$Q''_B = -C''_{ox}\gamma\sqrt{\phi_s} \tag{B.53}$$

- Potential relation

$$V_G = V_{FB} + \phi_s + \gamma\sqrt{\phi_s} - \frac{Q''_I}{C''_{ox}} \tag{B.54}$$

- Depletion region width l_B

$$l_B = \sqrt{\frac{2\epsilon_s}{eN_A}\phi_s} \tag{B.55}$$

- Surface electron concentration $n_{surface}$

$$n_{surface} \approx N_A e^{\frac{\phi_s - 2\phi_F}{\phi_t}} \tag{B.56}$$

Weak Inversion

- Surface potential condition

$$\boxed{\phi_F \leq \phi_s \leq 2\phi_F} \tag{B.57}$$

Moderate Inversion

- Surface potential condition

$$\boxed{2\phi_F \leq \phi_s \leq 2\phi_F + x\phi_t \qquad , x > 0} \tag{B.58}$$

Strong Inversion

- Surface potential condition

$$\boxed{\phi_s \geq 2\phi_F + x\phi_t \qquad , x > 0} \tag{B.59}$$

- Surface potential approximation

$$\phi_s \approx \phi_B \tag{B.60}$$

Strong inversion surface potential shift ϕ_B

$$\phi_B = 2\phi_F + 6\phi_t \tag{B.61}$$

- Inversion layer charge density Q''_I

$$Q''_I \approx -C''_{ox}(V_G - V_{T0}) \tag{B.62}$$

Extrapolated threshold voltage V_{T0}

$$V_{T0} = V_{FB} + \phi_B + \gamma\sqrt{\phi_B} \tag{B.63}$$

B.9 MOS Structure in Nonequilibrium

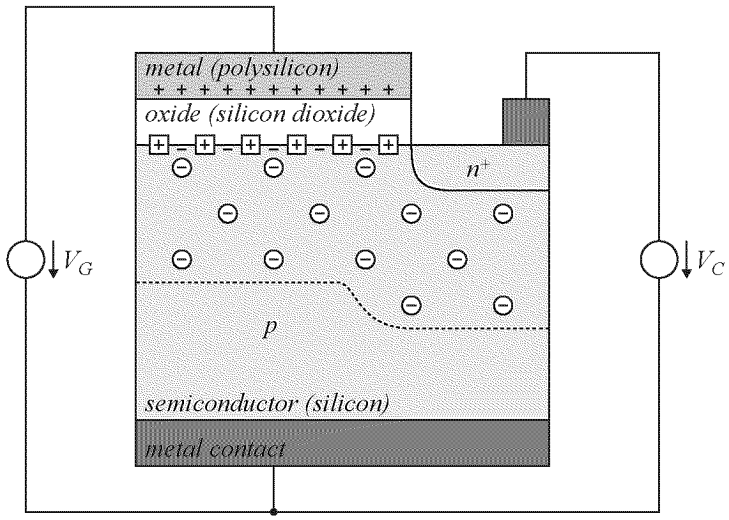


Fig. B.3: Three-terminal MOS structure in nonequilibrium (p-type substrate).

- Potential balance

$$V_G = \phi_{ox} + \phi_s + \phi_{MS} \tag{B.64}$$

- Charge balance

$$Q''_G + Q''_o + Q''_I + Q''_B = 0 \tag{B.65}$$

Gate charge density per unit area Q''_G

$$Q''_G = C''_{ox}\phi_{ox} \tag{B.66}$$

B.9.1 Inversion

- Conditions

$$\boxed{\begin{aligned} V_G &> V_{FB} \\ Q''_I + Q''_B &< 0 \\ \phi_s &> \phi_F + V_C \end{aligned}} \tag{B.67}$$

Diffusion voltage V_C (referred to substrate B)

- Semiconductor charge density $Q''_I + Q''_B$

$$Q''_I + Q''_B \approx -C''_{ox}\gamma\sqrt{\phi_s + \phi_t e^{\frac{\phi_s - (2\phi_F + V_C)}{\phi_t}}} \tag{B.68}$$

Depletion region charge density Q''_B

$$Q''_B = -C''_{ox}\gamma\sqrt{\phi_s} \tag{B.69}$$

- Potential relation

$$V_G = V_{FB} + \phi_s + \gamma\sqrt{\phi_s} - \frac{Q''_I}{C''_{ox}} \tag{B.70}$$

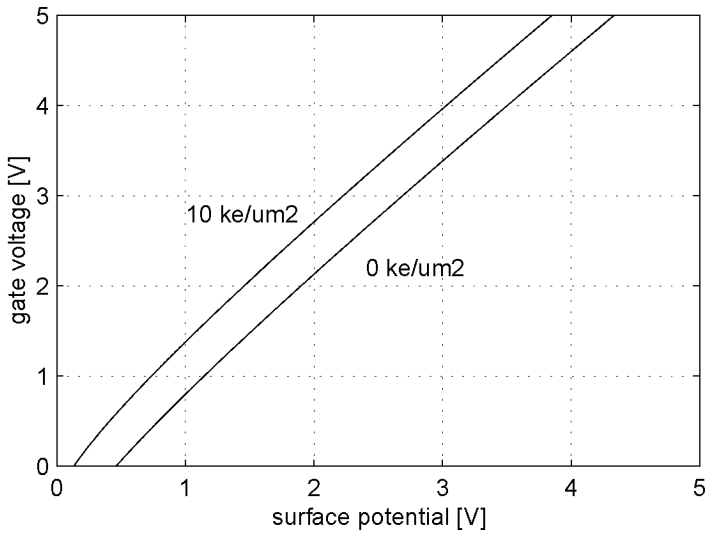


Fig. B.4: Gate voltage V_G according to (B.70) versus surface potential ϕ_s at different inversion layer charge densities Q''_I for the AMS 0.6μm CMOS process CUX.

- Surface potential

$$\phi_s = V_G - V_{FB} + \frac{Q''_I}{C''_{ox}} + \frac{\gamma^2}{2} - \sqrt{\left(\frac{\gamma^2}{2}\right)^2 + \gamma^2\left(V_G - V_{FB} + \frac{Q''_I}{C''_{ox}}\right)} \tag{B.71}$$

From (B.70)

$$\phi_s \approx \phi_{s0} + \gamma_s\left(V_G - V_{FB} + \frac{Q''_I}{C''_{ox}}\right) \tag{B.72}$$

Surface potential fitting parameter ϕ_{s0}
Surface potential approximation coefficient γ_s

$$\gamma_s = \frac{1}{1 + \frac{\gamma}{2\sqrt{\phi_s}}} \tag{B.73}$$

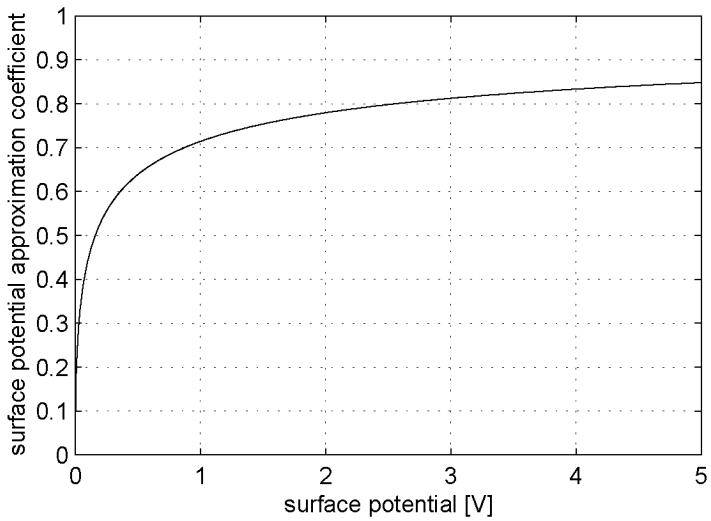


Fig. B.5: Surface potential approximation coefficient γ_s according to (B.73) versus surface potential ϕ_s for the AMS 0.6μm CMOS process CUX.

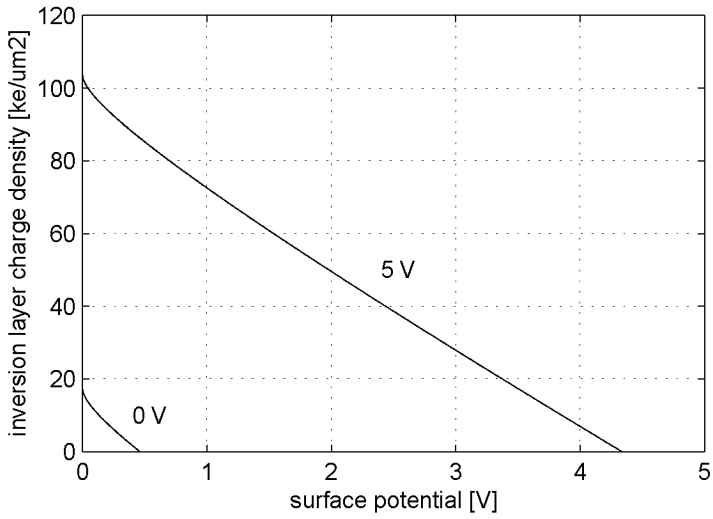


Fig. B.6: Inversion layer charge density Q_I'' according to (B.70) or (B.71) versus surface potential ϕ_s at different gate voltages V_G for the AMS 0.6μm CMOS process CUX.

- Depletion region width l_B

$$l_B = \sqrt{\frac{2\epsilon_s}{eN_A}\phi_s} \tag{B.74}$$

- Surface electron concentration $n_{surface}$

$$n_{surface} \approx N_A e^{\frac{\phi_s - (2\phi_F + V_C)}{\phi_t}} \tag{B.75}$$

Weak Inversion

- Surface potential condition

$$\boxed{\phi_F + V_C \leq \phi_s \leq 2\phi_F + V_C} \tag{B.76}$$

Moderate Inversion

- Surface potential condition

$$\boxed{2\phi_F + V_C \leq \phi_s \leq 2\phi_F + x\phi_t + V_C \qquad , x > 0} \tag{B.77}$$

Strong Inversion

- Surface potential condition

$$\boxed{\phi_s \geq 2\phi_F + x\phi_t + V_C \qquad , x > 0} \tag{B.78}$$

- Surface potential approximation

$$\phi_s \approx \phi_B + V_C \tag{B.79}$$

- Inversion layer charge density Q_I''

$$Q_I'' \approx -C_{ox}''[V_G - V_{GT}(V_C)] \tag{B.80}$$

Extrapolated gate-substrate threshold voltage $V_{GT}(V_C)$

$$V_{GT}(V_C) = V_{FB} + \phi_B + V_C + \gamma\sqrt{\phi_B + V_C} = V_T + V_C \tag{B.81}$$

Extrapolated gate-surface threshold voltage V_T

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi_B + V_C} - \sqrt{\phi_B}\right) \tag{B.82}$$

B.10 MOS Transistor

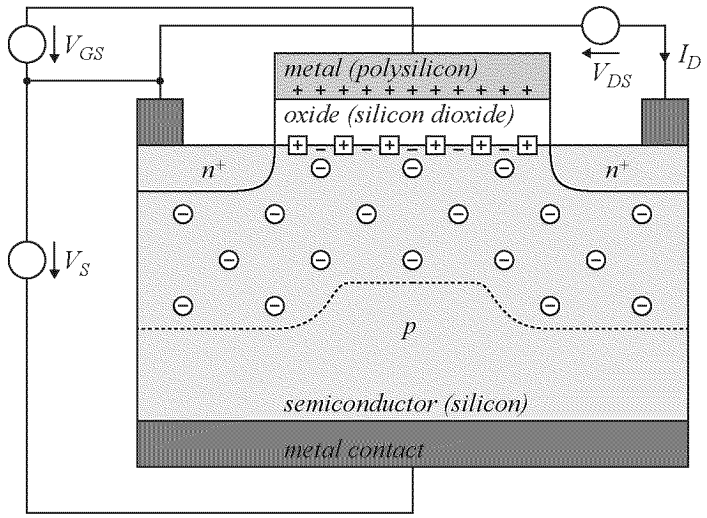


Fig. B.7: Four-terminal MOS transistor (n-channel).

- Drain current I_D
  Gate-source voltage V_{GS}
  Drain-source voltage V_{DS}
  Source voltage V_S (referred to substrate contact)

- Small-signal transconductance g_m

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{B.83}$$

- Small-signal output conductance g_o

$$g_o = \frac{\partial I_D}{\partial V_{DS}} \tag{B.84}$$

B.10.1 Weak Inversion (Approximate Model)

- Condition

The most heavily inverted channel end (usually the source channel end) is in weak inversion:

$$V_L \leq V_{GS} \leq V_M \tag{B.85}$$

Weak inversion limit voltage V_L

$$V_L = V_{FB} + \phi_F + \gamma\sqrt{\phi_F + V_S} \tag{B.86}$$

Moderate inversion limit voltage V_M

$$V_M = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F + V_S} \tag{B.87}$$

- Drain current I_D

$$I_D = \frac{W}{L} I_M e^{\frac{(V_{GS}-V_M)}{n_M \phi_t}} (1 - e^{-\frac{V_{DS}}{\phi_t}}) \tag{B.88}$$

Weak inversion gain current I_M

$$I_M = \mu C''_{ox} \phi_t^2 \frac{\gamma}{2\sqrt{2\phi_F + V_S}} \tag{B.89}$$

Weak inversion voltage fitting coefficient n_M

$$n_M \approx 1 + \frac{\gamma}{2\sqrt{2\phi_F + V_S}} \tag{B.90}$$

- Small-signal transconductance g_m

$$g_m = \frac{I_D}{n_M \phi_t} \tag{B.91}$$

B.10.2 Moderate Inversion

- Condition

> The most heavily inverted channel end (usually the source channel end) is in moderate inversion:
>
> $$V_M < V_{GS} < V_H$$ (B.92)

Strong inversion limit voltage V_H

$$V_H = V_M + V_Z \approx V_T + 6n\phi_t \tag{B.93}$$

Moderate inversion range voltage V_Z

$$V_Z \approx 0.5 \text{ V} \tag{B.94}$$

B.10.3 Strong Inversion (Approximate Model)

- Condition

> The most heavily inverted channel end (usually the source channel end) is in strong inversion:
>
> $$V_{GS} \geq V_H$$ (B.95)

- Threshold voltage (extrapolated gate-source threshold voltage) V_T

$$V_T = V_{T0} + \gamma \left(\sqrt{\phi_B + V_S} - \sqrt{\phi_B} \right) \tag{B.96}$$

Extrapolated threshold voltage V_{T0}

$$V_{T0} = V_{FB} + \phi_B + \gamma \sqrt{\phi_B} \tag{B.97}$$

Strong inversion surface potential shift ϕ_B

$$\phi_B = 2\phi_F + 6\phi_t \tag{B.98}$$

- Pinchoff voltage V_P

$$V_P = \frac{V_{GS} - V_T}{n} \tag{B.99}$$

Strong inversion voltage fitting coefficient n

$$n \approx 1 + \frac{\gamma}{2\sqrt{\phi_B + V_S}} \tag{B.100}$$

- Gain factor β

$$\beta = \frac{W}{L}\beta_0 \tag{B.101}$$

Normalized gain factor β_0

$$\beta_0 = \mu C''_{ox} \tag{B.102}$$

Nonsaturation (Ohmic / Linear / Triode Region)

- Condition

$$\boxed{V_{DS} \leq V_P} \tag{B.103}$$

- Drain current I_D

$$I_D = \beta \left[(V_{GS} - V_T)V_{DS} - \frac{1}{2} n V_{DS}^2 \right] \tag{B.104}$$

- Small-signal transconductance g_m

$$g_m = \beta V_{DS} \tag{B.105}$$

Saturation (Pinchoff Region)

- Condition

$$\boxed{V_{DS} > V_P} \tag{B.106}$$

- Pinchoff voltage V_P

$$V_P = \sqrt{\frac{2I_D}{\beta n}} \tag{B.107}$$

- Drain current I_D

$$I_D = \frac{\beta}{2n}(V_{GS} - V_T)^2 \tag{B.108}$$

- Small-signal transconductance g_m

$$g_m = \frac{\beta}{n}(V_{GS} - V_T) = \sqrt{\frac{2\beta I_D}{n}} = \frac{2I_D}{V_{GS} - V_T} \tag{B.109}$$

B.11 Parameters of Materials

		Silicon Si
Intrinsic carrier concentration	n_i	$1.45 \cdot 10^{10}$ cm^{-3}
Relative permittivity	ϵ_r	11.9
Electron mobility	μ_n	1500 cm^2/Vs
Hole mobility	μ_p	450 cm^2/Vs
Carrier saturation velocity	v_s	10^7 cm/s
Electron diffusion constant	D_n	35 cm^2/s
Hole diffusion constant	D_p	12.5 cm^2/s
Minority carrier lifetime	τ	$2.5 \cdot 10^{-3}$ s

		Silicon Dioxide SiO_2
Relative permittivity	ϵ_r	3.9

		Aluminum Al
Contact potential to intrinsic silicon	φ_J	0.6 V

B.12 Simulation Parameters for the AMS 0.6μm CMOS Process CUX

Gate doping	N_D	$1 \cdot 10^{20}$ cm^{-3}
Oxide thickness	d_{ox}	12.5 nm
Effective interface charge density	Q''_o	0 C/cm^2
Effective substrate doping	N_A	$1.45 \cdot 10^{17}$ cm^{-3}

C. SPECTRAL ANALYSIS

In this appendix the fundamental terms, definitions and relations of signal representations in the time and the frequency domain are given. The properties of white noise and 1/f noise are presented and the effects of basic signal processing techniques such as low-pass filtering, correlated double sampling as well as sampling and holding are investigated. There is special emphasis on correlated double sampling of 1/f noise. The expression for the total power of first-order low-pass filtered 1/f noise after correlated double sampling and the corresponding approximation (C.92) are used in the integrating sampled-data photosensing model for 1/f noise implementation.

C.1 Terms

C.1.1 Time Domain

- Signal $x(t)$
- Mean value $\overline{x}$

$$\overline{x} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t) dt \tag{C.1}$$

- Integrated square value x_{sum}^2 (signal energy)

$$x_{sum}^2 = \int_{-\infty}^{+\infty} [x(t)]^2 \, dt \tag{C.2}$$

- Mean square value x_{eff}^2 (signal power)

$$x_{eff}^2 = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} [x(t)]^2 \, dt \tag{C.3}$$

- Root mean square (rms) value x_{eff} (effective value)

$$x_{eff} = \sqrt{\lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} [x(t)]^2 \, dt} \tag{C.4}$$

- Autocorrelation function $R(\tau)$

$$R(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t)x(t+\tau)dt \tag{C.5}$$

- Autocorrelation integral function $\rho(\tau)$

$$\rho(\tau) = \int_{-\infty}^{+\infty} x(t)x(t+\tau)dt \tag{C.6}$$

C.1.2 Frequency Domain

- Spectral density $\underline{X}(\omega)$ (double-sided)

$$\underline{X}(\omega) = \int_{-\infty}^{+\infty} x(t)e^{-j\omega t}dt \tag{C.7}$$

- Energy spectral density $E(\omega)$ (double-sided)

$$E(\omega) = |\underline{X}(\omega)|^2 \tag{C.8}$$

- Power spectral density $S(\omega)$ (double-sided)

$$S(\omega) = \lim_{T\to\infty} \frac{1}{T} |\underline{X}(\omega)|^2 \tag{C.9}$$

  Power spectral density $2S(\omega)$ (single-sided)

$$2S(\omega) = 2 \lim_{T\to\infty} \frac{1}{T} |\underline{X}(\omega)|^2 \tag{C.10}$$

Root power spectral density $\sqrt{2S(\omega)}$ (single-sided)

$$\sqrt{2S(\omega)} = \sqrt{2 \lim_{T\to\infty} \frac{1}{T} |\underline{X}(\omega)|^2} \tag{C.11}$$

C.1.3 Relations

- Fourier transform

$$\underline{X}(\omega) = \int_{-\infty}^{+\infty} x(t) e^{-j\omega t} dt \tag{C.12}$$

Inverse Fourier transform

$$x(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \underline{X}(\omega) e^{j\omega t} d\omega \tag{C.13}$$

Fourier pair

$$x(t) \circ\!\!-\!\!\bullet\, \underline{X}(\omega) \tag{C.14}$$

Tables of Fourier pairs can be found e.g. in [124] and in [125]

Fourier pair

$$x(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \underline{X}(\omega) e^{j\omega t} d\omega \tag{C.15}$$

$$\circ\!\!\downarrow\!\!\bullet$$

$$\underline{X}(\omega) = \int_{-\infty}^{+\infty} x(t) e^{-j\omega t} dt \tag{C.16}$$

- Wiener-Khintchine theorem

$$R(\tau) \circ\!\!-\!\!\bullet\, S(\omega) \tag{C.17}$$

$$\rho(\tau) \circ\!\!-\!\!\bullet\, E(\omega) \tag{C.18}$$

- Total energy E_{tot}

$$E_{tot} = \frac{1}{2\pi}\int_{-\infty}^{+\infty} E(\omega)d\omega = x_{sum}^2 = \int_{-\infty}^{+\infty} [x(t)]^2\, dt = \rho(0) \tag{C.19}$$

- Total power S_{tot}

$$S_{tot} = \frac{1}{2\pi}\int_{-\infty}^{+\infty} S(\omega)d\omega = x_{eff}^2 = \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2} [x(t)]^2\, dt = R(0) \tag{C.20}$$

C.2 Signal Classification

		Finite Energy Signal (FES)	Finite Power Signal (FPS)
Spectrum	$\underline{X}(\omega)$	$\int_{-\infty}^{+\infty} x(t)e^{-j\omega t}dt$	–
Autocorrelation Integral Function	$\rho(\tau)$	$\int_{-\infty}^{+\infty} x(t)x(t+\tau)dt$	–
Energy Spectrum	$E(\omega)$	$\lvert\underline{X}(\omega)\rvert^2$	–
Total Energy	E_{tot}	$\frac{1}{2\pi}\int_{-\infty}^{+\infty} E(\omega)d\omega$	∞
Autocorrelation Function	$R(\tau)$	0	$\lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2} x(t)x(t+\tau)dt$
Power Spectrum	$S(\omega)$	0	$\lim_{T\to\infty}\frac{1}{T}\lvert\underline{X}(\omega)\rvert^2$
Total Power	S_{tot}	0	$\frac{1}{2\pi}\int_{-\infty}^{+\infty} S(\omega)d\omega$

Tab. C.1: Signal classification.

- Typical finite power signals (FPS):
  - Periodic signal
  - Stationary random signal

C.3 Signal Spectra

Time Domain		Frequency Domain
Continuous-Time Time-Limited Signal		Continuous Nonperiodic Spectrum
$x(t) = \frac{1}{2\pi}\int_{-\infty}^{+\infty} \underline{X}(\omega) e^{j\omega t} d\omega$	$\circ\!\!-\!\!\bullet$	$\underline{X}(\omega) = \int_{-\infty}^{+\infty} x(t) e^{-j\omega t} dt$
Discrete-Time Time-Limited Signal		Continuous Periodic Spectrum
$x^*(t) = x(t) s_s^\delta(t) = \sum_{k=-\infty}^{+\infty} x(kT_s)\delta(t-kT_s)$	$\circ\!\!-\!\!\bullet$	$\underline{X}^*(\omega) = \frac{1}{2\pi}\underline{X}(\omega) * S_s^\delta(\omega) = \frac{\omega_s}{2\pi}\sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s)$
$x(kT_s) = \frac{1}{\omega_s}\int_{-\omega_s/2}^{+\omega_s/2} \underline{X}^*(\omega) e^{j\omega kT_s} d\omega$	reverse Fourier series $\Longleftrightarrow$	$\underline{X}^*(\omega) = \sum_{k=-\infty}^{+\infty} x(kT_s) e^{-j\omega kT_s}$
Continuous-Time Periodic Signal		Discrete Nonperiodic Spectrum
$x_p(t) = x(t) * s_p^\delta(t) = \sum_{k=-\infty}^{+\infty} x(t-kT_p)$	$\circ\!\!-\!\!\bullet$	$\underline{X}_p(\omega) = \underline{X}(\omega) S_p^\delta(\omega) = \omega_p \sum_{n=-\infty}^{+\infty} \underline{X}(n\omega_p)\delta(\omega - n\omega_p) = \sum_{n=-\infty}^{+\infty} 2\pi \underline{c}_n \delta(\omega - n\omega_p)$
$x_p(t) = \sum_{n=-\infty}^{+\infty} \underline{c}_n e^{jn\omega_p t}$	Fourier series $\Longleftrightarrow$	$\underline{c}_n = \frac{1}{T_p}\int_{-T_p/2}^{+T_p/2} x_p(t) e^{-jn\omega_p t} dt = \frac{\omega_p}{2\pi}\underline{X}(n\omega_p)$

Tab. C.2: Signal spectra 1.

Time Domain		Frequency Domain
Discrete-Time Periodic Signal		Discrete Periodic Spectrum
$\begin{aligned} x_p^*(t) &= x_p(t)s_s^\delta(t) \\ &= \sum_{k=-\infty}^{+\infty} x_p(kT_s)\delta(t-kT_s) \\ &= x^*(t) * s_p^\delta(t) \\ &= \sum_{k=-\infty}^{+\infty} x^*(t-kT_p) \\ &= \sum_{k=-\infty}^{+\infty} x(k)\delta(t-kT_s) \end{aligned}$	$\circ\!\!-\!\!\bullet$	$\begin{aligned} \underline{X}_p^*(\omega) &= \frac{1}{2\pi}\underline{X}_p(\omega) * S_s^\delta(\omega) \\ &= \frac{\omega_s}{2\pi}\sum_{n=-\infty}^{+\infty}\underline{X}_p(\omega-n\omega_s) \\ &= \underline{X}^*(\omega)S_p^\delta(\omega) \\ &= \omega_p\sum_{n=-\infty}^{+\infty}\underline{X}^*(n\omega_p)\delta(\omega-n\omega_p) \\ &= \sum_{n=-\infty}^{+\infty} 2\pi\underline{c}_n^*\delta(\omega-n\omega_p) \\ &= \sum_{n=-\infty}^{+\infty}\underline{X}_{p1}^*(\omega-n\omega_s) \\ &= \omega_p\sum_{n=-\infty}^{+\infty}\underline{X}(n)\delta(\omega-n\omega_p) \end{aligned}$
$x^*(t) = \sum_{k=0}^{N-1} x(kT_s)\delta(t-kT_s)$		$\underline{X}_{p1}^*(\omega) = \sum_{n=0}^{N-1} 2\pi\underline{c}_n^*\delta(\omega-n\omega_p)$
$x_p^*(t) = \sum_{n=-\infty}^{+\infty}\underline{c}_n^* e^{jn\omega_p t}$	Fourier series $\Longleftrightarrow$	$\begin{aligned} \underline{c}_n^* &= \frac{1}{T_p}\sum_{k=0}^{N-1} x(kT_s)e^{-jn\omega_p kT_s} \\ &= \frac{\omega_p}{2\pi}\underline{X}^*(n\omega_p) \end{aligned}$
$x_p(kT_s) = \frac{2\pi}{\omega_s}\sum_{n=0}^{N-1}\underline{c}_n^* e^{jn\omega_p kT_s}$	discrete Fourier series $\Longleftrightarrow$	$\underline{c}_n^* = \frac{1}{T_p}\sum_{k=0}^{N-1} x(kT_s)e^{-jn\omega_p kT_s}$
$\begin{aligned} x(k) &= \frac{1}{N}\sum_{n=0}^{N-1}\underline{X}(n)e^{j\frac{2\pi}{N}nk} \\ &= x_p(kT_s) \end{aligned}$	discrete Fourier transform $\Longleftrightarrow$	$\begin{aligned} \underline{X}(n) &= \sum_{k=0}^{N-1} x(k)e^{-j\frac{2\pi}{N}nk} \\ &= \frac{2\pi}{\omega_p}\underline{c}_n^* \\ &= \underline{X}^*(n\omega_p) \end{aligned}$

Tab. C.3: Signal spectra 2.

Time Domain	Frequency Domain
Transformation Functions	
$s_s^\delta(t) = \sum_{k=-\infty}^{+\infty} \delta(t - kT_s)$	$S_s^\delta(\omega) = \omega_s \sum_{n=-\infty}^{+\infty} \delta(\omega - n\omega_s)$
	$\omega_s = \frac{2\pi}{T_s}$
$s_p^\delta(t) = \sum_{k=-\infty}^{+\infty} \delta(t - kT_p)$	$S_p^\delta(\omega) = \omega_p \sum_{n=-\infty}^{+\infty} \delta(\omega - n\omega_p)$
	$\omega_p = \frac{2\pi}{T_p}$
$T_p = NT_s$	$\omega_p = \frac{\omega_s}{N}$

Tab. C.4: Signal spectra 3.

C.4 Noise Power Spectra

- Stationary[1] stochastic signals

C.4.1 White Noise

- Power spectral density $S(\omega)$ (double-sided)

$$S(\omega) = S_0 \tag{C.21}$$

- Autocorrelation function $R(\tau)$

$$R(\tau) = S_0\delta(\tau) \tag{C.22}$$

Delta function $\delta(\tau)$

[1] Statistical properties are invariant to a shift of the origin

$$\delta(\tau) = 0 \quad , \tau \neq 0 \tag{C.23}$$

$$\int_{-\infty}^{+\infty} \delta(\tau) d\tau = 1 \tag{C.24}$$

- Total power S_{tot}

$$S_{tot} = R(0) = S_0 \delta(0) \tag{C.25}$$

C.4.2 Band-Limited White Noise

- Power spectral density $S(\omega)$ (double-sided)

$$S(\omega) = \begin{cases} S_0 & |\omega| \leq \omega_0 \\ 0 & |\omega| > \omega_0 \end{cases} \tag{C.26}$$

- Autocorrelation function $R(\tau)$

$$R(\tau) = \frac{S_0 \omega_0}{\pi} \frac{\sin(\omega_0 \tau)}{(\omega_0 \tau)} \tag{C.27}$$

- Total power S_{tot}

$$S_{tot} = R(0) = \frac{S_0 \omega_0}{\pi} = 2 S_0 B \tag{C.28}$$

Noise bandwidth B

$$\omega_0 = 2\pi B \tag{C.29}$$

C.4.3 1/f Noise

- Power spectral density $S(\omega)$ (double-sided)

$$S(\omega) = \frac{S_0}{|\omega|} \tag{C.30}$$

- Autocorrelation function $R(\tau)$

$$R(\tau) = \frac{S_0}{\pi} \int_0^\infty \frac{\cos(\omega\tau)}{\omega} d\omega \longrightarrow \infty \tag{C.31}$$

- Total power S_{tot}

$$S_{tot} = R(0) = \frac{S_0}{\pi} \int_0^\infty \frac{1}{\omega} d\omega \longrightarrow \infty \tag{C.32}$$

C.4.4 Band-Limited 1/f Noise

- Power spectral density $S(\omega)$ (double-sided)

$$S(\omega) = \begin{cases} \frac{S_0}{|\omega|} & |\omega| \leq \omega_0 \\ 0 & |\omega| > \omega_0 \end{cases} \tag{C.33}$$

- Autocorrelation function $R(\tau)$

$$R(\tau) = \frac{S_0}{\pi} \int_0^{\omega_0} \frac{\cos(\omega\tau)}{\omega} d\omega \longrightarrow \infty \tag{C.34}$$

- Total power S_{tot}

$$S_{tot} = R(0) = \frac{S_0}{\pi} \int_0^{\omega_0} \frac{1}{\omega} d\omega \longrightarrow \infty \tag{C.35}$$

C.5 Linear Systems

- Input signal $x(t)$
- Impulse response $g(t)$
- Output signal $y(t)$

$$y(t) = g(t) * x(t) = \int_{-\infty}^{+\infty} g(\tau) x(t-\tau) d\tau \tag{C.36}$$

- Input spectral density $\underline{X}(\omega)$ (double-sided)
- Transfer function $\underline{G}(\omega)$

$$g(t) \circ\!\!-\!\!\bullet\, \underline{G}(\omega) \tag{C.37}$$

- Output spectral density $\underline{Y}(\omega)$ (double-sided)

$$\underline{Y}(\omega) = \underline{G}(\omega)\underline{X}(\omega) \tag{C.38}$$

- Input power spectral density $S_x(\omega)$ (double-sided)
- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = |\underline{G}(\omega)|^2 S_x(\omega) \tag{C.39}$$

- Input autocorrelation function $R_x(\tau)$
- Output autocorrelation function $R_y(\tau)$

C.6 First-Order Low-Pass Filter

C.6.1 Transfer Function

- Impulse response $g(t)$

$$g(t) = \begin{cases} 0 & t < 0 \\ \omega_0 e^{-\omega_0 t} & t \geq 0 \end{cases} \tag{C.40}$$

  Cut-off angular frequency ω_0

$$\omega_0 = 2\pi B \tag{C.41}$$

  Bandwidth B

- Transfer function $\underline{G}(\omega)$

$$\underline{G}(\omega) = \frac{1}{1 + j\frac{\omega}{\omega_0}} \tag{C.42}$$

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \frac{1}{1 + (\frac{\omega}{\omega_0})^2} S_x(\omega) \tag{C.43}$$

C.6.2 White Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \frac{S_0}{1 + (\frac{\omega}{\omega_0})^2} \tag{C.44}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \frac{S_0 \omega_0}{2} e^{-\omega_0 |\tau|} \tag{C.45}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = \frac{S_0 \omega_0}{2} = 2 S_0 \frac{\pi}{2} B = 2 S_0 B_n \tag{C.46}$$

Noise-effective bandwidth B_n

$$B_n = \frac{\pi}{2} B \tag{C.47}$$

C.6.3 1/f Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \frac{S_0}{|\omega| \left[1 + (\frac{\omega}{\omega_0})^2\right]} \tag{C.48}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \frac{S_0}{\pi} \int_0^\infty \frac{\cos(\omega\tau)}{\omega \left[1 + (\frac{\omega}{\omega_0})^2\right]} d\omega \longrightarrow \infty \tag{C.49}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = \frac{S_0}{\pi} \int_0^\infty \frac{1}{\omega \left[1 + (\frac{\omega}{\omega_0})^2\right]} d\omega \longrightarrow \infty \tag{C.50}$$

C.7 Correlated Double Sampling

C.7.1 Transfer Function

- Impulse response $g(t)$

$$g(t) = \delta(t) - \delta(t - \Delta t) \tag{C.51}$$

Double sampling time Δt

$$\Delta t > 0 \tag{C.52}$$

- Output signal $y(t)$

$$y(t) = x(t) - x(t - \Delta t) \tag{C.53}$$

- Transfer function $\underline{G}(\omega)$

$$\underline{G}(\omega) = 1 - e^{-j\omega\Delta t} \tag{C.54}$$

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = 2\left[1 - \cos(\omega\Delta t)\right] S_x(\omega) \tag{C.55}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = 2R_x(\tau) - R_x(\tau + \Delta t) - R_x(\tau - \Delta t) \tag{C.56}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = 2\left[R_x(0) - R_x(\Delta t)\right] \tag{C.57}$$

This relation can also be found in [59]

C.7.2 White Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = 2S_0 \left[1 - \cos(\omega \Delta t)\right] \tag{C.58}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = S_0 \left[2\delta(0) - \delta(\tau + \Delta t) - \delta(\tau - \Delta t)\right] \tag{C.59}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = 2S_0 \left[\delta(0) - \delta(\Delta t)\right] \tag{C.60}$$

C.7.3 Band-Limited White Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \begin{cases} 2S_0 \left[1 - \cos(\omega \Delta t)\right] & |\omega| \leq \omega_0 \\ 0 & |\omega| > \omega_0 \end{cases} \tag{C.61}$$

- Output autocorrelation function $R_y(\tau)$

$$\begin{aligned} R_y(\tau) \quad = \quad & \frac{S_0 \omega_0}{\pi} \left(2 \frac{\sin(\omega_0 \tau)}{(\omega_0 \tau)} - \frac{\sin[\omega_0(\tau + \Delta t)]}{[\omega_0(\tau + \Delta t)]} \right. \\ & \left. - \frac{\sin[\omega_0(\tau - \Delta t)]}{[\omega_0(\tau - \Delta t)]} \right) \end{aligned} \tag{C.62}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = \frac{2S_0 \omega_0}{\pi} \left[1 - \frac{\sin(\omega_0 \Delta t)}{(\omega_0 \Delta t)} \right] \tag{C.63}$$

C.7.4 First-Order Low-Pass Filtered White Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = 2S_0 \frac{[1 - \cos(\omega \Delta t)]}{1 + (\frac{\omega}{\omega_0})^2} \tag{C.64}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \begin{cases} S_0\omega_0 \left[e^{-\omega_0|\tau|} - e^{-\omega_0 \Delta t} \cosh(\omega_0 \tau)\right] & |\tau| \leq \Delta t \\ S_0\omega_0 e^{-\omega_0|\tau|} \left[1 - \cosh(\omega_0 \Delta t)\right] & |\tau| > \Delta t \end{cases} \tag{C.65}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = S_0\omega_0 \left[1 - e^{-\omega_0 \Delta t}\right] \tag{C.66}$$

C.7.5 1/f Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = 2S_0 \frac{[1 - \cos(\omega \Delta t)]}{|\omega|} \tag{C.67}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \frac{2S_0}{\pi} \int_0^\infty \cos(\omega\tau) \frac{[1 - \cos(\omega \Delta t)]}{\omega} d\omega \longrightarrow \infty \tag{C.68}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = \frac{2S_0}{\pi} \int_0^\infty \frac{[1 - \cos(\omega \Delta t)]}{\omega} d\omega \longrightarrow \infty \tag{C.69}$$

C.7.6 Band-Limited 1/f Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \begin{cases} 2S_0 \frac{[1-\cos(\omega\Delta t)]}{|\omega|} & |\omega| \leq \omega_0 \\ 0 & |\omega| > \omega_0 \end{cases} \tag{C.70}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \frac{2S_0}{\pi} \int_0^{\omega_0} \cos(\omega\tau) \frac{[1-\cos(\omega\Delta t)]}{\omega} d\omega \tag{C.71}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = \frac{2S_0}{\pi} \int_0^{\omega_0} \frac{[1-\cos(\omega\Delta t)]}{\omega} d\omega \tag{C.72}$$

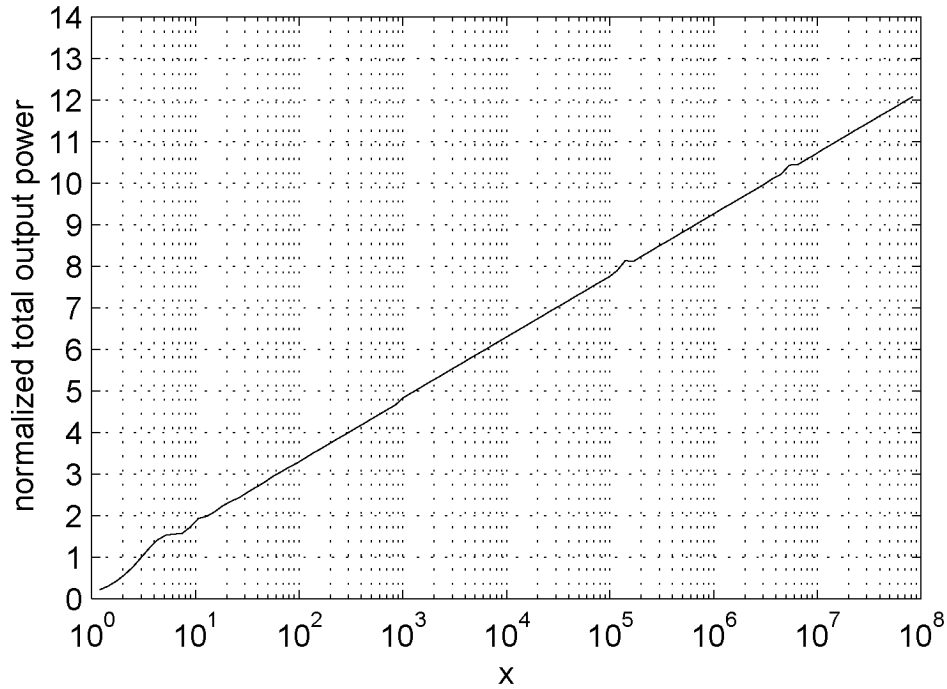


Fig. C.1: Total output power of band-limited 1/f noise (normalized by S_0) according to (C.72) versus the product of the bandwidth and the double sampling time ($x = \omega_0 \Delta t$).

C.7.7 First-Order Low-Pass Filtered 1/f Noise

- Output power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = 2S_0 \frac{[1-\cos(\omega\Delta t)]}{|\omega|\left[1+(\frac{\omega}{\omega_0})^2\right]} \tag{C.73}$$

- Output autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \frac{2S_0}{\pi}\int_0^\infty \cos(\omega\tau)\frac{[1-\cos(\omega\Delta t)]}{\omega\left[1+(\frac{\omega}{\omega_0})^2\right]}d\omega \tag{C.74}$$

- Total output power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = \frac{S_0}{\pi}\int_0^{\omega_0\Delta t}\left[e^x E_1(x) - e^{-x}E_1(-x)\right]dx \tag{C.75}$$

Exponential integral

$$E_1(x) = \int_x^\infty \frac{e^{-t}}{t}dt \tag{C.76}$$

- Derivation of (C.75):
Using (C.57)

$$S_{y_{tot}} = 2\left[R_x(0) - R_x(\Delta t)\right] = -2\int_0^{\Delta t}\frac{\partial\left[R_x(\tau)\right]}{\partial\tau}d\tau \tag{C.77}$$

Using (C.49)

$$\begin{aligned}\frac{\partial\left[R_x(\tau)\right]}{\partial\tau} &= -\frac{S_0}{\pi}\int_0^\infty \frac{\sin(\omega\tau)}{\left[1+(\frac{\omega}{\omega_0})^2\right]}d\omega \\ &= -\frac{S_0\omega_0^2}{\pi}\int_0^\infty \frac{1}{\omega^2+\omega_0^2}\sin(\omega\tau)d\omega \end{aligned} \tag{C.78}$$

$$\int_0^\infty \frac{1}{\omega^2+\omega_0^2}\sin(\omega\tau)d\omega$$

Fourier sine transform $g(y)$

$$g(y) = \int_0^\infty f(x)\sin(xy)dx \quad , y > 0 \tag{C.79}$$

of $f(x)$

$$f(x) = \frac{1}{x^2+a^2} \quad , a > 0 \tag{C.80}$$

with

$$\begin{aligned} x &= \omega \\ y &= \tau \\ a &= \omega_0 \end{aligned} \tag{C.81}$$

According to [125]

$$\int_0^\infty \frac{1}{\omega^2+\omega_0^2}\sin(\omega\tau)d\omega = \frac{1}{2\omega_0}\left[e^{-\omega_0\tau}\overline{\mathrm{Ei}}(\omega_0\tau) - e^{\omega_0\tau}\mathrm{Ei}(-\omega_0\tau)\right] \tag{C.82}$$

with

$$\overline{\mathrm{Ei}}(\omega_0\tau) = \frac{1}{2}[\mathrm{Ei}(\omega_0\tau + j0) + \mathrm{Ei}(\omega_0\tau - j0)] = \mathrm{Ei}(\omega_0\tau) \tag{C.83}$$

and

$$\mathrm{Ei}(\omega_0\tau) = -E_1(-\omega_0\tau) \tag{C.84}$$

Using (C.78)

$$\frac{\partial\left[R_x(\tau)\right]}{\partial\tau} = -\frac{S_0\omega_0}{2\pi}\left[e^{\omega_0\tau}E_1(\omega_0\tau) - e^{-\omega_0\tau}E_1(-\omega_0\tau)\right] \tag{C.85}$$

Using (C.77)

$$\begin{aligned} S_{y_{tot}} &= \frac{S_0\omega_0}{\pi}\int_0^{\Delta t}\left[e^{\omega_0\tau}E_1(\omega_0\tau) - e^{-\omega_0\tau}E_1(-\omega_0\tau)\right]d\tau \\ &= \frac{S_0}{\pi}\int_0^{\omega_0\Delta t}\left[e^{x}E_1(x) - e^{-x}E_1(-x)\right]dx \end{aligned} \tag{C.86}$$

Confirmation of (C.75)
Same result obtained in [41]

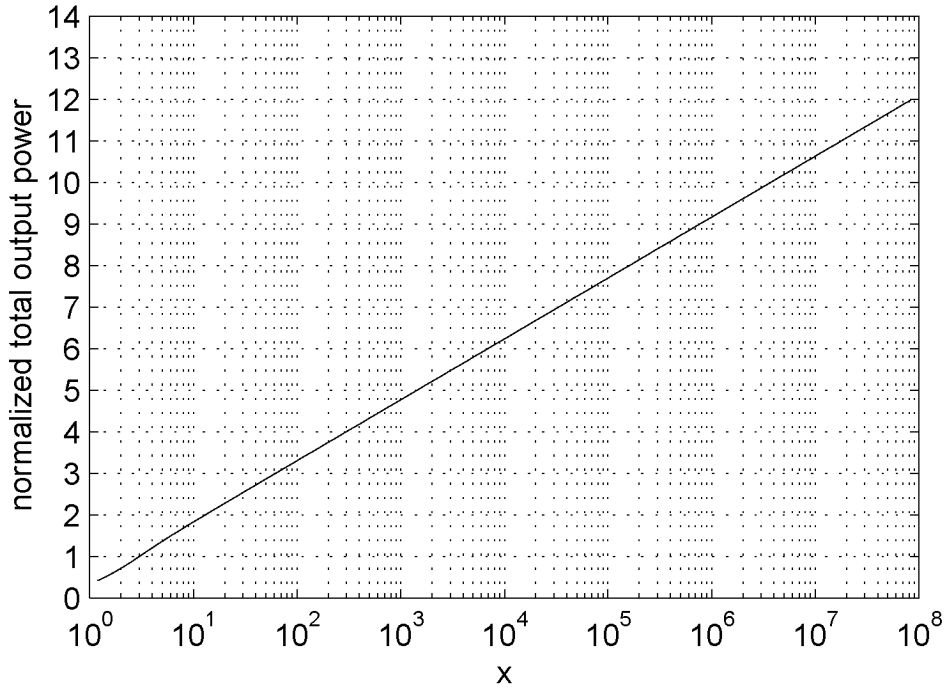


Fig. C.2: Total output power of first-order low-pass filtered 1/f noise (normalized by S_0) according to (C.75) versus the product of the bandwidth and the double sampling time ($x = \omega_0\Delta t$).

- Approximation of (C.75) for $\omega_0\Delta t \gg 1$:
  According to [126]

$$E_1(x) = \Gamma(0,x) = \lim_{a\to\infty}\Gamma(a,x) \tag{C.87}$$

Complementary incomplete gamma function $\Gamma(a,x)$
Asymptotic series

$$\begin{aligned} E_1(x) &= \frac{e^{-x}}{x}\left(1-\frac{1}{x}+\frac{2}{x^2}-\frac{6}{x^3}+...\right) \\ &\approx \frac{e^{-x}}{x} \quad ,x \gg 1 \end{aligned} \tag{C.88}$$

$$\begin{aligned} e^x E_1(x) - e^{-x} E_1(-x) &\approx e^x \frac{e^{-x}}{x} - e^{-x}\frac{e^x}{-x} \quad ,x \gg 1 \\ &\approx \frac{2}{x} \quad ,x \gg 1 \end{aligned} \tag{C.89}$$

For

$$\omega_0 \Delta t > x_0 \gg 1 \tag{C.90}$$

$$\begin{aligned} S_{y_{tot}} &\approx \frac{S_0}{\pi}\left[\int_0^{x_0}\left[e^x E_1(x) - e^{-x}E_1(-x)\right]dx + \int_{x_0}^{\omega_0\Delta t}\frac{2}{x}dx\right] \\ &\approx \frac{S_0}{\pi}\left[\int_0^{x_0}\left[e^x E_1(x) - e^{-x}E_1(-x)\right]dx - 2\ln(x_0)\right. \\ &\quad \left. +2\ln(\omega_0\Delta t)\right] \end{aligned} \tag{C.91}$$

- Substitution of (C.75)

$$S_{y_{tot}} \approx \frac{S_0}{\pi}\left[1+2\ln(\omega_0\Delta t)\right] \quad ,\omega_0\Delta t > 25 \tag{C.92}$$

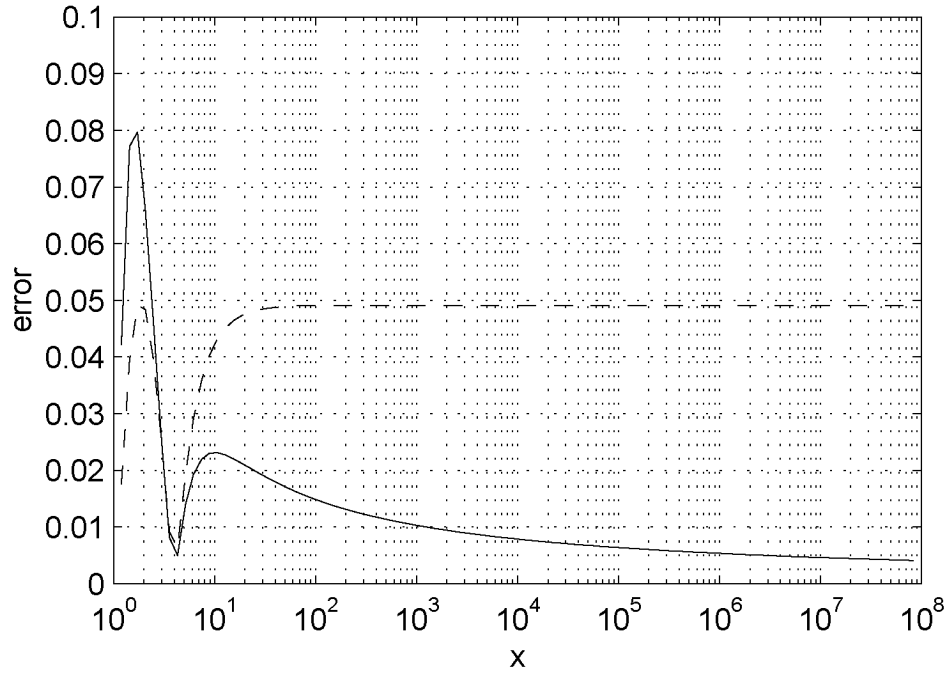


Fig. C.3: Absolute (- -) and relative (—) error of the substitution (C.92) compared to the exact total output power of first-order low-pass filtered 1/f noise according to (C.75). The values are plotted versus the product of the bandwidth and the double sampling time ($x = \omega_0 \Delta t$).

Relative error ϵ_r

$$\epsilon_r < 0.02 \quad , \omega_0 \Delta t > 25 \tag{C.93}$$

C.8 Sampling

C.8.1 Input Signal

- Input signal $x(t)$

$$x(t) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \underline{X}(\omega) e^{j\omega t} d\omega \tag{C.94}$$

- Input spectral density $\underline{X}(\omega)$ (double-sided)

$$\underline{X}(\omega) = \int_{-\infty}^{+\infty} x(t) e^{-j\omega t} dt \tag{C.95}$$

- Input power spectral density $S_x(\omega)$ (double-sided)

$$S_x(\omega) = \lim_{T\to\infty} \frac{1}{T} |\underline{X}(\omega)|^2 \tag{C.96}$$

- Input autocorrelation function $R_x(\tau)$

$$R_x(\tau) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} x(t) x(t+\tau) dt \tag{C.97}$$

- Total input power $S_{x_{tot}}$

$$S_{x_{tot}} = R_x(0) = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{+T/2} [x(t)]^2 \, dt \tag{C.98}$$

C.8.2 Transfer Characteristics

- Sampling function $f_s(t)$

$$f_s(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT_s) \tag{C.99}$$

  Sampling period T_s

- Output signal $y(t)$

$$y(t) = f_s(t) x(t) \tag{C.100}$$

- Sampling transfer characteristics $F_s(\omega)$

$$F_s(\omega) = \omega_s \sum_{n=-\infty}^{+\infty} \delta(\omega - n\omega_s) \tag{C.101}$$

  Sampling angular frequency ω_s

$$\omega_s = \frac{2\pi}{T_s} \tag{C.102}$$

- Output spectral density $\underline{Y}(\omega)$ (double-sided)

$$\underline{Y}(\omega) = \frac{1}{2\pi} F_s(\omega) * \underline{X}(\omega) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} F_s(\Omega)\underline{X}(\omega - \Omega)d\Omega \tag{C.103}$$

C.8.3 Sampled Signal

- Sampled signal $y(t)$

$$y(t) = \sum_{n=-\infty}^{+\infty} x(nT_s)\delta(t - nT_s) \tag{C.104}$$

Signal samples $x(nT_s)$

$$x(nT_s) = \frac{1}{\omega_s} \int_{-\omega_s/2}^{+\omega_s/2} \underline{Y}(\omega)e^{j\omega nT_s} d\omega \tag{C.105}$$

- Sampled spectral density $\underline{Y}(\omega)$ (double-sided)

$$\underline{Y}(\omega) = \frac{\omega_s}{2\pi} \sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s) = \sum_{n=-\infty}^{+\infty} x(nT_s)e^{-j\omega nT_s} \tag{C.106}$$

- Sampled power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \lim_{T\to\infty} \frac{1}{T} \left(\frac{\omega_s}{2\pi}\right)^2 \left| \sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s) \right|^2 \tag{C.107}$$

- Sampled autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \sum_{n=-\infty}^{+\infty} x_R(nT_s) \frac{1}{T_s} \delta(\tau - nT_s) \tag{C.108}$$

Autocorrelation samples function $x_R(nT_s)$

$$x_R(nT_s) = \lim_{N\to\infty} \frac{1}{2N} \sum_{k=-N}^{+N} x(kT_s)x([k+n]T_s) \tag{C.109}$$

- Total sampled power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = x_R(0)\frac{1}{T_s}\delta(0) = \lim_{N\to\infty} \frac{1}{2N} \sum_{k=-N}^{+N} [x(kT_s)]^2 \frac{1}{T_s}\delta(0) \tag{C.110}$$

C.9 Holding

C.9.1 Input Signal

- Input signal $y(t)$

$$y(t) = \sum_{n=-\infty}^{+\infty} x(nT_s)\delta(t - nT_s) \tag{C.111}$$

Signal samples $x(nT_s)$ in (C.105)

- Input spectral density $\underline{Y}(\omega)$ (double-sided)

$$\underline{Y}(\omega) = \frac{\omega_s}{2\pi} \sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s) = \sum_{n=-\infty}^{+\infty} x(nT_s)e^{-j\omega nT_s} \tag{C.112}$$

- Input power spectral density $S_y(\omega)$ (double-sided)

$$S_y(\omega) = \lim_{T\to\infty} \frac{1}{T} \left(\frac{\omega_s}{2\pi}\right)^2 \left| \sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s) \right|^2 \tag{C.113}$$

- Input autocorrelation function $R_y(\tau)$

$$R_y(\tau) = \sum_{n=-\infty}^{+\infty} x_R(nT_s)\frac{1}{T_s}\delta(\tau - nT_s) \tag{C.114}$$

Autocorrelation samples function $x_R(nT_s)$ in (C.109)

- Total input power $S_{y_{tot}}$

$$S_{y_{tot}} = R_y(0) = x_R(0)\frac{1}{T_s}\delta(0) = \lim_{N\to\infty}\frac{1}{2N}\sum_{k=-N}^{+N}\left[x(kT_s)\right]^2\frac{1}{T_s}\delta(0) \tag{C.115}$$

C.9.2 Transfer Function

- Impulse response $g_h(t)$

$$g_h(t) = \begin{cases} 1 & 0 \le t < T_s \\ 0 & \text{else} \end{cases} \tag{C.116}$$

- Transfer function $\underline{G}_h(\omega)$

$$\underline{G}_h(\omega) = \frac{2\pi}{\omega_s}\frac{\sin\left(\frac{\omega\pi}{\omega_s}\right)}{\left(\frac{\omega\pi}{\omega_s}\right)}e^{-j\frac{\omega\pi}{\omega_s}} \tag{C.117}$$

C.9.3 Signal after Hold

- Signal after hold $z(t)$

$$z(t) = \sum_{n=-\infty}^{+\infty} x(nT_s)g_h(t - nT_s) \tag{C.118}$$

Signal samples $x(nT_s)$ in (C.105)

- Spectral density after hold $\underline{Z}(\omega)$ (double-sided)

$$\underline{Z}(\omega) = \frac{\sin\left(\frac{\omega\pi}{\omega_s}\right)}{\left(\frac{\omega\pi}{\omega_s}\right)} e^{-j\frac{\omega\pi}{\omega_s}} \sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s) \tag{C.119}$$

- Power spectral density after hold $S_z(\omega)$ (double-sided)

$$S_z(\omega) = \lim_{T\to\infty} \frac{1}{T} \frac{\left[\sin\left(\frac{\omega\pi}{\omega_s}\right)\right]^2}{\left(\frac{\omega\pi}{\omega_s}\right)^2} \left| \sum_{n=-\infty}^{+\infty} \underline{X}(\omega - n\omega_s) \right|^2 \tag{C.120}$$

- Autocorrelation function after hold $R_z(\tau)$

$$R_z(\tau) = \sum_{n=-\infty}^{+\infty} x_R(nT_s) d_s(\tau - nT_s) \tag{C.121}$$

Autocorrelation samples function $x_R(nT_s)$ in (C.109)
Triangle function $d_s(\tau)$

$$d_s(\tau) = \begin{cases} 1 - \frac{|\tau|}{T_s} & |\tau| \le T_s \\ 0 & |\tau| > T_s \end{cases} \tag{C.122}$$

- Total power after hold $S_{z_{tot}}$

$$S_{z_{tot}} = R_z(0) = x_R(0) = \lim_{N\to\infty} \frac{1}{2N} \sum_{k=-N}^{+N} [x(kT_s)]^2 \tag{C.123}$$

D. CASCODE CONFIGURATIONS FOR SWITCHED CURRENT COPIERS

D.1 Introduction

Today's analog and digital CMOS integrated circuit design is highly dominated by miniaturization and low power requirements [15].
Device down-scaling is applied in order to reduce chip area and to achieve higher packing density in monolithic integrated circuits. In addition, smaller device dimensions imply lower parasitic capacitances, and decreasing MOS transistor channel length increases transconductances, which result both in higher speed performance or lower operating currents. However, short channels decrease output impedance and therefore reduce transistor dc voltage gain. This brings up the need for a "super transistor" with improved output impedance, which can be obtained by the use of cascode circuits [127].
Beside the accompanying loss of speed, down-scaling the operating currents doesn't pose major problems. More problems are involved by down-scaling the voltages. In the case of voltage-mode operated circuits, signal swings have to be reduced accordingly. They are further reduced by the non-saturation regions of the transistors which often cannot be down-scaled accordingly. This is particularly the case in circuits where low output conductances in short channel devices are required and therefore cascodes have to be used. Circuits based on high output resistances of the amplifying devices, i.e. cascodes, are found in many applications like current sources in differential amplifiers for common-mode and power-supply rejection, or operational transconductance amplifier (OTA) output stages with large voltage gain. Switched-capacitor circuits operated with OTA's are faced with this problem. Cascodes with minimum non-saturation region are therefore of high interest.
Current-mode circuits are an alternative approach in order to operate signal pro-

cessing circuits at low supply voltages. This technique also requires current sources with high output resistances. Therefore cascode circuits which operate down to small output voltages are needed here as well, if supply voltage is reduced. Of special interest in this context are switched-current (SI) circuits [115]. Their precision depends on the output resistance of the current storage cells which are basically MOS "super transistors" with open gates. In this application the cascode problem appears in a modified version. Beside high output resistance at low output voltages additional design rules have to be followed when operated as so-called "current copiers" [117].
The aim of this paper is to investigate methods for the reduction of the non-saturation region of different cascode circuits with special emphasis on the limitations in switched current copier applications.
The paper starts with a general discussion on cascode circuits. In section D.2 the basic investigated cascode circuits are presented with their corresponding small-signal parameters. Section D.3 compares the dynamic output ranges of the different cascode circuits. Several modifications of the basic cascode idea like regulated cascodes [127] and variations of this circuit with reduced non-saturation regions [128] are discussed and compared. Simple circuits for reference voltage or current generation and dynamic output range improvement are presented in section D.4. Section D.5 discusses switched current copier circuits and compares the dynamic ranges of the different cascode circuits for use in switched current copier applications.

D.2 Cascode Circuits

D.2.1 Single Transistor

If a single transistor (ST) as shown in fig. D.1 is used as a voltage-controlled current source, the output has to be operated in the saturation region yielding maximum output resistance.
In the ohmic region, the output characteristics of the transistor can be approximated by

$$I_D = \beta \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} n V_{DS}^2 \right], \tag{D.1}$$

where V_T is the threshold voltage of the transistor. Typical values for n range from 1 to 1.5. The output resistance for small V_{DS} is very low and therefore not suitable for current source operation. The transistor remains in ohmic operation

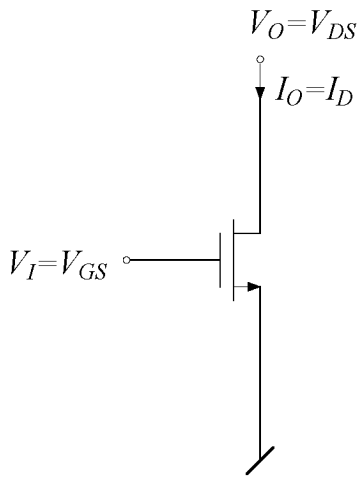


Fig. D.1: Single transistor (ST).

as long as V_{DS} does not exceed V_P, which is the value of V_{DS} that yields the maximum current I_D in (D.1) for a given V_{GS}:

$$V_P = \frac{V_{GS} - V_T}{n}. \tag{D.2}$$

If $V_{DS} \geq V_P$ the transistor is in the saturation region and in this simple model the large-signal output current becomes independent of the output voltage, thus yielding current source operation:

$$I_D = \frac{\beta}{2n}(V_{GS} - V_T)^2. \tag{D.3}$$

This is equivalent to

$$V_{GS} = V_T + \sqrt{\frac{2nI_D}{\beta}}. \tag{D.4}$$

This transfer function yields the small-signal transconductance

$$g_m = \frac{\beta}{n}(V_{GS} - V_T). \tag{D.5}$$

However there is a process dependent non-zero small-signal output conductance g_o that limits current source performance, mainly due to the channel length modulation.

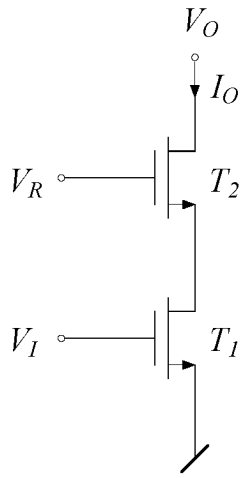


Fig. D.2: Normal cascode circuit with either a fixed (FBC) or an optimally adapted (OBC) reference voltage V_R.

D.2.2 Normal Cascode Circuit

The classical cascode circuit shown in fig. D.2 consists of a common-source stage followed by a common-gate stage that has to be biased by a reference voltage V_R. Whereas the optimally biased cascode circuit (OBC) is operated at minimum V_R still guaranteeing that both transistors are saturated for the actual output current, the fixed biased cascode circuit (FBC) has a fixed V_R that is optimal only for the maximum output current and deviates from optimum at lower currents. The transconductance of the normal cascode circuit is similar to that of the single transistor:

$$\begin{aligned} g_m(OBC) = g_m(FBC) &\approx \frac{\beta_1}{n}(V_I - V_{T1}) \\ &\approx g_{m1}. \end{aligned} \tag{D.6}$$

β_i, V_{Ti}, g_{mi} and g_{oi} refer to transistor T_i, and it is assumed that $g_{oi} \ll g_{mi}$. The output conductance in the saturation region is approximated by

$$g_o(OBC) = g_o(FBC) \approx g_{o1}\frac{g_{o2}}{g_{m2}}, \tag{D.7}$$

which is much smaller than that of the single transistor.

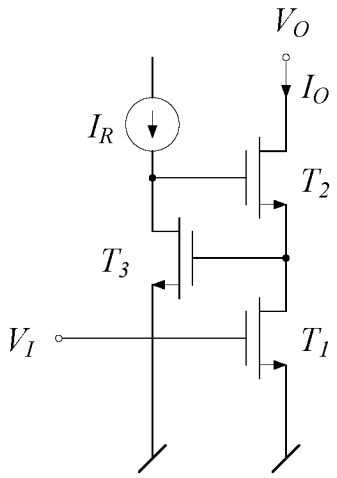


Fig. D.3: Regulated cascode circuit (RGC).

D.2.3 Regulated Cascode Circuit

The regulated cascode circuit shown in fig. D.3 is a normal cascode circuit with an amplifier stage T_3 regulating the reference voltage in order to keep V_{DS1} constant [127]. The transconductance is approximately the same as for the normal cascode circuit:

$$g_m(RGC) \approx g_{m1}. \tag{D.8}$$

The output conductance in the saturation region is further improved:

$$g_o(RGC) \approx g_{o1} \frac{g_{o2}}{g_{m2}} \frac{g_{o3}}{g_{m3}}. \tag{D.9}$$

D.2.4 Generalized Regulated Cascode Circuit

The concept of the regulated cascode circuit can be generalized to a normal cascode with an amplifier regulating the reference voltage so as to keep V_{DS1} at a defined constant value V_M. The amplifier has to sense and amplify deviations of V_{DS1} from the given reference V_M with high gain a. Fig. D.4 shows the generalized regulated cascode circuit (GRGC) consisting of a normal cascode circuit T_1 and T_2 and a differential amplifier A. The amplifier A has two inputs V_M and V_N and one output V_R. Its transfer function is given by

$$V_R = V_A + a(V_M - V_N), \tag{D.10}$$

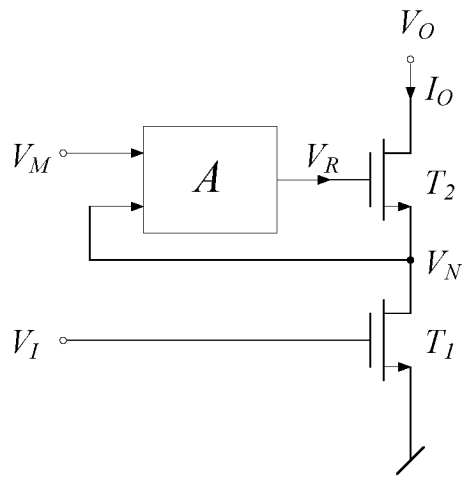


Fig. D.4: Symbolic representation of the generalized regulated cascode circuit (GRGC).

where V_A and V_M are operating point values and a is a small-signal gain. Very high gain

$$a \rightarrow \infty \tag{D.11}$$

yields the equivalence

$$V_N \approx V_M, \tag{D.12}$$

which is normally intended to obtain very high output conductance. The GRGC has again an approximated transconductance

$$g_m(GRGC) \approx g_{m1}. \tag{D.13}$$

The output conductance of this circuit with both transistors operating in saturation is approximately

$$g_o(GRGC) \approx g_{o1} \frac{g_{o2}}{g_{m2}} \frac{1}{a+1}. \tag{D.14}$$

It can be demonstrated that each of the above mentioned cascode circuits OBC, FBC and RGC represents a special case of the GRGC. It has to be emphasized that the reference V_M is not by all means a measurable voltage of the circuit, but it can be as well an implicit value of the amplifying circuit A. The amplifier A may have a non-linear transfer function, where (D.10) is the linearized transfer function in the operating point with the large-signal values V_A and V_M and with the small-signal gain a. Thus the OBC represents a GRGC

with $V_A = f_{OBC}(I_O)$ and $a = 0$, whereas the FBC is a GRGC with $V_A = V_R$ and $a = 0$ as well. The RGC represents a GRGC with $V_A = f_{RGC}(I_O)$, $V_M = V_{GS3}$ and $a = \frac{g_{m3}}{g_{o3}}$.
Another example of a GRGC would have a simple differential amplifier A with the transfer function $V_R = a(V_M - V_N)$ and an externally applied reference V_M [128].

D.3 Dynamic Output Range

D.3.1 Single Transistor

The saturation condition for the single transistor (ST) in fig. D.1 is $V_{DS} \geq V_P$. Equation (D.2) in combination with (D.3) yields the limit of the dynamic output voltage range

$$V_{O,sat}(ST) \geq \sqrt{\frac{2I_O}{\beta n}}. \tag{D.15}$$

Beside overload considerations and as long as the output voltage can be adapted accordingly, the output current range has no upper or lower limit:

$$I_{O,sat}(ST) \geq 0. \tag{D.16}$$

D.3.2 Optimally Biased Cascode Circuit

The optimally biased cascode circuit (OBC) in fig. D.2 is assumed to have a reference voltage V_R yielding the saturation limit $V_{DS1} = V_{P1}$ for transistor T_1. Thus the saturation condition for the OBC is the addition of the saturation conditions for each transistor T_1 and T_2 and yields for the limit of the dynamic output voltage range

$$V_{O,sat}(OBC) \geq \sqrt{\frac{2I_O}{\beta_1 n}} + \sqrt{\frac{2I_O}{\beta_2 n}}. \tag{D.17}$$

which is a reduction compared to the single transistor.
Assuming that the output voltage can still be adapted according to this saturation limit increase, the output current range has no upper or lower limit as well:

$$I_{O,sat}(OBC) \geq 0. \tag{D.18}$$

D.3.3 Fixed Biased Cascode Circuit

The saturation condition for the fixed biased cascode circuit (FBC) in fig. D.2 depends on the applied reference voltage V_R, since transistor T_2 is in saturation for $V_O - (V_R - V_{GS2}) \geq V_{P2}$. Using (D.3) this yields for the limit of the dynamic output voltage range

$$V_{O,sat}(FBC) \geq V_R - V_{T2} - \sqrt{\frac{2nI_O}{\beta_2}} + \sqrt{\frac{2I_O}{\beta_2 n}}. \tag{D.19}$$

The output current is limited by $V_{P1} \leq V_R - V_{GS2}$, which is the saturation condition for transistor T_1. Equations (D.2) and (D.3) yield for the output current range

$$0 \leq I_{O,sat}(FBC) \leq \left[\frac{V_R - V_{T2}}{\sqrt{\frac{2}{\beta_1 n}} + \sqrt{\frac{2n}{\beta_2}}} \right]^2. \tag{D.20}$$

Equation (D.19) can now be expressed in terms of the maximum output current I_{Max} by using the upper limit of $I_{O,sat}$ in (D.20), yielding the current range dependent limit of the dynamic output voltage range

$$\begin{aligned} V_{O,sat}(FBC) \quad \geq \quad & \sqrt{\frac{2I_{Max}}{\beta_1 n}} + \sqrt{\frac{2nI_{Max}}{\beta_2}} \\ & + \sqrt{\frac{2I_O}{\beta_2 n}} - \sqrt{\frac{2nI_O}{\beta_2}}. \end{aligned} \tag{D.21}$$

D.3.4 Regulated Cascode Circuit

In the regulated cascode circuit (RGC) in fig. D.3 the voltage V_{DS1} is kept at the constant value V_{GS3} resulting from I_R for T_3 operating in saturation. The saturation condition for transistor T_2 is $V_O - V_{GS3} \geq V_{P2}$ and yields the limit of the dynamic output voltage range

$$V_{O,sat}(RGC) \geq V_{T3} + \sqrt{\frac{2nI_R}{\beta_3}} + \sqrt{\frac{2I_O}{\beta_2 n}}. \tag{D.22}$$

The output current limit is given by the saturation condition for transistor T_1, which is $V_{GS3} \geq V_{P1}$. This yields for the output current range

$$\begin{aligned} 0 &\leq I_{O,sat}(RGC) \\ &\leq \left[\sqrt{\frac{\beta_1 n^2 I_R}{\beta_3}} + V_{T3}\sqrt{\frac{\beta_1 n}{2}}\right]^2 . \end{aligned} \tag{D.23}$$

Applying this equation for the maximum output current I_{Max} to (D.22) yields the current range dependent limit of the dynamic output voltage range

$$V_{O,sat}(RGC) \geq \sqrt{\frac{2I_{Max}}{\beta_1 n}} + \sqrt{\frac{2I_O}{\beta_2 n}}. \tag{D.24}$$

D.3.5 Generalized Regulated Cascode Circuit

Similar to the RGC, in the generalized regulated cascode circuit (GRGC) in fig. D.4 the voltage V_{DS1} is kept at a constant value, which is now V_M. The saturation condition for transistor T_2 is now $V_O - V_N \geq V_{P2}$ and yields with (D.12) the limit of the dynamic output voltage range

$$V_{O,sat}(GRGC) \geq V_M + \sqrt{\frac{2I_O}{\beta_2 n}}, \tag{D.25}$$

assuming a is very large.
$V_N \geq V_{P1}$ limits the output current range with (D.12) to

$$0 \leq I_{O,sat}(GRGC) \leq \frac{\beta_1 n V_M^2}{2}. \tag{D.26}$$

The current range dependent output voltage range corresponding to (D.25) with I_{Max} derived from (D.26) is

$$V_{O,sat}(GRGC) \geq \sqrt{\frac{2I_{Max}}{\beta_1 n}} + \sqrt{\frac{2I_O}{\beta_2 n}}. \tag{D.27}$$

which is exactly the same as for the RGC.
Fig. D.5 shows the output voltage ranges $V_{O,sat}$ of the discussed circuits operating in saturation in relation to the output current I_O at a given maximum output current I_{Max}. The ST has a large dynamic output voltage range and no output current limitation at a relatively poor output conductance. The OBC with improved output conductance still has no output current limit, but the dynamic output voltage range is reduced. The FBC has the same output conductance as the OBC, but its dynamic output voltage range is drastically reduced compared to the OBC, because the fixed reference voltage determined by the maximum output current leads to higher residual voltages at smaller output currents. Thus for the maximum output current the FBC achieves the output voltage range of the OBC, but any lower output current significantly reduces the output voltage range. The RGC with its lowest output conductance has a fixed reference current and is output current limited as well. Like the FBC the RGC achieves the output voltage range of the OBC only at the maximum output current. At lower output currents the dynamic output voltage range of the RGC is smaller than that of the OBC, but still much higher than the one of the FBC.
The discussed dynamic output voltage ranges suppose saturation of both cascaded transistors T_1 and T_2. According to (D.14) this results in lower output conductances for cascodes with $a \gg 1$. A comparison of the dynamic output voltage ranges for the different cascodes assuming a fixed upper limit of the output conductance would show considerably better results for circuits with $a \gg 1$ than those shown in fig. D.5. These circuits still have output conductance values comparable to those of classical cascodes if transistor T_2 operates in its ohmic region. A detailed analysis [129] reveals that cascodes with $a \gg 1$ (i.e. the RGC) have lower output conductances than conventional cascodes with $a = 0$ (i.e. the FBC) down to

$$V_O \approx V_M + \sqrt{\frac{I_O}{\beta_2}\frac{g_{m2}}{g_{o2}}\frac{1}{a}}. \tag{D.28}$$

The simulated curves in fig. D.6 of the output conductances of the different cascode types confirm the theoretical results for the dynamic output voltage ranges as well as the different obtainable levels of output conductances.

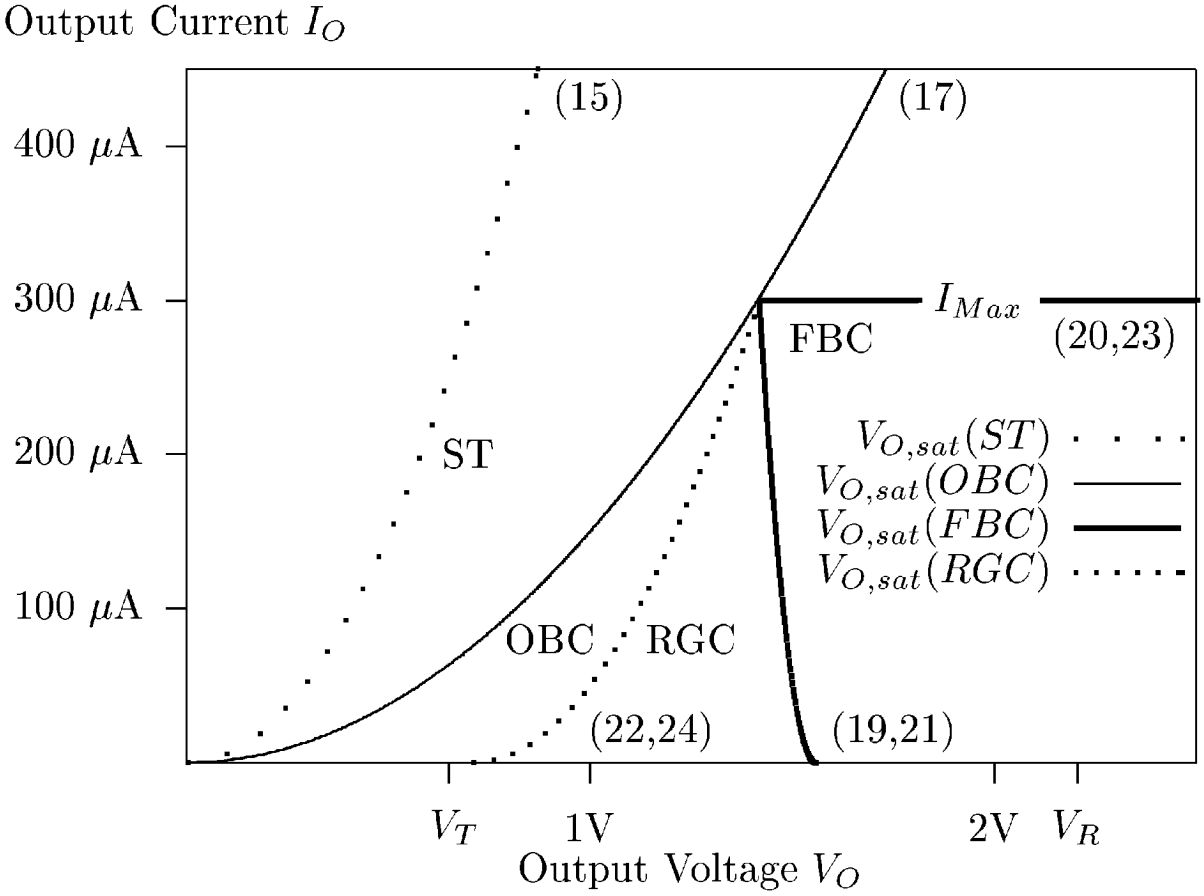


Fig. D.5: Saturation operating areas of the single transistor (ST), the optimally biased cascode circuit (OBC), the fixed biased cascode circuit (FBC) and the regulated cascode circuit (RGC). The output voltage ranges $V_{O,sat}$ are plotted in relation to the output current I_O at a given maximum occuring output current I_{Max}. The following values corresponding to a 1μ-SACMOS process are used: $V_T = 0.65$ V, $\beta = 1$ mA/V^2, $n = 1.2$, $I_{Max} = 300$ μA. The numbers in brackets indicate the equation number in the text of the corresponding curve.

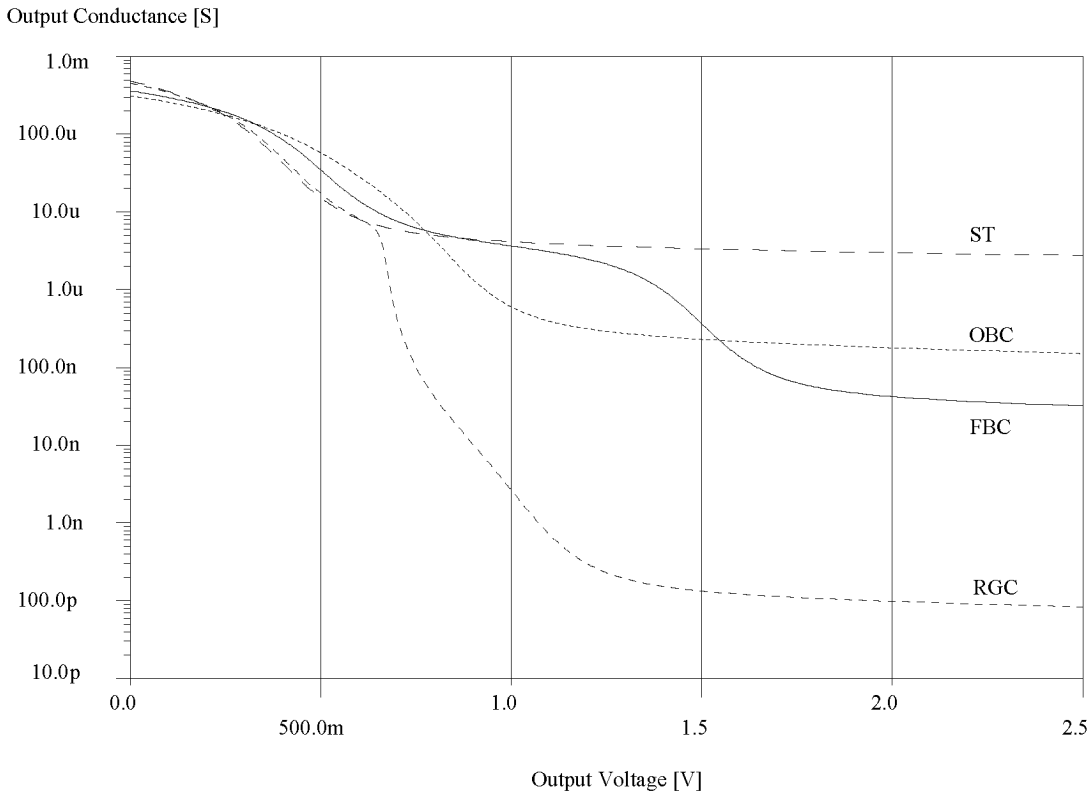


Fig. D.6: Simulated output conductances according to fig. D.5 at $I_O = 100\ \mu$A.

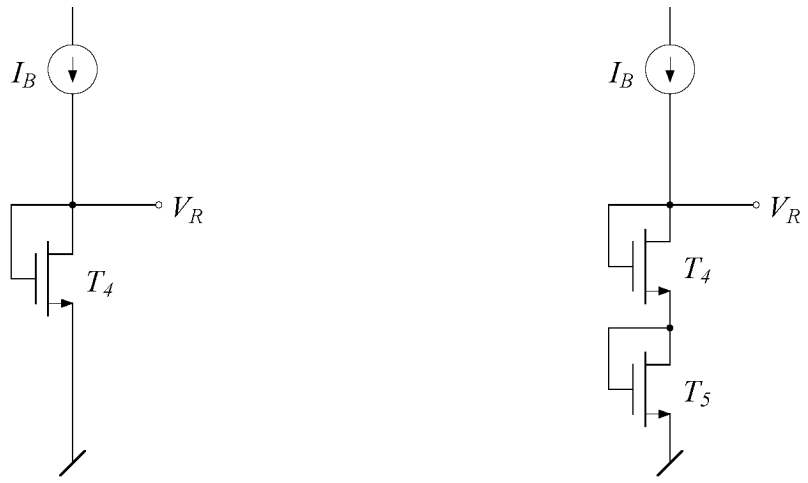


Fig. D.7: Simple constant reference voltage generation circuits.

D.4 Reference Voltage and Current Generation and Dynamic Output Range Improvement

D.4.1 Constant Reference Voltage and Current Generation

The reference voltage V_R for the OBC and FBC in fig. D.2 can be generated with a simple circuit shown in fig. D.7a. According to (D.3) the resulting voltage is

$$V_R = V_{T4} + \sqrt{\frac{2nI_B}{\beta_4}}. \tag{D.29}$$

This reference voltage can be adjusted by the selection of the bias current I_B and the transistor parameter β_4.
Significantly higher reference voltages can be generated accurately with a circuit shown in fig. D.7b. The reference voltage is now given by

$$V_R = V_{T4} + V_{T5} + \sqrt{\frac{2nI_B}{\beta_4}} + \sqrt{\frac{2nI_B}{\beta_5}}. \tag{D.30}$$

Reference voltages lower than V_{T4} may be generated with the circuit in fig. D.7a

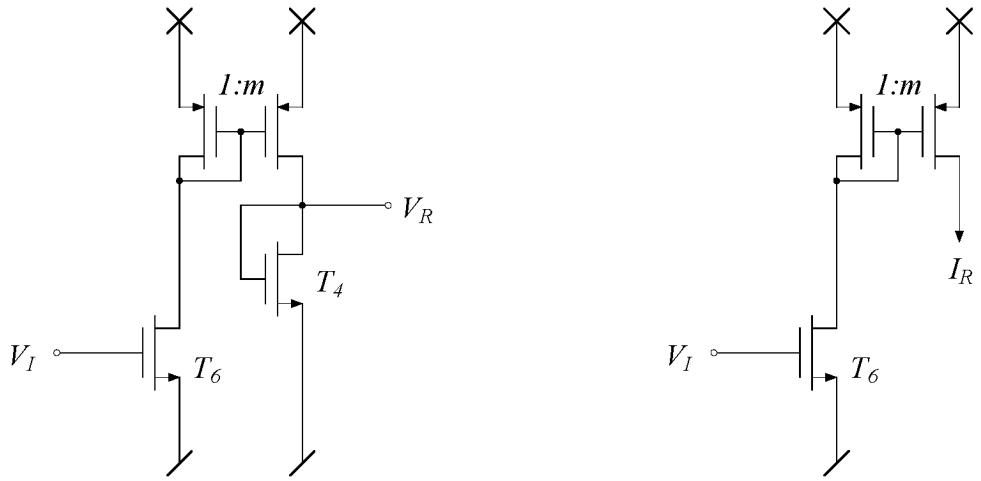


Fig. D.8: Reference voltage (a) and reference current (b) tracking circuits for adaptive cascode circuit biasing.

operating T_4 in the subthreshold region. Special care has to be taken for the equations, since (D.3) is no more valid.
Reference current generation as needed for the RGC in fig. D.3 is a standard building block in CMOS circuit design and is not discussed at this place.

D.4.2 Reference Voltage and Current Tracking

Dynamic output voltage range of the FBC in fig. D.2, the RGC in fig. D.3 and the GRGC in fig. D.4 is determined by the maximum occurring output current I_{Max} as described in (D.21), (D.24) and (D.27). An obvious solution for dynamic output voltage range improvement is the adaptation of the circuits to their actual output current level using reference voltage or current tracking. Fig. D.8a shows a circuit where the reference voltage V_R tracks the input signal V_I and fig. D.8b the corresponding circuit for the reference current I_R.
A FBC with reference voltage tracking is presented in fig. D.9. The reference voltage tracks the input voltage and the following relation between V_R and the output current I_O results:

$$V_R = \sqrt{\frac{2mn\beta_6}{\beta_1\beta_4}}\sqrt{I_O} + \sqrt{\frac{m\beta_6}{\beta_4}}(V_{T1} - V_{T6})$$

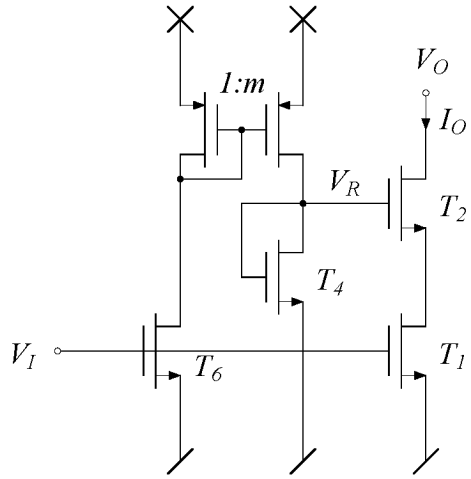


Fig. D.9: Adaptively biased normal cascode circuit derived from a fixed biased cascode circuit (FBC) with reference voltage tracking.

$$+V_{T4}. \tag{D.31}$$

Optimum biasing as assumed for the OBC is achieved for

$$V_R = \left[\sqrt{\frac{2}{\beta_1 n}} + \sqrt{\frac{2n}{\beta_2}}\right] \sqrt{I_O} + V_{T2}, \tag{D.32}$$

which can be accomplished i.e. with $\beta_1 = \beta_2 = \beta_4 = \beta_6$, $V_{T1} = V_{T2} = V_{T4} = V_{T6}$, and $m = (1 + \frac{1}{n})^2$. Thus using reference voltage tracking, the dynamic output voltage range of the FBC can be improved to that of the OBC.
A RGC with reference current tracking is presented in fig. D.10 [130]. The relation between the tracking reference current and the output current is

$$I_R = \left[\sqrt{\frac{m\beta_6}{\beta_1}}\sqrt{I_O} + \sqrt{\frac{m\beta_6}{2n}}(V_{T1} - V_{T6})\right]^2. \tag{D.33}$$

Optimum biasing for both transistors T_1 and T_2 operating in saturation at lowest possible output voltage would be achieved for

$$I_R = \left[\sqrt{\frac{\beta_3}{\beta_1 n^2}}\sqrt{I_O} - \sqrt{\frac{\beta_3}{2n}}V_{T3}\right]^2, \tag{D.34}$$

which can not be generally accomplished with (D.33). But in practice parameters have to be chosen in the way that (D.33) and (D.34) are equal for the

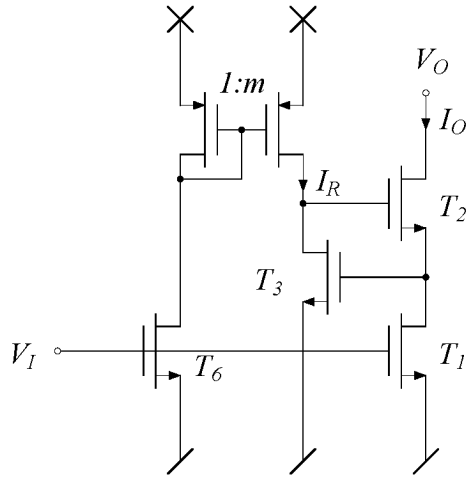


Fig. D.10: Regulated cascode circuit (RGC) with reference current tracking.

maximum occurring output current I_{Max} and that the two equations fit best for lower currents. Special care should be taken if transistor T_3 operates in the subthreshold region, since (D.3) and therefore (D.34) have to be modified. A way to further improve the fitting of (D.33) and (D.34) is to use some kind of level shifter from the gate of transistor T_3 to the drain of T_1. This is accomplished in the improved regulated cascode circuit (IRGC) that is discussed in the next chapter.
In the GRGC of fig. D.4 signal tracking would have to be accomplished for the voltage V_M. Assuming very high gain a, the requirement for V_M with (D.3) is

$$V_M = \sqrt{\frac{2I_O}{\beta_1 n}}. \tag{D.35}$$

This is the function for the signal tracking circuit generating V_M. A possible circuit realization of this function is based on the tracking circuit in fig. D.8a cascaded by a level shifting circuit in order to compensate the signal independent term in (D.31).

D.4.3 Improved Regulated Cascode Circuit

An improved regulated cascode circuit (IRGC) with signal tracking and level shifting technique is presented in fig. D.11. Assuming $V_{T1} = V_{T6}$ in (D.33), the

reference current is

$$I_R = \frac{m\beta_6}{\beta_1} I_O. \tag{D.36}$$

This yields

$$V_N = \sqrt{\frac{2mn\beta_6}{\beta_1\beta_3}}\sqrt{I_O} + V_{T3} - V_{T7} - \sqrt{\frac{2nI_B}{\beta_7}}. \tag{D.37}$$

The dynamic output voltage range of the OBC is achieved if $V_N = V_{P1}$, which yields

$$V_N = \sqrt{\frac{2}{\beta_1 n}}\sqrt{I_O}. \tag{D.38}$$

This condition can be accomplished for

$$V_{T3} = V_{T7} + \sqrt{\frac{2nI_B}{\beta_7}}, \tag{D.39}$$

which has to be adjusted to the process parameters and can also be adapted to the subthreshold region of transistor T_7 if necessary. In addition the following equation has to be fulfilled:

$$m = \frac{\beta_3}{\beta_6 n^2}. \tag{D.40}$$

This circuit achieves the dynamic output range of the OBC in combination with the high output resistance of the RGC.
In case (D.39) cannot be fulfilled, correct bias tracking is not possible. An additional bias current source applied to the drain of T_3 in fig. D.11 may then help to find a satisfactory tracking performance.

D.5 Switched Current Copiers

D.5.1 Single Transistor

A typical switched current copier cell is shown in fig. D.12 [117][119][131][118]. Single copier cells are used i.e. in dynamic current mirrors, SI output stages and complementary SI cells. In the copy phase the switch S is closed forcing

$$V_I = V_O, \tag{D.41}$$

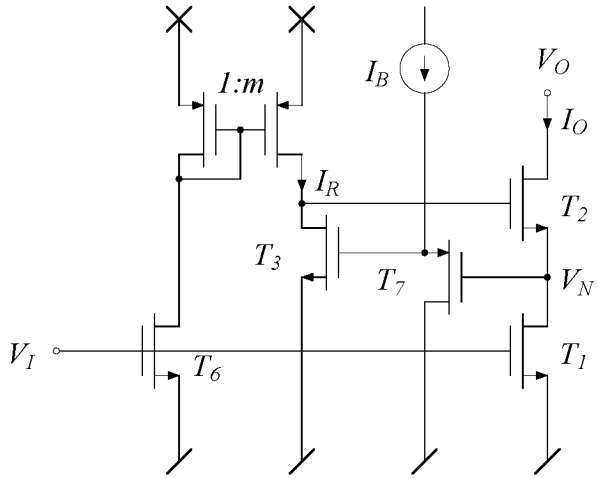


Fig. D.11: Improved regulated cascode circuit (IRGC) with reference current tracking and level shifter.

and the transistor has to be in saturation in order to yield small output conductance. The applied current I_O determines the voltage V_I that appears after a certain settling time. In the hold phase the switch S is open and the voltage V_I keeps its value, yielding the unchanged current I_O at the output as long as the transistor remains in saturation. The dynamic output voltage range in this hold phase is a key factor in circuits using switched current copiers. This range is principally the same as derived in section D.3, but it has to cover the output voltage determined by the copy phase according to (D.3) and (D.41), which is

$$V_{O,copy} = \sqrt{\frac{2nI_O}{\beta}} + V_T. \tag{D.42}$$

For the ST, (D.15) combined with (D.42) yields

$$\sqrt{\frac{2nI_O}{\beta}} + V_T \geq \sqrt{\frac{2I_O}{\beta n}}, \tag{D.43}$$

which is always true for $n \geq 1$. Thus the output current range of the ST in switched current copiers is not limited and (D.16) is still valid:

$$I_{O,copy}(ST) \geq 0. \tag{D.44}$$

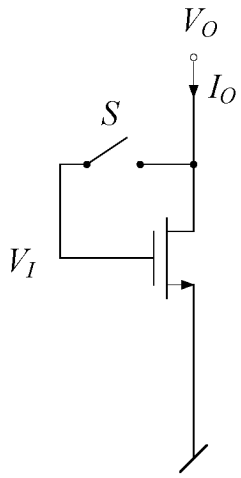


Fig. D.12: Switched current copier cell.

D.5.2 Optimally Biased Cascode Circuit

For the OBC in fig. D.2, (D.42) applies to transistor T_1. Combined with (D.17) and considering (D.18) it yields for the output current range of OBC switched current copiers

$$\begin{aligned} 0 &\leq I_{O,copy}(OBC) \\ &\leq \left[\frac{V_{T1}}{\sqrt{\frac{2}{\beta_1 n}} - \sqrt{\frac{2n}{\beta_1}} + \sqrt{\frac{2}{\beta_2 n}}}\right]^2 . \end{aligned} \tag{D.45}$$

This relation is valid for the IRGC as well.

D.5.3 Fixed Biased Cascode Circuit

In correspondence with the OBC the output current range of FBC switched current copiers is obtained from (D.19), (D.20) and (D.42) and yields

$$\begin{aligned} &\left[\frac{V_R - V_{T1} - V_{T2}}{\sqrt{\frac{2n}{\beta_1}} + \sqrt{\frac{2n}{\beta_2}} - \sqrt{\frac{2}{\beta_2 n}}}\right]^2 \\ &\leq I_{O,copy}(FBC) \leq \left[\frac{V_R - V_{T2}}{\sqrt{\frac{2}{\beta_1 n}} + \sqrt{\frac{2n}{\beta_2}}}\right]^2 . \end{aligned} \tag{D.46}$$

D.5.4 Regulated Cascode Circuit

For the RGC in fig. D.3, (D.22) and (D.23) together with (D.42) applied to transistor T_1 yield for the output current range of the RGC switched current copier:

$$\left[\frac{\sqrt{\frac{2nI_R}{\beta_3}}+V_{T3}-V_{T1}}{\sqrt{\frac{2n}{\beta_1}}-\sqrt{\frac{2}{\beta_2 n}}}\right]^2 \leq I_{O,copy}(RGC) \leq \left[\sqrt{\frac{\beta_1 n^2 I_R}{\beta_3}}+V_{T3}\sqrt{\frac{\beta_1 n}{2}}\right]^2. \quad \text{(D.47)}$$

D.5.5 Generalized Regulated Cascode Circuit

In the GRGC of fig. D.4, (D.42) applies to transistor T_1. Combined with (D.25) and considering (D.26), assuming a is very large, this yields the output current range of the GRGC switched current copier:

$$\left[\frac{V_M-V_{T1}}{\sqrt{\frac{2n}{\beta_1}}-\sqrt{\frac{2}{\beta_2 n}}}\right]^2 \leq I_{O,copy}(GRGC) \leq \frac{\beta_1 n V_M^2}{2}. \quad \text{(D.48)}$$

This is the same result as for the RGC switched current copier, but expressed in terms of the GRGC circuit.

Fig. D.13 shows the output voltage condition in the copy phase $V_{O,copy}$ according to (D.42) and the corresponding output ranges $V_{O,sat}$ and $I_{O,copy}$ of the discussed switched current copier circuits for saturation operation at a given maximum copy current I_{Max}. The ST switched current copier achieves the complete saturation operating area of the ST without any copy current limitation, but its output conductance is relatively poor. In comparison, the OBC switched current copier has an improved output conductance, but the saturation operating area is reduced due to the increased minimum output voltage and the upper copy current limit I_C, which results from the copy phase. The FBC switched current copier has only a small saturation operating area, since the fixed reference voltage refering to the maximum copy current causes a disadvatageous lower copy current limit in the copy phase and since the saturation voltage is generally

higher than that of the OBC. The maximum current in RGC switched current copiers must be lower than I_C and determines the border of the output voltage range. A lower copy current limit may exist. RGC and FBC versions achieve the minimum output voltage of the OBC version only at the maximum copy current. Compared to the FBC version, the output voltage range of the RGC version at lower copy currents is much higher and a lower copy current limit is much smaller.
The discussed operating areas suppose saturation of both cascaded transistors T_1 and T_2. Similar to the discussion of the dynamic output range in section D.3, a comparison of the operating areas for the different cascode switched current copiers assuming a fixed upper limit of the output conductance would show considerably better results for circuits with $a \gg 1$ (i.e. the RGC) than those shown in fig. D.13, since these circuits still have output conductance values comparable to those of classical cascodes (i.e. the FGC) if transistor T_2 operates in its ohmic region.
In applications where the output conductance of the ST is sufficient, the ST switched current copier is recommended due to its large operating area. If lower output conductances are required, the FBC switched current copier might be suitable due to its simple circuit design, but its small operating area may be insufficient. If even lower output conductances or larger operating areas are required, the RGC switched current copier can be used. The large operating area of the OBC switched current copier can be achieved with RGC circuits using reference current tracking.

D.5.6 Current Swing Limitations in SI Circuits

In SI circuits copier cells are often connected in cascade and operated with bias and superimposed signal current. A typical switched current copier pair is shown in fig. D.14. It can be used to memorize a signal current i_s within a two-phase clock period [119]. Single transistors are used in the two copier cells of fig. D.14 in order to simplify the drawing. They are replaced by cascode circuits for the dynamic range investigation to be presented in this section. RGCs are taken as an example, however the procedure can be used for the other cascode types as well.
A signal current i_s is copied into the left cell during the first clock phase by closing switches S_0 and S_{1a}. It is then transferred to the right cell by opening S_0 and S_{1a} and closing S_{1b} and S_{2a}. Fig. D.15 basically represents the RGC subset of the curves depicted in fig. D.13. In addition to fig. D.13, fig. D.15 shows the

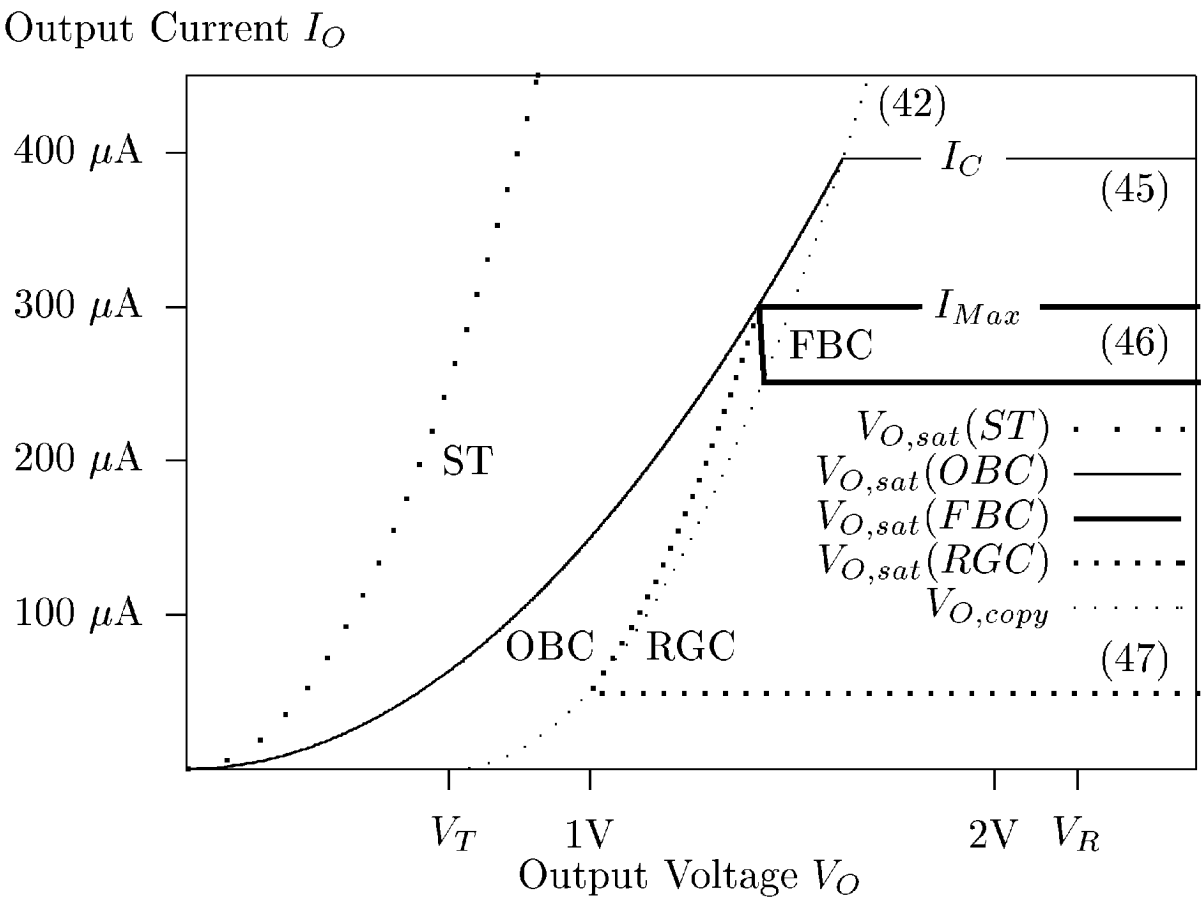


Fig. D.13: Saturation operating areas of switched current copier cells using a single transistor (ST), an optimally biased cascode circuit (OBC), a fixed biased cascode circuit (FBC) or a regulated cascode circuit (RGC). The range reduction compared to fig. D.5 is due to the feedback condition (copy voltage $V_{O,copy}$) in the copy phase. The numbers in brackets indicate the equation number in the text of the corresponding curve.

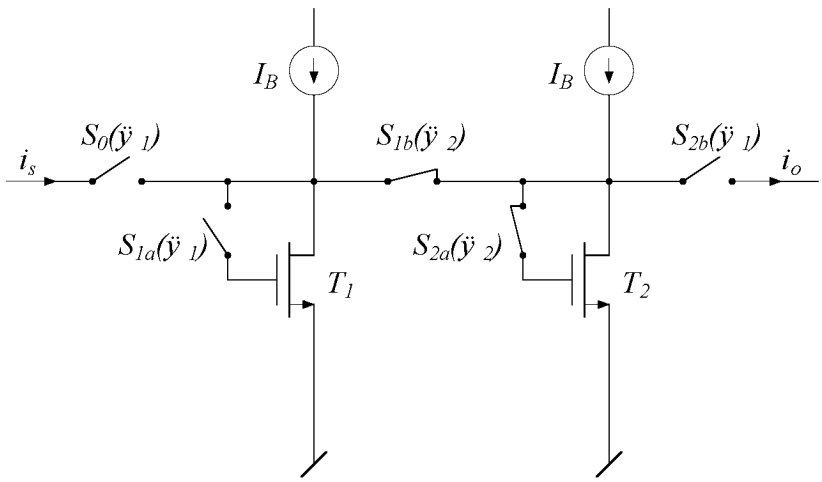


Fig. D.14: Pair of switched current copier cells representing a typical SI memory cell.

operating points of the cells when the maximum amount of positive signal current $i_{s,max}$ is applied. I_{Max} to be carried by the cells is then $I_B + i_{s,max}$.
The critical situation limiting the signal current range occurs when the positive $i_{s,max}$ is copied from the left into the right cell. The process starts with copying $I_{Max} = I_B + i_{s,max}$ into the left cell (pt. 1). According to our assumption this is the highest current flowing through the cascode. $I_{Max} \leq I_C$ has to be fulfilled for keeping $V_{O,copy} \geq V_{O,sat}(RGC)$. I_{Max} should however be chosen considerably smaller than I_C in order to allow for a dynamic range of signal currents. With the choice of I_{Max} the allowed operating area of the RGC (dotted area in fig. D.15) can be set according to (D.24) in combination with (47). The copy voltage V_H of the left cell lies well within this area (pt. 1). In the second half of the clock cycle with S_0 and S_{1a} open and S_{1b} and S_{2a} closed the current $I_B - i_{s,max}$ is flowing through the right cell. The associated copy voltage V_L of the right cell (pt. 3) is applied back to the output of the left cell still carrying I_{Max} (pt. 2). The illustration in fig. D.15 with pt. 2 (V_L, I_{Max}) lying on the $V_{O,sat}(RGC)$-curve thus characterizes the limiting situation and allows the determination of the bias current I_B which has to be chosen in the middle between pt. 2 and 3.
A similar analysis for the other discussed cascode structures shows that beside the RGC only the OBC, i.e. a normal cascode circuit with reference voltage tracking, yields a reasonable signal current range. Cascodes with fixed reference voltage are not suitable at all for switched current copier pairs.
Comparing the remaining solutions (RGC and OBC) under the assumption of

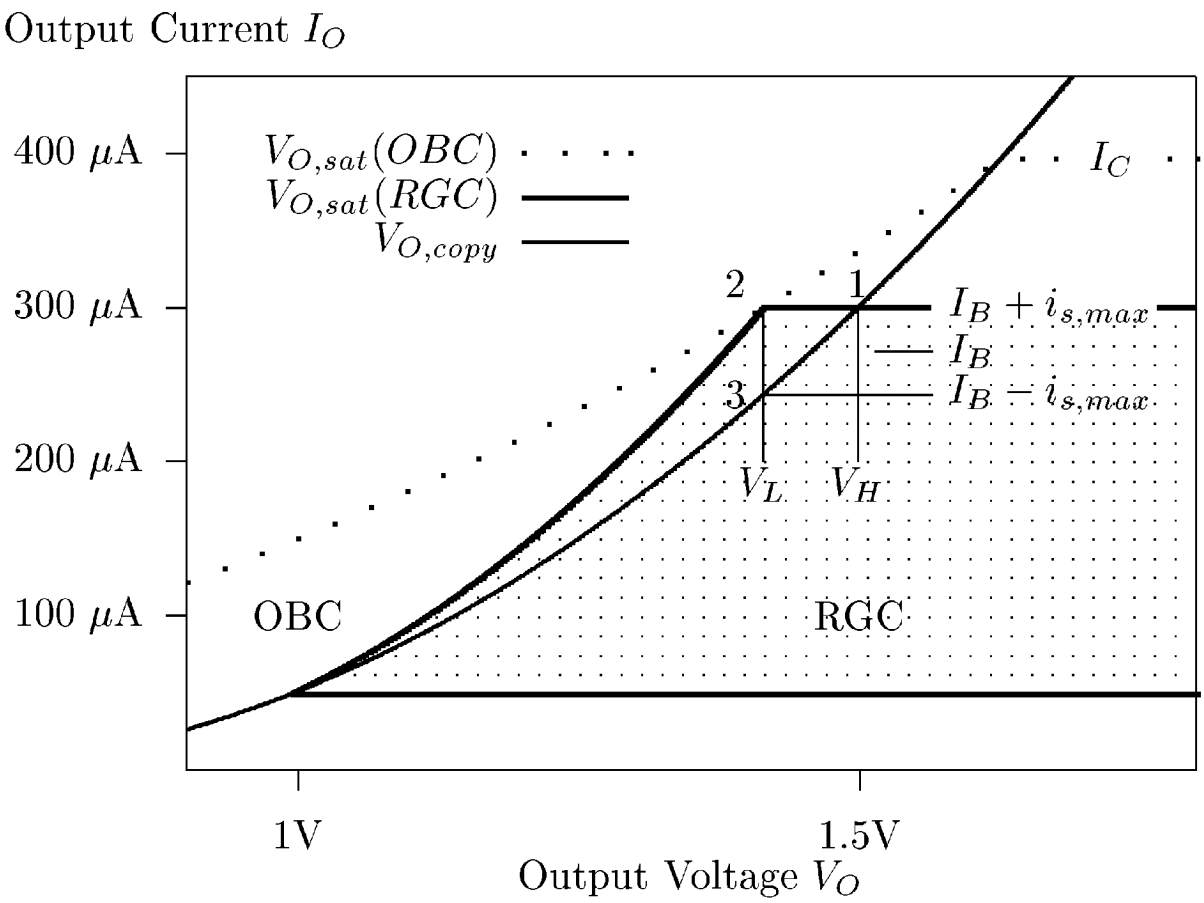


Fig. D.15: Saturation operating area of a switched current copier cell using a regulated cascode circuit (RGC) and illustration of the dynamic current range limiting situation if used as switched current copier pair.

equal output conductances of the cells, the RGC is definitely superior since its output conductance is comparable to that of the OBC even if the upper transistor is partly working in the ohmic region (See (D.28) and fig. D.6). A limited violation of the border $V_{O,sat}(RGC)$ is then tolerable. Using an IRGC doesn't enlarge the operating area in switched current copier pair applications compared to the RGC.

D.6 Conclusions

The dynamic output range and output limitations of different cascode circuits have been investigated. The cascode circuits improve the output resistance compared to the single transistor, but at the same time the non-saturation region of the output is increased and the dynamic output voltage range is reduced.
Apart from the conventional cascode circuits, we have discussed the cascode concept for an optimally biased cascode circuit, which is a simple cascode circuit with an optimal bias for the actual output current. This circuit implies the lower limit of the non-saturation region for all cascode circuits. The output resistance depends on whether a regulation feedback is applied or not.
The cascode circuits with regulation feedback have been presented as a generalized regulated cascode circuit, which is a general representation of all cascode circuits.
The dynamic output voltage range of cascode circuits with a constant reference voltage or current is determined by the maximum occurring output current. The corresponding saturation output voltage range depends on this current and is usually smaller than that of the optimally biased cascode circuit. At the maximum occurring output current the output voltage range is equal to that of the optimally biased cascode circuit. The dynamic output voltage range and the output current range for each cascode circuit have been derived.
The dynamic output range of the optimally biased cascode circuit can be approached by reference voltage or current tracking. This procedure adapts the reference voltage or current of the conventional or regulated cascode circuits respectively, so that the input transistor of the cascode circuit always operates at the limit of its saturation region. Different reference voltage and current tracking circuits for dynamic output range improvement have been proposed.
Furthermore an improved regulated cascode circuit that uses reference current tracking and that combines the large dynamic output range of the optimally biased cascode circuit with the high output resistance of the regulated cascode

circuit has been presented.
Finally the different cascode structures have been applied to switched current copiers. The additional restriction of the operating range due to the short circuit condition during the copy phase has been discussed. In signal processing applications SI memory cells are often used in cascade. A method for the discussion of their dynamic current range has been developped for a two-phase SI memory cell using two cascaded copier cells. It has been shown that a regulated cascode circuit suits best for this application.

E. SOFTWARE TOOL "PHOTOLIST"

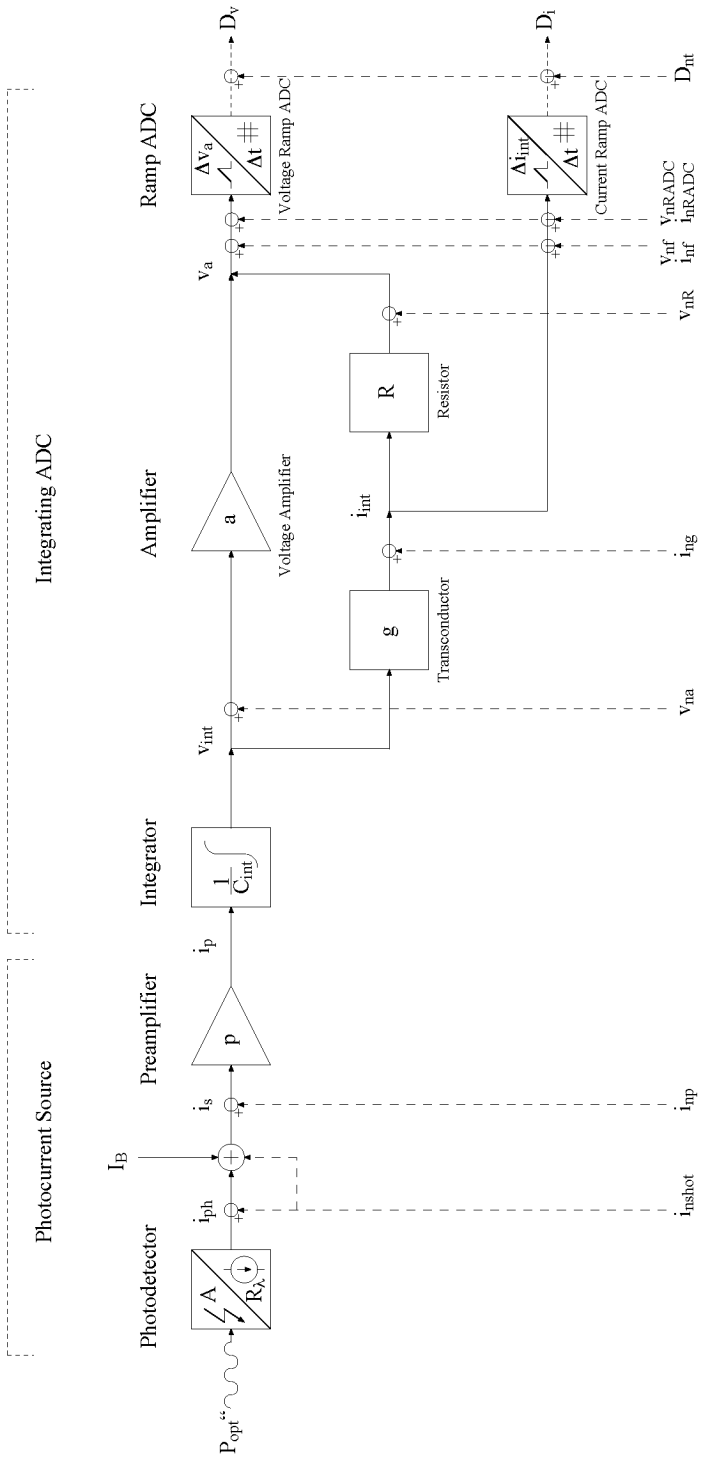
E.1 Introduction

This application is used to analyse and to design **Integrating Sampled-Data Photosensing (ISDPS)** systems. ISDPS systems are all photosensing systems that sample the incident optical power by integrating the photocurrent during the time between two successive samples and measuring the resulting value that is equivalent to the collected photogenerated charge.
A generic ISDPS model consists of a photocurrent source and an integrating analog-to-digital converter as well as a digital signal processor. The **photocurrent source** is made of a photodetector and eventually a preamplifier. The **photodetector** separates the electron-hole pairs generated by the impinging photons and transports the respective charge to the output thus generating a photocurrent that is proportional to the incident optical power. The **preamplifier** can be used to amplify the photocurrent or to provide certain output characteristics for the photocurrent source.
The **integrating analog-to-digital converter (integrating ADC)** is made of an integrator, an amplifier and a ramp analog-to-digital converter. The **integrator** collects the photogenerated charge by integrating the photocurrent and generates a ramp voltage for charge detection. The **amplifier** can be part of the integration circuit or can be used to amplify and convert the detected ramp voltage. The **ramp analog-to-digital converter (ramp ADC)** converts the analog signal to a digital sample by measuring the slope of the ramp. The digital signal processor (DSP) is used for further processing of the digital signal.

The structure of this application has four main sections. **Section I (ISDPS Model, System Definitions)** describes the ISDPS model and introduces the system parameters. **Section II (Operating Parameters, Photocurrent Source Parameters, Integrating ADC Parameters)** is the user input section for pa-

rameter definition that completely maps the specific photosensing system to the ISDPS model. **Section III (System Performance, Noise Performance)** is the output section that lists the system properties and performance tables. **Section IV (Noise Graphs, Illumination Graphs)** is the graphical output section of the system properties and performance.
The *green* fields are input fields. The *yellow* fields are output fields that are copied into the *grey* fields that are in line.

E.2 ISDPS Model



E.3 System Definitions

Operation

An ISDPS system measures the optical power density P''_{opt} of the incident light. This optical power per unit area ranges from a minimum optical power density P''_{optmin} to a maximum optical power density P''_{optmax} that can be measured in theory provided the area of illumination with the light spot size A_{opt} is centered on the photodetector of the system.
A key issue to ISDPS system operation is the timing. The maximum integration time Δt_{max} is equal to the maximum time available for a single measurement, and the minimum integration time Δt_{min} is related to the bandwidth of the system.
The influence of ambience and technology to the system is reflected in the temperature T and the transistor noise coefficient α. The latter describes the deviation of the transistor noise from the ideal transistor noise model.

Photocurrent Source

The incident light that falls on the photodetector area A has the optical power P_{opt} with the minimum optical power P_{optmin} and the maximum optical power P_{optmax} that can be measured in theory. The impinging photons generate electron-hole pairs that are separated and the charge carriers are transported to the output of the photodetector. The responsivity R_λ is the transfer coefficient from the incident optical power to the photocurrent i_{ph}. In theory a minimum photocurrent i_{phmin} and a maximum photocurrent i_{phmax} can be measured. The shot noise contribution $i_{n_{shot}}$ to the photocurrent is due to the quantum nature of the charge. During the integration time Δt the photogenerated charge q_{ph} is transported to the output, which corresponds to the number of photogenerated charge carriers N_{ph}. According to the specific photodetector capacitance C''_{ph}, which is the capacitance per unit area, a photodetector capacitance C_{ph} is present at the output of the photodetector.

A bias current I_B can be added to the photocurrent in order to have a desired signal current i_s with a determined minimum value. The shot noise contribution $i_{n_{shot}}$ is then determined by the total signal current, which is the sum of the bias

current and the photocurrent.

The preamplifier can amplify the signal current or provide certain output characteristics. The preamplifier thermal noise contribution i_{n_p} to the signal current is determined by the noise dominating elements of the preamplifier, which are typically its input transistors. The number of preamplifier noise-equivalent transistors n_p and the transconductance of preamplifier noise-equivalent transistors g_{mp} determine the noise-equivalent voltage at the input of the preamplifier and therefore at the output of the photodetector. n_p is equal to 1 for single-ended and equal to 2 for differential input stages. The noise-equivalent voltage is transformed to the preamplifier thermal noise contribution i_{n_p} by the photodetector capacitance C_{ph}. The preamplifier gain p transforms the signal current into the preamplified current i_p.

Integrating ADC

The integrator integrates the preamplified current on the integration capacitance C_{int} and the integration voltage v_{int} builds a voltage ramp for charge detection. After the integration time Δt the integration voltage drop Δv_{int} is obtained due to the collected charge q_{int}, which corresponds to the number of collected charge carriers N_{int}.

The amplifier is either a Voltage amplifier or it is a Transconductance amplifier that can be followed by a resistor.
The voltage amplifier thermal noise contribution v_{n_a} to the integration voltage is determined by the noise dominating elements of the voltage amplifier, which are typically its input transistors. The number of voltage amplifier noise-equivalent transistors n_a and the transconductance of voltage amplifier noise-equivalent transistors g_{ma} determine the noise-equivalent voltage at the input of the voltage amplifier. n_a is equal to 1 for single-ended and equal to 2 for differential input stages. The voltage amplifier amplifies the integration voltage with the voltage amplifier gain a and generates the amplified voltage v_a.
The transconductor has a number of transconductor noise-equivalent transistors n_g with the transconductance of transconductor noise-equivalent transistors g_{mg} and the transfer factor of the transconductor is given by the transconductor value g. n_g is equal to 1 for single-ended and equal to 2 for differential input stages. The transconductor transforms the integration voltage into the integration

current i_{int} that builds a current ramp. The transconductor thermal noise contribution i_{n_g} to the integration current is determined by the noise dominating elements of the transconductor, which are typically its input transistors.
The resistor with the resistor value R can be used to transform the integration current into the amplified voltage v_a. It adds the resistor thermal noise contribution v_{n_R} to the amplified voltage. The total gain of the transconductor and the resistor in series is equal to the voltage amplifier gain a and amplifies the integration voltage to the amplified voltage v_a that builds a voltage ramp.

The ramp ADC is either a Voltage ramp ADC or a Current ramp ADC. The ramp ADC determines the slope of its input signal ramp by either measuring the signal increase during a fixed measurement time or by measuring the time for a fixed signal drop. It is assumed here that the signal drop is fixed and the time for this drop is measured. Although if a fixed measurement time is given, multiple time measurements can be done during that fixed measurement time and the corresponding samples can be averaged to a final sample. This technique is equivalent to the mentioned measurement of the signal increase during a fixed measurement time.
It is further assumed that correlated double sampling is applied in order to cancel offsets generated by the signal reset between two samples. This means, that the input signal ramp is sampled at the beginning and at the end of the ramp and the difference of these two values is taken as effective sample, instead of only resetting and just taking the sample at the end of the ramp as effective sample.
The 1/f noise contribution v_{n_f} for the voltage ramp ADC or i_{n_f} for the current ramp ADC is the resulting contribution of all 1/f noise sources in the system and is determined by the 1/f voltage noise coefficient N_{vf} for the voltage ramp ADC or the 1/f current noise coefficient N_{if} for the current ramp ADC.
The ramp ADC thermal noise contribution $v_{n_{RADC}}$ for the voltage ramp ADC or $i_{n_{RADC}}$ for the current ramp ADC is determined by the ramp ADC input noise voltage $v_{nRADCeff}$ for the voltage ramp ADC or the ramp ADC input noise current $i_{nRADCeff}$ for the current ramp ADC, which are both effective noise values. In the voltage ramp ADC the amplified voltage drop Δv_a and in the current ramp ADC the integration current drop Δi_{int} is given and the integration time Δt that corresponds to this drop is measured with the timing resolution t_{res}. The integration time yields the digital output sample D_v or D_i that represents the measured optical power density of the incident light. Due to the timing resolution t_{res} of the time measurement circuit the quantization noise contribution D_{n_t} is added to the signal.

Performance

The system performance is determined for an analog bandwidth B that is the total bandwidth of the ramp ADC input path and corresponds to the minimum integration time Δt_{min} via the ramp-related bandwidth $1/\Delta t_{min}$. The noise-effective bandwidth B_n corresponds to the analog bandwidth B and represents the effective bandwidth limitation for the thermal noise contributions, which have constant spectral noise density. The measurement time is determined by the maximum integration time Δt_{max}. Minimum and maximum values are generally characterized by the subscript suffix $_{min}$ and $_{max}$.
Performance specifications are divided in two separate parts depending on whether a bias current is used or not. Specifications that refer to the use of a bias current are characterized by the subscript suffix $_b$.
Specifications generally refer to a single time measurement Δt with a fixed integration voltage drop Δv_{int}. If a fixed measurement time is given by the maximum integration time Δt_{max}, multiple time measurements with smaller integration time Δt can be done during that measurement time and their values can be averaged to a final value. Specifications that refer to this averaging technique are characterized by the subscript suffix $_{avg}$.
Noise contributions at any node can be transformed and expressed for every variable in the signal path of the system. This noise expression for a variable is called the noise-equivalent signal and is characterized by the subscript suffix $_{neq}$.

E.4 Operating Parameters

Temperature				
Temperature	T	=	300	K
CMOS Process				
Transistor noise coefficient	α	=	1	
Illumination				
Light spot size	A_{opt}	=	1.00E+06	μm^2
Timing				
Minimum integration time	Δt_{min}	=	1	µs
Maximum integration time	Δt_{max}	=	1	ms
Constants				
Pi	pi	=	3.14E+00	
Elementary charge	e	=	1.60E-19	C
Boltzmann constant	k	=	1.38E-23	J/K

E.5 Photocurrent Source Parameters

Photodetector				
Photodetector area	A	=	10000	μm^2
Specific photodetector capacitance	C_{ph}''	=	1	$fF/\mu m^2$
Photodetector capacitance	C_{ph}	=	10	pF
Responsivity	R_λ	=	0.1	A/W
Bias				
Bias current	I_B	=	1	nA
Preamplifier				
Preamplifier gain	p	=	1	
Number of preamplifier noise-equivalent transistors	n_p	=	2	
Transconductance of preamplifier noise-equivalent transistors	g_{mp}	=	0.1	mS

E.6 Integrating ADC Parameters

Integrator				
Integration capacitance	C_{int}	=	1	pF
Amplifier				
Voltage(0) or **T**ransconductance(1) amplifier:			0	
V: Voltage amplifier gain	a	=	1	
V: Number of voltage amplifier noise-equivalent transistors	n_a	=	2	
V: Transconductance of voltage amplifier noise-equivalent transistors	g_{ma}	=	0.1	mS
T: Transconductor value	g	=	1	mS
T: Number of transconductor noise-equivalent transistors	n_g	=	1	
T: Transconductance of transconductor noise-equivalent transistors	g_{mg}	=	1	mS
T: Resistor value	R	=	1	kΩ
Ramp ADC				
Timing resolution	t_{res}	=	100	ns
Single(1) or double(2) sampling:			2	
Voltage(0) or **C**urrent(1) ramp ADC:			0	
V: 1/f noise voltage coefficient	N_{vf}	=	1	$x10^{-10}$ V^2
V: Ramp ADC input noise voltage	$v_{nRADCeff}$	=	100	μV
V: Amplified voltage drop	Δv_a	=	1	V
C: 1/f noise current coefficient	N_{if}	=	1	$x10^{-16}$ A^2
C: Ramp ADC input noise current	$i_{nRADCeff}$	=	100	nA
C: Integration current drop	Δi_{int}	=	1000	μA

E.7 System Performance

Speed Requirements						
Analog bandwidth	B	=	4	MHz		
Speed Properties						
Ramp-related bandwidth	$1/\Delta t_{min}$	=	1	MHz		
Noise-effective bandwidth	B_n	=	6.283185	MHz		
Signal Properties						
Photogenerated charge	q_{ph}	=	1	pC		
Number of photogenerated charge carriers	N_{ph}	=	6250000			
Collected charge	q_{int}	=	1	pC		
Number of collected charge carriers	N_{int}	=	6250000			
Integration voltage drop	Δv_{int}	=	1	V		
Full-scale Signal Properties					**With Bias Current:**	
Maximum optical power density	P_{optmax}"	=	1000	W/m^2	999	W/m^2
Maximum optical power	P_{optmax}	=	10000	nW	9990	nW
Maximum photocurrent	i_{phmax}	=	1000	nA	999	nA
Minimum-scale Signal Properties						
Minimum optical power density	P_{optmin}"	=	1000	mW/m^2	0	mW/m^2
Minimum optical power	P_{optmin}	=	10000	pW	0	pW
Minimum photocurrent	i_{phmin}	=	1000	pA	0	pA

E.8 Noise Performance

		System		Illumination	Preampl
		Overall Performance	Range Limitations	Shot Noise	Thermal N
Noise:	Noise term			i_{nshot}	i_{np}
	Noise spectral density			0.017888544 pA/SQRT(nA*Hz)	0.001617112
	Effective noise			0.4 pA/nA	7469.119191
Without Bias Current:					
Photocurrent:	i_{phmax}	1000 nA	1000 nA	1000 nA	1000
	i_{phmin}	1000 pA	1000 pA	1000 pA	1000
	$i_{phneq}(I_{ph})$			0.4 pA/nA	0.645134246
	$i_{phneq}(I_{phmax})$	40832.19039 pA		400 pA	645.1342455
	$i_{phneq}(I_{phmin})$	0.777272944 pA		0.4 pA	0.645134246
Number of Photogenerated Charge Carriers:	$N_{phavg}(I_{ph})$	6250000 /nA	6250000 /nA	6250000 /nA	6250000
	$N_{phavg}(I_{phmax})$	6250000000	6250000000	6250000000	6250000000
	N_{ph}	6250000	6250000	6250000	6250000
	$N_{phneq}(I_{ph})$			2500	4032
	$N_{phneq}(I_{phmax})$	255201		2500	4032
	$N_{phneq}(I_{phmin})$	4858		2500	4032
Integration Voltage Drop:	$\Delta v_{intavg}(I_{ph})$	1 V/nA	1 V/nA	1 V/nA	1
	$\Delta v_{intavg}(I_{phmax})$	1000 V	1000 V	1000 V	1000
	Δv_{int}	1 V	1 V	1 V	1
	$v_{intneq}(I_{ph})$			0.4 mV	0.645134246
	$v_{intneq}(I_{phmax})$	40.83219039 mV		0.4 mV	0.645134246
	$v_{intneq}(I_{phmin})$	0.777272944 mV		0.4 mV	0.645134246
Signal-to-Noise Ratio:	$SNR(I_{ph})$			2500	1550
	$SNR(I_{phmin})$	1287		2500	1550
		62 dB		68 dB	64
	$SNR(I_{phmax})$	24		2500	1550
		28 dB		68 dB	64
	$SNR_{avg}(I_{ph})$			2500 /SQRT(nA)	1550
	$SNR_{avg}(I_{phmax})$	774		79057	49017
		58 dB		98 dB	94
Dynamic Range:	DR	1000	1000	1000	1000
		60 dB	60 dB	60 dB	60

Fig. E.1: Performance table listing the noise terms and the characteristic, limiting and noise-equivalent values of the photocurrent, the photogenerated charge carriers, the integration voltage drop, the signal-to-noise ratio and the dynamic range. The values are listed for the different noise contributions separately as well as for the whole system. This part represents the results without bias current.

		System		Illumination	Preampl
		Overall Performance	Range Limitations	Shot Noise	Thermal N
Noise:	Noise term			I_{nshot}	I_{np}
	Noise spectral density			0.017888544 pA/SQRT(nA*Hz)	0.001617112
	Effective noise			0.4 pA/nA	7469.119191
With Bias Current:					
Photocurrent:	i_{phbmax}	999 nA	999 nA	999 nA	999
	i_{phbmin}	0 pA	0 pA	0 pA	0
	$I_{phbneq}(I_{phbmax})$	40832.19039 pA		400 pA	645.1342455
	$I_{phbneq}(I_{phbmin})$	0.777272944 pA		0.4 pA	0.645134246
Number of Photogenerated Charge Carriers:	$N_{phbavg}(I_{phbmax})$	6243750000	6243750000	6243750000	6243750000
	$N_{phbavg}(I_{phbmin})$	0	0	0	0
	$N_{phb}(I_{phbmax})$	6243750	6243750	6243750	6243750
	$N_{phb}(I_{phbmin})$	0	0	0	0
	$N_{phbneq}(I_{phbmax})$	255201		2500	4032
	$N_{phbneq}(I_{phbmin})$	4858		2500	4032
Integration Voltage Drop:	$\Delta V_{intbavg}(I_{phbmax})$	999 V	999 V	999 V	999
	$\Delta V_{intbavg}(I_{phbmin})$	0 V	0 V	0 V	0
	$\Delta V_{intb}(I_{phbmax})$	0.999 V	0.999 V	0.999 V	0.999
	$\Delta V_{intb}(I_{phbmin})$	0 V	0 V	0 V	0
	$V_{intbneq}(I_{phbmax})$	40.83219039 mV		0.4 mV	0.645134246
	$V_{intbneq}(I_{phbmin})$	0.777272944 mV		0.4 mV	0.645134246
Signal-to-Noise Ratio:	$SNR_b(I_{phbmin})$	0		0	0
		#NUM! dB		#NUM! dB	#NUM!
	$SNR_b(I_{phbmax})$	24		2498	1549
		28 dB		68 dB	64
	$SNR_{bavg}(I_{phbmin})$	0		0	0
		#NUM! dB		#NUM! dB	#NUM!
	$SNR_{bavg}(I_{phbmax})$	774		78978	48968
		58 dB		98 dB	94
Dynamic Range:	DR_b	1285263	10000000000	2497500	1548515
		122 dB	200 dB	128 dB	124

Fig. E.2: Performance table listing the noise terms and the characteristic, limiting and noise-equivalent values of the photocurrent, the photogenerated charge carriers, the integration voltage drop, the signal-to-noise ratio and the dynamic range. The values are listed for the different noise contributions separately as well as for the whole system. This part represents the results with bias current.

E.9 Noise Graphs

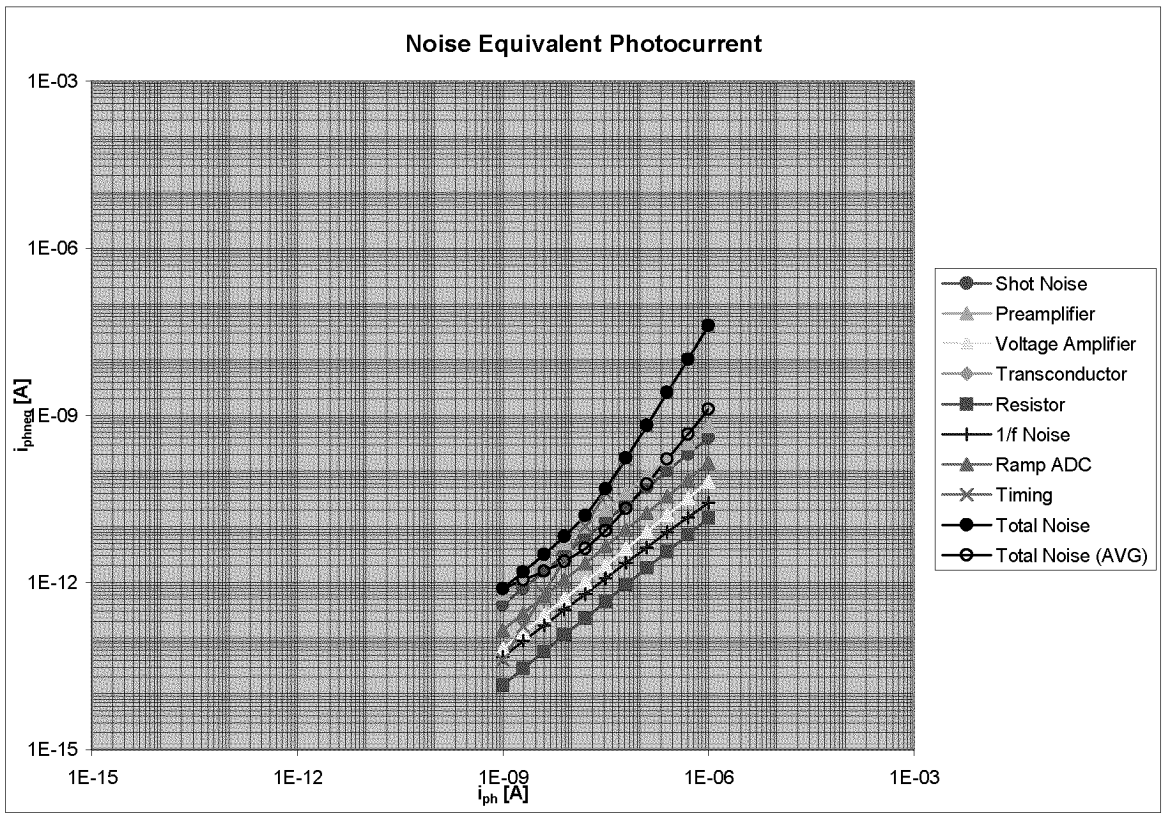


Fig. E.3: Noise-equivalent photocurrent versus photocurrent for the different noise contributions separately as well as for the whole system. This part represents the results without bias current.

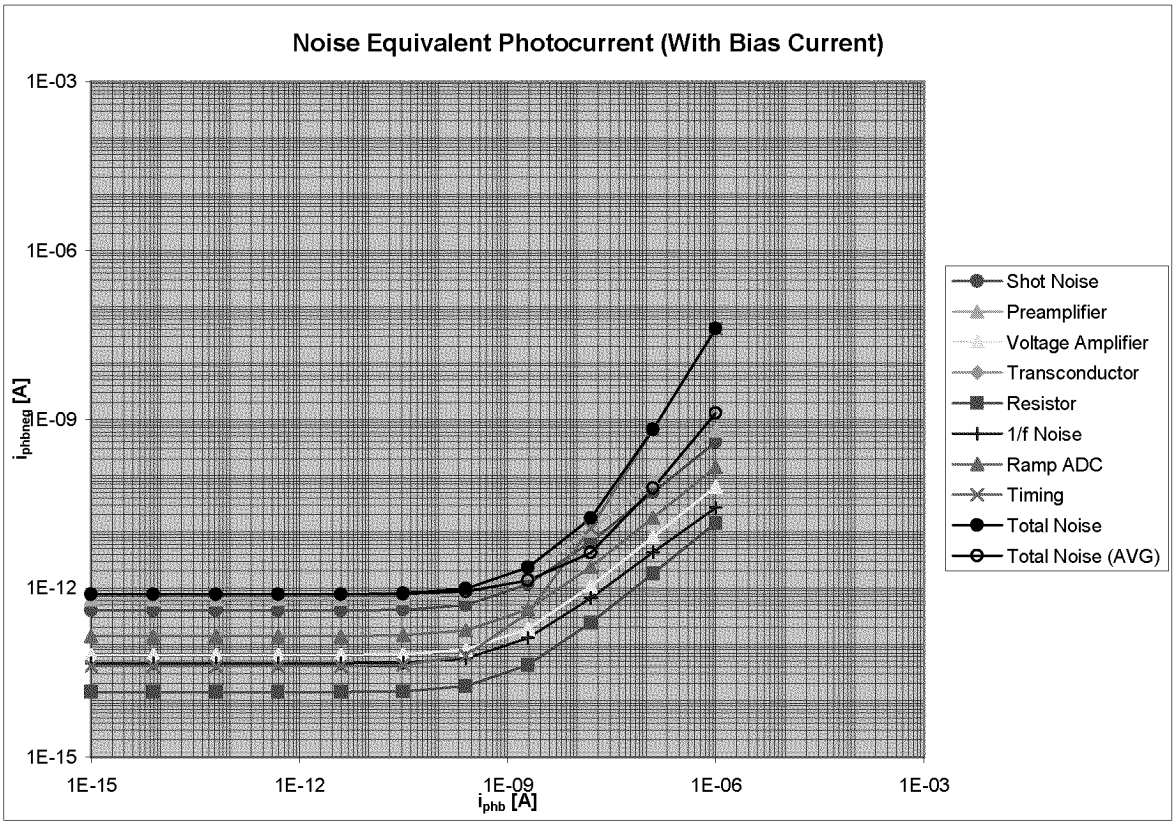


Fig. E.4: Noise-equivalent photocurrent versus photocurrent for the different noise contributions separately as well as for the whole system. This part represents the results with bias current.

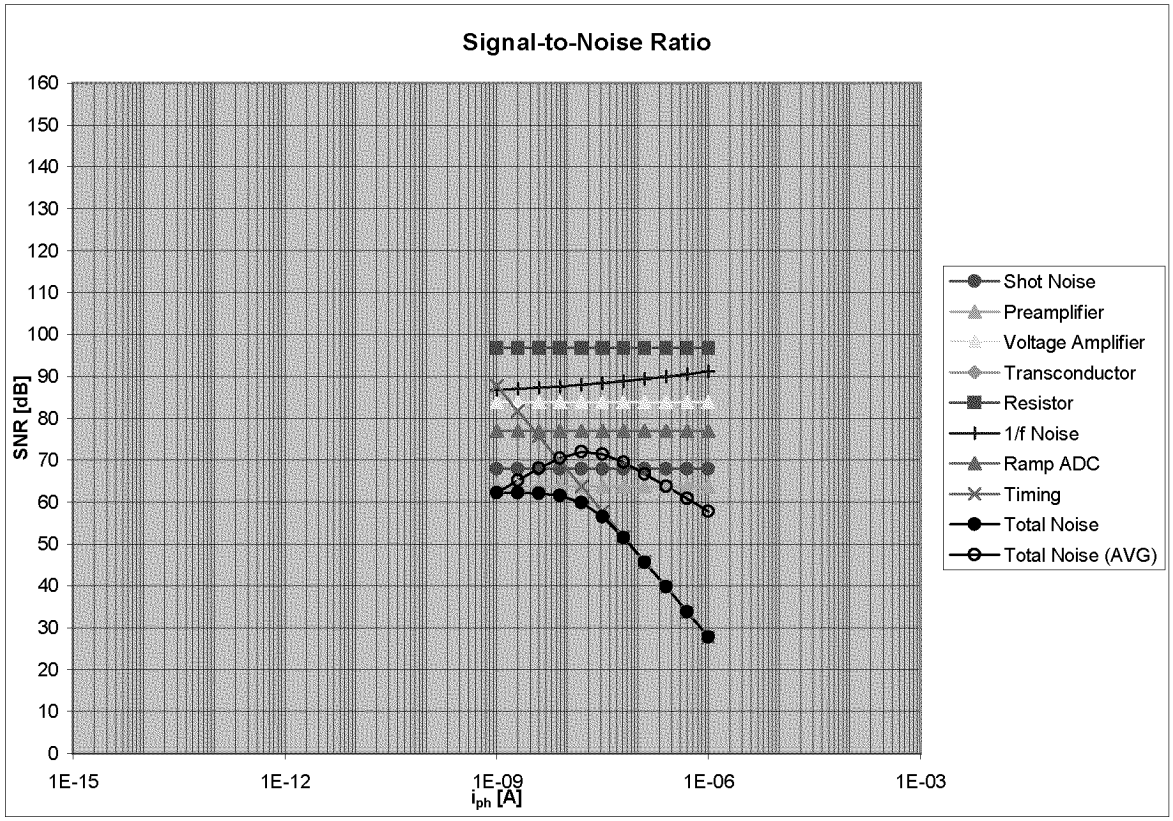


Fig. E.5: Signal-to-noise ratio versus photocurrent for the different noise contributions separately as well as for the whole system. This part represents the results without bias current.

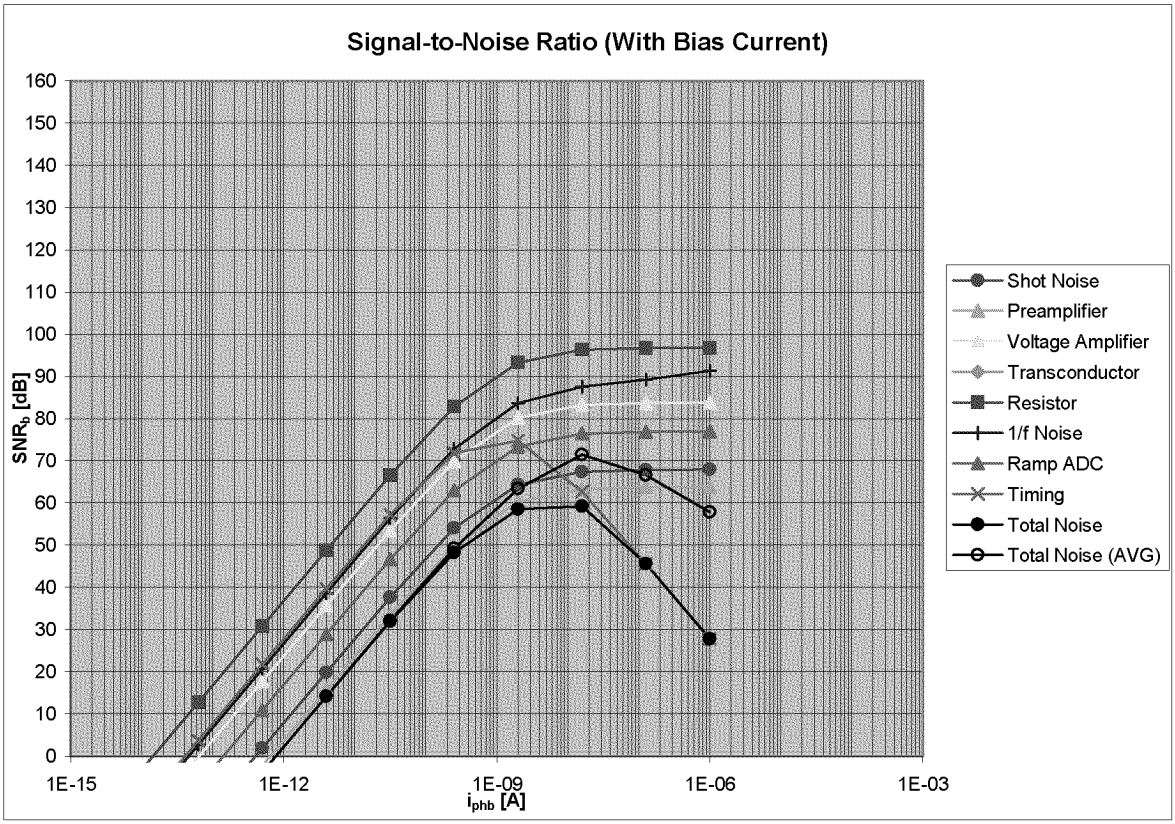


Fig. E.6: Signal-to-noise ratio versus photocurrent for the different noise contributions separately as well as for the whole system. This part represents the results with bias current.

E.10 Illumination Graphs

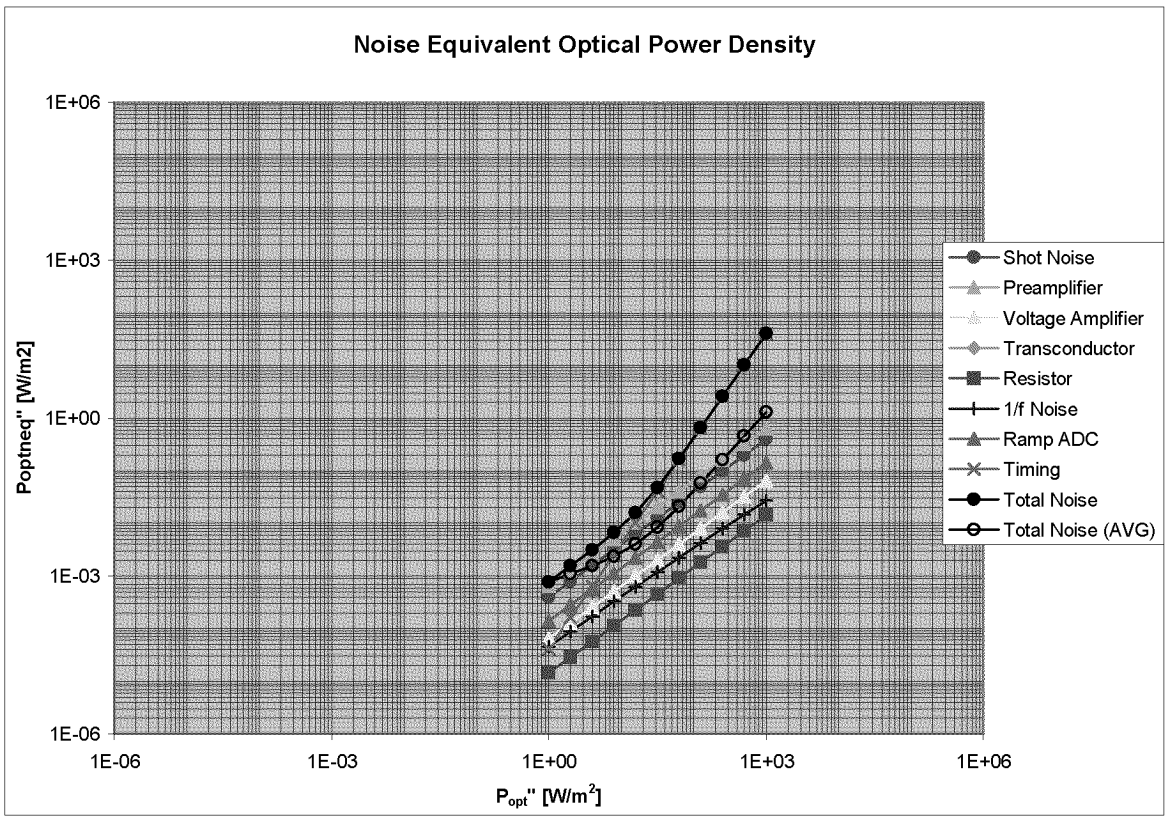


Fig. E.7: Noise-equivalent optical power density versus optical power density for the different noise contributions separately as well as for the whole system. This part represents the results without bias current.

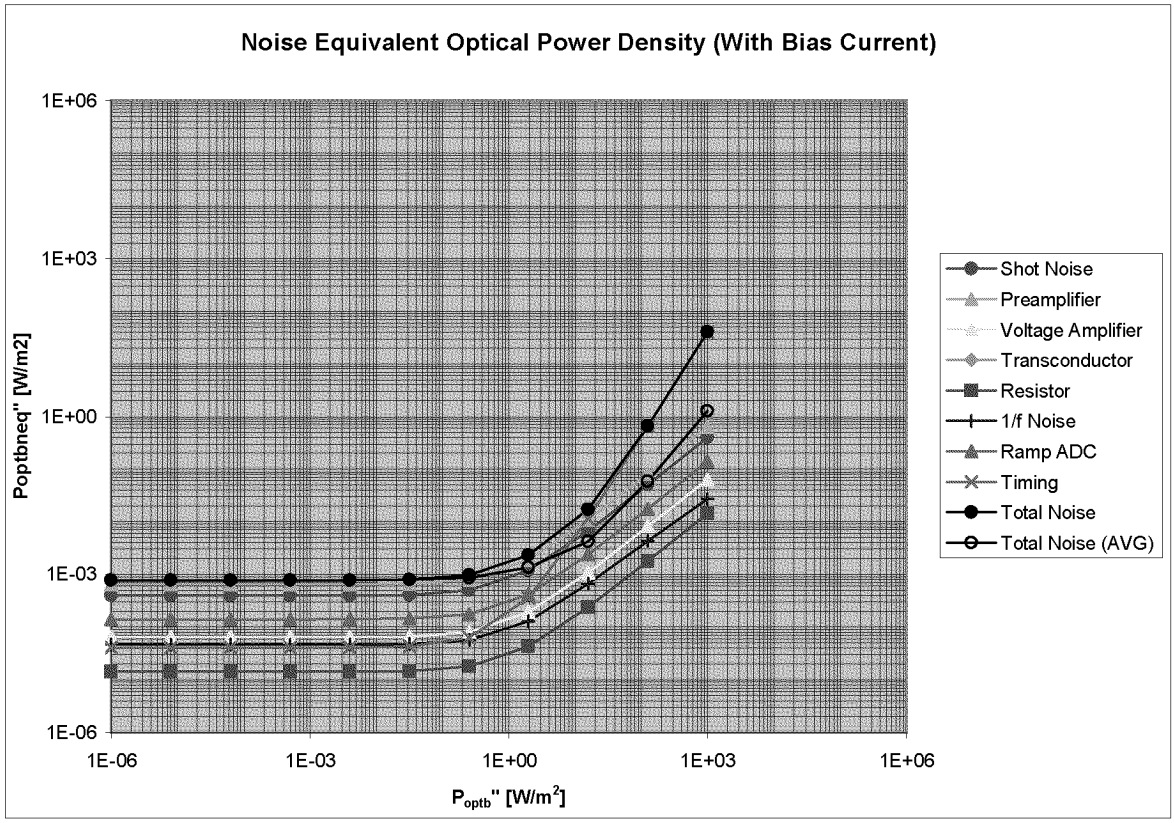


Fig. E.8: Noise-equivalent optical power density versus optical power density for the different noise contributions separately as well as for the whole system. This part represents the results with bias current.

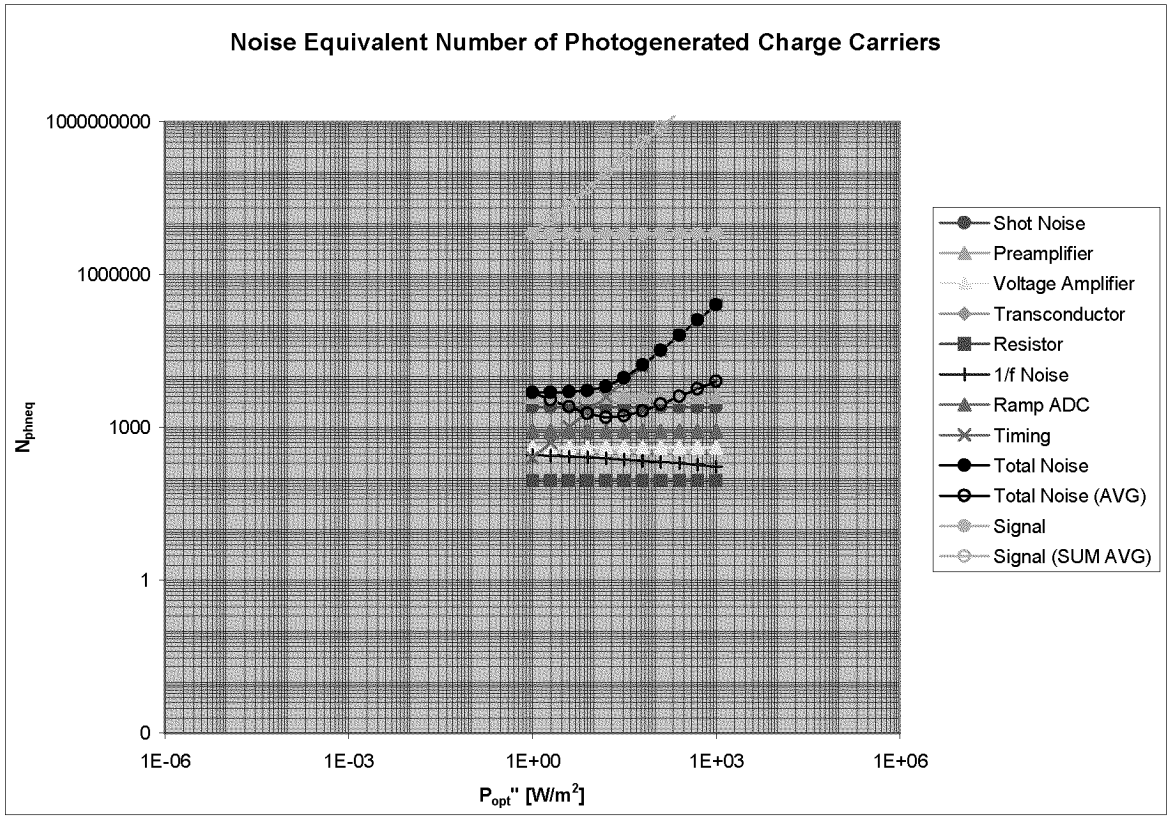


Fig. E.9: Noise-equivalent number of photogenerated charge carriers versus optical power density for the different noise contributions separately as well as for the whole system. This part represents the results without bias current.

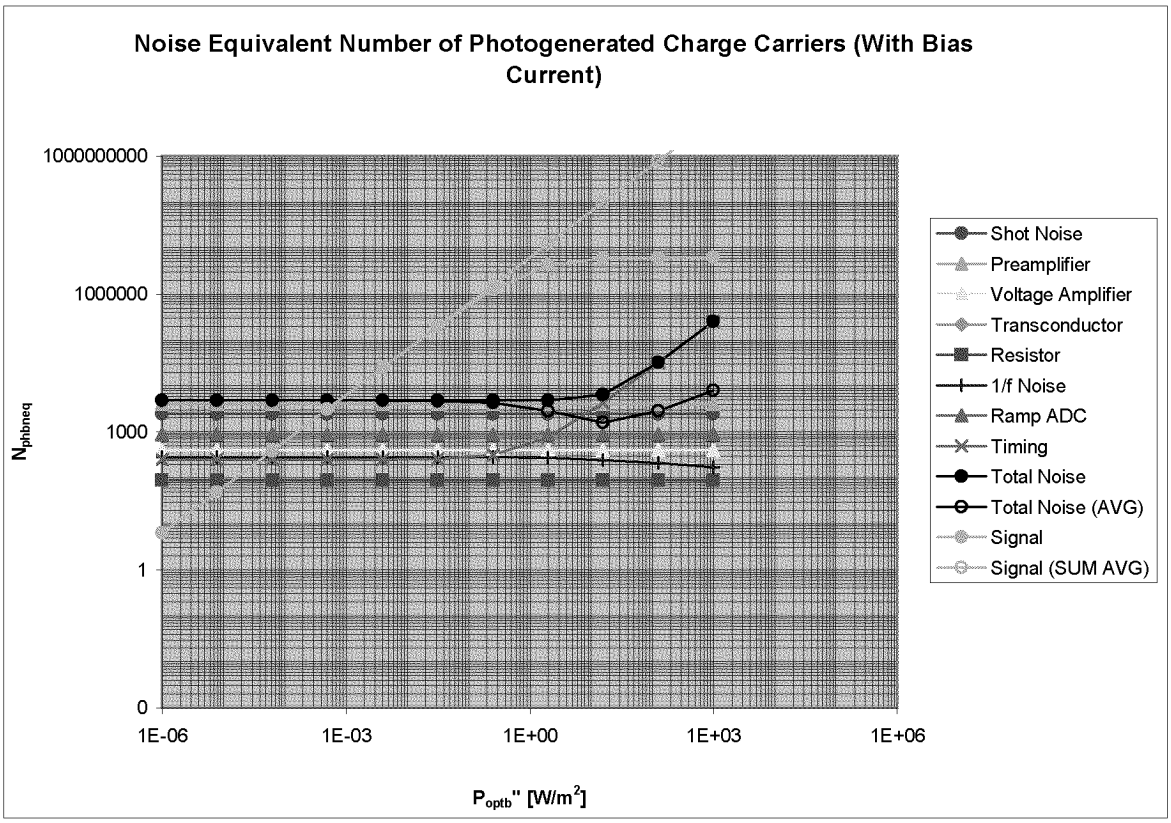


Fig. E.10: Noise-equivalent number of photogenerated charge carriers versus optical power density for the different noise contributions separately as well as for the whole system. This part represents the results with bias current.

F. CHIP LAYOUTS

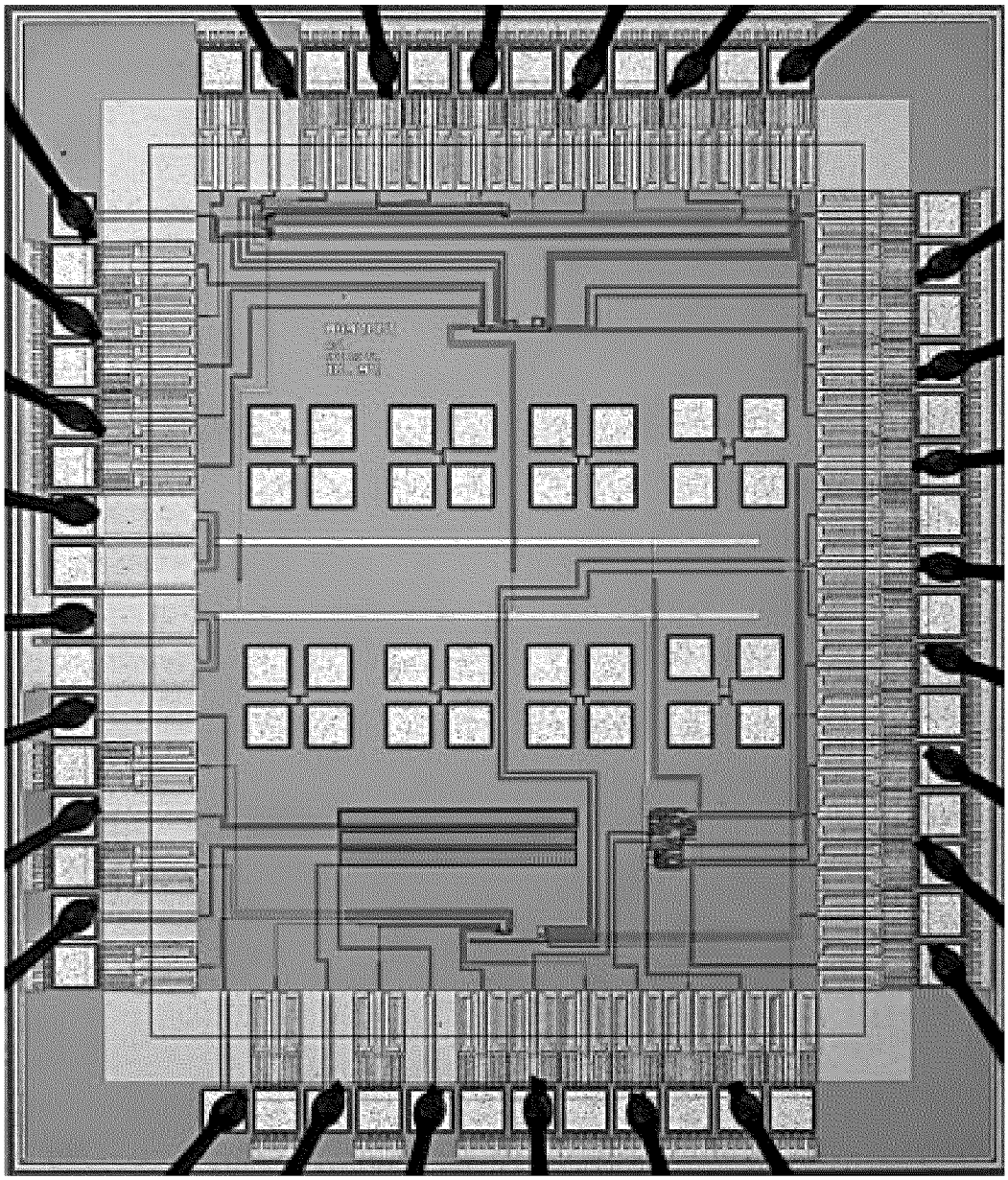


Fig. F.1: Chip photograph of “Simple Test Structures”.

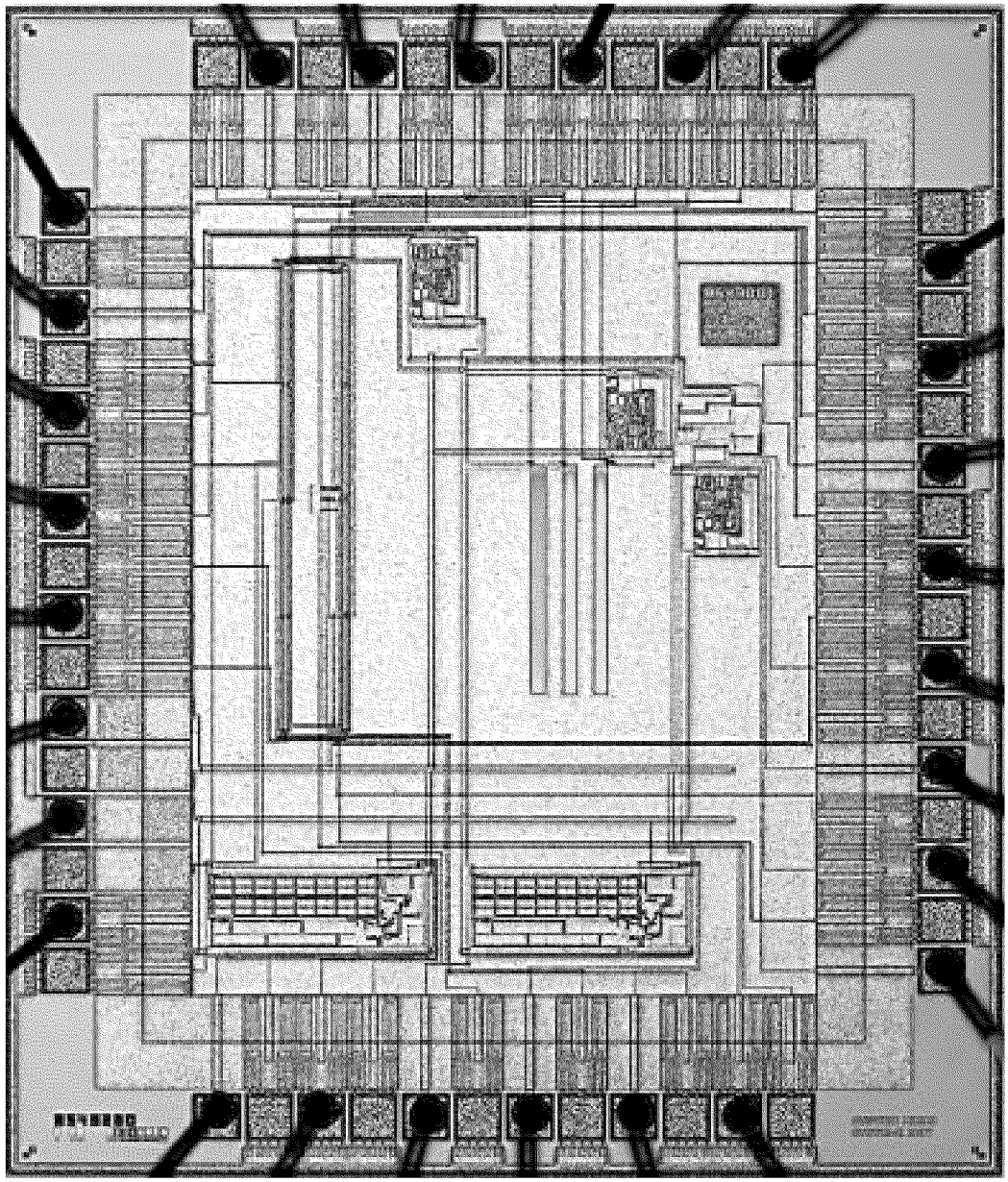


Fig. F.2: Chip photograph of “Advanced Test Structures”.

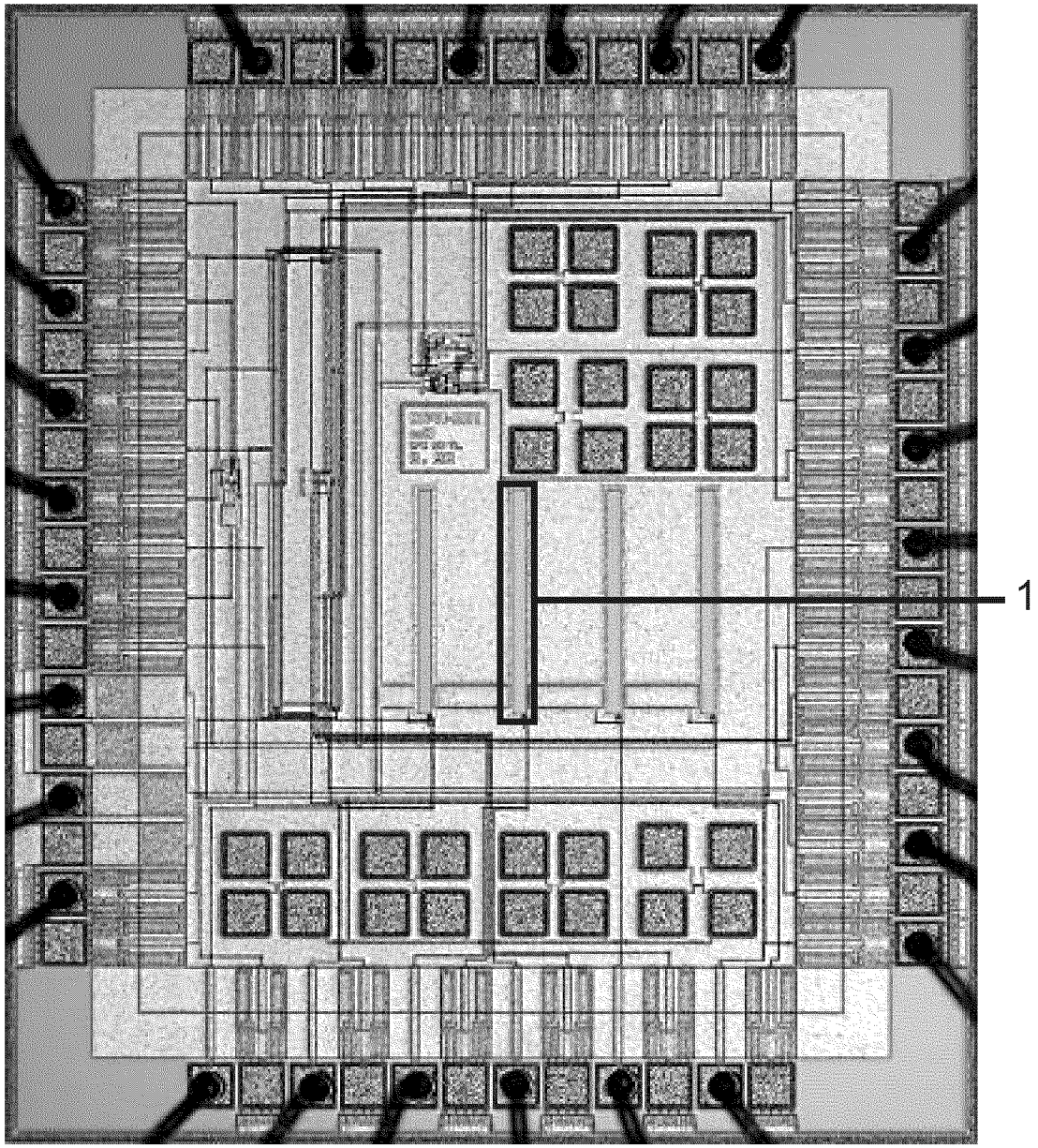


Fig. F.3: Chip photograph of “Photodetectors”. (1) PD.

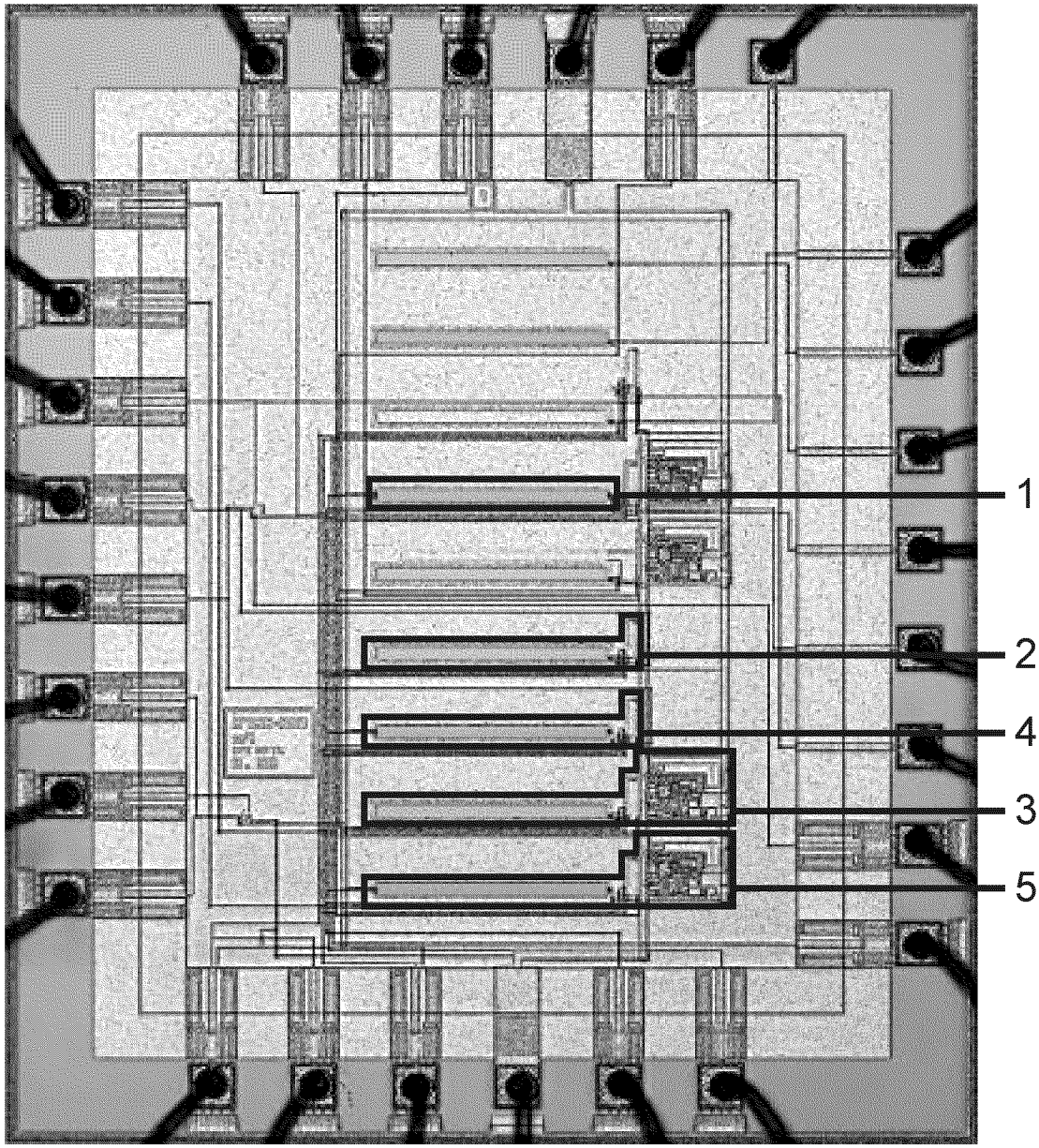


Fig. F.4: Chip photograph of “Single Detector Photosensing Architectures”. (1) PG, (2) PD+PI, (3) PD+AI, (4) PG+PI, (5) PG+AI.

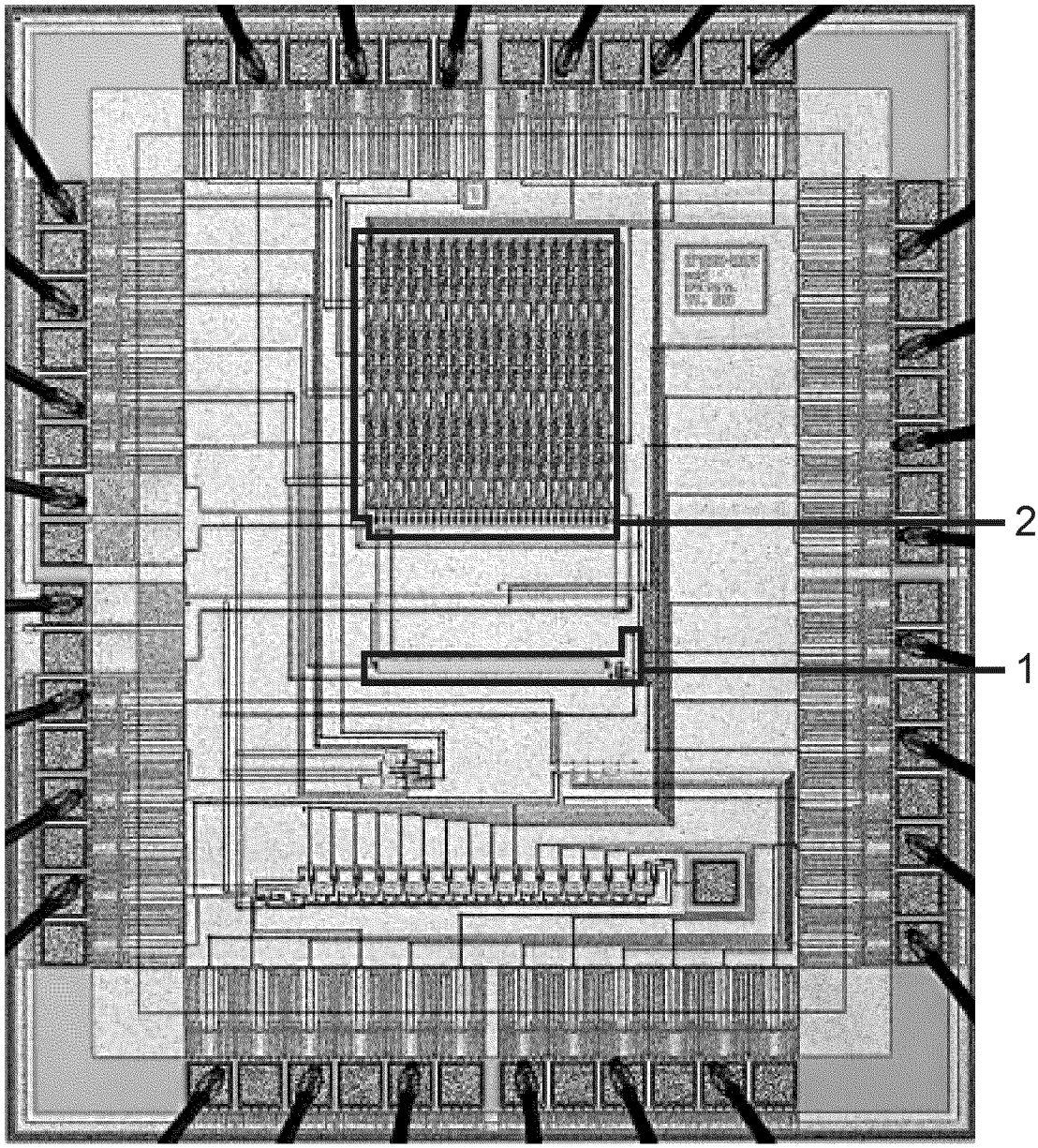


Fig. F.5: Chip photograph of "Advanced Photodetectors". (1) CPG+PI, (2) SSPG+SPI.

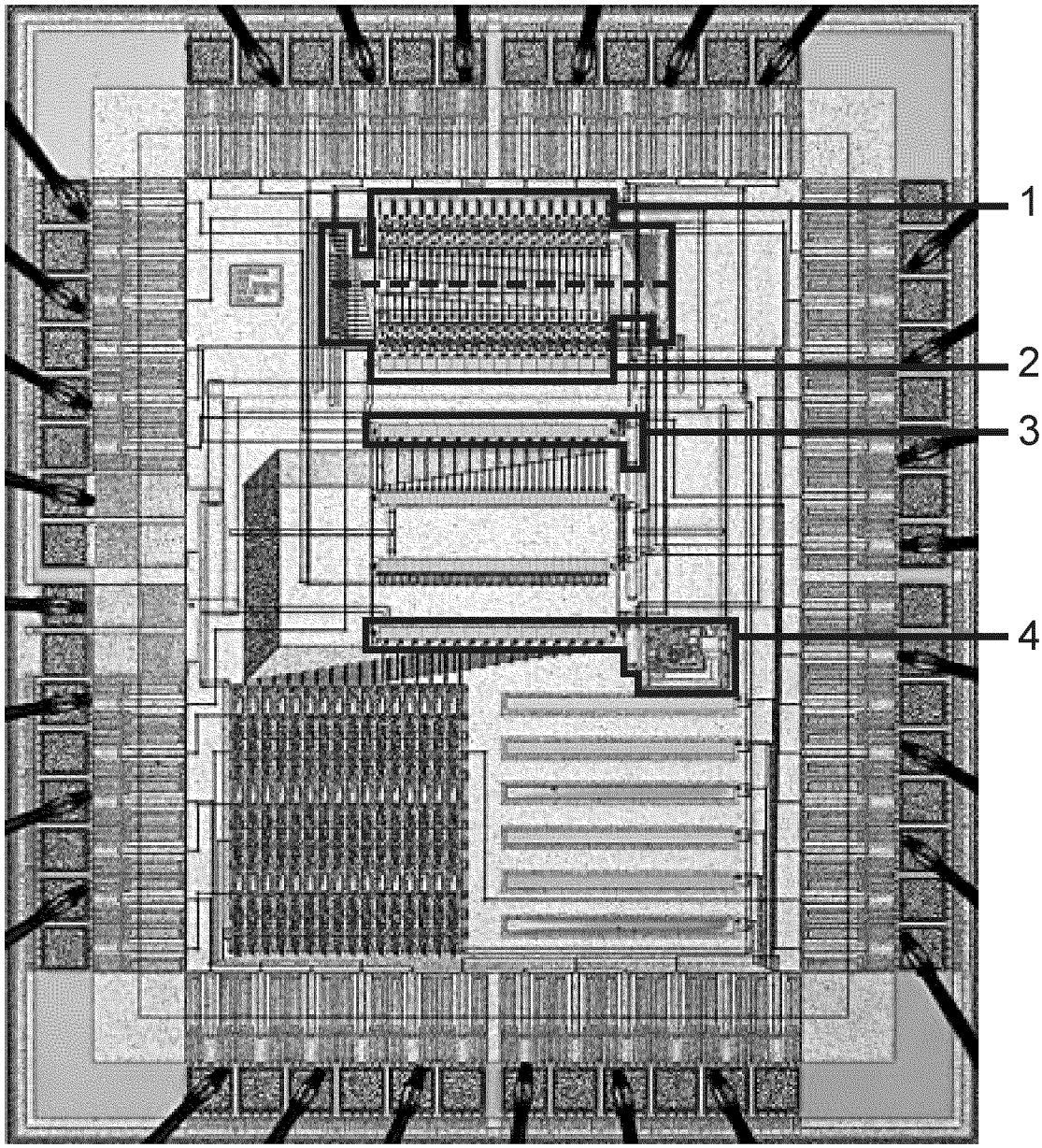


Fig. F.6: Chip photograph of "Array Photosensing Architectures". (1) SAPS, (2) PAPS, (3) CCD+PI (typical layout), (4) CCD+AI (typical layout).

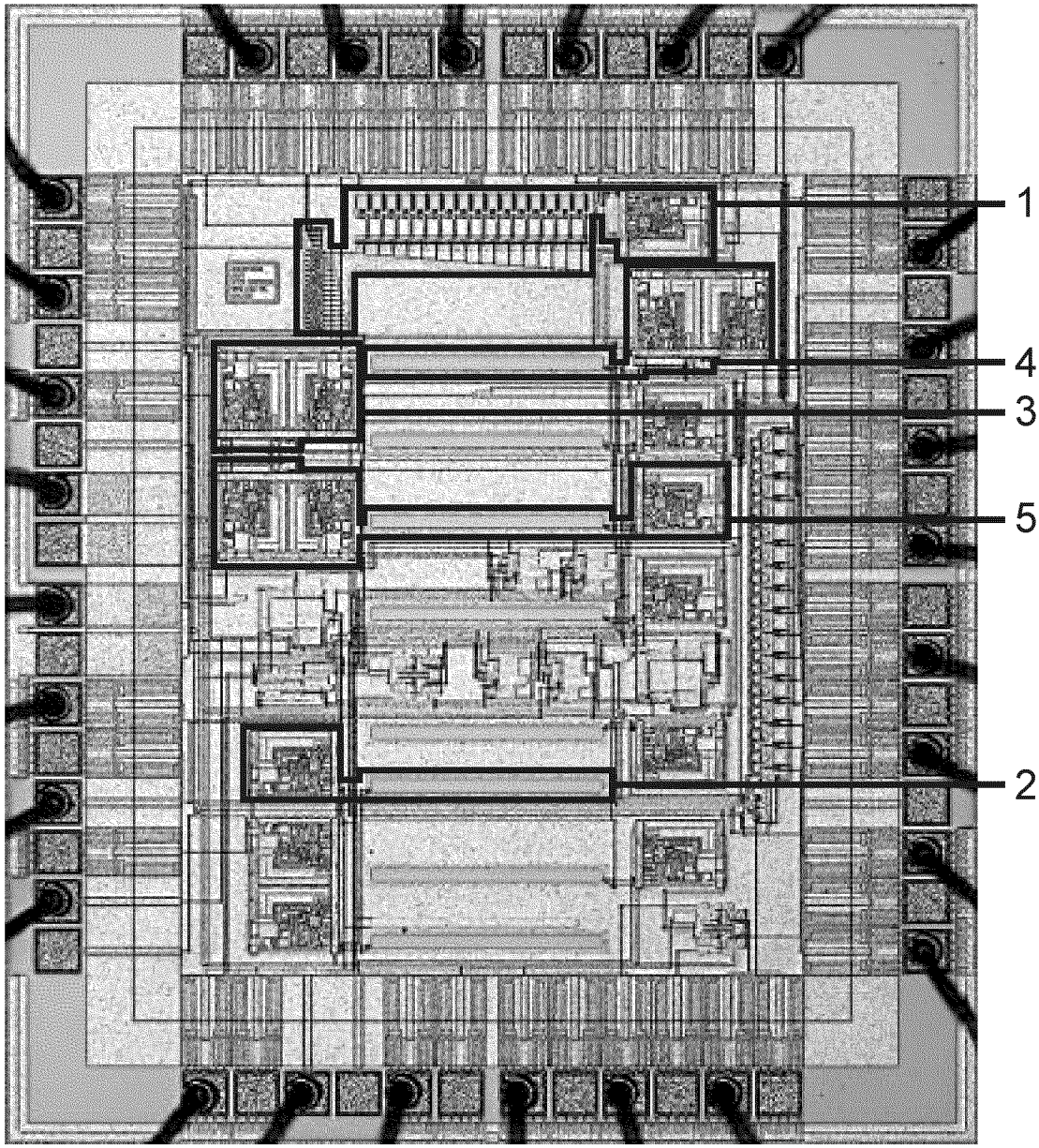


Fig. F.7: Chip photograph of "Advanced Architectures for Photosensing". (1) PDA+AI, (2) PDCS, (3) CMTI, (4) PD+CMTI, (5) PDCS+CMTI.

	A_{chip} [mm^2]
PD	0.027
PG	0.021
PD+PI	0.029
PD+AI	0.057
PG+PI	0.024
PG+AI	0.052
CPG+PI	0.024
SSPG+SPI	0.356
SAPS	0.143
PAPS	0.138
(CCD+PI)	(0.024)
(CCD+AI)	(0.052)
PDA+AI	0.113
PDCS	0.055
CMTI	0.061
PD+CMTI	0.088
PDCS+CMTI	0.116
OPAMP	0.028
PI	0.003
AI	0.031

Tab. F.1: Chip areas of realized structures.

G. ISDPS PARAMETERS FOR THE REALIZED ARCHITECTURES

Parameters correspond to a single pixel or array element in array architectures.

T	$300\,\mathrm{K}$
α	1
A_{opt}	$1 \cdot 10^{-6}\,\mathrm{m}^2$
C''_{ph}	$\frac{C_{ph}}{A}$
I_B	variable ($i_{phmin} \leq I_B \leq i_{phmax}$)
t_{res}	$1\,\mathrm{ns}$

Tab. G.1: Common parameters for the realized architectures.

	η[i] [%]	R_λ [A/W]	R_A[ii] [Am^2/W]	A [m^2]	v_p[iii] [V]	v_n[iii] [V]	C_{ph}[iv] [fF]	N_{ph}[ii]
PD+PI	70	0.35	$52 \cdot 10^{-10}$	$150 \cdot 10^{-10}$	1	3.7	6600	$50 \cdot 10^6$
PD+AI	70	0.35	$52 \cdot 10^{-10}$	$150 \cdot 10^{-10}$	1	1	11400	$4.4 \cdot 10^6$
PG+PI	30	0.15	$22 \cdot 10^{-10}$	$150 \cdot 10^{-10}$	0	3.7	710	$5.4 \cdot 10^6$
PG+AI	30	0.15	$22 \cdot 10^{-10}$	$150 \cdot 10^{-10}$	0	1	800	$4.4 \cdot 10^6$
SAPS	70	0.35	$3.2 \cdot 10^{-10}$	$9.4 \cdot 10^{-10}$	1	3.7	440	$3.4 \cdot 10^6$
PDA+AI	70	0.35	$3.2 \cdot 10^{-10}$	$9.4 \cdot 10^{-10}$	1	1	1600	$4.4 \cdot 10^6$
PAPS	30	0.15	$1.4 \cdot 10^{-10}$	$9.4 \cdot 10^{-10}$	0	3.7	75	$0.57 \cdot 10^6$
PD+CMTI	70	0.35	$52 \cdot 10^{-10}$	$150 \cdot 10^{-10}$	0.5	1.5	8500	$4.1 \cdot 10^6$
PDCS+CMTI	70	0.35	$52 \cdot 10^{-10}$	$150 \cdot 10^{-10}$	0.5	0.5	11400	$0.42 \cdot 10^6$

Tab. G.2: Photodetector parameters for the realized architectures.

	n_p[iv]	g_{mp}[iv] [μS]	p
PD+PI	0	-	1
PD+AI	2	50	1
PG+PI	0	-	1
PG+AI	2	50	1
SAPS	0	-	1
PDA+AI	2	50	1
PAPS	0	-	1
PD+CMTI	0	-	1
PDCS+CMTI	2	50	1

Tab. G.3: Preamplifier parameters for the realized architectures.

[i] Section 2.3, $\lambda = 612$ nm
[ii] Section 3.2
[iii] Potentials at the anode (p) and at the cathode (n) of the sensing diode
[iv] Section 3.4

	C_{int} [fF]	v_{int1} [i] [V]	v_{int2} [i] [V]	Δv_{int} [ii] [V]
PD+PI	6600	4.3	3.1	1.2
PD+AI	710	1.5	2.5	1
PG+PI	710	4.3	3.1	1.2
PG+AI	710	1.5	2.5	1
SAPS	440	4.3	3.1	1.2
PDA+AI	710	1.5	2.5	1
PAPS	75	4.3	3.1	1.2
PD+CMTI	8500	1.4	1.3	0.077
PDCS+CMTI	880	1.4	1.3	0.077

Tab. G.4: Integrator parameters for the realized architectures.

	n_a [iii]	g_{ma} [iii] [μS]	a	n_g [iii]	g_{mg} [iii] [mS]	g [mS]	R [kΩ]
PD+PI	1	18	0.82	(1)	(1)	(1)	(0.82)
PD+AI	2	50	1	(1)	(1)	(1)	(1)
PG+PI	1	18	0.82	(1)	(1)	(1)	(0.82)
PG+AI	2	50	1	(1)	(1)	(1)	(1)
SAPS	1	14	0.82	(1)	(1)	(1)	(0.82)
PDA+AI	2	50	1	(1)	(1)	(1)	(1)
PAPS	1	14	0.82	(1)	(1)	(1)	(0.82)
PD+CMTI	(1)	(1300)	(13)	1	1.3	1.3	10
PDCS+CMTI	(1)	(1300)	(13)	1	1.3	1.3	10

Tab. G.5: Amplifier parameters for the realized architectures.

[i] Voltages referring to the first (1) and second (2) reference level of the window comparator of the ramp ADC

[ii] Section 3.2

[iii] Section 3.4

	v_{a1} [i] [V]	v_{a2} [i] [V]	Δv_a [ii] [V]	N_{vf} [iii] [V^2]	$v_{nRADCeff}$ [iii] [μV]
PD+PI	2.5	1.5	1	$0.69 \cdot 10^{-10}$	100
PD+AI	1.5	2.5	1	$6.4 \cdot 10^{-10}$	100
PG+PI	2.5	1.5	1	$0.69 \cdot 10^{-10}$	100
PG+AI	1.5	2.5	1	$0.12 \cdot 10^{-10}$	100
SAPS	3.6	2.6	1	$0.69 \cdot 10^{-10}$	100
PDA+AI	1.5	2.5	1	$0.25 \cdot 10^{-10}$	100
PAPS	3.6	2.6	1	$0.69 \cdot 10^{-10}$	100
PD+CMTI	2	3	1	$370 \cdot 10^{-10}$	100
PDCS+CMTI	2	3	1	$1000 \cdot 10^{-10}$	100

Tab. G.6: Ramp ADC parameters for the realized architectures.

	C_{virt} [ii] [fF]	T_A [ii] [Vm^2/Ws]
PD+PI	8000	650
PD+AI	710	7300
PG+PI	870	2500
PG+AI	710	3100
SAPS	540	590
PDA+AI	710	460
PAPS	91	1500
PD+CMTI	650	7900
PDCS+CMTI	68	76000

Tab. G.7: Derived parameters for the realized architectures.

[i] Voltages referring to the first (1) and second (2) reference level of the window comparator of the ramp ADC

[ii] Section 3.2

[iii] Estimated values

	P''_{optmin} [i] [μW/m^2]	P''_{optmax} [i] [W/m^2]	i_{phmin} [i] [fA]	i_{phmax} [i] [nA]	Δt_{max} [i] [s]	Δt_{min} [i] [μs]	B_{max} [ii] [MHz]
PD+PI	310	77	1600	400	5	20	0.2
PD+AI	27	20	140	110	5	6.7	0.6
PG+PI	77	19	170	43	5	20	0.2
PG+AI	63	390	140	890	5	0.8	5
SAPS	160	220	54	74	10	7.3	0.55
PDA+AI	4400	1700	1400	550	0.5	1.3	3
PAPS	650	89	91	13	1	7.3	0.55
PD+CMTI	42	32	220	160	3	4	1
PDCS+CMTI	26	3.3	140	17	0.5	4	1

Tab. G.8: Limits for the realized architectures.

[i] Section 3.2

[ii] Maximum analog bandwidth B (Section 3.3) without bandwidth limiting filter

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ABBREVIATIONS

Abbreviation	Description	Reference
ADC	analog-to-digital converter	Chapter 1
AMS	Austria Mikrosysteme	Section 2.3
AVG	averaging	Section 5.1
CCD	charge-coupled device	Chapter 1
CCD+AI	charge-coupled device with active integrator	Section 5.2
CCD+PI	charge-coupled device with passive integrator	Section 5.2
CDS	correlated double sampling	Section 3.3
CMOS	complementary metal-oxide-semiconductor	Chapter 1
CMTI	current-mode transintegrator	Section 7.3
CPG	constant lateral field photogate	Section 6.2
CPG+PI	constant lateral field photogate with passive integrator	Section 6.2
dc	direct current	Section 3.3
DAC	digital-to-analog converter	Chapter 1
DR	dynamic range	Section 3.5
DSP	digital signal processor	Section 2.5
DUT	device-under-test	Section 3.7
IR	infrared	Chapter 1
IRADC	current ramp analog-to-digital converter	Section 5.4
ISDPS	integrating sampled-data photosensing	Chapter 3
LED	light emitting diode	Section 3.7
MOS	metal-oxide-semiconductor	Chapter 1
pixel	picture element	Chapter 1
pw	p-diffusion/n-well photodiode	Section 4.1
pw+sw	p-diffusion/n-well photodiode in combination with p-substrate/n-well photodiode	Section 4.1

Abbreviation	Description	Reference
PAPS	photogate active pixel sensor	Section 5.2
PD	photodiode	Section 4.1
PD+AI	photodiode with active integrator	Section 5.1
PD+CMTI	photodiode with current-mode transintegrator	Section 7.4
PD+PI	photodiode with passive integrator	Section 5.1
PD+TIA	photodiode with transimpedance amplifier	Section 5.1
PDA+AI	photodiode array with active integrator	Section 5.2
PDCS	photodiode current source	Section 7.2
PDCS+CMTI	photodiode current source with current-mode transintegrator	Section 7.5
PG	photogate	Section 4.2
PG+AI	photogate with active integrator	Section 5.1
PG+PI	photogate with passive integrator	Section 5.1
rms	root mean square	Section 3.4
sn	p-substrate/n-diffusion photodiode	Section 4.1
sw	p-substrate/n-well photodiode	Section 4.1
SAPS	standard active pixel sensor	Section 5.2
SNR	signal-to-noise ratio	Section 3.4
SPG	sweep photogate	Section 6.3
SSPG+SPI	shifted sweep photogate with sensitive passive integrator	Section 6.3

SYMBOLS

Symbol	Description	Unit	Reference
α	transistor noise coefficient	[-]	(3.93)
α_G	attenuation constant	[m^{-1}]	(6.11)
α_{opt}	absorption coefficient	[m^{-1}]	(2.9)
β_G	phase constant	[m^{-1}]	(6.11)
$\underline{\gamma}_G$	propagation constant	[m^{-1}]	(6.11)
γ_s	surface potential approximation coefficient	[-]	(6.5)
η	quantum efficiency	[%]	(2.8)
λ	wavelength	[m]	(2.6)
λ_G	wavelength (transmission line)	[m]	(6.14)
μ	mobility	[m^2/Vs]	(3.120)
μ_n	mean number of photogenerated charge carriers	[-]	(3.156)
μ_t	mean level-crossing time	[s]	(3.175)
μ_v	mean integration voltage	[V]	(3.166)
σ_n	standard deviation of the number of photogenerated charge carriers	[-]	(3.157)
σ_t	standard deviation of the level-crossing time	[s]	(3.176)
σ_v	standard deviation of the integration voltage	[V]	(3.167)
ϕ	potential	[V]	Fig. 4.1
ϕ_s	surface potential	[V]	Fig. 4.4, (6.5)
ω	angular frequency	[s^{-1}]	(3.70)

Symbol	Description	Unit	Reference
a	voltage amplifier gain	[-]	(3.7)
A	photodetector area	[m^2]	(3.1)
A_{chip}	chip area	[m^2]	Sect. 3.5
A_{opt}	light spot size	[m^2]	(2.1)
B	analog bandwidth	[Hz]	(3.55)
B_n	noise-effective bandwidth	[Hz]	(3.56)
B_{signal}	signal bandwidth	[Hz]	(2.14)
B_{ss}	sampling-limited signal bandwidth	[Hz]	(2.15)
c	speed of light	[m/s]	(2.7)
C	capacitance	[F]	Fig. 2.3
C'_G	specific gate capacitance per unit length	[F/m]	(6.8)
C_{int}	integration capacitance	[F]	(3.5)
C''_{ox}	specific oxide capacitance per unit area	[F/m^2]	(3.114)
C_{ph}	photodetector capacitance	[F]	(3.96)
C''_{ph}	specific photodetector capacitance per unit area	[F/m^2]	(3.96)
$C_{physical}$	physical capacitance	[F]	Sect. 3.6
C_{virt}	virtual integration capacitance	[F]	(3.20)
D	diffusion constant	[m^2/s]	(6.1)
D_i	digital output sample of the current ramp ADC	[-]	Sect. 3.1
D_n	digital output sample error	[-]	Fig. 3.1
D_{n_t}	digital output sample error due to quantization noise	[-]	Fig. 3.1
D_v	digital output sample of the voltage ramp ADC	[-]	Sect. 3.1
DR	dynamic range	[-],[dB]	(3.148)
DR_b	dynamic range (if a bias current is provided)	[-],[dB]	Tab. 5.3
e	elementary charge	[C]	(2.13)
E	electric field	[V/m]	Fig. 2.2
E_{opt}	optical energy	[J]	(2.2)
E_{photon}	photon energy	[J]	(2.4)
E_x	surface electric field in lateral direction	[V/m]	(6.4)

Symbol	Description	Unit	Reference
f	frequency	[Hz]	(2.6)
$f_n(n)$	density function of the number of photogenerated charge carriers	[-]	(3.162)
f_s	sampling frequency	[Hz]	(2.16)
$f_t(t)$	density function of the level-crossing time	[-]	(3.173)
$f_v(v)$	density function of the integration voltage	[-]	(3.165)
g	transconductor value	[S]	(3.8)
g_m	transconductance of the transistor	[S]	(3.120)
g_{ma}	transconductance of voltage amplifier noise-equivalent transistors	[S]	(3.100)
g_{mg}	transconductance of transconductor noise-equivalent transistors	[S]	(3.104)
g_{mp}	transconductance of preamplifier noise-equivalent transistors	[S]	(3.95)
G'_G	specific gate conductance per unit length	[S/m]	(6.8)
h	Planck constant	[Js]	(2.5)
h_{virt}	virtual integration coefficient	[s]	(3.24)
H_A	transfer coefficient	[Am^2/Ws]	(3.33)
i	current, (index)	[A], [-]	(3.83)
i_G	gate current	[A]	(6.8)
i_{int}	integration current	[A]	(3.8)
Δi_{int}	integration current drop	[A]	Sect. 3.1
i_n	noise current root power spectral density	[A/$\sqrt{\text{Hz}}$]	Fig. 3.1
i_{n_f}	noise current root power spectral density of 1/f noise	[A/$\sqrt{\text{Hz}}$]	(3.118)
i_{n_g}	noise current root power spectral density of the transconductor	[A/$\sqrt{\text{Hz}}$]	(3.104)
i_{n_p}	noise current root power spectral density of the preamplifier	[A/$\sqrt{\text{Hz}}$]	(3.95)
$i_{n_{RADC}}$	noise current root power spectral density of the ramp ADC	[A/$\sqrt{\text{Hz}}$]	(3.129)

Symbol	Description	Unit	Reference
$i_{n_{shot}}$	noise current root power spectral density of shot noise	[A/$\sqrt{\text{Hz}}$]	(3.90)
$i_{n_{transistor}}$	noise current root power spectral density of a single transistor	[A/$\sqrt{\text{Hz}}$]	(3.93)
i_{neff}	rms noise current	[A]	(3.97)
$i_{nRADCeff}$	ramp ADC input noise current	[A]	(3.128)
i_{out}	output current	[A]	Fig. 4.1
i_p	preamplified current	[A]	(3.4)
i_{ph}	photocurrent	[A]	(2.11)
i_{phavg}	photocurrent (if averaging is applied)	[A]	(3.58)
$i_{phavgneq}$	noise-equivalent photocurrent (if averaging is applied)	[A]	(3.143)
i_{phb}	photocurrent (if a bias current is provided)	[A]	(3.3)
i_{phbavg}	photocurrent (if a bias current is provided and averaging is applied)	[A]	(3.59)
$i_{phbavgneq}$	noise-equivalent photocurrent (if a bias current is provided and averaging is applied)	[A]	(3.144)
i_{phbneq}	noise-equivalent photocurrent (if a bias current is provided)	[A]	(3.141)
i_{phmax}	maximum photocurrent	[A]	(3.34)
i_{phmin}	minimum photocurrent	[A]	(3.35)
i_{phneq}	noise-equivalent photocurrent	[A]	(3.91)
i_{phneq_a}	noise-equivalent photocurrent for voltage amplifier thermal noise	[A]	(3.135)
i_{phneq_f}	noise-equivalent photocurrent for 1/f noise	[A]	(3.135)
i_{phneq_g}	noise-equivalent photocurrent for transconductor thermal noise	[A]	(3.137)
i_{phneq_p}	noise-equivalent photocurrent for preamplifier thermal noise	[A]	(3.135)
i_{phneq_R}	noise-equivalent photocurrent for resistor thermal noise	[A]	(3.137)
$i_{phneq_{RADC}}$	noise-equivalent photocurrent for ramp ADC thermal noise	[A]	(3.135)

Symbol	Description	Unit	Reference
$i_{phneq_{shot}}$	noise-equivalent photocurrent for shot noise	[A]	(3.135)
i_{phneq_t}	noise-equivalent photocurrent for quantization noise	[A]	(3.135)
$i_{phneq_{total}}$	total noise-equivalent photocurrent	[A]	(3.135), (3.137), (3.139)
i_s	signal current	[A]	(3.2)
$\underline{I}$	current (complex notation)	[A]	(6.12)
I_B	bias current	[A]	(3.3)
I_D	drain current	[A]	(3.120)
I_{DD}	supply current	[A]	(3.152)
$\underline{I}_G$	gate current (complex notation)	[A]	(6.10)
I_I	input current	[A]	Fig. 7.3
I_O	output current	[A]	Fig. 7.2
I_R	bias current (for transistors)	[A]	Fig. 5.2
j_x	surface current density in lateral direction per unit area	[A/m^2]	(6.1)
k	Boltzmann constant	[J/K]	(3.94)
K_f	1/f noise factor	[C^2/m^2]	(3.114)
L	gate length, inductance	[m], [H]	(3.114), Fig. 6.6
L'_G	specific gate inductance per unit length	[H/m]	(6.8)
m	number of integration samples per signal measurement	[-]	(3.57)
n	number of charge carriers, (index)	[-]	(3.155)
n'	(integration variable)	[-]	(3.161)
n_a	number of voltage amplifier noise-equivalent transistors	[-]	(3.100)
n_{CDS}	number of ramp samples per integration measurement	[-]	(3.95)
n_g	number of transconductor noise-equivalent transistors	[-]	(3.104)
n_{int}	number of collected charge carriers	[-]	(3.17)

Symbol	Description	Unit	Reference
n_p	number of preamplifier noise-equivalent transistors	[-]	(3.95)
n_{ph}	number of photogenerated charge carriers	[-]	(2.8)
n_{photon}	number of photons	[-]	(2.3)
n_t	number of time slots	[-]	(3.156)
N	number of integration samples (for performance extraction)	[-]	(3.153)
N_{if}	1/f noise current coefficient	[A^2]	(3.118)
$N_{if_{transistor}}$	1/f noise current coefficient of the single transistor	[A^2]	(3.119)
N_{int}	total number of collected charge carriers	[-]	(3.18)
N_{intb}	total number of collected charge carriers not generated by the bias current (if a bias current is provided)	[-]	(3.51)
$N_{intbias}$	total number of collected charge carriers generated only by the bias current	[-]	(3.50)
N_{neff}	rms noise in number of photogenerated charge carriers	[-]	(3.89)
N_{ph}	total number of photogenerated charge carriers, total number of apparently photogenerated charge carriers (if a bias current is provided)	[-]	(3.14), (3.43)
N_{phavg}	total number of photogenerated charge carriers (if averaging is applied)	[-]	(3.60)
N_{phb}	total number of photogenerated charge carriers (if a bias current is provided)	[-]	(3.45)
N_{phbavg}	total number of photogenerated charge carriers (if a bias current is provided and averaging is applied)	[-]	(3.61)

Symbol	Description	Unit	Reference
N_{phbias}	total number of apparently photogenerated charge carriers generated only by the bias current	[-]	(3.44)
N_{vf}	1/f noise voltage coefficient	[V^2]	(3.113)
$N_{vf_{transistor}}$	1/f noise voltage coefficient of the single transistor	[V^2]	(3.114)
p	preamplifier gain	[-]	(3.4)
p_n	probability that a charge carrier occurs in a single time slot	[-]	(3.156)
$P[\,]$	probability	[-]	(3.155)
$P[n_{ph} = n]$	probability of the number of photogenerated charge carriers	[-]	(3.155)
$P[n_{ph} \leq n]$	distribution function of the number of photogenerated charge carriers	[-]	(3.161)
$P[t_x \leq t]$	distribution function of the level-crossing time	[-]	(3.172)
$P[v_{int} \leq v]$	distribution function of the integration voltage	[-]	(3.164)
P_{DD}	consumed static power	[W]	(3.152)
P_{el}	electrical power	[W]	(3.83)
P_{elneq}	noise-equivalent electrical power	[W]	(3.82)
P_{noise}	noise power	[W]	(3.75)
P_{opt}	optical power	[W]	(2.1)
P''_{opt}	optical power density per unit area	[W/m^2]	(2.1)
P''_{optb}	optical power density (if a bias current is provided)	[W/m^2]	(3.39)
$P''_{optbavgneq}$	noise-equivalent optical power density (if a bias current is provided and averaging is applied)	[W/m^2]	Tab. 5.4
$P''_{optbmax}$	maximum optical power density (if a bias current is provided)	[W/m^2]	Tab. 5.3
$P''_{optbmin}$	minimum optical power density (if a bias current is provided)	[W/m^2]	Tab. 5.3
$P''_{optbneq}$	noise-equivalent optical power density (if a bias current is provided)	[W/m^2]	Tab. 5.3
P''_{optmax}	maximum optical power density	[W/m^2]	(3.36)
P''_{optmin}	minimum optical power density	[W/m^2]	(3.37)

Symbol	Description	Unit	Reference
P_{optneq}	noise-equivalent optical power	[W]	(3.78)
P''_{optneq}	noise-equivalent optical power density	[W/m^2]	(3.150)
P_{signal}	signal power	[W]	(3.74)
$P_{signal\ neq}$	noise-equivalent signal power	[W]	(3.75)
q_{int}	collected charge	[C]	(3.15)
q_{ph}	photogenerated charge	[C]	(3.11)
q''_s	surface charge density per unit area	[C/m^2]	(6.5)
q'''_s	surface charge density per unit volume	[C/m^3]	(6.1)
Q_{int}	total collected charge	[C]	(3.16)
Q_{intb}	total collected charge not generated by the bias current (if a bias current is provided)	[C]	(3.48)
$Q_{intbias}$	total collected charge generated only by the bias current	[C]	(3.47)
Q_{ph}	total photogenerated charge, total apparently photogenerated charge (if a bias current is provided)	[C]	(3.12), (3.40)
Q_{phb}	total photogenerated charge (if a bias current is provided)	[C]	(3.42)
Q_{phbias}	total apparently photogenerated charge generated only by the bias current	[C]	(3.41)
R	resistor value, resistance	[Ω]	(3.9), Fig. 5.1
R_λ	responsivity	[A/W]	(2.12)
R_A	specific responsivity	[Am^2/W]	(3.29)
R'_G	specific gate resistance per unit length	[Ω/m]	(6.8)
s	signal, signal voltage	[V]	Fig. 3.2, (3.65)
Δs	signal drop		Fig. 3.4
$s_n(t)$	noisy voltage	[V]	(3.64)
s_{neq}	noise-equivalent signal voltage	[V]	(3.73)
$S(\omega)$	power spectral density	[V^2/Hz]	(3.69)
S_{tot}	total power	[V^2]	(3.71)

Symbol	Description	Unit	Reference
SNR	signal-to-noise ratio	[-],[dB]	(3.86)
SNR_a	signal-to-noise ratio for voltage amplifier thermal noise	[-],[dB]	(3.136)
SNR_{avg}	signal-to-noise ratio (if averaging is applied)	[-],[dB]	(3.145)
SNR_b	signal-to-noise ratio (if a bias current is provided)	[-],[dB]	(3.142)
SNR_{bavg}	signal-to-noise ratio (if a bias current is provided and averaging is applied)	[-],[dB]	(3.146)
SNR_{el}	electrical signal-to-noise ratio	[-],[dB$_{el}$]	(3.82)
SNR_f	signal-to-noise ratio for 1/f noise	[-],[dB]	(3.136)
SNR_g	signal-to-noise ratio for transconductor thermal noise	[-],[dB]	(3.138)
SNR_{gen}	signal-to-noise ratio (general definition)	[-],[dB$_{gen}$]	(3.74)
SNR_n	signal-to-noise ratio of the number of photogenerated charge carriers	[-],[dB]	(3.158)
SNR_{opt}	optical signal-to-noise ratio	[-],[dB$_{opt}$]	(3.78)
SNR_p	signal-to-noise ratio for preamplifier thermal noise	[-],[dB]	(3.136)
SNR_R	signal-to-noise ratio for resistor thermal noise	[-],[dB]	(3.138)
SNR_{RADC}	signal-to-noise ratio for ramp ADC thermal noise	[-],[dB]	(3.136)
SNR_{shot}	signal-to-noise ratio for shot noise	[-],[dB]	(3.136)
SNR_t	signal-to-noise ratio for quantization noise, signal-to-noise ratio of the level-crossing time	[-],[dB]	(3.136), (3.177)
SNR_{total}	total signal-to-noise ratio	[-],[dB]	(3.136), (3.138), (3.140)
t	time	[s]	(3.6)
t'	(integration variable)	[s]	(3.171)
Δt	integration time	[s]	Sect. 3.1
Δt_A	measurement time	[s]	Tab. 5.2

Symbol	Description	Unit	Reference
Δt_i	integration samples	[s]	(3.153)
Δt_{max}	maximum integration time	[s]	Sect. 3.2
Δt_{min}	minimum integration time	[s]	Sect. 3.2
t_{neff}	rms noise in time	[s]	(3.132)
Δt_{neff}	rms noise in integration time	[s]	(3.154)
t_{res}	timing resolution	[s]	(3.132)
t_x	level-crossing time	[s]	(3.172)
T	period, temperature	[s], [K]	(3.67), (3.93)
T_A	transfer factor	[Vm^2/Ws]	(3.31)
T_s	sampling period	[s]	(2.16)
v	voltage	[V]	(3.64)
v'	(integration variable)	[V]	(3.164)
v_a	amplified voltage	[V]	(3.7)
Δv_a	amplified voltage drop	[V]	Sect. 3.1
v_D	voltage across the sensing diode	[V]	Tab. 5.6
v_g	group velocity	[m/s]	(6.16)
v_G	gate voltage	[V]	(6.5)
v_{in}	input voltage	[V]	Fig. 6.6
v_{int}	integration voltage	[V]	(3.5)
Δv_{int}	integration voltage drop	[V]	(3.19)
Δv_{intavg}	integration voltage drop (if averaging is applied)	[V]	(3.62)
Δv_{intb}	integration voltage drop not generated by the bias current (if a bias current is provided)	[V]	(3.54)
$\Delta v_{intbavg}$	integration voltage drop not generated by the bias current (if a bias current is provided and averaging is applied)	[V]	(3.63)
$\Delta v_{intbias}$	integration voltage drop generated only by the bias current	[V]	(3.53)
v_n	noise voltage root power spectral density	[V/$\sqrt{\text{Hz}}$]	Fig. 3.1, (3.72)
v_{n_a}	noise voltage root power spectral density of the voltage amplifier	[V/$\sqrt{\text{Hz}}$]	(3.100)

Symbol	Description	Unit	Reference
v_{n_f}	noise voltage root power spectral density of 1/f noise	[V/$\sqrt{\text{Hz}}$]	(3.113)
$v_{n_{resistor}}$	noise voltage root power spectral density of a resistor	[V/$\sqrt{\text{Hz}}$]	(3.108)
v_{n_R}	noise voltage root power spectral density of the resistor	[V/$\sqrt{\text{Hz}}$]	(3.109)
$v_{n_{RADC}}$	noise voltage root power spectral density of the ramp ADC	[V/$\sqrt{\text{Hz}}$]	(3.125)
$v_n(t)$	noise voltage	[V]	(3.66)
$v_{n\,eff}$	rms noise voltage	[V]	(3.68)
$v_{nRADC\,eff}$	ramp ADC input noise voltage	[V]	(3.124)
v_p	phase velocity	[m/s]	(6.15)
V	voltage	[V]	Fig. 5.25
$\underline{V}$	voltage (complex notation)	[V]	(6.12)
V_{DD}	supply voltage	[V]	(3.152)
V_{FB}	flat-band voltage	[V]	(6.5)
V_G	gate voltage	[V]	Fig. 4.4
$\underline{V}_G$	gate voltage (complex notation)	[V]	(6.10)
V_I	input voltage	[V]	Fig. 7.3
V_L	lateral voltage	[V]	Fig. 6.2
V_O	output voltage	[V]	Fig. 5.1
V_R	reset voltage, reference voltage	[V]	Fig. 5.2, Fig. 7.4
V_T	transfer gate voltage	[V]	Fig. 5.25
W	gate width	[m]	(3.114)
x	position (in lateral direction)	[m]	(6.1)
y	depth (in vertical direction)	[m]	(2.9)
y_{opt}	light penetration depth	[m]	(2.10)
$\underline{Z}_G$	characteristic impedance	[Ω]	(6.13)

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