14. Mai 1998

Diss. ETH No. 12389

Investigation of the 3-level Voltage Source Inverter (VSI) for Flexible AC-Transmission Systems (FACTS) exemplified on a Static Var Compensator (SVC)

A dissertation submitted to the SWISS FEDERAL INSTITUTE OF TECHNOLOGY ZURICH for the degree of Doctor of Technical Sciences

> presented by Gerald Scheuer Dipl. El. Ing. TH born August 16, 1962 citizen of Germany

accepted on the recommendation of Prof. Dr. H. Stemmler, examiner Prof. Dr. Å. Ekström, co-examiner

1997

Preface

The investigations in this thesis were performed in the years 1992-1997 during my employment as a research and teaching assistant at the Chair of Power Electronics and Electrometrology at the Swiss Federal Institute of Technology Zurich.

First of all, I want to thank Prof. Dr. H. Stemmler for his permanent support and encouragement during this project and also for the acceptance of the examination.

My special thanks also go to Prof. Dr. Å. Ekström for the critical review of this thesis and the commitment to act as co-examiner.

In addition, I am indebted to all my colleagues at the chair for their friendly support, especially to my friend Adrian Omlin for the numerous critical and fertile discussions.

More, I want to thank H. Altdorfer, J. Pellegrini, P. Seitz and U. Wenk from the electronic development laboratory for the construction of a 3-level VSI hardware model.

I am further bound in gratitude to all the students, who contributed with their student or diploma works to the success of this thesis.

Last but surely not least, I would like to thank my girl-friend Pia for her patience and understanding, especially during the final stage of this work.

This thesis was accomplished and financed as part of the research promotion program LESIT (power electronic systems and communication technology), which was founded by the Swiss Federal Government.

Leer - Vide - Empty

.

Table of contents

Pı	eface	e	1
Ta	able o	of contents	3
St	ımma	ary1	1
Zı	isam	menfassung 1	3
			_
1	Intr	roduction 1'	7
	1.1	The electric energy economy today 1'	7
	1.2	Traditional and todays AC-system controllers 18	8
	1.3	Flexible AC Transmission Systems (FACTS) -	
		the solution for the future 20	0
	1.4	2-level VSI versus 3-level VSI 22	2
	1.5	Scope of the thesis 2	3
2	The	3-level VSI in transmission applications	6
	2.1	Overview	6
	2.2	The 3-level VSI circuit and basic operation principles 20	6
	2.3	Model of the 3-level VSI in transmission applications 3	0
		2.3.1 Topology302.3.2 Notation of the quantities302.3.3 AC-system voltages312.3.4 Passive components312.3.5 Switching functions31)) 1 1 1
	2.4	3-level VSI system equations 33	3
		2.4.13-level VSI equations on the AC-side342.4.2System equations on the AC-side362.4.33-level VSI equations on the DC-side38	4 5 8
	2.5	Accuracy of approximations for s_{ph}^2 and $ s_{ph} $ 43	1
		2.5.1 Approximation of the switching functions by means	

·	of its fundamental component	42
	zero sequence system	43
2.6	Summary	44
3 Mo	dulation schemes	46
3.1	Overview	46
3.2	Requirements in transmission applications	46
3,3	Classification of the modulation schemes	48
,	 3.3.1 Asynchronous and synchronous modulation schemes 3.3.2 Symmetry attributes	48 48 49
34	Off-line optimized PWM (incl. FFM)	5 0
5.4	3.4.1 Introduction	50
	 3.4.2 Optimization criterias for transmission applications 3.4.3 Generation of the off-line optimized pulse patterns 3.4.4 Attributes of the off-line optimized pulse patterns 	50 51 52 54
3.5	Carrier based PWM	57
	3.5.1 Introduction3.5.2 Carrier based PWM pulse patterns with flat-top	57
	control signals	57
26	5.5.5 Characteristics of the carrier based pulse patterns	62
3.0	2 6 1 Operation and and and and and and and	00
	3.6.2 Influence of the AC-system strength	67 68
3.7	Comparison of off-line and carrier based PWM	70
	3.7.1 AC-side currents and filter requirements	71
	3.7.2 Influence on 3-level VSI design parameters	77
3.8	Compatibility with control requirements	83
3.9	Summary	84

4	Qu	alitative harmonic analysis			
	4.1	Overview			
	4.2	Motivation	. 87		
	4.3	Symmetrical operation conditions	. 88		
		4.3.1 Mathematical basics	88 91 96		
	4.4	Asymmetrical operation conditions	99		
		 4.4.1 Mathematical basics	100 101 105		
	4.5	Summary	105		
5	The	harmonic DC-side oscillation	107		
	5.1	Overview			
	5.2	Introduction 1			
	5.3	Driving force for the harmonic DC-side oscillation 10			
	5.4	Generation principle of the NP-current 10			
		 5.4.1 Driving forces for the NP-current 5.4.2 Operation mode considerations and simplifications 5.4.3 Generation principle and harmonics of the NP-current for EEM modulation 	110 111		
		5.4.4 Extension to off-line optimized and carrier based PWM	112		
	5.5	Influence of the modulation index	124		
		5.5.1 FFM modulation.5.5.2 Off-line optimized PWM5.5.3 Carrier based PWM	125 130 135		
	5.6	Influence of the switching frequency	141		
		5.6.1 Basic considerations.5.6.2 Influence on the 3rd NP-current harmonic.5.6.3 Influence on the higher ordered NP-current harmonics.	141 143 148		
	5.7	Summary	153		

6	Qua	ntitative harmonic analysis for a SVC application	156
	6.1 Overview		
	6.2	Solution methods for the system equations	156
	6.3	SVC	158
		6.3.1 Control scheme.6.3.2 Modulation schemes.6.3.3 System parameters .	158 160 160
	6.4	Symmetrical operation conditions	162
		 6.4.1 Harmonic orders	162 167 171 172
	6.5	Asymmetrical operation conditions	173
		6.5.1 Harmonic orders6.5.2 DC-side quantities	174 174
	6.6	Influence of the DC-side capacitor size	178
		6.6.1 DC-side voltages6.6.2 AC-side current harmonics6.6.3 AC-side current THD	179 183 186
	6.7	Summary	187
7	The	3-level VSI DC-side unbalance	190
	7.1	Overview	190
	7.2	Introduction	190
	7.3	Harmonic analysis in case of a DC-side unbalance	192
		7.3.1 DC-side harmonics.7.3.2 AC-side harmonics.7.3.3 Simulation results.	192 195 197
	7.4	3-level VSI self-balancing analysis	201
		7.4.1 Qualitative 3-level VSI self-balancing analysis7.4.2 Quantitative 3-level VSI self-balancing analysis7.4.3 Discussion	201 208 210

		7.4.4	Influence of the higher ordered even numbered	
			harmonics of the AC-side currents.	215
		7.4.5	Influence of the total DC-side voltage harmonics	216
		7.4.6	Simulation results	219
	7.5	DC-si	ide unbalance sources and their impact	223
		7.5.1	DC-side unbalance transfer functions	223
		7.5.2	DC-side unbalance caused by transient load steps	227
		7.5.3	DC-side unbalance caused by transients in the	•••
			AC-system voltages	229
		7.5.4	Unbalance caused by even numbered AC-system	221
			harmonics	231
		7.5.5	DC-side unbalance caused by switching inaccuracies	230
	7.6	Sum	nary	238
•	The	2 1000	I VSI DC side belance control	241
0	1 пе	J-leve	a vsi DC-side balance control	271
	8.1	Over	view	241
	8.2	Intro	duction	241
	8.3	DC-si	ide balancing control measures	243
		8.3.1	DC-side balancing control of type I for	
		0.0.1	pure active operation mode	243
		8.3.2	DC-side DC-balancing control of type I for	
			pure reactive operation mode	250
		8.3.3	DC-side DC-balancing control of type II for	
			pure active operation mode	252
		8.3.4	DC-side DC-balancing control of type II for	
			pure reactive operation mode	258
	8.4	Cont	rol design for a SVC	262
		8.4.1	Transfer functions for the DC-side balance control	
			of type II	263
		8.4.2	The critical operation point in dependancy on	
			system parameters	267
		8.4.3	Closed loop control design for the FFM	
			modulated SVC	273
		8.4.4	Feed-forward controller for the FFM modulated SVC .	278
		8.4.5	Phased Locked Loop (PLL)	279

		8.4.6 Simulation results	281
	8.5	Summary	288
	~		••••
9 (Con	itrol of the SVC	290
9	9.1	Overview	290
9	9.2	Introduction	290
9	9.3	SVC current control loop design	291
		9.3.1 Transfer functions of the SVC	291
		9.3.2 Control loop design	292
		9.3.3 Simulation results of the 3-level VSI SVC	300
9	9.4	SVC control during AC-system faults	320
		9.4.1 Basics	320
		9.4.2 Feed-forward controller design	321
		9.4.3 Separation of the positive and negative sequence	
		fundamental AC-system voltage components in	
		the d/q-plane	327
		9.4.4 Calculation of the control signals for the	
		FFM modulator	329
		9.4.5 Simulation results.	330
9	9.5	Summary	339
Арр	end	lix A	340
Nor	mal	lisation and capacitor time constant	340
A	4.1	Normalisation	340
		A.1.1 Reference quantities	340
		A.1.2 Per unit representation of individual quantities	341
		A.1.3 Per unit transformation of equations	342
		A.1.4 Laplace transform of per unit equations.	342
A	4.2	Definition of the capacitor time constant	343
		A.2.1 2-level VSI	343
		A.2.2 3-ievel VSI	543
Арр	end	lix B	345
3-lev	vel `	VSI switching functions	345
F	3.1	Fourier rows	345

	B.1.1	General definition	345
	B.1.2	3-level VSI switching functions with a symmetry to	
		a period	345
	B.1.3	3-level VSI switching functions with a symmetry to	
		half of a period	348
	B.1.4	3-level VSI switching functions with a symmetry to	
		a quarter of a period	349
B.2	FFM	switching functions	352
	B.2.1	3-level VSI FFM switching function	352
	B.2.2	Modified 3-level VSI FFM switching function for	
		the DC-side balance control of type I	355
	B.2.3	Modified 3-level VSI FFM switching function for	
		the DC-side balance control of type II	357
B. 3	PWM	I switching functions	. 360
	B.3.1	3-level VSI PWM switching functions with a symmetry	
		to a quarter of a period	361
	B.3.2	Modified 3-level VSI PWM switching function for	
		DC-side balance control of type I	363
	B.3.3	Modified 3-level VSI PWM switching function for	
		DC-side balance control of type II	366
Appen	dix C		370
Coord	inata ti	mancharms	370
CUUIU	inaut u	ansionins	570
C.1	The a	alpha/beta transform	. 370
	C.1.1	Transformation from 3-phase to alpha/beta	
		representation	373
	C.1.2	Transformation from alpha/beta to 3-phase	
		representation	374
C. 2	The d	l/q transform	. 372
	C.2.1	Transformation from alpha/beta to d/q representation	372
	C.2.2	Transformation from d/q to alpha/beta representation	374
Арреп	dix D		375
The dy	namic	phasor equations of the system	375
D.1	3-pha	ase to d/q transformation	375
	D.1.1	AC-side equations	376
	D.1.2	DC-side equations	377
D.2	State	-space representation and linearization	379
	D.2.1	State-space representation	379

	D.2.2	Linearization	380
Appen	dix E		382
Transf	er funo	ctions of the system	382
E.1	Tran	sfer functions for the control of fundamental	
	comp	onents	382
	E.1.1	Linearized state-space equations in a d/q frame	
		rotating with an angular velocity w1	382
	E.1.2	Transformation into the Laplace domain	384
	E.1.3	Calculation of the transfer functions	386
E.2	Trans	sfer functions for the control of the DC-side balance .	393
	E.2.1	Linearized state-space equations in a d/q frame	
		rotating with an angular velocity -2w1	393
	E.2.2	Transformation into the Laplace domain	395
	E.2.3	Calculation of the transfer functions	396
E.3	Trans	sfer functions for DC-side self-balancing analysis	400
	E.3.1	State-space equations in a d/q frame rotating with	
		an angular velocity -2w1	400
	E.3.2	Transformation into the Laplace domain	401
	E.3.3	Calculation of the transfer functions	402
Referer	nces	•••••	404
List of s	symbol	ls	410
Curricu	ılum v	itae	421
Lebens	lauf	••••••	423

Summary

Due to the arising liberalization and deregulation of the electric energy market, the demands on an AC-transmission system are steadily growing. Therefore, also more sophisticated AC-system controllers and topologies are highly needed.

This thesis is focusing on one of these more sophisticated topologies, the 3phase 3-level Voltage Source Inverter (shortly: 3-level VSI), which might become an interesting high power circuit for transmission applications.

In a first step, the mathematical equations of the 3-level VSI connected in shunt to an AC-system are derived, which has been performed in a most general way. The hereby achieved results are the basis for all further investigations in this thesis.

The proceeding chapter is dedicated to appropriate modulation schemes for 3-level VSI transmission applications. It is shown that off-line optimized pulse patterns with selective elimination of harmonics and a sophisticated carrier based PWM method are best suited to fulfil the requirements. In addition, both modulation schemes are compared with respect to their harmonic pollution of the AC-system and the utilization of the 3-level VSI in a wide frequency range (50Hz - 1450Hz).

A qualitative harmonic analysis results in the particular harmonic orders, which have to be expected in the individual 3-level VSI AC- and DC-side quantities. The analysis also includes the derivation of general harmonic transfer rules, which describe the relationship between the AC- and the DC-side harmonics. All investigations are performed for both symmetrical and asymmetrical operation conditions.

The harmonic analysis shows up a remarkable drawback of the 3-level VSI topology, which is manifested in an undesirable 3rd harmonic oscillation in the two DC-side voltages. The generation principle of this 3rd harmonic oscillation and its dependancy on the 3-level VSI operation mode, the modulation index of the switching functions and its switching frequencies will be studied in depth for off-line optimized and carrier based PWM.

The general valid results achieved in the two preceding chapters will then be verified by simulations. This will be performed for the pure reactive operation mode by means of a 3-level VSI Static Var Compensator (SVC) with realistic system parameters. The simulations do not only fortify the analyses

but also uncover further disadvantages caused by the 3rd harmonic DC-side oscillation, which yields the result that the 3-level VSI DC-side capacitors should not be chosen too small.

Another drawback of the 3-level VSI concerns the undesirable DC-unbalance of the two splitted DC-side voltages. Hence, detailed investigations with respect to the 3-level VSI self-balancing attributes are carried out and the various DC-unbalance sources are introduced. The theoretical results, which are basing on the general 3-level VSI transfer functions, are confirmed by simulations of a 3-level VSI SVC. In addition, the simulations show up the quantitative impact of all DC-unbalance sources and further prove that an active DC-balance control will be of high need.

Consequently, the chapter to follow is focusing on two possible DC-side DC-balance control measures, which consist in appropriate modifications of the pulse patterns. It can be seen that the efficiency of these control measures strongly depend on the operation point and the operation mode of the 3-level VSI. More, for the pure reactive operation mode, only one of the two proposed methods is suitable to control the DC-balance of the two DC-side voltages. This method will be investigated further in depth by designing a control scheme for a 3-level VSI SVC with realistic system parameters. The simulations both prove a high efficiency of the controller over a wide operation range but also uncover some inherent disadvantages, when operating in the pure capacitive region. In order to eliminate these drawbacks, very serious studies will be of high need.

Finally, the last chapter is dedicated to the control of the 3-level VSI ACside quantities under symmetrical and asymmetrical AC-system conditions. For that purpose, the dynamic transfer functions of the system are derived in its most general form, which also includes the influence of disturbances in the AC-system voltages. These transfer functions constitute a very good basis for studies concerning the dynamic system behaviour for all applications (connected in shunt to the AC-system). Basing on the above mentioned transfer functions, a current control is designed for a 3-level VSI SVC with realistic parameters. This is done with respect to symmetrical and asymmetrical AC-system conditions by means of both a closed loop and a feed-forward controller. In addition a current limiting controller, which exclusively is active in case of transient over-currents, is superimposed to the conventional control scheme. The simulations show a quite reasonable performance, even during large AC-system disturbances, if the AC-system is not weak. In weak AC-systems, the performance with respect to AC-system disturbances is bad and further in depth investigations are highly desirable.

Zusammenfassung

Aufgrund der zunehmenden Liberalisierung und Deregulation des elektrischen Energiemarktes wachsen in gleichem Mass auch die Anforderungen an das elektrische übertragungssystem. Daher wird schon in naher Zukunft ein steigender Bedarf nach moderneren Netzregeleinrichtungen und Schaltungen bemerkbar sein.

In dieses Arbeit wird eine dieser modernen Schaltungen, der 3-phasige 3-Punkt Spannungszwischenkreis Wechselrichter (kurz: 3-Punkt WR) untersucht.

In einem ersten Schritt werden die allgemeingültigen Gleichungen des parallel ans Netz geschalteten 3-Punkt WRs hergeleitet. Die hierbei erhaltenen Ergebnisse bilden die Basis für alle weiteren Untersuchungen in dieser Arbeit.

Das darauffolgende Kapitel widmet sich geeigneten Modulationsverfahren für 3-Punkt WR Netzanwendungen. Es wird gezeigt, dass off-line optimierte Pulsmuster mit Elimination von Harmonischen sowie ein sophistisches Trägerverfahren besonders gut geeignet sind für Netzanwendungen. Beide Modulationsverfahren werden dann bezüglich ihrer erzeugenden Netzverzerrungen und im Hinblick auf die Ausnutzung des 3-Punkt WRs in einem weiten Frequenzbereich (50Hz - 1450Hz) miteinander verglichen.

Eine allgemeine harmonische Analyse zeigt die Ordnungszahlen der Harmonischen auf, welche in den einzelnen AC- und DC- seitigen 3-Punkt WR Strömen und Spannungen erwartet werden müssen. Diese Analyse beinhaltet ebenfalls die Herleitung von allgemeinen harmonischen Transferregeln, welche den Zusammenhang zwischen den AC- und DC-seitigen Oberschwingungen beschreiben. Die erhaltenen Ergebnisse sind sowohl für symmetrische wie auch für asymmetrische Betriebsbedingungen gültig.

Die harmonische Analyse deckt des weiteren einen grossen Nachteil der 3-Punkt WR Topologie auf, welcher im Auftreten einer sehr unerwünschten 3ten Harmonischen (und deren ungeradzahlige Vielfache) in den beiden DCseitigen Spannungen besteht. Die Erzeugung dieser Harmonischen sowie ihre Abhängigkeiten von der 3-Punkt WR Betriebsart, dem Aussteuergrad der Schaltfunktionen und deren Schaltfrequenz werden sowohl für off-line optimierte als auch für trägerbasierte Verfahren eingehend untersucht.

Die in den beiden vorangegangenen Kapiteln erhaltenen (sehr allgemeingül-

tigen) Resultate werden dann mit Hilfe von Simulationen verifiziert. Das Simulationsmodell besteht aus einem 3-Punkt WR mit realistischen Systemparametern, der als reiner Blindleistungskompensator arbeitet. Die daraus resultierenden Ergebnisse bestätigen nicht nur die durchgeführten Analysen, sondern decken weitere Nachteile auf, welche wiederum auf die unerwünschten DC-seitigen Oszillationen zurückzuführen sind. Dies führt zu der Erkenntnis, dass die DC-seitigen Kapazitäten nicht zu klein ausgelegt werden sollten.

Ein weiterer Nachteil des 3-Punkt WRs besteht in einer möglichen DC-Unsymmetrie der beiden Zwischenkreisspannungen. Daher werden eingehende Untersuchungen bezüglich des Selbst-Symmetrierverhaltens des 3-Punkt WRs durchgeführt. Ebenfalls werden die verschiedenen Ursachen für eine DC-seitige Unsymmetrie vorgestellt. Die allgemeingültigen theoretischen Resultate, welche auf den dynamischen 3-Punkt WR übertragungsfunktionen basieren, werden aufgrund von Simulationen des 3-Punkt WR Blindstromkompensators bestätigt. Die Simulationen zeigen auch den quantitativen Einfluss der einzelnen Unsymmetrieursachen auf und bestätigen die Notwendigkeit einer zusätzlichen Symmetrierregelung.

Daher werden im darauffolgenden Kapitel zwei Symmetriermassnahmen vorgestellt, welche auf geeigneten Modifikationen der Pulsmuster basieren. Es kann gezeigt werden, dass die Leistungsfähigkeit dieser Massnahmen sehr stark sowohl von der Betriebsart (Wirk/Blind-Leistungsbetrieb) als auch vom spezifischen Arbeitspunkt innerhalb der Betriebsart abhängt. Des weiteren wird deutlich, dass für reinen Blindleistungsbetrieb nur eines dieser Verfahren angewendet werden kann. Basierend auf diesem Verfahren wird eine Symmetrierregelung für den 3-Punkt WR Blindstromkompensator mit realistischen Systemparametern entworfen. Die Simulationsergebnisse bestätigen der Regelung eine hohe Leistungsfähigkeit in einem weiten Betriebsbereich, zeigen jedoch auch einige Nachteile im kapazitiven Bereich. Um diese Nachteile zu eliminieren bedarf es eingehender weiterer Studien.

Das letzte Kapitel dieser Arbeit ist der Regelung der AC-seitigen 3-Punkt WR Grössen gewidmet. Zu diesem Zweck werden die allgemeingültigen dynamischen Übertragungsfunktionen des Systems hergeleitet, welche ebenfalls den Einfluss von Störungen in den Netzanschlussspannungen berücksichtigen. Diese Übertragungsfunktionen stellen eine ausgezeichnete Basis für Studien betreffend des dynamischen Systemverhaltens für alle 3-Punkt WR Anwendungen (mit Parallelschaltung ans Netz) dar. Basierend auf den oben erwähnten Übertragungsfunktionen wird eine Stromregelung für den 3-Punkt WR Blindstromkompensator mit realistischen Systemparametern entworfen. Diese Regelung berücksichtigt sowohl symmetrische wie auch asymmetrische Netzanschlussspannungen durch einen Führungsregelkreis für den Strom und eine Störgrössenaufschaltung bei Netzspannungsfehlern. Zusätzlich wird der Regelung ein strombegrenzender Regler, welcher ausschliesslich bei transienten Überströmen aktiviert wird, überlagert. Die Simulationen zeigen brauchbare Ergebnisse, sogar bei grossen Netzspannungs-einbrüchen und -unsymmetrien, solange kein schwaches Netz vorliegt. In schwachen Netzen ist das Störverhalten der Regelung schlecht und weitere tiefergehende Studien sind von Nöten.

Leer - Vide - Empty

i

1 Introduction

1.1 The electric energy economy today

Nowadays, the electrical utilities and the related industry are undergoing profound changes due to a generalizing world economy and the developing trend toward liberalization. Not only the electrical power generation but also the transmission and distribution will remarkably be affected by this progress ([1] - [6]).

On one hand, a steadily world wide growing demand for more electrical energy can be observed, which is opposed by very restricted permissions for the building of new transmission lines, which in addition is also very cost intensive.

On the other hand, pushed by liberalization and privatization, a competitive boundary exceeding open energy market will exist, where utilities have to recruit wholesale customers, which may be located more than thousand miles away from the utility's domicile. Electrical energy might then have to be delivered over long distances via prescribed routes in between a highly interconnected AC-system.

Hence, the requirements on a transmission network have increased in the past years and will continue to do so in the future. Besides a better utilization of existing transmission lines, also the fine-tuned and fast controllable flow of electrical energy through prescribed routes are the main topics to be addressed. This in its turn inherently also asks for an enhancement of the AC-system stability in order to still ensure high levels of reliability.

Further, the demands on power quality grow permanently, since todays industrial electronic control systems, basing on integrated circuits, are very sensitive to even short outages or sags and also to harmonics in the supplying network. A survey performed by several US industries estimate the financial losses due to power quality problems to be as high as 5 billion US dollars annually [4].

Unfortunately, our traditional electrical power systems are not designed to provide all the services mentioned above and therefore, are not capable to fulfil the tasks coming along with them. For example, up to today, power flow over the most lines is moreover determined by the line's impedance. This causes the currents in a meshed system not to flow the geographically shortest way, but the electrically shortest one according to Kirchhoff's law, which also might result in undesirable loop flows [3]. These loop flows in its turn might overload an AC-line and also reduce the system stability. From this example it is evident, that e.g. a fine-tuned control of individual line impedances could to a large amount improve the performance and utilization of an AC-system.

1.2 Traditional and todays AC-system controllers

Originally, either permanently connected or at most mechanically switched components (inductors, capacitors, tap changers, breakers etc.) have been installed in an AC-system for the purpose of optimized power transfer, compensation and stability (figure 1.1 a) and b)).

However, this very simple technology cannot provide a fine tuned controllable power flow and also, in case of e.g. a mechanically controlled series capacitor, might cause <u>Sub-Synchronous Resonances</u> (SSR) [3] to be excited. This SSR arises when the electrical resonance, determined by the series capacitor and the inductive part of the AC-system, interacts with the mechanical resonance of the turbine-generator system, which might cause serious damage to the generator shaft.

More, since mechanical switching is quite slow (about 5 AC cycles), also the response to a change in the AC-system is slow. As a consequence, in order to ensure stability, an operating safety margin has to be taken into account and the transmission lines are operated at a nominal level far below their rated thermal capacity, which represents the theoretical maximum of transferable power. Further drawbacks of mechanical switches are their moderate lifetime as well as the need for frequent maintenance.

The replacement of the mechanical switches by thyristors was a first decisive step towards more flexibility and controllability of an AC-transmission system (figure 1.1 c)). These thyristor switches convince with a more frequent and faster response (at most 2-3 AC cycles) than mechanical switches, have longer lifetimes, are more reliable and do not ask for extensive maintenance.

Further, basing on these thyristor switches and sophisticated control schemes, it is possible to realize variable reactances, either capacitors or inductors, which show up a much better performance with respect to power flow control, compensation and damping attributes.



(traditional), b) mechanically switched components (traditional), c) conventional thyristor switched components (state of the art), d) GTO based 2-level VSI (state of the art, future trend), e) GTO based progress of AC-system controllers exemplified on shunt type compensation: a) fixed components 3-level VSI (future trend) fig 1.1:

Milestones for this technology include the installation of two Static Var Compensators (SVC) in 1977 and 1978, a NGH-damper (Narain G. Hingorani) in the mid 80s [3] and a single and a 3-phase Thyristor Controlled Series Capacitor (TCSC) in 1991 and 1992 respectively ([7]).

The SVCs are capable to provide both voltage and stability control (damping), however this device is not well suited to control active power flow. The NGH-damper is installed across a mechanically controlled series capacitor and addresses the damping of the above mentioned sub-synchronous resonance (SSR). The TCSCs finally enable an increased power transfer over an AC-line, reduce power flow loops and also have inherent power oscillation damping attributes.

However, there are still quite a few problems left, which cannot be solved with the conventional thyristor technique. This is moreover caused by the limited performance of the thyristor itself, which, once switched on, only switches off, if the current through it equals 0. Hence, the switching frequency is limited to the fundamental frequency of the AC-system and with that also the control response to about 2-3 AC-cycles. From this, it also seems to be evident that with respect to power quality problems like transient voltage sags, flicker, harmonic pollution, the conventional thyristor based controllers might not be expected to do a good job.

1.3 Flexible AC Transmission Systems (FACTS) - the solution for the future

Fortunately, and actually just right in time, a new technology was pushed in the late 80s, particularly by the Electric Power Research Institute (EPRI) in the USA. EPRI coined this technology Flexible <u>AC</u> Transmission Systems (FACTS) and primarily intended to find solutions enabling fine tuned power flow and fast stability control as well as a better utilization of existing transmission lines.

In this context, the above mentioned 3 conventional thyristor based systems, the SVC, the NGH-SSR damper and the TCSC can be seen as a first generation of Flexible AC Transmission System (FACTS) controllers.

The basis for the second generation of FACTS controllers was the development of a new high power semiconductor switching device, the so-called <u>Gate-Turn-Off</u> thyristor (GTO). Compared to the conventional thyristor, the GTO thyristor can be **both** switched on **and** switched off. In the late 80s, where an intensive research concerning FACTS was just about to start, these GTOs have been well established in variable speed drives applications, where they constituted the heart of the meanwhile well known 2-level <u>Voltage Source Inverter</u> (2-level VSI, figure 1.1 d)).

Though state of the art in drives applications, only a few investigations regarding the benefits of the GTO based VSI for transmission applications have been performed up to that time ([8]). More, no practical experiences have been known so far.

Theoretical studies have soon shown that the VSI, connected to an AC-system either in shunt or in series, is capable to exchange any active or reactive power with the AC-system ([9], [10]). While the active power exchange will ask for an additional energy source or sink on the DC-side (e.g. battery, rectifier, back-to-back VSI), the pure reactive operation mode exclusively requires a small DC-side capacitor.

Further, depending on the switching frequency of the GTOs, also the response of the VSI to any changes in the AC-system can be made very fast and response times less than a quarter of a period may be absolutely realistic. In addition, based on the VSI topology, more sophisticated tasks (e.g. concerning power quality), which are far out of the scope of conventional thyristor controllers, could be fulfilled. Last but not least, remarkable savings on reactive components and on real estate can be achieved.

Hence, the principal features of these 2nd generation FACTS devices, realized with the VSI topology, promise the following advantages for the control of an AC-system ([11] - [18]):

- increased capacity by loading the transmission lines to levels nearer their thermal limits
- reduction of the need for building new expensive transmission lines
- reduction of individual generation reserve margins by an improved exchange of power between the particular utilities
- fine -tunable power flow control through prescribed routes
- avoidance of power loop flows
- decreased electrical losses
- enhancing the stability and damping of existing AC transmission systems
- · capability to improve electrical power quality

First representatives of large second generation FACTS controllers to be built include 3 Static Var Compensators with 2-level VSIs ([19] - [21]), which are also known as <u>Advanced Static Var Compensator</u> (ASVC), <u>STATic CON</u>denser (STATCON) or <u>STATic COM</u>pensator (STATCOM). The numerous advantages of an ASVC compared to a SVC with conventional thyristors is discussed in detail in e.g. [9] and [23] - [25].

Another topology, a Unified Power Flow Controller (UPFC), being the most versatile FACTS device, is presently under development and is going to be commissioned in the near future ([26] - [29]).

It can be expected that the 2nd and further generations of FACTS controllers will probably influence the development of future transmission systems to a large extent. This statement might be augmented by the fact that permanent improvements in the inverter and semiconductor technology can be expected, which will promise even faster control performance, lower losses and hopefully also lower prices.

With respect to the latter mentioned, the major disadvantage of the second generation of FACTS controllers is definitely their higher price compared to conventional equipment. This has to be seen as one of the main reasons why many utilities, at least in Europe, are still hesitating to integrate these powerful controllers in existing AC-systems. Therefore, a remarkable reduction of the costs for FACTS devices must be acknowledged as an important goal for future developments.

1.4 2-level VSI versus 3-level VSI

Quite a few different second generation FACTS topologies have been proposed yet, which are also intended to fulfil different tasks. However, all these different controllers have a common heart, which is, as mentioned above, the well known Voltage Source Inverter (VSI), equipped with GTO thyristors. The flexibility of the VSI for FACTS applications may be utilized in a modular design, which at the end could also reduce the engineering costs ([5]).

Further savings could be achieved by an extended version of the 2-level VSI, the so called 3-level VSI, which has been proposed some years ago and which is meanwhile quite well established in high power drives and traction applications (figure 1.1 e).

In comparison to the 2-level VSI, where the output terminals are either con-

nected to the positive or to the negative pole of the DC-side voltage, the 3level VSI is capable to contribute with 3 different potentials in its output voltages. Except of the positive and the negative pole of the DC-side voltage, also the DC-side mid-point voltage can be connected to the AC-side terminals. For that purpose, two capacitors are installed on the DC-side (instead of one for the 2-level VSI), whose midpoint potential represents the additional level of the 3-level VSI output voltages.

This 3-level VSI topology has a remarkable benefit in comparison to the 2-level VSI:

• due to the additional third potential, the 3-level VSI output-voltages can be much better synthesized to a pure sinusoidal waveform, which yields a reduced harmonic distortion. This in its turn will save the costs for ACside filters.

Hence, the 3-level VSI might be an interesting alternative for the 2-level VSI, which especially could contribute to the cost reduction, being essential for the attractiveness of modern FACTS controllers.

1.5 Scope of the thesis

Despite the two main advantages described in the previous chapter, there are still no practical experiences with the 3-level VSI in the field of high power FACTS applications, except of some small scale laboratory models for an ASVC and HVDC ([30] - [32]). This is moreover manifested by the fact that on second sight, the 3-level VSI also shows up some inherent drawbacks compared to the 2-level VSI, which ask for more serious investigations.

To analyse these 3-level VSI disadvantages and to make solution proposals is within the scope of this thesis.

Further, studies with regard to general 3-level VSI attributes and suitable modulation and control schemes will also be addressed in this work. For that purpose, the first two chapters cover the following topics:

- derivation of the general valid instantaneous 3-level VSI equations and
- requirements and investigations of appropriate 3-level VSI modulation functions.

One remarkable disadvantage of the 3-level VSI consists in an increased voltage stress for the DC-side capacitors because of the oscillating neutral

point potential, which cannot be avoided if the capacitors are not chosen too large. Therefore this thesis also includes a

- general harmonic analysis, showing the harmonic orders of all individual 3-level VSI quantities both for symmetrical and asymmetrical operation conditions, which is followed by
- investigations concerning the dependancy of the 3-level VSI specific DC-side harmonics on the operation mode and modulation scheme as well as on the switching frequency.

Another serious problem to have a closer look at is with respect to the balance of the two DC-side voltages. Ideally, these two voltages are assumed to be balanced, i.e. they contribute with the same DC-values. However, for several reasons, unbalance occurs, which results in an extra voltage stress for the semiconductor switches and capacitors and also introduces highly undesirable even numbered harmonics on the AC-side. In order get a better understanding for these phenomenons and also to find appropriate solutions, in particular the following topics are of high interest and will be studied in this thesis:

- self-balancing attributes of the 3-level VSI
- sources for a DC-side unbalance and their impact
- DC-side balancing control schemes

A further crucial point concerns the control of the 3-level VSI, both under symmetrical and asymmetrical AC-system conditions. The hereby arising problems are also present for the 2-level VSI and therefore, suitable control schemes for the 3-level VSI can also be applied to the 2-level VSI.

Especially during AC-system disturbances, the VSI is expected to provide support for the AC-system and thus, a disconnection is highly undesirable. Unfortunately, the 3-level VSI behaviour during asymmetrical AC-system conditions, e.g. line faults or voltage sags, is very critical, if no additional controller is implemented. In occurrence of these faults, the currents and voltages in the VSI might take on values of several times of the nominal rated values. This means to disconnect the device from the AC-system, since an overdimensioning to that extent cannot be tolerated from an economic point of view.

Hence, the need arises for appropriate fast control schemes to keep the VSI quantities in between reasonable boundaries during asymmetrical AC-system conditions, without the urge of disconnection.

The thesis under consideration also deals with this topic according to the following approach:

- derivation of the dynamic phasor equations of the 2- and 3-level VSI connected to an AC-system, also including the dynamics of the AC-system itself,
- influence of the different control variables and disturbance variables on the 2- or 3-level VSI system quantities and control performance,
- derivation of a 2- or 3-level VSI control scheme for a symmetrical AC-system,
- derivation of a 2- or 3-level VSI feed-forward controller with current limiter under asymmetrical AC-system conditions.

All general investigations performed are verified on a 3-level VSI SVC-example (ASVC), which might be the most promising application to be built and demonstrated in the near future.

Finally it should be emphasized that this thesis is exclusively focusing on a general analysis and on basic control schemes of the 3-level VSI topology. This does not include studies with respect to the various benefits, which this topology could provide for an AC-system (power flow control, stability enhancement or damping characteristics of the 3-level VSI). For that purpose the reader is referred to the literature cited in the previous chapters.

ţ

2 The 3-level VSI in transmission applications

2.1 Overview

In this chapter the 3-phase 3-level Voltage Source Inverter (3-level VSI) circuit and the principles of its operation are introduced.

Further, a mathematical analysis of the 3-phase 3-level VSI connected to a 3-phase AC-system is presented.

Hereby, the instantaneous equations of the 3-phase 3-level VSI are derived, both on the AC- and the DC-side. These equations will also include the interactions of the AC- with the DC-side and vice versa. The analysis is performed in a most general way and valid for all applications and modulation methods.

It will be shown that, compared to the 3-phase 2-level VSI, additional equations have to be taken into account for the 3-phase 3-level VSI topology.

2.2 The 3-level VSI circuit and basic operation principles

The 3-phase 3-level VSI, which from now will shortly denoted 3-level VSI, is an extended version of the 3-phase 2-level VSI (shortly: 2-level VSI) and will be discussed in this chapter. Concerning the 2-level VSI, it is presumed that the reader is confident with the topology and its operating principle, which is well described in power electronics literature (e.g. [33] - [35]). The circuit of the 3-level VSI is shown in figure 2.1.

Each phase ph=a,b,c of the 3-level VSI is built up of 4 semiconductor switches $(s1_{ph}...s4_{ph})$ and two additional clamping diodes $(d1_{ph},d2_{ph})$.

Every switch, as indicated in figure 2.1 for $s1_a$ (dotted box), consists of a semiconductor turn-off device (e.g. GTOs or IGBTs) and an antiparallel diode. With that, the phase currents $i_{a,b,c}$ may flow in both directions from the AC(DC)- to the DC(AC)-side.

The connection of each phase with the midpoint of the DC-side (Neutral Point NP) via the clamping diodes $d1_{ph}$ and $d2_{ph}$ assures, that the maximum



fig 2.1: The 3-level VSI circuit represented with GTO valves

voltage across each valve does not exceed the individual DC-side voltages u_{D1} or u_{D2} respectively. It should be mentioned at this point, that the DC-components of u_{D1} and u_{D2} are expected to take on the same value.

The output terminals a,b,c can either be connected to the positive DC-side potential u_{D1} , to 0 (the Neutral Point NP) or the negative DC-side potential u_{D2} according to the on/off states of $s1_{ph}...s4_{ph}$ shown in table 2.1.

u _{a,b,c}	s1 _{a,b,c}	s2 _{a,b,c}	s3 _{a,b,c}	s4 _{a,b,c}
u _{D1}	on	on	off	off
0	off	on	on	off
-u _{D2}	off	off	on	on

table 2.1: 3-level VSI output voltages $u_{a,b,c}$ in dependency on the on/ off-states of the turn-off devices $s_{1,2,3,4}$, $a_{a,b,c}$

"On" in table 2.1 means that the turn-off device of the corresponding switch is conducting, while "off" means that the turn-off device is blocking. Compared with the 2-level VSI an additional potential (the midpoint voltage of the two DC-voltages u_{D1} and u_{D2}) can be connected to the AC-terminals. Other on/off-combinations than those shown in table 2.1 for the turn-off devices of $s1_{ph}...s4_{ph}$ are not allowed.

Further it has to be ensured that two consecutive switching actions do not include a transition from $u_{ph} = u_{D1}$ to $u_{ph} = -u_{D2}$ or vice versa, since simultaneously firing or blocking of adjacent series connected devices might result in a critical voltage stress to the valves. Therefore the output voltages u_{ph} have to be controlled according to table 2.2.

actual state: u _{a,b,c} =	next permissible transition: $u_{a,b,c} =$
u _{D1}	0
0	u_{D1} or $-u_{D2}$
-u _{D2}	0

table 2.2: permissible transitions of the 3-level VSI output voltages $u_{a.b.c}$ in dependancy on their actual state

From table 2.2 and table 2.1 one can see, that via the additional potential 0 the advantages of a series connection (increase of the rated power) can be achieved without suffering the drawbacks (two adjacent turn-off devices are switched simultaneously).

An in depth analysis of the conduction and switching losses was not performed in this thesis. However, it can be assumed that basing on the rated power of the 2- and 3-level topologies, the losses of the 3-level VSI are slightly higher than those of the 2-level topology. This will mainly be caused by the more complex snubber circuits for the 3-level VSI, necessary to ensure maximum di/dt and du/dt-values for the individual valves. Nevertheless, as mentioned yet, this will not further be investigated here.

Depending on the sign of the phase currents i_{ph} , either the turn-off device or the antiparallel diode of a switch is conducting. The clamping diodes $d1_{ph}$ and $d2_{ph}$ only carry the current, if the NP is connected to the AC-side terminals. This is summarized in table 2.3 for the 3 possible output voltages $u_{ph} = u_{D1}$, 0, $-u_{D2}$.

Compared to the 2-level VSI, there are also some drawbacks, which are listed below and proved in the following chapters:

- higher voltage/current stresses for the switches and DC-side capacitors depending on the capacitors' size (discussed in chapter 6).
- drift of the neutral point NP on the DC-side (discussed in chapter 7).

$u_{ph} = u_{D1}$	path of the phase current i_{ph} from the AC- to the DC-side terminal via
$i_{ph} > 0$	$s1_{ph}$ (antiparallel Diode) and $s2_{ph}$ (antiparallel Diode)
i _{ph} < 0	$s1_{ph}$ (turn-off device) and $s2_{ph}$ (turn-off device)
u _{ph} = 0	path of the phase current i _{ph} from the AC- to the DC- side terminal via
i _{ph} > 0	s_{ph}^{3} (turn-off device) and d_{ph}^{2} (clamping diode)
i _{ph} < 0	$s2_{ph}$ (turn-off device) and $d1_{ph}$ (clamping diode)
$u_{ph} = -u_{D2}$	path of the phase current i _{ph} from the AC- to the DC- side terminal via
i _{ph} > 0	s3 _{ph} (turn-off device) and s4 _{ph} (turn-off device)
i _{ph} < 0	$s3_{ph}$ (antiparallel Diode) and $s4_{ph}$ (antiparallel Diode)



However, since the above mentioned lacks can be compensated by means of an appropriate design and control measures, the 3-level VSI is very interesting for many high power applications.

For further investigations, each phase of the 3-level VSI will be represented by an ideal change-over switch, as shown in figure 2.2.



fig 2.2: change-over switch representation of a 3-level VSI phase

This simplification is established by the fact, that this thesis concentrates on the system performance (including the AC-system and controls), rather than the behaviour of the individual semiconductors.

2.3 Model of the 3-level VSI in transmission applications

2.3.1 Topology

A model of the 3-level VSI, which is connected in shunt to an ideal AC-system, is shown in figure 2.3. Though the main application investigated in this



fig 2.3: simplified model of a 3-level VSI connected to an AC-system represented with ideal switches

thesis, a SVC, does not ask for any energy source or sink on the DC-side (e.g. another VSI (back to back), a DC-line etc.), it is nevertheless included here. This is due to the fact that all theoretical investigations are performed in a most general way. Exclusively the validity of the achieved results will be verified by means of a SVC-example.

Whenever we exclusively focus on the SVC application of the 3-level VSI, the DC-side source or sink will be omitted.

2.3.2 Notation of the quantities

The quantities are written in [p.u.] notation according to appendix A.1.2. Hereby, all voltages are related to the nominal fundamental amplitude U_L of the AC-system voltages u_{Lph} , ph=a,b,c. The currents in its turn are referred to the nominal fundamental amplitude I_1 of the 3-level VSI out-

put currents i_{ph} . The nominal impedance is defined by the quotient of the just mentioned nominal voltage and nominal current amplitudes and is the basis for the [p.u.] representation of the passive components. All p.u. quantities are written in *italic* style. Further, constant amplitude values are indicated by upper-case characters, while quantities varying in time are described by lower-case letters throughout this thesis.

2.3.3 AC-system voltages

The AC-system generator voltages u_{Gph} , ph = a,b,c, are represented by a set of 3 ideal stiff and cosinusoidal AC-sources. This can be written as

$$u_{Gph} = U_{Gph} \cdot \cos(\omega_1 t + D_{ph}); \quad \omega_1 = 2\pi f_1$$
(2.1)

where U_{Gph} denote the amplitudes and D_{ph} the phase-displacements between the 3 phases ph = a,b,c. ω_1 is the fundamental angular frequency and f_1 the fundamental frequency of the AC-system.

In a symmetrical AC-system the amplitudes have the same value in all 3 phases and the phase-displacements differ by $2/3 \cdot \pi$:

$$U_{Ga} = U_{Gb} = U_{Gc} = U_G$$
(2.2)

$$D_a = 0$$
 $D_b = -2/3 \cdot \pi$ $D_c = 2/3 \cdot \pi$ (2.3)

The AC-system voltages at the primary terminals of the converter transformer are represented by u_{Lph} , ph = a,b,c.

2.3.4 Passive components

The resistance r_L stands for the total losses and l_L for the total inductance of the AC-lines.

The resistance r corresponds to the transformer losses, also including the 3level VSI losses, while the inductance l equals the transformer stray inductance.

The DC-side capacitances c are assumed to be equal, however the voltages u_{D1} and u_{D2} across them might have different instantaneous values.

2.3.5 Switching functions

The values are modelled as ideal change-over switches and are described by the switching functions s_{pk} , which only can take on 3 values

according to the convention in eqn. (2.4).

 $s_{ph} = 1$, if the phase *ph* is connected to the upper capacitor *c*, (2.4) $s_{ph} = 0$, if the phase *ph* is connected to the neutral point *NP*, $s_{ph} = -1$, if the phase *ph* is connected to the lower capacitor *c*.

The most simple switching function s_{ph} , where each value of the 3-level VSI is switched on and off only once per period, is denoted Fundamental Frequency Modulation (FFM) and is presented for phase a in figure 2.4.



fig 2.4: switching function s_a of phase a for Fundamental Frequency Modulation (FFM) and definition of the Neutral Point (NP)-angle β

Herein, also the <u>Neutral Point</u> (NP)-angle β is introduced, which corresponds to the time segments where the neutral point NP is connected to the output terminals. This NP angle β fulfils two different tasks:

• adjustment of the modulation index m, which is defined as the amplitude of the fundamental component of s_{ph} (chapter 3.3.3, eqn. (3.1)). For FFM modulation, m can be expressed by $m = 4/\pi \cdot \cos\beta$. With that a large modulation index is achieved for small values of β , while a small modulation index is the result of a large NP angle β . It can be seen in figure 2.4, that the maximum value for β is $\beta = \pi/2$, which equals to m = 0. Hence, the NP-angle β also can be seen as a degree of freedom for the control of the 3-level VSI. • with an appropriate choice of β , harmonics in s_{ph} can be eliminated or minimized. A more detailed description of this optimization is given in chapter 3.4.

Finally it should be pointed out, that the 3-level VSI FFM switching functions s_{ph} also can be decomposed in a sum of two identical 2-level VSI FFM switching functions, which both are phase-displaced by an angle β in opposite directions. This graphical decomposition is shown more in detail in appendix B.2.1.

Now the instantaneous equations of the whole system will be derived in the next chapter basing on the assumptions made so far.

2.4 3-level VSI system equations

This chapter provides the derivation of the system equations for the 3-level VSI connected in shunt to an AC-system (figure 2.3).

Hereby, also the interaction of the 3-level VSI AC-side with the DC-side quantities and vice versa will be taken into account. This interaction cannot be neglected, when small DC-side capacitors have to be assumed, as it is a must in transmission applications (price!).

The procedure to perform this analysis is based on a 'closed loop' shown in (figure 2.5), which graphically describes the relationships between the



fig 2.5: 'closed loop' for the quantities of the 3-level VSI, which is connected in shunt to an AC-system

quantities of the system under investigation (figure 2.3).

Herein, the switching functions s_{ph} and their squared values s_{ph}^2 or their absolute values $|s_{ph}|$ respectively constitute the "interface"-variables, which determine the interaction of the DC-side (left half of figure 2.5) with the AC-side (right half of figure 2.5).

The DC-side voltages u_{D1} and u_{D2} , modulated with s_{ph} and s_{ph}^2 or $|s_{ph}|$, will be reflected to the AC-side as the 3-level VSI output voltages u_{ph} , ph=a,b,c (chapter 2.4.1).

The impressed 3-level VSI AC-side voltages u_{ph} , together with the AC-system voltages u_{Lph} , will be the driving force for the AC-side currents i_{ph} (chapter 2.4.2).

These AC-side currents i_{ph} , modulated with s_{ph} and s_{ph}^2 or $|s_{ph}|$, will result in the impressed 3-level VSI DC-side currents i_{D1} , i_{D2} and i_0 (chapter 2.4.3).

Finally, the DC-side currents i_{D1} , i_{D2} and i_0 will generate the DC-side voltages u_{D1} and u_{D2} across the capacitors c (chapter 2.4.3). With that, the loop is closed.

Last but not least, it should be mentioned that the above described closed loop will also be the basis for the qualitative harmonic analysis presented in chapter 4.

2.4.1 3-level VSI equations on the AC-side

First, the 3-level VSI output voltages u_{ph} will be presented, which can be described by eqn. (2.5) or eqn. (2.6).

$$u_{ph} = \frac{(s_{ph} + 1) \cdot s_{ph}}{2} \cdot u_{D1} - \frac{(s_{ph} - 1) \cdot s_{ph}}{2} \cdot u_{D2}$$
(2.5)

$$u_{ph} = \frac{s_{ph} + |s_{ph}|}{2} \cdot u_{D1} + \frac{s_{ph} - |s_{ph}|}{2} \cdot u_{D2}$$
(2.6)

Both equations fulfil the convention eqn. (2.4) for the switching functions s_{pk} , which can be verified with the help of figure 2.3. Though astonishing on first sight, this can be explained by the fact that the squared value and the absolute value of quantities, which exclusively equal to -1, 0, and +1 (eqn. (2.4)), will always be identical.

For sure, this will be subject to change, if the switching functions s_{ph}

for simplicity reasons are approximated by e.g. their fundamental component, which will be discussed more in depth in chapter 2.5.

Finally it should be mentioned, that the representation by means of the absolute value $|s_{ph}|$ (eqn. (2.6)) mathematically coincides with the approach of two 3-level VSI switching functions in each phase a,b,c (one for the upper and one for the lower 3-level VSI valves, [30]).

Rewriting eqn. (2.5) and eqn. (2.6) yields eqn. (2.7) and eqn. (2.8).

$$u_{ph} = \frac{s_{ph}}{2} \cdot (u_{D1} + u_{D2}) + \frac{s_{ph}^2}{2} \cdot (u_{D1} - u_{D2})$$
(2.7)

$$u_{ph} = \frac{s_{ph}}{2} \cdot (u_{D1} + u_{D2}) + \frac{|s_{ph}|}{2} \cdot (u_{D1} - u_{D2})$$
(2.8)

It should be emphasized that eqn. (2.7) and eqn. (2.8) also include the case of unbalanced DC-side voltages u_{D1} and u_{D2} .

With

$$(u_{D1} + u_{D2}) = u_{Dsum}$$
 and $(u_{D1} - u_{D2}) = u_{Ddiff}$ (2.9)

eqn. (2.7) and eqn. (2.8) can finally be written as eqn. (2.10) and eqn. (2.11).

$$u_{ph} = \frac{s_{ph}}{2} \cdot u_{Dsum} + \frac{s^2_{ph}}{2} \cdot u_{Ddiff}$$
(2.10)
or
$$u_{ph} = \frac{s_{ph}}{2} \cdot u_{Dsum} + \frac{|s_{ph}|}{2} \cdot u_{Ddiff}$$
(2.11)

It is an interesting result, that u_{ph} both depends on the sum u_{Dsum} and the difference u_{Ddiff} of the two DC-side voltages u_{D1} and u_{D2} . While the first summand in eqn. (2.7)-eqn. (2.11) is well known from the 2level VSI, the second one exclusively contributes to the 3-level VSI topology.

At this point it has to be noted that this second summand in eqn. (2.7) or eqn. (2.10) is of major importance for further investigations and must not be neglected. Especially the following two topics can only be explained by referring to the term being a function of the difference
u_{Ddiff}:

- analysis of the DC-side self-balancing behaviour of the 3-level VSI, which will be shown in chapter 7.4.
- appearance of specific harmonic orders in the AC-side currents despite their elimination in the switching functions s_{ph} , which will be discussed in chapter 6.4

Therefore it makes sense to split u_{ph} into two parts u_{phsum} and u_{phdiff} according to

$$u_{ph} = u_{phsum} + u_{phdiff} \tag{2.12}$$

with

$$u_{phsum} = \frac{s_{ph}}{2} \cdot (u_{D1} + u_{D2}) = \frac{s_{ph}}{2} \cdot u_{Dsum}$$
(2.13)

and

$$u_{phdiff} = \frac{s_{ph}^2}{2} \cdot (u_{D1} - u_{D2}) = \frac{s_{ph}^2}{2} \cdot u_{Ddiff}$$
(2.14)

or

$$u_{phdiff} = \frac{|s_{ph}|}{2} \cdot (u_{D1} - u_{D2}) = \frac{|s_{ph}|}{2} \cdot u_{Ddiff}$$
(2.15)

Both parts u_{phsum} and u_{phdiff} contribute to the harmonics on the AC-side, which will be analysed in chapter 4.

In a next step, the system equations on the AC-side, which determine the AC-side currents i_{nh} , will mathematically be described.

2.4.2 System equations on the AC-side

The Kirchhoff law applied to the AC-side of the system in figure 2.3 yields eqn. (2.16).

$$u_{Gph} + u_{SP} = u_{Zph} + u_{ph} \tag{2.16}$$

The voltages u_{Zph} across the AC-system impedance and the decoupling impedance, consisting of r and l, can be expressed by

$$u_{Zph} = (r_L + r) \cdot i_{ph} + (l_L + l) \cdot \frac{di_{ph}}{dt} = r_{tot} \cdot i_{ph} + l_{tot} \cdot \frac{di_{ph}}{dt}$$

Inserting u_{Zph} in eqn. (2.16) results in the system equation (eqn. (2.17)).

$$u_{Gph} + u_{SP} = r_{tot} \cdot i_{ph} + l_{tot} \cdot \frac{di_{ph}}{dt} + u_{ph}$$
(2.17)

According to eqn. (2.12) $(u_{ph} = f(u_{phsum}, u_{phdiff}))$, the currents i_{ph} will also be split in two terms:

$$i_{ph} = i_{phsum} + i_{phdiff} \tag{2.18}$$

The first term i_{phsum} in eqn. (2.18) is generated by the AC-system generator voltages u_{Gph} and the term u_{phsum} of the inverter output voltages. The second term i_{phdiff} is generated only by means of u_{phdiff} .

Therefore eqn. (2.17) can be written as eqn. (2.19) and eqn. (2.20), where u_{SPsum} and u_{SPdiff} denote the zero-sequence voltages originated by u_{phsum} , u_{phdiff} and u_{Gph} (eqn. (2.21), eqn. (2.22)).

$$u_{Gph} + u_{SPsum} = r_{tot} \cdot i_{phsum} + l_{tot} \cdot \frac{di_{phsum}}{dt} + u_{phsum}$$
(2.19)

$$0 + u_{SPdiff} = r_{tot} \cdot i_{phdiff} + l_{tot} \cdot \frac{di_{phdiff}}{dt} + u_{phdiff}$$
(2.20)

$$u_{SPsum} = \frac{1}{3} \cdot \left[(u_{asum} + u_{bsum} + u_{csum}) - (u_{Ga} + u_{Gb} + u_{Gc}) \right] \quad (2.21)$$

$$u_{SPdiff} = \frac{1}{3} \cdot (u_{adiff} + u_{bdiff} + u_{cdiff})$$
(2.22)

Note: for symmetrical ideal cosinusoidal AC-system generator voltages u_{Gph} , the second summand in eqn. (2.21) $(u_{Ga} + u_{Gb} + u_{Gc})$ equals 0 for all time instants.

Performing this separation of the voltages and the currents makes sense since it is now easier to assess their individual contributions with regard to the harmonics or, which will be shown in chapter 7.4 and chapter 8.4.1, to the DC-side self-balancing and DC-side balancing control.

2.4.3 3-level VSI equations on the DC-side

The equations for the DC-side currents i_{D1} and i_{D2} as a function of the AC-side currents i_{ph} and the switching functions s_{ph} and s_{ph}^2 or $|s_{ph}|$ respectively are given by eqn. (2.23) - eqn. (2.26).

$$i_{D1} = i_{a} \cdot s_{a} \frac{s_{a} + 1}{2} + i_{b} \cdot s_{b} \frac{s_{b} + 1}{2} + i_{c} \cdot s_{c} \frac{s_{c} + 1}{2}$$
(2.23)

$$= \frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot s_{ph} + \sum_{ph = a,b,c} i_{ph} \cdot s^{2}_{ph} \right)$$
or

$$i_{D1} = i_{a} \cdot \frac{|s_{a}| + s_{a}}{2} + i_{b} \cdot \frac{|s_{b}| + s_{b}}{2} + i_{c} \cdot \frac{|s_{c}| + s_{c}}{2}$$
(2.24)

$$= \frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot s_{ph} + \sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}| \right)$$

$$i_{D2} = i_{a} \cdot s_{a} \frac{s_{a} - 1}{2} + i_{b} \cdot s_{b} \frac{s_{b} - 1}{2} + i_{c} \cdot s_{c} \frac{s_{c} - 1}{2}$$
(2.25)

$$= \frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot s_{ph} - \sum_{ph = a,b,c} i_{ph} \cdot s^{2}_{ph} \right)$$
or

$$i_{D2} = i_{a} \cdot \frac{|s_{a}| - s_{a}}{2} + i_{b} \cdot \frac{|s_{b}| - s_{b}}{2} + i_{c} \cdot \frac{|s_{c}| - s_{c}}{2}$$
(2.26)

$$= \frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot s_{ph} - \sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}| \right)$$

Again the reader is invited to verify their validity with the help of figure 2.3 and the convention eqn. (2.4) for the switching functions s_{ph} .

Further, for the calculation of u_{Dsum} (eqn. (2.36)), the difference i_{Ddiff} of the two DC-side currents i_{D1} and i_{D2} will be a helpful auxiliary variable, which is calculated in eqn. (2.27).

$$i_{Ddiff} = i_{D1} - i_{D2} = i_a \cdot s_a + i_b \cdot s_b + i_c \cdot s_c = \sum_{ph = a,b,c} i_{ph} \cdot s_{ph} \quad (2.27)$$

In the same way the NP-current $i_0 (= -(i_{D1} + i_{D2}))$ can be expressed according to eqn. (2.28) or eqn. (2.29).

$$i_0 = i_a \cdot (1 - s_a^2) + i_b \cdot (1 - s_b^2) + i_c \cdot (1 - s_c^2)$$
(2.28)

or

$$i_0 = i_a \cdot (1 - |s_a|) + i_b \cdot (1 - |s_b|) + i_c \cdot (1 - |s_c|)$$
(2.29)

Since $i_a + i_b + i_c = 0$ is true for all time instants, eqn. (2.28) and eqn. (2.29) can be simplified to eqn. (2.30) and eqn. (2.31).

$$i_{0} = -(i_{a} \cdot s_{a}^{2} + i_{b} \cdot s_{b}^{2} + i_{c} \cdot s_{c}^{2}) = -\sum_{ph = a,b,c} i_{ph} \cdot s_{ph}^{2}$$
(2.30)
or
$$i_{0} = -(i_{a} \cdot |s_{a}| + i_{b} \cdot |s_{b}| + i_{c} \cdot |s_{c}|) = -\sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}|$$
(2.31)

It should be emphasized here, that a closer look at eqn. (2.30) or eqn. (2.31) yields valuable results about the DC-side self-balancing behaviour of the 3-level VSI and is also very helpful for the analysis of a DC-side balance control scheme for SVC-applications. This will be performed in chapter 7.4 and chapter 8.4.1.

Further, it is an interesting fact, that i_0 does not depend on the DC-side load current i_D , but only on i_{D1} and i_{D2} :

$$i_0 = -[(i_{D1} + i_D) + (i_{D2} - i_D)] = -(i_{D1} + i_{D2})$$
(2.32)

ł

The DC-side voltages u_{D1} and u_{D2} are a function of the currents i_{D1} , i_{D2} and i_D , which are flowing through them:

$$i_{D1} + i_D = c \cdot \frac{du_{D1}}{dt}$$
 $i_{D2} - i_D = -c \cdot \frac{du_{D2}}{dt}$ (2.33)

Solving eqn. (2.33) for the individual DC-side voltages u_{D1} and u_{D2} results in eqn. (2.34) and eqn. (2.35).

$$u_{D1} = \frac{1}{c} \int (i_{D1} + i_D) dt + const$$
(2.34)

$$u_{D1} = \frac{1}{c} \int \left(\frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot s^2_{ph} + \sum_{ph = a,b,c} i_{ph} \cdot s_{ph}\right) + i_D\right) dt + const$$
or

$$u_{D1} = \frac{1}{c} \int \left(\frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}| + \sum_{ph = a,b,c} i_{ph} \cdot s_{ph}\right) + i_D\right) dt + const$$
(2.35)

$$u_{D2} = -\frac{1}{c} \int \left(\frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot s^2_{ph} - \sum_{ph = a,b,c} i_{ph} \cdot s_{ph}\right) - i_D\right) dt + const$$
or

$$u_{D2} = -\frac{1}{c} \int \left(\frac{1}{2} \cdot \left(\sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}| - \sum_{ph = a,b,c} i_{ph} \cdot s_{ph}\right) - i_D\right) dt + const$$
or

The sum u_{Dsum} and the difference u_{Ddiff} of the two DC-side voltages u_{D1} and u_{D2} can now be calculated according to eqn. (2.36) and eqn. (2.37).

$$u_{D1} + u_{D2} = u_{Dsum} = \frac{1}{c} \int (i_{D1} - i_{D2} + 2i_D) dt + const$$
(2.36)
$$u_{D1} + u_{D2} = u_{Dsum} = \frac{1}{c} \int (i_{Ddiff} + 2i_D) dt + const$$

$$u_{D1} + u_{D2} = u_{Dsum} = \frac{1}{c} \int \left(\sum_{ph = a,b,c} i_{ph} \cdot s_{ph} + 2i_D \right) dt + const$$

It should be noted, that the sum $u_{D1} + u_{D2}$ depends on the difference $i_{D1} - i_{D2}$, while $u_{D1} - u_{D2}$ is a function of $i_{D1} + i_{D2}$ (= $-i_0$).

More, from eqn. (2.37) it can be concluded, that the individual DC-side voltages u_{D1} and u_{D2} will not have identical instantaneous values, since the NP-current i_0 cannot be assumed to equal 0 at each time instant.

$$u_{D1} - u_{D2} = u_{Ddiff} = \frac{1}{c} \int (i_{D1} + i_{D2})dt + const$$

$$u_{D1} - u_{D2} = u_{Ddiff} = -\frac{1}{c} \int i_0 dt + const$$

$$u_{D1} - u_{D2} = u_{Ddiff} = \frac{1}{c} \int \left(\sum_{ph = a,b,c} i_{ph} \cdot s^2{}_{ph} \right) dt + const$$
or
$$u_{D1} - u_{D2} = u_{Ddiff} = \frac{1}{c} \int \left(\sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}| \right) dt + const$$

With that, all quantities of the 3-level VSI, which is connected in shunt to an AC-system, are mathematically described.

Of course, these equations can also be applied to the 2-level VSI by defining $u_{D1} = u_{D2} = u_D/2$ (u_D = total 2-level VSI DC-voltage) and $s_{ph} = \pm 1$.

2.5 Accuracy of approximations for s_{ph}^2 and $|s_{ph}|$

It was shown in chapter 2.4, that the 3-level VSI DC- and AC-side quantities can be expressed in dependency on

- either the switching functions s_{ph} and their squared values s_{ph}^2
- or the switching functions s_{ph} and their absolute values $|s_{ph}|$.

If the switching functions s_{ph} are described by their exact values -1, 0, +1, it can easily be verified that s_{ph}^2 and $|s_{ph}|$ will be identical in each time instant: $s_{ph}^2 = |s_{ph}|$.

However, this might be subject to change, if an approximation will be chosen for s_{ph} in order to e.g. simplify a mathematical analysis. Then, the squared value of this approximation (s_{ph}^2) might no longer coincide with its absolute value $(|s_{ph}|)$. As a consequence the question will arise, which approximated quantity, s_{ph}^2 or $|s_{ph}|$, will yield more accurate results with respect to the calculation of the 3-level VSI quantities. The investigations to come will focus on an answer for this question.

2.5.1 Approximation of the switching functions by means of its fundamental component

In order to simplify mathematical analyses, the switching functions s_{ph} are often approximated by their fundamental component s_{ph1} according to eqn. (2.38).

$$s_{ph} \approx s_{ph1} = S_1 \cdot \cos(\omega_1 t + D_{ph} + \phi_u)$$
(2.38)

with

$$ph = a,b,c$$
 $D_a = 0, D_b = -2/3 \cdot \pi, D_c = 2/3 \cdot \pi$
and
 $\phi_{\mu} = \angle (u_{ab}, u_{Lab})$ (eqn. (4.1), chapter 4.3.1).

Applying eqn. (2.38) to s_{ph}^2 and $|s_{ph}|$ yields eqn. (2.39) and eqn. (2.40).

$$s_{ph}^{2} \approx s_{ph1}^{2} = (S_{1} \cdot \cos(\omega_{1}t + D_{ph} + \phi_{u}))^{2}$$

$$= \frac{1}{2}S_{1}^{2} \cdot \{1 + \cos[2(\omega_{1}t + D_{ph} + \phi_{u})]\}$$
(2.39)

$$\begin{aligned} |s_{ph}| \approx |s_{ph1}| &= |S_1 \cdot \cos(\omega_1 t + D_{ph} + \phi_u)| \\ &= \frac{2S_1}{\pi} \left\{ 1 - 2 \sum_{k=2,4...}^{\infty} \frac{1}{k^2 - 1} \cos(k\frac{\pi}{2}) \cos[k(\omega_1 t + D_{ph} + \phi_u)] \right\} \\ &|s_{ph1}| \approx \frac{2S_1}{\pi} \left\{ 1 + \left(\frac{2}{3} \cos[2(\omega_1 t + D_{ph} + \phi_u)] - \frac{2}{15} \cos[4(\omega_1 t + D_{ph} + \phi_u)]\right) \right\} \end{aligned}$$

Regarding the third line of eqn. (2.40), it is evident that $|s_{ph1}|$ constitutes an approximation of an approximation, since only the first 3 terms of the fourier row for the approximation $|s_{ph1}|$ have been taken into account. However, this additional simplification introduces a negligible error, since the higher ordered harmonics of $|s_{ph1}|$ (the 6th, 8th,...) exclusively contribute with (very) small amplitudes (1/35, 1/63, 1/99,...).

Finally, by comparing eqn. (2.39) with eqn. (2.40), it is obvious that these 2 different approximations will not yield the same results. Hence, it will be of high interest, which approximation $(s_{ph1}^2 \text{ or } |s_{ph1}|)$ will show up smaller deviations from the exact values of the 3-level VSI quantities.

This has been studied by means of simulations with MATLAB, where the

exact values for predominant NP-current harmonics (eqn. (2.30) and eqn. (2.31)) have been compared with the values achieved with the approximations presented in eqn. (2.39) and eqn. (2.40). Hereby, both switching functions s_{ph} with and without significant zero sequence systems (predominantly a 3rd harmonic) have been taken into account.

With respect to switching functions s_{pk} without significant zero sequence systems (especially a negligible 3rd harmonic), it could be seen that the approximation $|s_{pk1}|$ (eqn. (2.40)) yielded more accurate results than the approximation of s_{pk1}^2 (eqn. (2.39)). However, in case that the switching functions s_{pk} showed up significant zero sequence systems (predominantly a 3rd harmonic), both approximations $|s_{pk1}|$ and s_{pk1}^2 resulted in major deviations from the exact values of the NP-current harmonics.

Hence, it can be concluded that for switching functions s_{ph} with significant zero sequence systems (predominantly a 3rd harmonic), the approximation s_{ph1} has to be extended. This proves right at least for calculations concerning 3-level VSI DC-side quantities and will be performed in the chapter to come.

2.5.2 Approximation of the switching functions by means of its fundamental component and a 3rd harmonic zero sequence system

A more accurate approximation for switching functions s_{ph} with significant zero sequence systems (predominantly a 3rd harmonic) is given by eqn. (2.41).

$$s_{ph} \approx S_1 \cos(\omega_1 t + D_{ph} + \phi_u) + S_3 \cos[3(\omega_1 t + D_{ph} + \phi_u) + \phi_3] \quad (2.41)$$

Basing on eqn. (2.41), the calculation of s_{ph}^2 and $|s_{ph}|$ yields eqn. (2.42)

$$\begin{split} s_{ph}^2 &\approx \{S_1 \cos(\omega_1 t + D_{ph} + \phi_u) + S_3 \cos[3(\omega_1 t + D_{ph} + \phi_u) + \phi_3]\}^2 (2.42) \\ s_{ph}^2 &\approx \frac{1}{2} S_1^2 \{1 + \cos[2(\omega_1 t + D_{ph} + \phi_u)]\} + \\ &+ S_1 S_3 \{\cos[2(\omega_1 t + D_{ph} + \phi_u) + \phi_3] + \cos[4(\omega_1 t + D_{ph} + \phi_u) + \phi_3]\} + \\ &+ \frac{1}{2} S_3^2 \{1 + \cos[6(\omega_1 t + D_{ph} + \phi_u) + 2\phi_3]\} \end{split}$$

and eqn. (2.43).

$$|s_{ph}| \approx |S_1 \cos(\omega_1 t + D_{ph} + \phi_u) + S_3 \cos[3(\omega_1 t + D_{ph} + \phi_u) + \phi_3]| \quad (2.43)$$

In order to verify the accuracy of these approximations, the same simulations as in the previous chapter have been carried out for switching functions s_{ph} with significant zero sequence systems (predominantly a 3rd harmonic). The results can be summarized in the following statement:

For switching functions s_{ph} with significant zero sequence systems (predominantly a 3rd harmonic), the approximation of $|s_{ph}|$ (eqn. (2.43)) yields more accurate results than the approximation of s_{ph}^2 (eqn. (2.42)).

However, it has to be noted that for further analytical analyses (e.g. calculation of i_0 , see chapter 5.6.2), the approximation of s_{ph}^2 (eqn. (2.42)) will be better suited, though it will not be as accurate as the approximation of $|s_{ph}|$ (eqn. (2.43)). This is true, since the absolute value operation is not very well suited for analytical calculations and an additional simplification of eqn. (2.43) (e.g. a fourier row description) was found to be quite tricky for general values of S_1 , S_3 and ϕ_3 .

2.6 Summary

In this chapter the 3-level VSI circuit and its operation principle was introduced. It was shown that this topology can promise some economic and technical advantages compared to the 2-level VSI, especially in high power applications.

In a following step, the instantaneous equations of the 3-phase 3-level VSI connected in shunt to an AC-system have been derived. Hereby, also the interaction from the DC- to the AC-side and vice versa has been taken into account. This interaction is unavoidable for realistic small capacitor values and was briefly explained by means of a graphical closed loop model.

It could be seen from the resulting equations that the 3-level VSI output voltages are a function of both the sum u_{Dsum} and the difference u_{Ddiff} of the two individual DC-side voltages u_{D1} and u_{D2} .

Further, compared to the 2-level VSI, additional terms appeared in all equations for the 3-level VSI, which are a function of the squared switching - 45 -

functions s_{ph}^2 or the absolute value $|s_{ph}|$ of s_{ph} .

More, the equation for the Neutral Point current i_0 , which depends on the AC-side currents i_{ph} and the squared switching functions s_{ph}^2 or the absolute value $|s_{ph}|$ of s_{ph} , constitutes a new equation, which exclusively contributes to the 3-level VSI topology.

3 Modulation schemes

3.1 Overview

This chapter deals with 3-level VSI modulation schemes for high power transmission applications.

First, the requirements in transmission applications are presented, focusing hereby on the utilization of the 3-level VSI and the harmonic distortion of the AC-system. This is followed by a classification of the modulation methods and the requirements on the modulation signal attributes.

Basing on this, off-line optimized PWM and carrier based PWM are studied concerning their suitability to fulfil the particular demands.

Finally a comparison of both modulation schemes is performed, focusing hereby on the resulting utilization of the 3-level VSI and the harmonic pollution of the AC-system. This yields the interesting result, that carrier based PWM can compete with off-line-optimized PWM, if appropriate carrier based schemes are chosen!

3.2 Requirements in transmission applications

In comparison to low or medium power applications, high power transmission plants are very expensive and therefore savings of even a few percent are not negligible. Hence, it is highly desirable in transmission applications to utilize the VSI as much as possible. This means to minimize the power rating (and with that the prize) of the individual components (valves, capacitors etc.) with respect to a given power rating of the whole system.

Further, the demands for the harmonic distortion in a high power AC-transmission system are very strict. The individual harmonics of both the ACside currents i_{ph} and the AC-system voltages u_{Lph} often must not exceed values as small as 0.01 [p.u.]. Unfortunately, the VSI topology contributes to this harmonic pollution to a large extend, which is caused by the pulse shaped VSI output voltages. This especially is true, if the switching frequency of the VSI is low, which up to now proves right in transmission applications. Therefore normally large expensive filters have to be installed on the AC-side, which damp the harmonics produced by the VSI's output voltages. Minimizing these filters is another requirement in order to save the costs of the whole system.

Both the maximum utilization and the minimum harmonic pollution can effectively be influenced by appropriate modulation or switching functions s_{ph} . Therefore, the demands on a modulation scheme in transmission applications might slightly differ from those in low or medium power applications.

With regard to the statements made above, the requirements for a modulation scheme in transmission applications can be summarized as follows:

- a large modulation index m is highly desirable. As introduced in chapter 3.3.3, eqn. (3.1), m is defined as the amplitude of the fundamental component of the switching functions s_{ph} . A larger amplitude of the fundamental component of s_{ph} yields smaller resulting DC-side voltages and with that a smaller voltage stress for the valves and DC-side capacitors. Hence, a higher voltage utilization of the VSI can be achieved and the costs for the inverter can be reduced.
- a low harmonic content of the modulation functions is favourable, since this minimizes the costs of the filters on the AC-side. This is especially true, if some harmonics of the pulse patterns can be eliminated.
- low switching frequencies of the modulation functions (at most a few hundred Hz) are still a must in order to reduce the switching losses of the system and with that the operation costs.

It should be mentioned at this point, that in the near future the requirement of low switching frequencies might no longer be of that importance. Recent technological developments of the semiconductor switches like the high power IGBT or the hard driven GTO ([36]) also include a decrease of the device's switching losses. Therefore switching frequencies in the range between some hundred Hz up to 1kHz (or perhaps more) might be realistic in a few years, even in transmission applications.

Now that the requirements in transmission applications are derived, the question arises, which modulation schemes will be best suited to fulfil these demands. In order to answer this question, a classification of the different modulation schemes will be performed in the next chapter.

3.3 Classification of the modulation schemes

3.3.1 Asynchronous and synchronous modulation schemes

In general, modulation schemes can be classified in two large groups: synchronous and asynchronous schemes ([37]).

Synchronous methods yield periodic modulation signals and generate a discrete harmonic amplitude spectrum, where the harmonics are integer numbered multiples of the fundamental frequency. Synchronous methods include e.g. off-line optimized PWM and carrier based PWM with carrier frequencies being integer numbered multiples of the fundamental frequency.

Asynchronous schemes generate non-periodical modulation signals and are characterized by inter-harmonics, which are no longer integer numbered multiples of the fundamental frequency.

In high power transmission applications asynchronous modulation is highly undesirable, mainly because of the inter-harmonics in the switching functions s_{ph} . Therefore, the further investigations exclusively will focus on synchronous modulation schemes.

Speaking of synchronous modulation schemes, an additional classification concerning the symmetry of the pulse patterns can be performed, which will be discussed in the following sub-chapter.

3.3.2 Symmetry attributes

Concerning the synchronous modulation class, the symmetry of its individual pulse patterns might be of high importance, especially in transmission applications.

No symmetry at all will yield harmonics to arise, whose orders are odd and even numbered multiples of the fundamental frequency (incl. DC-components). Modulation signals with symmetries to half or a quarter of a period however only show up harmonic orders being odd numbered multiples of the fundamental frequency and the DC-component always equals to 0 [37].

It is evident, that the latter ones will be much better suited for transmission applications, where a large harmonic content, especially even numbered harmonics, is extremely undesirable. In addition it should be anticipated here, that even numbered harmonics with an appropriate phase sequence will cause a DC-component in the NP-current i_0 , which in its turn inherently results in an unbalance of the two DC-side voltages u_{D1} and u_{D2}

(chapter 7). Hence pulse patterns with no symmetry at all should not be chosen for 3-level VSI applications.

To proceed one step further, the choice of a switching function with a symmetry to a quarter of a period is highly recommendable. Though still not mathematically proven, it is an empiric fact, that pulse patterns with a symmetry to a quarter of a period always result in the best approximation of a pure cosinusoidal reference signal (here: the AC-system voltages u_{Lph}). This means that a minimum harmonic distortion (THD) will be achieved both for the AC-system voltages u_{Lph} and the AC-side currents i_{ph} .

Finally, it is desirable that the switching functions have the same shape in all 3 phases a,b,c. It is then ensured that all harmonics being multiples of 3 constitute zero sequence systems. Assuming that the secondary transformer starpoint S is not connected with the midpoint NP on the DC-side (figure 2.3), these harmonics will ineffectively drop over S and NP and will therefore not generate harmonics of these orders in the AC-side currents i_{ph} .

With that the desirable attributes of modulation signals for transmission applications are derived and can be summarized as follows:

- the chosen modulation signals should belong to the class of synchronous modulation schemes
- they should have a symmetry to a quarter of a period, since this guarantees the lowest THD both for the AC-system voltages u_{Lph} and the AC-side currents i_{ph}
- they should have the same shape in all 3 phases a,b,c, since then all harmonics being multiples of 3 constitute zero sequence systems and will not contribute to the AC-side currents i_{ph} .

3.3.3 Investigated modulation schemes, switching frequencies and definition of the modulation index

The most common modulation schemes, which can fulfil these demands, are off-line optimized and carrier based PWM, which will be discussed and compared in the chapters to come. This hopefully might answer the question, which method is better suited for transmission applications.

Concerning the pulse patterns' switching frequencies f_{s_p} , quite a large range between $f_{s_p} = 50$ Hz (FFM) and $f_{s_p} = 1450$ Hz will be covered both for off-line optimized and carrier based PWM. Though switching frequencies larger than a few hundred Hz are presently not realistic in transmission applications, they might be in the future.

Further, it should be noted that the switching frequency $f_{s_{ph}}$ of a pulse pattern equals the switching frequency of each 3-level VSI valve.

The modulation index m of the switching functions s_{ph} is defined according to eqn. (3.1):

Definition of the modulation index:

 $m = S_1;$ $S_1:$ amplitude of the switching functions' (3.1) fundamental component

Finally, the fundamental frequency of the AC-system is assumed to be $f_1=50$ Hz throughout this thesis. According to appendix A.1.2, also the switching frequency $f_{s_{ph}}$ will be transformed to per unit representation $f_{s_{ph}}$ with a reference frequency $f_{ref}=f_1=50$ Hz.

3.4 Off-line optimized PWM (incl. FFM)

3.4.1 Introduction

Off-line optimized PWM includes all pulse patterns, whose switching instants are off-line calculated and then storaged in an existing modulator hardware. Speaking of 3-level VSI switching functions, it should be emphasized, that also Fundamental Frequency Modulation (FFM), belongs to this class of modulation schemes as the simplest representative.

The non-linear methods used to perform these optimizations will not be discussed in depth in this thesis. They originate from the economic mathematical field (operations research), but are also very well suited for the kind of task described in this chapter. For more detailed informations on the algorithms and its application, the reader is referred to e.g. [37] - [40].

The results presented in this thesis are basing on an extended version of a computer program, which was written during a diploma work at ETH with the simulation tool MATLAB ([38]). Especially the mathematical optimization toolbox provided with MATLAB ([41]) was found to be very helpful.

Hereby, optimization criterias are chosen, which are well suited for transmission applications according to chapter 3.2 and chapter 3.3. In detail, this will be discussed in the following.

3.4.2 Optimization criterias for transmission applications

In chapter 3.2, the requirements in transmission applications were derived. In order to fulfil these demands in a best suitable way, the distinctive optimization criterias for off-line optimized PWM will be shortly presented and the most appropriate ones will be chosen.

The criterias for the optimization of switching functions s_{ph} are varying and strongly depend on the application.

In general, it is possible to maximize the modulation index m, while at the same time particular harmonics are minimized or even eliminated. Another approach might minimize the total harmonic distortion (THD) of the phase currents i_{ph} .

Further, in control schemes, which ask for a variable modulation index m, it makes sense to calculate a set of optimized pulse patterns with different modulation indices m and particular harmonics to be minimized or eliminated. Hence, the demands on the resolution of m define the number of optimization runs necessary. The results achieved hereby will then be storaged e.g. in a DSP system and the control system chooses the appropriate modulation functions for a specific operation point.

The off-line optimized pulse patterns presented in this thesis are based on the maximizing of the modulation index m and simultaneously on the elimination of particular harmonics, which makes sense according to the explanations in chapter 3.2.

A minimization of especially lower ordered harmonics is not recommendable, since even minimized harmonics often cannot fulfil the very strict harmonic requirements in a high power AC-system. Hence, due to the minimization, an additional cost intensive AC-side filter has to be installed, which could be omitted, if particular harmonic would be eliminated.

Further, in order to avoid expensive low order harmonic filters, preferably the lowest order current harmonics should be eliminated.

Concerning the symmetry of the off-line optimized pulse patterns, it was shown in chapter 3.3.2 that a symmetry to a quarter of a period would be desirable. For off-line optimized 3-level VSI pulse patterns this can be fulfilled for switching frequencies being both even or odd numbered multiples of the fundamental frequency. However, the optimizations showed that switching frequencies being even numbered multiples of the fundamental frequency resulted in smaller modulation indices m. Hence, only switching frequencies

cies being exclusively odd numbered multiples of the fundamental frequency have been taken into account.

With that the optimization criterias are derived, which will now be followed by a description of the generation of the 3-level VSI off-line optimized pulse patterns.

3.4.3 Generation of the off-line optimized pulse patterns

Generating these off-line optimized pulse patterns s_{ph} means to solve an equation system for its particular harmonic amplitudes S_k . Each harmonic amplitude is represented by one equation, which results from a general fourier row analysis for the 3-level VSI switching functions according to appendix B.3.1. Assuming a symmetry to a quarter of a period this yields

$$S_k = \frac{4}{k \cdot \pi} \cdot \sum_{i=1}^{N} (-1)^{i+1} \cdot \sin k \alpha_i$$
(3.2)

Herein k denotes the order of the harmonic and N the number of switching angles α_i in a quarter of a period. It is also obvious from eqn. (3.2), that each harmonic amplitude S_k is a function of all switching angles α_i .

In case of elimination of an individual harmonic, the corresponding equation for the harmonic amplitude has to equal to 0. Further, it is evident from a mathematical point of view, that the maximum number of harmonics, which can be eliminated, coincides with the number N of switching angles α_i .

Since the equation system is non-linear, more than one solution might be obtained. An additional objective function for the modulation index m ensures that those solution is chosen which results in the largest value for m. In order to achieve pulse patterns being symmetrical to a quarter of a period, the switching angles α_i are further restricted to values smaller than $\pi/2$.

The statements made above are exemplified in eqn. (3.3) and figure 3.1 for the elimination of the 5th, 7th and 11th harmonic:

$$S_5 = \frac{4}{5 \cdot \pi} (\sin 5\alpha_1 - \sin 5\alpha_2 + \sin 5\alpha_3) = 0$$
$$S_7 = \frac{4}{7 \cdot \pi} (\sin 7\alpha_1 - \sin 7\alpha_2 + \sin 7\alpha_3) = 0$$

$$S_{11} = \frac{4}{11 \cdot \pi} (\sin 11\alpha_1 - \sin 11\alpha_2 + \sin 11\alpha_3) = 0$$
(3.3)

$$S_1 = m = \frac{4}{\pi} \cdot (\sin\alpha_1 - \sin\alpha_2 + \sin\alpha_3) \rightarrow max$$

$$\alpha_1, \alpha_2, \alpha_3 < \frac{\pi}{2}$$

fig 3.1: 3-level VSI pulse pattern with a symmetry to a quarter of a period and a switching frequency $f_{s_{ph}} = 150$ Hz ($f_{s_{ph}} = 3$ [p.u.])

From figure 3.1 it can also be seen that the number of switching instants α_i equals the number of on/off cycles for each valve of the 3-level VSI. Hence, the switching frequency $f_{s_{ab}}$ of each valve can be calculated according to

$$f_{s_{nk}} = N \cdot f_1 \text{ [p.u.]} \tag{3.4}$$

where N denotes both the number of switching angles α_i and the number of eliminated harmonics and f_1 the fundamental frequency in per unit notation $(f_1=1 \text{ [p.u.]})$.

For the example in figure 3.1, the switching frequency for each valve results to $f_{s_{ph}} = 150$ Hz, which corresponds to $f_{s_{ph}} = 3$ [p.u.].

It should be noted at this point, that the same optimization (elimination of 3 harmonics, symmetry to a quarter of a period) applied to the 2-level VSI would result in a switching frequency of $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) for each valve. This underlines one of the 3-level VSI advantages compared to the 2-level VSI.

In the consecutive chapter, the attributes of the pulse patterns, which are achieved by these optimizations, are presented.

3.4.4 Attributes of the off-line optimized pulse patterns

The attributes of interest are with regard to the elimination of harmonics, the modulation index *m* and the minimum pulse length of particular switching functions s_{ph} . As mentioned yet, the investigations exclusively include switching frequencies being odd numbered multiples of the fundamental frequency and a range from $f_{s_{ph}} = 50$ Hz ($f_{s_{ph}} = 1$ [p.u.]) up to $f_{s_{ph}} = 1450$ Hz ($f_{s_{ph}} = 29$ [p.u.]).

a) Harmonics elimination

In order to reduce the harmonic content of the switching functions s_{ph} , as many as possible harmonics will be eliminated. Hereby the harmonics are eliminated in ascending order, starting with exclusively the 5th for a switching frequency $f_{s_{ph}} = 50$ Hz $(f_{s_{ph}} = 1$ [p.u.]) and ending with the 5th, 7th, 11th,... 89th for a switching frequency $f_{s_{ph}} = 1450$ Hz $(f_{s_{ph}} = 29$ [p.u.]). All multiple orders of 3 are not eliminated, since they constitute zero sequence systems and will therefore not appear on the primary side of the converter transformer.

Hence, for all switching frequencies a non-linear equation system according to eqn. (3.3) had to be solved for the elimination of a certain number of switching function harmonics. In the case of e.g. $f_{s_{ph}} = 1450$ Hz $(f_{s_{ph}} = 29$ [p.u.]), this becomes as large as 29 equations with 29 switching angles α_i for the elimination of 29 switching function harmonics. The optimization results for the whole investigated frequency range are summarized in table 3.1.

Hereby, todays realistic switching frequencies (50Hz - 350Hz) are high-lighted.

Line diagrams and spectra of these pulse patterns for switching frequencies $f_{s_{ph}} = 50$ Hz, 150Hz, 250Hz and 950Hz ($f_{s_{ph}} = 1, 3, 5, 19$ [p.u.]) will be presented in chapter 3.7.1. This will also include a comparison to carrier based PWM modulation signals s_{nh} with the same switching frequencies.

switching frequency	eliminated harmonics in s_{ph}	т	min. pulse length
50 Hz	5	1.211	2000 µs
150 Hz	5, 7, 11	1.176	321.3 µs
250 Hz	5, 7, 11, 13, 17	1.166	132.6 µs
350 Hz	5, 7, 11, 13, 17, 19, 23	1.162	66.5 µs
450 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29	1.160	37.9 µ <i>s</i>
550 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35	1.158	23.5 µs
650 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41	1.157	15.6 μ <i>s</i>
750 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47	1.157	10.9 μ <i>s</i>
850 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53	1.156	7.9 μ <i>s</i>
950 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53, 55, 59	1.156	5.9 µ <i>s</i>
1050 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53, 55, 59, 61, 65	1.156	4.5 μ <i>s</i>
1150 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53, 55, 59, 61, 65, 67, 71	1.156	3.5 µ <i>s</i>
1250 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53, 55, 59, 61, 65, 67, 71, 73, 77	1.155	2.8 μ <i>s</i>
1350 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53, 55, 59, 61, 65, 67, 71, 73, 77, 79, 83	1.155	2.3 μ <i>s</i>
1450 Hz	5, 7, 11, 13, 17, 19, 23, 25, 29, 31, 35, 37, 41, 43, 47, 49, 53, 55, 59, 61, 65, 67, 71, 73, 77, 79, 83, 85, 89	1.156	1.9 μ <i>s</i>

table 3.1: eliminated harmonics, modulation index m and minimum pulse length for off-line optimized 3-level VSI pulse patterns s_{ph} ; **bold: realistic (50Hz - 350Hz),** plain: future (450Hz - 1450Hz)

b) Modulation index m

Concerning the modulation indices m(eqn. (3.1) in chapter 3.3.3), which are given in the 3rd column of table 3.1, quite large values between 1.21 [p.u.] for 50Hz and still 1.156 [p.u.] for 1450Hz can be achieved. Especially the results for switching frequencies $f_{s_{ph}} > 1\text{kHz} (f_{s_{ph}} > 20[\text{p.u.}])$ are gratifying. Apparently, m = 1.155 seems to represent a maximum value for these higher switching frequencies. A comparison of the modulation indices mwith regard to those achieved with carrier based PWM, will be given in chapter 3.7.2.

These large modulation indices in its turn also have an influence on the individual pulse lengths of the modulation functions s_{ph} , which will be discussed in the next sub-chapter.

c) Minimum pulse length of s ph

It could be observed, that with an increasing switching frequency, the width of the individual switching function pulses will decrease, which also can be clearly seen in table 3.1 (4th column). The largest pulses, which are achieved for a switching frequency $f_{s_{ph}} = 50 \text{ Hz} (f_{s_{ph}} = 1[\text{p.u.}], \text{FFM})$, have a pulse length of 2ms, while the shortest ones, which result for a switching frequency of $f_{s_{ph}} = 1450 \text{ Hz} (f_{s_{ph}} = 29[\text{p.u.}])$, are as small as $1.9 \mu s$.

In the optimizations performed in this thesis, no restrictions on the minimum pulse length have been taken into account. This is due to the fact, that these additional constraints will increase the dimension of the non-linear optimization problem, which yields an exponential increase in the number of solutions and the time to calculate them. Hence, probably no solutions would have been obtained for switching frequencies larger than a few hundred Hz.

The optimization results in table 3.1 seem to be representative for todays high power semiconductor devices, at least for a certain frequency range. The minimum turn-off times for presently available IGBT's are about $2-5\mu s$ and those for the (hard driven) GTO's are about ten times higher, $50\mu s$.

Therefore, nearly all of these pulse patterns in table 3.1 could be applied for IGBT applications and those up to $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) for GTO applications. The limited switching frequency range for GTO applications does not imply a severe drawback here, since 350 Hz presently seems to be the maximum realistic switching frequency for today's high power GTOs

anyhow. Future improvements might increase the GTO's switching frequencies, however in addition it can be expected that in the same way the minimum turn-off times of these semiconductors will decrease.

3.5 Carrier based PWM

3.5.1 Introduction

With increasing switching frequencies of high power semiconductor devices, also carrier based PWM might become an interesting modulation scheme for transmission applications.

Especially the comparison with off-line optimized PWM concerning the utilization of the 3-level VSI and the harmonic pollution will be of highest interest.

There are many distinctive carrier based PWM methods known today, which are based on different types of carrier and control signals. Modifications of the carrier signals might yield an improved harmonic spectrum, while manipulations of the control signal might result in a larger modulation index m.

This thesis will not present a general analysis of the carrier based PWM and will further not focus on the numerous methods to generate its pulse patterns. For that purpose, the reader is referred to the well known literature, e.g. [33], [34], [42], [44]. Here, the basics of carrier based PWM are presupposed and only the comparison to off-line optimized pulse patterns will be of importance.

In this work, a carrier based PWM method for the 3-level VSI is chosen, which is especially well suited for transmission applications! It will be shown, that even for low switching frequencies up to 350Hz, the lower ordered switching function harmonics will contribute with negligible or at most very small values.

Though not discussed in detail, a brief description will be presented in the following. For detailed informations, the reader is referred to [34].

3.5.2 Carrier based PWM pulse patterns with flat-top control signals

a) Control signals

Speaking of carrier based PWM, it is well known (e.g. [34]) that the control

signal mainly determines the following attributes of the resulting switching functions s_{ph} :

- the fundamental frequency of s_{ph} , which coincides with the fundamental frequency of the control signal.
- the fundamental's amplitude of s_{ph} (the modulation index *m*), which at least for higher switching frequencies $f_{s_{ph}} > 350 \text{Hz} (f_{s_{ph}} > 7[\text{p.u.}])$ exclusively depends on the shape and the amplitude of the control signal.
- the phase angle of the fundamental of s_{ph} which equals the phase angle of the fundamental of the control signal.

This proves right both for the 2-level and 3-level VSI.

Hence, in 3-level VSI transmission applications, for each phase ph = a,b,c, one control signal cs_{ph} is chosen with the same fundamental frequency f_1 as the AC-system. With regard to the individual phases a,b,c, these control signals have identical shape but are phase-displaced by $2\pi/3$ to each other.

In order to increase the modulation index m to values larger than m=1[p.u.], as it is desirable in transmission applications, the usually pure sinusoidal control signal should be modified in an appropriate way.

Here, this will be done according to a simple method, which effectively can be applied for modulation indices between $1 \le m \le 1.1547$ ([34]).

For that purpose, the purely sinusoidal 3-phase control signals $cs_{a,b,c}$ with an amplitude in the range $1 \le m \le 1.1547$ (figure 3.2, graphic a)) are superimposed with a zero sequence component cs_0 (figure 3.2, graphic b)). This results in the modified control signals $cs_{a,b,c+0}$ (figure 3.2, graphic c)):

$$cs_{a, b, c+0} = cs_{a, b, c} + cs_0$$

In order to achieve the zero sequence component cs_0 , all segments of the purely sinusoidal control signals $cs_{a,b,c}$, which overtop the amplitudes of the carrier signals (peak-value of 1[p.u.)]), are added and multiplied with (-1). These segments are represented in the graphics a) and b) of figure 3.2 by the filled areas.

The modified control signals $cs_{a, b, c+0}$ (figure 3.2, graphic c) will then show up a 'flat-top' with a constant amplitude value, which is exactly equal to the peak-value of the carrier signals.

This has two significant consequences:

1.) No over-modulation will occur, since the resulting control signals



fig 3.2: generation of the carrier based PWM pulse patterns s_{ph} : 'flat-top' control signals $cs_{a,b,c+0}$; triangular shaped carrier signals $c1_{a,b,c}$, $c2_{a,b,c}$; m=1.1547; $f_{s_{ph}}=150$ Hz; $f_c=250$ Hz

 $cs_{a,b,c+0}$ will not have larger peak-values than the carrier signals. This in its turn yields the advantage that the switching function harmonics do not increase for modulation indices larger than m=1.0 (up to m=1.1547).

2.) The very short and ineffective switching function pulses in the centre of each half-period, which are characteristic for other carrier based modulation methods, will disappear. Due to this, the carrier frequency f_c will be larger than the resulting switching frequency $f_{s_{ph}}$ of the pulse pattern s_{ph} . Therefore, compared to conventional carrier based methods with the same switching frequency $f_{s_{ph}}$, the first predominant harmonics of s_{ph} will appear at higher orders.

These two significant consequences are also graphically manifested in figure 3.2 for a switching frequency of $f_{s_{ph}} = 150$ Hz ($f_{s_{ph}} = 3$ [p.u.]) and a carrier frequency of $f_c = 250$ Hz ($f_c = 5$ [p.u.]).

b) Carrier signals

As mentioned yet, the types of carrier signals are varying in a wide range. It is well known from the literature (e.g. [34], [45]) that, depending on their various shapes, they mainly determine the following attributes of the resulting modulation signals s_{ph} :

- the switching frequency of s_{ph} and with that of the individual VSI valves.
- the resulting harmonic amplitudes and their orders k.

Hereby, carrier based PWM for the 2-level VSI presupposes one carrier signal c_{ph} in each phase ph = a,b,c.

This is subject to change for the 3-level VSI, where two carrier waves $c1_{ph}$ and $c2_{ph}$ are chosen, which have identical shape and frequency but a phasedisplacement of π with respect to their period. This is shown high-lighted in figure 3.2, graphic a) or c) for phase *a* and a carrier frequency $f_c=250$ Hz ($f_c=5$ [p.u.]).

It should be noted at this point, that using two identical, by π phase-displaced carrier signals, yields the advantage to eliminate specific harmonic frequency bands. This will be discussed more in detail in chapter 3.5.3.

It is also evident from figure 3.2, that the carriers $c1_{ph}$ and $c2_{ph}$ are assumed to have a triangular shape, which was found to be very good suited for 3-level VSI transmission applications. A carrier with the shape of a sawtooth always produces even numbered harmonics, which here is highly un-

desirable ([34], [45]). More, for large modulation indices m (m > 0.9), as demanded in this thesis, the harmonic distortion of the AC-side currents i_{ph} is smaller with triangular shaped carriers. This will turn into the opposite for small modulation indices m (m < 0.9), which however will not be of major interest in these studies.

Additionally, the phase displacements of the carriers $c1_{ph}$ and $c2_{ph}$ with respect to the control signals $cs_{a,b,c+0}$ is fixed to $\pm \pi/2$ of the carrier period (figure 3.2, graphic a) or c)). With that measure it is ensured, that the 3-level VSI pulse patterns will inherently have a symmetry to a quarter of a period. This is true for all carrier frequencies being any integered multiples of the control signal frequency.

Further, the carrier pairs $c1_{ph}$ and $c2_{ph}$ for the 3 phases ph = a,b,c are phase-displaced by $2\pi/3$ to each other. This guarantees that the switching functions s_{ph} will have the same shape, and with that all harmonics being multiples of 3 will be zero sequence systems which do not contribute to the AC-side currents i_{ph} .

It should be mentioned at this point, that for the 2-level VSI usually 3 phasedisplaced carrier waves instead of one carrier wave for all 3 phases a,b,cwill result in a much higher harmonic distortion for the AC-side currents i_{nb} . This however could not be observed for the 3-level VSI.

For the 3-level VSI and high modulation indices m (m > 0.9), the AC-side current THDs are nearly the same, no matter whether one carrier pair or 3 phase-displaced carrier pairs are chosen. More, for smaller modulation indices m (m < 0.9), simulations have shown that 3 phase-displaced carrier pairs compared to exclusively one carrier pair, even result in lower THDs for the AC-side currents. This is an astonishing result, which however will not be proved or further investigated here in this thesis.

As mentioned above, applying 3 carrier pairs being phase-displaced by $2\pi/3$, yields the advantage not to generate AC-side current harmonics being multiples of 3. Especially for low carrier frequencies (250 Hz and 350 Hz) and applying the same carrier pair for all 3 phases a,b,c, a 3rd harmonic will arise in the VSI output voltages u_{ph} and the AC-side currents i_{ph} . This in its turn would demand a cost intensive large filter, which has to be omitted.

With that, also the carrier signals $c1_{ph}$ and $c2_{ph}$ are described. Together with the control signal $cs_{a,b,c+0}$, the 3-level VSI pulse patterns can now be generated according to a convention, which will be presented in the next

sub-chapter.

c) generation of the switching functions

In order to obtain the 3-level VSI switching functions s_{ph} from the control signals $cs_{a, b, c+0}$ and the carrier signals $c1_{ph}$ and $c2_{ph}$, the following convention has been used:

$$\begin{split} s_{ph} &= 1, & \text{if} \quad cs_{ph+0} > c1_{ph} & \text{and} \quad cs_{ph+0} > c2_{ph} \\ s_{ph} &= 0, & \text{if} \quad cs_{ph+0} > c1_{ph} & \text{and} \quad cs_{ph+0} < c2_{ph} \\ s_{ph} &= 0, & \text{if} \quad cs_{ph+0} < c1_{ph} & \text{and} \quad cs_{ph+0} > c2_{ph} \\ s_{ph} &= -1, & \text{if} \quad cs_{ph+0} < c1_{ph} & \text{and} \quad cs_{ph+0} < c2_{ph} \end{split}$$

Hence, the 3-level VSI switching functions s_{ph} will change its values at each intersection of the control signal $cs_{a,b,c+0}$ with either the carrier signal $c1_{ph}$ or the carrier signal $c2_{ph}$. This can also graphically be verified for the pulse pattern s_a in figure 3.2.

Basing on this generation convention and the carrier/control signals described in this chapter, modulation signals s_{ph} were generated, the attributes of which will be discussed in the considerations to come.

3.5.3 Characteristics of the carrier based pulse patterns

The characteristics of interest are with regard to the harmonic content, the modulation index and the minimum pulse length of the particular switching functions in dependency on the switching frequency.

For comparison reasons with off-line optimized PWM, the investigations also include switching frequencies being exclusively odd numbered multiples of the AC-system's fundamental frequency f_1 , ranging from 50Hz up to 1450Hz.

Analog to off-line optimized PWM (table 3.1), the most important parameters are presented in table 3.2.

a) Harmonic content

Concerning carrier based PWM, it is well known that usually individual harmonics will not be eliminated in the switching functions, as this proves right for off-line optimized PWM. However, there is still a chance especially for

switching fre- quency f _{sph}	carrier frequency $f_{\rm c}$	modulation index m	min. pulse length of s _{ph}
50 Hz	150 Hz	1.221	1830 μ <i>s</i>
150 Hz	300 Hz	1.158	489 μs
250 Hz	450 Hz	1.155	136 μs
350 Hz	600 Hz	1.155	57 μ <i>s</i>
450 Hz	750 Hz	1.155	29 µs
550 Hz	900 Hz	1.155	17 μs
650 Hz	1050 Hz	1.155	11 µs
750 Hz	1200 Hz	1.155	7.2 μ <i>s</i>
850 Hz	1350 Hz	1.155	5.0 μ <i>s</i>
950 Hz	1500 Hz	1.155	3.9 µs
1050 Hz	1650 Hz	1.155	2.8 μ <i>s</i>
1150 Hz	1800 Hz	1.155	2.2 μ <i>s</i>
1250 Hz	1950 Hz	1.155	1.7 μ <i>s</i>
1350 Hz	2100 Hz	1.155	1.1 μ <i>s</i>
1450 Hz	2250 Hz	1.155	1.1 μ <i>s</i>

table 3.2: carrier frequencies f_c , modulation index m and minimum pulse length for carrier based 3-level VSI pulse patterns s_{ph} ; **bold: realistic (50Hz - 350Hz),** plain: future (450Hz - 1450Hz)

the carrier based PWM method introduced in the previous chapter, that low ordered harmonic amplitudes will take on very small values (e.g. < 0.01 [p.u.]), which do not ask for an additional AC-side filter.

The spectra of carrier based PWM pulse patterns can be described by frequency bands, which are arranged around specific centre frequencies. For synchronous schemes these centre frequencies are integer numbered multiples of the chosen carrier frequency f_c . With respect to the harmonic amplitudes, it can qualitatively be said, that their values decrease with increasing deviation from the centre frequency. However, for low carrier frequencies (up to a few hundred Hz), these frequency bands will overlap and the significant band structure might not clearly be apparent.

These statements will be confirmed for pulse patterns with representative switching frequencies of 50Hz, 150Hz, 250Hz and 950Hz ($f_{s_{ph}}$ =1, 3, 5, 19[p.u.]) in chapter 3.7.1.

The particular harmonic orders k of a specific pulse pattern depend on the shape of the carrier waves and are a function of the carrier frequency f_c and the fundamental frequency f_1 of the control signal. For the 3-level VSI control and carrier signals assumed in this thesis (chapter 3.5.2), the harmonic orders k of the resulting pulse patterns s_{ph} can be calculated according to eqn. (3.5):

$$k = n \cdot f_c \pm v \cdot f_1 \tag{3.5}$$

where n = 2, 4, 6, ... and v = 1, 3, 5, ...

Herein $n \cdot f_c$ denotes the centre frequencies, while the frequencies of the corresponding side band harmonics deviate by $\pm v \cdot f_1$ from these frequencies.

In addition, for the carriers chosen here (3 carrier pairs phase-displaced by $2\pi/3$), all harmonic orders k, being multiples of 3, will result in zero sequence systems.

It could be seen in figure 3.2, graphics c) and d), that for the herein described carrier based PWM, the carrier frequency f_c will be higher than the switching frequency $f_{s_{ph}}$ of the resulting pulse patterns, which constitutes one powerful characteristic of this modulation scheme.

Hence, according to eqn. (3.5), also the orders will for the first dominant harmonics will increase in comparison to the conventional carrier based schemes, where the carrier frequency f_c equals the switching frequency $f_{s_{ph}}$.

The highest achievable carrier frequencies f_c for the particular investigated switching frequencies $f_{s_{ph}}$ are summarized in the second column of table 3.2.

It is apparent in table 3.2, that for lower switching frequencies up to 250Hz $(f_{s_{ph}} = 5 \text{ [p.u.]})$, the carrier frequency f_c can almost be doubled (!) with regard to the resulting pulse pattern switching frequency $f_{s_{nh}}$!

More, also for the higher values of $f_{s_{ph}}$, the carrier frequency f_c will be at least 1.5 times larger than $f_{s_{ph}}$. This is quite an impressive result, which can

be expected to have a very positive influence on the harmonic content of the AC-side currents i_{ph} (chapter 3.7).

Finally, it should be noted at this point, that eqn. (3.5) also can be applied to the 2-level VSI, however then the parameter n includes all odd and even numbered integers: n = 1, 2, 3, ... From this it is evident that for the 2-level VSI, twice the number of frequency bands are present in the spectra of the modulation signals s_{ph} .

This phenomenon is caused by the two opposite signed carrier waves $c1_{ph}$ and $c2_{ph}$ for the 3-level VSI instead of one carrier signal c_{ph} for the 2-level VSI. With that measure, all frequency bands with centre frequencies being odd numbered multiples of the carrier frequency, are eliminated. Simultaneously, the switching frequency for each individual 3-level VSI valve remains the same as for the 2-level VSI, which also for carrier based PWM proves one advantage of the 3-level VSI topology.

For more detailed information, the reader is referred to [34] and [45].

b) modulation index m

According to the choice of the control signal $cs_{a,b,c+0}$ in chapter 3.5.2 a), the maximum modulation index *m* of the resulting pulse patterns s_{ph} is expected to be m = 1.155 for all investigated switching frequencies. However, it can be observed in table 3.2 (third column), that for low switching frequencies $f_{s_{ph}} = 50$ Hz and 150Hz ($f_{s_{ph}} = 1, 3[p.u.]$), this is not proved to be right. Especially for $f_{s_{ph}} = 50$ Hz ($f_{s_{ph}} = 1[p.u.]$), quite a large value m = 1.22is achieved.

This is mainly caused by the superposition of the switching function's fundamental component with one or more side band harmonics, whose frequencies coincide with the fundamental frequency. Eqn. (3.5) proves the validity of this statement.

For higher carrier/switching frequencies, this effect will then become really negligible, as also can be verified in table 3.2, where for higher switching frequencies $f_{s_{ph}} > 150$ Hz ($f_{s_{ph}} > 3$ [p.u.]) the modulation index *m* coincides with the fundamental of the control signals $cs_{a,b,c+0}$.

A comparison of the modulation indices m in figure 3.2 with those for offline optimized PWM (chapter 3.4.4, table 3.1) will be performed in chapter 3.7.2. First however, some comments should be made about the minimum pulse length of the achieved switching functions s_{ph} , which in practical applications might be a driving force for a decrease of the modulation index m.

c) Minimum pulse length of s_{ph}

For conventional carrier based PWM schemes, where the carrier frequency equals the switching frequency of the resulting pulse pattern, very small minimum pulse lengths have to be expected, when high modulation indices are applied. This is caused by the very narrow and in addition ineffective pulses in the centre region of each half-period.

Therefore, at least in high power applications, where the minimum turn-on/ off times of GTO's are restricted to about $50\mu s$, the modulation indices would have to be decreased in order to ensure this minimum time interval.

This however will be subject to change for the carrier based PWM method investigated here, where no pulses in the centre region of each half-period are present (figure 3.2, graphic d)).

As a consequence, all pulse patterns in the todays realistic switching frequency range up to $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) can fulfil the requirement of a minimum turn-off time of $50\mu s$ for todays available GTOs without the need to decrease the high modulation index of m = 1.155 (table 3.2).

Concerning IGBT valves, the pulse lengths in table 3.2 are still in good agreement with the minimum turn-off requirements at least for a frequency range up to about 1kHz.

Now the basics are derived for both off-line optimized and carrier based PWM. Before performing a more in depth comparison of these two modulation schemes with regard to their effects on the AC-side currents i_{ph} and the AC-system voltages u_{Lph} , the 3-level VSI operation mode and other system parameters have to be known. This will be discussed in the next chapter.

3.6 Studied system

When calculating the harmonic distortion of AC-system voltages u_{Lph} or AC-side phase currents i_{ph} , the exclusive knowledge of the pulse patterns s_{ph} is not sufficient. In addition, representative (worst case) conditions must be assumed concerning the following points of interest:

- the operation mode of the 3-level VSI,
- system parameters such as the ohmic part r and the inductive part l of

the decoupling impedance (chapter 2.3, figure 2.3),

• the strength of the AC-network.

The considerations to come will focus on these topics.

3.6.1 Operation mode and system parameters

It is well known, that the 3-level VSI in general is capable to both generate and absorb any active and reactive power. With a control strategy, basing on a fixed pulse pattern over the whole operating range, the largest harmonic amplitudes will arise when the 3-level VSI generates a pure nominal reactive power. This means, that the 3-level VSI acts like a capacitor installed on the AC-side (pure capacitive operation mode). Hereby, the AC-system is defined as a source, while the 3-level VSI is defined as a sink.

Generating a pure reactive power (pure capacitive 3-level VSI operation mode) asks for the largest fundamental component in the 3-level VSI output voltages u_{ph} , which corresponds to the largest value for the 3-level VSI total DC-side voltage $u_{D1} + u_{D2}$. This in its turn, for a fixed pulse pattern over the whole operating range, also yields the largest harmonic amplitudes both in the 3-level VSI output voltages u_{ph} and the AC-side currents i_{ph} .

It makes sense to choose this worst case concerning the harmonic pollution for the comparison of the two modulation schemes. All other operation modes (generating/absorbing pure active power, absorbing pure reactive power) will show up smaller harmonic amplitudes to arise in u_{ph} and i_{ph} .

With regard to the amplitudes U_{Lph} of the AC-system voltages and the fundamental component of the phase currents i_{ph} , pure nominal reactive power means that these quantities will have a value of 1 [p.u.].

Finally, the DC-side voltages u_{D1} and u_{D2} will here be assumed to constitute balanced and ripplefree DC-quantities. The various influences of harmonics or an unbalance in these voltages is discussed in depth in chapter 4 chapter 6 (DC-side harmonic influence) and chapter 7 (DC-side unbalance).

With that and a given modulation function s_{ph} , the 3-level VSI output voltages u_{ph} and their spectra are clearly determined. For the calculation of the AC-side currents i_{ph} and their harmonics however, at least the decoupling impedance has to be known.

Hence, reasonable values for the decoupling impedance, consisting of the ohmic part r and the inductive part l, have to be determined. For a transmission application,

$$r = 0.005$$
 [p.u.] and $l = 0.2$ [p.u.]

seem to be quite realistic values and have been chosen throughout this thesis. With that, for a given operation mode and pulse pattern s_{ph} , the AC-side currents i_{ph} and its harmonics can be calculated, if the AC-system impedance is neglected (r_L =0 and l_L =0 in figure 2.3 of chapter 2.3).

The resulting AC-side currents i_{ph} and its harmonics presented in chapter 3.7 are basing on an infinite strong AC-network, i.e. it is assumed, that the AC-system impedance equals to 0. Therefore, the AC-side current harmonic amplitudes will represent worst case values, since an AC-system impedance would yield an additional damping of these harmonics.

Similar considerations are performed for the harmonic distortion of the ACsystem voltages u_{Lph} . For an infinite strong AC-system, u_{Lph} will remain ideal cosinusoidal, since all harmonics generated by the 3-level VSI output voltages u_{ph} will drop over the decoupling impedance and will not appear in u_{Lph} . In the theoretical worst case of an infinite weak AC-system however $(r_L \rightarrow \infty, l_L \rightarrow \infty)$, the harmonic distortions of u_{Lph} and u_{ph} will become the same. Concerning the harmonic distortion of the AC-system voltages u_{Lph} , this worst case of an infinite weak AC-system is presupposed in the results presented in chapter 3.7.

In order to take into account a specific AC-network strength, a definition of this notion is given in the consecutive chapter. Basing on this, correction factors are derived, which, multiplied with the harmonic distortion worst case values, yield the proper results for a specific AC-system strength.

3.6.2 Influence of the AC-system strength

a) Definition of the AC-network strength

According to [46], [47], the strength of an AC-system is defined by the ratio of the AC-system short circuit capacity to the nominal apparent power of the transmission application (here: the 3-level VSI). From this it is evident that the strength of an AC-system is inversely proportional to its impedance, since the AC-system impedance determines its short circuit capacity.

A common abbreviation for the AC-system strength is SCR (Short Circuit Ratio). In particular

- a strong AC-system is categorized by a SCR value larger than 3,
- a weak AC-system is categorized by a SCR value between 2 and 3,

• a very weak AC-system is categorized by a SCR value lower than 2.

Basing on this, correction factors for the multiplication of the harmonic distortion worst case values will be derived in the following.

b) Correction factors for the harmonic distortion worst case values

Since an AC-system usually is characterized by the short cut ratio SCR, it will be convenient to express the correction factors for the harmonic distortion worst case values as a function of this parameter SCR. Hereby, it will be distinguished between a correction factor $corr_i$, which has to be multiplied with the harmonic distortion worst case values of the AC-side currents i_{ph} , and a correction factor $corr_u$, for the AC-system voltages u_{Lph} .

Neglecting the ohmic parts r_L and r in both the AC-system and the decoupling impedance, which does not introduce a major error, results to

$$corr_i = \frac{1}{1 + 1/(l \cdot SCR)}$$
 (3.6)

$$corr_{u_L} = \frac{1}{1 + l \cdot SCR} \tag{3.7}$$

With a transformer stray inductance of l=0.2[p.u.] and the definitions according to sub-chapter a), eqn. (3.6) and eqn. (3.7) yield figure 3.3 and table 3.3.



fig 3.3: correction factors $corr_i$ and $corr_{u_L}$ for the harmonic distortion worst case values of i_{ph} and u_{Lph} in dependancy on the AC-system strength SCR

AC-system strength	corr _i	corr _{ul}
strong ($SCR > 3$)	<i>corr</i> _i > 0.375	<i>corr_{u_L} <</i> 0.625
weak $(2 \leq SCR \leq 3)$	$0.286 \le corr_i \le 0.375$	$0.625 \le corr_{u_L} \le 0.714$
very weak $(SCR < 2)$	<i>corr_i</i> < 0.286	$corr_{u_{l}} > 0.714$

table 3.3: range of the correction factors $corr_i$ and $corr_{u_L}$ for the harmonic distortion worst case values of i_{ph} and u_{Lph} for a strong, weak, and very weak AC-system

Now it is easy to achieve proper harmonic distortion values in dependancy on a given AC-system strength. Simply multiplying any harmonic distortion worst case value of e.g. a particular harmonic amplitude or a THD with the appropriate factors $corr_i$ or $corr_{u_L}$ for a specific SCR value, yields the desired result.

3.7 Comparison of off-line and carrier based PWM

A comparison of off-line optimized PWM with carrier based PWM will be of high interest and will therefore be performed in this chapter.

In detail, these two schemes will be compared with regard to the following features:

- assessment of the filter sizes necessary to fulfil the harmonic requirements of a high power AC-system (chapter 3.7.1)
- line diagram of the AC-side phase currents i_{ph} (chapter 3.7.1)
- modulation indices m in dependancy on the switching frequency (chapter 3.7.2)
- peak-values of the AC-side phase currents i_{ph} in dependancy on the switching frequency (chapter 3.7.2)
- power rating of the 3-level VSI in dependancy on the switching frequency (chapter 3.7.2)
- resulting Total Harmonic Distortion (THD) of the AC-system voltages u_{Lph} in dependancy on the switching frequency (chapter 3.7.2)
- resulting Total Harmonic Distortion (THD) of the AC-side phase currents i_{ph} in dependancy on the switching frequency (chapter 3.7.2)

3.7.1 AC-side currents and filter requirements

In this chapter, the variations in time and the spectra of particular off-line optimized and carrier based PWM switching functions s_{ph} and their corresponding AC-side currents i_{ph} will be presented. Basing on this, a comparison of the above mentioned modulation schemes will be performed, which will primarily focus on

- the filter sizes necessary to fulfil the harmonic requirements of a transmission system. Hereby, it is assumed that each AC-side current harmonic or each AC-system voltage harmonic having an amplitude larger than 0.01 [p.u.], will ask for a filter on the AC-side.
- the variation in time of the AC-side currents i_{ph} .

The switching frequencies of the representative pulse patterns s_{ph} are chosen to $f_{s,ph} = 50$ Hz, 150Hz, 250Hz and 950Hz ($f_{s,ph} = 1, 3, 5, 19$ [p.u.]), both for off-line optimized and carrier based PWM. While switching frequencies up to 250Hz are realistic for todays available high power GTOs, a switching frequency of 950Hz might be in the future. The results are given in figure 3.4- figure 3.7.

a) Assessment of the filter sizes

In order to assess the necessary filter sizes, the amplitude spectra of the switching functions s_{ph} and the AC-side currents i_{ph} are of great help (graphics b) and d) in figure 3.4- figure 3.7).

The amplitude spectra of the 3-level VSI output voltages u_{ph} will be achieved by multiplying the amplitude spectra of the switching functions s_{ph} with half of the total DC-side voltage $u_{Dsum} = u_{D1} + u_{D2}$. Hereby, u_{Dsum} is close to a value of 1 [p.u.] for the operation mode and the system parameters described in chapter 3.6.1. Hence the amplitude spectra of s_{ph} are in addition quite a good representation of the amplitude spectra of u_{ph} . Further, it should be recalled in mind, that the harmonic amplitudes of u_{ph} in its turn can also be seen as worst case values for the AC-system voltages u_{Lph} .

The dotted line in the graphics b) and d) of figure 3.4 - figure 3.7 indicates the maximum permitted values of 0.01 [p.u.] for each harmonic amplitude without the need of an AC-side filter. It should be noted, that hereby all switching function harmonics with orders equal to multiples of 3, must not be taken into account, since they constitute zero sequence systems.

In particular, the following quantitative statements can be verified from the
- 72 -



fig 3.4: line diagram and amplitude spectra of s_{ph} and i_{ph} for off-line optimized and carrier based PWM, switching frequency $f_{s_{ph}} = 50$ Hz ($f_{s_{ph}} = 1$ [p.u.]), l = 0.2[p.u.], r = 0.005[p.u.], pure cap. operation mode; further parameters: table 3.1, figure 3.2, table 3.2



fig 3.5: line diagram and amplitude spectra of s_{ph} and i_{ph} for off-line optimized and carrier based PWM, switching frequency $f_{s_{ph}} = 150$ Hz $(f_{s_{ph}} = 3[p.u.])$, l=0.2[p.u.], r=0.005[p.u.], pure capacitive operation mode; further parameters:table 3.1, figure 3.2, table 3.2

- 74 -



fig 3.6: line diagram and amplitude spectra of s_{ph} and i_{ph} for off-line optimized and carrier based PWM, switching frequency $f_{s_{ph}} = 250$ Hz $(f_{s_{ph}} = 5[p.u.])$, l = 0.2[p.u.], r = 0.005[p.u.], pure capacitive operation mode; further parameters:table 3.1, figure 3.2, table 3.2



fig 3.7: line diagram and amplitude spectra of s_{ph} and i_{ph} for off-line optimized and carrier based PWM, switching frequency $f_{s_{ph}} = 950$ Hz ($f_{s_{ph}} = 19$ [p.u.]), l = 0.2[p.u.], r = 0.005[p.u.], pure capacitive operation mode; further parameters:table 3.1, figure 3.2, table 3.2

- 75 -

graphics b) and d) in figure 3.4- figure 3.7, where the results in the left columns correspond to off-line optimized PWM and those in the right columns to carrier based PWM.

Starting with FFM ($f_{s_{ph}} = 1$ [p.u.], figure 3.4), it can be seen in the graphics b) and d) for the amplitude spectra, that the first harmonic to be filtered will be the 5th for carrier based PWM and the 7th for off-line optimized PWM. This proves right both for the AC-side currents i_{ph} and the AC-system voltages u_{Lph} . Concerning off-line optimized FFM, it is furthermore obvious, that in addition to the 5th harmonic all odd numbered multiples of five are eliminated.

For a switching frequency $f_{s_{ph}} = 150$ Hz ($f_{s_{ph}} = 3$ [p.u.], figure 3.5), the first harmonic, which asks for a filter, will still be the 5th for carrier based PWM and the 13th for off-line optimized PWM.

In the case of a switching frequency $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.], figure 3.6), off-line optimized PWM will satisfy the harmonic requirements, if filters for the 19th harmonic and higher orders will be installed. However now, also the sophisticated carrier based PWM pulse pattern shows up almost negligible values for the 5th and 7th harmonic and a filter tuned for the 11th and higher ordered harmonics will be sufficient to fulfil the harmonic demands.

Finally, off-line optimized and carrier based PWM pulse patterns with a higher switching frequency $f_{s_{ph}} = 950$ Hz ($f_{s_{ph}} = 19$ [p.u.], figure 3.7) are compared. Now, both the off-line generated and the carrier based modulation signal show up very similar good results, which, if at all, will ask for only very small filters.

The influence of a specific AC-network strength can be assessed with the correction factors $corr_i$ and $corr_{u_i}$, given in figure 3.3 of chapter 3.6.2.

With respect to the AC-side currents i_{ph} , the corresponding correction factors $corr_i$ will vary between 0.2 (SCR=1) and 0.8 (SCR=20) for realistic AC-systems. Multiplying these factors with the amplitudes of the lowest order current harmonics might result in amplitude values smaller than 0.01 [p.u.], which then will no longer ask for an additional AC-side filter. From this it can be concluded that a further small reduction of the AC-side filters will be realistic for both modulation schemes.

Slightly worse results will be achieved when focusing on the reduction of filters with respect to the AC-system voltage harmonic distortion. Exclusively for the carrier based method, correction factors $corr_{u_L}$ between 0.8 (SCR=1) and 0.2 (SCR=20) (figure 3.3) might be just small enough to re-

duce one of the predominant lowest order harmonics to values smaller than 0.01 [p.u.] (figure 3.4 - figure 3.6).

Hence, for the pulse patterns presented above, the necessary filter size to fulfil the harmonic requirements for both i_{ph} and u_{Lph} will only little be influenced by the AC-system strength.

It can therefore be summarized, that for low switching frequencies up to a few hundred Hz, off-line optimized PWM will ask for smaller AC-side filters than the carrier based PWM method. This is not astonishing since the off-line optimized pulse patterns are especially tuned for the elimination of the lowest order harmonics in order to reduce the filter size.

However, it was indicated by the simulation in figure 3.7 ($f_{s_{ph}} = 950$ Hz ($f_{s_{ph}} = 19$ [p.u.])), that for higher switching frequencies, the proposed carrier based PWM method apparently can compete with the off-line optimized PWM, which will further be confirmed in the studies to come.

b) Line diagram of the AC-side currents i_{ph}

Another point of interest concerns the line diagram of the AC-side currents i_{ph} (graphics c) in figure 3.4 - figure 3.7), which briefly will be discussed in this sub-chapter.

Comparing the graphics c) for carrier based and off-line optimized PWM, it is evident that for the switching frequencies $f_{s_{ph}} = 50$ Hz, 250Hz and especially for $f_{s_{ph}} = 950$ Hz, the line diagrams of i_{ph} look quite similar, which proves that the proposed carrier based method can truly be seen as an alternative to the off-line optimized PWM. Exclusively for a switching frequency $f_{s_{ph}} = 150$ Hz, off-line optimized PWM yields a much better result.

Concerning the peak-values of i_{ph} , a more representative comparison of the two modulation schemes for the whole investigated frequency range will be given in chapter 3.7.2. This also will be performed for the modulation indices m and other specific quantities, e.g. the THDs for both the AC-system voltages u_{Lph} and the AC-side currents i_{ph} , which will be introduced in the studies to come.

3.7.2 Influence on 3-level VSI design parameters

As mentioned yet, a specific modulation signal s_{ph} will not only determine the required filter size, but will furthermore have an influence on the utilization of the 3-level VSI. This also proves right for the power rating of the 3level VSI valves, which e.g. depends on the peak-values of the AC-side currents.

Hence, the investigations to follow will concentrate more in depth on these relevant parameters for the inverter design. In addition, another very common harmonic quantity, namely the Total Harmonic Distortion THD will be introduced. The studies will include all off-line optimized and carrier based modulation signals presented in table 3.1 of chapter 3.4 and table 3.2 of chapter 3.5 with switching frequencies between 50Hz and 1450Hz.

In particular, the following specific quantities will be investigated in dependancy on the switching frequency $f_{s_{nk}}$:

- the modulation indices m,
- the peak-values of the AC-side currents i_{ph} ,
- the power ratings of the 3-level VSI
- the THDs of the AC-system voltages u_{Lph} ,
- the THDs of the AC-side currents i_{ph} .

Once more, it will be focused on the comparison of the off-line optimized PWM with the proposed carrier based method. The achieved results are presented in figure 3.8 and will briefly be discussed in the following with regard to the above listed features.

a) modulation index m

Concerning the modulation index m, it will be distinguished between the frequency range up to 350 Hz, which is realistic for todays high power GTOs, and those including the higher frequencies up to 1450Hz.

With regard to the switching frequencies up to 350Hz (excluding FFM), it can be seen in figure 3.8a) that the off-line optimized pulse patterns yield only slightly better results. Hence, even in this lower switching frequency range, the carrier based method is a real alternative to off-line optimized PWM.

Further it is obvious, that off-line optimized FFM $(f_{s_{ph}}=1[p.u.])$ contributes with an exceptional large modulation index, which drastically drops if the switching frequency is increased. This also clearly indicates the favourable position of FFM modulation with respect to the voltage utilization of the inverter.

The pulse patterns s_{ph} with switching frequencies between 450Hz and 1450Hz are characterized by an almost constant modulation index m=1.15,



fig 3.8: modulation index m, peak values of i_{ph} , power rating S_{ph-VSI} and THDs (worst case) of u_{Lph} and i_{ph} in dependancy on the switching frequency, off-line optimized and carrier based PWM, pure capacitive operation mode, further parameters: table 3.1, figure 3.2, table 3.2

which is approximately the same for both modulation schemes.

Hereby, it is interesting, that for off-line optimized PWM with higher switching frequencies, the resulting modulation index m always coincides with the maximum value m = 1.155 for carrier based PWM. This modulation index might indicate a theoretical maximum for all modulation schemes with selective harmonic elimination or an optimized Total Harmonic Distortion (THD).

b) peak-values of the AC-side currents i_{ph}

Concerning the design of the 3-level VSI, also the peak-values I_{phpeak} of the AC-side currents i_{ph} must not be neglected. This is true, since these peak-values determine the minimum current rating of the semiconductor valves and therefore also the necessary power rating of the inverter.

Assuming nominal ideal sinusoidal AC-side currents i_{ph} and any operation mode, the corresponding current peak-values I_{phpeak} will not exceed a value of 1 [p.u.]. However, due to the influence of the current harmonics, this is subject to change, which will be discussed in the following for offline optimized and carrier based PWM in dependancy on the switching frequency.

Hereby, it can clearly be seen in figure 3.8, graphics b), that the AC-side current peak value I_{phpeak} will take on quite a large value for the carrier based PWM with a switching frequency $f_{s_{ph}}=150$ Hz, $(f_{s_{ph}}=3$ [pu.]).

Obviously this switching frequency $(f_{s_{ph}} = 150 \text{Hz})$ constitutes a special case and should be avoided for this kind of carrier based pulse pattern. However, for all other switching frequencies, especially for those larger than $f_{s_{ph}} = 250 \text{Hz}$, $(f_{s_{ph}} = 5[\text{pu.}])$, the here proposed carrier based PWM method shows up the same results as the off-line optimized PWM and can absolutely compete with the latter one.

c) power rating of the 3-level VSI

Concerning the required power rating of the 3-level VSI, both the peak-values of the AC-side currents i_{ph} and the modulation index *m* have to be taken into account. As mentioned yet, a larger modulation index *m* yields a smaller resulting DC-side voltage and with that also the blocking voltage of the semiconductor valves can be reduced. Hence, the power rating of the inverter decreases as well.

The power rating S_{ph-VSI} of one 3-level VSI leg a,b,c (one 3-level VSI valve) is hereby defined as

$$S_{ph-VSI} = \frac{u_{Dsum}}{2} \cdot I_{phpeak} = \frac{u_{D1} + u_{D2}}{2} \cdot I_{phpeak}$$
(3.8)

where u_{Dsum} equals the total DC-side voltages with respect to the pure capacitive operation mode and the modulation indices of figure 3.8, graphic a).

The results are presented in figure 3.8, graphic c) for off-line optimized and carrier based PWM in dependancy on the switching frequency.

It can be seen, that exclusively for the low switching frequencies up to about $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]), off-line optimized PWM is slightly better suited than the proposed carrier based scheme. For higher values of $f_{s_{ph}}$ however, there is no reason, why off-line optimized PWM should be preferred to the proposed carrier based method.

Further, it is clearly shown that off-line optimized FFM modulation, despite its outstanding large modulation index m, asks for the highest power to be installed in comparison to the higher switching frequencies. Obviously, the AC-side current stress equalizes the benefits achieved by the large modulation index m. However, in 12-pulse star-delta configurations, where the 5th, 7th,... AC-side current harmonics are eliminated, FFM modulation might constitute an excellent choice with respect to the necessary power rating of the inverter.

d) THD of the AC-system voltages u_{Lph}

Another quantity, which also represents a measure for the harmonic pollution, is with respect to the total harmonic distortion THD. In this sub-chapter the THD of the AC-system voltages u_{Lph} will be defined and the resulting values for both modulation schemes in dependancy on the switching frequency will be shortly discussed.

The *THD* of the AC-system voltages u_{Lph} is described by the following equation:

$$THD_{u_{L}} = \frac{\sqrt{\sum_{K} U_{Lk}^{2}}}{U_{L1}} \qquad k \in K = 5,7,11,13,...$$
(3.9)

Herein, U_{Lk} denotes the amplitude of the k-th AC-system voltage harmonic and U_{L1} the amplitude of the AC-system voltage fundamental, which here is presumed to be $U_{L1}=U_{Lph}=1$ [p.u.]. Further, the calculation of the THD_{u} , includes all harmonic orders up to k=500.

As mentioned yet in chapter 3.6.1, worst case values for U_{Lk} are assumed, which implies that the AC-system was chosen to be infinitely weak. Therefore, the harmonic amplitudes U_{Lk} will equal those of the 3-level VSI output voltages u_{ph} . A specific AC-system strength *SCR* can be taken into account by multiplying the THD_{u_L} -values with the *SCR* depending $corr_{u_L}$ -value given in figure 3.3 of chapter 3.6.2 b).

The worst case values for THD_{u_L} in dependancy on the switching frequency are presented in figure 3.8 d) for off-line optimized and carrier based PWM.

Also here, the off-line optimized PWM will only be slightly better in the lower switching frequency range up to about $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]). For higher switching frequencies, both modulation schemes yield almost the same results.

Further, it is interesting that also with regard to THD_{u_L} , FFM modulation yields by far the best results.

Last but not least, as well the total harmonic distortion THD of the AC-side currents i_{ph} will be of interest, which will be presented in the next sub-chapter.

e) THD of the AC-side currents i_{ph}

According to eqn. (3.9) (*THD* of the AC-system voltages u_{Lph}), the corresponding quantity for the AC-side currents i_{ph} is defined by eqn. (3.10):

$$THD_{i} = \frac{\sqrt{\sum_{K} I_{k}^{2}}}{I_{1}} \qquad k \in K = 5,7,11,13,\dots \quad (3.10)$$

In eqn. (3.10), I_k denotes the amplitude of the k-th AC-side current harmonic and I_1 the amplitude of the AC-side current fundamental, which here is presupposed to be $I_1 = 1$ [p.u.]. Further, the calculation of the THD_i includes all harmonic orders up to k=500.

More, as mentioned yet in chapter 3.6.1, this total harmonic distortion THD_i represents worst -case values, hereby assuming an infinite strong

AC-system. Hence, for a given AC-system strength SCR, the THD_i -values will have to be multiplied by an appropriate correction factor $corr_i$ (figure 3.3 in chapter 3.6.2).

The particular THD_i worst case values are presented in figure 3.8 e) in dependancy on the switching frequency for both off-line optimized and carrier based PWM.

It is an interesting fact, that the achieved results are qualitatively very similar to those achieved in sub-chapter b) for the peak-values of the AC-side currents i_{ph} . Hence, the statements made in sub-chapter b) will also prove right for the THD_i -values investigated here in sub-chapter e).

3.8 Compatibility with control requirements

Up to now, the investigations of the modulation schemes exclusively focused on the utilization of the 3-level VSI and the harmonic pollution of the AC-system. With regard to these topics, the results showed that at least for lower switching frequencies, off-line optimized PWM is slightly better suited for transmission applications than carrier based PWM.

However, another important topic concerns the compatibility of the modulation schemes with control requirements, which will shortly be discussed in this chapter. For further informations, the reader is referred to [48] and [49].

If the demands on the control speed are high (response time to load steps in between a few milliseconds), as it is a must e.g. in power quality applications, off-line optimized PWM is not suited to fulfil this task. Then, carrier based PWM will clearly be the better choice.

According to [30], off-line optimized PWM will excite low frequency oscillations, which are badly damped in a high power transmission system. In order to eliminate or at least to limit this undesired phenomenon to small values, the gains of the PI-controllers have to take on moderate values, which on the other hand results in a slower control performance.

However, under symmetrical operation conditions, the control actions in a high voltage AC transmission system should not be faster than 10ms to avoid the risk of the excitation of an AC-system resonance, which normally might vary between 100Hz and 250Hz. Hence, also off-line optimized PWM can compete with carrier based PWM and both modulation schemes could be applied. This proves right for e.g. SVCs, UPFCs with power ratings up to a few hundred MVA or generally all kind of applications, which are capable to increase the utilization and stability of existing AC-lines or to control its load flow.

It should be noted at this point, that control actions in an AC transmission system are defined to be fast, if the response time to a load step is in the range of 10ms to 100ms ([50]).

Exclusively during disturbances of the AC-system (voltage drops, single line faults,...) a fast control is necessary in order to protect the VSI from overcurrents/overvoltages. This in its turn can be achieved by e.g. an appropriate feedforward controller, which also can be realized with off-line optimized PWM, as shown for 3-level VSI FFM modulation in chapter 9.4.

Therefore, it can be concluded from a control point of view, that both offline optimized and carrier based PWM are suited for transmission applications, where the dynamic control demands are moderate. This normally is true in high power plants (up to a few hundred MVA), which shall improve the utilization and stability of an existing AC-system.

However, if the dynamic control demands are high, carrier based PWM is the better choice. This particularly proves right for applications concerning power quality, which usually have a power rating up to 50 MVA.

3.9 Summary

In this chapter, first the requirements for transmission applications and also for the corresponding 3-level VSI modulation schemes have been derived. These demands include a high modulation index m for the switching functions s_{ph} in order make profit of a high utilization of the 3-level VSI.

Further, a low harmonic distortion of the pulse patterns is highly desirable. This reduces the need for installing cost intensive large filters necessary to fulfil the very strict norms concerning harmonic pollution of an AC transmission system.

This chapter was focusing on synchronous modulation schemes with pulse patterns having a symmetry to a quarter of a period. With that it is ensured, that their harmonics will exclusively be integer numbered multiples of the AC-system fundamental frequency. In addition, no even numbered switching function harmonics will appear.

Two types of synchronous modulation schemes, the off-line optimized

PWM with selective elimination of particular harmonics and a sophisticated carrier based PWM method have been investigated further in depth and compared.

This sophisticated carrier based PWM is especially well suited for transmission applications compared to other carrier based PWM schemes, since its carrier frequencies can be chosen much higher (by a factor of 1.5 to 2!) than the resulting switching frequencies of the pulse patterns. Hence, a remarkable improvement of the harmonic content will be achieved. Further, high modulation indices up to 1.155 can be chosen, while simultaneously the minimum pulse length is limited to still reasonable values larger than $50\mu s$ for switching frequencies up to 350Hz.

Both modulation schemes have been investigated in a frequency range between 50 Hz - 1450 Hz and compared with regard to the following system design parameters:

- filter sizes on the AC-side
- the modulation indices m
- the peak-values of the AC-side phase currents i_{nh}
- necessary power rating of the 3-level VSI
- the total harmonic distortion (THD) of both the AC-system voltages u_{Lph} and the AC-side currents i_{ph}

From this it could be concluded that exclusively with respect to the filter sizes and only in the lower switching frequency range up to a few hundred Hz, off-line optimized PWM showed up advantages compared to the carrier based method. Concerning the other design parameters, merely slightly better results could be observed for off-line optimized PWM.

For higher switching frequencies than about 250Hz however, both modulation schemes are almost equal.

This clearly shows that sophisticated carrier based PWM can thoroughly be a real alternative to off-line optimized methods.

Finally, the suitability of these two modulation schemes with respect to control demands and performance has been discussed. From this it could be concluded, that off-line optimized PWM is well suited for transmission applications with moderate dynamic control demands (power system stability and utilization improvement).

Carrier based PWM in its turn is capable to cover a much wider range of

transmission applications, also including those concerning power quality, which might ask for high dynamic control requirements.

Therefore, it can be summarized, that both off-line optimized PWM and carrier based PWM are quite well suited for transmission applications. However, regarding carrier based PWM, sophisticated control and carrier signals are a must in order to compete with off-line optimized PWM.

4 Qualitative harmonic analysis

4.1 Overview

Basing on the 3-level VSI equations derived in chapter 2, a qualitative harmonic analysis is performed, showing the principles of the harmonic transfer from the AC- to the DC-side and vice versa. This is done for both symmetrical and asymmetrical operation conditions. In addition the differences with regard to the 2-level VSI are discussed.

Moreover, it will be shown that the Neutral-Point (NP) potential inherently oscillates with a 3rd harmonic (and its odd numbered multiples) for symmetrical operation conditions and with a fundamental component for asymmetrical operation conditions.

Further, this analysis will be valid for all 3-level VSI operation modes (any reactive or active power exchange with the AC-system).

Quantitative simulation results for a realistic dimensioned 3-level VSI SVC (pure reactive power exchange with the AC-system) will be presented in chapter 6.

4.2 Motivation

The motivation to perform a qualitative harmonic analysis can be described by the following two reasons:

- derivation of rules, showing how harmonics are transferred from the $AC \rightarrow DC$ -side and the $DC \rightarrow AC$ -side. With that the appearing harmonic orders in the individual 3-level VSI quantities can be calculated (particularly those, which are not known from the 2-level VSI).
- knowledge of the individual harmonic orders of the 3-level VSI quantities, in order to explain some interesting phenomenons, which will be discussed in depth in chapter 6.4, chapter 6.6 and chapter 7.3.

A qualitative harmonic analysis for the 2-level VSI has been presented in [51] and, by means of simulations, for the 3-level VSI in [30]. In this thesis a mathematical analysis will be performed for the 3-level VSI to get an in

depth understanding valid for all applications. Especially the influence of u_{phdiff} and i_0 (terms which are not known from the 2-level VSI), both for symmetrical and asymmetrical operation, is of high interest.

The following chapter will first focus on a suitable mathematical description of the 3-level VSI quantities needed for the qualitative harmonic analysis.

Then a DC-side harmonic analysis (harmonic orders of $i_{D1/D2}$, $u_{D1/D2}$, i_0 ,...) for symmetrical operation conditions will be performed. This yields the harmonic transfer rule from the AC- to the DC-side and the harmonic orders of the DC-side quantities.

In a next step, the results will be applied to the AC-side $(u_{ph}, i_{ph},...)$, including the harmonic transfer rule from the DC- to the AC-side and in addition the harmonic orders of the AC-side quantities.

The analysis will finally be extended to asymmetrical operation conditions.

It should be mentioned, that the system is assumed to be in a steady-state operating point, i.e. the DC-components of u_{D1} and u_{D2} are equal and constant. The same is true for the absolute DC-values of i_{D1} , i_{D2} and i_D .

4.3 Symmetrical operation conditions

In order to have a simpler approach to the problem, we shall start with symmetrical operation conditions, before we focus more in depth on asymmetrical conditions in chapter 4.4.

In this thesis, symmetrical operation conditions are met, if each 3-phase AC-side quantity x_{ph} , ph = a,b,c fulfils the following 2 requirements:

- x_a , x_b and x_c have the same shape
- x_a , x_b and x_c have a mutual phase-displacement of $2/3\pi$ with regard to their fundamental period.

This in its turn implies, that both the fundamental component and the particular harmonics of an AC-side quantity will either be a positive, a negative or a zero sequence component.

4.3.1 Mathematical basics

Before performing the harmonic analysis some basics have to be provided. Important quantities for this investigation are the switching functions s_{ph} and either their squared value s_{ph}^2 or their absolute value $|s_{ph}|$ respectively. Further, also the AC-currents i_{ph} have to be defined in an appropriate way.

The switching functions s_{ph} are assumed to have the following attributes:

- symmetry to half or a quarter of a period, which yields only odd numbered harmonics.
- the pulse patterns s_{ph} fulfil the requirements for symmetrical operation conditions (identical shape in the 3 phases a,b,c and mutual phase-displacement by $2/3\pi$ with respect to their fundamental period). This implies that all harmonics, which are a multiple of 3, will constitute zero sequence components.

These presumptions are valid for many off-line-optimized modulation schemes (including FFM) and can also be fulfilled for carrier based PWM as shown in chapter 3.

With regard to the calculation of harmonics it makes sense to represent the switching functions s_{ph} by means of a fourier row (appendix B.1). A description for symmetrical operation conditions is given by eqn. (4.1),

$$s_{ph} = \sum_{K} S_{k} \sin[k(\omega_{1}t + D_{ph} + \phi_{u}) + \phi_{s_{k}}]$$

$$k \in K = 1,3,5,...\infty \qquad D_{ph} = 0, -\frac{2}{3}\pi, \frac{2}{3}\pi$$
(4.1)

where S_k represents the amplitude and ϕ_{S_k} the phase angle of the k-th harmonic of s_{ph} .

 ϕ_u denotes the phase-displacement of the fundamental component of s_{ph} with regard to the fundamental of the AC-system voltages u_{Lph} . The quantitative representation of S_k , ϕ_{S_k} and ϕ_u depends on a specific application and modulation scheme and is not of importance for the following general valid analysis.

For the calculation of either s_{ph}^2 or $|s_{ph}|$, on first sight two different operations have to be performed. To obtain s_{ph}^2 , eqn. (4.1) only has to be squared, while the calculation of $|s_{ph}|$ in addition asks for the square root operation $(|s_{ph}| = +\sqrt{s_{ph}^2}, [52])$.

However, due to the fact that s_{ph} exclusively takes on the values -1, 0 or +1, the square root operation $+\sqrt{s_{ph}^2}$ will not affect the value of s_{ph}^2 . Therefore $|s_{ph}|$ will equal to $|s_{ph}| = s_{ph}^2$.

Squaring eqn. (4.1), hereby using the trigonometric function ([52])

$$\sin x \sin y = 1/2 \cdot \left[\cos(x-y) - \cos(x+y)\right]$$

yields eqn. (4.2).

$$\begin{split} s_{ph}^{2} &= \left| s_{ph} \right| = \frac{1}{2} \left\{ \sum_{K} \sum_{L} S_{k} S_{l} \cos[(k-l)(\omega_{1}t + D_{ph} + \phi_{u}) + \phi_{S_{k}} - \phi_{S_{l}}] (4.2) \right. \\ &\left. - \sum_{K} \sum_{L} S_{k} S_{l} \cos[(k+l)(\omega_{1}t + D_{ph} + \phi_{u}) + \phi_{S_{k}} + \phi_{S_{l}}] \right\} \\ &\left. k, l \in K, L = 1, 3, 5, 7 \dots \qquad |k \pm l| = 0, 2, 4, 6, \dots \end{split}$$

To derive an expression for the AC-side currents i_{ph} , it is assumed in a first step that u_{Dsum} is a pure DC-component and u_{Ddiff} equals 0. Then the ACcurrents i_{ph} will have the same harmonics as the switching functions s_{ph} , except of the zero sequence components. This is due to the fact, that the zero sequence components are cophasal and therefore do not find a path to flow, if the starpoint S in figure 2.3 is not connected to the neutral point NP. With that, i_{ph} is described by eqn. (4.3).

$$i_{ph} = \sum_{K} I_k \sin[k(\omega_1 t + D_{ph} + \phi_u) + \phi_{S_k} + \phi_{I_k}]$$

$$k \in K = 1, 5, 7, 11...\infty$$
(4.3)

Herein I_k is the amplitude of the k-th harmonic of i_{ph} , and ϕ_{I_k} is the phase angle between the k-th harmonics of s_{ph} and i_{ph} .

Further, s_{ph} , s_{ph}^2 or $|s_{ph}|$ and i_{ph} have to be separated in their symmetrical components (positive, negative or zero sequence component) ([53]) according to table 4.1 - table 4.3.

decomposition of s_{ph} in	harmonic order <i>l</i>	
positive sequence components	$l = 6 \cdot i + 1$	i = 0, 1, 2, 3
negative sequence components	$l = 6 \cdot i - 1$	i = 1, 2, 3
zero sequence components	$l = 6 \cdot i + 3$	i = 0, 1, 2, 3

table 4.1: decomposition of s_{ph} in symmetrical components for symmetrical operation conditions

decomposition of s_{ph}^2 or $ s_{ph} $ in	harmonic order l	
positive sequence components	$l = 6 \cdot i + 4$	i = 0, 1, 2, 3
negative sequence components	$l = 6 \cdot i - 4$	i = 1, 2, 3
zero sequence components	$l = 6 \cdot i$	i = 0, 1, 2, 3

table 4.2: decomposition of s_{ph}^2 or $|s_{ph}|$ in symmetrical components for symmetrical operation conditions

decomposition of i_{ph} in	harmonic order k	
positive sequence components	$k = 6 \cdot j + 1$ $j = 0, 1, 2, 3$	
negative sequence components	$k = 6 \cdot j - 1$ $j = 1, 2, 3$	
zero sequence components	none	

table 4.3: decomposition of
$$i_{ph}$$
 in symmetrical components for symmetrical operation conditions (and ripplefree DC-side voltages)

This decomposition in symmetrical components will be of great help for the analysis to come.

Now the basics are provided and we can focus on the derivation of the DCside harmonic orders.

4.3.2 DC-side harmonics

According to eqn. (2.23) - eqn. (2.30), the DC-side currents i_{D1} , i_{D2} and i_0 are a function of the following product terms which are summed up over the 3 phases a,b,c.

$$\sum_{ph = a,b,c} i_{ph} \cdot s_{ph} \quad \text{and} \quad \sum_{ph = a,b,c} i_{ph} \cdot s_{ph}^2 \quad \text{or} \quad \sum_{ph = a,b,c} i_{ph} \cdot |s_{ph}| \,.$$

Since i_{ph} , s_{ph} , s_{ph}^2 or $|s_{ph}|$ are represented by means of a fourier row, the product of their rows yields a sum of product terms of particular, also different ordered, harmonics.

As an example, we now want to consider only one of these particular product terms, which consists of the k-th current harmonic i_{phk} and the l-th switching function harmonic s_{phl} , needed for the calculation of i_{D1} and i_{D2} (eqn. (2.23)-(2.25)). The contribution $i_{D1/D2}^*$ of i_{phk} and s_{phl} to the harmonic content of i_{D1} and i_{D2} can be expressed by

$$i_{D1/D2}^* = \pm \frac{1}{2} \cdot \sum_{ph} i_{phk} \cdot s_{phl}.$$

Inserting the individual expressions i_{phk} and s_{phl} of eqn. (4.1) and eqn. (4.3) and using the trigonometric function ([52])

$$\sin x \sin y = 1/2 \cdot [\cos(x-y) - \cos(x+y)]$$

yields the following equation:

$$i_{D1/D2}^{*} = \pm 1/4I_{k}S_{l} \cdot \left\{ \sum_{ph=a,b,c} \cos[(k-l)(\omega_{1}t + D_{ph} + \phi_{u}) + \phi_{S_{k}} - \phi_{S_{l}} + \phi_{I_{k}}] - \sum_{ph=a,b,c} \cos[(k+l)(\omega_{1}t + D_{ph} + \phi_{u}) + \phi_{S_{k}} + \phi_{S_{l}} + \phi_{I_{k}}] \right\}$$

Inserting any positive or negative sequence orders k and l from table 4.1 and table 4.3 (decomposition of i_{ph} and s_{ph} in symmetrical components) yields the following result:

one of the two sum term forms a symmetrical 3-phase system, which adds to 0, while the other one forms a zero sequence system, the amplitude of which results to the triple value of the individual harmonics' amplitude.

Therefore, $i_{D1/D2}^*$ always is described by only one harmonic and not, as could be expected, by two. Further, it depends on the combination of the phase sequences of i_{phk} and s_{phl} , which harmonic order, k-l or k+l, is not present in $i_{D1/D2}^*$ and which contributes to it.

However, if one of the two AC-side harmonics i_{phk} or s_{phl} is a zero sequence component, both sum terms form a symmetrical 3-phase system, which adds to 0. Hence, no harmonic will appear on the DC-side. More, assuming that both AC-side harmonics constitute a zero sequence component (which is only possible if the starpoint S in figure 2.3 is connected to the neutral point NP), both sum terms form a zero sequence system. Then two harmonics with orders k - l and k + l appear on the DC-side.

With that the harmonic transfer rule from the AC- to the DC-side for symmetrical operation conditions can be formulated as presented in table 4.4.

This harmonic transfer rule from the AC- to the DC-side is also summarized in table 4.5, assuming that the AC-side currents do not have zero sequence For symmetrical operation conditions, each AC-side current harmonic i_{phk} of the order k and each switching function harmonic s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ of the order l is described by either a positive or a negative or a zero sequence component.

• If the AC-side current harmonic i_{phk} and the switching function harmonic s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ are either positive or negative sequence components, their convolution $(i_{phk} \text{ with } s_{phl} \text{ or } s_{phl}^2)$ or $|s_{ph}|_l$) results in one single DC-side harmonic of the order p.

If the AC-side current harmonic i_{phk} and the switching function harmonic s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ have the same / different phase sequences, the resulting order p on the DC-side will be the difference k-l / sum k+l of the particular AC-side harmonic orders.

- However, if either the AC-side current harmonic i_{phk} or the switching function harmonic s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ is a zero sequence component, no corresponding harmonic appears on the DC-side.
- If both the AC-side current harmonic i_{phk} and the switching function harmonic s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ constitute a zero sequence component, their convolution yields two harmonics on the DC-side with orders equal to the sum k+l and the difference k-l of the particular AC-side harmonic orders. However, usually the AC-side current will not include zero sequence components.

table 4.4: Harmonic transfer rule from the AC- to the DC-side for symmetrical operation conditions

components.

Note, that the above presented transfer rule does not apply for asymmetrical operation conditions, which will be studied in chapter 4.4.

Now it is easy to deduce, which harmonics are to be expected in the sum terms $\sum_{ph} i_{ph} \cdot s_{ph}$ and $\sum_{ph} i_{ph} \cdot s_{ph}^2$ or $\sum_{ph} i_{ph} \cdot |s_{ph}|$, describing the DC-side currents.

Applying the harmonic transfer rule to all sequence system combinations of i_{phk} with s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ (table 4.1 - 4.3) and summarizing the particular results yields table 4.6.

With that and the equations for i_{D1} , i_{D2} and i_0 (eqn. (2.23) - (2.30)), the

AC-side	AC-side	DC-side
seq. sys- tem i _{phk}	seq. system s_{phl}, s_{phl}^2 or $ s_{ph} _l$	$\sum_{ph} i_{phk} \cdot s_{phl}, \sum_{ph} i_{phk} \cdot s_{phl}^2 \text{ or } \sum_{ph} i_{phk} \cdot s_{ph} _l =$
pos. seq.	pos. seq.	harmonic with order $ k - l $
pos. seq.	neg. seq.	harmonic with order $k + l$
neg. seq.	pos. seq.	harmonic with order $k + l$
neg. seq.	neg. seq.	harmonic with order $ k - l $
pos. seq.	zero seq.	0
neg. seq.	zero. seq.	0

table 4.5: Harmonic transfer rule for the resulting harmonic orders in the DC-side quantities in dependancy on the phase sequences of the AC-side harmonics for symmetrical operation conditions

sum term	harmonic orders p in the sum term	
$\sum_{ph} i_{ph} \cdot s_{ph}$	$p = 6 \cdot n$	n = 0, 1, 2, 3
$\sum_{ph} i_{ph} \cdot s_{ph}^2$ Or $\sum_{ph} i_{ph} \cdot s_{ph} $	$p = 6 \cdot n + 3$	n = 0, 1, 2, 3

table 4.6: harmonic orders of $\sum_{ph} i_{ph} \cdot s_{ph}$, $\sum_{ph} i_{ph} \cdot s_{ph}^2$ or $\sum_{ph} i_{ph} \cdot |s_{ph}|$ for symmetrical operation conditions

harmonic orders of the DC-side currents are known and presented in table 4.7.

In order to derive the harmonic orders of the DC-side voltages u_{D1} , u_{D2} , their sum u_{Dsum} (the total DC-side voltage) and their difference u_{Ddiff} , we refer to eqn. (2.34) - eqn. (2.37), which describe their dependancy on the DC-side currents. Knowing the harmonic orders of i_{D1} , i_{D2} and i_0 (table 4.6), those of the DC-side voltages are also determined. Hereby the source/sink current i_D is assumed to have the same harmonic orders as i_{D1} and i_{D2} . The result is shown in table 4.8.

DC-side current	harmonic orders p in the DC-side currents	
i _{D1}	$p = 3 \cdot n$	n = 0, 1, 2, 3
i _{D2}	$p = 3 \cdot n$	n = 0, 1, 2, 3
i ₀	$p = 6 \cdot n + 3$	n = 0, 1, 2, 3

table 4.7: harmonic orders of the DC-side currents i_{D1} , i_{D2} and i_0 for symmetrical operation conditions

DC-side voltage	harmonic orders p in the DC-side voltages	
<i>u</i> _{D1}	$p = 3 \cdot n$	n = 0, 1, 2, 3
<i>u</i> _{D2}	$p = 3 \cdot n$	n = 0, 1, 2, 3
u _{Dsum}	$p = 6 \cdot n$	n = 0, 1, 2, 3
u _{Ddiff}	$p = 6 \cdot n + 3$	n = 0, 1, 2, 3

table 4.8: harmonic orders of the DC-side voltages u_{D1} , u_{D2} , u_{Dsum} and u_{Ddiff} for symmetrical operation conditions

It should be emphasized, that the individual voltages u_{D1} and u_{D2} comprise all harmonic orders, which are equal to a multiple of 3, while the sum of both, u_{Dsum} , only points to harmonic orders being a multiple of 6. This is due to the fact, that the odd numbered harmonics in u_{D1} and u_{D2} have the same amplitude but a phase-displacement by π (eqn. (2.34), eqn. (2.35) in chapter 2.4.3). Therefore they will be eliminated in the sum. Analog considerations can be performed for u_{Ddiff} yielding the conclusion that u_{Ddiff} contributes with harmonics, being exclusively odd numbered multiples of 3.

Since the voltage stress of the 3-level VSI valves is determined by the particular DC-side voltages $u_{D1/D2}$ and not by their sum u_{Dsum} (as it is true for the 2-level VSI), additional harmonics (all odd numbered of 3) have to be taken into account. Therefore an increased stress for the 3-level VSI valves can be expected. The dependancy of these undesirable harmonics on a specific 3-level VSI operation mode (pure active/reactive power), on the modulation index of the switching functions and its switching frequency will be investigated more in depth in chapter 5. Further, a quantitative verification by means of a Static VAr Compensator application will be presented in chapter 6. More, the number of the harmonic orders in the DC-side quantities will even increase, if the presumption of identical shaped switching functions s_{ph} is no longer fulfilled. This e.g. proves right for carrier based PWM with one carrier wave for all 3 phases a,b,c and carrier frequencies being not a multiple of 3 of the fundamental frequency. This kind of pulse patterns do not coincide with the assumed requirements for symmetrical operation conditions, since particular harmonics cannot be described by exclusively one symmetrical component (pos. or neg. or zero sequence). With respect to these modulation schemes, the harmonic transfer rule from the AC- to the DC-side has to be extended, which will be performed in chapter 4.4.

Finally it should be recalled in mind, that the voltage stress of the 2level VSI valves for symmetrical operation conditions is exclusively determined by harmonic orders being multiples of 6.

4.3.3 AC-side harmonics

Now we want to focus on the AC-side. The 3-level VSI output voltages u_{ph} (eqn. (2.7) or eqn. (2.8)) are separated in two terms u_{phsum} and u_{phdiff} , which are the basis for the derivation of the harmonic transfer rule from the DC- to the AC-side. For clearness reasons, they are presented here once again.

$$u_{phsum} = \frac{s_{ph}}{2} \cdot u_{Dsum} \qquad u_{phdiff} = \frac{s_{ph}^2}{2} \cdot u_{Ddiff} = \frac{|s_{ph}|}{2} \cdot u_{Ddiff}$$

Recalling in mind, that s_{ph} , s_{ph}^2 , $|s_{ph}|$, u_{Dsum} and u_{Ddiff} are described by means of fourier rows, both u_{phsum} and u_{phdiff} are calculated by a sum of product terms of particular harmonics. Again, using the trigonometric function ([52])

$$\sin x \sin y = 1/2 \cdot [\cos(x-y) - \cos(x+y)]$$

yields the general harmonic transfer rule from the DC- to the AC-side in table 4.9.

It should be pointed out, that this *harmonic transfer rule from the DC- to the AC-side* is valid for both symmetrical and asymmetrical operation conditions.

Each product term consisting of any k-th AC-side switching function harmonic s_{phk} , s_{phk}^2 or $|s_{ph}|_k$ with any *l*-th DC-side voltage harmonic u_{Dsuml} or u_{Ddiffl} results in a sum term of two harmonics on the AC-side with orders equal to the sum k + l and the difference k - l of the individual harmonic orders k and l.

The phase sequence of the resulting AC-side harmonics with the orders k + l and k - l is determined according to the following rule:

- for the AC-side harmonic with the order k+l, the phase sequence will be the same than those of the k-th switching function harmonic s_{phk} , s_{phk}^2 or $|s_{ph}|_k$.
- for k-l>0, the phase sequence of the AC-side harmonic with the order k-l will be the same than those of the k-th switching function harmonic s_{phk} , s_{phk}^2 or $|s_{ph}|_k$.
- for k l < 0, the phase sequence of the AC-side harmonic with the order k - l will be opposite signed than those of the k-th switching function harmonic s_{phk} , s_{phk}^2 or $|s_{ph}|_k$.
- In case that the k-th switching function harmonic s_{phk} , s_{phk}^2 , or $|s_{ph}|_k$ is a zero sequence system, both resulting AC-side harmonics with the orders k+l and k-l will also be zero sequence systems.
- table 4.9: General harmonic transfer rule from the DC- to the ACside for both symmetrical and asymmetrical operation conditions

Applying the harmonic transfer rule to all sequence system combinations of u_{Dsuml} and u_{Ddiffl} with s_{phk} , s_{phk}^2 or $|s_{ph}|_k$ (table 4.1 - 4.2, table 4.8) and sorting for the phase sequences results in table 4.10.

In comparison to the 2-level VSI, the 3-level VSI contributes with an additional term (u_{phdiff}) to the harmonics in u_{ph} . As emphasized yet, neglecting this term by assuming $u_{D1} = u_{D2}$ might yield surprising results, as discussed in chapter 6, and makes it impossible to perform a DC-side self-balancing analysis (chapter 7.4).

However, both the harmonic orders and the related phase sequences are the same in u_{phsum} and u_{phdiff} . For that reason table 4.10 can be simplified to table 4.11, summarizing the harmonic orders in u_{ph} .

$u_{phsum} = \frac{s_{ph}}{2} \cdot u_{Dsum}$	harmonic orders p
pos. seq. components	$p = 6 \cdot n + 1$ $n = 0, 1, 2, 3$
neg. seq. components	$p = 6 \cdot n - 1$ $n = 1, 2, 3$
zero seq. components	$p = 6 \cdot n + 3$ $n = 0,1,2,3$
$u_{phdiff} = \frac{s_{ph}^2}{2} \cdot u_{Ddiff}$ or $u_{phdiff} = \frac{ s_{ph} }{2} \cdot u_{Ddiff}$	harmonic orders <i>p</i>
pos. seq. components	$p = 6 \cdot n + 1$ $n = 0, 1, 2, 3$
neg. seq. components	$p = 6 \cdot n - 1$ $n = 1, 2, 3$
zero seq. components	$p = 6 \cdot n + 3$ $n = 0, 1, 2, 3$

table 4.10: harmonic orders of u_{phsum} and u_{phdiff} for symmetrical operation

u _{ph}	harmonic orders p	
pos. seq. components	$p = 6 \cdot n + 1$	n = 0, 1, 2, 3
neg. seq. components	$p = 6 \cdot n - 1$	n = 1, 2, 3
zero seq. components	$p = 6 \cdot n + 3$	$n = 0, 1, 2, 3 \dots$

table 4.11: harmonic orders of u_{ph} for symmetrical operation

Concerning the AC-currents i_{phsum} , i_{phdiff} and i_{ph} the same harmonic orders except of the zero sequence components, which do not find a path to flow, are to be expected according to table 4.12 - table 4.13.

By comparison of table 4.13 with table 4.3, it can be seen that the harmonics in u_{Dsum} and u_{Ddiff} do not introduce other harmonic orders in i_{ph} than those appearing for ripple-free DC-side voltages (table 4.3).

i _{phsum}	harmonic orders p	
pos. seq. components	$p = 6 \cdot n + 1$	n = 0, 1, 2, 3
neg. seq. components	$p = 6 \cdot n - 1$	n = 1, 2, 3
i_{phdiff}	harmonic o	orders p
<i>i_{phdiff}</i> pos. seq. components	$p = 6 \cdot n + 1$	n = 0, 1, 2, 3

table 4.12: harmonic orders of i_{phsum} and i_{phdiff} for symmetrical operation

i _{ph}	harmonic orders p
pos. seq. components	$p = 6 \cdot n + 1$ $n = 0, 1, 2, 3$
neg. seq. components	$p = 6 \cdot n - 1$ $n = 1, 2, 3$

table 4.13: harmonic orders of i_{ph} for symmetrical operation

4.4 Asymmetrical operation conditions

In the previous chapter the harmonic transfer rules and the resulting harmonic orders of the individual 3-level VSI quantities were derived for symmetrical operation conditions. In a next step, the same will be performed for asymmetrical operation conditions.

In this thesis, asymmetrical operation conditions are met, if at least one 3-phase AC-side quantity x_{ph} , ph = a,b,c fulfils one or all of the following requirements:

- x_a, x_b and x_c do not have the same shape
- x_a , x_b and x_c do not have a mutual phase-displacement of $2/3\pi$ with regard to their fundamental period.

Then, in general, the fundamentals and each particular harmonic cannot be described by exclusively one symmetrical component, but has to be decomposed in a sum of positive, negative and zero sequence components.

In the analysis to follow, the operation with both asymmetrical AC-side cur-

rents and asymmetrical switching functions will be assumed. These asymmetrical conditions might be caused e.g. by line faults of the AC-system voltages U_{Lph} and an appropriate control scheme to compensate for them. The procedure to perform the analysis is the same as shown in chapter 4.3.

4.4.1 Mathematical basics

The description of s_{ph} for asymmetrical operation conditions by means of a fourier row is given by eqn. (4.4).

$$s_{ph} = \sum_{K} S_{phk} \sin[k(\omega_1 t + D_{ph}) + \phi_{S_{phk}}]$$

$$k \in K = 1,3,5,7... \quad D_{ph} = \text{any value}$$
(4.4)

In general the particular harmonic amplitudes S_{phk} and phase-displacements $\phi_{S_{phk}}$ do not have the same values in all 3 phases ph = a,b,c. Also D_{ph} may take on any values. However, each individual switching function s_{ph} still fulfils the attribute to be symmetrical to half or a quarter of a period (only odd numbered harmonics).

With that, s_{ph}^2 or $|s_{ph}|$ and i_{ph} are determined according to eqn. (4.5) and eqn. (4.6). Concerning i_{ph} , it is assumed in a first step that u_{Dsum} is a pure DC-component and u_{Ddiff} equals 0.

$$(4.5)$$

$$s_{ph}^{2} = |s_{ph}| = \frac{1}{2} \left\{ \sum_{K} \sum_{L} S_{phk} S_{phl} \cos[(k-l)(\omega_{1}t + D_{ph}) + \phi_{S_{phk}} - \phi_{S_{phl}}] - \sum_{K} \sum_{L} S_{phk} S_{phl} \cos[(k+l)(\omega_{1}t + D_{ph}) + \phi_{S_{phk}} + \phi_{S_{phl}}] \right\}$$

$$k, l \in K, L = 1, 3, 5, 7... \qquad |k \pm l| = 0, 2, 4, 6, ...$$

$$i_{ph} = \sum_{K} I_{phk} \sin[k(\omega_{1}t + D_{ph}) + \phi_{S_{phk}} + \phi_{I_{phk}}]$$

$$k \in K = 1, 5, 7, 11... \qquad (4.6)$$

The decomposition of s_{ph} , s_{ph}^2 or $|s_{ph}|$ and i_{ph} in symmetrical components is given in table 4.14- table 4.16.

decomposition of s_{ph} in	harmonic order l	
positive sequence components	$l = 2 \cdot i + 1$	i = 0, 1, 2, 3
negative sequence components	$l = 2 \cdot i + 1$	i = 0, 1, 2, 3
zero sequence components	$l = 2 \cdot i + 1$	i = 0, 1, 2, 3

table 4.14: decomposition of s_{ph} in symmetrical components for asymmetrical operation conditions

decomposition of s_{ph}^2 or $ s_{ph} $ in	har	monic order <i>l</i>
positive sequence components	$l = 2 \cdot i$	i = 0, 1, 2, 3
negative sequence components	$l = 2 \cdot i$	i = 1, 2, 3
zero sequence components	$l = 2 \cdot i$	i = 0, 1, 2, 3

table 4.15: decomposition of s_{ph}^2 or $|s_{ph}|$ in symmetrical components for asymmetrical operation conditions

decomposition of i_{ph} in	harm	ionic order k
positive sequence components	$k = 2 \cdot j + 1$	j = 0, 1, 2, 3
negative sequence components	$k = 2 \cdot j + 1$	j = 0, 1, 2, 3
zero sequence components		none

table 4.16: decomposition of i_{ph} in symmetrical components for asymmetrical operation conditions

4.4.2 DC-side harmonics

In order to calculate the DC-side harmonics, first the harmonic transfer rule from the AC- to the DC-side for asymmetrical operation conditions will be derived.

į

As just shown, each harmonic of i_{ph} , s_{ph} , s_{ph}^2 or $|s_{ph}|$ for asymmetrical operation conditions is generally described by more than only one symmetrical component, which can be expressed by the following equations:

$$i_{phk} = i_{phk_{pos}} + i_{phk_{neg}}$$
$$s_{phl} = s_{phl_{pos}} + s_{phl_{neg}} + s_{phl_{zero}}$$

$$s_{phl}^2 = s_{phl_{pos}}^2 + s_{phl_{neg}}^2 + s_{phl_{zero}}^2$$
 or $|s_{ph}|_l = |s_{ph}|_{l_{pos}} + |s_{ph}|_{l_{neg}} + |s_{ph}|_{l_{zero}}$

Herein, the index *pos* denotes the positive sequence component, *neg* the negative sequence component and *zero* the zero sequence component of the particular AC-side current and switching function harmonics with orders k and l.

As a consequence, each sum term $\sum_{ph} i_{phk} \cdot s_{phl}$, $\sum_{ph} i_{phk} \cdot s_{phl}^2$ or $\sum_{ph} i_{phk} \cdot |s_{ph}|_l$ consists of 6 sub-sum terms as exemplified below for $\sum_{ph} i_{phk} \cdot s_{phl}$ (eqn. (4.7)).

$$\sum_{ph} i_{phk} \cdot s_{phl} = \sum_{ph} (i_{phk_{pos}} + i_{phk_{neg}}) \cdot (s_{phl_{pos}} + s_{phl_{neg}} + s_{phl_{zero}})$$

$$= \sum_{ph} i_{phk_{pos}} \cdot s_{phl_{pos}} + \sum_{ph} i_{phk_{pos}} \cdot s_{phl_{neg}} + \sum_{ph} i_{phk_{pos}} \cdot s_{phl_{zero}}$$

$$+ \sum_{ph} i_{phk_{neg}} \cdot s_{phl_{pos}} + \sum_{ph} i_{phk_{neg}} \cdot s_{phl_{neg}} + \sum_{ph} i_{phk_{neg}} \cdot s_{phl_{zero}}$$

$$(4.7)$$

According to the harmonic transfer rule from the AC- to the DC-side for symmetrical operation conditions, each of these 6 sub-sum terms might now contribute with a DC-side harmonic. The order of these harmonic (k + l or k - l) will be determined by the particular sequence system combination (*pos/pos, pos/neg, pos/zero,...*) of i_{phk} and s_{phl} .

Since hereby different sequence system combinations have to be considered, the resulting harmonic contribution of all 6 sub-sum terms to the DC-side can include harmonics of both the order k + l and k - l. This is summarized in the harmonic transfer rule from the AC- to the DC-side for asymmetrical operation conditions in table 4.17.

Now the harmonic orders of the sum terms $\sum_{ph} i_{ph} \cdot s_{ph}$ and $\sum_{ph} i_{ph} \cdot s_{ph}^2$ or $\sum_{ph} i_{ph} \cdot |s_{ph}|$, which determine the DC-side quantities, can be calculated by applying the above derived transfer rule (table 4.17) to table 4.14 - table 4.16. The result is presented in table 4.18.

For asymmetrical operation conditions, each AC-side current harmonic i_{phk} of the order k and each switching function harmonic s_{phl} , s_{phl}^2 or $|s_{ph}|_l$ of the order l is in general described by the sum of both a positive and a negative and a zero sequence component.

Therefore, the convolution of an AC-side current harmonic i_{phk} of the order k with a switching function harmonic s_{phl} , s_{phl}^2 or $|s_{phl}|_l$ of the order l results in a sum of product terms, each of which corresponds to one of the possible sequence system combinations.

These product terms individually contribute to the DC-side harmonics according to the harmonic transfer rule from the AC- to the DC-side for symmetrical operation conditions.

Since the sequence system combinations of the particular product terms are different, the total DC-side contribution usually results in two harmonics with orders of both the sum k + l and the difference k - l of the individual AC-side harmonic orders k and l.

table 4.17:	Harmonic transfer rule from the AC- to the DC-side for
	asymmetrical operation conditions

sum term	harmo	nic orders p
$\sum_{ph} i_{ph} \cdot s_{ph}$	$p = 2 \cdot n$	n = 0, 1, 2, 3
$\sum_{ph} i_{ph} \cdot s_{ph}^2$	$p=2\cdot n+1$	n = 0,1,2,3
$\sum_{ph} i_{ph} \cdot s_{ph} $		

table 4.18: harmonic orders of $\sum_{ph} i_{ph} \cdot s_{ph}$, $\sum_{ph} i_{ph} \cdot s_{ph}^2$ or $\sum_{ph} i_{ph} \cdot |s_{ph}|$ for asymmetrical operation conditions

With that, the harmonic orders of the DC-side currents i_{D1} , i_{D2} , i_0 (eqn. (2.23) - (2.30)) and the DC-side voltages u_{D1} , u_{D2} , u_{Dsum} , u_{Ddiff} (eqn. (2.34) - (2.37)) are known, which is documented in table 4.19 and table 4.20.

DC-side current	harmon	ic orders <i>p</i>
<i>i</i> _{D1}	p = n	n = 0, 1, 2, 3
i _{D2}	p = n	n = 0, 1, 2, 3
i ₀	$p = 2 \cdot n + 1$	n = 0, 1, 2, 3

table 4.19: harmonic orders of the DC-side currents i_{D1} , i_{D2} and i_0 for asymmetrical operation conditions

DC-side voltage	harmonic orders p	
<i>u</i> _{D1}	p = n	n = 0, 1, 2, 3
' u _{D2}	p = n	n = 0, 1, 2, 3
U _{Dsum}	$p = 2 \cdot n$	n = 0, 1, 2, 3
u _{Ddiff}	$p = 2 \cdot n + 1$	n = 0, 1, 2, 3

table 4.20: harmonic orders of the DC-side voltages u_{D1} , u_{D2} , u_{Dsum} and u_{Ddiff} for asymmetrical operation conditions

As it proves right for symmetrical operation conditions, different harmonic orders appear in the individual DC-side currents and voltages compared with their sums or differences.

Concerning the stress of the 3-level VSI valves all even and odd numbered harmonics have to be taken into account, also including a DC-(p = 0) and the fundamental harmonic component (p = 1). This will also be shown quantitatively in chapter 6.

The latter mentioned statement will further prove right for carrier based PWM with one carrier wave for all 3 phases a,b,c and carrier frequencies being not a multiple of 3 of the fundamental frequency. This is true since this kind of pulse patterns fulfil the attributes of an asymmetrical 3-phase system (no identical shape in all 3 phases a,b,c).

Last but not least it should be recalled in mind, that the voltage stress of the 2-level VSI valves for asymmetrical operation conditions is exclusively determined by only even numbered harmonics. Finally the harmonic orders of the AC-side voltages u_{ph} and currents i_{ph} can be calculated. This will be performed with the general harmonic transfer rule from the DC- to the AC-side (table 4.9, chapter 4.3.3, valid for both symmetrical and asymmetrical operation conditions). The results are presented in table 4.21 and table 4.22.

u _{ph}	harmonic orders p	
pos. seq. components	$p = 2 \cdot n + 1 \qquad n = 0,$	1,2,3
neg. seq. components	$p = 2 \cdot n + 1 \qquad n = 0,$	1,2,3
zero seq. components	$p = 2 \cdot n + 1 \qquad n = 0,$	1,2,3

table 4.21: harmonic orders of u_{ph} for asymmetrical operation conditions

i_{ph}	harmonic orders p
pos. seq. components	$p = 2 \cdot n + 1$ $n = 0, 1, 2, 3$
neg. seq. components	$p = 2 \cdot n + 1$ $n = 0, 1, 2, 3$

table 4.22: harmonic orders of i_{ph} for asymmetrical operation conditions

Also here, it can be seen by comparison of table 4.22 with table 4.16, that the harmonics in u_{Dsum} and u_{Ddiff} do not introduce other harmonic orders in i_{ph} than those appearing for ripplefree DC voltages (table 4.16).

4.5 Summary

In this chapter, a qualitative harmonic analysis for the 3-level VSI has been performed, basing on its equations derived in chapter 2. From this, rules have been derived, describing the harmonic orders of the particular 3-level VSI quantities both for symmetrical and asymmetrical operation conditions.

It could be shown that additional harmonic orders, which are not known from the 2-level VSI, appear in the individual DC-side voltages u_{D1} and u_{D2} and the DC-side currents i_{D1} , i_{D2} and i_0 . They include all odd num-

bered multiples of 3 for symmetrical operation conditions and all odd numbered orders for asymmetrical operation conditions.

These harmonics are phase-displaced by π in u_{D1} and u_{D2} . Therefore they are eliminated in the sum $u_{Dsum} = u_{D1} + u_{D2}$ but have doubled amplitudes in the difference $u_{Ddiff} = u_{D1} - u_{D2}$.

It was further shown that these harmonics are to be expected in all applications and operation modes (reactive, active) and for all pulse patterns.

5 The harmonic DC-side oscillation

5.1 Overview

This chapter exclusively focuses on the undesirable but 3-level VSI specific harmonic oscillations in the particular DC-side voltages u_{D1} and u_{D2} .

First, the driving forces for these harmonic oscillations will be presented, which is followed by the derivation of a graphical model suitable to form a simple idea of the harmonics' generation. This graphical model also shows up the harmonic orders to be expected and indicates the fundamental influence of various parameters, e.g. the 3-level VSI operation mode (reactive, active power exchange with the AC-system) or the modulation index m of the pulse patterns s_{ph} .

The dependancy of the DC-side oscillations in u_{D1} and u_{D2} on these parameters will then be investigated more in depth, either with the help of the graphical model or simplified mathematical considerations. This will be performed for FFM modulation, off-line optimized and carrier based PWM.

In addition, also the impact of the pulse patterns switching frequency $f_{s_{ph}}$ on the DC-side oscillations in u_{D1} and u_{D2} will be studied.

5.2 Introduction

It was shown in chapter 4.3 for symmetrical operation conditions, that the two DC-side voltages u_{D1} and u_{D2} show up harmonic orders being odd numbered multiples of 3. The entirety of these harmonics will therefore result in an oscillation, whose fundamental frequency will coincide with those of a 3rd harmonic. This oscillation is not known from the 2-level VSI and highly undesirable, since it is responsible for some drawbacks, which will be discussed more in depth in chapter 6.

As proven in chapter 4.3, this harmonic oscillation is an inherent attribute of the 3-level VSI and will be present in all 3-phase 3-level VSI applications. Therefore, it is of major interest to investigate its generation and the influence of a specific operation mode on the amplitude of particular oscillation harmonics. Also the modulation index m and the switching frequency $f_{s_{ph}}$ of the chosen pulse patterns s_{ph} might result in different amplitudes for these harmonics being odd numbered multiples of 3. In the chapters to fol-
low these topics will be studied more in depth.

5.3 Driving force for the harmonic DC-side oscillation

When speaking about the 3-level VSI specific harmonic oscillation in the DC-side voltages u_{D1} and u_{D2} , the question arises for the driving force of this undesirable phenomenon. In order to find an answer, a closer look at the 3-level VSI DC-side might be very helpful. For that purpose and the investigations to come, the simplified model, introduced in chapter 2.4, will be presented here once again in figure 5.1.



fig 5.1: simplified model of a 3-level VSI connected to an AC-system

In chapter 2.4.1 the sum and the difference of the two DC-side voltages u_{D1} and u_{D2} were defined to

$$u_{Dsum} = u_{D1} + u_{D2}$$
 and $u_{Ddiff} = u_{D1} - u_{D2}$.

With that, the individual DC-side voltages u_{D1} and u_{D2} can be expressed by

$$u_{D1} = \frac{u_{Dsum} + u_{Ddiff}}{2}$$
 and $u_{D2} = \frac{u_{Dsum} - u_{Ddiff}}{2}$ (5.1)

It was further shown in chapter 4.3.2, table 4.8, that for symmetrical operation conditions, u_{Dsum} contributes with harmonic orders being multiples of six, which are also well known from the 2-level VSI. On the other side, u_{Ddiff} will be responsible for all harmonic orders being odd numbered multiples of 3, which, according to eqn. (5.1), represent the undesirable oscillation in u_{D1} and u_{D2} .

These voltages u_{Ddiff} in its turn can be expressed by

$$u_{D1} - u_{D2} = u_{Ddiff} = -\frac{1}{c} \int i_0 dt + const$$
 (5.2)

which was shown in chapter 2.4.3 (eqn. (2.37)). Inserting eqn. (5.2) in eqn. (5.1) yields eqn. (5.3).

$$u_{D1} = \frac{u_{Dsum}}{2} - \frac{1}{2} \cdot \frac{1}{c} \int i_0 dt + const$$

$$u_{D2} = \frac{u_{Dsum}}{2} + \frac{1}{2} \cdot \frac{1}{c} \int i_0 dt + const$$
(5.3)

From eqn. (5.3) it is evident that the NP-current i_0 will be the driving force for the harmonic oscillation in the DC-side voltages u_{D1} and u_{D2} . It is also evident in eqn. (5.3), that this oscillation, except of a phase-displacement by π , will be the same in both DC-side voltages.

Hence, the NP-current i_0 will be an appropriate quantity to represent the harmonic oscillation in u_{D1} and u_{D2} , if in addition the following two aspects are taken into account:

- the harmonic oscillation peak-value in u_{D1} and u_{D2} will depend on a chosen capacitor size c, which varies with the particular applications.
- due to the integral relationship, the individual harmonics in i_0 will experience a damping in u_{D1} and u_{D2} , which will be proportional to the frequency of the particular harmonics.

5.4 Generation principle of the NP-current

In this chapter, the driving forces for the NP-current i_0 and its generation principle by means of a simple graphical model will be presented. This will be performed for two appropriate 3-level VSI operation modes. For clearness and simplicity reasons, the investigations will first focus on FFM modulation, which in chapter 5.4.4 will be extended to off-line optimized and carrier based PWM.

However, it should be emphasized here, that the type of carrier based PWM used in this chapter will be distinctive to those proposed in

chapter 3.5 due to the following reasons.

Both the off-line optimized and the sophisticated carrier based PWM pulse patterns introduced in chapter 3.5 (figure 3.2) show up a very similar shape. All switching instants are concentrated in the vicinity of the pulse patterns' fundamental zero crossings, while no switching actions occur in the centre regions of each half-period. Therefore, their influence on the generation of the NP-current i_0 can also be expected to be very similar.

This is subject to change for the conventional carrier based modulation schemes (carrier frequency f_c is equal to the switching frequency $f_{s_{ph}}$), where the NP-angles are distributed over the whole period. Though really not recommended by the author for transmission applications, the influence of this kind of carrier based PWM on the arising NP-current i_0 might also be of interest.

In addition, the proposed sophisticated carrier based scheme can only be applied for modulation indices m>1. Hence, for smaller modulation indices m<1, anyhow another conventional method has to be applied, when studying the influence of the modulation index m on the arising NP-current i_0 .

5.4.1 Driving forces for the NP-current

In chapter 5.3, the NP-current i_0 has been found to be the driving force for the 3-level VSI specific harmonic oscillation in the DC-side voltages u_{D1} and u_{D2} . This sub-chapter will now concentrate on the driving forces for the NP-current i_0 itself. For that purpose, eqn. (2.28) or eqn. (2.29) in chapter 2.4.3 have to be recalled in mind and will for simplicity reasons be presented here once again:

$$i_0 = i_a \cdot (1 - s_a^2) + i_b \cdot (1 - s_b^2) + i_c \cdot (1 - s_c^2), \qquad (5.4)$$

$$i_0 = i_a \cdot (1 - |s_a|) + i_b \cdot (1 - |s_b|) + i_c \cdot (1 - |s_c|)$$
(5.5)

or

$$i_0 = \sum_{ph} i_{ph} \cdot (1 - s_{ph}^2) = \sum_{ph} i_{ph} \cdot (1 - |s_{ph}|) = \sum_{ph} i_{0ph}$$
(5.6)

It can be seen in eqn. (5.4) and eqn. (5.5), that the NP-current i_0 will be driven by the AC-side currents i_{ph} , however only during time intervals where the pulse patterns s_{ph} equal to $s_{ph} = 0$. This in its turn implies that the neutral point NP is connected to the output terminals of the 3-level

VSI, which can easily be verified in figure 5.1 and also makes sense from a physical point of view.

Hence, the NP-current i_0 will consist of pieces cut out of the AC-side currents i_{ph} . More, it is evident in eqn. (5.4) and eqn. (5.5), that the shape of these current sections will depend on both the location of the NP-angles and the relative phase-displacement of the pulse patterns s_{ph} with respect to the AC-side currents i_{ph} . This in its turn is determined by a specific 3-level VSI operation mode, which therefore might also have an influence on the NP-current i_0 . For that reason, all studies to come have been performed for two appropriate operation modes, which will be introduced in the next sub-chapter.

5.4.2 Operation mode considerations and simplifications

In order to investigate the dependancy of the NP-current i_0 on a specific 3level VSI operation mode, both the pure reactive and the pure active operation have been considered. It will be anticipated here (and confirmed in the next chapter), that the results achieved for these two operation modes are quite well suited for statements concerning the whole possible operating range of the 3-level VSI.

Pure reactive or active operation mode means that a pure reactive or pure active power will be exchanged with the AC-system. In all simulations to come, as representative cases, the 3-level VSI is assumed to generate a pure reactive power (acts like a capacitor installed on the AC-side, capacitive operation mode) or absorbs a pure active power. Hereby, according to the notation in figure 5.1, the AC-system is defined as a source, while the 3-level VSI is defined as a sink. The representation of these two operation modes by means of a phasor diagram is given in figure 5.2. With that, also the phase displacements of i_{ph} with regard to the 3-level-VSI output voltages u_{ph} and the switching functions s_{ph} can be calculated. The transformation rules from 3-phase quantities to phasor quantities are presented in appendix C.2.1.

Further it should be noted that in case the 3-level VSI absorbs a pure reactive power (pure inductive operation mode) or generates a pure active power, only the sign of the NP-current i_0 will change.

More, assuming mixed operation mode (both dominantly active and reactive power exchange) will yield quantitative values between those values achieved for pure reactive and pure active operation mode.



fig 5.2: phasor diagram for pure reactive and pure active operation mode

For the simulations to come, the AC-system is chosen to be infinitely strong $(r_L=0, l_L=0)$ and both the amplitudes of the AC-system voltages u_{Lph} and the phase currents i_{ph} will have a value of 1 [p.u.]. In addition, for clearness reasons, u_{Lph} and i_{ph} are assumed to be ideal cosinusoidal or sinusoidal, since the harmonics in these quantities can be expected not to have a major influence on the qualitative results.

Last but not least, the ohmic and inductive part of the decoupling impedance are determined to be r=0 and l=0.2[p.u.].

5.4.3 Generation principle and harmonics of the NP-current for FFM modulation

Now that the basics are derived, the generation principle for the NP current i_0 will be studied with the help of a simple graphical model.

This model consists in the simplified graphical representation of eqn. (5.4) or eqn. (5.5), describing the origin of the NP current i_0 for a chosen switching function s_{ph} and for phase currents i_{ph} corresponding to a specific operation mode.

Concerning the switching function s_{ph} , at first, the most simple one is assumed, which is FFM modulation (chapter 3.4). Hereby, the modulation index *m* was chosen to m = 1.15.

The simulation results, showing graphically the generation of i_0 , are given in figure 5.3. Herein, the left column shows the relationships for pure capacitive operation mode and the right column those for pure active operation mode. For clearness reasons, the upper graphic in each column only takes into account the contribution of one 3-level VSI phase, which is denoted i_{0ph} according to eqn. (5.6). As a representative, phase *a* is chosen in the graphics, which results in the contribution i_{0a} . The graphics in the middle of figure 5.3 present the resulting NP-current i_0 (bold line), which is completed by the amplitude spectrum of i_0 in the lower graphics. The individual graphics will be discussed in the following sub-chapters.

a) Contribution of one 3-level VSI phase to the NP-current

The considerations performed in this sub-chapter will be with respect to the contribution of exclusively one 3-level VSI phase (here: phase a) to the NP-current i_0 . Though not an all extensive comprehension of the NP-current's generation will be achieved, some important aspects can all the same be derived.

By comparison of the two upper graphics in the left and right column of figure 5.3, it can clearly be seen that the shape and the current-time area of the particular contributions i_{0a} strongly differ from each other. This is obviously caused by the different operation mode dependant phase-displacements of the phase current i_a and the switching function s_a . Hence it is confirmed that the operation mode will have a remarkable influence on the arising NP-current i_0 and with that on the harmonics in the DC-side voltages u_{D1} and u_{D2} . For example, the NP-current contribution i_{0a} in the left column, corresponding to a pure capacitive operation mode, will yield a remarkably larger oscillation in u_{D1} and u_{D2} than those in the right column, which represents a pure active operation mode.

In general, for the here given NP-angles β , the pure reactive operation mode stands for the largest DC-side voltage oscillations, while a pure active operation mode represents very small oscillation peak-values. This can easily be verified by continuously shifting the phase current i_a in the left upper graphic of figure 5.3 in any direction. Hereby, the reactive current phasor component will decrease, while simultaneously the active current phasor component will increase. The current time areas and also the peak-values of i_{0a} will decrease, which results in smaller DC-side voltage oscillations.

Graphically varying the phase-displacement of the AC-side current i_a also shows, that the smallest oscillation peak-values would be achieved, if i_a is





phase displaced by $\pi/2$ with respect to the switching functions s_a . For the given stray inductance l=0.2[p.u.], this operation mode coincides with the following current phasor components with respect to the AC-system voltage phasor \underline{u}_L :

 $i_d = \pm 0.98$ [p.u.] and $i_q = -0.2$ [p.u.]

However, the deviations between this predominant active and the pure active operation mode are quite moderate and therefore the more convenient pure active operation mode was chosen here.

Another point of interest concerns the location and the length of the NP-angles. It is evident in the upper graphics of figure 5.3, that both another location or a decreased/increased length of the NP-angle β could significantly affect the shape and the harmonics of i_{0a} . With that, also the statement concerning the oscillations' peak-values in dependancy on the operation mode might change or even turn into the opposite.

It should be noted, that the location of the NP-angles is a modulation scheme specific attribute, while their length usually depends on the chosen modulation index m of the switching functions s_{ph} . From this it is obvious that besides a specific operation mode, also the class of modulation scheme and a particular modulation index m will be decisive factors for the assessment of the arising harmonics in the DC-side voltages u_{D1} and u_{D2} . This will be investigated more in depth in chapter 5.5 for FFM modulation, off-line optimized and carrier based PWM.

However, though the shapes of the contributions i_{0a} may vary in a wide range, they all the same show up common attributes. It is obvious in the upper graphics of figure 5.3, that for all operation modes and modulation schemes the fundamental frequency of i_{0a} will coincide with those of the AC-system (f_1) . Further, harmonics being odd numbered multiples of the fundamental component (3rd, 5th, 7th,...) have to be expected here, since a symmetry to a quarter of a period is fulfilled for both s_a and i_a . However, assuming s_a or i_a to have no symmetry at all, any harmonic orders, which are multiples of the fundamental frequency of the AC-system (2nd, 3rd, 4th,...), will appear in i_{0a} .

The studies so far, basing on the simple graphical model, indicated the influence of various parameters and also showed up the harmonic orders to be expected in the NP-current contributions i_{0ph} . The results could be achieved without any complicated mathematical analyses, which also proves the great value of this graphical model.

b) Contribution of all 3-level VSI phases to the NP-current

In the previous sub-chapter, exclusively the NP-current contribution of one 3-level VSI phase, namely phase a, has been investigated. Now, also the two remaining phases b and c will be taken into account in order to obtain the resulting NP-current i_0 .

The individual FFM pulse patterns s_{ph} and AC-side currents i_{ph} show up identical shape in all 3 phases a,b,c and only differ by a phase-displacement of $2/3\pi$. Hence, the same will be true for the individual NP-current contributions i_{0ph} , which are composed of these two quantities. According to eqn. (5.6), adding all 3 contributions i_{0ph} yields the resulting NP-current i_0 , which is presented in the middler graphics of figure 5.3.

With respect to the statements in the previous paragraph, the result is not very astonishing at first sight. However, by having a closer look at the middler graphics of figure 5.3, it might be a surprise that the fundamental frequency of i_0 no longer coincides with those of the individual contributions i_{0ph} . It is obvious, that i_0 now exhibits a fundamental frequency which equals those of a 3rd harmonic on the AC-side.

Apparently, the attributes of a symmetrical 3-phase system, i.e. same shape in all 3 phases and phase displacements by $2/3\pi$, are the origin of this 3rd harmonic fundamental component in the NP-current i_0 .

Concerning the higher ordered harmonics in i_0 , it is evident in the middler graphics, that now all odd numbered multiples of 3 have to be expected (the 9th, 15th,...). With that also the harmonics with orders 5, 7,11, 13,..., are no longer present in i_0 .

However, in case of asymmetrical 3-phase conditions either for the pulse patterns s_{ph} (e.g. no identical shapes for the phases a,b,c) or the AC-side currents i_{ph} , the fundamental frequency of i_0 will furtheron be identical with those on the AC-side. This can be verified with the graphical model and was furthermore mathematically confirmed in chapter 4.4.2. More, in general all harmonics being present in i_{0ph} , will also appear in the resulting NP-current i_0 . Then, as well the two DC-side voltages u_{D1} and u_{D2} will moreover show up a low ordered harmonic with the fundamental frequency f_1 , which in addition will be badly damped by the capacitors c.

As mentioned yet in chapter 4.3.2, e.g. carrier based modulation signals with one carrier wave for all 3 phases a,b,c and carrier frequencies being not a multiple of 3 of the fundamental frequency f_1 fulfils the attributes of an asymmetrical 3-phase system. Hence, also with respect to the harmonic

oscillation of the two DC-side voltages u_{D1} and u_{D2} , these modulation signals should be avoided!

Since exclusively the symmetry attributes of the two 3-phase systems s_{ph} and i_{ph} determine the fundamental frequency and the harmonic orders of i_0 , the statements made above will prove right for all operation modes, modulation indices and switching frequencies.

The quantitative values of the fundamental component and the harmonics however are expected to be influenced by these latter mentioned parameters. As an example, it is evident in the middler graphics of figure 5.3, that the DC-side voltage oscillations generated with a pure capacitive operation mode will have larger peak-values than those for a pure active one.

From a mathematical point of view, the generation of the NP-current i_0 might be compared with the calculation of a zero sequence system. Hereby, the product terms $i_{ph} \cdot (1 - s_{ph}^2)$ ($=i_{0ph}$) correspond to the 3 individual phase quantities, the sum of which yields its zero sequence components. As it is well known for symmetrical 3-phase systems, only harmonics with orders being multiples of 3 will be achieved.

This is finally also confirmed by the amplitude spectra in figure 5.3, lower graphics. Herein, it can be seen that the 3rd harmonic will be the most dominant component for both operation modes. The higher ordered harmonics (9th, 15th...) will not have a significant influence on the oscillation in the DC-side voltages u_{D1} and u_{D2} , since they additionally will be better damped by the DC-side capacitors c than the 3rd harmonic of i_0 . However, this might be subject to change, if the switching frequency $f_{s_{ph}}$ of the pulse patterns s_{ph} is increased, which will be discussed more in depth in chapter 5.6.

Further, it is evident in the lower graphics of figure 5.3 that the 3rd harmonic for pure active operation mode (0.36 [p.u.]) is remarkably smaller than those for pure capacitive operation mode (1.20 [p.u.]). A mixed operation mode (both dominant reactive and active current phasor components) will yield 3rd harmonic amplitude values between those for the pure reactive and active operation mode.

At this point, it should be emphasized, that this harmonic oscillation with a fundamental frequency of a 3rd harmonic will not show up in single phase AC-system applications (e.g. railway interties etc.). This can be explained by the fact that in single phase applications the AC-side currents and switching functions will not be phase-displaced by $2/3\pi$ to each other in the individual phases. The DC-side oscillations appearing hereby have to be investigated separately, but a similar model as introduced here in this chapter might as well be of great help.

It should also be pointed out, that the combination of two or more 3-level VSI units with appropriate staggered switching on the AC-side and common DC-side capacitors is not well suited to remarkably reduce this 3rd harmonic oscillation. Appropriate staggered switching means, that particular AC-side harmonics will be minimized, or better, eliminated. Unfortunately, suitable phase displacements of the individual 3-level VSI units do not coincide with those necessary for minimizing or eliminating the harmonic oscillations in the DC-side voltages.

Up to now, for simplicity reasons, FFM modulation was assumed in order to derive fundamental statements concerning the generation and the harmonics of the NP-current i_0 . In the next chapter, these statements will be verified for representative off-line optimized and carrier based PWM pulse patterns.

5.4.4 Extension to off-line optimized and carrier based PWM

Off-line optimized or carrier based PWM belong to the class of modulation schemes, which are very suitable for most 3-level VSI applications. Hence, it will be of interest to study the generation and the harmonics of the NP-current $i_{0,1}$ if one of these two modulation schemes is chosen.

A fundamental distinction between off-line and the conventional carrier based PWM concerns the location of the NP-angles within the switching functions s_{ph} . Off-line optimized PWM pulse patterns (incl. FFM) have the inherent attribute to locate all NP-angles in the vicinity of the zero-crossing of their fundamental component. No NP-angles can be observed in the close vicinity of the peak-value of the fundamental component, even not for (reasonable) high switching frequencies, which can be verified in figure 3.4 - figure 3.7 of chapter 3.7.

Carrier based PWM pulse patterns in its turn normally distribute their NP angles over the whole period. While smaller NP angles can be observed in the vicinity of their fundamental's amplitude, larger ones appear in the vicinity of their fundamental's zero crossing.

From the above mentioned points of view, it might make sense to distinguish between these two different types of modulation schemes, when investigating their influence on the generation and the harmonics of the NP-current i_0 .

This will be performed in this chapter for an off-line optimized and a carrier based PWM pulse pattern, both having a representative switching frequency $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) and quite a large modulation index of m = 1.15. Hereby, the same simple graphical model as introduced in the previous chapter will be applied.

a) Off-line optimized PWM

The results for the off-line optimized pulse pattern are presented in figure 5.4. Compared to FFM modulation, it is evident for the switching function s_a in the upper graphics, that the number of the NP-angles has increased due to the higher switching frequency $f_{s_{ph}}$. In addition, the NP-angles are distributed over a slightly larger interval of the period.

However, the largest NP-angles are still in the close vicinity of the pulse pattern's fundamental zero crossing as it also is true for FFM modulation. Further, no NP-angles are present nearby the peak-value of the pulse pattern's fundamental. The latter mentioned two attributes can generally be observed for this kind of off-line optimized PWM, which focuses on the elimination of particular harmonics and simultaneously asks for a large modulation index m.

Hence, at least the envelopes of the individual contributions i_{0a} for both operation modes will be similar to those achieved with FFM modulation. With regard to the arising oscillations in u_{D1} and u_{D2} , it can be expected that here again the pure capacitive operation mode will exhibit quite large values, while the opposite proves right for a predominant active operation mode.

Concerning the harmonics of i_{0a} , the same orders will be present as derived in the previous chapter, since off-line optimized PWM fulfils the attributes of a symmetrical 3-phase system. With respect to the harmonic amplitudes however, it might turn out that particular higher ordered harmonics show up larger amplitudes than those for FFM modulation, which is caused by the higher switching frequency $f_{s_{at}}$.

It was shown for FFM modulation, that the resulting NP-current i_0 will exclusively be described by harmonics being odd numbered multiples of 3, if both the AC-side currents i_{ph} and the switching functions s_{ph} constitute symmetrical 3-phase systems. This is also evident for off-line optimized PWM from the middler and lower graphics of figure 5.4, describing the variations in time and the spectra of i_0 for the two operation modes.



Regarding the harmonics, which mainly will determine the voltage oscillations in u_{D1} and u_{D2} , again the 3rd harmonic contributes with the lion's share. Despite the increased switching frequency $f_{s_{Ph}}$, still quite large amplitudes for this 3rd harmonic can be observed. Further, it can be seen in both the middler and lower graphics, that the pure active operation mode contributes with remarkably smaller 3rd harmonic amplitudes (0.33 [p.u.]) than the pure reactive one (0.86 [p.u.]). This is as well in good agreement with the statements made for FFM modulation.

The higher ordered harmonics of i_0 with significant amplitudes (the 21st, 27th,...), have been shifted to higher orders in comparison to FFM modulation. Even if their amplitudes can compete with those of the 3rd harmonic, they hardly will be seen in u_{D1} and u_{D2} , since they are very well damped by the DC-side capacitors. This result indicates that the switching frequency $f_{s_{ph}}$ of the pulse patterns s_{ph} might have an influence on the higher ordered harmonics of i_0 , which will be investigated more detailed in chapter 5.6.

Finally it should be emphasized that the statements made in this chapter for off-line optimized PWM can also be applied to the sophisticated carrier based PWM introduced in chapter 3.5.

b) Carrier based PWM

To complete the picture, the generation of the NP-current i_0 for a conventional carrier based PWM will also be investigated. This will be performed for a representative pulse pattern with a switching frequency of $f_{s_{ph}}$ =350Hz ($f_{s_{nh}}$ =7[p.u.]).

Hereby, the same triangular shaped carriers are chosen as for the sophisticated scheme introduced in chapter 3.5.2. The control signals however will now be generated by the superposition of a 3rd harmonic to a pure overmodulated sinus (amplitude >1). The generation of these kind of carrier based PWM is illustrated figure 5.5. Also with this method, modulation indices of about m=1.15 can be achieved.

The impact of these scheme on the generation of the NP-current i_0 is presented in figure 5.6 for the above mentioned switching frequency $f_{s_{ab}}=350$ Hz and a high modulation index m=1.15.

Starting with the upper graphics in figure 5.6, it is evident that for carrier based PWM the NP-angles are distributed over the whole period of the modulation signals. Though the largest NP-angles are still located in the close vicinity of the pulse pattern's fundamental zero crossing, all the same very



fig 5.5: generation of a conventional 3-level VSI carrier based switching function s_a , carrier frequency $f_c=150$ Hz $(f_c=3[p.u.])$, injection of a 3rd harmonic

small NP-angles show up nearby the peak-value of the pulse pattern's fundamental. The latter is an inherent attribute of carrier based pulse patterns, which could not be observed for the kind of off-line optimized PWM presented in the previous sub-chapter.

However, since these NP-angles close to the peak-value of the switching function's fundamental are very small, they will not to a large extent contribute to the current time area of i_{0a} , which is proportional to the DC-side voltage oscillation. Therefore, similar results can be expected as for off-line optimized PWM and FFM modulation, which is confirmed in the middler and lower graphics of figure 5.6.

Again it is obvious, that the fundamental component of i_0 , the 3rd harmonic, will be the predominant component in the DC-side voltages u_{D1} and u_{D2} . It is further evident, that the 3rd harmonic will be less pronounced for a pure active operation mode (0.26 [p.u.]) than for a pure reactive one (0.72 [p.u.]). This is not astonishing, since the location of the largest NP-angles is in the close vicinity of the pulse pattern's fundamental zero crossing, as it also proved right for off-line optimized PWM and FFM modulation.

With respect to the higher ordered harmonics of i_0 (9th, 15th,...), similar re-



sults are achieved as for off-line optimized PWM. It can be seen in the lower graphics of figure 5.6 that e.g. the 15th and the 21st harmonic of i_0 have equivalent large amplitudes than the 3rd harmonic. However, they will experience quite a good damping by the capacitors on the DC-side and will therefore, compared to the 3rd harmonic, not have a remarkable influence on the oscillations in u_{D1} and u_{D2} .

According to the spectra in the upper graphics of figure 5.6, the 15th harmonic in i_0 has the largest amplitude. It should be recalled in mind that the off-line optimized PWM pulse pattern with the same switching frequency $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.], lower graphics of figure 5.4) showed up the first dominant harmonics at higher orders, namely the 21st and 27th.

Hence, compared to off-line optimized PWM, it might be expected that carrier based PWM will show up significant higher ordered harmonics in i_0 at lower frequencies. This assumption will be confirmed in chapter 5.6 and also proved right for the harmonics of the AC-side currents i_{ph} in chapter 3.7.1.

Up to now, for all investigated modulation schemes, the modulation indices m were assumed to be quite large. This corresponds to relatively small NP-angles, which simultaneously will mainly be located in the vicinity of the switching function fundamental's zero crossing. Hereby, this specific location of the NP-angles determined the dependancy of the 3rd harmonic amplitude on the operation mode of the 3-level VSI.

Hence it will be of high interest, to investigate the influence of smaller modulation indices, i.e. larger NP angles, on the statements made so far. The studies to come will deal with this topic.

5.5 Influence of the modulation index

As mentioned yet in the previous chapter, one point of interest concerns the dependancy of the NP-current harmonics on the modulation index m of the switching functions s_{ph} . Though normally a large modulation index m is highly desirable, some operation conditions might also ask for smaller values.

Concerning the 3-level VSI, smaller modulation indices of the switching functions s_{ph} usually will be achieved by increasing the portion of the NP angles with regard to the portions where $s_{ph} = \pm 1$.

The influence of this measure will be investigated first for the FFM pulse pattern with the help of the simple graphical model. Then the studies will be extended to off-line optimized and carrier based modulation signals.

5.5.1 FFM modulation

Speaking of FFM, only the length of the unique NP angle β can be varied to decrease or increase the modulation index m. The influence of this measure on the NP-current i_0 will be investigated in the following.

In the upper and middler graphics of figure 5.3 it is obvious that for any time instant at most one 3-level VSI phase will be connected to the neutral point NP. Due to this, during the time intervals $s_{ph}=0$, the resulting NP-current i_0 equals the individual contributions i_{0ph} . Hence, no interference of the individual phase contributions i_{0ph} can be observed. However, according to the definition of β in figure 2.4 (chapter 2.3), this will only prove right for values $\beta \le \pi/6$, which corresponds to a total NP angle in between one period of $4\beta \le 2/3\pi$.

For values $\beta > \pi/6$ ($4\beta > 2/3\pi$), the NP angles of the individual switching functions s_{ph} will overlap and therefore at least two ($\pi/6 \le \beta \le \pi/3$) or even all 3 phases ($\beta > \pi/3$) will simultaneously load the NP current i_0 during certain time intervals of a period.

Then, the individual phase current contributions i_{0ph} might either compensate or amplify each other to some extend, or, if all 3 phases are connected with the NP, even result to 0 ($i_0 = i_a + i_b + i_c = 0$). These relationships are shown in figure 5.7 for $\beta = \pi/4$ (m=0.9, $\pi/6 \le \beta \le \pi/3$) and in figure 5.8 for $\beta = 5\pi/12$ (m=0.33, $\beta > \pi/3$).

The impact of these overlapping NP-angles on the NP-current i_0 will be investigated first for its fundamental component, the 3rd harmonic.

a) 3rd harmonic of the NP-current

It can be seen in the upper graphics of figure 5.7, that with an increasing NP angle β , also the current-time area of the individual contribution i_{0a} will increase for both operation modes. This might give rise to the assumption, that larger oscillations in u_{D1} and u_{D2} have to be expected. However, with respect to all 3 phases a,b,c it is obvious, that for pure capacitive operation mode (left column, middler graphic) the overlapping NP current contributions i_{0ph} compensate each other to some extend. Due to these opposing effects, the resulting amplitude of the dominant 3rd harmonic has a smaller







value (0.95 [p.u.]) than those in figure 5.3 for a large modulation index m=1.15 (1.20 [p.u.]).

Unfortunately, for pure active operation mode, in addition to larger currenttime areas of i_{0ph} , its overlapping contributions for all 3 phases even amplify each other to some extend. This yields a 3rd harmonic to arise in i_0 with an amplitude, which is about 3 times higher (0.95 [p.u.]) than those in figure 5.3 for m=1.15 (0.36 [p.u.]). More, with respect to this 3rd harmonic amplitude, no difference can be observed any more between pure capacitive and pure active operation mode.

Increasing the NP angle β to values $\beta > \pi/3$, as shown in figure 5.8 for $\beta = 5\pi/12$ (m=0.33), yields smaller resulting amplitudes for the 3rd harmonic especially for pure capacitive (0.06 [p.u.]) but also for pure active operation mode (0.87 [p.u.]). As mentioned before, this can be explained by the fact, that now during certain time intervals, all 3 phases simultaneously contribute to the NP current, which yields $i_0=0$. However, it has to be emphasized that now, in contrary to a large modulation index m, the pure capacitive operation mode no longer exhibits the largest amplitudes for the 3rd harmonic, but the pure active one.

To complete the picture, the amplitudes of the 3rd, 9th and 15th harmonic were determined in dependancy on the whole range of the modulation index m, which corresponds to the NP angle β according to

$$m = \frac{4}{\pi} \cdot \cos\beta.$$

Hereby *m* is varied between its minimum and maximum values $0 \le m \le 1.27$ ($\pi/2 \ge \beta \ge 0$). This was performed both for pure capacitive and pure active operation mode and is presented in figure 5.9.

Though the results in figure 5.9 shall not be discussed in depth, they all the same show, that for all operation modes quite a large 3rd harmonic may appear in the NP current, which strongly depends on the chosen modulation index m.

For NP-angles $0 < \beta < \pi/6$ (1.27<m < 1.1), the 3rd harmonic of i_0 increases with increasing NP-angles β (decreasing modulation index m) for both operation modes and will be most pronounced for the pure capacitive operation mode.

In the range $\pi/6 \le \beta \le \pi/3$ (0.64<*m*<1.1) a decrease of the 3rd harmonic amplitude with increasing NP-angle β (decreasing modulation index *m*)



fig 5.9: Dependancy of the 3rd, 9th, 15th and 21st harmonic amplitude of i_0 on the modulation index *m* for FFM modulation

can be observed for pure capacitive operation mode, while the opposite is true for pure active operation mode. Up to $\beta = \pi/4$ (m=0.9), the pure capacitive operation mode contributes with larger 3rd harmonic amplitudes than the pure active one, which for $\beta > \pi/4$ (m < 0.9) however turns into the opposite.

Finally, if $\pi/3 \le \beta \le \pi/2$ (0<m<0.64) is fulfilled, the 3rd harmonic amplitude will decrease with increasing NP-angle β (decreasing modulation index m) for both operation modes. Hereby, the pure active operation mode exhibits larger 3rd harmonic amplitudes than the pure capacitive one.

In addition, it can clearly be seen in figure 5.9 that preferably a modulation index m close to its maximum value of m=1.27 should be chosen, which guarantees smallest 3rd harmonic amplitudes for both operation modes.

b) Higher ordered harmonics of the NP-current

Concerning the higher ordered harmonics, the 9th, 15th and the 21st, it is evident in both graphics of figure 5.9 that they only might have an influence for small modulation indices. This is true since they have smaller amplitudes than the 3rd harmonic over a reasonable large range of m and will further be better damped by the capacitors c on the DC-side.

It is interesting, that their dependancy on the modulation index m is very similar to the dependancy of the AC-side current harmonics on the firing angle of a thyristor controlled reactor ([54]).

Finally, also a simulation with a mixed operation mode (both reactive and active power delivery/consumption) was performed for the 3rd, 9th, 15th and 21st NP-current harmonic in dependancy on the modulation index m. For a given modulation index m, this simulation yielded quantitative values for the 3rd and the higher ordered harmonics, which are between those values presented for the pure reactive and pure active operation mode in figure 5.9. This furthermore confirmed, that the pure active and the pure reactive operation mode are quite well suited to represent the whole possible operating range of the 3-level VSI.

It should be emphasized at this point, that for comparison reasons the simulations presented so far assumed the AC-side currents i_{ph} to have an amplitude of 1 [p.u.] for all modulation indices m. In many cases of real applications however, a small modulation index m may correspond to also small amplitudes in i_{ph} . Since the magnitude of the NP current i_0 is proportional to the amplitude of the AC-side phase currents i_{ph} , which can clearly be seen in figure 5.3, smaller values for the harmonics in i_0 can be expected for smaller amplitudes of i_{ph} . Especially for $i_{ph}=0$ the contribution to i_0 will be 0.

The statements made so far are valid for FFM modulation. The influence of a smaller modulation index m on the NP-current for off-line optimized and carrier based PWM pulse patterns will be investigated in the chapters to come.

5.5.2 Off-line optimized PWM

Up to now, off-line optimized PWM pulse patterns were assumed to have a large modulation index m. In addition, as many as possible harmonics are eliminated. The impact of a smaller modulation index m on the NP-current i_0 for this type of PWM switching functions will be the topic to be studied in this chapter.

The off-line optimized pulse pattern chosen has the same switching frequency of $f_{s_{ph}}$ as in chapter 5.4.4, namely $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]), however now the modulation index *m* is determined to be m = 0.9 and m = 0.3 in-

stead of m=1.15. The simulation results are presented in figure 5.10 and figure 5.11 respectively.

Having a closer look at the upper graphics of figure 5.10 and figure 5.11, it is evident that the NP-angles in the vicinity of the pulse pattern's fundamental zero crossing will increase with decreasing modulation index m. Simultaneously, the individual switching function pulses are shifted towards the peak-value of the pulse patterns fundamental, where really no pulses could be observed for large modulation indices. This is an inherent attribute for this kind of optimized pulse patterns, where specific harmonics are subject to be eliminated, and also proves right for other switching frequencies than $f_{s_{ab}}=350$ Hz ($f_{s_{ab}}=7$ [p.u.]).

As could be observed for FFM modulation with smaller modulation indices, the NP angles of the switching functions s_{ph} in figure 5.10 and figure 5.11 do not only have increased but also are distributed over an interval larger than $2/3\pi$. It then turns out, that at least two or even 3 phases might simultaneously be connected to the neutral point NP, which yields the resulting NP-currents i_0 in the middler graphics of figure 5.10 and figure 5.11.

a) 3rd harmonic of the NP-current

Concerning figure 5.10 (m=0.9), quite an impressive 3rd harmonic with approximately the same amplitude for both operation modes can clearly be seen in the NP-currents i_0 and is furthermore confirmed in the corresponding spectra (upper graphics of figure 5.10). Compared with the results for a large modulation index m=1.15 in figure 5.4 of chapter 5.4.4 a), it can be seen that the 3rd harmonic has decreased for pure capacitive operation mode (from 0.86 [p.u.] to 0.78 [p.u.]), while the opposite must be observed for the pure active operation mode (from 0.33 [p.u.] to 0.76 [p.u.]).

For a small modulation index m=0.3, the amplitude of the 3rd harmonic in i_0 will even be larger for the pure active (0.40 [p.u.]) than for the pure capacitive operation mode (0.26 [p.u.]), which is indicated in the middler and confirmed in the lower graphics of figure 5.11.

These results are furthermore confirmed in figure 5.12, which shows the 3rd, 9th and 15th harmonic amplitude of i_0 in dependancy on the modulation index m, covering the whole range between m=0 and m=1.15.

Finally it should be noted, that with respect to the 3rd harmonic, quite a good coincidence with FFM modulation (figure 5.9) can be observed in the modulation index range 0 < m < 1.15. This proves right both qualitatively and







fig 5.12: 3rd, 9th, 15th and 21st harmonic amplitude of i_0 in dependancy on the modulation index *m* for off-line optimized PWM, pure capacitive and pure active operation mode, $f_{s_{ab}}=350$ Hz ($f_{s_{ab}}=7$ [p.u.])

also more or less quantitatively, which indicates that an increased switching frequency $f_{s_{ph}}$ seems not to have a significant impact on the amplitude of the 3rd harmonic.

b) Influence of a 3rd harmonic zero sequence system in the switching functions

Regarding off-line optimized PWM pulse patterns with elimination of the zero sequence components (especially the 3rd), it could be observed that the operation mode dependancy of the 3rd harmonic amplitude of i_0 will be subject to change.

This has been verified in a simulation with an off-line optimized pulse pattern with the same switching frequency than presented above in figure 5.12 $(f_{s_{ph}}=350\text{Hz} \ (f_{s_{ph}}=7[\text{p.u.}])$ however with elimination of the 3rd, 5th, 9th, 11th, 13th and 15th harmonic. Hereby, the amplitude of i_{03} almost linearly increased with increasing modulation index *m* for both the pure reactive and the pure active operation mode (see also figure 5.15 in chapter 5.5.3). The maximum values for the amplitudes of i_{03} have been found to be around 0.8 [p.u.] for the pure reactive operation mode and about 0.6 [p.u.] for the pure active operation mode.

However, since it usually does not make sense to eliminate zero sequence system harmonics in the switching functions, this phenomenon will not further be investigated here.

c) Higher ordered harmonics of the NP-current

Concerning the higher ordered harmonics of i_0 , it can be seen from figure 5.10 - figure 5.12 that also for middler and small modulation indices their amplitudes usually are smaller or at most of the same size than those of the 3rd harmonic. Due to the additional damping by the DC-side capacitors, they will not contribute with significant DC-side voltage oscillations, which almost exclusively will be determined by the 3rd harmonic of i_0 .

Compared to FFM modulation, the increased switching frequency $f_{s_{ph}}$ for off-line optimized PWM obviously also yields an increased order for the first significant higher ordered harmonic of i_0 , as can clearly be seen by opposing figure 5.9 to figure 5.12. While for FFM modulation the 9th harmonic of i_0 shows up largest amplitudes, the same is true for the 21st, if off-line optimized PWM with a switching frequency $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) will be applied. More in depth studies concerning the influence of the switching frequency $f_{s_{ph}}$ will be presented in chapter 5.6.

Finally a simulation with a mixed operation mode (both predominant reactive and active power delivery/consumption) has been carried out. The achieved quantitative results, which, for a given modulation index m, were between those values presented in figure 5.12, once more confirmed that the pure reactive and pure active operation mode are quite well suited to represent the whole operating range of the 3-level VSI.

5.5.3 Carrier based PWM

Since carrier based PWM is going to become an interesting modulation scheme for transmission applications, the influence of the hereby varying modulation index m on the arising harmonics in i_0 will be discussed in the following.

The carrier based pulse patterns chosen have the same switching frequency as in chapter 5.4.4, namely $f_{s_{ph}} = 350$ Hz $(f_{s_{ph}} = 7[p.u.])$, however now the modulation index *m* is determined to be m=0.9 and m=0.3 instead of

m=1.15. The simulation results are presented in figure 5.13 and figure 5.14 respectively.

Comparing the upper graphics of figure 5.13 and figure 5.14, it is evident that the NP-angles of s_{ph} increase with decreasing modulation index m, as this also proved right for off-line optimized PWM.

As a result, also a continuous increase of those intervals, where two or even all 3 phases a,b,c are connected to the neutral point NP, can be observed. This becomes most evident for the small modulation index m=0.3 (figure 5.14). Though the contributions of the individual phases a,b,c are quite impressive (upper graphics in figure 5.14), they compensate each other to a large extend in the resulting NP current i_0 (middler and lower graphics in figure 5.14).

However, in opposite to off-line optimized PWM, no displacement of the NP-angles for decreasing modulation indices can be observed. The centres of the individual NP-angles remain at almost the same location and exclusively their width will be subject to change. Further, compared to off-line optimized PWM, one can clearly see in the upper graphics of figure 5.13 and figure 5.14, that the NP angles are more or less continuously distributed over the whole period of s_{ph} and not mainly concentrated in the vicinity of the fundamentals zero crossing. For sure, these inherent attributes for carrier based pulse patterns are also fulfilled for other switching frequencies than $f_{s_{ab}}=350$ Hz ($f_{s_{ab}}=7$ [p.u.]).

Therefore, one might expect that the influence of a smaller modulation index m on the harmonics of i_0 is slightly different for carrier based than for off-line optimized PWM.

a) 3rd harmonic of the NP-current

With respect to the 3rd harmonic of i_0 , it can clearly be seen in figure 5.13 and figure 5.14, that for both modulation indices m=0.9 and m=0.3, the pure capacitive operation mode contributes with larger amplitudes (0.57[p.u.] for m=0.9 and 0.19[p.u.] for m=0.3) than the pure active operation mode (0.2[p.u.] for m=0.9 and 0.07[p.u.] for m=0.3). This also proved right for a modulation index m=1.15 (figure 5.6 in chapter 5.4.4b)) and might therefore be expected to be fulfilled over the whole range of the modulation index m. Further, with decreasing m, also the 3rd harmonic amplitude seems to decrease, which is evident in figure 5.13 and figure 5.14 both for the pure capacitive and the pure active operation mode.





Indeed, these presumptions are confirmed in figure 5.15, showing the dependancy of the 3rd, 9th, 15th and 21st harmonic amplitude of i_0 on the whole modulation index range $0 \le m \le 1.15$ for the pure capacitive and the pure active operation mode.



fig 5.15: 3rd, 9th, 15th and 21st harmonic amplitude of i_0 in dependancy on the modulation index *m* for carrier based PWM, pure capacitive and pure active operation mode, $f_{s_{ph}}=350$ Hz $(f_{s_{ph}}=7[p.u.])$

In addition, it is evident in figure 5.15, that the influence of the modulation index m on the 3rd harmonic amplitude of i_0 can be described by a simple linear function. This is true for both investigated operation modes. Also here, a simulation with a mixed operation mode (both reactive and active power delivery/consumption) has been performed, which shows the same linear behaviour of the 3rd harmonic amplitude with quantitative values between those presented in figure 5.15.

Comparing figure 5.15 with figure 5.9 and figure 5.12 (FFM, off-line optimized PWM), the most remarkable distinction consists in the linear dependancy of the 3rd harmonic amplitude on the modulation index m for both operation modes. Another dissimilarity consists in the fact that, regardless of the modulation index m, the pure active operation mode always contributes with smaller 3rd harmonic amplitudes than the pure reactive one. This in its turn is obviously caused by the different locations of the NP-angles for these two modulation schemes.

Finally, it should be pointed out that additional simulations qualitatively confirmed the above mentioned statements also for other switching frequencies than $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) and other control signals (without injection of a 3rd harmonic) and carrier signals (e.g. sawtooth).

b) Influence of a 3rd harmonic zero sequence system in the switching functions

Regarding carrier based PWM without injection of a 3rd harmonic, it could be observed, that the operation mode dependancy of the 3rd harmonic amplitude of i_0 is much less pronounced compared to the results presented in figure 5.15 (see also chapter 5.5.2b)).

This could clearly be shown in a simulation with the same carrier based PWM modulation scheme than those presented in figure 5.15 ($f_{s_{ph}}$ =350Hz ($f_{s_{ph}}$ =7[p.u.]), however without injection of a 3rd harmonic.

While the quantitative values for the amplitudes of i_{03} in the pure capacitive operation mode increased by about 20%, those in the pure active operation mode even were doubled in comparison to figure 5.15.

c) Higher ordered harmonics of the NP-current

Concerning the higher ordered harmonics of i_0 (lower graphics of figure 5.13 and figure 5.14), the 15th harmonic shows up quite impressive amplitudes, which are 3-5 times larger than those of the 3rd harmonic. More, focusing on figure 5.15, it is evident that for a middler modulation index (m=0.6) and pure active operation mode, the 15th harmonic amplitude might reach values up to seven times larger than the 3rd harmonic.

Though the 15th harmonic will by a factor of 5 be better damped than the 3rd harmonic, it might all the same exhibit equivalent or even larger amplitudes in the DC-side voltages u_{D1} and u_{D2} than the 3rd harmonic.

The 27th harmonic of i_0 on the other side (lower graphics of figure 5.13 and figure 5.14), which also contributes with pretty large values, experiences a damping about twice as much as the 15th, and might therefore not be subject to cause significant oscillations in the two DC-side voltages u_{D1} and u_{D2} .

Opposed to off-line optimized PWM with the same switching frequency

 $f_{s_{ph}}$ =350Hz ($f_{s_{ph}}$ =7[p.u.], figure 5.10 and figure 5.11 in chapter 5.5.2), the orders of the dominant harmonics of i_0 are lower for carrier based PWM (15th instead of 21st). This was also confirmed for a large modulation index (m=1.15) in chapter 5.4.4.

The investigations up to now mainly focused on the dependancy of the NPcurrent harmonics on either the operation mode of the 3-level VSI or the modulation index m of the switching functions s_{ph} . However, it could clearly be seen, that the switching frequency $f_{s_{ph}}$ of the pulse patterns s_{ph} also seems to be a parameter which has an influence on the NP-current harmonics. Therefore, the next chapter will concentrate more in depth on this topic.

5.6 Influence of the switching frequency

Usually, the switching frequency $f_{s_{ph}}$ of the modulation signals s_{ph} will have a remarkable influence on the harmonics of the AC-side currents i_{ph} or the AC-system voltages u_{Lph} , as was clearly shown in chapter 3. Hereby, a higher switching frequency $f_{s_{ph}}$ will result in the elimination or at least reduction of additional harmonics in i_{ph} and u_{Lph} .

This might also be expected for the harmonics in the NP-current i_0 , however cannot be proved right or wrong on first sight. Hence, more detailed studies will be desirable in order to find accurate answers, which will be the topic of this chapter.

5.6.1 Basic considerations

The graphical model introduced in chapter 5.4 was of great help for basic investigations, however more or less fails for studies with regard to the dependancy of the NP-current harmonics on the switching frequency $f_{s_{ph}}$. Hence another approach, which especially for that purpose is more suitable, will be presented in the following.

This more mathematical approach is based on the NP-current equation and the harmonic transfer rule from the AC- to the DC-side. According to eqn. (2.30) in chapter 2.4.3, the NP-current i_0 is given by

$$i_0 = -(i_a \cdot s_a^2 + i_b \cdot s_b^2 + i_c \cdot s_c^2) = -\sum_{ph = a,b,c} i_{ph} \cdot s_{ph}^2$$
(5.7)

It should be noted at this point, that for the investigation to come, the repre-

sentation of the NP-current equation by means of the absolute value $|s_{ph}|$ (eqn. (2.31)) will not be chosen.

According to chapter 2.5, no general analytical approximation for $|s_{ph}|$ could be achieved, if the switching functions s_{ph} will be approximated by their fundamental component s_{ph1} and their 3rd harmonic s_{ph3} . It is advisable also to take into account the 3rd harmonic s_{ph3} , since this harmonic usually will not be eliminated in off-line optimized pulse patterns and also appears in carrier based modulation schemes with superposition of a 3rd harmonic to the control signals. This can be verified in figure 3.4 - figure 3.7 of chapter 3.7.

It could be seen in simulations, that an approximation of s_{ph} by exclusively its fundamental component s_{ph1} will yield quite large deviations for the 3rd NP-current harmonic amplitudes i_{03} from the exact value. This statement proves right for switching functions s_{ph} with a 3rd harmonic s_{ph3} , independently on the NP-current representation by means of s_{ph}^2 or $|s_{ph}|$.

However, if the switching functions s_{ph} will not show up a 3rd harmonic s_{ph3} , the simplified approximation by exclusively its fundamental component s_{ph1} can be used to calculate the NP-current. It should be pointed out at this point, that then the NP-current representation by means of $|s_{ph}|$ will yield more accurate results than those by means of s_{ph}^2 .

Coming back to eqn. (5.7), individual harmonics of i_0 are basically determined by the convolution of particular harmonics of i_{ph} with particular harmonics of s_{ph}^2 .

With respect to the AC-side currents i_{ph} , only the fundamental component will be of major interest, since it can be expected that the higher ordered harmonics contribute with negligible values compared to the fundamental component.

The switching functions s_{ph} in its turn usually show up both a dominant fundamental component and in addition higher ordered harmonics. The amplitude of the fundamental component can be adjusted to a constant value for any switching frequency $f_{s_{ph}}$, while the amplitudes of the higher ordered harmonics depend on the modulation scheme and the switching frequencies. This was clearly shown in chapter 3 for off-line optimized and carrier based PWM. Further, for simplicity reasons presuming middler and large modulation indices (m > 0.9), the fundamental component of the switching functions s_{ph} will contribute with the lion's share compared to the higher ordered switching function harmonics.

Based on the above mentioned considerations, the dependancy of the 3rd and higher ordered NP-current harmonics on the switching frequency $f_{s_{pk}}$ will be studied in the following. As in the previous chapters, it will hereby be distinguished between investigations with regard to exclusively the 3rd NP-current harmonic and those concentrating on the higher ordered NP-current harmonics.

5.6.2 Influence on the 3rd NP-current harmonic

a) Qualitative discussions

According to the considerations in the previous chapter, the 3rd harmonic of i_0 will mainly be the result of the convolution of the AC-side current fundamental component with the 2nd and the 4th harmonic of the squared switching functions s_{ph}^2 . This can also be verified by the harmonic transfer rule from the AC- to the DC-side (table 4.5 in chapter 4.3.2) and the individual decompositions of i_{ph} and s_{ph}^2 in symmetrical components (table 4.2 and table 4.3 in chapter 4.3.1).

Presuming a middler or a large modulation index (m>0.9), the 2nd and 4th harmonic of s_{ph}^2 in its turn are quite good approximated by the convolutions of the switching function fundamental component with itself and with its 3rd harmonic.

As mentioned yet, it is advisable also to take into account the 3rd harmonic since it normally is not eliminated in off-line optimized pulse patterns and also appears in carrier based modulation schemes with superposition of a 3rd harmonic to the control signals.

In addition, the convolution of a significant 5th harmonic in s_{ph} with the fundamental component of s_{ph} might contribute to the 4th harmonic in s_{ph}^2 and with that to the 3rd harmonic of i_0 . However, since for higher switching frequencies the 5th harmonic of s_{ph} is either eliminated or strongly reduced, their influence will only have to be taken into account for very low switching frequencies.

Finally, convolutions of exclusively higher ordered switching function harmonics (e.g. 7th, 9th, 11th,...), which also would result to a 2nd (e.g. 7th with 9th) or a 4th harmonic (e.g. 7th with 11th), are here for simplicity reasons neglected.
Therefore, it can be summarized that the fundamentals of the AC-side currents i_{ph} and the switching functions s_{ph} and, if present with significant values, also a 3rd switching function harmonic can be seen to predominantly determine the 3rd harmonic of the NP-current i_0 .

Hence, with the notation and the symbols introduced in chapter 4.3.1, the AC-side currents i_{ph} and the switching functions s_{ph} can sufficiently be approximated by the following equations:

$$i_{ph} = I_1 \cdot \sin(\omega_1 t + D_{ph} + \phi_u + \phi_{S_1} + \phi_{I_1})$$
(5.8)

$$s_{ph} = S_1 \sin(\omega_1 t + D_{ph} + \phi_u + \phi_{S_1}) + S_3 \sin[3(\omega_1 t + D_{ph} + \phi_u) + \phi_{S_3}] \quad (5.9)$$

The phase angles ϕ_{μ} between the AC-system voltages and the 3-level VSI output voltages and ϕ_{I_1} between the fundamental components of the AC-side currents i_{ph} and the switching functions s_{ph} strongly depend on the 3-level VSI operation mode.

The phase angle ϕ_{S_1} of the switching function fundamental is given to

$$\phi_{S_1} = \pi/2$$

both for the off-line optimized and the carrier based PWM presented in this thesis. The phase angle ϕ_{S_3} of the 3rd switching function harmonic in its turn is subject to vary with the modulation index *m* and the modulation scheme. With that eqn. (5.8) and eqn. (5.9) can be written to

$$i_{ph} \approx I_1 \cdot \cos(\omega_1 t + D_{ph} + \phi_u + \phi_{I_1})$$

$$s_{ph} \approx S_1 \cdot \cos(\omega_1 t + D_{ph} + \phi_u) + S_3 \cdot \sin[3(\omega_1 t + D_{ph} + \phi_u) + \phi_{S_3}].$$

Inserting these expressions in eqn. (5.7) $(i_0 = f(i_{ph}, s_{ph}^2))$ yields after some trigonometric conversions a rough approximation for the 3rd NP-current harmonic i_{03} , which is given by eqn. (5.10).

$$i_{03} \approx -\frac{3}{4} I_1 S_1 \{ S_1 \cos[3(\omega_1 t + \phi_u) + \phi_{I_1}] +$$

$$+4 S_3 \sin[3(\omega_1 t + \phi_u) + \phi_{S_3}] \cos \phi_{I_1} \}$$
for $S_1 = m \ge 0.9$
(5.10)

Herein, the fundamental amplitude of i_{ph} , I_1 , will exclusively be deter-

mined by the operation point of the 3-level VSI. Usually values up to 1 [p.u.] have to be expected in any nominal operation mode, which is absolutely independent on the pulse patterns' switching frequency $f_{s_{rel}}$.

Concerning the fundamental amplitude of s_{ph} , S_1 , which is known to coincide with the modulation index m, also quite large values up to about m=1.15 can be achieved even for high switching frequencies. This was shown in chapter 3 and is a must in order to ensure an optimal utilization of the 3-level VSI.

Finally as well the 3rd harmonic of s_{ph} , if present, at most slightly varies with the switching frequency $f_{s_{ph}}$ as can also be verified in figure 3.4 - figure 3.7 of chapter 3.7.

With that, it has to be expected that the switching frequency $f_{s_{ph}}$ of a pulse pattern s_{ph} will not have a significant influence on the amplitude of i_{03} , at least for large modulation indices.

Further, it should be noted at this point that eqn. (5.10) would also be appropriate to qualitatively study the dependancy of i_{03} on the operation mode of the 3-level VSI, however exclusively for large modulation indices. Concerning smaller modulation indices, the influence of the higher ordered switching function harmonics will no longer be negligible in eqn. (5.10) and an extended mathematical analysis will be of need. This in its turn might become quite complex and cannot compete with the graphical model, especially from a clearness and simplicity point of view, and was therefore discarded in this work.

In order to verify the investigations made up to now, simulations will be presented in the following sub-chapter, showing the dependancy of the 3rd NPcurrent harmonic on the switching frequency $f_{s_{nh}}$ of the pulse patterns s_{ph} .

b) Simulation results

As representative modulation schemes, off-line optimized and carrier based PWM, which have been introduced in chapter 3.4 and chapter 5.4.4b), are chosen again. The modulation indices are determined to either m=1.15 or, in order to also take into account smaller values, to m=0.3. The switching frequency range varies from $f_{s_{ph}} = 50$ Hz to $f_{s_{ph}} = 1450$ Hz in steps of 100Hz. To complete the picture, all simulations are performed for both the pure capacitive and the pure active operation mode.

The results are given in figure 5.16 for a large modulation index m=1.15 and in figure 5.17 for a small modulation index m=0.3 respectively.



fig 5.16: 3rd, 9th, 15th and 21st harmonic amplitude of i_0 in dependancy on the switching frequency $f_{s_{ph}}$ for off-line optimized and carrier based PWM, pure capacitive and pure active operation mode, large modulation index (m=1.15)



fig 5.17: 3rd, 9th, 15th and 21st harmonic amplitude of i_0 in dependancy on the switching frequency $f_{s_{ph}}$ for off-line optimized and carrier based PWM, pure capacitive and pure active operation mode, small modulation index (m=0.3)

Focusing on the amplitude of the 3rd harmonic i_{03} in the simulations of figure 5.16, it is evident that for low switching frequencies (50Hz- 250Hz), the amplitude of i_{03} might be subject to change with the switching frequency $f_{s_{ph}}$. This will moreover be caused by higher ordered harmonics of the switching functions s_{ph} (e.g. the 5th), which, as mentioned in the previous sub-chapter, might have a more or less significant influence on the 3rd NP-current harmonic for lower switching frequencies. However, for values larger than 250Hz, the impact of the switching frequency $f_{s_{ph}}$ on the 3rd harmonic amplitude is very moderate or really negligible, as is clearly shown in figure 5.16 for both operation modes and modulation schemes.

With that, it is confirmed that for off-line optimized and carrier based PWM, even high switching frequencies are not capable to reduce or eliminate the amplitude of the 3rd harmonic oscillation!

Apparently this as well proves right for small modulation indices, which was not investigated mathematically, but is undeniably manifested in figure 5.17 for both operation modes and modulation schemes.

Finally, it will now be interesting to also study the influence of the switching frequency $f_{s_{ph}}$ on the higher ordered harmonics of i_0 (9th, 15th,...), which will be performed in the next chapter.

5.6.3 Influence on the higher ordered NP-current harmonics

a) Qualitative discussions

In the previous chapter the studies were based on simplified assumptions for the AC-side currents i_{ph} and the switching functions s_{ph} in order to investigate the influence of the switching frequency $f_{s_{ph}}$ on the 3rd harmonic amplitude of i_0 .

These simplified assumptions will now be adapted with respect to investigations concerning the influence of the switching frequency $f_{s_{ph}}$ on the higher ordered harmonics of i_0 .

While the AC-side currents i_{ph} furtheron can sufficiently be approximated by eqn. (5.11),

$$i_{ph} \approx I_1 \cdot \sin(\omega_1 t + D_{ph} + \phi_u + \phi_{S_1} + \phi_{I_1})$$
(5.11)

the switching functions s_{ph} will now be written to

$$s_{ph} \approx S_1 \sin(\omega_1 t + D_{ph} + \phi_u + \phi_{S_1}) + S_k \sin[k(\omega_1 t + D_{ph} + \phi_u) + \phi_{S_k}] \quad (5.12)$$

where S_k and ϕ_{S_k} denote the amplitude and the phase angle of the k-th significant harmonic of s_{ph} . As it proved right for s_{ph} (eqn. (5.9)) in the previous chapter, it is also here presumed that the fundamental component of s_{ph} contributes with quite a large value. Only then eqn. (5.12) can be seen as an approximation of s_{ph} .

Calculating $i_{ph} \cdot s_{ph}^2$ with eqn. (5.11) and eqn. (5.12) and neglecting all terms, which would result in low ordered components (fundamental, 3rd harmonic) or which would contribute with small amplitudes (S_k^2) , yields eqn. (5.13).

$$i_{ph} \cdot s_{ph}^{2} \approx 1/2 \cdot I_{1}S_{1}S_{k} \cdot \{ \sin[(k-2)(\omega_{1}t+D_{ph}+\phi_{u})+\phi_{S_{k}}-\phi_{I_{1}}] + (5.13)$$

+2\sin[k(\omega_{1}t+D_{ph}+\phi_{u})+\phi_{S_{k}}] \cdot \cos\phi_{I_{1}} +
+\sin[(k+2)(\omega_{1}t+D_{ph}+\phi_{u})+\phi_{S_{k}}+\phi_{I_{1}}] \}

It is evident in eqn. (5.13), that the particular convolutions $i_{ph} \cdot s_{ph}^2$ consist of 3 oscillation terms, having a centre frequency equal to those of the significant switching function harmonic and a lower and a higher side-band frequency. It can further be seen, that the term with the centre frequency strongly depends on the operation mode of the 3-level VSI, which is indicated in eqn. (5.13) by the term $\cos\phi_{I_1}(\cos\phi_{I_1} \approx 0$ for pure reactive and $\cos\phi_{I_1} \approx 1$ for pure active operation mode).

However, though 3 terms are present in $i_{ph} \cdot s_{ph}^2$, only those terms which constitute a zero sequence system will finally contribute to i_0 , since all other terms will sum up to 0. Hence, depending on the numeric value of k, either one of the oscillations with a side-band frequency k+2, k-2 or the oscillation with the centre frequency k will be apparent in i_0 with its triple amplitude.

With that, it generally can be expected that the first higher ordered harmonic of i_0 with a significant amplitude (e.g. comparable to those of the 3rd harmonic), will coincide or will be in the close neighbourhood of the first remarkable harmonic of the switching functions s_{ph} .

If the first remarkable switching function harmonic with order k constitutes a zero sequence system (odd numbered multiple of 3), it will also appear with the same order in i_0 . It will then show up a remarkable amplitude for the pure active operation mode $(\cos \phi_{I_1} \approx 1)$, but will be almost negligible for the pure reactive operation mode $(\cos \phi_{I_1} \approx 0)$, which can be verified in eqn. (5.13).

If the first remarkable switching function harmonic with order k constitutes a positive or a negative sequence system, it will be reflected to either the next lower ordered (k-2) or the next higher ordered harmonic (k+2), which are an odd numbered multiple of 3.

For sure, it will therefore also happen that two or more adjacent switching function harmonics will contribute to the same NP-current harmonic, which will then either amplify or compensate each others contributions to i_0 . Whether they amplify or compensate each others contributions strongly depends on their individual phase angles (ϕ_{S_k}) and the operation mode of the 3-level VSI (ϕ_{I_k}), as can clearly be seen in eqn. (5.13).

Due to the fact that the orders k of the significant switching function harmonics will increase with increasing switching frequency $f_{s_{pk}}$, it can be concluded that in opposite to the 3rd harmonic of i_0 , the higher ordered harmonics of i_0 show a remarkable dependancy on the switching frequency $f_{s_{ph}}$. The higher the switching frequency $f_{s_{ph}}$, the higher also the frequency of the first significant higher ordered harmonic of i_0 .

The validity of the statements made in this chapter will now be verified for off-line optimized and carrier based PWM by means of representative simulation results.

b) Simulation results

The simulation results for the higher ordered harmonics of i_0 (9th, 15th, 21st) in dependancy on the switching frequency ($f_{s_{ph}}$ =50Hz.... 1450Hz) are shown in figure 5.16 for a large modulation index m=1.15.

First, it will be focused on off-line optimized PWM, which is represented in the left column of figure 5.16.

As an example, for $f_{s_{ph}} = 150$ Hz $(f_{s_{ph}} = 3$ [p.u.]) the first switching function harmonics with significant amplitudes are the 11th and 13th. According to eqn. (5.13), the 11th harmonic of s_{ph} is "reduced" to the 9th NP-current harmonic, while the 13th will be "lifted" to the 15th NP-current harmonic. This statement is in good agreement with the simulation results in the left column of figure 5.16, where for $f_{s_{ph}} = 150$ Hz $(f_{s_{ph}} = 3$ [p.u.]), the 9th and the 15th at least for the pure reactive operation mode contribute with the most significant values. Or, for $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]), the first significant higher ordered switching function harmonic will be the 17th and the 19th, which will, according to eqn. (5.13), be responsible for the generation of a 15th and a 21st harmonic in i_0 . Again, figure 5.16 proves the validity of this consideration.

Further, it is also obvious from both simulations in the left column of figure 5.16, that with increasing switching frequencies, also the orders of the dominant NP-current harmonics will increase: while the 9th NP-current harmonic will be the most significant for $f_{s_{ph}}=50$ Hz ($f_{s_{ph}}=1$ [p.u.]), the same proves right for the 15th with $f_{s_{ph}}=150$ Hz ($f_{s_{ph}}=3$ [p.u.]) and for the 21st with $f_{s_{ph}}=250$ Hz ($f_{s_{ph}}=5$ [p.u.])

Therefore, it can be seen to be proven that for this type of off-line optimized PWM (elimination of particular harmonics), an increased switching frequency $f_{s_{ph}}$ of the pulse patterns s_{ph} will also shift the significant higher ordered harmonics of i_0 to higher frequencies.

For carrier based PWM, as described by eqn. (3.5) in chapter 3.4.3 a), the lowest orders of significant switching function harmonics are given to

$$k = 2 \cdot f_c \pm v \cdot f_1 = 2 \cdot f_{s_{-1}} \pm v \cdot f_1; \qquad v = 1;$$

Hence, for e.g. $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]), k results to k=9 and k=11, which corresponds to a significant 9th and 11th switching function harmonic. According to the statements in the previous sub-chapter, these two harmonics will be reflected to the 9th NP-current harmonic, which clearly can be verified in the right column of figure 5.16. Analog considerations for $f_{s_{ph}} = 350$ Hz ($f_{s_{ph}} = 7$ [p.u.]) or $f_{s_{ph}} = 550$ Hz ($f_{s_{ph}} = 11$ [p.u.]) claim the 15th or 21st NP-current harmonic to be the most dominant, which also is in very good agreement with the results achieved in figure 5.16.

With that it is also confirmed for carrier based PWM, that higher switching frequencies of the pulse patterns s_{ph} simultaneously yield higher orders for the first significant NP-current harmonic, except of the 3rd for sure, which unfortunately does not follow this rule.

It is interesting that for $f_{s_{ph}} = 150$ Hz $(f_{s_{ph}} = 3$ [p.u.]) and $f_{s_{ph}} = 450$ Hz $(f_{s_{ph}} = 9$ [p.u.]), none of the higher ordered NP-current harmonics (9th, 15th, 21st) contributes with exceptional large values, which proves right for both operation modes. This behaviour will not be investigated more in depth here but could generally be validated by additional simulations for this kind of carrier based PWM and switching frequencies being an odd numbered multiple of 3. Apparently, adjacent switching function harmonics compensate

each others contributions to the NP-current i_0 , independently on the operation mode. Hence, with respect to small higher ordered NP-current harmonic amplitudes, it is advisable to choose the switching frequencies as an odd numbered multiple of 3. However, when e.g. selecting other carrier waves, this positive attribute might be subject to change, as can be verified in [30].

With respect to both off-line optimized and carrier based PWM, it is also evident that a specific operation mode can have a remarkable influence on the amplitudes of the particular higher ordered NP-current harmonics. This could undeniably be seen in eqn. (5.13) and can also be verified by comparison of the upper and lower graphics of figure 5.16.

Further, as mentioned yet in chapter 5.4.4 and chapter 5.5.3, it is once more confirmed in figure 5.16, that for the same switching frequency $f_{s_{ph}}$, the carrier based PWM exhibits lower ordered NP-current harmonics than off-line optimized PWM.

However, all in all it can be concluded, that for large modulation indices the influence of the higher ordered harmonics of i_0 on the DC-side voltages u_{D1} and u_{D2} will not be significant compared to the impact of the 3rd NP-current harmonic.

Unfortunately, this might be subject to change for smaller modulation indices. Hence, though not investigated mathematically, also a small modulation index (m=0.3) has been taken into account, which is manifested in the simulations of figure 5.17 for both operation modes and modulation schemes.

Concerning the dependancy of the significant NP-current harmonic orders on the switching frequency $f_{s_{ph}}$, the results achieved for a large modulation index *m* are confirmed. Also here, the higher the switching frequency $f_{s_{ph}}$, the higher the orders of the significant NP-current harmonics.

However, compared with the 3rd NP-current harmonic amplitude, the higher ordered NP-current harmonics now exhibit quite large amplitudes, if the modulation indices m are small.

For off-line optimized PWM (left column of figure 5.17), the higher ordered harmonic amplitudes still do not exceed those values of the 3rd harmonic. More, they experience a better damping by the DC-side capacitors and therefore, the 3rd harmonic can furtheron be seen as the predominant oscillation in the DC-side voltages. The latter mentioned proves right for all switching frequencies and also for modulation indices even smaller than m=0.3, as could be verified by additional simulations.

This is subject to change for carrier based PWM (right column of figure 5.17), where the 9th, 15th and 21st of i_0 may take on values up to 7 times larger or more than those of the 3rd NP-current harmonic, especially in the pure active operation mode. Though they are better damped by the DC-side capacitors than the 3rd harmonic of i_0 , they all the same might show up oscillations in u_{D1} and u_{D2} with larger amplitudes than those of the 3rd harmonic. For m=0.3, this will be true with respect to switching frequencies up to 750Hz, or, as further simulations with even smaller modulation indices m showed, up to more than 1kHz. For higher switching frequencies, the first higher ordered significant harmonic will then sufficiently be damped by the DC-side capacitors and will therefore no longer remarkably contribute to the oscillations in u_{D1} and u_{D2} .

Also for small modulation indices, another way to reduce the influence of the higher ordered NP-current harmonics for this kind of carrier based PWM consists in choosing the switching frequency $f_{s_{ph}}$ as an odd numbered multiple of 3. This was proven in additional simulations and is as well obvious in the left column of figure 5.17.

5.7 Summary

In this chapter, it was first of all shown that the NP-current i_0 is the driving force for the 3-level VSI specific oscillations in the two DC-side voltages u_{D1} and u_{D2} . These undesirable oscillations have an identical shape in both DC-side voltages u_{D1} and u_{D2} , however a phase-displacement by π .

The NP-current i_0 in its turn was found to depend on the switching functions s_{ph} and the AC-side currents i_{ph} . The location of the NP-angles as well as the relative phase-displacement of the pulse patterns s_{ph} with respect to the AC-side currents i_{ph} will have a remarkable influence on i_0 . This could be seen with the help of a graphical model, which is a powerful simple tool to describe the generation, the operation mode dependancy and the harmonic orders of the NP-current i_0 .

For symmetrical operation conditions $(s_{ph} \text{ and } i_{ph} \text{ are symmetrical 3-phase systems})$, it was proved that the harmonic orders of i_0 will be odd numbered multiples of 3 with respect to the fundamental frequency f_1 on the AC-side.

In case of asymmetrical 3-phase conditions either for the pulse patterns s_{ph} or the AC-side currents i_{ph} , the fundamental frequency of the NP-current i_0 equals those on the AC-side (f_1) .

These general valid results have not only been verified for FFM modulation but also for off-line optimized and carrier based PWM.

In addition, investigations have been performed to show how the 3rd harmonic in i_0 and their multiples depend on the following parameters:

• the operation mode of the 3-level VSI

• the modulation index m of the pulse patterns s_{ph}

• the switching frequency $f_{s_{ph}}$ of the pulse patterns s_{ph} .

For FFM and off-line optimized PWM and high modulation indices (m > 0.9), the amplitude of the 3rd harmonic in i_0 has the highest amplitudes in the purely reactive operation mode and the lowest in the purely active operation mode. This is also to be expected for the carrier based PWM with the sophisticated flat-top control signal (chapter 3.5, carrier frequency f_c is higher than the switching frequency $f_{s_{ph}}$), since the shape of its pulse patterns s_{ph} is quite similar to those of off-line optimized PWM.

With decreasing modulation index however (m < 0.9, FFM and off-line optimized), this turns into the opposite (highest 3rd harmonic amplitudes in i_0 for the pure active operation mode, smallest ones for the pure reactive operation mode).

The multiples of the 3rd harmonic in i_0 have only a moderate influence.

For conventional carrier based PWM (carrier frequency f_c equals the switching frequency $f_{s_{ph}}$), the 3rd harmonic amplitude showed up highest values for a pure reactive and smallest values for a pure active operation mode. The 3rd harmonic amplitude is a linear function of the modulation index m, regardless of the operation mode.

Concerning the higher ordered harmonics of i_0 (9th, 15th,...), it turned out that for conventional carrier based PWM, quite impressive amplitudes have to be expected, especially for small modulation indices and a pure active operation mode. Hence, despite a reasonable good damping, oscillations may arise in the DC-side voltages u_{D1} and u_{D2} , which have similar or even slightly larger amplitudes than those of the 3rd harmonic.

Finally, the influence of the switching frequency $f_{s_{ph}}$ on the 3rd harmonic of i_0 and its multiples has been studied.

It can roughly be said that the switching frequency $f_{s_{ph}}$ has no major influence on the 3rd harmonic of i_0 , at least for switching frequencies larger than 250Hz.

The multiples of the 3rd NP-current harmonic however can be reduced to negligible values by increasing the switching frequency $f_{s_{nk}}$.

These statements concerning the dependancy of the NP-current harmonics on the switching frequency $f_{s_{ph}}$ are valid for both off-line optimized (incl. FFM), and conventional carrier based PWM pulse patterns (carrier frequency f_c equals to the switching frequency $f_{s_{ph}}$).

6 Quantitative harmonic analysis for a SVC application

6.1 Overview

In chapter 4 a qualitative harmonic analysis of the 3-level VSI was performed, which is valid for all 3-level VSI operation modes (reactive and active power exchange with the AC-system). In order to quantitatively verify the achieved results, the system equations derived in chapter 2.4.2 are solved with the method of the matrix exponential and the simulation tool MATLAB. This was performed for the pure reactive operation mode by means of a 3-level VSI SVC.

Hereby especially small DC-side capacitor sizes are taken into account. It will be shown that a 3-level VSI with a small DC-side capacitor $(c_{tot}=0.5[p.u.] \text{ or } \tau_{c_{tot}}=1.44 \text{ msec})$ will have some inherent drawbacks, which are not known from the 2-level VSI.

Finally, the influence of the 3-level VSI DC-side capacitor size on relevant system quantities (harmonics, Total Harmonic Distortion (THD), stress of valves and passive components) is studied and compared with the 2-level VSI. As well a reasonable capacitor size for the investigations in the following chapters is derived.

The modulation schemes chosen include Fundamental Frequency Modulation (FFM) and off-line optimized PWM with a switching frequency $f_{s_{ph}}=250$ Hz ($f_{s_{ph}}=5$ [p.u.]).

6.2 Solution methods for the system equations

Assuming infinite values $c \to \infty$ for the 3-level VSI DC-side capacitors ensures that the DC-side voltages u_{D1} and u_{D2} constitute ripplefree DC-quantities. Hence, there will be no feedback from the AC-side current harmonics to the DC-side voltages and vice versa. It is then possible to solve the system equation on the AC-side (eqn. (2.17) in chapter 2.4.2) for the currents i_{ph} with analytical methods. In many applications (e.g. drives), the DC-side capacitors have reasonable large values and it is sufficient to use these analytical methods.

However, if smaller capacitor values are required, as it is desirable in transmission applications, a not negligible interaction between the AC-side current harmonics and the DC-side voltage harmonics exists. Then, the ACside current harmonics will cause a ripple in the DC-side voltages which in its turn has an influence on the AC-side current harmonics. Therefore, the system equation (eqn. (2.17) in chapter 2.4.2) has to be solved also with respect to the DC-side equations (chapter 2.4.3). Unfortunately, this is not possible with the simple analytical methods.

Mathematically spoken, eqn. (2.17) together with the DC-side equations derived in chapter 2.4.3, is a system of linear differential equations with piecewise constant coefficients. These piece-wise constant coefficients are represented by the switching functions s_{ph} , which piece-wise take on the constant values 1, -1 or 0. A periodical solution for this kind of differential equation can not be calculated with simple analytical methods.

Many simulation tools (e.g. SABER etc.) are capable to deal with this problem by using numerical algorithms, e.g. those proposed by **Newton-Raphson** or **Katznelson**. These algorithms provide an approximated solution of the Kirchhoff laws for each time instant, the accuracy of which can be influenced by an eligible step-size and other parameters. Hereby, very small deviations from the exact values might in consecutive calculation steps sum up to values which are no longer negligible. Hence, the simulation results sometimes remarkably differ from the exact results, which can be interpreted as a numerical instability. In order to avoid this problem, a very fine resolution of the program's step-size and other accuracy parameters are required, which yields very long computing times for a sufficient output. Further, the influences of an implemented control scheme or the excitation of badly damped system resonances might falsify the steady state result of a harmonic analysis.

However, this kind of simulation tools have the advantage, that there is no need for an exact mathematical description of the investigated system. Usually, solely the individual system components have to be specified and connected to each other in form of a net-list, which actually is similar to the circuit plans of a real hardware model. These net-lists will then be compiled to an appropriate equation system, which will be solved with the above mentioned numerical methods. The system components are given by the simulator software or can also be user-defined. In general, they may include all kind of electrical or electronic components, switches and control blocks or, as just mentioned, user-defined functions.

Another approach focuses on the solution of the differential equation system by means of the matrix exponential, which also includes the construction of periodic results. Hereby, in a first step, the equations are solved at each switching instant, the latter of which are determined by the switching functions s_{ph} . The particular achieved results are then used as initial values for further calculations. During the time intervals between two consecutive switching actions, the linear differential equations have constant coefficients with values 1, -1 or 0. Hence, together with the above mentioned initial values, a periodical solution can be calculated with the help of the matrix exponential. This approach is much less computing time intensive than other approximation methods, numerically very stable, free of control system or resonance influences and always yields an exact steady-state solution. Further, it is also easy to take into account the splitted 3-level VSI output voltages u_{phsum}, u_{phdiff} and currents i_{phsum}, i_{phdiff} in order to assess their individual contributions. However, this method will only be useful, if the system to be analysed will completely mathematically be described, which sometimes might not be trivial at all, especially if in addition a control scheme should also be included.

Here in this chapter a steady-state harmonic analysis of a system, which is completely mathematically defined, will be presented. Hence, the following results are based on the mathematical solution of the differential system equations by means of the matrix exponential. The implementation was realized with MATLAB in collaboration with the Institute of Applied Mathematics of ETH. For more detailed information, the reader is referred to [55] and [56].

6.3 SVC

The example chosen is a Static Var Compensator (SVC) with a 3-level VSI, since this is the main application investigated in this thesis. Due to the fact that no active power is provided to the AC-system, there is no need for a source or a sink on the DC-side and figure 2.1 can be simplified according to figure 6.1.

6.3.1 Control scheme

The control scheme of the 3-level VSI SVC is described in depth in chapter 9. However, for a better understanding, the most important features will be summarized shortly.



fig 6.1: simplified model of a SVC with 3-level VSI

First of all, it should be pointed out that the modulation index m of the chosen pulse pattern (FFM or PWM) is assumed to be constant over the whole operation range of the SVC. This implies that the fundamental component of the 3-level VSI output voltages u_{ph} has to be controlled via the DC-side voltage. Therefore, in order to set a desired reactive current, the DC-side capacitors have to be charged or discharged. This will be achieved by a brief increase of the angle ϕ_u between the fundamentals of the AC-system voltages u_{Lph} and the 3-level VSI output voltages u_{ph} in either direction. As a result an active component in the 3-level VSI currents i_{ph} will appear and energy will be drawn or delivered to the DC-side capacitors.

More details about the control strategy are given in chapter 9, since here only investigations on harmonics and the design of the DC-side capacitor are of interest.

Both for symmetrical and asymmetrical operation conditions the SVC works in the nominal capacitive operation mode. This is assumed due to the fact, that this operating point implies the worst case concerning both the stress of the valves (highest DC-voltages $u_{D1/D2}$) and the amplitudes of the AC-side current harmonics, which is also confirmed in the phasor diagram of figure 5.2 in chapter 5.4.2.

Nominal capacitive operation mode means (neglecting the losses), that the fundamental positive sequence component of the AC-currents i_{ph} has an amplitude equal to 1 [p.u.] and is leading by $\pi/2$ with respect to the fundamental positive sequence component of u_{Lph} .

6.3.2 Modulation schemes

The modulation schemes will include FFM and off-line optimized PWM with a switching frequency $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]). The generation and the attributes of the pulse-patterns were described in chapter 3.4. The studies in this chapter are restricted to off-line optimized switching functions, since carrier based PWM modulation would not yield principally distinctive results.

FFM is chosen because this modulation scheme yields a minimum of switching losses in the valves, which is, especially in high power transmission applications, highly desirable. Further, it is the most challenging touchstone for a control scheme with respect to the dynamic behaviour. It will be anticipated here, that therefore FFM modulation was chosen for the investigations concerning the 3-level VSI control in chapter 9.

Hereby, the unique NP-angle β of the FFM switching function was optimized to $\beta = \pi/10$. With that, according to table 3.1 in chapter 3.4, the 5th harmonic is eliminated. In addition, the 7th harmonic is reduced. The modulation index results to m=1.211.

With regard to the off-line optimized pulse pattern, the 5th, 7th, 11th, 13th and 17th harmonics are eliminated by additional switching pulses. For todays available high power semiconductors, the switching frequency $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]) can be assumed to be realistic even for applications up to a few hundred megawatts. Also the modulation index m = 1.166 is still quite high.

6.3.3 System parameters

a) AC-system and transformer impedance

For the studies in this chapter, the AC-system impedance consisting of r_L and l_L will be neglected, i.e. an infinite strong AC-system will be assumed:

$$l_L = 0$$
 [p.u.] $r_L = 0$ [p.u.].

The transformer impedance is chosen to

$$l = 0.2$$
 [p.u.] $r = 0.005$ [p.u.].

b) DC-side capacitors

With regard to the DC-side capacitors c, quite a small value is assumed,

which will be desirable in transmission applications:

$$c = 1$$
 [p.u.] \Rightarrow total capacitance $= c_{tot} = \frac{c}{2} = 0.5$ [p.u.]

It should be mentioned at this point, that capacitors with a size of c=1[p.u.], installed in each phase on the AC-side, would absorb the same capacitive power from the AC-system as the 3-level VSI in the nominal capacitive operation mode. However, the per unit definition of c or c_{tot} presumes a maximum voltage stress equal to the amplitude of the AC-system voltages u_{Lph} , which unfortunately does not have to prove right for the capacitors on the 3level VSI DC-side. Hence, the per unit definition of the capacitors is suitable for its representation in normalized equations but not for the assessment of their real size including their necessary voltage rating.

Another, more appropriate definition for c or c_{tot} is by means of a time constant. This time constant is defined by the ratio between the stored capacitor energy at a nominal rated DC-side voltage and the nominal apparent power of the 3-level VSI. This time constant can also be expressed in dependancy on the per unit representation of the capacitors c and the modulation index m of a specific pulse patterns, which results in

$$\tau_c = \frac{c}{3 \cdot m^2 \cdot w_1} \text{ [sec.]} \quad \text{and} \quad \tau_{c_{tot}} = \frac{4 \cdot c_{tot}}{3 \cdot m^2 \cdot w_1} \text{ [sec.]} \quad (6.1)$$

with $w_1 = 2\pi \cdot f_1 = 2\pi \cdot 50 \text{Hz}$

A more detailed derivation of eqn. (6.1) is presented in appendix A.2.

With that and c=1[p.u.], $c_{tot}=0.5$ [p.u.] the time constants τ_c and $\tau_{c_{tot}}$ for FFM modulation (m=1.211) are calculated to

$$\tau_c = 0.72 \text{ msec}$$
 and $\tau_{c_{ini}} = 2\tau_c = 1.44 \text{ msec}$

For the off-line optimized PWM pulse pattern, slightly larger time constants τ_c and τ_{ctot} are achieved due to the smaller modulation index m=1.166:

$$\tau_c = 0.78 \text{ msec}$$
 and $\tau_{c_{iot}} = 2\tau_c = 1.56 \text{ msec}$

In order to absorb the same capacitive power from the AC-system as the 3level VSI in the nominal capacitive operation mode, 3 AC-side capacitors, each with a time constant τ_{cAC} of - 162 -

$$\tau_{cAC} = \frac{1}{3 \cdot w_1} = 1.06 \text{ msec},$$

have to be installed on the AC-side. This results in a total time constant $\tau_{c_{\text{relAC}}}$ of

$$\tau_{c_{totAC}} = 3 \cdot \tau_{cAC} = \frac{1}{w_1} = 3.18 \text{ msec}$$

The capacitor size definition based on a time constant both combines the size and the DC-side voltage stress of a specific capacitor and will therefore be an appropriate quantity to assess its real size and with that its price.

In the studies to follow, the capacitor values c or c_{tot} are given with respect to both the per unit and the time constant definition.

Finally, all parameters for the simulations of the system in figure 6.1 will be summarized in table 6.1.

6.4 Symmetrical operation conditions

Now that the basics are derived, this chapter presents the quantitative harmonic analysis results for the SVC-example. First of all symmetrical operation conditions are presumed according to the definition in chapter 4.3.

The following figures 6.2I - 6.2III and 6.3I- 6.3III show the line diagrams and the spectra of all currents and voltages introduced in chapter 2.3 for the FFM and off-line optimized PWM modulated SVC example under symmetrical operation conditions.

It should be mentioned that herein u_{phsum} , i_{phsum} , u_{phdiff} and i_{phdiff} only constitute objective variables, which are practicably not measurable but they are of great value for proving later described phenomenons.

6.4.1 Harmonic orders

By comparing the harmonic orders of the individual quantities in the right columns of figures 6.2I - 6.2III and 6.3I- 6.3III with the results of chapter 4 one can easily verify the good agreement. Especially the fact that the harmonic orders of the DC-side quantities i_{D1} , i_{D2} and u_{D1} , u_{D2} differ from the harmonic orders of their sum $(i_{D1} + i_{D2} (=-i_0), u_{D1} + u_{D2})$ or their difference $(i_{D1} - i_{D2}, u_{D1} - u_{D2})$ can clearly be seen in figure 6.2III.

System parameters: AC-system impedance: $l_L = 0$ [p.u.]; $r_L = 0$ [p.u.] decoupling impedance: l = 0.2 [p.u.] r = 0.005 [p.u.] DC-side capacitance: $c_{tot}=0.5$ [p.u.] or $\tau_{c_{tot}}=1.44$ msec. (FFM); $\tau_{c_{ini}} = 1.56$ msec. (off-line opt. PWM); Per unit [p.u.] and capacitor time constant $\tau_{c_{int}}$ definition in appendix A.1 and appendix A.2 respectively Modulation schemes: Fundamental frequency modulation (FFM): switching frequency: 50Hz eliminated harmonic: 5th harmonic m = 1.211modulation index: (NP-angle $\beta = \pi/10$, table 3.1 in chapter 3.4) off-line optimized PWM: switching frequency: 250Hz eliminated harmonics: 5th, 7th, 11th, 13,th 17th harmonic modulation index: m = 1.166 (table 3.1 in chapter 3.4) table 6.1: parameters of the SVC (figure 6.1) for the simulations in chapter 6.4 - chapter 6.6, chapter 7.3 - chapter 7.5 (if not otherwise explicitly stated)

ł



fig 6.2I: line diagram and amplitude spectra of u_{Lph} , s_{ph} , u_{ph} , u_{Zph} and i_{ph} for the FFM modulated SVC in the nominal capacitive mode at symmetrical operation conditions, parameters according to table 6.1



fig 6.2II: line diagram and amplitude spectra of u_{SP} , u_{phsum} , i_{phsum} , u_{phdiff} and i_{phdiff} for the FFM modulated SVC in the nominal capacitive mode at symmetrical operation conditions, parameters according to table 6.1



fig 6.2III: line diagram and amplitude spectra of $i_{D1/D2}$, $u_{D1/D2}$, i_{Ddiff} , i_0 , u_{Dsum} and u_{Ddiff} for the FFM modulated SVC in the nominal capacitive mode at symmetrical operation conditions, parameters according to table 6.1

6.4.2 DC-side quantities

Concerning design questions, the individual variations in time of the 3-level VSI voltages and currents are of great help. Though not all subplots of figures 6.21 - 6.2III and 6.3I- 6.3III are discussed in depth, they nevertheless are presented in order to get familiar with the 3-level VSI quantities.

Having a closer look at the variations in time in figure 6.2III left column, plot b) and d), it is important to mention that the peak values of each DC-voltage u_{D1} and u_{D2} are higher than the peak value of half the sum of both $u_{Dsum}/2 = (u_{D1} + u_{D2})/2$.

It should be pointed out, that the stress of the capacitors and, what is more worse, of the valves is determined by the particular DC-voltages u_{D1} and u_{D2} and not by half of their sum $(u_{D1} + u_{D2})/2$. Here, an overdimensioning of about 15% for the valves and capacitors with regard to the expected values is necessary. It should be emphasized, that this, especially in high power applications, is quite a lot and will cause undesirable higher costs!

This phenomenon can be explained by the harmonics being odd numbered multiples of 3 in u_{D1} and u_{D2} , which are eliminated in u_{Dsum} . Especially the 3rd harmonic contributes with the largest amount to the peak values of u_{D1} and u_{D2} , which can be verified in their spectra in figure 6.2III right, plot b).

These results are principally not astonishing from a qualitative point of view, since they mathematically and graphically have been derived yet in chapter 4.3.2 and chapter 5.4.3. However, here their quite impressive quantitative influence on the dimensioning of the 3-level VSI can clearly be seen for the first time.

In order to investigate the influence of the switching frequency on this 3level VSI specific drawback, the off-line optimized pulse pattern with a switching frequency $f_{s_{ph}}=250$ Hz ($f_{s_{ph}}=5$ [p.u.]) was chosen and a simulation with otherwise the same parameters has been performed. The results can be seen in the figures 6.3I - 6.3III. For reasons of clarity all AC-side quantities are represented only by means of phase a, since the phases b and c look the same except of the phase shift $2/3\pi$.

By comparison of figure 6.2III left column, plot d) with figure 6.3III left column, plot d) it can be concluded that the ripple of the total DC-side voltage u_{Dsum} has decreased for the off-line optimized PWM modulated SVC.

However, the ripple and the peak values of the individual DC-side voltages

amplitude spectrum line diagram 1.5 10⁰ a) u_{La} u_{Lph} 0.5 ['n'd] [p.u.] (10⁻² -0.5 -1 10-3 -1.5 5 10 15 20 25 0 0 1.5 r 0.015 0.02 0.005 0.01 10⁰ b) s_a s_{ph} 1 0.5 [--10-1 [bir] [b.u.] 10-2 -0.5 -1 10-3 -1.5 10 15 20 25 0 5 0.005 0.015 0.02 0.01 n 1.5 10⁰ c) u_{ph} иа 1 0.5 [---10-1 [bir] [p.u.] 10⁻² -0.5 -110-3 -1.5 20 25 5 10 15 0 0.015 0.02 0.005 0.01 n 1 d) 10⁰ u_{Za} u_{Za} 0.5 [i] 10⁻ [b.u.] 10-2 -0.5 10⁻³ -110 15 25 5 20 0 0 1.5 -0.015 0.02 0.005 0.01 10⁰ i_a i_{ph} e) 1 0.5 [i 10⁻¹ d [b.u.] 0 10-2 -0.5 -1 -1.5 0 10-3 0 5 10 15 20 25 0.005 0.01 0.015 0.02

fig 6.3I: line diagram and amplitude spectra of u_{Lph} , s_{ph} , u_{ph} , u_{Zph} and i_{ph} for the off-line optimized PWM modulated SVC in the nominal capacitive mode at symmetrical operation conditions, parameters according to table 6.1

t[sec.]

harmonic order k



fig 6.3II: line diagram and amplitude spectra of u_{SP} , u_{phsum} , i_{phsum} , u_{phdiff} and i_{phdiff} for the off-line optimized PWM modulated SVC in the nominal capacitive mode at symmetrical operation conditions, parameters according to table 6.1



fig 6.3III: line diagram and amplitude spectra of $i_{D1/D2}$, $u_{D1/D2}$, i_{Ddiff} , i_0 , u_{Dsum} and u_{Ddiff} for the off-line optimized PWM modulated SVC in the nominal capacitive mode at symmetrical operation conditions, parameters according to table 6.1

 u_{D1} and u_{D2} (figure 6.3III left column, plot b)) nearly have remained the same in comparison to FFM modulation (figure 6.2III left column, plot b))! By opposing the spectra of u_{D1} and u_{D2} for the two different pulse patterns, it can be observed that the most dominant harmonic component, the 3rd harmonic, has about the same size in both simulations.

The fact that the 3rd harmonic of u_{D1} and u_{D2} does not exhibit a significant dependancy on the switching frequency of the pulse patterns was also confirmed by the statements and simulation results in chapter 5.6.

A reduction of the 3rd harmonic in u_{D1} and u_{D2} could be achieved by installing a filter or by increasing the size of the DC-side capacitors c, which might constitute the cheaper solution. The latter will be investigated more in depth in chapter 6.6.

6.4.3 AC-side quantities

Another interesting point to focus on is with respect to the harmonic content of the phase currents i_{ph} on the AC-side, which will be performed in the following.

The PWM pulse patterns for the example in figures 6.3I - 6.3III were optimized for the elimination of the 5th, 7th, 11th, 13th and 17th harmonic. This can be verified by the spectra of s_{ph} in figure 6.3I right column, plot b), where no 5th, 7th, 11th, 13th and 17th harmonic are present. Therefore, these harmonics are also not to be expected in the AC-side currents i_{ph} .

However, due to their elimination in s_{ph} , these harmonics appear in the 3level VSI output voltages u_{ph} and currents i_{ph} as it is proved in figure 6.3I right, plot c) and e). This is an astonishing result! Though the amplitudes of the 11th, 13th and 17th harmonic are very small, those of the 5th (0.03 [p.u.]) and 7th harmonic (0.01 [p.u.]) are not negligible in a high voltage transmission application, where the harmonic emission limits usually are very strict.

Hence it is of great interest to study the origin of this phenomenon. For that purpose, the two parts u_{phsum} and u_{phdiff} of the splitted 3-level VSI output voltages u_{ph} are of great help. By comparing their spectra in figure 6.3II right column, plot b) and d), it is evident that mostly u_{phdiff} contributes to the 5th and 7th harmonic in the AC-side currents i_{ph} , or exactly i_{phdiff} . u_{phdiff} in its turn is a function of u_{Ddiff} and the squared switching functions s_{ph}^2 or $|s_{ph}|$ (eqn. (2.7) or eqn. (2.8) in chapter 2.4.1).

According to the decomposition of s_{ph}^2 or $|s_{ph}|$ and u_{Ddiff} (table 4.2 and

table 4.8 in chapter 4.3) and the harmonic transfer rule from the DC- to the AC-side (table 4.9 in chapter 4.3.3), the generation of the 5th and 7th harmonic is determined. The 5th harmonic will mainly be caused by the convolution of the lowest ordered harmonic of u_{Ddiff} (the 3rd) with the lowest ordered harmonic of s_{ph}^2 or $|s_{ph}|$ (the 2nd). The 7th harmonic will predominantly be the result of the convolution of the 3rd harmonic in u_{Ddiff} with the 4th harmonic of s_{ph}^2 or $|s_{ph}|$.

Since these lowest ordered harmonics in u_{Ddiff} and s_{ph}^2 do not decrease significantly with increasing switching frequencies, this phenomenon as well can only be influenced by means of a 150 Hz filter for $u_{D1/D2}$ or a larger DC-capacitor size (see also chapter 6.6.2).

It was shown that the 3rd harmonic in $u_{D1/D2}$ will cause a 5th and 7th harmonic to arise in i_{phdiff} and with that also in i_{ph} . More, these 5th and 7th harmonic in i_{ph} , convoluted with the fundamental component of s_{ph} , will in its turn yield a small 6th harmonic to arise in u_{Dsum} (eqn. (2.36) in chapter 2.4.3). Then, this 6th harmonic in u_{Dsum} will be transferred back as a small 5th and 7th harmonic in u_{phsum} (eqn. (2.13) in chapter 2.4.1), which finally also causes harmonic components of the same orders to appear in i_{phsum} . The graphic d) in the right column of figure 6.3III and the graphics b) and c) in the right column of figure 6.3II prove the validity of these statements.

Of course, also the higher ordered harmonics of u_{Ddiff} will at least theoretically have an influence on the 3-level VSI AC-side harmonics in the same way as described above. However, they usually show up quite small amplitudes and therefore their AC-side contributions can be neglected in most cases.

Hence, it can be summarized that the odd numbered harmonics in $u_{D1/D2}$ (predominantly the 3rd) will cause odd numbered AC-side current harmonics to arise (predominantly the 5th and 7th), independently on their elimination in the switching functions s_{ph} .

6.4.4 Influence of AC-system voltage harmonics

Up to now, the AC-system voltages u_{Lph} have been assumed to form an ideal cosinusoidal 3-phase system. Hence, the AC-system did not contribute with harmonics, which were entirely caused by the 3-level VSI and its switching functions.

Usually the very low harmonic distortion of a high voltage AC-system will

not have a significant influence on the harmonics apparent on the AC- and the DC-side of the VSI. However some exceptional cases exist, where a specific harmonic in the AC-system voltages u_{Lph} will cause an increased stress for the 2-level or 3-level VSI.

This might happen, if e.g. a specific harmonic in u_{Lph} would coincide with one of the system resonances, which are determined by the reactive components of both the AC-system and the 2- or 3-level VSI. The hereby arising problems have been investigated in depth in [60] - [62] for the 2-level VSI and are also present for the 3-level VSI topology. Hence, this will not further be studied in this thesis.

It was also shown in [62], that a positive sequence 2nd harmonic in u_{Lph} will yield DC-components to arise in the AC-side phase currents i_{ph} , which in its turn will saturate the inverter transformer. Though this was proved for the 2-level VSI, it is also valid for the 3-level VSI topology, which could be verified with the general harmonic transfer rules presented in chapter 4.3.2 and chapter 4.3.3.

On the other side, a negative sequence 2nd harmonic in u_{Lph} usually will not cause any serious trouble for the 2-level VSI, presuming that there is no excitation of a system's resonance. However, this will be subject to change, if the 3-level VSI topology is chosen instead of the 2-level VSI. It should be anticipated here, that for a 3-level VSI a negative sequence 2nd harmonic in u_{Lph} will cause an unbalance in the DC-side voltages u_{D1} and u_{D2} . This phenomenon will be investigated more in depth in chapter 7.5.4.

6.5 Asymmetrical operation conditions

The steady state performance of the 3-level VSI under asymmetrical operation conditions will also be of major importance. Especially investigations on the stress of the 3-level VSI components and valves are of high interest. Therefore this will be studied in this chapter for the 3-level VSI SVC example.

As a case for asymmetrical operation conditions a single line voltage drop of 75% in the AC-system voltage u_{La} is assumed.

Hereby, the fundamentals of the AC-currents i_{ph} are controlled in a way that they form a symmetrical 3-phase system. This will be achieved by a feed-forward controller, which ensures that the stress of all components can be kept at a tolerable level. The feed-forward controller is described in detail

in chapter 9.4. However, it should be mentioned, that both the higher ordered harmonics of i_{ph} and all harmonics of s_{ph} , including the fundamental, constitute an asymmetrical 3-phase system according to the definition in chapter 4.4.

The following figures 6.4I - 6.4III present the simulation results. It should be noted that for clarity reasons, the AC-side spectra are only represented by phase a, since no other harmonic orders appear in phase b and c. Though the particular harmonic amplitudes are not the same for all 3 phases, they are not of importance here.

6.5.1 Harmonic orders

First of all, concerning the harmonic orders of the individual 3-level VSI quantities, one can verify the good agreement with the qualitative harmonic analysis performed in chapter 4.4.

Especially the fact that the harmonic orders of the DC-side quantities $i_{D1/D2}$, $u_{D1/D2}$ show up all even and odd numbered harmonics, which is different from the 2-level VSI, can clearly be seen in figure 6.4III right column, plot a) and b). Also, in analogy to symmetrical operation conditions, it is shown that specific harmonic orders (either the even or the odd numbered) are eliminated in the sum or difference of $i_{D1/D2}$ and $u_{D1/D2}$ (figure 6.4III right column, plot c) and d)).

Regarding the AC-side, it is further evident in figure 6.4I - 6.4II that the ACside current spectra now also include all odd numbered multiples of 3 as predicted in chapter 4.4.1.

6.5.2 DC-side quantities

The most significant harmonics in $u_{D1/D2}$ (figure 6.4III right column, plot b)), which simultaneously are exclusively caused by asymmetrical operation conditions, are the 50Hz and the 100Hz component.

The 50Hz harmonic is principally generated by the convolution of the ACside current fundamental with the 2nd harmonic of s_{ph}^2 (positive sequence component). The 100 Hz harmonic on its side is mainly the result of the convolution of the fundamentals of i_{ph} and s_{ph} . This can easily be verified with the help of the harmonic transfer rule deduced in chapter 4.4 and the decomposition of i_{ph} , s_{ph} and s_{ph}^2 in symmetrical components (table -4.16 in chapter 4.4.1).

It should be pointed out, that also these 50 Hz and 100Hz harmonics cannot



fig 6.4I: line diagram and amplitude spectra of u_{Lph} , s_{ph} , u_{ph} , u_{Zph} and i_{ph} for the FFM modulated SVC in the nominal capacitive mode at asymmetrical operation conditions (single line voltage drop of 0.75 [p.u.] in phase a), parameters according to table 6.1



fig 6.4II: line diagram and amplitude spectra of u_{SP} , u_{phsum} , i_{phsum} , u_{phdiff} and i_{phdiff} for the FFM modulated SVC in the nominal capacitive mode at asymmetrical operation conditions (single line voltage drop of 0.75 [p.u.] in phase a), parameters according to table 6.1



fig 6.4III: line diagram and amplitude spectra of $i_{D1/D2}$, $u_{D1/D2}$, i_{Ddiff} , i_0 , u_{Dsum} and u_{Ddiff} for the FFM modulated SVC in the nominal capacitive mode at asymmetrical operation conditions (single line voltage drop of 0.75 [p.u.] in phase a), parameters according to table 6.1

be remarkably reduced by means of a higher switching frequency, since mainly the fundamentals of i_{ph} , s_{ph} and s_{ph}^2 contribute to their generation.

In opposite, during asymmetrical operation conditions, the 2-level VSI mainly contributes with only a 100 Hz component in the DC-side voltage. In order to reduce this 100 Hz component, it often makes sense to install a filter on the DC-side ([68]).

It should be emphasized, that the same measure applied to the 3-level VSI asks for 50 Hz- and 100 Hz filters instead of one 100 Hz filter, which will increase the costs in comparison to the 2-level VSI! Especially the 50 Hz filters will have a larger size than the 100 Hz filters and will therefore be more expensive.

The simulation of the off-line optimized PWM modulated 3-level SVC at asymmetrical operation conditions does not yield new results and will therefore not be presented.

The discussions in the two chapters 6.4 and 6.5 confirmed the usefulness of the detailed 3-level VSI equations (chapter 2.4) and the qualitative harmonic analysis (chapter 4). With their help it was quite simple to analyse some 3-level VSI specific effects, which are not known from the 2-level VSI.

It can be concluded that both for a reasonable system design and for a proper elimination of specific low ordered AC-side harmonics, the DC-side capacitor value must not be chosen too small.

6.6 Influence of the DC-side capacitor size

The previous chapter showed that the size of the DC-side capacitors has to be chosen carefully in order to keep the stress of the components at a tolerable level.

As discussed yet, increasing the switching frequency is not capable to reduce the specific DC-side harmonics in u_{D1} and u_{D2} in a sufficient way.

DC-side filters would fulfil these requirements, however they produce additional costs and losses. Especially for the 3-level VSI, where filters for 50 Hz, 100Hz and 150 Hz would be necessary to deal both with symmetrical and asymmetrical operation conditions, this solution is not competitive at all. A reasonable approach might be therefore to increase the DC-capacitor size. Another point of interest concerns the dependancy of the individual AC-side current harmonics and of the THD (Total Harmonic Distortion) on the DC-side capacitor size.

Both subjects will now be investigated more in depth for FFM and off-line optimized PWM ($f_{s_{ph}} = 250$ Hz, $f_{s_{ph}} = 5$ [p.u.]) by means of the 3-level SVC-example. The same system parameters as up to now are assumed (table 6.1), except of a varying DC-side capacitor size. In addition the results will be compared with those of a FFM and off-line optimized PWM ($f_{s} = 250$ Hz, $f_{s_{ph}} = 5$ [p.u.]) modulated 2-level VSI SVC-example. The 2-level VSI SVC has identical system parameters as the 3-level VSI SVC and is also supposed to work in the nominal capacitive mode. However, no harmonics can be eliminated for off-line optimized PWM with a switching frequency of $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]). Therefore, on first sight, a larger stress for the valves and the DC-side capacitors should really be expected for the 2-level VSI compared with the 3-level VSI.

In this chapter only results for symmetrical operation conditions are presented due to the following two reasons:

- concerning the influence of the capacitor size on the DC-side voltages $u_{D1/D2}$, it will be anticipated here, that both for symmetrical and asymmetrical operation conditions very similar qualitative results were achieved for the SVC-example.
- with regard to particular harmonics and the THD it makes no sense to investigate the influence of the capacitor size under asymmetrical operation conditions. During disturbances the most important task of the SVC is to limit its currents and voltages and to stabilize the AC-network, however not to be as mains friendly as possible.

Finally it should be mentioned that also the results presented in this chapter are basing on the solution of the system equations by means of the matrix exponential. Here again this method is of great value.

6.6.1 DC-side voltages

The minimal stress for the valves and the capacitors is achieved with an infinite capacitor value, which implies that u_{Dsum} is a pure DC-component and u_{Ddiff} equals 0.

However, very large sized capacitors cause higher costs and also might
make it impossible to design a control with fast response times. This is true for control schemes, where the DC-side voltages have to be increased or decreased in order to change the values of the control variables, as more detailed described in chapter 9.3.

Therefore, this chapter focuses on finding a reasonable small capacitor value, which simultaneously ensures that the DC-side voltage harmonics will be sufficiently damped.

The peak values \hat{u}_{D1} and \hat{u}_{D2} of u_{D1} and u_{D2} for a specific total DC-side capacitance c_{tot} will be a good measure to assess the influence of the harmonic ripple. Comparing them with the theoretical minimum peak value of u_{D1} and u_{D2} (achieved for $c_{tot} \rightarrow \infty$), yields the increase of the 3-level VSI power rating due to the harmonic ripple on the DC-side.

Based on this minimum peak value $\hat{u}_{D1/D2}(c_{tot} \rightarrow \infty)$, figure 6.5 shows the extra harmonic voltage stress $\Delta \hat{u}_{D1/D2}$ in dependancy on the capacitor size, varying from $c_{tot}=0.5$ [p.u.] or $\tau_{c_{tot}}=1.44$ msec up to a reasonable large size $c_{tot}=4$ [p.u.] or $\tau_{c_{tot}}=1.52$ msec.

 $\Delta \hat{u}_{D1/D2}$ is hereby defined according to eqn. (6.2)

$$\Delta \hat{u}_{D1/D2}(c_{tot}) = \hat{u}_{D1/D2}(c_{tot}) - \hat{u}_{D1/D2}(c_{tot} \to \infty) \quad [\text{p.u.}]$$
(6.2)

The analog definition for the 2-level VSI is given by eqn. (6.3):

$$\Delta \hat{u}_D(c_{tot}) = \hat{u}_D(c_{tot}) - \hat{u}_D(c_{tot} \to \infty) \quad [\text{p.u.}]$$
(6.3)

With that the results are independent on the topology (2- or 3-level VSI) and the individual DC-components of $u_{D1/D2}$ (u_D), the latter of which vary with the modulation index m of the switching functions s_{ph} .

It can be seen in figure 6.5, that the deviations $\Delta \hat{u}_{D1/D2}$ ($\Delta \hat{u}_D$) from the above mentioned stress minimum decrease with larger capacitor sizes c_{tot} . As one could expect, $\Delta \hat{u}_{D1/D2}$ is reciprocally proportional to c_{tot} .

For further investigations, the tolerable extra stress is assumed to be about 5%. Hence, c_{tot} for the 3-level VSI has to be chosen to at least $c_{tot}=1.5$ [p.u.] or $\tau_{c_{tot}}=4.32$ msec to fulfil this demand. The 2-level VSI in its turn satisfies this request with approximately the same capacitor size, as shown in the right graphic of figure 6.5.

On first sight the result is a little bit astonishing since for the 2-level VSI, compared to the 3-level VSI, the 5th and 7th AC-side harmonics are not eliminated or reduced, but contribute with quite large values. These two har-



fig 6.5: DC-side harmonic voltage stress in dependancy on the capacitance c_{tot} for the FFM modulated 3-level and 2-level VSI, pure capacitive operation mode

monics generate a predominant 6th harmonic in the DC-side voltage u_D , which mainly causes the extra stress of the 2-level VSI capacitor and valves. For the 3-level VSI, this 6th DC-side harmonic cannot be expected to be as large as for the 2-level VSI, since its generating AC-side harmonics, the 5th and the 7th, are eliminated or at least reduced. All the same it is evident in figure 6.5, that the extra stress $\Delta \hat{u}_{D1/D2}$ for the inverter valves and capacitors is slightly higher for the 3-level VSI than for the 2-level VSI.

This can be explained by the fact, that the stress of the 3-level VSI components is caused by the individual DC-side voltages $u_{D1/D2}$ which in addition to the harmonics being multiples of six also include all odd numbered multiples of 3. Hereby it could be observed for the FFM modulated 3-level VSI that the extra stress is almost exclusively determined by the 3rd harmonic in $u_{D1/D2}$.

More, as shown in chapter 5.6 and chapter 6.4, the switching frequency has no significant influence on the amplitude of this 3rd harmonic. On the other side, the harmonics being multiples of six can be reduced since they do not arise from fundamentals of AC-side quantities but from higher ordered harmonics (5th, 7th...), which in its turn can be eliminated by e.g. off-line optimized PWM.

In order to prove the latter mentioned statement, a simulation has been performed for the off-line optimized PWM modulated 3- and 2-level VSI SVC. The results for a switching frequency $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]) are presented in figure 6.6.



fig 6.6: DC-side harmonic voltage stress in dependancy on the capacitance c_{tot} for the off-line optimized PWM modulated 3-level and 2-level VSI, switching frequency $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]), pure capacitive operation mode

While the size of the 3-level VSI capacitors only slightly can be reduced in order to guarantee $\Delta \hat{u}_{D1/D2} \leq 0.05$, the 2-level VSI capacitor might be shrinked to less than $c_{tot} = 1$ [p.u.] or $\tau_{c_{tot}} = 2.88$ msec.

Again, as discussed in chapter 6.4, this can be explained by the fact, that the most dominant component in $u_{D1/D2}$, the 3rd harmonic, has not significantly decreased. Also here it could be observed that the peak-value of the individual DC-side voltage ripples were close to the amplitude value of the 3rd harmonic.

The small decrease of $\Delta \hat{u}_{D1/D2}$ for off-line optimized PWM in comparison to FFM modulation is moreover established by a decrease in the fundamental component (the modulation index m) of the switching functions s_{ph} . According to table 3.1 of chapter 3.4.4, the modulation index has decreased from m=1.211 for FFM modulation to m=1.166 for a switching frequency $f_{s_{ph}}=250$ Hz ($f_{s_{ph}}=5$ [p.u.]). Since the amplitude of the 3rd harmonic in $u_{D1/D2}$ is proportional to the squared value of the switching function's fundamental amplitude, the same is true for the peak-value of the ripple $\Delta \hat{u}_{D1/D2}$.

As it is also evident in table 3.1 of chapter 3.4.4, the pulse patterns with higher switching frequencies than $f_{s_{ph}} = 250 \text{Hz} (f_{s_{ph}} = 5[\text{p.u.}])$ also can show up similar large fundamental amplitudes (modulation indices m) of about 1.15 [p.u.]. Hence, the 3rd harmonic amplitude in $u_{D1/D2}$ will not remarkably decrease if the switching frequency is further increased, which in addition is shown in chapter 5.6 (figure 5.16, figure 5.17).

In contrary to that, no 3rd harmonic will be present in the DC-side voltage u_D of the 2-level VSI. Therefore the increase of the switching frequency yields a more impressive decrease for the DC-side ripple due to the elimination of the 5th and 7th AC-side harmonics, which as a result eliminate the 6th harmonic on the DC-side. The elimination of additional higher ordered harmonics (11th, 13th,...) by further increasing the switching frequency will reduce the extra stress $\Delta \hat{u}_D$ for the 2-level VSI capacitor and values to negligible values.

Therefore, it can be concluded that for the 3-level VSI a larger capacitor size has to be chosen than for a 2-level VSI in order to guarantee the same DC-side voltage ripple. Hereby, the same power rating for both topologies is assumed.

However, this drawback of the 3-level VSI can be compensated by an advantage, which will become evident in the next two chapters.

6.6.2 AC-side current harmonics

Concerning the harmonic content of the AC-side currents i_{ph} , it is not evident that for a given switching function s_{ph} an infinite large capacitor yields the best results as it is true for the harmonic voltage stress of the components. To find general valid answers to this question, if at all possible, a probably complex mathematical analysis has to be performed, which was not carried out in this thesis. Hence, only the simulation results for the FFM and the off-line optimized PWM ($f_{s_{ph}} = 250$ Hz, $f_{s_{ph}} = 5$ [p.u.]) modulated 3-level SVC example are presented and compared with those of the 2-level SVC.

As representative AC-side current harmonics, the lower ordered from the 5th up to the 13th are taken into account. The results for FFM modulation are shown in figure 6.7.

It is interesting that the individual harmonics do not manifest a similar behaviour. While the 5th harmonic decreases with increasing capacitor size, the opposite is true for the 7th - 13th. As mentioned yet, the reasons for this phenomenon will not be studied in depth. The only intention here is to get a quantitative feeling for the variation of the particular harmonic amplitudes in dependancy on the capacitor size. From figure 6.7 it can be summarized that this decrease/increase is not larger than ± 0.05 [p.u.] over the investigated capacitor range.

Further it can be seen in figure 6.7 that for $c_{tot} \ge 3$ [p.u.] or



fig 6.7: 5th, 7th, 11th and 13th AC-side current harmonics in dependancy on the capacitance c_{tot} for the FFM modulated 3-level and 2-level VSI, pure capacitive operation mode

 $\tau_{c_{tot}} \ge 8.64$ msec the amplitudes of the particular AC-side current harmonics nearly remain at a constant value. This applies both for the 3- and 2-level VSI. Hence, it can be concluded that for capacitance values $c_{tot} \ge 3$ [p.u.] or $\tau_{c_{tot}} \ge 8.64$ msec, the simplified analysis with analytical methods (assuming $c_{tot} \to \infty$) would yield excellent approximation results for the ACside quantities.

It is also obvious, that the 5th harmonic is significantly reduced for the 3level VSI compared to the 2-level VSI, which is achieved by the optimized NP-angle (take notice of the different scale for the vertical axes in figure 6.7). Also the 7th harmonic shows up a smaller amplitude for the 3level VSI than for the 2-level VSI. Besides its nearly doubled power rating without the need for a more sophisticated transformer topology, this exhibits another advantage of the 3-level VSI in contrary to the 2-level VSI.

Figure 6.8 presents the results for the off-line optimized PWM modulated 3and 2-level SVC. Again, the switching frequency is chosen to $f_{s_{ph}}=250$ Hz ($f_{s_{nh}}=5$ [p.u.]).

Concerning the 3-level VSI, it could be expected that all harmonics up to the 17th order will not be present in the AC-side currents i_{ph} , since they are eliminated in the pulse patterns s_{ph} . With regard to the 2-level VSI, exclusively the 5th and 7th harmonic should be eliminated in s_{ph} and with that also in i_{ph} .

While the 2-level VSI clearly confirms these assumptions (right graphic in figure 6.8), the same does not prove right for the 3-level SVC (left graphic



fig 6.8: 5th, 7th, 11th and 13th AC-side current harmonics in dependancy on the capacitance c_{tot} for the off-line optimized PWM modulated 3-level and 2-level VSI, switching frequency $f_{s_{ph}} = 250$ Hz $(f_{s_{ph}} = 5[p.u.])$, pure capacitive operation mode

in figure 6.8). Especially the 5th and 7th harmonic contribute with not negligible values, at least for capacitor values $c_{tot} \le 1.5$ [p.u.] or $\tau_{c_{tot}} \le 4.32$ msec and might therefore ask for an additional AC-side filter. The 11th and 13th AC-side current harmonics are very close to 0 and will for sure not have to be filtered.

Again, as discussed in chapter 6.4, this phenomenon can be explained by the 3-level VSI specific 3rd harmonic in $u_{D1/D2}$, which is not apparent in the 2-level VSI DC-voltage u_D . In order to limit the effect of this harmonic, the capacitors on the DC-side have to be designed carefully. It is evident in the left graphic of figure 6.8, that also here a total capacitance of at least $c_{tot} = 1.5$ [p.u.] or $\tau_{c_{tpl}}$ =4.32 msec will restrict all low ordered AC-side current harmonics to values smaller than 0.01 [p.u.].

Finally, it should be noted that the same phenomenon can also be observed for the 5th AC-side current harmonic of the FFM modulated 3-level SVC in the left graphic of figure 6.7. This 5th harmonic really should not be present in i_{ph} since it is eliminated in s_{ph} , however all the same appears with values up to 0.025 [p.u.], driven by the 3rd harmonic in $u_{D1/D2}$. Also here, a minimum total capacitance of about $c_{tot} = 1.5$ [p.u.] or $\tau_{c_{tot}} = 4.32$ msec is appropriate to limit the 5th harmonic to a value not larger than 0.01 [p.u.].

6.6.3 AC-side current THD

In order to also take into account the higher ordered harmonics, the dependancy of the THD of the AC-side currents on the capacitor size will be studied. For that purpose the AC-side current harmonics up to the 500th order are considered. Hereby the THD is defined according to the definition introduced in chapter 3.7.2e) (eqn. (3.10):

$$THD_i = \frac{\sqrt{\sum_{k} I_k^2}}{I_1}$$
 [p.u.] $k \in K = 5,7,11,13,...$ (6.4)

The results for the FFM modulation are given in figure 6.9. It can be ob-



fig 6.9: THD of the AC-side currents i_{ph} in dependancy on the capacitance c_{tot} for the FFM modulated 3-level and 2-level SVC, pure capacitive operation mode

served that the influence of the capacitor size on the THD_i is small, especially for the 3-level topology. More, for capacitor values $c_{tot} \ge 3$ [p.u.] or $\tau_{c_{tot}} \ge 8.64$ msec, the THD_i nearly remains at a constant value. The last statement even is true over the whole investigated capacitor range for the off-line optimized PWM modulated SVC, as presented in figure 6.10.

Finally, figures 6.9 - 6.10 prove the benefit of the 3-level VSI's additional degree of freedom, the NP-angles, where an impressive improvement of the THD_i can be achieved by eliminating or reducing specific harmonics. It should be emphasized, that hereby the switching frequency of the individual valves is the same for the 3- and 2-level VSI. Therefore no extra losses arise for the 3-level VSI. More, remarkable savings on AC-side filters can be ob-



fig 6.10: THD of the AC-side currents i_{ph} in dependancy on the capacitance c_{iot} for the off-line optimized PWM modulated 3-level and 2-level VSI, switching frequency $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5$ [p.u.]), pure capacitive operation mode

tained. This advantage easily compensates for the drawback of larger capacitor sizes for the 3-level VSI compared to the 2-level topology.

6.7 Summary

In this chapter, the piece-wise linear differential equations of the 3-level VSI connected to an AC-system (chapter 2.4) have been solved using the matrix exponential method and the simulation tool MATLAB. Hereby, also small DC-side capacitor values have been taken into account. This has been performed for exclusively reactive power exchange with the AC-system by means of a static Var Compensator.

Advantages of the matrix exponential solution method include numerical stability, exact steady state results with no influences of control and resonances and last but not least simulation time savings.

The validity of the qualitative harmonic analysis was confirmed and in addition some possible disadvantages of the 3-level VSI showed up.

For desirable small capacitor sizes of about $c_{tot} = 1$ [p.u.] or $\tau_{c_{tot}} = 2.88$ msec, one drawback is manifested in an extra stress for the valves and capacitors in comparison to the 2-level VSI, which is caused by the oscillating neutral-point (NP) potential.

Also another disadvantage is caused by these oscillations of the neutral-

point (NP) potential, which increase with smaller capacitor values. For offline optimized PWM (chapter 3.4) with selective elimination of specific harmonics and a finite capacitor size, the eliminated switching function harmonics will not appear the AC-side currents. However, applying small capacitor sizes ($c_{tot} = 1$ [p.u.] or $\tau_{c_{tot}} = 2.88$ msec), this is subject to change for the 3-level VSI. Due to the oscillating neutral point potential, which also appears in the 3-level VSI output voltages, harmonics of the eliminated orders can be generated. This is especially true for the 5th and 7th harmonic, which might reach amplitudes up to 0.03[p.u.].

It was shown in chapter 5, that the undesirable 3rd harmonic oscillation in the individual DC-side voltages u_{D1} and u_{D2} can hardly be reduced by increasing the switching frequency. In this chapter, these results have been confirmed for a SVC with realistic parameters (r=0.005[p.u.], l=0.2[p.u.]) and a small DC-side capacitance ($c_{tot} = 0.5[p.u.]$, $\tau_{c_{tot}} = 1.44$ msec) by means of line diagrams. Hereby, the switching frequencies of the off-line optimized pulse patterns have been chosen to $f_{s_{ph}} = 50$ Hz ($f_{s_{ph}} = 1[p.u.]$) and $f_{s_{ph}} = 250$ Hz ($f_{s_{ph}} = 5[p.u.]$). It could also be seen, that this DC-side 3rd harmonic oscillations is quite large for a small capacitor ($c_{tot} = 0.5[p.u.]$, $\tau_{c_{tot}} = 1.44$ msec) and will reach peak-values of about 0.15[p.u.].

Finally, the influence of the DC-side capacitor size on the stress of the components and the influence on the AC-side currents (individual harmonics, THD) was investigated. From this it could be concluded once more, that especially for the 3-level VSI, the capacitors must not be chosen too small in order to limit the overdimensioning of the components with regard to a theoretical minimum achieved for $c_{tot} \rightarrow \infty$.

For an infinite capacitor size $c \to \infty$, the 3-level VSI output voltage harmonics would be exactly proportional to the switching function harmonics. It could be shown, that this will also approximately be fulfilled for a total DC-side capacitance larger than $c_{tot} \ge 3$ [p.u.] or $\tau_{c_{tot}} \ge 8.64$ msec. Decreasing the capacitor size down to values $c_{tot} = 0.5$ [p.u.] or $\tau_{c_{tot}} = 1.44$ msec, in fact no additional harmonic orders will arise (chapter 4), however the harmonic amplitudes in the AC-side currents might vary. In addition, eliminated lower ordered switching function harmonics might also arise in the AC-side currents due to the remarkably oscillating NP-current potential.

On the other side, it could be shown that the <u>Total Harmonic Distortion</u> (*THD*) of the AC-side currents, will hardly be influenced by a varying capacitor size.

Comparing the *THD* of the 3- and 2-level VSI of course yielded an important advantage of the 3-level topology. Despite the same switching frequency for each 3- and 2-level VSI valve, the 3-level SVC exhibited a much smaller *THD*. This is due to its additional degree of freedom, the NP-angles, which enable the elimination or reduction of specific harmonics.

7 The 3-level VSI DC-side unbalance

7.1 Overview

This chapter is focusing on the DC-side DC-unbalance phenomenon, which constitutes one of the major 3-level VSI drawbacks. Hereby, the theoretical studies cover all operation modes (reactive and active power exchange with the AC-system).

After a short introduction, a harmonic analysis presents the additional harmonics to be expected on both the AC- and the DC-side in case of a DC-side DC-unbalance.

In a next step, the ability of the 3-level VSI to counteract to a DC-side DCunbalance without any extra control implemented (self-balancing) will be investigated in depth by mathematical analyses and by simulations with SABER.

Finally, the main sources causing a DC-side DC-unbalance are identified and their transient and steady-state impact will be investigated. The results will then be verified for a purely reactive SVC by means of mathematical analyses and simulations with SABER and MATLAB.

7.2 Introduction

The 3-level VSI is nowadays an interesting topology for high power transmission applications. Besides its advantages, one of the most important problems is to keep the DC-side voltages u_{D1} and u_{D2} balanced with regard to their DC-components.

When speaking of DC-side unbalance, one should for clearness reasons distinguish between two types of this undesirable phenomenon:

- AC-unbalance and
- DC-unbalance.

AC-unbalance between the DC-side voltages u_{D1} and u_{D2} is defined as the opposite signed oscillations in u_{D1} and u_{D2} , which vary periodically in time, but do not include a DC-component. These undesirable oscillations have been investigated yet in depth in chapter 4 - chapter 6.

DC-unbalance, in opposite to AC-unbalance, is characterized by the appearance of a DC-component in u_{Ddiff} , which means that the DC-side voltages u_{D1} and u_{D2} will have different DC-values. This chapter will exclusively focus on this DC-unbalance.

Under ideal conditions, no DC-unbalance will occur. However, there are various sources, which might introduce this kind of unbalance in the DC-side voltages. They are described in the following listing:

- transient events like AC-system faults or load steps in the controlled variables,
- even numbered harmonics in the AC-system voltages with an appropriate phase sequence,
- inaccuracies in the switching instants of the individual pulse patterns due to manufacturing tolerances of the valves or the electronic components of the gate-units.

All these listed topics will cause a DC-component to arise in the NP-current i_0 and therefore also in u_{Ddiff} , which means that the two DC-side voltages u_{D1} and u_{D2} become unbalanced. More detailed studies concerning this topic will be presented in chapter 7.5.

An existing DC-side DC-unbalance results in an increased stress for the valves and the capacitors on the DC-side. In addition, even numbered harmonics will appear in the 3-level VSI output voltages and currents, which will be analysed in chapter 7.3.

Further, regardless of the need for a control scheme to keep the DC-balance on the DC-side, also the question arises for the self-balancing abilities of the 3-level VSI, i.e. the capability to counteract to a disturbance in the DC-side DC-balance without an additional controller implemented. This topic has been the motive for many discussions, which however only were based on experimental observations on 3-level VSI hardware models. Therefore it will be of great interest to perform a mathematical analysis general valid for all applications, which gives clear answers to this question. This will also be performed here in chapter 7.4.

Finally, in the investigations to come, a DC-side DC-unbalance will shortly be denoted DC-side unbalance.

7.3 Harmonic analysis in case of a DC-side unbalance

In chapter 4, a harmonic analysis for all 3-level VSI quantities was performed, including both symmetrical and asymmetrical AC-side operation conditions.

Now the same will be done, however assuming that the AC-system voltages u_{Lph} and the switching functions s_{ph} are symmetrical 3-phase systems, while the DC-side voltages u_{D1} and u_{D2} do not have the same DC-values.

That means to answer the question for the additional harmonics arising in the 3-level VSI quantities introduced by a DC-side unbalance.

The procedure to perform this analysis is the same as in detail shown in chapter 4. Therefore, here only the results will be presented.

7.3.1 DC-side harmonics

In case of a DC-side unbalance $(U_{Ddiff} \neq 0)$, the 3-level VSI output voltage term $u_{phdiff} = s_{ph}^2 \cdot u_{Ddiff} = |s_{ph}| \cdot u_{Ddiff}$ will show up even numbered harmonics, which are generated by the convolution of the DC-component U_{Ddiff} of u_{Ddiff} with all harmonics of s_{ph}^2 or $|s_{ph}|$.

These even numbered voltage harmonics in u_{phdiff} for sure will cause even numbered current harmonics to arise in i_{phdiff} , which in its turn contribute to the resulting AC-side phase currents $i_{ph}=i_{phsum}+i_{phdiff}$. Therefore, as a basis for the harmonic analysis, the representation of i_{ph} , s_{ph} , s_{ph}^2 or $|s_{ph}|$ by symmetrical components yields table 7.1 - table 7.3.

decomposition of s_{ph} in	harmonic orders l	
positive sequence components	$l = 6 \cdot j + 1$	j = 0, 1, 2, 3
negative sequence components	$l = 6 \cdot j - 1$	j = 1, 2, 3
zero sequence components	$l = 6 \cdot j + 3$	j = 0, 1, 2, 3

table 7.1: decomposition of s_{ph} in symmetrical components in case of a DC-side unbalance (no balance control implemented)

It should be noted that with no balance control implemented the switching functions s_{ph} and s_{ph}^2 or $|s_{ph}|$ furtheron contribute with the same harmonic orders as for balanced DC-side voltages (table 4.1 and table 4.2 in chapter 4.3.1), while exclusively the AC-side currents i_{ph} show up additional harmonics (table 4.3 in chapter 4.3.1).

decomposition of s_{ph}^2 or $ s_{ph} $ in	harmonic orders l	
positive sequence components	$l = 6 \cdot j + 4$	j = 0, 1, 2, 3
negative sequence components	$l = 6 \cdot j - 4$	j = 1, 2, 3
zero sequence components	$l = 6 \cdot j$	j = 0,1,2,3

table 7.2: decomposition of s_{ph}^2 or $|s_{ph}|$ in symmetrical components in case of a DC-side unbalance (no balance control implemented)

decomposition of i_{ph} in	harmonic orders k	
positive sequence components	$k = 3 \cdot i + 1$	i = 0,1,2,3
negative sequence components	$k = 3 \cdot i - 1$	i = 1, 2, 3
zero sequence components	none	

table 7.3: decomposition of i_{ph} in symmetrical components in case of a DC-side unbalance

The harmonic orders of the sum terms $\sum_{ph} i_{ph} \cdot s_{ph}$ and $\sum_{ph} i_{ph} \cdot s_{ph}^2$ or $\sum_{ph} i_{ph} \cdot |s_{ph}|$, which according to chapter 2.4.3 determine all DC-side quantities, can then be calculated with the harmonic transfer rule from the AC- to the DC-side (chapter 4.3.2). The results are presented in table 7.4.

sum term	harmonic orders p of the sum term	
$\sum_{ph} i_{ph} \cdot s_{ph}$	$p = 3 \cdot i$	i = 0, 1, 2, 3
$\sum_{ph} i_{ph} \cdot s_{ph}^2$	$p = 3 \cdot i$	i = 0, 1, 2, 3
$\sum_{ph} i_{ph} \cdot s_{ph} $		

table 7.4: harmonic orders of $\sum_{ph} i_{ph} \cdot s_{ph}$ and $\sum_{ph} i_{ph} \cdot s_{ph}^2$ or $\sum_{ph} i_{ph} \cdot |s_{ph}|$ in case of a DC-side unbalance (no balance control implemented) With that and the equations derived in chapter 2.4.3, also the harmonic orders of all 3-level VSI DC-side quantities are known, which are given in table 7.5 and table 7.6.

DC-side current	harmonic orders p in the DC-side currents		
i _{D1}	$p = 3 \cdot i$	i = 0, 1, 2, 3	
i _{D2}	$p = 3 \cdot i$	i = 0, 1, 2, 3	
i ₀	$p = 3 \cdot i$	i = 0, 1, 2, 3	

table 7.5: harmonic orders of the DC-side currents i_{D1} , i_{D2} and i_0 in case of a DC-side unbalance

DC-side voltage	harmonic orders p in the DC-side voltages	
<i>u</i> _{D1}	$p = 3 \cdot i$	i = 0, 1, 2, 3
<i>u</i> _{D2}	$p = 3 \cdot i$	i = 0, 1, 2, 3
u _{Dsum}	$p = 3 \cdot i$	i = 0, 1, 2, 3
u _{Ddiff}	$p = 3 \cdot i$	i = 0, 1, 2, 3

table 7.6: harmonic orders of the DC-side voltages u_{D1} , u_{D2} , u_{Dsum} and u_{Ddiff} in case of a DC-side unbalance

From table 7.5 and table 7.6 it is evident that now all harmonic orders being multiples of 3 will be present in each 3-level VSI DC-side quantity.

By comparing these results with those for symmetrical operation conditions with balanced DC-side voltages (table 4.7 and table 4.8 in chapter 4.3.2), it can be concluded that the additional harmonics, introduced by the DC-side unbalance, are either even numbered multiples of 3 (in i_0 and u_{Ddiff}) or odd numbered multiples of 3 (in u_{Dsum}).

In addition also a DC-component will be present in i_0 , which for symmetrical operation conditions with no DC-side unbalance (table 4.7 in chapter 4.3.2) constitutes a DC-free quantity.

The harmonic orders of the individual DC-side voltages u_{D1} and u_{D2} will be the same in both u_{D1} and u_{D2} . Now however, their amplitudes must no longer be assumed to have identical values in u_{D1} and u_{D2} and also their phase-displacements with regard to u_{D1} and u_{D2} of either 0 or π will no more be guaranteed. The validity of this statement is strongly indicated by the fact, that no harmonics of u_{D1} and u_{D2} will be eliminated in their sum u_{Dsum} or their difference u_{Ddiff} .

Hence, in addition to unequal DC-values, also unequal harmonic amplitudes have to be expected for the two DC-side voltages u_{D1} and u_{D2} in case of a DC-side unbalance.

Finally another interesting point, which is with respect to the NP-current i_0 , should be mentioned. According to table 7.5, apparently a DC-component arises in case of a DC-side unbalance. Since this DC-component, presuming the appropriate sign, is capable to counteract to its origin, the DC-side unbalance, it might represent a self-balancing attribute of the 3-level VSI. This however will not be further investigated here but in chapter 7.4.

7.3.2 AC-side harmonics

Knowing the harmonics of the 3-level VSI DC-side quantities, it is now possible to determine the harmonics appearing on the AC-side. Applying the harmonic transfer rule from the DC- to the AC-side to the convolutions of s_{ph} with u_{Dsum} (= u_{phsum}) and s_{ph}^2 or $|s_{ph}|$ with u_{Ddiff} (= u_{phdiff}) results to table 7.7.

$u_{phsum} = \frac{s_{ph}}{2} \cdot u_{Dsum}$	harmonic	orders p
pos. seq. components	$p = 3 \cdot i + 1$	i = 0, 1, 2, 3
neg. seq. components	$p = 3 \cdot i - 1$	<i>i</i> = 1,2,3
zero seq. components	$p = 3 \cdot i$	i = 0, 1, 2, 3
$u_{phdiff} = \frac{s_{ph}^2}{2} \cdot u_{Ddiff} = \frac{ s_{ph} }{2} \cdot u_{Ddiff}$	harmonic orders p	
pos. seq. components	$p = 3 \cdot i + 1$	i = 0, 1, 2, 3
neg. seq. components	$p = 3 \cdot i - 1$	i = 1, 2, 3
zero seq. components	$p = 3 \cdot i$	i = 0, 1, 2, 3

table 7.7: harmonic orders of u_{phsum} and u_{phdiff} in case of a DC-side unbalance

Since both the harmonic orders and the related phase sequences are the same in the objective variables u_{phsum} and u_{phdiff} , table 7.7 can be summa-

rized to table 7.8, representing the harmonic orders to be expected in the measurable 3-level VSI output voltages u_{ph} .

u _{ph}	harmonic orders p	
pos. seq. components	$p = 3 \cdot i + 1$ $i = 0, 1, 2, 3 \dots$	
neg. seq. components	$p = 3 \cdot i - 1$ $i = 1, 2, 3 \dots$	
zero seq. components	$p = 3 \cdot i$ $i = 0, 1, 2, 3 \dots$	

table 7.8: harmonic orders of u_{ph} in case of a DC-side unbalance

Concerning the AC-side currents i_{phsum} , i_{phdiff} and i_{ph} , the same harmonic orders, except of the zero sequence components which do not find a path to flow, will arise as in the corresponding voltages u_{phsum} , u_{phdiff} and u_{ph} . This is manifested in table 7.9 and table 7.10.

i _{phsum}	harmonic orders p	
pos. seq. components	$p = 3 \cdot i + 1$	$i = 0, 1, 2, 3 \dots$
neg. seq. components	$p = 3 \cdot i - 1$	i = 1, 2, 3
i _{phdiff}	harmonic orders p	
pos. seq. components	$p = 3 \cdot i + 1$	$i = 0, 1, 2, 3 \dots$
neg. seq. components	$p = 3 \cdot i - 1$	i = 1, 2, 3

table 7.9: harmonic orders of i_{phsum} and i_{phdiff} in case of a DC-side unbalance

i _{ph}	harmonic orders p
pos. seq. components	$p = 3 \cdot i + 1$ $i = 0, 1, 2, 3 \dots$
neg. seq. components	$p = 3 \cdot i - 1$ $i = 1, 2, 3 \dots$

table 7.10: harmonic orders of i_{ph} in case of a DC-side unbalance

From table 7.8 and table 7.10 it is confirmed that in case of a DC-side unbalance, both the 3-level VSI output voltages u_{ph} and the AC-side currents i_{ph} will contribute with even numbered harmonics. Therefore it should be pointed out that not only the 3-level VSI itself, but also the

AC-system, to which the inverter is connected, will be stressed with highly undesirable even numbered harmonics.

7.3.3 Simulation results

In order to verify the results of the above presented analysis, a simulation with the MATLAB program introduced in chapter 6.2 was performed for the FFM modulated SVC-example described in table 6.1 of chapter 6.3.3.

Hereby, an artificial unbalance on the DC-side was generated by two different valued resistors in parallel to the two DC-side capacitors ($r_{c1}=100$ [p.u.], $r_{c2}=150$ [p.u.]), which yielded a steady-state DC-side unbalance of about $U_{Ddiff0}=-0.25$ [p.u.]. This value is quite large, however still in a realistic range which will be proved by the simulations in chapter 7.5.

The AC-side quantities s_{ph} and u_{Lph} will constitute symmetrical 3-phase systems. In addition, according to the recommendations in chapter 6.6.1, the total DC-side capacitance c_{tot} was chosen to $c_{tot} \approx 1.5$ [p.u.] or $\tau_{c_{tot}} \approx 4.32$ msec. All other parameters remained the same as given in chapter 6.3.

The simulation results are presented in figure 7.11 - figure 7.111. Though not all graphics of figure 7.11 - figure 7.1111 will be discussed in the following, the most interesting points shall all the same be mentioned here.

First of all, one can clearly see by the amplitude spectra in the right columns that the harmonic orders of the individual 3-level VSI quantities are in good agreement with those derived in the previous harmonic analysis.

Another important aspect concerns the even numbered harmonics arising in the AC-side currents i_{ph} . It is evident in the corresponding graphic figure 7.11 e) that these even numbered harmonics cause large peak-values for i_{ph} , which results, besides the increased voltage stress on the DC-side, also in an increased current stress for the inverter valves.

Further, it can be seen from the amplitude spectrum for i_{ph} , that the predominant 2nd harmonic takes on very large values of more than 0.1[p.u.]. These values are far beyond of those permitted to be injected into an ACsystem, especially since they belong to a class of harmonics, for which the harmonic requirements in an AC-system are particularly strict.

It is interesting, though not very astonishing, that the even numbered harmonics in i_{ph} are predominantly generated by i_{phdiff} , which is proportional to u_{Ddiff} (and with that to U_{Ddiff}). This is clearly manifested in the graphics



fig 7.1I: line diagram and amplitude spectra of u_{Lph} , s_{ph} , u_{ph} , u_{Zph} and i_{ph} for the FFM modulated SVC in the nominal capacitive operation mode in case of a steady-state DC-side unbalance U_{Ddiff0} =-0.25[p.u.], c_{tot} =1.5[p.u.] ($\tau_{c_{tot}}$ =4.32msec), other parameters according to table 6.1 in chapter 6.3.3



fig 7.1II: line diagram and amplitude spectra of u_{SP} , u_{phsum} , i_{phsum} , u_{phdiff} and i_{phdiff} for the FFM modulated SVC in the nominal capacitive mode in case of steady-state DC-side unbalance U_{Ddiff0} =-0.25[p.u.], c_{tot} =1.5[p.u.] (τ_{cot} =4.32msec), other parameters according to table 6.1 in chapter 6.3.3



fig 7.1III: line diagram and amplitude spectra of $i_{D1/D2}$, $u_{D1/D2}$, i_{Ddiff} , i_0 , u_{Dsum} and u_{Ddiff} for the FFM modulated SVC in the nominal capacitive mode in case of steady-state DC-side unbalance U_{Ddiff0} =-0.25[p.u.], c_{tot} =1.5[p.u.] ($\tau_{c_{tot}}$ =4.32msec), other parameters according to table 6.1 in chapter 6.3.3

c) and e) of table 7.1II. Also u_{Dsum} , which together with s_{ph} and u_{Lph} determines i_{phsum} , only shows up small amplitudes for the odd numbered multiples of three, which are introduced by the DC-side unbalance (graphics d) in figure 7.1III).

Finally it should be emphasized that the simulation results indicate that the 3-level VSI at least for the chosen capacitive operation mode shows up selfbalancing abilities. This is true since no extra balance control is implemented and despite this fact the DC-side unbalance is limited to a steadystate value of about U_{Ddiff} =-0.25[p.u.]. Actually one could have expected that for the given artificial unbalance source, the upper DC-side capacitor would be totally discharged in steady state. This is quite an interesting phenomenon, and therefore the following chapter will focus in a more general way on the self-balancing attributes of the 3-level VSI.

7.4 3-level VSI self-balancing analysis

Before focusing on additional control schemes to balance the DC-side voltages u_{D1} and u_{D2} , the question arises for the self-balancing attributes of the 3-level VSI. This means to seriously investigate whether the 3-level VSI has principally inherent abilities to counteract against a DC-side unbalance without any additional control scheme and if yes, to which amount. Only uncertain answers have been given so far without a theoretical background and mainly based on observations made on small scaled hardware models.

Also of importance is the question for the system parameters, which mainly determine this possible self-balancing behaviour. Therefore, it is highly desirable to perform a self-balancing analysis, which will be done in the following.

It should be mentioned that in [57] a self-balancing analysis for switching functions with a symmetry to a quarter of a period has been performed in the 3-phase plane, which however resulted in quite complicated expressions. Here, another more clear and simple approach in a d/q plane will be presented.

7.4.1 Qualitative 3-level VSI self-balancing analysis

a) Self-balancing transfer functions

In appendix E.3, the phasor transfer functions describing the 3-level VSI

self-balancing abilities in case of a DC-side unbalance are derived and are here for clearness reasons presented once again in table 7.11 and table 7.12.

Before calculated in the Laplace domain, these equations have been transformed from the 3-phase plane into a d/q plane, which rotates with an angular velocity $-2\omega_1$. This has been performed since the usually used d/q plane, rotating with an angular velocity ω_1 , is not suitable for studies concerning a DC-side unbalance and its control. For more detailed information on this, the reader is referred to appendix E.2.

In order to distinguish between the phasor components in the two different d/q frames (appendix C.2.1), the following notation will be used:

 $\underline{x} = \underline{x}''; \quad x_d = x_d'', \ x_q = x_q'', \quad \text{if the d/q frame rotates with an} \\ \underline{x} = x'; \quad x_d = x_d', \ x_q = x_q', \quad \text{if the d/q frame rotates with an} \\ angular \ velocity \ -2\omega_1; \\ \underline{x} = x'; \quad x_d = x_d', \ x_q = x_q', \quad \text{if the d/q frame rotates with an} \\ angular \ velocity \ \omega_1; \\ \end{array}$

The derivation of the equations in table 7.11 presumes that initially a steadystate DC-side unbalance $U_{Ddiff0} \neq 0$ exists, however the steady-state values of potential unbalance sources (chapter 7.5) are assumed to equal to 0. With that it is ensured, that exclusively the influence of the 3-level VSI topology itself on the DC-side unbalance will be taken into account.

This DC-side unbalance $U_{Ddiff0} \neq 0$, as proved in chapter 7.3.2, will cause a negative sequence 2nd harmonic to arise in the AC-side currents i_{ph} . With that and a d/q frame rotating with an angular velocity $-2\omega_1$, as chosen in eqn. (7.1), also steady-state DC-values I_{d0} " and I_{q0} " unequal to 0 will appear in the AC-side current phasor components i_d " and i_q ".

It is evident in eqn. (7.1) that $u_{Ddiff}(s)$, $i_d''(s)$ and $i_q''(s)$ are represented in dependancy on their initial values U_{Ddiff0} , I_{d0}'' and I_{a0}'' .

More, speaking of self-balancing, it is important to understand that also the pulse patterns must not be manipulated by means of an additional NP-control scheme. This implies that the switching functions s_{ph} have a symmetry to half or a quarter of a period and will not contribute with a negative sequence 2nd harmonic (table 7.1 in chapter 7.3.1). Therefore, in a d/q frame rotating with an angular velocity $-2\omega_1$, their phasor components S_{d0} " and S_{q0} " will equal to 0. This has furthermore been taken into account by the derivation of eqn. (7.1) in table 7.11.







table 7.12: Quantities in the 3-level VSI self-balancing transfer functions (table 7.11)

On the other hand, the squared switching functions s_{ph}^2 will show up a negative sequence 2nd harmonic, which was shown in table 7.2 of chapter 7.3.1. Hence, in a d/q frame rotating with an angular velocity $-2\omega_1$, their phasor components S_{d0}^2 and S_{q0}^2 will be unequal to 0, which has been considered in eqn. (7.1).

With that and supposing the 3-level VSI to have self-balancing abilities, the individual quantities $i_d''(s)$, $i_q''(s)$ and $u_{Ddiff}(s)$ are expected to approach to 0 for $t \to \infty$ in the time domain. This will be studied in the following subchapter.

b) Self-balancing studies by means of the finite value theorem of the Laplace transform

When having the intention to study the 3-level VSI's answer to a DC-side unbalance U_{Ddiff0} , applying the inverse Laplace transform to eqn. (7.1) might constitute the right choice.

Unfortunately, due to the complexity of the denumerator poles, it was found that this operation yields unreasonable complicated mathematical expressions, which also with the symbolic calculation tools of the simulation program MATLAB couldn't be simplified.

Therefore, in a next step, another powerful and simple theorem of the Laplace transform has been applied. This theorem is known as the 'final value theorem' of the Laplace transform ([58]) and can mathematically be expressed by eqn. (7.2):

$\lim (s \cdot F(s)) =$	$\lim f(t)$	(7.2)
$s \rightarrow 0$	$t \rightarrow \infty$	

With eqn. (7.2) it is now at least qualitatively possible to assess whether the 3-level VSI has self-balancing abilities or not.

Applying eqn. (7.2) to eqn. (7.1) $(F(s)=i_d"(s), i_q"(s), u_{Ddiff}(s))$, nearly at first sight results to eqn. (7.3):

$$\lim_{t \to \infty} i_d''(t) = 0; \quad \lim_{t \to \infty} i_q''(t) = 0; \quad \lim_{t \to \infty} u_{Ddiff}(t) = 0$$
(7.3)

Roughly spoken, eqn. (7.3) proves that after an infinite time t the initially apparent DC-side unbalance U_{Ddiff0} and the hereby caused AC-side current phasor components I_{d0} " and I_{q0} " (negative sequence 2nd harmonic in the 3-phase plane) will totally have disappeared.

With other words, it can be said that the 3-level VSI will inherently be capa-

ble to 'self-control' a DC-side unbalance to zero. The obvious driving force for this self-balancing must be seen in the initial AC-side current phasor components I_{d0} " and I_{q0} " itself, since all other sources have been neglected in this analysis.

These AC-side current phasor components I_{d0} " and I_{q0} " (negative sequence 2nd harmonic in the 3-phase plane) will be reflected back to the DC-side via the convolution with the phasor components S_{d0}^2 " and S_{q0}^2 " of the squared switching functions s_{ph}^2 according to

$$\frac{d}{dt}u_{Ddiff} = -\frac{1}{c} \cdot i_0 = \frac{3}{2c} [S^2{}_{d0}" \cdot i_d" + S^2{}_{q0}" \cdot i_q"].$$

This convolution will result in a balancing DC-component in the NP-current i_0 .

Hence it can be summarized, that a DC-side unbalance U_{Ddiff0} causes a negative sequence 2nd AC-side current harmonic to arise in the 3-phase plane, which in its turn counteracts to its driving force, the DC-side unbalance. From this point of view, the 3-level VSI self-balancing actually can be compared to the self-induction law of a coil (rule of Lenz).

More, it has to be emphasized that eqn. (7.3) will prove right for all switching functions (with a symmetry to at least a half or a quarter of a period) and all 3-level VSI operation modes.

This is true since the phasor steady-state values S_{d0}^2 and S_{q0}^2 , which constitute the only quantities in eqn. (7.1) corresponding to a specific pulse pattern and a specific 3-level VSI operation mode, will have no influence on the result (eqn. (7.3)) of the operation eqn. (7.2).

c) Self-balancing studies with simplified transfer functions (r=0)

The previous sub-chapter provided very important qualitative statements concerning the self-balancing attributes of the 3-level VSI topology. However, no quantitative results could be achieved due to the complexity of the corresponding transfer functions.

Therefore, another very common approach for an approximated solution of eqn. (7.1) will be applied here, which consists in a simplification of the complicate transfer functions.

Hereby, in a high power system, the usually very small ohmic part r will be neglected, resulting in simplified transfer functions, which then can more

easily be transformed back into the time domain.

Neglecting the ohmic part r of the system, eqn. (7.1) results to eqn. (7.4), or, transformed back into the time domain, to eqn. (7.5).

$$i_{d}"(s) = \frac{I_{d0}"}{s}; \ i_{q}"(s) = \frac{I_{q0}"}{s}; \ u_{Ddiff}(s) = \frac{U_{Ddiff0}}{s} \quad \text{for } r=0 \quad (7.4)$$

$$i_{d}"(t) = I_{d0}"; \ i_{q}"(t) = I_{q0}"; \ u_{Ddiff}(t) = U_{Ddiff0} \quad \text{for } r=0 \quad (7.5)$$

It is obvious and quite astonishing that the results manifested in eqn. (7.3) and eqn. (7.5) are totally different.

While eqn. (7.3) clearly underlines that an initial DC-side unbalance U_{Ddiff0} and the hereby caused AC-side current phasor components I_{d0} " and I_{q0} " will be 'self-controlled' to 0 (for $r \neq 0$), they will in opposite to that remain at their initial values, if the ohmic system part is neglected (r=0).

Hence, it can be concluded that in case of no ohmic system part (r=0), the 3-level VSI will not show up any self-balancing abilities at all! A DC-side unbalance will, presuming no additional balance control, not experience any changes.

Also here it has to be pointed out, that this will prove right for all operation modes and switching functions (with a symmetry to at least half or a quarter of a period), which also becomes evident when evaluating eqn. (7.1) for r=0.

Up to now, the question for the 3-level VSI self-balancing attributes could only qualitatively be answered, which on the other side all the same yielded very interesting results. A more quantitative analysis however, also showing the analytical dependencies on specific system parameters, failed.

This was due to the fact that the general self-balancing transfer functions $(r \neq 0)$ yield unreasonable complicated time domain expressions and their simplification (r=0) coincides with the exceptional special case of no self-balancing at all.

Another solution or better, approximation, which finally will result in a useful quantitative description of the self-balancing phenomenon, will be presented in the chapter to come.

7.4.2 Quantitative 3-level VSI self-balancing analysis

a) System order reduction

Generally, the main reason for the complexity of transfer functions in the Laplace domain is manifested by the fact that these equations do not exclusively describe steady-state operation (as the well known complex analysis) but also take into account the system's transient response. Especially in systems with voltage source inverters (both 2- and 3-level VSIs), the transient responses usually consist of at least two terms in the time domain, which are briefly characterized in the following.

The first term is free of oscillations and describes the variation in time of the variable under investigation as response to e.g. a load step. In most cases, these variations in time result in a linear function in time or an exponential function, which also includes the steady-state values.

The second term is superimposed to the first one and is characterized by an exponentially more or less well damped oscillation, depending on the size of the ohmic part r. This oscillation either corresponds to a DC-component in the 3-phase quantities on the AC-side $(c \rightarrow \infty)$ or to an interharmonic oscillation $(c \neq \infty)$. Due to its decaying character it will however not contribute to the steady-state values. For more detailed informations with respect to this undesirable phenomenon, the reader is referred to [59] - [62].

Concerning the self-balancing analysis as performed in this chapter, those transient dynamics, which are determined by the above described second term, truly are not of highest interest and will therefore be neglected in the following. This simply means to reduce the order of the system, which in its turn yields less complicated transfer functions.

b) Analysis

The way to perform the just mentioned system order reduction can be described as follows.

In a first step, basing on the corresponding steady-state equations (eqn. (D.16), appendix D.2.2), linear expressions for the AC-side current phasor components $i_d''(s)$ and $i_q''(s)$ in dependancy on the DC-side unbalance $u_{Ddiff}(s)$ are derived. These expressions will then be inserted in the state-space equation for $u_{Ddiff}(s)$ and the result will finally be solved for $u_{Ddiff}(s)$ and transformed into the time domain.

A similar analysis for the AC-side current phasor components $i_d''(s)$ and $i_q''(s)$ will not be performed, since they depend on $u_{Ddiff}(s)$ and the same dynamics have to be expected for them as for $u_{Ddiff}(s)$.

As mentioned above, the basis for the studies to come is constituted by the general steady-state equations, given in appendix D.2.2, eqn. (D.16). Together with the general assumptions made in chapter 7.4.1a), these steadystate equations result to eqn. (7.6).

$$\begin{bmatrix} 0\\0\\0\\0 \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & -2\omega_{1} & \frac{S^{2}_{d0}}{2l}\\ 2\omega_{1} & -\frac{r}{l} & \frac{S^{2}_{q0}}{2l}\\ \frac{3}{2}\frac{S^{2}_{d0}}{c} & \frac{3}{2}\frac{S^{2}_{q0}}{c} & 0 \end{bmatrix} \cdot \begin{bmatrix} I_{d0}\\ I_{q0}\\ U_{Ddiff0} \end{bmatrix}$$
(7.6)

Solving the upper two equations for the two steady-state values I_{d0} " and I_{a0} " in dependancy on U_{Ddiff0} yields eqn. (7.7) and eqn. (7.8).

$$I_{d0}'' = -\frac{rS^2_{d0}'' - 2\omega_1 IS^2_{q0}''}{2(r^2 + 4\omega_1^2 I^2)} \cdot U_{Ddiff0}$$
(7.7)

and

$$I_{q0}'' = -\frac{rS_{q0}'' + 2\omega_1 lS_{d0}''}{2(r^2 + 4\omega_1^2 l^2)} \cdot U_{Ddiff0}.$$
(7.8)

Now, in a next step, the DC-side unbalance U_{Ddiff0} is supposed to slowly vary in time.

Further, neglecting any transient oscillations (subchapter a)) and assuming the AC-side time constant l/r smaller than the variation in time of U_{Ddiff0} , eqn. (7.7) and eqn. (7.8) can be transformed into the Laplace domain according to eqn. (7.9) and eqn. (7.10).

$$i_d(s) \approx -\frac{rS^2_{d0} - 2\omega_1 lS^2_{q0}}{2(r^2 + 4\omega_1^2 l^2)} \cdot u_{Ddiff}(s)$$
(7.9)

$$i_q(s) \approx -\frac{rS^2_{q0} + 2\omega_1 lS^2_{d0}}{2(r^2 + 4\omega_1^2 l^2)} \cdot u_{Ddiff}(s).$$
(7.10)

It should be anticipated here that the validity of these assumptions will be confirmed in the simulation results presented in chapter 7.4.6.

These equations eqn. (7.9) and eqn. (7.10) manifest the before mentioned linear expressions for the AC-side current phasor components $i_d''(s)$ and $i_q''(s)$ in dependancy on the DC-side unbalance $u_{Ddiff}(s)$.

Proceeding with the analysis, the state-space equation for $u_{Ddiff}(s)$, which was derived in eqn. (E.37) of appendix E.3.2 has to be recalled in mind and is here presented once again in eqn. (7.11).

$$s \cdot u_{Ddiff}(s) = \frac{3}{2c} [S_{d0}^2 \cdot i_d''(s) + S_{q0}^2 \cdot i_q''(s)] + U_{Ddiff0}$$
(7.11)

Inserting eqn. (7.9) and eqn. (7.10) in eqn. (7.11) and solving for $u_{Ddiff}(s)$ yields the desirable simple transfer function eqn. (7.12), which is very well suited for the quantitative investigations of the 3-level VSI self-balancing attributes.

$$u_{Ddiff}(s) \approx \frac{1}{s + \frac{3r[(S^2_{d0}")^2 + (S^2_{q0}")^2]}{4c(r^2 + 4\omega_1^2 l^2)}} \cdot U_{Ddiff0}$$
(7.12)

Finally, the inverse Laplace transform of eqn. (7.12) will no longer constitute a problem and therefore, $u_{Ddiff}(s)$ can be written in the time domain according to eqn. (7.13).

$$u_{Ddiff}(t) \approx U_{Ddiff0} \cdot e^{-\frac{t}{\tau_{bal}}} \quad \text{with} \quad \tau_{bal} = \frac{4c(r^2 + 4\omega_1^2 l^2)}{3r[(S^2_{d0}")^2 + (S^2_{q0}")^2]} \quad (7.13)$$

$$\tau_{bal} \colon \text{self-balancing time constant}$$

It should be mentioned that due to their assumed linear dependancy on $u_{Ddiff}(t)$, also the variations in time for $i_d''(t)$ and $i_q''(t)$ will now be determined via eqn. (7.9) and eqn. (7.10).

With that, the quantitative self-balancing analysis is performed and the achieved results will now be discussed in the following chapter.

7.4.3 Discussion

First of all, as the most important fact, it should again be stated, that the 3-

level VSI in the presence of an ohmic system part $r \neq 0$ will always show up self-balancing abilities.

This is true since the self-balancing time constant τ_{bal} in eqn. (7.13) will always take on a positive value and hence the exponential function will always decay to 0 for $t \to \infty$.

In the following sub-chapters, the quantitative influences of the individual parameters r, l, $(S_{d0}^2)^2 + (S_{a0}^2)^2$ and c will be discussed and explained.

a) Influence of the system parameters r and l

Assuming the ohmic part r of the system being very small compared to the inductive part l, which is true for almost all high power applications, it can be concluded from eqn. (7.13) that the self-balancing time constant is inversely proportional to r and proportional to the squared value of l.

These dependencies can be better understood with the help of a simple graphical model, which is presented in figure 7.2.



fig 7.2: Graphical model for the assessment of the influence of the ohmic and inductive system part r and l on the 3-level VSI self-balancing abilities

In case of a DC-side unbalance $U_{Ddiff0} \neq 0$, the objective 3-level VSI output voltage term u_{phdiff} , which is well known to be defined to

$$u_{phdiff} \,=\, \frac{U_{Ddiff0}}{2} \cdot s_{ph}^2 \,=\, \frac{U_{Ddiff0}}{2} \cdot \left|s_{ph}\right|, \label{eq:updiff}$$

will take on a shape as presented for phase *a* in figure 7.2. Hereby, the DCside unbalance U_{Ddiff0} was arbitrarily assumed to equal to $U_{Ddiff0}=0.25$ and all harmonics in u_{phdiff} will be neglected.

It is evident in figure 7.2 that the fundamental component of u_{adiff} will be a 2nd harmonic (represented in figure 7.2 by the dotted line). The negative phase sequence of this 2nd harmonic is meanwhile well known and will be presumed here, though not obvious in figure 7.2.

Further, the large DC-component in u_{adiff} constitutes a 0 sequence system and hence will not contribute to the currents on the AC-side.

As mentioned yet before, u_{adiff} will cause a negative sequence 2nd AC-side current harmonic to arise in i_{adiff} , whose amplitude and phase-displacement with regard to the fundamental of u_{adiff} will exclusively be determined by r and l. This proves right since no counter-voltage of this frequency will be present in the system. In figure 7.2 this is exemplified for a large value r=0.1[p.u.] and l=0.2[p.u.].

Simultaneously, this 2nd harmonic in i_{adiff} will be reflected back to the DCside via s_a^2 or $|s_a|$, where it will generate the NP-current i_0 as indicated by the thick line in figure 7.2. It can clearly be seen by the filled current-time area of i_0 that the NP-current shows up a DC-component.

Now, it is also evident from figure 7.2 that the magnitude of this NP-current DC-component, which is known to be the driving self-balancing force, strongly depends on the phase-displacement between s_a^2 or $|s_a|$ and the 2nd AC-side current harmonic.

Assuming r=0 (fundamental of i_{adiff} is lagging by $\pi/2$ with respect to the fundamental of u_{adiff}), it is quite easy to see in figure 7.2 that the resulting DC-component in i_0 will equal to zero, which simply means that no self-balancing will occur (chapter 7.4.1c)).

For any ohmic part $r \neq 0$ however, the phase-displacement of the fundamental of i_{adiff} (the negative sequence 2nd current harmonic) with respect to s_a^2 or $|s_a|$, will become smaller than $\pi/2$ and a DC-component in i_0 will be the result.

Since r in practical applications is usually very small compared to l, this DC-component in i_0 also has to be expected to be quite small, which would yield large self-balancing time constants τ_{bal} .

Further, for these conditions ($r \ll \omega_1 l$), the arising DC-component in i_0 will

be approximately linear to r. This can be verified in figure 7.2 when virtually shifting i_{adiff} by small phase-displacements around the pure inductive phase-displacement of $\pi/2$.

With that, the linear dependancy of the self-balancing time constant τ_{bal} on the ohmic system part r will be discussed sufficiently, which will now also be done for the inductive system part l.

An increase of the inductive part l will have a double influence on the arising 2nd current harmonic.

First of all, linearly to the increase of l, the 2nd AC-side current harmonic amplitude will for $r \ll \omega_1 l$ roughly linearly decrease, which also yields the same linear decrease for the self-balancing DC-component in i_0 .

In addition to that, while presuming a constant ohmic part r, the phase-displacement of the 2nd AC-side current harmonic with respect to the NP-angles will for an increasing inductive part l inherently shift towards the pure inductive mode. Hence, the self-balancing DC-component in i_0 will once more be reduced.

Since both effects are approximately inversely proportional to l, the resulting dependancy on l will be inversely proportional to l^2 .

With that also the influence of l on the 3-level VSI self-balancing attributes hopefully has become more transparent.

Finally, another general valid 3-level VSI self-balancing dependancy, namely those on the 3-level VSI operation mode, can clearly be derived with the help of figure 7.2.

Assuming constant system parameters r and l, the resulting NP-current will not loose its DC-component, if the switching functions are phase-shifted or if the NP-angles (the modulation index m) will be varied in order to set up another operation mode. The validity of this statement will be explained in the following.

Since the relative phase-displacement of the fundamentals of u_{adiff} and i_{adiff} is exclusively determined by the impedance r and l, the filled NP-current segments in figure 7.2 will remain the same, if the switching functions are phase displaced. With other words, i_{adiff} is coupled to s_{ph}^2 or $|s_a|$ and the self-balancing DC-component in i_0 will not change its value when exclusively a phase-displacement is applied to s_{ph} .

On the other hand, by virtually varying the NP-angles (modulation indices

m) in figure 7.2, it is evident that the DC-component of i_0 will change, however still a value unequal to 0 will be result.

This graphically shows the qualitative independence of the self-balancing attributes on a specific 3-level VSI operation mode.

Last but not least a special case should shortly be discussed. As can be clearly seen in eqn. (7.13), no self-balancing occurs, if no ohmic part r will be present in the system.

Though this is physically not realistic, the ohmic part r in a high power system usually takes on very small values. Therefore, large time constants τ_{bal} will have to be expected, which quantitatively will be verified in chapter 7.4.6.

In contrary, in small scaled hardware models, the ohmic part r normally is quite large and due to this, a good self-balancing behaviour of the 3-level VSI can be observed with no or almost no need for an additional NP-controller.

b) Influence of the 2nd harmonic of the squared switching functions

With respect to a d/q plane rotating with an angular velocity $-2\omega_1$, the expression $(S^2_{d0}")^2 + (S^2_{q0}")^2$ in eqn. (7.13) represents the squared amplitude value of the fundamental of s^2_{ph} , which is known to be a negative sequence 2nd harmonic (table 7.2 in chapter 7.3.1). As can be seen in eqn. (7.13), the time constant τ_{bal} will be inversely proportional to these squared amplitude. To get a better understanding of this dependancy, the harmonic analysis performed in chapter 7.3 and the harmonic transfer rules derived in chapter 4.3 will be of great help.

The harmonic analysis in chapter 7.3 indicated the self-balancing attributes of the 3-level VSI. It could be seen in table 7.5 of chapter 7.3.1 that in case of a DC-side unbalance U_{Ddiff0} , i_0 shows up a DC-component, which for sure must either have an increasing or a decreasing effect on U_{Ddiff0} .

According to the NP-current equation

$$i_0 = -\sum_{ph = a,b,c} i_{ph} \cdot s_{ph}^2 = -\sum_{ph = a,b,c} i_{ph} \cdot \left| s_{ph} \right|,$$

this DC-component in i_0 will in case of $U_{Ddiff0} \neq 0$ predominantly be generated by the convolution of the negative sequence 2nd harmonics of i_{ph} and s_{ph}^2 or $|s_{ph}|$ respectively. The negative sequence 2nd harmonic of i_{ph} in

its turn is caused by the convolution of again s_{ph}^2 or $|s_{ph}|$ with U_{Ddiff0} $(u_{phdiff} = s_{ph}^2 \cdot U_{Ddiff0} = |s_{ph}| \cdot U_{Ddiff0}).$

Hence, the magnitude of the arising DC-component in i_0 in case of $U_{Ddiff0} \neq 0$ will be proportional to the squared amplitude of the 2nd harmonic of s_{ph}^2 or $|s_{ph}|$ and in addition to the DC-side unbalance U_{Ddiff0} itself.

Further, as it was clearly shown in the previous analysis, this DC-component in i_0 will always have the appropriate sign to counteract to an existing DC-side unbalance U_{Ddiff0} .

From that it is now evident that the self-balancing time constant τ_{bal} in eqn. (7.13), will be inversely proportional to the squared amplitude of the negative sequence 2nd harmonic of s_{ph}^2 or $|s_{ph}|$.

More, it can be expected that the numeric values of the negative sequence 2nd harmonic amplitude of s_{ph}^2 or $|s_{ph}|$ does not vary in a wide range for different modulation schemes and switching frequencies. This is due to the fact, that this amplitude will predominantly be determined by the convolution of the fundamental component of the chosen switching functions s_{ph} with itself, which normally takes on large values, especially in transmission applications.

c) Influence of the capacitor size

Last but not least, the influence of the capacitor size c will also shortly be discussed.

According to eqn. (7.13), the self-balancing time constant τ_{bal} shows up a simple linear dependancy on the capacitor size c. Also this result is in very good agreement with what would have been expected from a logical point of view, which further strengthens the trust in the validity of eqn. (7.13).

7.4.4 Influence of the higher ordered even numbered harmonics of the AC-side currents

The performed self-balancing analysis only has taken into account the selfbalancing contribution of the negative sequence 2nd harmonics of i_{ph} . This proves right since in a d/q frame rotating with an angular velocity $-2\omega_1$ only this component will show up steady-state DC-values I_{d0} " and I_{q0} " unequal to 0.

For sure, also the higher ordered even numbered harmonics according to
table 7.2 and table 7.3 in chapter 7.3.1 will yield appropriate signed DC-components to arise in i_0 , which will support the 3-level VSI DC-side self-balancing effect.

This could be shown by performing the same analysis as presented in chapter 7.4.2b), however now choosing a d/q frame rotating with e.g. $4\omega_1$, $-8\omega_1$ or $10\omega_1$, which corresponds to the harmonic orders of interest. Then, nearly the same results as in eqn. (7.13) for $-2\omega_1$ would be achieved except of larger multiplication factors (16, 64, 100) for ω_1^2 , which indicate remarkably larger time constants τ_{hal} .

In addition, appropriate values for the phasor components S^2_{d0} " and S^2_{q0} " of s^2_{ph} or $|s_{ph}|$ must be inserted, which no longer coincide with the fundamental component of s^2_{ph} (negative sequence 2nd harmonic), but with the 4th, 8th, or 10th etc.. These higher ordered harmonics of s^2_{ph} or $|s_{ph}|$ in its turn can usually be expected to contribute with smaller values than its fundamental component.

Hence, it can be expected that the influence of the higher ordered even numbered harmonics on the DC-side self-balancing behaviour will be small.

7.4.5 Influence of the total DC-side voltage harmonics

a) General considerations

In the investigations up to now, the influence of the harmonics in the total DC-side voltage u_{Dsum} on the 3-level VSI self-balancing abilities has not been taken into account.

This was due to the fact that in the here chosen d/q frame (rotating with an angular frequency $-2\omega_1$), the equation for the total DC-side voltage u_{Dsum} is totally decoupled from the other 3 system equations, as clearly shown in eqn. (E.34) of appendix E.3.1.

However, it was shown in the harmonic analysis in chapter 7.3.1 (table 7.6), that in case of a DC-side unbalance, the harmonic orders in u_{Dsum} will change. In addition to all even numbered multiples of six, all odd numbered multiples of 3 will also be present.

These odd numbered multiples of 3 will be generated by the convolution of the switching functions s_{ph} with the even numbered AC-side current harmonics, which in its turn are the result of the DC-side unbalance itself.

For sure, also these harmonics of u_{Dsum} , being odd numbered multiples of

three, will be reflected back to the AC-side $(u_{phsum}$ in table 7.7 of chapter 7.3.2), where they will be the driving force for even numbered AC-side current harmonics $(i_{phsum}$ in table 7.9 of chapter 7.3.2).

Hence, it should not be excluded that these harmonics will have an influence on the 3-level VSI self-balancing attributes, which will be investigated in the following.

b) Mathematical analysis

In a first step, the steady-state influence of the AC-side current phasor components I_{d0} " and I_{q0} " (caused by a DC-side unbalance U_{Ddiff0}) on the total DC-side voltage u_{Dsum} will mathematically be described. For that purpose, the state-space equation for u_{Dsum} will be recalled in mind, which, according to eqn. (D.14) in appendix D.2.1 can be written to eqn. (7.14).

$$\frac{d}{dt}u_{Dsum} = \frac{3}{2c}[S_{d0}' \cdot i_{d}' + S_{q0}' \cdot i_{q}']$$
(7.14)

Herein, the switching function phasor components s_d' and s_q' are assumed to be constant and therefore are represented by their steady-state values S_{d0}' and S_{q0}' . Further, the DC-side source/sink current i_D is set to zero, since it will not have an influence on the investigation to come.

By means of complex phasors, eqn. (7.14) can be expressed by

$$\frac{d}{dt}u_{Dsum} = \frac{3}{2c} \operatorname{real}\{\underline{S}_{0}^{'*} \cdot \underline{i}'\}$$
(7.15)

with

$$\underline{S}_{0}^{*} = S_{d0}^{'} - j \cdot S_{q0}^{'}$$
 and $i' = i_{d}^{'} + j \cdot i_{q}^{'}$ (7.16)

It has to be noted, that eqn. (7.14) - eqn. (7.16) are valid in a d/q-frame rotating with an angular velocity ω_1 . Only in this frame, the phasor components S_{d0}' and S_{q0}' of the switching function's fundamental will take on values unequal to zero.

Hence, before inserted in one of these two equations, the current phasor components I_{d0} " and I_{q0} " calculated in a d/q frame rotating with an angular velocity $-2\omega_1$ have to be transformed in a d/q frame rotating with an angular velocity ω_1 . Mathematically, this can be described by eqn. (7.17).

$$i' = I_0'' \cdot e^{-j3\omega_1 t}; \qquad I_0'' = I_{d0}'' + j \cdot I_{q0}''$$
 (7.17)

with

i: current phasor in a d/q frame rotating with an angular velocity ω_1

 I_0 ": current phasor in a d/q frame rotating with an angular velocity $-2\omega_1$

Inserting eqn. (7.17) in eqn. (7.15) and solving for u_{Dsum} yields eqn. (7.18).

$$u_{Dsum} = \frac{3}{2c} \cdot \int \operatorname{real} \{ \underline{S}_0^{'*} \cdot \underline{I}_0^{''} \cdot e^{-j3\omega_1 t} \} dt$$
(7.18)

Calculating the integral of the real part of $\underline{S}_0^{'*} \cdot \underline{I}_0^{''} \cdot e^{-j3\omega_1 t}$ (real (z)=1/2(z + z*), [52]) results to eqn. (7.19).

$$u_{Dsum} = j \frac{1}{4\omega_1 c} (\underline{S}_0'^* \cdot \underline{I}_0'' \cdot e^{-j3\omega_1 t} - \underline{S}_0' \cdot \underline{I}_0''^* \cdot e^{j3\omega_1 t})$$
(7.19)

Reflected back to the AC-side, u_{Dsum} will be the driving force for a current phasor i_{aux} , which in steady-state is determined to eqn. (7.20).

$$i_{aux'} = -\frac{\underline{S}_0'}{2} \cdot j \frac{1}{4\omega_1 c} \left(\frac{\underline{S}_0'^* \cdot \underline{I}_0'' \cdot e^{-j3\omega_1 t}}{r - j \cdot 2\omega_1 l} - \frac{\underline{S}_0' \cdot \underline{I}_0''^* \cdot e^{j3\omega_1 t}}{r + j \cdot 4\omega_1 l} \right)$$
(7.20)

Now, eqn. (7.20) will be transformed back in a d/q frame rotating with an angular velocity $-2\omega_1$, which, according to

$$i_{aux}$$
" = i_{aux} ' $\cdot e^{j3\omega_1 t}$

yields the current phasor i_{aux} " in eqn. (7.21).

$$i_{aux}'' = -\frac{\underline{S}_{0}'}{2} \cdot j \frac{1}{4\omega_{1}c} \left(\frac{\underline{S}_{0}'^{*} \cdot \underline{I}_{0}''}{r - j \cdot 2\omega_{1}l} - \frac{\underline{S}_{0}' \cdot \underline{I}_{0}''^{*} \cdot e^{j\delta\omega_{1}l}}{r + j \cdot 4\omega_{1}l} \right)$$
(7.21)

In eqn. (7.21), the first term in the brackets (DC-term) corresponds to a negative sequence 2nd harmonic, while the second term (oscillating with $e^{j6\omega_1 t}$) represents a positive sequence fourth harmonic in the 3-phase plane.

Here, only the DC-term (negative sequence 2nd harmonic) of eqn. (7.21) will be of interest for further studies and therefore the oscillating term will be neglected from now on. With that, i_{aux} " can be rewritten in the form of eqn. (7.22).

$$i_{aux''} = \frac{\sum_{0} \sum_{0}^{j} (2\omega_{1}l - j \cdot r)}{8\omega_{1}c(r^{2} + 4\omega_{1}^{2}l^{2})} I_{0}^{"}$$
(7.22)

Separating the real and the imaginary part and replacing $\underline{S}_0'S_0'^*$ by $(S_{d0}')^2 + (S_{e0}')^2$ finally results to eqn. (7.23).

$$i_{aux}" = \frac{\omega_1 l((S_{d0}')^2 + (S_{q0}')^2)}{4\omega_1 c(r^2 + 4\omega_1^2 l^2)} I_0" - j \cdot \frac{r((S_{d0}')^2 + (S_{q0}')^2)}{8\omega_1 c(r^2 + 4\omega_1^2 l^2)} I_0" \quad (7.23)$$

c) Discussion

With the help of eqn. (7.23), it can now be shown that this current phasor i_{aux} ", which originally is caused by the self-balancing current phasor $I_0^{"} = I_{d0}^{"} + jI_{q0}^{"}$, in addition contributes to the 3-level VSI self-balancing abilities.

Simply neglecting the imaginary term in eqn. (7.23), which for $r \ll \omega_1 l$ will not introduce a major fault, it is evident that i_{aux} " will be in phase with I_0 ", which means that the resulting negative sequence 2nd harmonic and with that the balancing DC-component in the NP-current i_0 will increase. However, for realistic system parameters $(l=0.2[p.u.], c=3[p.u], (S_{d0}')^2 + (S_{q0}')^2 = 1.4)$, the additional self-balancing component i_{aux} " will take on moderate values $(i_{aux}" = 0.14 \cdot I_0")$.

This supporting influence could also be observed in simulations performed with different capacitor sizes. Hereby, the same simulation as presented in chapter 7.3.3 with the same DC-side unbalance source (unequal resistors in parallel to the DC-side capacitors) have been carried out for c_{tot} =0.5[p.u.] ($\tau_{c_{tot}}$ =1.44msec), c_{tot} =1.5[p.u.] ($\tau_{c_{tot}}$ =4.32msec) and c_{tot} =2.5[p.u.] ($\tau_{c_{tot}}$ =7.2msec).

The validity of the statements made in this chapter were manifested in steady-state DC-unbalancies U_{Ddiff0} , which decreased with decreasing capacitor values. For c_{tot} =0.5[p.u.] ($\tau_{c_{tot}}$ =1.44msec) U_{Ddiff0} resulted to U_{Ddiff0} =0.15[p.u.], for c_{tot} =1.5[p.u.] ($\tau_{c_{tot}}$ =4.32msec) U_{Ddiff0} equals U_{Ddiff0} =0.25[p.u.] (as presented in chapter 7.3.3) and finally for c_{tot} =2.5[p.u.] ($\tau_{c_{tot}}$ =7.2msec) U_{Ddiff0} =0.27[p.u.] was achieved as the steady-state DC-unbalance.

7.4.6 Simulation results

This chapter presents some simulation results with SABER, which will

prove the validity of the mathematical self-balancing analysis carried out in the previous chapters.

Again, the FFM modulated 3-level VSI SVC with the same parameters as in chapter 7.3.3 is chosen as a representative example to confirm the theoretical investigations.

However now, the two DC-side capacitors are initially charged to different DC-voltages, which yields a DC-side unbalance U_{Ddiff0} at t=0 of

$$U_{Ddiff0} = 0.1 \text{ [p.u.]}.$$

In addition, it is assumed that the SVC will work in the pure capacitive operation mode during the whole simulation $(i_q'=I_{q0}'=1[p.u.])$.

Further, in order to exclusively take into account the self-balancing contribution of the 3-level VSI itself, the controlled variable i_q' was filtered with a comb filter, which is tuned to all harmonics being odd numbered multiples of 3.

This has to be done, since these odd numbered multiples of 3, which in the 3-phase plane correspond to the even numbered AC-side current harmonics caused by the DC-unbalance, will be present in i_q' and will then via the control variable ϕ_u also cause undesirable modifications in the switching functions.

These undesirable modifications in the switching functions will yield a DCcomponent to arise in the NP-current i_0 , which in the whole inductive and up to about 0.7[p.u.] in the capacitive operation mode supports the self-balancing while it counteracts to it between 0.7[p.u.] and 1[p.u.] in the capacitive operation mode. This effect will be explained more in depth in chapter 8. Since this is a control specific influence, it will not be of interest here and would only falsify the results. Therefore, it has been eliminated by appropriate filtering of i_q' . This has been done for all simulations in chapter 7.

Now, before focusing on the simulation results, the self-balancing time constant τ_{bal} according to eqn. (7.13) will be calculated. For the given system parameters

$$r = 0.005$$
 [p.u.], $l = 0.2$ [p.u.], $c = 3$ [p.u]

and

$$(S_{d0}^2)^2 + (S_{q0}^2)^2 = 0.14,$$

the latter of which resulted from a FFT of the chosen FFM switching functions ($\beta = \pi/10$), the self-balancing time constant τ_{bal} is given to

$$\tau_{bal} \approx 2.9 \text{ sec.}$$

As it was shown in chapter 7.4.5b), also those harmonics in the total DCside voltage u_{Dsum} , which are caused by the DC-side unbalance U_{Ddiff0} , will positively contribute to the self-balancing effect by also generating a self-balancing negative sequence 2nd harmonic.

For the parameters given here, this additional current phasor component i_{aux} " can be calculated to i_{aux} " = 0.153 $\cdot I_0$ ", which roughly will decrease the self-balancing time constant to about 15%, which yields

$$\tau_{bal} \approx 2.45$$
 sec.

This time constant is quite large (about 120 AC-system cycles), and even if the self-balancing contributions of the entirety of all remaining even numbered AC-side current harmonics might yield a further small decrease of this value, still a really large value has to be expected.

This calculated value for τ_{bal} will now be compared with the simulation result, which is presented in figure 7.3, graphic a).

Herein the response of u_{Ddiff} to its initial DC-side unbalance U_{Ddiff0} is shown. In addition, for clearness reasons, u_{Ddiff} is filtered by means of a 2nd order notch filter (150Hz, quality factor 0.56) in order to get rid of the inherent 3rd harmonic oscillation (chapter 5).

The variation in time of u_{Ddiff} can clearly be identified to coincide with those of an exponential function, which is in very good agreement with eqn. (7.13).

Also the time constant τ_{bal} , which in the simulation can be estimated to about 2.3 sec. is also in quite good agreement with the calculated value. The fact, that the time constant τ_{bal} achieved by the simulation is smaller than the calculated one, confirms the small, but positive influence of the entirety of all remaining even numbered AC-side current harmonics.

To proceed further, the two simulations in the graphics b) and c) of figure 7.3 are focusing on the dependency of the ohmic and the inductive system part r and l on the 3-level VSI self-balancing attributes.

In graphic b), the resistive part r has been doubled to r=0.01 [p.u.] and the inductive part l has remained the same (l=0.2 [p.u.]), while in graphic c)



fig 7.3: self-balancing behaviour of the 3-level VSI FFM modulated SVC example as response to an initial DC-side unbalance U_{Ddiff0} for different system parameters

the ohmic part remains at its initial value (r=0.005 [p.u.]) and the inductive part is chosen to $l=0.2/\sqrt{2}$ [p.u.].

According to eqn. (7.13), in both cases the time constant τ_{bal} will shrink to half of its value. By comparing graphic a) with graphic b) and c), it can be concluded that the simulations are in good agreement with the theory.

Finally, also the theoretical special case r=0 has been investigated. The achieved results in figure 7.3, graphic d) must not be further discussed, since they totally confirm the expectations.

With that, the 3-level VSI self-balancing attributes are sufficiently investigated and the time has come to have a closer look at both the most common and the most serious DC-side unbalance sources, which will constitute the topic of the next chapter.

7.5 DC-side unbalance sources and their impact

It was mentioned yet in chapter 7.2 that various sources exist, which are responsible for a 3-level VSI DC-side unbalance. For practical applications it will be of highest interest to get a feeling for the quantitative impact of these individual unbalance sources. Hereby the knowledge of realistic values for both the arising unbalance magnitude and the corresponding dynamics is very desirable. The achieved results might then also show up the most critical DC-side unbalance sources.

In addition the studies will be of great help to answer the questions, whether an additional balance controller will be necessary or not, and, if yes, which dynamic requirements have to be fulfilled by this controller.

Therefore this chapter will focus more in depth on these aspects with respect to the particular DC-side unbalance sources introduced in chapter 7.2. Again, this will be exemplified on the 3-level VSI SVC with a total DC-side capacitance $c_{tot}=1.5$ [p.u.] or $\tau_{c_{tot}}=4.32$ msec and otherwise the same parameters as given in chapter 6.3. Further, no additional DC-side balancing controller is implemented.

7.5.1 DC-side unbalance transfer functions

A good insight in possible DC-side unbalance sources can be achieved by having a closer look at the transfer functions for the DC-side voltage u_{Ddiff} in dependancy on the control and the disturbance variables. These transfer

functions are derived in appendix E.2 (table E.9) and are here once more presented in table 7.13. The herein appearing quantities are in addition summarized in table 7.14.

Hereby it should be recalled in mind that these transfer functions for $u_{Ddiff}(s)$ is valid in a d/q frame, which rotates with an angular velocity $-2\omega_1$.

Therefore, it has to be emphasized that DC-load-steps in the control variables $\Delta s_d''(s)$ and $\Delta s_q''(s)$ (switching function phasor) as well as in the disturbance variables $\Delta u_{Ld}''(s)$ and $\Delta u_{Lq}''(s)$ (AC-system voltage phasor components) will correspond to negative sequence 2nd harmonics in the 3-phase plane.

In eqn. (7.24) it is not difficult to recognize, that negative sequence 2nd harmonics in the above mentioned control or disturbance variables will cause a DC-component to arise in $u_{Ddiff}(s)$.

By simply assuming DC-load-steps in $\Delta s_d"(s)$, $\Delta s_q"(s)$, $\Delta u_{Ld}"(s)$ and $\Delta u_{Lq}"(s)$ according to

$$\Delta s_d''(s) = \frac{\Delta S_{d0}''}{s}, \qquad \Delta s_q''(s) = \frac{\Delta S_{q0}''}{s},$$
$$\Delta u_{Ld}''(s) = \frac{\Delta U_{Ld0}''}{s}, \qquad \Delta u_{Lq}''(s) = \frac{\Delta U_{Lq0}''}{s}$$

and applying the 'final value theorem' of the Laplace transform ([58])

$$\lim_{s\to 0} (s \cdot F(s)) = \lim_{t\to\infty} f(t),$$

to eqn. (7.24) results after a short analysis to eqn. (7.26).

In eqn. (7.26) it can clearly be seen, that for any DC-side unbalance source ΔS_{d0} ", ΔS_{q0} ", ΔU_{Ld0} " and ΔU_{Lq0} ", the resulting DC-side unbalance lim u_{Ddiff} will not be infinite, but limited to values, which can now be calculated with eqn. (7.26).

This once again proves that the 3-level VSI has the inherent ability to counteract to a DC-unbalance:

In presence of a DC-side unbalance source, U_{Ddiff} increases up to that point, where the 3-level VSI self-balancing DC-component in i_0 equals



System parameters:		
<i>r</i> :	resistive part of the system in [p.u.]	
<i>l</i> :	stray reactance of the transformer in [p.u.]	
ω ₁ :	fundamental frequency of the AC-system in [rad]	
AC-side phasor quantities with respect to a d/q frame rotating with an angular velocity of a negative sequence 2nd harmonic $-2\omega_1$:		
$\Delta s_d''(s)$:	deviations in the d-component of the switching function phasor in [p.u.]	
Δs_q "(s):	deviations in the q-component of the switching function phasor in [p.u.]	
$\Delta u_{Ld}^{"}(s)$	deviations in the d-component of the AC-system voltage phasor in [p.u.]	
$\Delta u_{Lq}^{"}(s)$	deviations in the q-component of the AC-system voltage phasor in [p.u.]	
<i>S²d0</i> ":	steady-state d-component of the squared switching function phasor in [p.u.]	
<i>S²q</i> 0":	steady-state q-component of the squared switching function phasor in [p.u.]	
<i>I_{d0}</i> ":	initial d-component of the AC-side current phasor in [p.u.]	
<i>I_{q0}</i> ":	initial q-component of the AC-side current phasor in [p.u.]	
DC-side quantities:		
u _{Ddiff} (s):	variation in time of the DC-side unbalance in [p.u.]	
U _{Dsum0} :	steady-state total DC-side voltage in [p.u.]	

table 7.14: Quantities in the 3-level VSI DC-side unbalance transfer functions (table 7.13)

$$\lim_{t \to \infty} u_{Ddiff} = -\frac{(rS^2_{d0}" + 2\omega_1 lS^2_{q0}")U_{Dsum0}}{r[(S^2_{d0}")^2 + (S^2_{q0}")^2]} \Delta S_{d0}" -$$
(7.26)
$$-\frac{(rS^2_{q0}" - 2\omega_1 lS^2_{d0}")U_{Dsum0}}{r[(S^2_{d0}")^2 + (S^2_{q0}")^2]} \Delta S_{q0}" +$$
$$+\frac{2(rS^2_{d0}" + 2\omega_1 lS^2_{q0}")}{r[(S^2_{d0}")^2 + (S^2_{q0}")^2]} \Delta U_{Ld0}" +$$
$$+\frac{2(rS^2_{q0}" - 2\omega_1 lS^2_{d0}")}{r[(S^2_{d0}")^2 + (S^2_{q0}")^2]} \Delta U_{Lq0}"$$

those introduced by the DC-side unbalance source.

However, the hereby resulting steady-state values $\lim_{t\to\infty} u_{Ddiff}$ can take on unreasonable large values, which will be shown in chapter 7.5.4.

The above described limiting behaviour of the 3-level VSI will be subject to change, if no ohmic part will be in the system. Then the transfer functions in eqn. (7.24) will result to eqn. (7.25).

Applying the 'final value theorem' of the Laplace transform ([58]), it can easily be seen that $\lim_{t\to\infty} u_{Ddiff}$ will strain after infinity for any DC-side unbalance source $\Delta S_{d0}^{"}$, $\Delta S_{a0}^{"}$, $\Delta U_{Ld0}^{"}$ and $\Delta U_{Lq0}^{"}$ unequal to 0.

7.5.2 DC-side unbalance caused by transient load steps

Probably one of the most frequent DC-side unbalance sources is with respect to transient load steps in the controlled variables of the 3-level VSI.

Mathematically, the influence of these DC-side unbalance sources can hardly quantitatively be described. In order to get a quantitative feeling for their impact, simulations with representative parameters are very well suited to fulfil this task.

Hence, a simulation with the well known SVC-example was performed, in which the compensator is undergoing two load-steps in its control variable, which is the reactive phasor component i_a' of the AC-side currents i_{ph} .

During the first 500ms, the SVC is working in a neutral mode $(i_q'=0)$, which is followed by a load step into the nominal capacitive mode $(i_q'=1)$ at

t=500ms. Finally, at t=1sec. the compensator is forced into the nominal inductive operation mode $(i_q'=-1)$ for the rest of the simulation. Concerning the applied control strategy, the reader is referred to chapter 6.3.1 for a brief and to chapter 9.3 for a more detailed description.

The variation in time of i_q' is presented in the upper graphic of figure 7.4. Simultaneously, the response of the DC-side voltage u_{Ddiff} to these transient load steps in i_q' is given in the lower graphic of figure 7.4.



AC-side current phasor component i_a

fig 7.4: response of the (filtered) DC-side voltage u_{Ddiff} to load steps in the controlled variable i_q' of the FFM modulated SVC-example

Here again, for clearness reasons, u_{Ddiff} is filtered by means of 2nd order notch filters (150Hz, quality factor 0.56).

It can be clearly seen in the upper graphics of figure 7.4, that fortunately the transient load steps in i_q' will only cause a small DC-side unbalance of the two DC-side voltages u_{D1} and u_{D2} of not more than about 0.01[p.u.].

However, though the DC-side capacitor value is chosen not too small, the

dynamic of u_{Ddiff} is quite fast, which would also ask for a controller with a similar fast dynamic performance in order to rapidly counteract to this DC-unbalance. This in its turn is difficult to realize, since the necessary filtering of u_{Ddiff} (small DC-component compared to a large 3rd harmonic) always introduces a certain delay into the closed control loop.

Last but not least, also the self-balancing attributes of the 3-level VSI are once more underlined in the upper graphic of figure 7.4. Since they are quite moderate, an additional DC-side unbalance controller will therefore be quite desirable.

Finally it should be mentioned that the badly damped oscillations, which are apparent in both graphics of figure 7.4 especially after the second load step at t=1sec., correspond to the resonance of the system, which is determined by the zeros of the denumerator. These oscillations are superimposed to U_{Ddiff} and will in addition slightly increase the DC-side unbalance transiently.

It was shown in [59] - [62], that these oscillations will be present in all 2level VSI quantities. Here, it is now evident from both the transfer functions in table 7.13 and the simulation results, that they also have to be expected in those quantities, which exclusively exist for the 3-level VSI.

7.5.3 DC-side unbalance caused by transients in the AC-system voltages

Another possible DC-side unbalance source is represented by transients in the AC-system voltages u_{Lph} , like voltage drops, single line faults, etc.

Their quantitative impact will be studied by means of a large single line voltage drop of 0.75[p.u.] in the AC-system voltage u_{La} . This type of AC-system voltage transient counts responsible for roughly 90% of all AC-system voltage disturbances.

At t=40ms, the SVC is connected to the AC-system and controlled into the nominal capacitive operation mode $(i_q'=1)$. Then, at t=105ms, the above described voltage drop of 0.75[p.u.] in u_{La} will take place, which will be cleared 200ms later, at t=305ms.

The fundamentals of the AC-side currents i_{ph} are controlled to constitute a symmetrical 3-phase system, also during the severe AC-system fault. This will be achieved by an additional feed-forward controller, which will be described in detail in chapter 9.4.



fig 7.5: response of the filtered and unfiltered DC-side voltage u_{Ddiff} to an AC-system voltage drop of 0.75[p.u.] in u_{La} , feed-forward controller implemented for the controlled variable i_a' of the FFM modulated SVC

The variation in time of u_{La} , i_q' and, of course, the unfiltered and filtered DC-side voltage u_{Ddiff} , which represents the dynamic of the DC-side unbalance, are shown in figure 7.5.

From the lowest graphic in figure 7.5 it can be seen, that the magnitude of the DC-side unbalance U_{Ddiff} , introduced by this severe AC-system fault, is still in a reasonable range and limited to slightly more than 0.05[p.u]. Also here however, the dynamic of the arising unbalance U_{Ddiff} is pretty fast, which constitutes a challenging touchstone of an additional DC-side unbalance control scheme.

Further, with respect to the unfiltered DC-side voltage U_{Ddiff} (third graphic from the top), a remarkable 50Hz component is present during the AC-system fault, which once more confirms the qualitative and quantitative harmonic analysis performed in chapter 4.4 and chapter 6.5.

Finally it should be noted that this harmonic with fundamental frequency must also not be forgotten, when designing the necessary filter for u_{Ddiff} in an additional DC-side unbalance control!

7.5.4 Unbalance caused by even numbered AC-system harmonics

In the two previous chapters, the influence of transient DC-side unbalance sources have been investigated, which however will not introduce a steady-state DC-side unbalance U_{Ddiff0} .

This proves right, since their influence will be limited to a short time, after which the 3-level VSI itself is capable to slowly 'self-control' this DC-side unbalance to 0.

This will now be subject to change in the following chapters, where the influence of steady-state DC-side unbalance sources will be studied quantitatively.

As could be seen in eqn. (7.26), a negative sequence 2nd harmonic in the AC-system voltages u_{Lph} represents one of those steady-state DC-side unbalance sources and will therefore be investigated more in depth.

a) Simulations

For that purpose, two simulations have been performed for the SVC example with SABER. In the first simulation a negative sequence 2nd AC-system harmonic with an amplitude of 0.02 [p.u.] is assumed to be in phase a cophasal with the AC-system voltage fundamental of u_{La} . In the second

simulation, this harmonic will have the same amplitude, however a lagging phase-displacement of $\pi/2$ with respect to the fundamental of u_{La} is chosen. Further, the compensator is working in the nominal capacitive mode $(i_a'=1)$ during the whole simulation interval.

It should be noted, that in practical applications, such a magnitude can easily arise for this harmonic in case that the inverter transformer or another transformer in the vicinity of the inverter is saturating.

The two simulation results, showing the response of the reactive AC-side current phasor component i_q' and the filtered DC-side voltage u_{Ddiff} are given in figure 7.6 and figure 7.7. Additionally, in figure 7.7, the line diagrams of the two individual DC-side voltages u_{D1} and u_{D2} are also included.



AC-side current phasor component i_a

fig 7.6: response of i_q' and u_{Ddiff} (filtered) to a negative sequence 2nd harmonics in u_{Lph} with an amplitude of 0.02[p.u.], cophasal to the fundamental of u_{Lph}



fig 7.7: response of i_q' , u_{Ddiff} (filtered), u_{D1} and u_{D2} to a negative sequence 2nd harmonic in u_{Lph} with an amplitude of 0.02[p.u.], phase-displaced by $\pi/2$ to the fundamental of u_{Lph}

b) Discussion

As can be seen in the corresponding graphics for the filtered DC-side voltage u_{Ddiff} in figure 7.6 and figure 7.7, the steady-state DC-side unbalance U_{Ddiff0} remarkably differs for the two simulations, which becomes evident when having a closer look at the scales of the vertical axes.

On the first sight, these results might be astonishing, since it could not be expected that the phase of this AC-system 2nd harmonic would have such a drastic influence.

However, remembering the graphical model introduced in figure 7.2 of chapter 7.4.3a), quite a simple explanation can be derived.

The negative sequence 2nd harmonic in u_{Lph} will for sure cause an AC-side current harmonic to arise with the same frequency and phase sequence. This AC-side current harmonic in its turn will be transformed to the DC-side and will also contribute to the generation of the NP-current i_0 and in particular to its DC-component.

Now, according to figure 7.2 in chapter 7.4.3, the phase-displacement between the AC-side current harmonic and the (squared) switching functions $(s_{ph}^2) s_{ph}$ determines the arising DC-component in i_0 and with that the magnitude for the driving DC-side unbalance force.

In case of the simulation where the negative sequence 2nd AC-system harmonic is cophasal with the AC-system voltage fundamental, the corresponding AC-side current harmonic will be phase-displaced by roughly $\pi/2$ with respect to the (squared) switching function fundamental. This can easily be verified by a phasor diagram (e.g. figure 5.2 in chapter 5.4.2) for a pure reactive 3-level VSI operation mode as assumed here.

Hence, according to figure 7.2 in chapter 7.4.3, only a very small DC-component will be introduced in i_0 .

Similar considerations can be performed for the case that the negative sequence 2nd AC-system voltage harmonic is phase-displaced by $\pi/2$ with respect to the fundamental of the AC-system voltage u_{La} . It will then be apparent that the resulting DC-component in i_0 will have an almost maximum value, which will therefore also yield an unreasonable large steady-state DC-side unbalance U_{Ddiff0} , to which the 3-level VSI might hardly counteract.

Latest at this point, the simulations have shown that an additional DC-side unbalance controller will be absolutely necessary in order to protect the 3level VSI from destruction. This can be clearly seen in figure 7.7 for the reactive current phasor component i_q' and the individual DC-side voltages u_{D1} and u_{D2} . After a few hundred milliseconds they will take on values, which would destroy both the 3-level VSI valves and the DC-side capacitors due to the large voltage and current stress.

With respect to i_q' in figure 7.7 it should be noted, that the arising large oscillation, superimposed to the DC-component $i_q'=1$ [p.u.], represents a 3rd harmonic, which in the 3-phase plane corresponds to a negative sequence 2nd harmonic. This negative sequence 2nd harmonic is generated by the DC-side unbalance and will increase up to that moment, where its DC-contribution to the NP-current will be as large as those caused by the small negative sequence 2nd harmonic in u_{Lab} .

However, as can also be seen in figure 7.6, the dynamic of the arising DC-side unbalance U_{Ddiff} is very slow and therefore, it should not be a problem to design an appropriate controller.

c) Mathematical verification of the simulation results

Finally, to verify the validity of the achieved simulation results, the steadystate DC-side unbalance U_{Ddiff0} for both simulations will in addition be calculated with eqn. (7.26).

Herein, the given negative sequence 2nd AC-system voltage harmonics result to

$$\Delta U_{Ld0}$$
" = 0.02 [p.u.] and ΔU_{Lq0} " = 0 [p.u.]

for those being cophasal with the AC-system voltage fundamental of u_{La} , and to

$$\Delta U_{Ld0}^{"} = 0$$
 [p.u.] and $\Delta U_{La0}^{"} = 0.02$ [p.u.]

for those being phase-displacement by $\pi/2$ with respect to the AC-system voltage fundamental of u_{La} .

This proves right, since according to chapter 8.4.5, the d-axes of the d/qframes used in this thesis always coincide with the d-component of the ACsystem voltage phasor.

The phasor components S_{d0}^2 and S_{q0}^2 of the squared FFM ($\beta = \pi/10$) switching functions s_{ph}^2 were determined by means of a FFT and resulted to

$$S_{d0}^2 = 0.374,$$
 $S_{q0}^2 = 3.8 \cdot 10^{-3}.$

Together with the other system parameters,

r = 0.005 [p.u.] and l = 0.2 [p.u.],

the corresponding terms in eqn. (7.26) result to

$$\lim_{t \to \infty} u_{Ddiff} = 0.194 \text{ [p.u.]} \text{ and } \lim_{t \to \infty} u_{Ddiff} = -8.55 \text{ [p.u.]}$$

The finally resulting steady-state values for u_{Ddiff} have to be expected to be smaller than this calculated value (about 15% according to eqn. (7.23) for the SVC example), since the self-balancing contribution of the harmonics in u_{Dsum} (chapter 7.4.5) are not taken into account in eqn. (7.26). The same proves right for the entirety of all higher ordered even numbered AC-side current harmonics, which in addition might slightly contribute to the selfbalancing (chapter 7.4.4).

Having the latter mentioned in mind, it can be concluded that both the analysis and the SABER simulation are in very good agreement.

A third verification was achieved by performing the same two simulations with the MATLAB program introduced and described in chapter 6.2.

The hereby achieved steady-state values for all 3-level VSI quantities were in excellent coincidence with those from the SABER simulations.

It should again be emphasized here, that the SABER simulator and this 3level VSI specific MATLAB program are basing on absolutely different solution algorithms. Due to this, these two programs can be seen as independent simulation tools, which are quite well suited for the consolidation of at least steady-state results.

Hence, it can be concluded that a negative sequence 2nd harmonic in the AC-system voltages u_{Lph} will constitute one of the most serious DC-side unbalance sources.

In general, the same is true for all other even numbered harmonics in u_{Lph} with an appropriate phase sequence, e.g. a positive sequence 4th harmonic, a negative sequence 8th harmonic etc.. However their influence will be better damped by the decoupling inductance l.

7.5.5 DC-side unbalance caused by switching inaccuracies

Another very common steady-state DC-side unbalance source, which proba-

bly will be present in every 3-level VSI, is with respect to inaccuracies in the switching instants of the 3-level VSI pulse patterns.

Due to unavoidable manufacturing tolerances, the electronic parts in the gate-drives and also the high power switches itself are physically not identical and hence will always cause deviations in the switching instants.

The influence of these deviations should therefore not be forgotten and it will be interesting to get a quantitative feeling for their impact on the DCbalance of u_{D1} and u_{D2} .

For that purpose, quite a large delay of 50µs in the arbitrarily chosen upper valve of phase a was assumed for the FFM modulated SVC-example. This one large delay will also be representative for the sum of many smaller deviations, which may occur when the switching frequency is higher than those for FFM.

Again a simulation was performed with SABER, the result of which is given in figure 7.8. AC-side current phasor component i_{a}



fig 7.8: response of i_q' and the (filtered) DC-side voltage u_{Ddiff} to a steady-state delay of 50µs in the switching instant of the upper valve in phase a for the FFM modulated SVC-example

It is interesting to see, that this kind of DC-side unbalance does not introduce a major stress for the 3-level VSI, since the steady-state value for U_{Ddiff} will be limited by the self-balancing abilities to less than 0.04[p.u.]. This even proves right for the quite large switching instant delay of 50µs, which in most cases will not be that huge.

In addition, the dynamics of this DC-side unbalance drift are quite slow.

Also the reactive phasor component i_q' does not seem remarkably be influenced by this switching inaccuracy, though for sure small, here obviously not visible, even numbered AC-side current harmonics will be present in the 3-phase plane.

Hence, it can be concluded that this kind of unbalance source will not constitute a major challenge for an additional DC-side balance controller.

Finally, in order to consolidate the achieved results, the steady-state values of the most important 3-level VSI quantities $(i_{ph}, i_0, u_{D1}, u_{D2}, u_{Ddiff}, u_{Dsum}$ and s_{ph}) achieved at t=10sec. have been compared with those resulting from a simulation with the MATLAB program described in chapter 6.2. Again, a very good coincidence could be observed.

Last but not least, it should be noted, that in small scaled hardware models, where the 3-level VSI self-balancing abilities are quite good and the low power valves are more accurate, only a very small, really negligible DC-side unbalance U_{Ddiff0} can be expected.

7.6 Summary

This chapter was focusing on the effects caused by a DC-side unbalance, which constitutes one of the major 3-level VSI drawbacks. In addition, the most common DC-side unbalance sources and their individual quantitative impacts were presented.

In a first step it was shown that in case of a DC-side unbalance additional harmonics will have to be expected in the 3-level VSI quantities.

On the AC-side, even numbered 3-level VSI output-voltage harmonics will arise, which generate even numbered current harmonics. These even numbered current harmonics do not only yield an extra stress for the inverter valves but also a highly undesirable harmonic distortion for the AC-system.

On the DC-side, the harmonic orders of the individual DC-side voltages

 u_{D1} and u_{D2} will be the same as for balanced DC-side conditions. However, in case of a DC-side unbalance, the individual harmonics will no longer show up the same amplitudes in both voltages u_{D1} and u_{D2} and also their mutual phase-displacements will no longer equal to 0 or π .

As a result of this, u_{Dsum} will contribute with harmonics which are odd numbered multiples of 3 (without DC-unbalance: multiples of six), while u_{Ddiff} will show up harmonics which are multiples of six (without DC-unbalance: odd numbered multiples of three).

In a next step, the 3-level VSI self-balancing attributes have been investigated in depth. It could be shown that the 3-level VSI topology will be inherently self-balancing.

This is due to the fact, that in case of a DC-side unbalance U_{Ddiff0} , the 3level VSI always generates a DC-component in the NP-current i_0 , which is proportional to U_{Ddiff0} itself and which counteracts to it.

This DC-component in i_0 will be generated by the convolution of the even numbered AC-side current harmonics (which in its turn are caused by the DC-unbalance) with the squared switching functions s_{ph}^2 .

These statements will prove right for all 3-level VSI operation modes (reactive and active power exchange with the AC-system), for all switching functions with at least a symmetry to half of a period and for any switching frequencies.

However, if no ohmic part r will be present in the system, no self-balancing will occur.

The self-balancing response of the 3-level VSI to an initial DC-side unbalance U_{Ddiff0} can quite well be approximated by an exponential function, the time constant τ_{bal} of which will be

- approximately inversely proportional to the ohmic part r of the system.
- approximately proportional to the squared decoupling inductance l^2 of the system.
- proportional to the capacitor size c
- inversely proportional to the squared amplitude of the 2nd harmonic of the squared switching functions s_{ph}^2 .

In high power systems, where the ohmic part r is very small, the self-balancing time constant τ_{bal} will be very large (a few seconds), which makes an additional DC-side balance controller at least recommendable.

Finally, the impact of various DC-side unbalance sources have been investigated. It could be seen that a DC-side unbalance will predominantly be caused by

- transient load steps of controlled variables
- transient disturbances of the AC-system voltages u_{Lph}
- even numbered harmonics with an appropriate phase sequence in the AC-system voltages u_{Lph}
- inaccuracies in the switching instants of the 3-level VSI valves

Transient load steps cause only a moderate DC-side unbalance in U_{Ddiff} , which usually will be limited to small values (about 0.02 [p.u.]) for reasonable sized capacitors ($c_{tot}=1.5$ [p.u.] or $\tau_{c_{tot}}=4.32$ msec).

Transient disturbances of the AC-system voltages u_{Lph} can introduce a DCside unbalance U_{Ddiff} with still tolerable magnitudes of about 0.05 [p.u.]. This however presumes, that the size of the DC-side capacitors, which can limit U_{Ddiff} to reasonable values, must not be chosen too small!

Even numbered harmonics in the AC-system voltages u_{Lph} seem to be the most powerful DC-side unbalance sources. Even quite small negative sequence 2nd harmonics (or 4th positive sequence harmonics) can cause a very large DC-unbalance. Hereby, the 3-level VSI self-balancing abilities will no longer be capable to limit their impact to reasonable small values. This could be shown by both mathematical analysis and simulations with SABER.

Inaccuracies in the switching instants of the 3-level VSI valves, for example switching delays of 50 μ s, cause only moderate steady-state DC-unbalance, which is kept at a low level of about U_{Ddiff0} =0.03[p.u.] by the self-balancing abilities.

The results of the studies clearly showed, that an additional active balance controller is highly recommendable in high power applications, where unusual operation conditions could cause severe DC-unbalance, which cannot be limited by the self-balancing abilities to moderate steady-state values.

Hence, additional DC-side balance control will be investigated in the next chapter.

8 The 3-level VSI DC-side balance control

8.1 Overview

This chapter focuses on investigations concerning the active DC-side balance control of the two DC-side voltages u_{D1} and u_{D2} .

An introduction describes traditional solutions with their basic principle and their application field. In addition their validity limits are explained, which confirms the need for a new method suitable for applications, which exclusively (e.g. SVCs) have to provide a pure or almost pure reactive power.

In a first step, two different DC-side control measures, which are basing on modifications of the switching functions s_{ph} , are introduced and discussed with the help of a simplified graphical model. It will be shown, that for the pure reactive operation mode, exclusively one of the two proposed methods will be suitable.

In a next step, the graphical results will mathematically be verified with the 3-level VSI transfer functions for the pure reactive operation mode by means of a SVC with realistic system parameters. It will be shown, that the system behaviour has to be described by both the transfer functions derived in a d/q frame rotating with an angular velocity ω_1 and those achieved in a d/q frame rotating with an angular velocity $-2\omega_1$.

Further, basing on the transfer functions, a DC-side balance control will be designed for the FFM modulated SVC application. This control scheme will mainly consist in a conventional closed loop with PI-controller for the controlled variable u_{Ddiff} . In addition, a feed-forward controller for disturbances introduced by the AC-system voltages u_{Lph} , will be superimposed.

Finally, the performance of the designed control scheme will be verified with the simulation tool SABER by means of the different DC-side unbalance sources introduced in chapter 7.5.

8.2 Introduction

Possible hardware solutions for the DC-side balancing include the installa-

tion of resistors in parallel to the capacitors or more sophisticated chopper circuits, which only become active if a DC-side unbalance occurs. However, since for all these solutions additional components are necessary, which will cause higher costs and losses, they are not interesting for high power applications.

Therefore, control schemes, where additional hardware components can be avoided, are highly desirable. These control schemes are based on modifications of the switching functions s_{ph} , which, as is well known, constitute the control variables of the (3-level) VSI. Hereby, it is preferable not to increase the switching frequency by the DC-side balancing control scheme.

Many publications concerning DC-side balancing control methods, especially for drives applications, have been published in the last few years (e.g. [63], [44]). The principle of many of these proposed control schemes is rather simple and consists in the introduction of an appropriate DC-component in the switching functions s_{ph} . This measure is quite efficient, if the load to be fed by the 3-level VSI is an AC-drive, or, more general, if the 3level VSI delivers or absorbs an active power.

Unfortunately this control scheme fails, if the 3-level VSI is operated in a pure reactive operation mode (e.g. SVC) as will be shown in chapter 8.3. Also the AC-drive will be disconcerted, when operating with no mechanical load (i.e. consuming the mainly reactive magnetization current from the 3-level VSI).

Another approach is based on the 3-level VSI output voltage vectors in the α/β -plane (appendix C.1.1) [65]. This kind of DC-side balance control scheme has the advantage that the controller does not affect the AC-side currents, since its operation principle consists in modifications of the 3-level VSI output voltages by means of zero sequence systems. However, both an increased switching frequency $f_{s_{ph}}$ and smaller modulation indices *m* (inner voltage vectors!) have to be taken into account.

Therefore a DC-side balancing control scheme, which both does not increase the switching frequency and is suitable for a pure reactive power transfer, is highly desirable. A solution for carrier based PWM was proposed yet in [64]. However, this scheme is not directly applicable for FFM or off-line-optimized pulse patterns. Therefore, a control measure to deal with these modulation schemes will be presented in chapter 8.3.

8.3 DC-side balancing control measures

This chapter introduces two different DC-side balance control principles, which both are basing on suitable modifications of the switching functions s_{ph} . These suitable modifications in s_{ph} focus on the generation of a balancing DC-component in the NP-current i_0 . Hereby, the influence of both control measures on the resulting NP-current i_0 will in addition be separately be studied for a pure active and a pure reactive operation mode.

The investigations will be performed with the help of the graphical model introduced in chapter 5.4.3 (e.g. figure 5.3). Again, it will be of great help for studies concerning the generation of a DC-component in the NP-current, necessary to control a DC-side unbalance to 0.

The quantities used in the following graphics are for clearness reasons summarized in table 8.1.

8.3.1 DC-side balancing control of type I for pure active operation mode

Having the intention to introduce a DC-component into the NP-current i_0 , one might have the idea to modify the switching functions by shortening the positive pulses, while simultaneously lengthening the negative ones, or vice versa.

In order to distinguish this DC-side balance control measure (unequal pulse length for the corresponding pos. and neg. pulses) from the one introduced in chapter 8.3.2, it will here be coined **DC-side balance control of type I.**

This pulse pattern modification is shown in graphic a) of figure 8.1 for FFM modulation and a pure active operation mode. Hereby the positive block of s_a is shortened while the negative one is lengthened. It is obvious, that this measure will yield a zero sequence DC-component to arise in the switching functions, which will ineffectively drop over the transformer's secondary starpoint SP and the neutral point NP on the 3-level VSI DC-side.

It is further shown in graphic a) of figure 8.1, that the NP angles in fact are shifted to the left and right side respectively, their length however still remains the same in the two half-periods.

a) Influence of the AC-side current fundamental

This switching function modification has a remarkable influence on the re-

Switching function related quantities:		
s _a (original)	: original switching function without DC-side balance control measure applied	
s_a (modified): switching function of phase a with DC-side balance control measure applied		
γ:	DC-side balance control variable (= phase-displacement of switching instants)	
AC-side current related quantities:		
<i>i_{a, b, c1}</i> :	AC-side current fundamentals for the 3 phases $ph=a,b,c$	
<i>i_{a, b, c2}</i> :	AC-side current neg. seq. 2nd harmonic caused by the DC- side balance control measure for the 3 phases $ph=a,b,c$	
NP-current related quantities:		
<i>i</i> 0_ <i>ia1</i> :	NP-current generated by the AC-side current fundamental i_{a1} of phase a	
<i>i</i> 0_ <i>iph1</i> :	NP-current generated by all 3 AC-side current fundamentals i_{ph1}	
<i>i</i> _{0_<i>i</i>_{a2}:}	NP-current generated by the AC-side current	
	neg. seq. 2nd harmonic i_{a2} of phase a	
<i>i</i> 0_ <i>iph</i> 2:	NP-current generated by all 3 AC-side current	
	neg. seq. 2nd harmonics i_{pk2}	
$I_{0DC_i_{phI}}$:	NP-current DC-component caused by $i_{0_{-i_{phl}}}$	
$I_{0DC_i_{ph2}}$:	NP-current DC-component caused by $i_{0_{-i_{ph2}}}$	
$I_{0DC_i_{phl+2}}:$	NP-current DC-component caused by $i_{0_{-i_{ph1}}}$ and $i_{0_{-i_{ph2}}}$	
<i>I_{0DC}</i> :	DC-component of the NP-current i_0 , including $I_{0DC_i_{phl+2}}$ and the contributions of all higher ordered even and odd	
	numbered AC-side current narmonics	

table 8.1: Quantities used in figure 8.1 - figure 8.5



Impact of the AC-side current fundamental $i_{a, b, c1}$

fig 8.1: DC-side balance control of type I (different pulse lengths for the corresponding pos. and neg. pulses of the switching functions s_{ph}) and its impact on the NP-current i_0 for pure active operation mode (figure 5.2), r=0, l=0.2[p.u], $\beta=\pi/10$, $\gamma=0.2$ rad, see also table 8.1

sulting NP-current i_0 . Assuming the pure active AC-side current i_a to be represented by its fundamental i_{a1} , it can clearly be seen in graphic a) of figure 8.1 that its contribution $i_{0_i_{a1}}$ to the NP-current i_0 will show up a large DC-component.

This DC-component, presuming the appropriate sign, could now be used for actively controlling the DC-side balance. Further, its magnitude increases with increasing values for the DC-side balance control angle γ .

Taking into account all three phases a,b,c, yields the resulting NP-current $i_{0_i_{ph1}}$ in graphic b) of figure 8.1, which contributes with the triple DC-value compared to $i_{0_i_{al}}$. However, assuming $i_{a1}=0$, no balancing DC-component will be present in i_0 , as can also clearly be seen in graphic a) of figure 8.1.

The statements made so far will also qualitatively prove right for a mixed operation mode (both active and reactive power exchange with the AC-system). Exclusively the magnitude of the arising DC-component in i_0 will be smaller than for a pure active operation mode.

b) Influence of the negative sequence 2nd AC-side current harmonic

To proceed further, it is as well obvious from graphic a) in figure 8.1, that due to the above described modification, the FFM switching function has lost its symmetry to a quarter of a period and will now have a symmetry to its whole period. This in its turn will introduce even numbered harmonics in its spectrum, which will cause even numbered AC-side currents to arise.

The influence of its most predominant representative, the neg. seq. 2nd ACside current harmonic i_{a2} is shown for phase *a* in graphic c) of figure 8.1. Hereby, the amplitude corresponds to the modified FFM switching function with a NP-angle $\beta = \pi/10$ ($\beta = 18^{\circ}$) and a decrease/increase of the pos./ neg. switching function blocks of $\gamma=0.2$ rad. Further, for simplicity reasons, the ohmic part of the system is neglected (r=0) and the decoupling inductance is assumed to be l=0.2[p.u.].

Though quite a large amplitude can be observed for i_{a2} , no DC-component will be introduced in the resulting NP-current $i_{0_{-}i_{a2}}$ as can be verified in graphic c) of figure 8.1.

This is due to the fact, that the phase-displacement of i_{a2} with respect to the fundamental of the switching functions will for r=0 be exactly $\pi/2$ (quarter period of i_{a2}). As a result of this, no DC-component will be apparent in the NP-current $i_{0,i_{a2}}$.

More, since this AC-side current 2nd harmonic is exclusively caused by the modification of the switching functions, its phase displacement with regard to the modified NP-angles will be constant for all operation modes (all phase-displacements of s_{ph} with regard to the AC-system voltages u_{Lph}).

The statements derived above are also mathematically proved in appendix B.2.2 and appendix B.3.2 for both FFM and off-line optimized PWM pulse patterns. It could be shown in eqn. (B.25) (FFM) and eqn. (B.34) (offl. opt. PWM), that in general all even numbered switching function harmonics, generated by the DC-side balance control measure of type I, will be cophasal or anti-phasal to the switching function fundamental. This in its turn, presuming the decoupling impedance to be pure inductive, will cause even numbered AC-side current harmonics, which are phase-displaced by $\pm \pi/2$ with regard to its generating switching function harmonics.

For $r \neq 0$, i_{a2} will no longer be phase-displaced by $\pi/2$ (quarter period of i_{a2}) with respect to the fundamental of the switching functions. This will cause a DC-component to arise in $i_{0_{a2}}$, which however for the realistic small values of r will be negligible to those DC-component generated by the fundamental components i_{a1} of the AC-side currents i_{a} .

Finally, the above mentioned statements will also prove right, if all three phases a,b,c will be taken into account, as becomes evident in graphic d) of figure 8.1.

c) Dependancy on the pure active operation mode range

Finally, the dependancy of the described DC-side balance control measure on the pure active operation mode range varying between $i_d' = -1$ and $i_d' = 1$ will be studied.

For that purpose, a simulation with varying values for i_d has been performed with a MATLAB program, in which the 3-level VSI is modelled according to the equations derived in chapter 2.4. In addition, for simplicity reasons, the ripple of the DC-side voltages is not taken into account. The chosen FFM switching functions are modified with a constant DC-side balance control angle $\gamma=0.2$ [rad] over the whole investigated operation mode range.

Further, the particular DC-components in the NP-current i_0 are determined by calculating the mean value of the particular NP-current equations given in eqn. (8.1) - eqn. (8.4).

$$I_{0DC_i_{phl}} = mean(-(i_{a1} \cdot s_a^2 + i_{b1} \cdot s_b^2 + i_{c1} \cdot s_c^2))$$
(8.1)

$$I_{0DC_{-}i_{ph2}} = mean(-(i_{a2} \cdot s_a^2 + i_{b2} \cdot s_b^2 + i_{c2} \cdot s_c^2))$$
(8.2)

$$I_{0DC_i_{phl+2}} = I_{0DC_i_{phl}} + I_{0DC_i_{ph2}}$$
(8.3)

$$I_{0DC} = mean(-(i_a \cdot s_a^2 + i_b \cdot s_b^2 + i_c \cdot s_c^2))$$
(8.4)

The herein used AC-side current fundamentals i_{ph1} and neg. seq. 2nd harmonics i_{ph2} resulted from a FFT for the total AC-side current i_{ph} .

The particular arising DC-components $I_{0DC_i_{phl}}$, $I_{0DC_i_{ph2}}$ and $I_{0DC_i_{phl+2}}$, which are caused by $i_{0_i_{ph1}}$, $i_{0_i_{ph2}}$ and their sum respectively, are presented in the upper three graphics a) - c) of figure 8.2.

In addition, I_{0DC} , which coincides with the total DC-component of i_0 , (all higher ordered odd and even numbered AC-side current harmonics have also been taken into account), is as well shown in graphic c) of figure 8.2.

From graphic a) in figure 8.2, it can be seen, that both the amplitude and the sign of the DC-component $I_{0DC_{-}i_{phl}}$ depends on the pure active operation point. Further, for $i_d' = 0$, no balancing DC-component $I_{0DC_{-}i_{phl}}$ will be present in $i_{0_i_{phl}}$. These results could also be verified in figure 8.1 by virtually varying the amplitude of i_{ph1} .

However, it should be emphasized, that fortunately, this zero crossing of the resulting DC-component $I_{0DC_{-i_{phl}}}$ is not depending on varying system parameters like the AC-system impedance, or a variable 3-level VSI DC-side voltage. This makes it much easier for a control design, where also the sign of e.g a PI-controller has to be reversed, if the zero crossing of $I_{0DC_{-i_{phl}}}$ takes place.

The neg. seq. 2nd harmonics i_{ph2} fulfil the expectations by not contributing at all with a DC-component $I_{0DC_i_{ph2}}$ over the whole active operation mode range, as clearly shown in graphic b) of figure 8.2.

Hence, also the sum of their impacts, $I_{0DC_i_{phl+2}}$, will be equal to $I_{0DC_i_{phl}}$, as it is evident in graphic c) of figure 8.2.

Finally, graphic c) of figure 8.2 also proves, that $I_{0DC_{-i_{phl+2}}}$ furthermore co-



DC-side balance control of type I, pure active operation mode range

fig 8.2: NP-current DC-components $I_{0DC_i_{pkl}}$, $I_{0DC_i_{pk2}}$, $I_{0DC_i_{pk1+2}}$ and I_{0DC} caused by DC-side balance control of type I (figure 8.1, 8.3) in dependancy on the pure active and pure reactive operation mode range, r=0, l=0.2[p.u], $\beta=\pi/10$, $\gamma=\text{const.}=0.2$ rad, see also table 8.1

incides with I_{0DC} , (total arising DC-component in the NP-current i_0). Therefore, the higher ordered even and odd numbered AC-side current harmonics will, if at all, only have negligible influence.

With that it can be concluded, that for a pure active operation mode, the impact of the DC-side balance control of type I (unequal pulse length for the corresponding pos. and neg. switching function pulses) almost exclusively depends on the following quantities:

- the magnitude of the DC-side balance control variable γ
- the amplitude of the pure active AC-side current fundamental i_{ph1} .
- the direction of active power exchange with the AC-system

This is true for at least FFM and off-line optimized PWM pulse patterns.

Finally, it should be mentioned, that the above discussed DC-side balance control measure of type I constitutes the basis for the control schemes, which have been proposed in the literature up to now (e.g. [63], [44]) for preferably AC-drives applications. Hereby, its implementation is realized in many different ways.

8.3.2 DC-side DC-balancing control of type I for pure reactive operation mode

Now, the impact of the DC-side balancing control of type I on a pure reactive operation mode will be studied.

a) Influence of the AC-side current fundamental

In figure 8.3, the same modifications for s_a are assumed as in figure 8.1, however now the operation mode will be a pure reactive one $(i_q' = 1)$ with respect to the AC-system voltages.

As one can clearly see in graphic a) of figure 8.3, the AC-side current fundamental i_{a1} will no longer contribute with a DC-component in the corresponding NP-current $i_{0,i_{a1}}$.

This is an astonishing and quite undesirable result!

Unfortunately, the phase-displacement of i_{a1} with respect to the switching function's modified NP-angles does not allow a DC-component to arise in $i_{0,i_{a1}}$.

Also the contributions of all three phases a,b,c will not change this fact, which is indicated in graphic b) of figure 8.3.



Impact of the AC-side current fundamental $i_{a, b, c1}$

fig 8.3: DC-side balance control of type I (different pulse lengths for the corresponding pos. and neg. pulses of the switching functions s_{ph}) and its impact on the NP-current i_0 for pure cap. operation mode (figure 5.2), r=0, l=0.2[p.u], $\beta=\pi/10$, $\gamma=0.2$ rad, see also table 8.1
b) Influence of the negative sequence 2nd AC-side current harmonic

In addition, the neg. seq. 2nd AC-side harmonics i_{ph2} (and all even numbered multiples) will not introduce a DC-component $i_{0_{-}i_{ph2}}$ in the NP-current, which is confirmed in graphic c) and d) of figure 8.3.

Hence, it can be summarized up to now, that the DC-side balance control measure of type I will not be suited for the pure reactive operation mode.

Also a small ohmic part $r \neq 0$ will not yield a sufficient large phase-displacement for both i_{ph1} and i_{ph2} to introduce a remarkable DC-component in $i_{0_i_{ph1}}$ and $i_{0_i_{ph2}}$.

c) Dependancy on the pure reactive operation mode range

Finally, these undesirable results are clearly confirmed with the help of the MATLAB program in the graphics d) - f) of figure 8.2 for the whole reactive operation mode range $(-1 \le i_a' < 1)$.

It must therefore be concluded, that the DC-side balance control measure of type I cannot be applied if the 3-level VSI exchanges a pure or almost pure reactive power with the AC-system.

8.3.3 DC-side DC-balancing control of type II for a pure active operation mode

Due to the fact, that the DC-side balance control measure of type I cannot be applied for pure reactive operation modes (SVC), another measure will have to be derived, which will be suitable for these applications.

For that purpose, the switching functions s_{ph} will be modified in another way, which will here be coined **DC-side balance control of type II**.

DC-side balance control of type II means to modify the switching functions s_{ph} by shifting corresponding pos. and neg. pulses in opposite directions, while simultaneously keeping their (equal) pulse lengths unchanged.

This is shown in graphic a) of figure 8.4 for the simple modified FFM switching function s_a in phase a. Herein, it is also evident, that now the individual switching function pulse lengths will remain the same, while the length of the NP-angles will become different.

Hence, in comparison to the DC-side balance control of type I, no DC-component will be apparent in the modified switching function s_{α} .



Impact of the AC-side current fundamental $i_{a, b, c1}$

fig 8.4: DC-side balance control of type II (phase-displacement of the pos. and neg. pulses of the switching functions s_{ph} in opposite directions) and its impact on the NP-current i_0 for pure active operation mode (figure 5.2), r=0, l=0.2[p.u], $\beta=\pi/10, \gamma=0.2$ rad, see also table 8.1

The impact of this measure on the resulting DC-component(s) in the NPcurrent i_0 will now be investigated in the same manner as performed in the previous two chapters for the DC-side balance control of type I.

For comparison reasons, the same system parameters (given in the legend of figure 8.4 - figure 8.5) and the same magnitude for the control variable, the DC-side balance control angle γ , has been chosen, which is $\gamma=0.2$ [rad]. Further, it will first be focused on the pure active operation mode.

a) Influence of the AC-side current fundamental

Starting with the NP-current contribution $i_{0_{i_{al}}}$ of the AC-side current fundamental i_{a1} (graphic a) of figure 8.4), it becomes evident, that once again a remarkable DC-component will be present. Further, its magnitude increases with increasing values for the DC-balancing control angle γ

Obviously also the DC-side balance control measure of type II is well suited for a pure active operation mode. This will additionally be underlined in graphic b) of figure 8.4, where the contributions $i_{0_{i_{phl}}}$ of all three AC-side current fundamentals have been taken into account.

b) Influence of the negative sequence 2nd AC-side current harmonic

Due to the modification, s_a has lost its symmetry to a quarter of a period. Hence, also here even numbered switching function harmonics will have to be expected, which will be the driving force for even numbered AC-side current harmonics.

The influence of its most predominant representative, the neg. seq. 2nd ACside current harmonic i_{a2} is shown for phase a in graphic c) of figure 8.4.

In contrary to the DC-side balance control of type I, now quite a large DCcomponent can be observed in the resulting NP-current $i_{0,i_{1,2}}$.

This is due to the fact, that for r=0, i_{a2} will be cophasal to the fundamental of the switching functions. As a result of this, a maximum DC-component will be arise for the NP-current $i_{0,i_{a2}}$.

More, since this neg. seq. 2nd AC-side current harmonic is exclusively caused by the modification of the switching functions, its phase displacement with regard to the modified NP-angles will be constant for all operation modes (all phase-displacements of s_{nb} with regard to the AC-system

voltages u_{Lph}).

This also implies, that for a given control angle γ , the sign of the DC-component in $i_{0,i_{\alpha}}$ will not change, no matter, which operation mode is chosen.

However, it should be emphasized, that the amplitude of i_{a2} might vary with the operation mode. This is due to the fact, that the amplitude of i_{a2} will be proportional to the 3-level VSI DC-side voltage u_{Dsum} , which in its turn may vary, if the operation point varies. Further, the amplitude of i_{a2} will roughly be inversely proportional to the decoupling inductance, and in addition to a varying AC-system impedance. This effect is highly undesirable, which will be shown in subchapter c).

The statements derived above are also mathematically proved in appendix B.2.3 and appendix B.3.3 for both FFM and off-line optimized PWM pulse patterns. It could be shown in eqn. (B.28) (FFM) and eqn. (B.36) (offl. opt. PWM), that in general all even numbered switching function harmonics, generated by the DC-side balance control of type II, will be phase-displaced by $\pm \pi/2$ to the switching function fundamental. This in its turn, presuming the decoupling impedance to be pure inductive, will cause even numbered AC-side current harmonics, which are co- or anti-phasal with regard to the switching function fundamental.

Finally, the above mentioned statements will also prove right, if all three phases a,b,c will be taken into account, as can be clearly seen in graphic d) of figure 8.4.

c) Dependancy on the pure active operation mode range

Finally, the dependancy of the described DC-side balance control measure of type II on the pure active operation mode range $(-1 \le i_d' < 1)$ will be studied with the MATLAB program. Hereby, the relationships in figure 8.4 correspond to $i_d' = 1$.

The particular arising DC-components $I_{0DC_i_{phl}}$, $I_{0DC_i_{ph2}}$ and $I_{0DC_i_{ph1+2}}$, caused by $i_{0_i_{ph1}}$, $i_{0_i_{ph2}}$ and their sum respectively, are presented in the upper three graphics a) - c) of figure 8.6.

In addition, I_{0DC} , which coincides with the total DC-component of i_0 has also been included in graphic c) of figure 8.5.

Graphic a) in figure 8.5 shows that exclusively the magnitude but not the positive sign of $I_{0DC_{i_{nhl}}}$ (caused by i_{ph1}) depends on the pure active oper-



DC-side balance control of type II, pure active operation mode

fig 8.5: NP-current DC-components $I_{0DC_i_{ph1}}$, $I_{0DC_i_{ph2}}$, $I_{0DC_i_{ph1+2}}$ and I_{0DC} caused by DC-side balance control of type II (figure 8.4, 8.6) in dependancy on the pure active and pure reactive operation mode range, r=0, l=0.2[p.u], $\beta=\pi/10$, $\gamma=\text{const.}=0.2$ rad, see also table 8.1

ation point. Further, for $i_d' = 0$, no balancing DC-component $I_{0DC_{-i_{phl}}}$ will be present in $i_{0_{-i_{phl}}}$, as this also proved right yet for the DC-side balance control measure of type I.

The neg. seq. 2nd AC-side current harmonics i_{ph2} fulfil the expectations by now contributing with an almost constant negative DC-component $I_{0DC_{-}i_{ph2}}$ over the whole active operation mode range, as clearly shown in graphic b) of figure 8.5.

This negative DC-component $I_{0DC_i_{ph2}}$ will for the given decoupling inductance l=0.2[p.u.] be even larger than the opposite signed positive DC-component $I_{0DC_i_{ph1}}$. This is valid for the whole pure active operation mode range $-1 \le i_d' < 1$.

Hence, the sum of their impacts, $I_{0DC_i_{phl+2}}$, will for all values $-1 \le i_d' < 1$ always contribute with a negative DC-component in i_0 , as it is evident in graphic c) of figure 8.5. This is desirable, since now for all operation points a balancing DC-component can be introduced in i_0 . In addition, no zero crossing of $I_{0DC_i_{phl+2}}$ has to be taken into account, if a control will be designed.

However, it should be emphasized here, that a strongly varying AC-system impedance (or a larger decoupling inductance than l=0.2[p.u.) might cause the amplitude of i_{ph2} to decrease, which then would also yield a decrease in the corresponding DC-component $I_{0DC_i_{ph2}}$ of i_0 . As a consequence, $I_{0DC_i_{ph1+2}}$ might show up two zero crossings (symmetrical to $i_d' = 0$), which, if not detected and corrected by a sign reverse of e.g. the PI-controller, will cause a given DC-unbalance to increase instead to decrease.

Nevertheless, if this is guaranteed not to happen, the DC-side balance control measure of type II will have to be preferred to type I for the pure active operation mode range.

Finally, graphic c) of figure 8.5 also proves, that the higher ordered even and odd numbered AC-side current harmonics will have an additional amplifying influence on the resulting NP-current DC-component I_{0DC} . It could be observed in simulations, that almost exclusively the higher ordered even numbered harmonics, caused by the modification of the switching function s_{ph} , are responsible for this additional DC-component. This could also be

verified by a harmonic analysis, which here however will not be performed.

With that it can be concluded, that for a pure active operation mode, the impact of the DC-side balance control of type II (shifting corresponding pos. and neg. switching function pulses in opposite directions) depends on the following quantities:

- the magnitude of the DC-side balance control variable γ
- the amplitude of the pure active AC-side current fundamental i_{nh1} .
- the amplitude of the neg. seq. 2nd AC-side current harmonic, which is caused by the modification of s_{ph} and which
 - depends on the system impedance
 - might (slightly) depend on the 3-level VSI operation mode
- depends on the higher ordered even numbered AC-side current harmonics, caused by the modification of s_{ph}

This is true for at least FFM and off-line optimized PWM pulse patterns.

8.3.4 DC-side DC-balancing control of type II for pure reactive operation mode

Last but not least, the suitability of the DC-side balancing control of type II for a pure reactive operation mode will be investigated. In fact, this operation mode was the driving force for the derivation of this type II control measure and will now hopefully fulfil the expectations. The graphical results are presented in figure 8.6.

a) Influence of the AC-side current fundamental

In graphic a) of figure 8.6 it can clearly be seen that the AC-side current fundamental i_{a1} will now cause quite a large DC-component to arise in its contribution $i_{0,i_{a1}}$. Further, it is obvious that the magnitude of this DC-component $I_{0DC,i_{ab1}}$ will increase with increasing NP-control angles γ .

More, the high efficiency of the DC-side balancing control of type II for a pure reactive (here: capacitive) operation mode is underlined by the fact that small changes in the control variable γ yield maximum changes in the DC-component of $I_{0DC_i_{ph1}}$. This proves right, since the NP-current contribution $i_{0_i_{a1}}$ of i_{a1} consists of segments in the vicinity of its fundamental's peak-value, where changes in γ yield the most impressive changes in



Impact of the AC-side current fundamental $i_{a, b, c1}$

fig 8.6: DC-side balance control of type II (phase-displacement of the pos. and neg. pulses of the switching functions s_{ph} in opposite directions) and its impact on the NP-current i_0 for pure cap. operation mode (figure 5.2), r=0, l=0.2[p.u], $\beta=\pi/10$, $\gamma=0.2$ rad, see also table 8.1

 $I_{0DC_i_{ph1}}.$

Also the contributions $i_{0_{j_{ph1}}}$ of all three phases a,b,c in graphic b) of figure 8.6 confirm the above mentioned statements.

b) Influence of the negative sequence 2nd AC-side current harmonic

Regarding the impact of the neg. seq. 2nd AC-side harmonic i_{a2} , very similar results as for the pure active operation mode in subchapter b) of chapter 8.3.3 will be achieved.

Except of a slightly higher amplitude (due to a higher DC-side voltage u_{Dsum}), all other characteristics will remain the same.

Especially the phase-displacement of i_{a2} with respect to the fundamental of s_{ph} will not have changed since it does not depend on the operation mode. This was discussed yet in subchapter b) of chapter 8.3.3 and can be verified now by comparing the graphics c) of figure 8.4 and figure 8.6.

Therefore, all statements and considerations made in chapter 8.3.3 b), can also be applied here.

c) Dependancy on the pure reactive operation mode range

Finally, the dependancy of the described DC-side balance control measure of type II on the pure reactive operation mode range $(-1 \le i_q' < 1)$ will be studied with the MATLAB program. Hereby, the relationships in figure 8.6 correspond to $i_q' = 1$.

The particular arising DC-components $I_{0DC_i_{phl}}$, $I_{0DC_i_{ph2}}$ and $I_{0DC_i_{ph1+2}}$, caused by $i_{0_i_{ph1}}$, $i_{0_i_{ph2}}$ and their sum respectively, are presented in the upper three graphics d) - f) of figure 8.6

In addition, I_{0DC} , which coincides with the total DC-component of i_0 , is also included in graphic f) of figure 8.5.

Graphic d) in figure 8.5 shows that now both the magnitude and the sign of $I_{0DC_{i_{phl}}}$ (caused by i_{ph1}) depend on the pure reactive operation point. Further, for $i_{q'} = 0$, no balancing DC-component $I_{0DC_{i_{phl}}}$ will be present in $i_{0_{i_{phl}}}$.

The neg. seq. 2nd AC-side current harmonics i_{ph2} fulfil the expectations by now contributing with a negative DC-component $I_{0DC_{i_{ph2}}}$ over the whole

reactive operation mode range. This is clearly shown in graphic e) of figure 8.5.

Now however, their magnitude $I_{0DC_i_{ph2}}$ visibly depends on the pure reactive operation point. This is due to the fact that, for the here presumed constant modulation index m (FFM, $\beta = \pi/10$), the DC-side voltage u_{Dsum} will vary in a not negligible range, if the reactive AC-side current phasor component i_a' is varied between $-1 \le i_a' < 1$.

Therefore, as discussed yet in subchapter c) of chapter 8.3.3, also the DC-component $I_{0DC_{i_{ph2}}}$ (caused by i_{ph2}) will be subject to vary.

To proceed further, the resulting DC-component $I_{0DC_i_{phl+2}}$ (sum of both contributions $I_{0DC_i_{ph1}}$ and $I_{0DC_i_{ph2}}$) is presented in graphic f) of figure 8.5.

From this it is first of all obvious, that $I_{0DC_i_{phl+2}}$ shows up an undesirable zero crossing in between the nominal pure reactive operation mode range $0 \le i_q' < 1$. This zero crossing of $I_{0DC_i_{phl+2}}$, which for $I_{0DC_i_{phl}}$ could be found to correspond to the operation point $i_q' = 0$, has now been shifted into the pure capacitive operation mode range.

Further, in the vicinity of this zero crossing, an active DC-side balance controller of type II will show up a bad performance due to the very small DCcomponents $I_{0DC_ip_{hl+2}}$ introduced in the NP-current i_0 . Since the magnitude of the control variable γ is limited by the NP-angles (appendix B.3.3, eqn. (B.36)), this drawback cannot be compensated with an increase of γ .

In addition, a varying AC-system impedance might cause the amplitude of i_{ph2} to decrease/increase, which then would also yield a decrease/increase in the corresponding DC-component $I_{0DC_i_{ph2}}$ of i_0 . As a consequence, as well the zero crossing of $I_{0DC_i_{ph1+2}}$ will experience a varying shift towards the inductive/capacitive operation mode range.

More detailed studies concerning the dependancy of this critical operation point will be presented in chapter 8.4.2 b).

The latter mentioned two facts constitute a major challenge for a DC-side balance control scheme of type II. Especially the varying zero crossing of the resulting DC-component $I_{0DC-i_{phl+2}}$ will, if not detected and corrected

by a sign reverse of e.g. the PI-controller, cause a given DC-side unbalance to increase instead to decrease. Fortunately however, the DC-side unbalance will in this case increase with a moderate dynamic, since the magnitude of the DC-component $I_{0DC_i_{phl+2}}$ in the vicinity of its zero crossing will be small. Therefore, a zero crossing detection logic would probably not ask for very fast dynamic requirements, at least if the zero crossing range of $I_{0DC_i_{phl+2}}$ in a real application can be expected to be within reasonable small boundaries.

Another possible solution consists in the deactivation of the DC-side balance controller in the critical reactive operation mode range. This measure could be justified by the fact that the 3-level VSI is inherently self-balancing (chapter 7.4) and anyhow only a moderate performance of the DC-side balance controller can be expected in this critical reactive operation mode range.

With that it can be concluded, that for a pure reactive operation mode, the impact of the DC-side balance control of type II (shifting corresponding pos. and neg. switching function pulses in opposite directions) depends on the following quantities:

- the magnitude of the DC-side balance control variable γ
- the amplitude and the sign of the pure reactive AC-side current fundamental i_{ph1} .
- the amplitude of the neg. seq. 2nd AC-side current harmonic, which is caused by the modification of s_{ph} and which
 - · depends on the AC-system impedance
 - might depend on the 3-level VSI operation mode
- depends on the higher ordered even numbered AC-side current harmonics, caused by the modification of s_{ph} .

8.4 Control design for a SVC

The general investigations in the previous chapter focused on the inherent characteristics of two possible DC-side balance control measures for FFM modulation and off-line optimized pulse patterns. It could be shown, that the choice of the appropriate controller will depend on the operation mode of the 3-level VSI.

With regard to a SVC application (pure reactive operation mode), it became evident that exclusively the DC-side balance control of type II (shifting corresponding pos. and neg. switching function pulses in opposite directions) will be suitable as a DC-side balance control measure.

Basing on this DC-side balance control of type II, this chapter presents the fundamentals for the design of a DC-side balance control scheme, which then will be applied to a FFM modulated SVC with realistic system parameters.

8.4.1 Transfer functions for the DC-side balance control of type II

a) Transfer function for the contribution of the AC-side current fundamental

It could be seen in figure 8.6 (chapter 8.3.4), that in case of DC-side balance control of type II the fundamental of the AC-side currents i_{ph1} will contribute with a remarkable DC-component in the NP-current i_0 .

This effect must also mathematically be describable by means of a transfer function. Since the fundamental i_{ph1} of the AC-side currents i_{ph} will not appear (as a DC-component) in a d/q frame rotating with an angular velocity $-2\omega_1$, the transfer functions presented in chapter 7.5.1 (table 7.13), will not constitute the right choice.

For that purpose, one has to focus on an appropriate equation derived in a d/ q frame rotating with an angular velocity ω_1 .

In order to distinguish between the phasor components in the two different d/q frames (appendix C.2.1), the following notation will be used:

$\underline{x} = x';$	$x_d = x_d', x_q = x_q',$	if the d/q frame rotates with an angular velocity ω_1 ;
$\underline{x} = \underline{x}$ ";	$x_d = x_d^{"}, x_q = x_q^{"},$	if the d/q frame rotates with an angular velocity $-2\omega_1$;

The equation of interest is given by eqn. (E.9) (appendix E.1.2), which will here be presented once again according to eqn. (8.5).

$$\Delta u_{Ddiff}(s) = \frac{3}{2} \frac{I_{d0}'}{sc} \cdot \Delta s^2_{d}'(s) + \frac{3}{2} \frac{I_{q0}'}{sc} \cdot \Delta s^2_{q}'(s)$$
(8.5)

Basing on eqn. (8.5), the NP-current $\Delta i_{0_i phl}(s)$, generated by the fundamental components i_{phl} of the AC-side currents i_{ph} , can be expressed by eqn. (8.6).

$$\Delta i_{0_i_{phl}}(s) = -sc\Delta u_{Ddiff}(s) = -\frac{3}{2}I_{d0}' \cdot \Delta s^2_{d}'(s) - \frac{3}{2}I_{q0}' \cdot \Delta s^2_{q}'(s)$$
(8.6)

Herein, I_{d0}' and I_{q0}' are representing the phasor (DC-) components of the AC-side current fundamental i_{ph1} , while DC-components in $\Delta s^2_{d}'(s)$ and $\Delta s^2_{q}'(s)$ represent a fundamental in the squared switching functions s^2_{ph} .

On first sight, it might be astonishing, that the squared switching functions s_{ph}^2 contribute with a fundamental component, since they up to now were known to show up exclusively even numbered harmonics (table 4.2 in chapter 4.3.1, table 4.15 in chapter 4.4.1 and table 7.2 in chapter 7.3.1).

This however will be subject to change, if one of the two DC-side balance control measures of type I or type II is applied to the switching functions s_{ph} . Then, due to the generated neg. seq. 2nd harmonic in s_{ph} , also a fundamental component will arise in their squared quantities s_{ph}^2 , which causes a balancing DC-component to arise in u_{Ddiff} (eqn. (8.5)). Predominantly the convolution of the fundamental of s_{ph} with its 2nd harmonic counts responsible for this effect.

Now, the results achieved in the graphics a) and b) of figure 8.6 (and figure 8.3), are also confirmed by means of the appropriate transfer function (eqn. (8.6)).

Further, for a pure reactive operation mode and r=0, as assumed for the control design in this chapter, the active AC-side current phasor component I_{d0} equals to I_{d0} =0 and the transfer function eqn. (8.6) can be simplified to eqn. (8.7).

$$\Delta i_{0_{i_{phl}}}(s) = -\frac{3}{2}I_{q0}' \cdot \Delta s_{q}^{2}'(s)$$
(8.7)

b) Transfer function for the contribution of the neg. seq. 2nd AC-side current harmonic

Regarding the impact of the neg. seq. 2nd harmonic of the modified switching functions s_{ph} (graphic c) and d) in figure 8.6), the transfer functions introduced in chapter 7.5.1 (table 7.13 and table 7.14) are well suited to verify the graphical results. It should be recalled in mind, that these transfer functions, in opposite to the one described by eqn. (8.7), are referred to a d/q frame rotating with an angular velocity $-2\omega_1$.

For further investigations, the usually very small ohmic part r will be neglected, which results in eqn. (8.8).

$$\Delta u_{Ddiff}(s) = -\frac{3S_{q0}^{2} U_{Dsum0}\left(s + 2\omega_{1} \frac{S_{q0}^{2}}{S_{q0}^{2}}\right)}{den} \Delta s_{d}^{"}(s) \qquad (8.8)$$

$$-\frac{3S_{q0}^{2} U_{Dsum0}\left(s - 2\omega_{1} \frac{S_{q0}^{2}}{S_{q0}^{"}}\right)}{den} \Delta s_{q}^{"}(s) \qquad + \frac{6S_{d0}^{2} \left(s + 2\omega_{1} \frac{S_{q0}^{2}}{S_{q0}^{"}}\right)}{den} \Delta u_{Ld}^{"}(s) \qquad + \frac{6S_{q0}^{2} \left(s - 2\omega_{1} \frac{S_{q0}^{2}}{S_{q0}^{"}}\right)}{den} \Delta u_{Lq}^{"}(s)$$

$$den = 4lc \cdot s \cdot \left\{ s^2 + \left[\frac{3}{4lc} ((S^2_{d0})^2 + (S^2_{q0})^2) + 4\omega_1^2 \right] \right\}$$

With eqn. (8.8), the NP-current $\Delta i_{0_i_{ph2}}(s)$, representing the contribution of the neg. seq. 2nd harmonics i_{ph2} of the AC-side currents i_{ph} , is determined to eqn. (8.9).

$$\Delta i_{0,i_{ps2}}(s) = -s \cdot c \Delta u_{Ddiff}(s) = + \frac{3S^2_{d0} U_{Dsum0}(s + 2\omega_1 \frac{S^2_{d0}}{S^2_{d0}})}{den} \Delta s_d''(s) \quad (8.9)$$
$$+ \frac{3S^2_{q0} U_{Dsum0}(s - 2\omega_1 \frac{S^2_{d0}}{S^2_{q0}})}{den} \Delta s_q''(s)$$
$$- \frac{6S^2_{d0} (s + 2\omega_1 \frac{S^2_{q0}}{S^2_{d0}})}{den} \Delta u_{Ld}''(s)$$

. .

$$\frac{6S_{q0}^{2}"\left(s-2\omega_{1}\frac{S_{d0}^{2}"}{S_{q0}^{2}"}\right)}{den}\Delta u_{Lq}"(s)$$

$$den = 4l \cdot \left\{ s^2 + \left[\frac{3}{4lc} ((S^2_{d0})^2 + (S^2_{q0})^2) + 4\omega_1^2 \right] \right\}$$

Herein, for a pure reactive operation mode and r=0, the operation point phasor component S_{q0}^2 of the squared switching functions s_{ph}^2 will result to S_{q0}^2 =0.

This is due to the fact, that the fundamental of the switching function will be co-phasal to the d-component of the AC-system voltage phasor, which in its turn is synchronized with the d-axes of both d/q frames used in this work (angular velocities ω_1 and $-2\omega_1$). Since the neg. seq. 2nd harmonic of the squared switching functions s_{ph}^2 will also be cophasal with the fundamental of s_{ph} , their phasor q-component will equal to 0.

Further, the arising neg. seq. 2nd harmonic in s_{ph} , caused by the DC-side balance control measure of type II, will be lagging by $\pi/2$ to the switching function fundamental (subchapter b) of chapter 8.3.3).

Hence, exclusively the deviations $\Delta s_q''(s)$ will be unequal to 0 in eqn. (8.9), which means that the deviations $\Delta s_d''(s)$ do no longer have to be taken into account. It should be noted here, that applying the DC-side balance control measure of type I, would yield the opposite result ($\Delta s_q''(s) = 0$, $\Delta s_d''(s) \neq 0$).

Finally, with respect to the discussion to follow, the influence of the AC-system inductance will be taken into account by substituting the decoupling inductance l in the denumerator term of eqn. (8.9) by $l+l_L$ (l_L =AC-system inductance).

With that, for a pure reactive operation mode and assuming r=0, eqn. (8.9) can be simplified to eqn. (8.10).

$$\Delta i_{0_i_{ph2}}(s) = -\frac{6\omega_1 S^2_{d0} U_{Dsum0}}{den} \Delta s_q''(s) - \frac{6S^2_{d0} s_{d0}}{den} \Delta u_{Ld}''(s) + \frac{12\omega_1 S^2_{d0}}{den} \Delta u_{Lq}''(s)$$

$$den = 4(l+l_L) \cdot \left\{ s^2 + \left[\frac{3}{4(l+l_L)c} (S^2_{d0})^2 + 4\omega_1^2 \right] \right\}$$
(8.10)

Eqn. (8.10) describes the influence of a neg. seq. 2nd harmonic, either generated by the DC-side balance control of type II $(\Delta s_q''(s))$ or by the disturbance variables $\Delta u_{Ld}''(s)$ and $\Delta u_{Lq}''(s)$, on a DC-component in the NP-current for the pure reactive operation mode.

8.4.2 The critical operation point in dependancy on system parameters

a) Derivation of the equation for the critical operation point

When designing a DC-side balance control of type II, it will be highly desirable to know the critical operation point I_{q0crit} , where the generated DC-component in the NP-current i_0 will both equal to 0 (= reverses its sign). Further, the variation of this critical operation point I_{q0crit} in dependancy on varying system parameters should also mathematically be describable.

Therefore, basing on the transfer functions eqn. (8.7) and (8.10), an expression for the critical operation point I_{q0crit} will be derived in this chapter for the FFM modulated SVC.

For that purpose, the steady-state values of eqn. (8.7) and eqn. (8.10) will be calculated first. Replacing all Δx -quantities in eqn. (8.7) and eqn. (8.10) by corresponding steps $\Delta X/s$ and applying the final value theorem of the Laplace transform (eqn. (7.2) in chapter 7.4.1), yields eqn. (8.11) and eqn. (8.12).

$$\Delta i_{0_i_{phI}}(s \to 0) = I_{0DC_i_{phI}} = -\frac{3}{2}I_{q0}' \cdot \Delta S^2_{q'}$$
(8.11)

$$\Delta i_{0_{-i_{ph2}}}(s \to 0) = I_{0DC_{-i_{ph2}}} = -\frac{6\omega_1 S^2_{d0} U_{Dsum0}}{den} \Delta S_q'' \qquad (8.12)$$
$$-\frac{6S^2_{d0} \cdot 0}{den} \Delta U_{Ld}''$$
$$+\frac{12\omega_1 S^2_{d0}}{den} \Delta U_{Lq}''$$
$$den = \frac{3}{c} (S^2_{d0})^2 + 16\omega_1^2 (l+l_L)$$

From eqn. (8.12) it is evident, that for the pure reactive operation mode and

r=0, a disturbance ΔU_{Ld} " in the d-component of the AC-system voltage phasor (neg. seq. 2nd harmonic in the 3-phase plane), will not contribute with a DC-component in $I_{0_{-}i_{nk2}}$.

In a next step, the steady state values ΔS_q^2 (eqn. (8.11)) and $\Delta S_q^{"}$ (eqn. (8.12)) will be expressed by means of the DC-side balance control angle $\Delta \gamma$. The dependancy of these two quantities on γ cannot be described by a general relationship for all pulse patterns, but must be determined for a specific switching function.

For FFM modulation, these dependencies can be expressed by the simple eqn. (8.13) and eqn. (8.14).

$$\Delta S_q^2 = -\frac{4}{\pi} \cos\beta \sin(\Delta \gamma) \approx -\frac{4}{\pi} \cos\beta \cdot \Delta \gamma$$
(8.13)

$$\Delta S_{q}'' = \frac{2}{\pi} \sin 2\beta \sin (2 \cdot \Delta \gamma) \approx \frac{4}{\pi} \sin 2\beta \cdot \Delta \gamma \qquad (8.14)$$

- ΔS_q^2 : DC-component in a d/q frame rotating with ω_1 corresponding to a fundamental in s_{ph}^2
- ΔS_q ": DC-component in a d/q frame rotating with $-2\omega_1$ corresponding to a neg. seq. 2nd harmonic in s_{ph}

The relationship for ΔS_q^2 was derived with the help of the general fourier row eqn. (B.6) (appendix B.1.2) and figure B.7, while the equation for $\Delta S_q^{"}$ results from eqn. (B.28) (appendix B.2.3). In addition, the approximation $\sin \gamma \approx \gamma$, which is valid for realistic small values of γ has been taken into account. It should also be noted, that the negative sign in eqn. (8.13) contributes to the fact, that cophasal 3-phase quantities will show up opposite signed q-components in the two d/q frames rotating with an angular velocity ω_1 and $-2\omega_1$.

Further, it will be convenient for the following investigations to express the total DC-side voltage U_{Dsum0} in eqn. (8.12) in dependency on the steady state value I_{q0}' of the reactive AC-side current phasor component i_q' . According to the steady-state eqn. (D.16) in appendix D.2.2, U_{Dsum0} can be substituted by eqn. (8.15).

$$U_{Dsum0} = (U_{Ldo}' + \omega_1 II_{q0}') \cdot \frac{2}{S_{d0}'} = (U_{Ldo}' + \omega_1 II_{q0}') \cdot \frac{\pi}{2\cos\beta} \quad (8.15)$$

In addition, a correction factor $(1+\Delta h_{ev})$ will be defined for eqn. (8.12),

which takes the DC-contributions of the higher ordered even numbered harmonics into account. For a constant NP-angle β , as assumed here for the control of the SVC, this correction factor will be constant over the whole reactive operation mode range.

With that, the resulting DC-components in the NP-current for the FFM modulated SVC can be written according to eqn. (8.16) and eqn. (8.17).

$$I_{0DC_i_{phl}} = \frac{6}{\pi} I_{q0}' \cos\beta \cdot \Delta\gamma$$
(8.16)

$$I_{0DC_{-i_{ph2}}} = -(1 + \Delta h_{ev}) \cdot \frac{24\pi\omega_1 S^2_{d0}"\sin\beta(U_{Ldo}' + \omega_1 lI_{q0}')}{\pi \left[\frac{3}{c} (S^2_{d0}")^2 + 16\omega_1^2 (l + l_L)\right]} \cdot \Delta \gamma$$
(8.17)

Now eqn. (8.16) and eqn. (8.17) will be added to achieve the resulting DC-component I_{0DC} .

Hereby, the operation point phasor component S_{d0}^2 of s_{ph}^2 will be expressed by the FFM NP-angle β according to eqn. (8.18).

$$S_{d0}^{2} = \frac{2}{\pi} \cdot \sin 2\beta$$
 (8.18)

Eqn. (8.18) for S_{d0}^2 will be achieved from the general fourier row eqn. (B.14) in appendix B.1.4 for the squared FFM switching functions s_{ph}^2 .

This finally results to eqn. (8.19) in table 8.2 for the DC-component I_{0DC} of the NP-current i_0 , introduced by the DC-side balance control of type II. Additionally, the contribution from the disturbance variable ΔU_{Lq} " (neg. seq. 2nd harmonic in the 3-phase plane) has also been taken into account.

Though eqn. (8.19) does not look very inviting, it is nevertheless the basis for the calculation of the critical operation point I_{q0crit} in dependancy on all system parameters, which have an influence on this quantity.

Setting the numerator of the term depending on $\Delta\gamma$ to 0 and solving for I_{q0}' yields the desired eqn. (8.20) for I_{q0crit}' , which is also presented in table 8.2.

b) Discussion

Now it is possible to investigate the influence of the particular parameters, which have a more or less remarkable influence on this critical operation

$$I_{0DC} = \frac{6}{\pi} \omega_{1} \cos\beta \left\{ -(1+\Delta h_{ev}) U_{Ldo} \sin^{2}\beta + \left[\frac{3\sin^{2}(2\beta)}{4\pi^{2}\omega_{1}c} + \omega_{1}l \left(\cos^{2}\beta + \frac{l_{L}}{l} - \Delta h_{ev} \sin^{2}\beta \right) \right] I_{qo} \right\}}{\frac{3\sin^{2}(2\beta)}{4\pi^{2}\omega_{1}c} + \omega_{1}l \left(1 + \frac{l_{L}}{l} \right)} \Delta \gamma \frac{3\sin^{2}(2\beta)}{4\pi^{2}\omega_{1}c} + \omega_{1}l \left(1 + \frac{l_{L}}{l} \right)} + \frac{\frac{3}{2\pi} \sin^{2}\beta}{\frac{3\sin^{2}(2\beta)}{4\pi^{2}\omega_{1}c} + \omega_{1}l \left(1 + \frac{l_{L}}{l} \right)} \Delta U_{Lq}^{"}}$$

$$I_{q0Crit} = \frac{(1 + \Delta h_{ev})\sin^{2}\beta \cdot U_{Ldo}}{\frac{3\sin^{2}(2\beta)}{4\pi^{2}\omega_{1}c} + \omega_{1}l \left(\cos^{2}\beta + \frac{l_{L}}{l} - \Delta h_{ev}\sin^{2}\beta \right)} \qquad (8.20)$$
System parameters:
$$I: \quad \text{decoupling inductance, here: } I = 0.2[\text{p.u.}]$$

$$I_{L}: \quad \text{AC-system inductance, here: } I = 0.2[\text{p.u.}]$$

$$C: \quad \text{DC-side capacitor, here: } c = 3[\text{p.u.}], (c_{tot} = 1.5[\text{p.u.}], \tau_{c_{tot}} = 4.32\text{msec.})$$

$$\omega_{1}: \quad \text{fundamental frequency of the AC-system}$$

$$\beta: \quad \text{NP-angle of the FFM switching functions } s_{ph}, \text{ here: } \beta = \pi/10$$

$$\Delta h_{ev}: \text{ correction factor, contribution of the higher ordered even numbered harmonics of } s_{ph}; \text{ here: } \Delta h_{ev} = 0.65$$

$$\Delta Y: \quad \text{DC-side balance control angle (phase shift of the positive and negative switching function blocks in opposite directions)$$

$$\Delta U_{Lq}: \text{ disturbance variable, corresponding to a neg. seq. 2nd harmonic in the AC-system voltages u_{Lph}
Phasor quantities with respect to a d/q frame rotating with an angular velocity of the fundamental $\omega_{1}: I_{q0}$:
$$I_{q0}: \quad \text{q-component of the AC-system voltage phasor, here } U_{Ld0} = 1[\text{p.u.}]$$
table 8.2: equations for the resulting DC-component I_{0DC} of the NP-current i_{0} (introduced by the DC-side balance control of$$

current I_0 (introduced by the DC-side balance control of type II) and the critical operation point I_{q0crit} ($I_{0DC}=0$, sign reverse of I_{0DC}) for FFM modulation

point. For that purpose, a simulation has been performed, where these parameters have been varied in reasonable ranges.

The results are represented in figure 8.7. Herein, six parameters have been varied, which include the AC-system impedance (l_L) , the amplitude of the AC-system voltages (U_{Ld0}) , the decoupling inductance of the inverter (l), the NP-angle of the switching functions (β) , the DC-side capacitor (c) and the correction factor Δh_{ev} for the contribution of the higher ordered even numbered harmonics.

It can be seen from graphic a) in figure 8.7 that the AC-system impedance, which here is varied between $l_L=0$ (SCR = ∞) and $l_L=0.5$ (SCR = 2), has quite a strong influence on the location of I_{q0crit} . The weaker the AC-system, the closer the location of I_{q0crit} at $I_{q0crit}=0$. This dependency can be explained by the fact, that the contribution of the even numbered harmonics will shrink, if the strength of the AC-system decreases. Therefore, it would be highly desirable to know its exact value, which unfortunately is quite difficult to determine.

Also the AC-system voltage amplitude (graphic b) in figure 8.7) has a major impact on the value of I_{q0crit} . However, this parameter can be measured and with that I_{a0crit} can be adopted.

With respect to the decoupling inductance l in graphic c) of figure 8.7 it can be said, that it is theoretically possible to shift I_{q0crit} outside of the nominal operation mode range by choosing appropriate small values for l. However, taking into account realistic AC-system impedances, this will be subject to fail.

A very strong influence can be observed for the NP-angle β (graphic d) in figure 8.7), which for larger values than usually assumed here ($\beta = \pi/10$), will shift I_{q0crit} far outside of the operation mode range. On the other side, large NP-angles, which correspond to small modulation indices *m*, will not be realistic due to the moderate utilization of the inverter.

It should be noted at this point, that control schemes for asymmetrical operation conditions (e.g. AC-system faults) will ask for large and also asymmetrical NP-angles in order to counteract to these faults. This special case is not taken into account in eqn. (8.19). Therefore, during AC-system faults, it is proposed here, to switch the DC-side balance controller off. This will not constitute a major drawback, since these faults introduce only a moderate transient DC-unbalance (figure 7.5, chapter 7.5.3), which will decrease due to the 3-level VSI self-balancing attributes.



fig 8.7: Dependancy of the critical operation point I_{q0crit} (I_{0DC} =0, sign reverse of I_{0DC}) on different system parameters; system parameters, if not subject to be varied: c_{tot} =1.5[p.u.] or $\tau_{c_{tot}}$ =4.32ms, l=0.2[p.u.], l_L =0, r=0, $\beta = \pi/10$, Δh_{ev} =0.65

The influence of the DC-side capacitor size c_{tot} , shown in graphic e) of figure 8.7, will be small for reasonable large values $(c_{tot}>1.5[p.u.])$ or $\tau_{c_{tot}}>4.32ms$. In addition, this parameter is well known and therefore I_{q0crit} can be adopted.

Last but not least, the influence of the correction factor Δh_{ev} will be investigated. This correction factor itself strongly depends on the switching functions s_{ph} and can hardly be calculated. An approximation can be achieved with simulations (e.g. with the MATLAB program presented here). If a control scheme assumes the same switching function over the whole operation mode range, Δh_{ev} will be constant, otherwise it would have to be determined for the whole modulation index range. A wrong correction factor Δh_{ev} of a few percent will cause an error in the calculation of I_{q0crit} in the same range, as becomes evident in graphic f) of figure 8.7.

Finally, it should be noted that the ohmic system part r, which here for simplicity reasons was neglected, has only a really negligible influence (<0.01[p.u.]) on the location of I_{q0crit} for reasonable small values r (e.g. r=0.005[p.u.]). This could be verified in simulations with the MATLAB program introduced in chapter 8.3.1 c).

8.4.3 Closed loop control design for the FFM modulated SVC

This chapter describes the design of the DC-side balance control of type II for the FFM modulated SVC. A block diagram of the resulting control scheme is presented in figure 8.8.

a) Steady state characteristics of the DC-side balance control of type II for the SVC example

In figure 8.5, it could be seen that for a given constant control angle γ , the arising DC-component I_{0DC} in i_0 shows an almost linear dependancy on the operation point I_{q0}' with a zero-crossing in the capacitive operation mode. Hereby, the control angle γ in figure 8.5 has been chosen quite large in order to clearly demonstrate its impact.

In practical applications however, remarkable smaller values for γ will be applied in order not to influence the control of the AC-side current fundamental. Due to the fact, that the particular DC-components $I_{0DC_i_{ph1}}$ and $I_{0DC_i_{ph2}}$ will not be exactly proportional to γ , as can be verified e.g. in figure 8.6, also the zero crossing of their resulting DC-component I_{0DC} will be subject to change, if γ is remarkably changed. This can be clearly seen in



fig 8.8: Block diagram of the DC-side balance control of type II for the FFM modulated SVC, transfer functions see eqn. (8.19) $(G_{\Delta Y})$, eqn. (8.21) $(G_{fil_{\Delta u}D_{aij}}(s))$, eqn. (8.22) (PI-controller & adoption), eqn. (8.23) $(G_{ff_{-}DCbal})$, eqn. (8.24) $(G_{fil_{-}\Delta u_{L_{q}}}(s))$ and table 7.13, table 7.14 in chapter 7.5.1 $(G_{\Delta u_{L_{q}}}(s))$, $G_{\Delta u_{L_{q}}}(s)$)

figure 8.9, which shows the relationships for a practically realistic value of $\gamma=0.02$ [rad] and otherwise the same parameters as in figure 8.5, which coincide with those of the SVC example.



fig 8.9: NP-current DC-components $I_{0DC_i_{ph1}}$, $I_{0DC_i_{ph1}}$, $I_{0DC_i_{ph1}+2}$ and I_{0DC} caused by DC-side balance control of type II (figure 8.4, 8.6) in dependancy on the operation mode of the SVC, r=0.005, l=0.2[p.u], $\beta=\pi/10$, $\gamma=const=0.02rad$, see also table 8.1

It is evident from figure 8.9, that now the sign reverse of I_{0DC} has significantly moved very close to nominal capacitive operation, while those of $I_{0DC,i_{phI+2}}$ has only slightly been shifted into the capacitive region. Though the now achieved zero crossing of I_{0DC} might remain nearly unchanged for small values of γ , it all the same once more shows that the varying zero crossing of I_{0DC} constitutes a serious drawback of this control measure.

First of all, the validity of eqn. (8.20) will be verified by calculating the critical operation point I_{q0crit} . For the given system parameters (table 8.2) and neglecting the contributions of the higher ordered even numbered harmonics $(\Delta h_{ev}=0)$, I_{a0crit} results to

$$I_{q0crit} = 0.503$$
[p.u.]

Comparing this value with the value achieved in figure 8.9 c) for

 $I_{0DC_i_{ph1+2}}$, one can see an excellent agreement. In eqn. (8.20), also the size of the DC-side capacitor has been taken into account, which in the MAT-LAB simulations resulting to figure 8.9 had to be assumed to be infinite large. However, it should be noted, that the capacitor has only a small influence on the value of $I_{q0crit}' = 0.503$ [p.u.]. Calculating eqn. (8.20) for an infinite capacitor would give $I_{a0crit}' = 0.528$ [p.u.].

Also I_{0DC} , corresponding to the total resulting DC-component in the NPcurrent i_0 , was computed with a correction factor $\Delta h_{ev}=0.65$ [p.u.]. This value for Δh_{ev} was roughly determined with the help of the simulation presented in figure 8.9. With that I_{a0crit} increased to

$$I_{q0crit} = 0.90[p.u.],$$

which is as well in very good coincidence with the value achieved in graphic c) of figure 8.9.

b) Filter requirements

Unfortunately, the DC-component in u_{Ddiff} , which here constitutes the controlled variable, will usually be small compared to the superimposed 3rd harmonic oscillation. More, under asymmetrical operation conditions, u_{Ddiff} will in addition to that also contribute with a fundamental component (and higher ordered odd numbered harmonics), as shown in chapter 4.4.2 (table 4.20) and chapter 6.5 (figure 6.4III).

In order to design a proper control, these undesirable harmonics have to be filtered. It was found that for a capacitor size of $c_{tot}=1.5$ [p.u.] or $\tau_{c_{tot}}=4.32$ msec, as chosen for the SVC, a 2nd order Tschebyscheff low-pass filter (0.5 dB over-shoot) with a cutoff frequency $f_{cut}=22.5$ Hz ($f_{cut}=0.45$ [p.u.]) will fulfil the demands sufficiently. The transfer function of this filter is described in eqn. (8.21) and graphically represented in the block diagram in figure 8.8.

$$G_{fil_\Delta u_{Ddiff}}(s) = \frac{A_0 \omega_{cut}^2}{1.383 \cdot s^2 + 1.361 \omega_{cut} \cdot s + \omega_{cut}^2}$$
(8.21)
$$A_0 = 1; \qquad \omega_{cut} = 0.45[p.u.]$$

A design with notch filters yields an undesirable oscillatory dynamic, hence they have been avoided here. In addition, it could be seen, that they cannot increase the control speed remarkably, which more or less is limited by the system itself.

c) Controller

Since the system to be controlled roughly behaves like an integrator, a PIcontroller with a simple adoption to the operation point I_{q0} ' has been chosen.

It should be noted, that an exact dynamic transfer function, which takes into account both contributions of the AC-side current fundamental i_{ph1} and the neg. seq. 2nd harmonic i_{ph2} will be difficult to achieve. This is manifested in the fact, that their individual transfer functions are derived in different d/q planes rotating with ω_1 and $-2\omega_1$.

The adoption with respect to the operation point I_{q0}' has a linear characteristic and was derived with the help of figure 8.9 and some representative simulations with SABER. This also includes a sign reverse for $I_{q0}'>0.95[p.u.]$ and a deactivation of the PI-controller in the operation point range $0.85[p.u.] \le I_{q0}' \le 0.95[p.u.]$ and during AC-system faults in order to avoid an unstable control performance. A quantitative description is given in eqn. (8.22).

$$G_{PI}(s) = factor \cdot \frac{K_P \cdot s + K_I}{s}$$

$$K_P = 1[p.u.], K_I = 0.002[rad][p.u.]$$

$$factor = -(0.15 + I_{q0}' \cdot 0.1) \text{ for } -1[p.u.] \le I_{q0}' < 0.85[p.u.]$$

$$factor = 0 \qquad \text{for } 0.85[p.u.] \le I_{q0}' \le 0.95[p.u.]$$

$$factor = 0.35 - I_{q0}' \cdot 0.1 \qquad \text{for } 0.95[p.u.] < I_{q0}' \le 1[p.u.]$$

The PI-controller and its adoption/sign reverse is also graphically represented in figure 8.8.

d) Generation of the switching functions

The generation of the FFM switching functions for the DC-side balance control of type II is described in detail in appendix B.2.3. For convenience reasons, it will here at least graphically be explained by means of figure 8.10.



fig 8.10: Graphical generation principle of a 3-level VSI FFM switching function for NP-control of type II

Finally, it should be noted, that also off-line optimized PWM pulse patterns can be generated according to the same principle, as shown in appendix B.3.3. With that, the DC-side balance control of type II can also easily be transferred to off-line optimized modulation signals with higher switching frequencies.

8.4.4 Feed-forward controller for the FFM modulated SVC

The investigations in chapter 7.5.4 showed that a neg. seq. 2nd AC-system voltage harmonic constitutes the most powerful DC-unbalance source at all. This is also confirmed in the steady-state equations (eqn. (8.19)), where for $\Delta U_{Lq}" \neq 0$ (neg. seq. 2nd harmonic in u_{Lph}) an unbalance causing DC-component will arise in I_{0DC} . In order to compensate this serious unbalance source, an additional feed-forward controller will be included in the closed loop.

According to eqn. (8.19) in table 8.2, the condition given by eqn. (8.23) has to be fulfilled in order to compensate $(I_{0DC}=0)$ a disturbance generated by ΔU_{Lq} " (a neg. seq. 2nd harmonic in u_{Lph}).

This feed-forward controller is also graphically illustrated in the block dia-

$$\Delta \gamma_{ff} = -\frac{\sin\beta}{2\omega_1 \left\{ -(1 + \Delta h_{ev})U_{Ldo}' \sin^2\beta + \left[\frac{3\sin^2(2\beta)}{4\pi^2\omega_1 c} + \omega_1 l \left(\cos^2\beta + \frac{l_L}{l} - \Delta h_{ev} \sin^2\beta\right)\right] I_{q0}' \right\}} \Delta U_{Lq}''$$

$$\Delta \gamma_{ff} = G_{ff_DCbal} \cdot \Delta U_{Lq}''$$

gram in figure 8.8.

In practical applications, the disturbance variable ΔU_{Lq} " must also be filtered, since it will contribute with a 3rd harmonic in case of an AC-system voltage phase-shift or, even worse, with a fundamental component during asymmetrical AC-system conditions (e.g. line faults).

Further, it must not be excluded, that harmonics in the AC-system voltages u_{Lph} (5th, 7th,...) might be present, especially in weak AC-systems.

Therefore, ΔU_{Lq} will be filtered with a comb filter, which in the Laplacedomain can be written according to eqn. (8.24).

$$G_{fil_{\Delta u_{Lq}}}(s) = \frac{1 + e^{-0.5s}}{2}$$
(8.24)

8.4.5 Phased Locked Loop (PLL)

In order to synchronize the 3-level VSI phasor controls with the AC-system voltages and also to provide the arguments $\omega_1 t$ and $-2\omega_1 t$ for the d/q transforms, a Phased Lock Loop will be needed.

In this work, a PLL in the d/q phasor plane rotating with ω_1 is chosen, which is presented in figure 8.11.

This PLL synchronizes the 3-level VSI controls with the d-component of the AC-system voltage phasor u_{Ld}' by indirectly (via $atan(u_{Lq}'/u_{Ld}'))$ controlling its orthogonal q-component u_{Ld}' to zero.

In case that u_{Lq}' will not equal to 0 (atan $(u_{Lq}'/u_{Ld}') \neq 0$), the output variable Δf_1 (frequency deviation) of a PI-controller forces an integrator $(\omega t = \int 2\pi (f_1 + \Delta f_1)dt)$ to de- or increase the argument ωt for the trigonometric functions used in the d/q transform. As soon as ωt will coincide with the argument of the rotating AC-system voltage phasor $(u_L^2 = u_{L\alpha} + j \cdot u_{L\beta}, u_{Lq}')$ will equal to 0 and the PLL is locked. In order to avoid, that the rotating AC-system voltage phasor is locked to the negative value of u_{Ld}' , which





also would result in $u_{Lq'}=0$, the $atan(u_{Lq'}/u_{Ld'})$ is chosen as the control variable instead of $u_{Lq'}$.

The low-pass filter for $atan(u_{Lq}'/u_{Ld}')$ ensures, that for asymmetrical ACsystem conditions, the arising 2nd harmonic in u_{Ld}' and u_{Lq}' will not have an influence on the control. Hence, the resulting argument ωt will always be synchronized with the positive sequence fundamental component of the AC-system voltages and disturbances in u_{Lph} will not be transferred through the PLL.

8.4.6 Simulation results

In order to verify the results achieved so far and to assess the effectiveness of the proposed DC-side balance control measure, simulations have been performed with the SABER simulator tool. For that purpose, the control scheme discussed in the previous chapter has been implemented for the SVC with system parameters being the same as in table 8.2. The results are presented in figure 8.12 - figure 8.15.

a) Verification of the critical operation point

First of all the sign reverse, which was calculated in the previous chapter to $I_{q0crit}' = 0.9$ [p.u.] will be verified. This is done by deactivating the sign logic, which means that the DC-side balance control is expected to be unstable for operation points larger than $I_{q0crit}' = 0.9$ [p.u.]. Indeed, this is confirmed in figure 8.12 a) for the first 250ms, where the SVC works in the capacitive operation point $I_{q0}' = 0.95$ [p.u.]. After this time, a load step is applied from $I_{q0}' = 0.95$ [p.u.] to $I_{q0}' = 0.85$ [p.u.], which corresponds to quite a slow, but stable DC-side balance control.

b) DC-side balance controller response to load-steps

In figure 8.12 b) load-steps from $I_{q0}' = 0$ to $I_{q0}' = 1$ [p.u.] (at t=250ms) and then to $I_{q0}' = -1$ (at t=500ms) have been applied. When comparing the line diagram of the resulting (filtered) unbalance u_{Ddiff} with those in figure 7.4 (chapter 7.4.2) showing the self-balancing behaviour, it becomes evident that the DC-side balance controller remarkably reduces the balancing time constants. Factors of about 10 for the pure capacitive and even of about 50 for the pure inductive operation mode can be assumed to be realistic.

In addition, it is indicated by the small notch in the current phasor i_q' at about t=280ms, that the DC-side balance control angle γ must not be chosen



a): verification of the sign reverse in I_{0DC}

fig 8.12: a): verification of the sign reverse in the DC-component I_{0DC} of i_0 for DC-side balance control of type II; b): response of the DC-side balance controller to load-steps in the reactive AC-side current phasor component i_q ; r=0.005[p.u.], other SVC system parameters in table 8.2



a): step in Δu_{Id} "(s) of 0.02 [p.u.] at t=1sec.

fig 8.13: a): response of the DC-side balance controller to a step in $\Delta u_{Ld}''(s)$ of 0.02 [p.u.] (neg. seq. 2nd harmonics in u_{Lph} , cophasal to the fundamental); b): response to a steady state delay of 50µs in the switching instant of the upper valve in phase a; r=0.005[p.u.], other SVC system parameters in table 8.2



a): step in $\Delta u_{Lq}^{"}(s)$ of 0.02[p.u.] at t=1sec., feed-forward controller

off

fig 8.14: response of the DC-side balance controller to a step in $\Delta u_{Lq}''(s)$ of 0.02 [p.u.] (neg. seq. 2nd harmonics in u_{Lph} , phase-displaced by $\pi/2$ to the fundamental) with feed-forward controller deactivated (a)) and activated (b)); r=0.005[p.u.], $I_{q0}'=1$ [p.u.], other SVC system parameters in table 8.2



a): step in $\Delta u_{Lq}^{(s)}$ of 0.02 [p.u.] at t=1sec., feed-forward controller off

fig 8.15: response of the DC-side balance controller to a step in $\Delta u_{Lq}''(s)$ of 0.02 [p.u.] (neg. seq. 2nd harmonics in u_{Lph} , phase-displaced by $\pi/2$ to the fundamental) with feed-forward controller deactivated (a) and activated (b)); r=0.005[p.u.], $I_{a0}'=-1$ [p.u.], other SVC system parameters in table 8.2

to large in order to prevent an interaction with the control of the fundamental quantities.

c) DC-side balance controller response to a neg. seq. 2nd AC-system voltage harmonic, cophasal to the fundamental

The DC-side balance controller response to a neg. seq. 2nd AC-system voltage harmonic (ΔU_{Ld} "=0.02[p.u.]), which is cophasal to the fundamental of u_{Lph} , is presented in figure 8.13 a). For r=0, as shown in eqn. (8.12), this disturbance will not have an influence at all. Since here a realistic small ohmic part r=0.005[p.u.] is taken into account, also a small impact can be observed, which however does not constitute a major problem for the DCside balance controller. This proves right despite the fact that the SVC is operated in the nominal capacitive operation mode, where the DC-side balance controller performance is quite moderate.

However, without an active DC-side balance control implemented, things work out to become much more worse, as could be clearly shown in figure 7.6 of chapter 7.5.4.

d) DC-side balance controller response to a switching instant delay

The controller response to a steady-state switching instant delay of $50\mu s$ in phase *a* is given in figure 8.13 b). It is confirmed that the DC-side balance controller is well suited to counteract to this probably very frequent DC-unbalance source, even when operating in a range with moderate performance $(I_{a0}' = 1)$.

e) DC-side balance controller response to a neg. seq. 2nd AC-system voltage harmonic, phase-displaced by $\pi/2$ to the fundamental

The DC-side balance controller response to a neg. seq. 2nd AC-system voltage harmonic (ΔU_{Ld} "=0.02[p.u.]), which is phase-displaced by $\pi/2$ to the fundamental of u_{Lph} , is presented in figure 8.14 and figure 8.15.

The two figures differ from each other by the chosen operation point of the SVC, which equals to $I_{q0}' = 1$ in figure 8.14 and to $I_{q0}' = -1$ in figure 8.15. In addition, the graphics a) correspond to simulations, where the feed-forward controller is deactivated, while the graphics b) show the results with an activated feed-forward controller.

First of all, it is obvious, that the additional feed-forward controller fulfils quite a good job by transiently limiting the arising DC-side unbalance. This

proves right in both operation points $I_{q0}' = 1$ and $I_{q0}' = -1$. Further it is once again confirmed that the performance of the control scheme in the pure inductive operation mode will be better than in the high capacitive operation mode.

The small deviations between the feed-forward control angles γ_{ff} and the resulting steady-state NP-angle is manifested in the fact, that the correction factor $\Delta h_{ev} = 0.65$ obviously is slightly mis-tuned, which also yields a small error in γ_{ff} (eqn. (8.23)). It was found that $\Delta h_{ev} = 0.64$ constitutes the correct value for Δh_{ev} . Though the impact of this mis-tuning is not remarkable, it all the same shows the importance to determine Δh_{ev} with great care.

Further, it can be seen in figure 8.14 for $I_{q0}' = 1$, that the resulting DC-side balance control angle reaches quite large values of about 0.15[rad]. For a given NP-angle $\beta = \pi/10 = 0.314$ [rad], which constitutes the theoretical maximum for its resulting value (figure 8.10), this neg. sequence 2nd harmonic in u_{Lph} should roughly not exceed 0.04[p.u.]. Otherwise, in this operation point $I_{q0}' = 1$, the DC-side balance controller couldn't compensate its DC-component introduced in the NP-current i_0 .

Another very undesirable effect can be observed when having a closer look at the AC-side current phasor component i_q' in figure 8.14 for $I_{q0}' = 1$. Apparently, quite a large oscillation arises in i_q' , which was found to be predominantly determined by a neg. seq. 2nd harmonic in the 3-phase plane (3rd harmonic in i_q'). With an amplitude of more than 0.3[p.u.], it contributes with the lion's share, beside a pos. seq. 4th harmonic, which also shows up in the AC-side currents. On the other side, if not compensated, the neg. seq. 2nd harmonics in u_{Lph} of 0.02[p.u.] will for the given system parameters cause a corresponding AC-side current harmonic of at most 0.05[p.u.].

This neg. seq. 2nd harmonic will further not be generated by a resonance of the system (which is at about 84 Hz), but exclusively by the DC-side balance controller.

When focusing on figure 8.9, it becomes evident that for $I_{q0}' = 1$ quite a large DC-side balance control angle γ_{ff} will be necessary to compensate for the NP-current DC-component introduced by the neg. seq. 2nd harmonic in u_{Lph} . This is true, since the opposite signed contributions of the AC-side current fundamental i_{ph1} and the even numbered harmonics compensate each other to a large amount in the NP-current on the DC-side. Unfortunately, this will not prove right on the AC-side, where the large even numbered harmonics in the modified switching functions s_{ph} are the driving force for even larger even numbered AC-side current harmonics.

According to figure 8.9, the opposite has therefore to be expected in the in-
ductive operation range, which is clearly confirmed in the simulations presented in figure 8.15.

8.5 Summary

This chapter was dealing with DC-side balance control (in addition to the 3-level VSI self-balancing abilities).

In a first step, two possible DC-side balance control measures, which consist in appropriate modifications of the switching functions s_{ph} , have been introduced by means of graphical models. This was done with the simple FFM pulse patterns. In addition, the AC-side currents i_{ph} were exclusively represented by its fundamental i_{ph1} and a neg. seq. 2nd harmonic i_{ph2} .

The first control measure, which here was coined control measure of type I, modifies the switching functions s_{ph} by shortening the positive pulses, while simultaneously lengthening the negative ones, or vice versa.

It could be shown with the graphical model, that the DC-side balance control measure of type I is well suited for 3-level VSI applications, where an active power will be exchanged with the AC-system. However, if the 3-level VSI works in a pure reactive operation mode, this method fails.

It was further proved (assuming r=0), that exclusively the AC-side current fundamental i_{ph1} will be responsible for the arising DC-component in the NP-current i_0 , caused by the switching function's modification. A neg. seq. 2nd harmonic i_{ph2} (and its even numbered multiples), which are also caused by the switching function's modification, will not contribute with a DCcomponent in i_0 . More, if plotted over the whole pure active operation mode range $(-1 \le i_d' < 1)$, I_{0DC} will change its sign, if the direction of the active power transfer will be reversed (at $i_d'=0$).

The second control measure, which here was coined control measure of type II, modifies the switching functions s_{ph} by shifting corresponding pos. and neg. pulses in opposite directions, while simultaneously keeping their (equal) pulse lengths unchanged.

It could be shown with the graphical model, that the DC-side balance control measure of type II is well suited for all 3-level VSI applications, no matter of the operation mode.

It was further proved (assuming r=0), that both the AC-side current fundamental i_{ph1} and a neg. seq. 2nd harmonic i_{ph2} (and its even numbered multiples) will contribute with a DC-component to the NP-current i_0 . Also here, the neg. seq. 2nd harmonic i_{ph2} (and its even numbered multiples) are The resulting NP-current DC-component I_{0DC} for a given control angle γ will then be determined by the sum of both contributions. More, if plotted over the whole pure active or reactive operation mode range $(-1 \le i_d, i_q' < 1)$, I_{0DC} might change its sign, which has to be taken into account when designing a DC-side balance controller. Unfortunately, this zero crossing of I_{0DC} also depends on a varying AC-system impedance, which constitutes a drawback of this DC-side balance control measure of type II.

In a next step, the achieved graphical results have also mathematically been verified with the help of the transfer functions for the pure reactive operation mode by means of a SVC with realistic parameters.

Finally, in order to show the efficiency of the DC-side balance control measure of type II, a controller has been designed for a FFM modulated SVC. This controller includes a conventional closed loop with PI-controller for the controlled variable u_{Ddiff} and in addition a feed-forward controller for disturbances, being introduced by the AC-system voltages u_{Lph} . The control scheme was implemented in a SABER program.

The simulation results achieved with SABER once more confirmed the validity of the transfer functions and further showed, that an active DC-side balance control can improve the behaviour of the 3-level VSI during a DCside unbalance.

Concerning transient DC-side unbalance sources (load-steps in the controlled variable), a DC-side balance control yields control time constants, which are at least a factor of ten smaller than those achieved in the self-balancing studies. Also switching instant delays (here: $50\mu s$) will be controlled to 0 before they cause a remarkable DC-side unbalance.

With respect to the most critical steady state DC-side unbalance source, even numbered harmonics in the AC-system voltages (neg. seq. 2nd harmonic, pos. seq. 4th harmonic, etc.), the controller can limit their impact to quite small values of only a few percent. However, due to the limited range of the NP-control angle γ , these even numbered harmonics should not have larger amplitudes than 0.05[p.u.]. In addition, quite large neg. seq. 2nd harmonics appear in the AC-side currents i_{ph1} when applied in the higher capacitive operation range.

Therefore, and because of the undesirable and with the AC-system impedance varying sign reverse of the resulting balancing DC-component I_{0DC} , it must be concluded, that other or additional, more sophisticated control strategies will be highly desirable at least for disturbances introduced by the ACsystem.

9 Control of the SVC

9.1 Overview

This chapter is focusing on a basic AC-side current control scheme for the FFM modulated 3-level VSI SVC.

In a first step, the dynamic phasor transfer functions of the 3-level VSI SVC are presented, which also include the influence of dynamics in the AC-system voltages u_{Lph} .

Basing on these transfer functions, a conventional control loop will be designed for the reactive current phasor component i_q' . Simulations with MATLAB and SABER show a reasonable good performance for load-steps in the controlled variable i_q' . At disturbances in the AC-system voltages u_{Lph} however, the controller cannot sufficiently limit the peak-values of the AC-side currents.

Therefore, an additional feed-forward controller will be designed, which compensates the impact of these AC-system voltage disturbances in the AC-side currents. The efficiency and performance of the feed-forward control scheme will finally be verified by simulations with SABER.

9.2 Introduction

When focusing on the design of a control scheme for the 3-level VSI connected to an AC-system, the dynamic phasor transfer functions of the system might be of great value.

The chosen d/q frame for the transformation from the 3-phase to the phasor quantities will hereby rotate with the fundamental angular velocity ω_1 (k=1, appendix C.2.1). In order to distinguish the phasor components in this d/q frame from those in a d/q frame rotating with an angular velocity $-2\omega_1$ (k=-2, appendix C.2.1, chapter 7, chapter 8), the following notation will be used:

The dynamic phasor transfer functions in the Laplace domain are derived in appendix D.2 and appendix E.1 in a most general way and are valid for all 3-level VSI applications connected in shunt to an AC-system. Herein, also the influence of the AC-system voltages u_{Lph} and finite DC-side capacitors are taken into account.

In addition, the equations are presented in dependancy on two sets of control variables, namely the switching function phasor components $\Delta s_d'(s)$ and $\Delta s_a'(s)$ and also by their corresponding quantities $\Delta \phi_u(s)$ and $\Delta m(s)$.

In this thesis, the latter ones $(\Delta \phi_u(s) \text{ and } \Delta m(s))$, are chosen for the control design of a FFM modulated 3-level VSI SVC.

Further, the influence of the AC-system strength will not be taken into account for the design of the control schemes in this thesis. For that purpose, the reader is referred to e.g. [30]. Here, an infinite strong AC-system is assumed for the verification of the designed control schemes.

9.3 SVC current control loop design

In this chapter, a current control loop will be designed for the reactive ACside current phasor component i_a' of the 3-level VSI SVC.

This also includes studies concerning the influence of AC-system voltage disturbances (incl. asymmetrical operation conditions) on the performance of the controller. Hereby, the control design will be performed with the help of the dynamic transfer functions of the 3-level VSI SVC.

9.3.1 Transfer functions of the SVC

For reasons of convenience, the general transfer functions derived in appendix E.1 (eqn. (E.11), eqn. (E.13), eqn. (E.15) in table E.1 - table E.3) are once more presented in table 9.1 and table 9.2 for a SVC application. The individual parameters and phasor quantities herein are described in table 9.4. In addition, the 3-level VSI SVC model, which is taken as a basis for the derivation of the transfer functions, is given in figure 9.1.

Since the dynamic transfer functions do not look very inviting in its most general form $(r \neq 0)$, they will be simplified by assuming the resistive system part r=0, which for a SVC application coincides with the fact that the steady-state quantities I_{d0} and Φ_{u0} (table 9.4) will equal to 0. The resulting simplified SVC phasor equations are presented in table 9.3.

With respect to the closed loop controller design, the most general equations (table 9.1) have been used, while for the design of some parts of the feed-



fig 9.1: model of the 3-level VSI SVC for studies concerning dynamic system behaviour and control design

forward controller (chapter 9.4), the simplified ones (table 9.3) have been presumed.

9.3.2 Control loop design

a) Control principle

For the control of the pure reactive current phasor component i_q' of a 3-level VSI SVC, the control variable ϕ_u (phase angle between the AC-system voltages u_{Lph} and the 3-level VSI output voltages u_{ph}) constitutes a suited control quantity ([8], [62], [67] - [70]).

For a SVC application with a small ohmic system part ($r \approx 0.005$ [p.u.]), the steady-state operation point Φ_{u0} of ϕ_u is close to 0 and corresponds to a very small active AC-side current phasor component I_{d0} ', which exclusively covers the losses of the SVC. Hence, the 3-level VSI output voltage phasor \underline{u}' and the AC-system voltage phasor \underline{u}_L' are almost co-phasal for steady-state conditions. If the amplitude of the 3-level VSI output voltage phasor \underline{u}' is larger than those of the AC-system voltage phasor \underline{u}_L' , the SVC generates a pure reactive power (capacitive operation mode). In case that the 3-level VSI output voltage phasor \underline{u}' , the SVC absorbs a pure reactive power (inductive operation mode). This is graphically represented by means of the phasor diagram in figure 9.2.

Deviations $\Delta \phi_u(s)$ from its steady-state operation point Φ_{u0} will inherently cause a deviation $\Delta i_d'(s)$ in the active current phasor component $i_d'(s)$,

$\Delta i_{a'}(s) = \frac{-(2\omega_{1}lcM_{0}U_{Dsum0} + 31M_{0}^{2}I_{q0'}) \cdot s + 3M_{0}^{2}[1/2M_{0}\Phi_{u0}U_{Dsum0} - I_{q0'}(r + \omega_{1}!\Phi_{u0})]}{den}\Delta \phi_{u}(s) $ (((9.1)
$-\frac{lcU_{Dsum0} \cdot s^2 + [(r+\omega_1 l\Phi_{u0}) cU_{Dsum0} + 3/2 lM_0 (I_{a0}' + \Phi_{u0} I_{q0}')] \cdot s + 3/2 M_0 (r+\omega_1 l\Phi_{u0}) (I_{a0}' + \Phi_{u0} I_{q0}')}{den} \Delta m(s)$	
$+ \frac{4lc \cdot s^2 + 4rc \cdot s + 3M_0^2 \Phi_{u0}^2}{den} \Delta u_{Ld}(s) + \frac{4\omega_1 lc \cdot s - 3M_0^2 \Phi_{u0}}{den} \Delta u_{Lq}(s)$	
$\Delta i_d'(s) = G_{\Delta i_d' - \Delta \phi_u}(s) \cdot \Delta \phi_u(s) + G_{\Delta i_d' - \Delta m}(s) \cdot \Delta m(s) + G_{\Delta i_d' - \Delta u_{L_d}}(s) \cdot \Delta u_{L_d}(s) + G_{\Delta i_d' - \Delta u_{L_d}}(s) \cdot \Delta u_{L_d}(s) $	(9.2)
$\Delta i_q^{*}(s) = \frac{-2lcM_0U_{Dsum0} \cdot s^2 - (2rcM_0U_{Dsum0} + 3lM_0^2 I_{q0}^{*} \Phi_{u0}) \cdot s - 3M_0^2 [1/2M_0U_{Dsum0} + I_{q0}^{*} (r\Phi_{u0} - \omega_1 I)]}{den} \Delta \phi_u(s) $ (6)	(9.3)
$-\frac{2^{lcU_{Dsum0}\Phi_{u0}\cdot s^{2}+[cU_{Dsum0}(r\Phi_{u0}-\omega_{1}l)+3/21M_{0}\Phi_{u0}(I_{a0}^{}+\Phi_{u0}I_{q0}^{})]\cdot s+3/2M_{0}(r\Phi_{u0}-\omega_{1}l)(I_{a0}^{}+I_{q0}^{}\Phi_{u0}^{})}{den}$	کاس(s)
$-\frac{4\omega_1 lc \cdot s + 3M_0^2 \Phi_{u0}}{den} \Delta u_{Ld}(s) + \frac{4 lc \cdot s^2 + 4 rc \cdot s + 3M_0^2}{den} \Delta u_{Lq}(s)$	
$\Delta i_q^{\prime}(s) = G_{\Delta i_{q-}^{\prime}\Delta \phi_u}(s) \cdot \Delta \phi_u(s) + G_{\Delta i_{q-}^{\prime}\Delta m}(s) \cdot \Delta m(s) + G_{\Delta i_{q-}^{\prime}\Delta u_{Ld}^{\prime}}(s) \cdot \Delta u_{Ld}^{\prime}(s) + G_{\Delta i_{q-}^{\prime}\Delta u_{Ld}^{\prime}}(s) \cdot \Delta u_{Ld}^{\prime}(s)$	(9.4)
$den = 4l^2 c \left\{ s^3 + 2\frac{r}{l} \cdot s^2 + \left[\frac{3}{4lc} M_0^2 (1 + \Phi_{u0}^2) + \left(\frac{r^2}{l^2} + \omega_1^2 \right) \right] \cdot s + \frac{3r}{4l^2 c} M_0^2 (1 + \Phi_{u0}^2) \right\}$	(9.5)
table 9.1: general transfer functions $(r \neq 0)$ for the 3-level VSI SVC $(\Delta i_d'(s), \Delta i_q'(s))$ in dependancy on control variables $\Delta \phi_1(s), \Delta m(s)$ and the disturbance variables Δu_2 . $I(s), \Delta u_2, I(s), \Delta u_3$ frame rough the disturbance variables Δu_2 . $I(s), \Delta u_3, I(s), \Delta u_3$	on the



	$3M_{0}[2l^{2}I_{n0},s^{2}+(4rlI_{n0},-lM_{0}\Phi_{n0}U_{n,m,n})\cdot s+2I_{n0}(r^{2}+\omega_{0}^{2}l^{2})-M_{0}U_{Dsum0}(r\Phi_{n0}+\omega_{1}l)]$	
$\Delta u_{Dsum}(s) =$	$\frac{1}{2}$	(0.4)
+	$ \begin{array}{l} & & & & & & & & & & & & & & & & & & &$	m(s
+ 6M 0[$\frac{l\cdot s + (r - \omega_1 l \Phi_{u0})}{den} \Delta u_{Ld}(s) + \frac{6M_0 [l \Phi_{u0} \cdot s + (r \Phi_{u0} + \omega_1 l)]}{den} \Delta u_{Lq}(s)$	
	$den = 4l^2 c \left\{ s^3 + 2\frac{r}{l} \cdot s^2 + \left[\frac{3}{4lc} M_0^2 (1 + \Phi_{u0}^2) + \left(\frac{r^2}{l^2} + \omega_1^2 \right) \right] \cdot s + \frac{3r}{4l^2 c} M_0^2 (1 + \Phi_{u0}^2) \right\}$	(7.6)
$\Delta u_{Dsum}(s) =$	$\mathcal{G}_{\lambda u_{D_{1em}}-\Delta \phi_{u}}(s) \cdot \Delta \phi_{u}(s) + G_{\Delta u_{D_{1em}}-\Delta m}(s) \cdot \Delta m(s) + G_{\Delta u_{D_{1em}}-\Delta u_{L_{d}}}(s) \cdot \Delta u_{L_{d}}(s) + G_{\Delta u_{D_{1em}}-\Delta u_{L_{q}}}(s) \cdot \Delta u_{L_{d}}(s)$	(9.8)
table 9.2:	general transfer function $(r \neq 0)$ for the 3-level VSI SVC DC-side voltage $\Delta u_{Dsum}(s)$ in depende on the control variables $\Delta \phi_u(s)$, $\Delta m(s)$ and the disturbance variables $\Delta u_{Ld}(s)$, $\Delta u_{Lq}(s)$, d/q fr rotating with an angular velocity ω_1 ($k=1$), description of the quantities in table 9.4	ancy ame

(9.11)	$+ \frac{\frac{3IM_0UD_{sum0} \cdot s}{den}}{\frac{den}{den}\Delta u_{Lq}(s)}$	$D_{zum}(s) = \frac{3IM_0[2II_{q0}^{\circ} \cdot s^2 + \omega_1(2\omega_1II_{q0}^{\circ} - M_0UD_{sum0})]}{den} \Delta \phi_u(s) + \frac{6IM_0 \cdot s}{den} \Delta u_{Ld}(s)$ $den = 4I^2 c \cdot s \cdot \left\{ s^2 + \left[\omega_1^2 + \frac{3M_0^2}{4ic} \right] \right\}$
(9.11)	$\frac{3IM_0U_{D_{stund}}\cdot s}{den}\Delta m(s)$	$D_{5um}(s) = \frac{3IM_0[2II_{q0} \cdot s^2 + \omega_1(2\omega_1II_{q0} - M_0U_{5um0})]}{den} \Delta \phi_u(s)$
	$+ \frac{4lc \cdot s^2 + 3M_0^2}{den} \Delta u_{Lq}(s)$	$-\frac{4\omega_1lc\cdot s}{den}\Delta u_{Ld}(s)$
(9.10)	$+ \frac{2\omega_1 lc U_{D_{2um0}} \cdot s}{den} \Delta m(s)$	$I_{1}^{\prime}(s) = -\frac{2lcM_{0}U_{Dsum0} \cdot s^{2} + 3M_{0}^{2}(1/2M_{0}U_{Dsum0} - \omega_{1}lI_{q0})}{den}\Delta\phi_{u}(s)$
	$+ \frac{4\omega_1 lc \cdot s}{den} \Delta u_{Lq}(s)$	$+\frac{4lc\cdot s^2}{den}\Delta u_{Ld}(s)$
(6.9)	$\frac{2lcU_{Dsum0}\cdot s^2}{den}\Delta m(s)$	$h'(s) = -\frac{l(2\omega_1 c M_0 U D_{sum0} + 3M_0^2 I_{q0}) \cdot s}{den} \Delta \phi_u(s)$

 $\Delta \phi_u(s)$, $\Delta m(s)$ and the disturbance variables $\Delta u_{Ld}(s)$, $\Delta u_{Lq}(s)$, d/q frame rotating with an angular velocity ω_1 (k=1), description of the quantities in table 9.4

System parameters:

- r: ohmic part of the system; here: r=0.005[p.u.];
- *l*; stray reactance of the transformer; here: *l*=0.2[p.u.];
- c: 3-level VSI DC-side capacitors; here: $c_{tot} = c/2 = 1.5$ [p.u.], $\tau_{c_{rot}} = 4.32$ ms;

 ω_1 : fundamental frequency of the AC-system;

AC-side phasor quantities with respect to a d/q frame rotating with an angular velocity of the fundamental ω_1 :

I _{d0} ':	steady-state operation point of the d-component of the AC-side current phasor	
I _{q0} ':	steady-state operation point of the q-component of the AC-side current phasor	
Φ _{μ0} :	steady-state phase angle between the AC-system voltage phasor and the 3-level VSI SVC output voltage phasor	
M ₀ :	steady state modulation index of the switching functions s_{ph} ; here: $M_0 = 4/\pi \cdot \cos\beta = 4/\pi \cdot \cos(\pi/10) = 1.2109$;	
$\Delta i_d'(s)$:	deviations from I_{d0}	
$\Delta i_q'(s)$:	deviations from I_{q0}	
$\Delta \phi_u(s)$:	deviations from Φ_{u0}	
$\Delta m(s)$:	deviations from M_0	
$\Delta u_{Ld}'(s)$:	deviations in the d-component of the AC-system voltage phasor	
$\Delta u_{Lq}'(s)$:	deviations in the q-component of the AC-system voltage phasor	
DC-side quantities:		
U_{Dsum0} :	steady-state total 3-level VSI DC-side voltage	
$\Delta u_{Dsum}(s)$: deviations from U_{Dsum0}	

table 9.4: Quantities in the 3-level VSI SVC phasor transfer functions (table 9.1 - table 9.3)



fig 9.2: Phasor diagrams for the 3-level VSI SVC in the capacitive and inductive operation mode; \underline{u}' : 3-level VSI output voltage phasor; \underline{u}_L' : AC-system voltage phasor; \underline{u}_Z' : voltage phasor across the decoupling impedance; see also figure 9.1

which in its turn, depending on the sign of $\Delta i_d'(s)$ (of $\Delta \phi_u(s)$), will charge or discharge the DC-side capacitors. As a consequence, presuming a fixed modulation index for the switching functions s_{ph} , the amplitude of the 3level VSI output voltage phasor \underline{u}' will also increase or decrease. According to the phasor diagram in figure 9.2, also the voltage phasor across the decoupling impedance will change and with that the reactive current phasor component i_a' .

The control via exclusively the other control variable m(s) is not suitable at all, since in the presence of a resistive system part $r \neq 0$, only negligible changes in $\Delta i_q(s)$ can be achieved without the additional help of the other control variable $\phi_u(s)$. This can be verified by applying the final value theorem of the Laplace transform to $G_{\Delta i_q'-\Delta m}$ in eqn. (9.3) (table 9.1) and is also in good agreement with physical considerations.

b) Bode diagrams of the controlled system

The bode diagrams of the controlled system $G_{\Delta i_q' - \Delta \phi_u}(s)$ for three different steady state operation points $I_{a0}'=1, 0, -1$ [p.u.] are presented in figure 9.3.





fig 9.3: Bode diagrams of the 3-level VSI SVC transfer function $G_{\Delta i_{q'}-\Delta \phi_{u}}(s)$ for different operation points I_{q0} ', see also table 9.1

An in depth discussion of these transfer functions has been performed yet in [8], [62], [67] - [70] for the 2-level VSI SVC. Since the results are also valid for the 3-level VSI, the reader is referred to the literature.

The undesirable system resonance ω_{res} for the here investigated 3-level VSI SVC can be calculated from the denumerator term (eqn. (9.12)) of the simplified transfer functions (table 9.3) which results to eqn. (9.13).

$$\omega_{res} = \sqrt{\omega_1^2 + \frac{3M_0^2}{4lc}} = 1.68 \text{ [p.u.]}$$
(9.13)

c) Filter for the reactive current phasor component

The reactive current phasor component i_q' should be filtered, since it predominantly shows up a 6th harmonic, which results from the 7th AC-side current harmonic in the 3-phase plane. In addition, during asymmetrical operation conditions, a 2nd harmonic appears in i_q' , which mainly has its origin in the neg. seq. fundamental component arising in the AC-side currents in the 3-phase plane.

Unfortunately, filtering the latter mentioned 2nd harmonic highly increases the risk for an unstable control loop, since the phase of the open loop transfer function in the vicinity of the resonance ω_{res} might take on values larger than π . This will prove right for both low-pass and also notch- or comb-filters. Therefore, the filtering of this 2nd harmonic has to be renounced here and its impact on the reactive current control during asymmetrical operation conditions has to be tolerated.

For the filtering of the 6th harmonic in i_q' , a 2nd order Tschebyscheff filter (0.5 dB over-shoot) with a cutoff frequency $f_{cut}=200$ Hz ($f_{cut}=4$ [p.u.]) will fulfil the demands sufficiently. The transfer function of this filter is described by eqn. (9.14).

$$G_{fil_\Delta i_{q}}(s) = \frac{A_{0}\omega_{cut}^{2}}{1.383 \cdot s^{2} + 1.361\omega_{cut} \cdot s + \omega_{cut}^{2}}$$

$$A_{0} = 1; \qquad \omega_{cut} = 4[p.u.]$$
(9.14)

d) PI-controller

In order to close the open loop, a simple PI-controller was found to show a reasonable dynamic for the basic investigations performed here. The chosen

values for the amplification K_P and the integral part K_I of the PI-controller constitute a compromise between a still acceptable resulting dynamic for i_q' and a still moderate excitation of the resonance frequency. Its transfer function and the quantitative values for K_P and K_I are given in eqn. (9.15).

$$G_{PI}(s) = \frac{K_P \cdot s + K_I}{s}$$

$$K_P = 0.087 [rad]/[p.u.], K_I = 0.0028 [rad]/[p.u.]$$
(9.15)

With that, the open loop transfer functions

$$G_{\Delta i_{q}'-ol}(s) = G_{Pl}(s) \cdot G_{\Delta i_{q}'-\Delta \phi_{u}}(s) \cdot G_{fil_{\Delta i_{q}'}}(s)$$
(9.16)

in the 3 different steady-state operation points I_{q0} '=1, 0, -1[p.u.] result to those presented in figure 9.4. A block diagram of the control scheme, also including a feed-forward controller (chapter 9.4), is given in figure 9.5.

e) Step responses of the closed loop

In order to basically assess the performance of the designed control scheme, steps have been applied for the controlled variable Δi_q of 1[p.u.] and for the disturbance variables Δu_{Lq} and Δu_{Lq} of 0.25[p.u.]. The results for the 3 steady-state operation points I_{a0} =1, 0, -1[p.u.] are shown in figure 9.6.

From this, it can be concluded that the performance of the designed controller is quite acceptable for a step in the controlled variable i_q' , however very bad if disturbances occur in the AC-system voltage phasor components $u_{Ld'}$ and $u_{Lq'}$.

Hence, an additional control measure, suitable to counteract against these disturbances, will be highly desirable.

9.3.3 Simulation results of the 3-level VSI SVC

In order to also verify the controller performance in a more realistic manner, simulations with SABER have been performed for the 3-level VSI SVC.

In accordance to figure 9.6, these simulations present the dynamics of the controlled variable i_q' after steps in the controlled variable i_q' itself and after steps in the disturbance variables $u_{Ld'}$ and $u_{Lq'}$. In addition, simulations have been performed for asymmetrical operation conditions, which are



Block diagram of the control for the 3-level VSI SVC, transfer functions see eqn. (9.14) $(G_{fil_{\Delta l_q}}(s))$, eqn. (9.15) (Pl-controller), eqn. (9.3) $(G_{\Delta l_{q'}^{-}\Delta \phi_{u}}(s), G_{\Delta l_{q'}^{-}\Delta u_{L_{d'}}}(s), G_{\Delta l_{q'}^{-}\Delta u_{L_{d'}}}(s))$, dqframe rotating with an angular velocity ω_1 fig 9.5:



fig 9.4: Bode diagrams of the 3-level VSI SVC open loop transfer function $G_{\Delta i_q'-ol}(s)$ for different operation points I_{q0}' , control via the phase angle ϕ_u between the 3-level VSI output voltages and the AC-system voltages



fig 9.6: Responses of the controlled variable i_q' to steps in the controlled variable i_q' itself (1 [p.u.]) and the disturbance variables $u_{Ld'}$ and $u_{Lq'}$ (0.25[p.u.]) for different operation points $I_{q0'}$, control via the phase angle ϕ_u between the 3level VSI output voltages and the AC-system voltages

caused by a large single line AC-system voltage drop in phase a of 0.75[p.u.].

With respect to disturbances in the AC-system voltage phasor component u_{Lq}' (AC-system voltage phase shifts) and to asymmetrical operation conditions, also the influence of the PLL (chapter 8.4.5, figure 8.11) has been investigated. The simulation results, showing the most important quantities, are presented in figure 9.7I - figure 9.13II.

a) Controller response to load-steps in i_a'

Regarding the behaviour of the SVC in case of load-steps in i_q' (figure 9.7I, figure 9.7II) it can be concluded, that very similar results are achieved as presented in figure 9.6.

b) Controller response to 3-phase voltage drops

Also during disturbances in u_{Ld} (3-phase AC-system voltage drops, figure 9.8I and figure 9.8II), the 3-level VSI SVC shows the same response as in figure 9.6 for the nominal capacitive operation point I_{q0} =1[p.u.]. Hereby 3-phase voltage drops in the AC-system voltages of $\Delta U_{Ld} = \mp 0.25$ [p.u.] at t=105ms and t=305ms respectively have been simulated.

c) Controller response to AC-system voltage phase shifts

For AC-system voltage phase shifts (disturbances in u_{Lq}), the results strongly depend on the adjustment of the PLL (chapter 8.4.5, figure 8.11).

With an very slow tuned PLL (step response time ca. 15 sec.), a step in u_{Lq} of $\Delta U_{Lq}'=\pm 0.25$ [p.u.] causes very high over-currents on the AC-side when the disturbance occurs at t=105ms (figure 9.9I, graphic d)-f)). At t=305ms, when a reverse step ($\Delta U_{Lq}'=-0.25$ [p.u.]) is applied, no over-currents can be observed. However, as can be clearly seen in the filtered reactive AC-side current phasor component i_{qfil} (figure 9.9I g)), the SVC now reverses its operation point into the inductive operation mode.

The same simulation with a very fast tuned PLL (step response time ca. 2ms.) shows remarkably better dynamics (figure 9.10I, figure 9.10II). No high over-currents can be observed both at t=105ms and t=305ms when the AC-system voltage phase shifts (ΔU_{La} '=±0.25[p.u.]) occur.

While the specific influence of the PLL tuning could be foreseen for this



fig 9.7I: response of the 3-level VSI SVC to steps in the controlled variable i_q' (at t=50ms, 150ms, 250ms, 400ms): a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfil}'



fig 9.7II: response of the 3-level VSI SVC to steps in the controlled variable i_q' (at t=50ms, 150ms, 250ms, 400ms): a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.8I: response of the 3-level VSI SVC to 3-phase voltage drops in u_{Lph} of 0.25[p.u.] ($\Delta u_{Ld}'=\mp 0.25$ [p.u.] at t=105ms and reverse at t=305ms, graphic a)-c)): a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfil}'



fig 9.8II: response of the 3-level VSI SVC to 3-phase voltage drops in u_{Lph} of 0.25[p.u.] (Δu_{Ld} '= \mp 0.25[p.u.] at t=105ms and reverse at t=305ms): a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.9I: response of the 3-level VSI SVC to AC-system voltage phase-shifts ($\Delta u_{Lq}'=\pm 0.25$ [p.u.] at t=105ms and reverse at t=305ms, graphic a)-c)), very slow PLL (step response time ca. 15 sec.): a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfi} '



fig 9.9II: response of the 3-level VSI SVC to AC-system voltage phase-shifts ($\Delta u_{Lq}' = \pm 0.25$ [p.u.] at t=105ms and reverse at t=305ms), very slow PLL (step response time ca. 15 sec.): a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.10I: response of the 3-level VSI SVC to AC-system voltage phase-shifts ($\Delta u_{Lq}'=\pm 0.25$ [p.u.] at t=105ms and reverse at t=305ms, graphic a)-c)), very fast PLL (step response time ca. 2ms.): a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfi}



fig 9.10II: response of the 3-level VSI SVC to AC-system voltage phase-shifts ($\Delta u_{Lq}' = \pm 0.25$ [p.u.] at t=105ms and reverse at t=305ms), very fast PLL (step response time ca. 2ms.): a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.11I: response of the 3-level VSI SVC to an AC-system voltage drop in phase *a* of 0.75[p.u.] (at t=105ms and cleared at t=305ms, graphic a)-c)), very slow PLL (step response time ca. 15 sec.), a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfi}



fig 9.11II: response of the 3-level VSI SVC to an AC-system voltage drop in phase *a* of 0.75[p.u.] (at t=105ms and cleared at t=305ms), very slow PLL (step response time ca. 15 sec.), a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.12I: response of the 3-level VSI SVC to an AC-system voltage drop in phase *a* of 0.75[p.u.] (at t=105ms and cleared at t=305ms, graphic a)-c)), very fast PLL (step response time ca. 2ms.), a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfil}



fig 9.12II: response of the 3-level VSI SVC to an AC-system voltage drop in phase *a* of 0.75[p.u.] (at t=105ms and cleared at t=305ms), very fast PLL (step response time ca. 2ms.), a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.13I: response of the 3-level VSI SVC to an AC-system voltage drop in phase *a* of 0.75[p.u.] (at t=105ms and cleared at t=305ms, graphic a)-c)), very fast PLL (step response time ca. 2ms.), a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{afil}



fig 9.13II: response of the 3-level VSI SVC to an AC-system voltage drop in phase *a* of 0.75[p.u.] (at t=105ms and cleared at t=305ms), very fast PLL (step response time ca. 2ms.), a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}

simulation (AC-system voltage phase shifts), the relationships become more complicated in case of asymmetrical operation conditions.

d) Controller response to single phase AC-system faults

In case of single phase AC-system faults (in general: at asymmetrical AC-system voltages), the phasor components u_{Ld} and u_{Lq} of the AC-system voltages contribute with a 2nd harmonic.

A very fast tuned PLL (step response time ca. 2ms.) will then also see a remarkable 2nd harmonic in its control signal. This proves right, since the low-pass filter in the PLL control-loop (chapter 8.4.5, figure 8.11) will have a high cut-off frequency in order to guarantee a fast step response.

As a consequence, the reference signals for the d/q transform won't show up a pure sinusoidal shape, which in its turn will influence the control scheme. At least on first sight, this will for sure be highly undesirable.

In opposite, a very slow tuned PLL (step response time ca. 15sec.) will not be influenced by the 2nd harmonic in u_{Ld} and u_{Lq} , which will now sufficiently be damped by a very low cut-off frequency of the low-pass filter in its control-loop.

The impact of these two different PLL tunings can be verified in figure 9.11I - figure 9.13II for a single line AC-system voltage drop in phase a of 0.75[p.u.].

In figure 9.11I and figure 9.11II, the PLL is tuned to be very slow, which results in remarkable asymmetrical over-currents on the AC-side with amplitudes up to 5[p.u.] (graphics d) - f) in figure 9.11I). Also the DC-side voltages u_{D1} and u_{D2} (graphic e) and f) in figure 9.11II) show up very large oscillations (fundamental component and 2nd harmonic).

For a very fast PLL and a nominal capacitive operation mode $(I_{q0}'=1[p.u.])$, a much better system behaviour can be observed in figure 9.12I and figure 9.12II. The arising over-currents on the AC-side are much smaller now and also the other 3-level VSI quantities are kept at still reasonable values.

However, things become worse again, if the same single line AC-system fault occurs when the SVC is operating in the nominal inductive operation mode $(I_{q0}'=-1[p.u.])$. According to the simulations in figure 9.13I and figure 9.13II, the AC-side currents i_{ph} exhibit quite large peak-values of more than 3[p.u.]. In addition, they constitute a highly asymmetrical 3-

phase system. Though the results are not as worse as for a very slow tuned PLL (figure 9.11I and figure 9.11II), they are still really not acceptable.

Summarized, it can therefore be concluded, that during disturbances in the AC-system voltages, an additional controller will be of high need in order to limit the arising AC-side current peak-values.

9.4 SVC control during AC-system faults

9.4.1 Basics

In the simulations performed in the previous chapter, it could be seen that the performance of the current controller is pretty bad, if disturbances in the AC-system voltages u_{Lph} occur. In order to improve this behaviour, a feed-forward controller will be designed in this chapter.

Hereby, only AC-system voltage disturbances, which can be described by a positive sequence and/or a negative sequence **fundamental** component, are taken into account. The compensation of other AC-system voltage disturbances (e.g. flicker) cannot properly be achieved, when FFM modulation is presumed.

3-phase AC-system voltage drops or 3-phase AC-system voltage phaseshifts are described by exclusively a disturbance in the positive sequence fundamental component of the AC-system voltages u_{Lph} . E.g. single phase faults however show up both disturbances in the positive sequence and the negative sequence fundamental component (which usually equals to 0).

In a d/q-plane rotating with an angular velocity ω_1 (k=1, appendix C.2.1), positive sequence fundamental disturbances in u_{Lph} are represented by DC-quantities in $\Delta U_{Ld}'$ and $\Delta U_{Lq}'$. On the other side, negative sequence fundamental components are appearing as a clockwise rotating 2nd harmonic phasor $\Delta u_{L2}'$ with a constant amplitude.

In this thesis, the control laws for the feed-forward controller presume a very slow tuned PLL (step response time of about 1sec.), which will be synchronized with the d-component U_{Ld} of the AC-system voltage phasor. This yields the advantage, that AC-system voltage disturbances will not have an influence on the basic quantities $\cos \omega_1 t$ and $\sin \omega_1 t$ (chapter 8.4.5, figure 8.11) necessary for the d/q-transform. Hence, a d/q frame with a very high inertia will be achieved and disturbances in u_{Lph} will exactly be reflected in the AC-system voltage phasor components u_{Ld} and

 u_{Lq}' . Their influence on the AC-side currents can then be compensated by a feed-forward controller, which calculates the reference values for the fundamental components of 3-level VSI output voltages u_{ph} .

For asymmetrical AC-system voltages u_{Lph} (neg. seq. fundamental components), this will also result in asymmetrical 3-level VSI output voltages u_{ph} , which means that the modulation indices m_a , m_b , m_c will no longer be the same in the 3 phases a,b,c. As well the phase-displacements D_a , D_b and D_c will differ from their values $0, -2\pi/3, 2\pi/3$ for symmetrical operation conditions.

A very efficient and fast control scheme for asymmetrical operation conditions, which however only can be applied for carrier based PWM modulation, is proposed in [72] and [73].

In the following, an approach for FFM modulation or off-line optimized PWM will be presented.

9.4.2 Feed-forward controller design

a) Feed-forward controller for the compensation of positive sequence fundamental disturbances in the AC-system voltages

As mentioned above, positive sequence fundamental disturbances in u_{Lph} constitute DC-components $\Delta U_{Ld}'$ and $\Delta U_{Lq}'$ in a d/q plane rotating with an angular velocity ω_1 . Hence, it will be sufficient in this sub-chapter to exclusively focus on the DC-components (upper-case letters) of the individual phasor quantities.

In order to compensate the impact of these DC-components ΔU_{Ld} and ΔU_{Lq} in the AC-side current phasor I of the 3-level VSI SVC, an appropriate control law for a feed-forward controller has to be derived. For that purpose, the phasor diagram presented in figure 9.14, will be of great help.

Herein, the phasor quantities show up the index *pos* in order to emphasize that these quantities refer to pos. seq. fundamental components in the 3-phase plane. This also ensures a clear distinction from phasor quantities corresponding to neg. seq. fundamental components, which will be introduced in the sub-chapter to come.

In general, the pos seq. fundamentals of the SVC AC-side currents i_{ph} will not change at all, if \underline{U}_{refpos} ' will be controlled in the following way:

• the 3-level VSI output voltage phasor \underline{U}_{refpos} will always be co-phasal



fig 9.14: Phasor diagram of the 3-level VSI SVC for the derivation of the feed-forward control law with respect to positive sequence fundamental AC-system voltage disturbances

to the AC-system voltage phasor \underline{U}_{Lpos} and

• the absolute value of the phasor $|\underline{U}_{Zrefpos}'| = |\underline{U}_{Lpos}' - \underline{U}_{refpos}'|$ (voltage phasor across the transformer stray reactance) will always remain the same.

These relationships are represented in figure 9.14 for the case that there is no disturbance in the AC-system voltage phasor $\underline{U}_{Lpos}' (\underline{U}_{Lpos}' = \underline{U}_{L0pos}')$ and for the case of a pos. seq. fundamental disturbance $\Delta \underline{U}_{Lpos}' = \Delta U_{Ldpos}' + j\Delta U_{Lqpos}' (\underline{U}_{Lpos}' = \underline{U}_{L0pos}' + \Delta \underline{U}_{Lpos}')$.

From figure 9.14 it can further be seen, that in a d/q frame with a very high inertia, the AC-side current phasor I_{0pos} will have to be phase-displaced by $\Delta \Phi_{\mu}$ in order to keep the 3-level VSI output voltage phasor co-phasal to the AC-system voltage phasor. This results in a reference current phasor I_{refnos} , which is described by eqn. (9.17).

$$I_{refpos}' = I_{drefpos}' + jI_{arefpos}' = I_0' \cdot e^{j\Delta\Phi_u} = jI_{a0}' \cdot (\cos\Phi_{upos} + j\sin\Phi_{upos}) \quad (9.17)$$

with

$$I_{drefpos}' = -I_{q0}' \sin \Phi_{upos}, I_{qrefpos}' = I_{q0}' \cos \Phi_{upos}, \Phi_{upos} = \operatorname{atan} \frac{U_{Lqpos}'}{U_{Ldpos}'}$$

With that, the d and q components $U_{drefpos}$ and $U_{qrefpos}$ of the 3-level VSI output voltage reference phasor

$$\underline{U}_{refpos}' = \underline{U}_{Lpos}' - \underline{U}_{Zrefpos}' = \underline{U}_{Lpos}' - j\omega_1 l \cdot I_{refpos}'$$
(9.18)

can be calculated according to eqn. (9.19) - eqn. (9.21).

$$U_{drefpos'} = U_{Ldpos'} + \omega_1 l I_{qrefpos'} = U_{Ldpos'} + \omega_1 l I_{q0pos'} \cos \Phi_{upos} \quad (9.19)$$

$$U_{qrefpos}' = U_{Lqpos}' - \omega_1 l I_{drefpos}' = U_{Lqpos}' + \omega_1 l I_{q0pos}' \sin \Phi_{upos} \quad (9.20)$$

$$\Phi_{upos} = \operatorname{atan} \frac{U_{Lqpos}}{U_{Ldpos}},$$
(9.21)

Eqn. (9.19) - eqn. (9.21) constitute appropriate control laws, which will keep the pure reactive AC-side currents i_{ph} symmetrical and at their setvalue in case of positive sequence fundamental disturbances in the AC-system voltages u_{Lph} .

The next sub-chapter will now focus on equivalent control laws for the compensation of neg. seq. fundamental components in u_{Lph} , as always present in asymmetrical AC-system voltages.

b) Feed-forward controller for the compensation of negative sequence fundamental components in the AC-system voltages

Negative sequence fundamental components in u_{Lph} will be reflected in the d/q plane as a phasor $u_{L2}' = u_{Ld2}' + j \cdot u_{Lq2}'$, which rotates clockwise with an angular velocity of a 2nd harmonic component and a constant amplitude.

Transforming this rotating phasor \underline{u}_{L2}' in a d/q frame rotating with a neg. seq. fundamental angular velocity $-\omega_1$ by multiplying \underline{u}_{L2}' with $e^{j2\omega_1 t}$ results in a still standing phasor \underline{U}_{Lnee}' (eqn. (9.22)).

$$\underline{U}_{Lneg}' = \underline{u}_{L2}' \cdot e^{j2\omega_l t} = U_{Ldneg}' + jU_{Lqneg}'$$
(9.22)

Since no negative sequence fundamental components will be desirable in the AC-side currents i_{ph} , the neq. seq. reference phasor \underline{U}_{refneg} ' for the 3-level VSI output voltages coincides with \underline{U}_{Lneg} ' (eqn. (9.23)).
$$\underline{U}_{refneg}' = U_{drefneg}' + jU_{qrefneg}' = \underline{U}_{Lneg}' = U_{Ldneg}' + jU_{Lqneg}' \quad (9.23)$$

Applying eqn. (9.23) as a control law for the feed-forward controller with respect to the compensation of a neg. seq. fundamental component in i_{ph} will yield sufficient results, if the DC-side capacitors are pretty large.

Otherwise, a more or less remarkable second harmonic arises in u_{Dsum} , which is determined by the convolution of the positive sequence AC-side current fundamentals with the neg. seq. switching function fundamentals.

This second harmonic in u_{Dsum} will be reflected back to the AC-side as a negative sequence fundamental (and a 3rd harmonic) and will cause undesirable negative sequence fundamental AC-side currents to arise.

At this point the dynamic transfer functions are of great help, since they make it possible to properly compensate this effect, which will be shown in the following.

For that purpose, eqn. (9.9) for $\Delta i_d'(s)$ and eqn. (9.10) for $\Delta i_q'(s)$ in table 9.3 will be set to 0, and the two resulting equations will be solved for the two control variables $\Delta \phi_u(s)$ and $\Delta m(s)$ in dependancy on the disturbance variables $\Delta u_{Ld}'(s)$ and $\Delta u_{Lq}'(s)$. This results in eqn. (9.24) and eqn. (9.25).

$$\Delta \phi_{uref}(s) = \frac{2}{M_0 u_{Dsum0}} \cdot \Delta u_{Lq2}'(s)$$
(9.24)

$$\Delta m_{ref}(s) = \frac{2}{u_{Dsum0}} \cdot \Delta u_{Ld2}'(s) - \frac{3I_{q0}M_0}{c \cdot U_{Dsum0}^2} \cdot \frac{\Delta u_{Lq2}'(s)}{s}$$
(9.25)

Inserting these two feed-forward control laws in eqn. (9.11) for $\Delta u_{Dsum}(s)$ (table 9.3), yields eqn. (9.26).

$$\Delta u_{Dsum2}(s) = \frac{3I_{q0}'}{cU_{Dsum0}} \cdot \frac{\Delta u_{Lq2}'(s)}{s}$$
(9.26)

Eqn. (9.26) corresponds to the arising 2nd harmonic in the sum of the two DC-side voltages, if the 3-level VSI is controlled according to eqn. (9.24) and eqn. (9.25).

In a d/q-plane rotating with an angular velocity ω_1 , the 3-level VSI outputvoltage phasor \underline{u}_{ref} can be described by eqn. (9.27).

$$\underline{u}_{ref}' = \frac{1}{2} \cdot m_{ref} \cdot e^{j\phi_{uref}} \cdot u_{Dsum}$$
$$= \frac{1}{2} (M_0 + \Delta m_{ref}) \cdot e^{j(\Phi_{u0} + \Delta \phi_{uref})} \cdot (U_{Dsum0} + \Delta u_{Dsum}) \qquad (9.27)$$

If no losses are present in the system, as assumed for the dynamic phasor transfer functions in table 9.3, the steady-state phase-displacement Φ_{u0} between the 3-level VSI output voltages and the AC-system voltages equals to $\Phi_{u0}=0$ for a SVC application. Further, since the deviations $\Delta \phi_{uref}$ will usually be small, the complex exponential function $e^{j\Delta \phi_{uref}}$ can be simplified to

$$e^{j\Delta\phi_{uref}} = \cos\Delta\phi_{uref} + j \cdot \sin\Delta\phi_{uref} \approx 1 + j \cdot \Delta\phi_{uref}$$
(9.28)

With that, eqn. (9.27) can be written to eqn. (9.29).

$$\underline{u}_{ref}' = \frac{1}{2}(M_0 + \Delta m_{ref}) \cdot (1 + j \cdot \Delta \phi_{uref}) \cdot (U_{Dsum0} + \Delta u_{Dsum}) \quad (9.29)$$

An additional simplification of eqn. (9.29), which consists in the negligence of all Δ -product terms, results in eqn. (9.30).

$$\underline{u}_{ref}' = \frac{1}{2}M_0 U_{Dsum0} \cdot \left[\left(1 + \frac{\Delta m_{ref}}{M_0} + \frac{\Delta u_{Dsum}}{U_{Dsum0}} \right) + j \cdot \Delta \phi_{uref} \right]$$
(9.30)

Further, with respect to negative sequence fundamental components in the 3-level VSI output voltages, the DC-components in eqn. (9.30) have not to be taken into account, which finally yields eqn. (9.31).

$$\underline{u}_{2ref}' = \frac{1}{2}M_0U_{Dsum0} \cdot \left[\left(\frac{\Delta m_{ref}}{M_0} + \frac{\Delta u_{Dsum}}{U_{Dsum0}} \right) + j \cdot \Delta \phi_{uref} \right]$$
(9.31)

Inserting now eqn. (9.24), eqn. (9.25) and eqn. (9.26) (transformed into the time domain) in eqn. (9.31), yields a well known result (eqn. (9.32)), which is identical with those achieved in eqn. (9.23).

$$\underline{u}_{2ref}' = \Delta u_{Ld2}' + j \cdot \Delta u_{Lq2}' \tag{9.32}$$

On one side, this proves the validity of the transfer functions presented in table 9.3. On the other side it also shows that sometimes more simple approaches will have the same outcome.

However here, the intention is to eliminate the influence of the second DCside harmonic on the AC-side currents, which even for not too small capacitor sizes as presumed here ($c_{tot} = 1.5$ [p.u.] or $\tau_{c_{tot}} = 4.32$ msec) will have a not negligible influence. This can also be seen in the simulation results in chapter 9.4.5. Therefore the more complex approach via the dynamic transfer functions will be justifiable.

It can be seen from eqn. (9.31), that the term depending on Δu_{Dsum} must not be taken into account, when calculating a neq. seq. reference phasor \underline{U}_{refneg} . Otherwise, the calculation of the appropriate switching function modulation indices $m_{ph}=m_{a,b,c}$ and phase-displacements $D_{ph}=D_{a,b,c}$ (subchapter xxx) will yield wrong results.

Hence, a neq. seq. reference phasor $\underline{U}_{refnegcorr}$, corresponding to the contribution of Δu_{Dsum} will be calculated in the following, which finally has to be subtracted from eqn. (9.23).

In the time domain and in a d/q frame rotating with an angular velocity of a positive sequence fundamental ω_1 , the contribution of Δu_{Dsum} can be written to eqn. (9.33).

$$\begin{split} \underline{u}_{2refcorr'} &= \frac{3M_0 I_{q0'}}{2c U_{Dsum0}} \cdot \int \Delta u_{Lq2'} \cdot dt \\ &= \frac{3M_0 I_{q0'}}{2c U_{Dsum0}} \cdot \int U_{L2'} \cdot \sin(2\omega_1 t + \Phi_{uneg}) \cdot dt \\ &= \frac{3M_0 I_{q0'}}{4\omega_1 c U_{Dsum0}} \cdot U_{L2'} \cdot \cos(2\omega_1 t + \Phi_{uneg}) \\ &= \frac{3M_0 I_{q0'}}{8\omega_1 c U_{Dsum0}} \cdot U_{L2'} \cdot (e^{j(2\omega_1 t + \Phi_{uneg})} + e^{-j(2\omega_1 t + \Phi_{uneg})}) \end{split}$$

Transforming this rotating phasor $\underline{u}_{2refcorr}$ ' in a d/q plane rotating with an angular velocity of a negative sequence fundamental $-\omega_1$, yields the desirable still-standing correction phasor $\underline{U}_{refneecorr}$ ' (eqn. (9.34)).

In addition, a component rotating counter-clockwise with a 4th harmonic appears, which corresponds to a third harmonic in the 3-phase plane. Since only the still-standing component is responsible for 3-phase neg. seq. fundamental components, the 4th harmonic component will be neglected in eqn. (9.34).

With that the resulting neq. seq. reference phasor \underline{U}_{refneg} can be calculated

$$\underline{U}_{refnegcorr'} = \frac{3M_0I_{q0'}}{8\omega_1 c U_{Dsum0}} \cdot U_{L2'} \cdot e^{-j\Phi_{uneg}}$$

$$\underline{U}_{refnegcorr'} = \frac{3M_0I_{q0'}}{8\omega_1 c U_{Dsum0}} \cdot (U_{Ldneg'} + jU_{Lqneg'})$$

$$\underline{U}_{refnegcorr'} = \frac{3M_0I_{q0'}}{8\omega_1 c U_{Dsum0}} \cdot \underline{U}_{Lneg'}$$
(9.34)

to eqn. (9.35).

$$\underline{U}_{refneg'} = \left(1 - \frac{3M_0 I_{q0'}}{8\omega_1 c U_{Dsum0}}\right) \cdot \underline{U}_{Lneg'}$$

$$\underline{U}_{Lneg'} = \underline{u}_{L2'} \cdot e^{j2\omega_1 t} = U_{Ldneg'} + jU_{Lqneg'}$$
(9.35)

9.4.3 Separation of the positive and negative sequence fundamental AC-system voltage components in the d/q-plane

In order to calculate the reference phasors \underline{U}_{refpos} and \underline{U}_{refneg} for the 3-level VSI output-voltages, it will be necessary to separate the pos. and the neg. seq. fundamental components in the AC-system voltages u_{Lph} .

This can very fastly be achieved in the d/q-plane, where it corresponds to the separation of the DC-components and a 2nd harmonic. The separation is graphically represented in the block diagram in figure 9.15.

Herein, the necessary time for the separation (time delay x msec.) is variable and can also be chosen very small. For the simulations presented in chapter 9.4.5, this time delay x was chosen to

$$x = 0.1$$
 msec.

which ensures that the separation will be performed almost immediately.

However, it should be noted that such small separation times presume that the AC-system voltage phasor components u_{Ld} and u_{Lq} will nearly be ripplefree (except of the 2nd harmonic).

This has to be fulfilled, since harmonics in $u_{Ld'}$ and $u_{Lq'}$ will be strongly amplified by the factor $1/(\sin \omega_1 x)$ which becomes quite large, if x has a small value.

This factor $1/(\sin\omega_1 x)$ will be necessary to achieve the original amplitude



i

fig 9.15: Block diagram for the separation of the 2nd harmonic and the DC-components in the AC-system voltage phasor components u_{Ld} ' and u_{Lq} '

of the 2nd harmonic after the delay operation and the subsequent subtraction.

Another drawback of this separation consists in the delay and the coupling of the d and q components due to the rotation $e^{j(\pi/2 - \omega_1 x)}$. Hence, during the time interval x, wrong values will be achieved for the quantities U_{Ldpos}' , U_{Lqpos}' , U_{Ldneg}' and U_{Lqneg}' . This will on the other side not have a significant impact on the control, if x takes on a very small value. The rotation $e^{j(\pi/2 - \omega_1 x)}$ in its turn ensures that the 2nd harmonics in u_{Ld}' and $u_{Lq'}'$ show up the original phase before they are transformed into a phasor.

For the basic investigations performed in this thesis (infinite strong AC-system with ideal sinusoidal AC-system voltages), this kind of separation fulfils an excellent job. Its performance in case of a weaker AC-system however might be worse (larger time delays, influence of the d/q component coupling).

Finally, it should be mentioned that also in the (still-standing) α/β plane, the positive and negative sequence fundamental components can be separated, which however asks for a fixed given time delay of 5 msec [74].

9.4.4 Calculation of the control signals for the FFM modulator

In order to feed the FFM modulator with the proper control signals $cs_{I(a,b,c)}$ and $cs_{II(a,b,c)}$ (figure B.5 in appendix B.2.1) for the generation of the switching functions s_{ph} , the amplitude and the phase-displacements of the 3-level VSI output-voltages have to be known.

For that purpose, the 3-level VSI output voltages u_{ph} will be represented by phasor components \underline{U}_{ph} , which can be calculated according to eqn. (9.36) ([68], [53]).

$$\begin{bmatrix} \underline{U}_{a} \\ \underline{U}_{b} \\ \underline{U}_{c} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ e^{-j 2\pi/3} & e^{j 2\pi/3} & 1 \\ e^{j 2\pi/3} & e^{-j 2\pi/3} & 1 \end{bmatrix} \cdot \begin{bmatrix} \underline{U}_{refpos'} \\ \underline{U}_{refneg'} \\ 0 \end{bmatrix}$$
(9.36)

With that, the individual modulation indices $m_{ph}=m_{a,b,c}$ and phase-displacements $D_{ph}=D_{a,b,c}$ are determined by the following eqn. (9.37) and eqn. (9.38).

$$m_{ph} = m_{a,b,c} = \frac{2 \cdot |\underline{U}_{a,b,c}|}{U_{Dsum0}} = \frac{2 \cdot \sqrt{U_{d(a,b,c)}^2 + U_{q(a,b,c)}^2}}{U_{Dsum0}}$$
(9.37)

$$D_{a,b,c} = \operatorname{atan} \frac{U_{q(a,b,c)}}{U_{d(a,b,c)}}$$
(9.38)

The individual NP-angles $\beta_{a,b,c}$ for the control signals $cs_{I(a,b,c)}$ and $cs_{II(a,b,c)}$ are given by eqn. (9.39).

$$\beta_{a,b,c} = \operatorname{acos}\left(\frac{\pi}{4} \cdot m_{a,b,c}\right)$$
(9.39)

Now, also the control signals $cs_{I(a,b,c)}$ and $cs_{II(a,b,c)}$ can be calculated according to eqn. (9.40) and eqn. (9.41).

$$cs_{I(a,b,c)} = Re\{e^{j(\omega_{1}t + D_{a,b,c} - \beta_{a,b,c})}\}$$
(9.40)

$$cs_{II(a,b,c)} = Re\{e^{j(\omega_1 t + D_{a,b,c} + \beta_{a,b,c})}\}$$
(9.41)

9.4.5 Simulation results

In order to verify the performance of the feed-forward controller, some simulations have been performed for the 3-level VSI SVC. The results are presented in figure 9.16I - figure 9.19II.

It can be concluded, that the feed-forward controller remarkably improves the performance of the 3-level VSI SVC. This proves right for all three types of AC-system voltage disturbances (single phase/3-phase voltage drops, AC-system voltage phase shifts).

Also the influence of the 2nd harmonic in the total DC-side voltage u_{Dsum} can be clearly seen by comparing the simulation results in figure 9.181 - figure 9.19II. Especially the large 2nd harmonic amplitude in the reactive AC-side current phasor component i_{afil} in graphic g) of figure 9.18I indicates unsymmetrical AC-side current fundamental amplitudes.

In addition, a fourier analysis for the AC-side currents i_{ph} has been performed. For the case where the influence of the 2nd harmonic in u_{Dsum} was not taken into account (figure 9.18I, figure 9.18II), the fundamental amplitudes of i_{ph} resulted to I_{a1} =0.83[p.u.], I_{b1} =1.17[p.u.], I_{c1} =1.17[p.u.]. In the simulation, where the influence of the 2nd harmonic in u_{Dsum} has been taken into account, the fourier analysis confirmed that the fundamental am-



fig 9.16I: response of the 3-level VSI SVC to 3-phase voltage drops in u_{Lph} of 0.25[p.u.] (Δu_{Ld} '= \mp 0.25[p.u.] at t=105ms and reverse at t=305ms, graphic a)-c)); feed-forward controller implemented: a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{afi} '



fig 9.16II: response of the 3-level VSI SVC to 3-phase voltage drops in u_{Lph} of 0.25[p.u.] ($\Delta u_{Ld}'=\mp 0.25$ [p.u.] at t=105ms and reverse at t=305ms); feed-forward controller implemented: a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.17I: response of the 3-level VSI SVC to AC-system voltage phase-shifts ($\Delta u_{Lq}'=\pm 0.25$ [p.u.] at t=105ms and reverse at t=305ms, graphic a)-c)); feed-forward controller implemented: a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfil}'



fig 9.17II: response of the 3-level VSI SVC to AC-system voltage phase-shifts ($\Delta u_{Lq}'=\pm 0.25$ [p.u.] at t=105ms and reverse at t=305ms); feed-forward controller implemented: a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.181: response of the 3-level VSI SVC to an AC-system voltage drop in phase a of 0.75[p.u.] (at t=105ms and cleared at t=305ms, graphic a)-c)); feed-forward controller implemented, influence of the 2nd harmonic in u_{Dsum} not taken into account: a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfi}



fig 9.18II: response of the 3-level VSI SVC to an AC-system voltage drop in phase a of 0.75[p.u.] (at t=105ms and cleared at t=305ms); feed-forward controller implemented, influence of the 2nd harmonic in u_{Dsum} not taken into account: a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}



fig 9.19I: response of the 3-level VSI SVC to an AC-system voltage drop in phase a of 0.75[p.u.] (at t=105ms and cleared at t=305ms, graphic a)-c)); feedforward controller implemented, influence of the 2nd harmonic in u_{Dsum} taken into account: a) u_{La} , b) u_{Lb} , c) u_{Lc} , d) i_a , e) i_b , f) i_c , g) i_{qfi}



fig 9.19II: response of the 3-level VSI SVC to an AC-system voltage drop in phase a of 0.75[p.u.] (at t=105ms and cleared at t=305ms); feed-forward controller implemented, influence of the 2nd harmonic in u_{Dsum} taken into account: a) u_a , b) u_b , c) u_c , d) ϕ_u , e) u_{D1} , f) u_{D2} , g) u_{Dsum} , u_{Ddiff}

plitudes of the AC-side currents i_{ph} are almost equal.

9.5 Summary

This chapter was focusing on a basic AC-side current control scheme for the FFM modulated 3-level VSI SVC. Hereby, the AC-system strength was not taken into account, e. g. the AC-system was assumed to be infinite strong.

In a first step, the dynamic phasor transfer functions of the 3-level VSI SVC were presented, which also included the influence of dynamics in the AC-system voltages u_{Lph} and finite DC-side capacitor sizes.

Basing on these transfer functions, a conventional control loop (PI-controller) has been designed for the reactive current phasor component i_q' . Simulations with MATLAB and SABER proved a reasonable good performance for load-steps in the controlled variable i_q' .

At disturbances in the AC-system voltages u_{Lph} however, the controller couldn't sufficiently limit the peak-values of the AC-side currents i_{ph} .

Therefore, an additional feed-forward controller was designed, which compensates the impact of these AC-system voltage disturbances in the AC-side currents i_{ph} . Hereby, only AC-system voltage disturbances, which can be described by a positive sequence (3-phase voltage drops) or a negative sequence fundamental component (single phase voltage drops) were taken into account.

In order to verify the efficiency and performance of the feed-forward control scheme, simulations with SABER for the FFM modulated 3-level VSI SVC have been performed.

It could be seen that during AC-system voltage disturbances (single phase/ 3-phase voltage drops, AC-system voltage phase shifts), the feed-forward controller limits the arising peak-values in the AC-side currents to reasonable small values. In addition, the fundamentals of the AC-side currents are controlled to constitute an almost symmetrical 3-phase system, also in the case of highly asymmetrical AC-system voltages u_{Lnh} .

Appendix A

Normalisation and capacitor time constant

A.1 Normalisation

A.1.1 Reference quantities

The nominal peak-values U_L of the AC-system voltages u_{Lph} and the nominal apparent power S_{VSI} of the VSI constitute the reference quantities for the normalisation.

$$U_{ref} = U_L[V] \qquad S_{ref} = S_{VSI}[VA] \qquad (A.1)$$

With that, the reference value Iref for the currents can be calculated to

$$I_{ref} = \frac{2}{3} \cdot \frac{S_{ref}}{U_{ref}} [A] = \frac{2}{3} \cdot \frac{S_{VSI}}{U_L} [A]$$
(A.2)

The reference impedance Z_{ref} is defined to

$$Z_{\text{ref}} = \frac{U_{\text{ref}}}{I_{\text{ref}}} \left[\Omega\right] = \frac{3}{2} \cdot \frac{U_{\text{L}}^2}{S_{\text{VSI}}} \left[\Omega\right]$$
(A.3)

Reference values f_{ref} for the frequency f and w_{ref} for the angular frequency w are given by the nominal fundamental frequency f_1 of the AC-system:

$$f_{ref} = f_1 = 50Hz$$

$$w_{ref} = w_1 = 2\pi \cdot f_{ref} = 2\pi \cdot f_1$$
(A.4)
(A.5)

Basing on the reference impedance Z_{ref} and the reference angular frequency w_{ref} , the following reference values for a resistance R_{ref} , an inductance L_{ref} and a capacitance C_{ref} can be derived:

$$R_{ref} = Z_{ref}; \qquad (A.6)$$

$$L_{ref} = \frac{Z_{ref}}{w_{ref}}; \qquad (A.7)$$

$$C_{ref} = \frac{1}{w_{ref} \cdot Z_{ref}}; \qquad (A.8)$$

A.1.2 Per unit representation of individual quantities

The amplitudes (uppercase letters) and variation in time (lowercase letters) of all voltages, currents and passive components are referred to the above defined reference quantities. This yields the per unit ([p.u.]) representation, which is indicated by *italic* characters.

Per unit representation of voltage amplitudes and corresponding variations in time:

$$U_{x} = \frac{U_{x}}{U_{ref}} [p.u.] \qquad \qquad u_{x} = \frac{u_{x}}{U_{ref}} [p.u.] \qquad (A.9)$$

Per unit representation of current amplitudes and corresponding variations in time:

$$I_x = \frac{I_x}{I_{ref}} [p.u.] \qquad \qquad i_x = \frac{i_x}{I_{ref}} [p.u.] \qquad (A.10)$$

Per unit representation of impedances, resistances, inductances and capacitances:

$$z_x = \frac{Z_x}{Z_{ref}} [p.u.]$$
(A.11)

$$r = \frac{R}{R_{ref}} [p.u.] \qquad l = \frac{L}{L_{ref}} [p.u.] \qquad c = \frac{C}{C_{ref}} [p.u.] \qquad (A.12)$$

Per unit representation of frequencies and angular frequencies:

$$f_x = \frac{f_x}{f_{ref}} [p.u.] \qquad \qquad \omega_x = \frac{w_x}{w_{ref}} [p.u.] \qquad (A.13)$$

The time t will also be normalized to per unit quantities according to the following convention:

$$t = w_{ref} \cdot t \text{ [rad]}$$
(A.14)

Hence the real time t with its physical unit [sec.] (seconds) will be transformed to the normalised time t, which represents an equivalent value in [rad] (radiants).

Quantities, which do not have a physical unit like the modulation index m of the switching functions s_{ph} or the switching functions s_{ph} itself, are invariant with respect to the per unit normalization:

m = m [p.u.]; $s_{ph} = s_{ph} [p.u.]$ (A.15)

A.1.3 Per unit transformation of equations

With regard to the above presented definitions, all equations in the time domain can easily be transformed from the physical unit to the normalized per unit representation. Simply replacing the quantities with physical units by their normalized representatives, yields accurate results.

Hence, the voltage equations for a resistance, a inductance and a capacitance in physical unit representation

$$u(t) = R \cdot i(t),$$
 $u(t) = L \cdot \frac{di(t)}{dt},$ $u(t) = \frac{1}{C} \cdot \int i(t)dt$

will be transformed to

$$u(t) = r \cdot i(t), \qquad u(t) = l \cdot \frac{di(t)}{dt}, \qquad u(t) = \frac{1}{c} \cdot \int i(t) dt$$

in per unit representation.

Also the arguments of the trigonometric functions are transformed in the same way. For example,

$$\mathbf{u}(\mathbf{t}) = \mathbf{U} \cdot \cos(\mathbf{w}_{\mathbf{x}} \cdot \mathbf{t})$$

in physical units will be transformed to

 $u(t) = U \cdot \cos(\omega_x \cdot t)$

in per unit representation.

A.1.4 Laplace transform of per unit equations

If time domain equations in per unit representation have to be transformed into the Laplace domain, also the Laplace operator $s = j \cdot w$ has to be applied in a normalized per unit form.

Hereby, the normalized per unit representation of s is given by

$$s = \frac{s}{w_{ref}} = \frac{j \cdot w}{w_{ref}} = j \cdot \omega$$
 (A.16)

A.2 Definition of the capacitor time constant

It is common to represent the DC-side capacitors C of the 2- or 3-level VSI by means of a time constant in physical units. This time constant can be defined by the ratio between the stored capacitor energy W_C at a nominal rated voltage U_{Dnom} and the nominal apparent power S_{VSI} of the 2- or 3-level VSI.

$$\tau_{\rm C} = \frac{W_{\rm C}}{S_{\rm VSI}} = \frac{1/2 \cdot C \cdot U_{\rm Dnom}^2}{S_{\rm VSI}} [\rm{sec.}] \tag{A.17}$$

Hereby, U_{Dnom} equals those DC-side voltage, which results if the VSI neither absorbs nor delivers any fundamental active or reactive power from the AC-system. Then, the fundamental amplitudes U_1 of the VSI output voltages u_{ph} and U_L of the AC-system voltages u_{Lph} have identical values:

$$U_1 = \frac{m \cdot U_{Dnom}}{2} = U_L; \quad m = modulation index of s_{ph}$$
 (A.18)

With that, U_{Dnom} can be easily calculated from eqn. (A.18).

A.2.1 2-level VSI

Concerning the 2-level VSI, U_{Dnom} is given by

$$U_{Dnom} = \frac{2U_L}{m}$$
(A.19)

Hence, τ_{C} (eqn. (A.17)) can be written as

$$\tau_{\rm C} = \frac{2 \cdot {\rm C} \cdot {\rm U}_{\rm L}^2}{{\rm S}_{\rm VSI} \cdot {\rm m}^2} \, [{\rm sec.}] = \frac{4 \cdot {\rm C} \cdot {\rm Z}_{\rm ref}}{3 \cdot {\rm m}^2} \, [{\rm sec.}] \tag{A.20}$$

If the capacitor C is given in per unit representation (c), the corresponding time constant τ_c will be calculated according to

$$\tau_c = \frac{4 \cdot c}{3 \cdot m^2 \cdot w_1} \text{ [sec.]}; \qquad w_1 = 2\pi \cdot f_1 \tag{A.21}$$

A.2.2 3-level VSI

Concerning the 3-level VSI, it should be distinguished between the time constant τ_C of the individual capacitors C and the time constant $\tau_{C_{rat}}$ of the

total installed capacitance $C_{tot}=C/2$.

For the calculation of the time constant τ_C the voltage across the individual capacitor C has to be chosen as U_{Dnom} , which is determined to

$$U_{\text{Dnom}} = \frac{U_{\text{L}}}{m} \tag{A.22}$$

Inserting eqn. (A.22) in eqn. (A.17) yields

$$\tau_{\rm C} = \frac{1/2 \cdot {\rm C} \cdot {\rm U}_{\rm L}^2}{{\rm S}_{\rm VSI} \cdot {\rm m}^2} \, [{\rm sec.}] = \frac{{\rm C} \cdot {\rm Z}_{\rm ref}}{3 \cdot {\rm m}^2} \, [{\rm sec.}] \tag{A.23}$$

With respect to the calculation of the time constant $\tau_{C_{tot}}$, the voltage across the total capacitance C_{tot} must be considered as U_{Dnom} :

$$U_{\text{Dnom}} = \frac{2U_L}{m} \tag{A.24}$$

With that, $\tau_{C_{tot}}$ can be written as

$$\tau_{C_{tot}} = \frac{2 \cdot C_{tot} \cdot U_L^2}{S_{VSI} \cdot m^2} [sec.] = \frac{4 \cdot C_{tot} \cdot Z_{ref}}{3 \cdot m^2} [sec.]$$
(A.25)

If the capacitors C or C_{tot} are given in per unit representation (c or c_{tot}), the corresponding time constants τ_c and $\tau_{c_{tot}}$ will be calculated according to

$$\tau_c = \frac{c}{3 \cdot m^2 \cdot w_1} \text{ [sec.]}; \qquad w_1 = 2\pi \cdot f_1 \qquad (A.26)$$

and

$$\tau_{c_{tot}} = \frac{4 \cdot c_{tot}}{3 \cdot m^2 \cdot w_1} [\text{sec.}]; \quad w_1 = 2\pi \cdot f_1$$
(A.27)

Appendix B

3-level VSI switching functions

B.1 Fourier rows

B.1.1 General definition

Each periodical function f can be described by means of a fourier row, which in a most general form is defined according to eqn. (B.1) - eqn. (B.3) ([52]).

$$f(\omega t) = \frac{A_0}{2} + \sum_{K} (A_k \cdot \cos k\omega t + B_k \cdot \sin k\omega t)$$
(B.1)
$$= \frac{A_0}{2} + \sum_{K} \sqrt{A_k^2 + B_k^2} \cdot \sin\left(k\omega t + \operatorname{atan} \frac{A_k}{B_k}\right)$$

with
$$k \in K = 0, 1, 2, 3, \dots \infty$$

$$A_k = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\omega t) \cdot \cos k\omega t \cdot d\omega t;$$
(B.2)
$$B_k = \frac{1}{\pi} \int_{-\pi}^{\pi} f(\omega t) \cdot \sin k\omega t \cdot d\omega t$$
(B.3)

Hence, also any periodical 3-level VSI switching function s may be represented by a fourier row. Hereby it can be distinguished between switching function s with a symmetry to a period, a symmetry to half of a period and a symmetry to a quarter of a period. The particular general fourier rows for these switching functions will be deduced in the chapters to come in dependency on the individual switching angles.

B.1.2 3-level VSI switching functions with a symmetry to a period

For a general 3-level VSI switching function s with a symmetry to its period as shown in figure B.1, the fourier coefficients A_0 , A_k and B_k are calculated in a most general way according to eqn. (B.4).



figure B.1: 3-level VSI switching function s with a symmetry to a period

$$A_{0} = \frac{1}{\pi} \left(s(0) \cdot 2\pi + (-1)^{s(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \alpha_{i} \right),$$
(B.4)

$$A_{k} = (-1)^{s(0)} \frac{1}{k\pi} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i},$$

$$B_{k} = -(-1)^{s(0)} \frac{1}{k\pi} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i}$$

with $k \in K = 1, 2, 3, ... \infty$ and $0 \le \alpha_{i} \le 2\pi$;

The particular quantities herein are defined in eqn. (B.5), which will also be referred to in the chapters to come.

$$s(\alpha_i) = \lim_{\epsilon \to 0} \{s(\alpha_i + \epsilon) + s(\alpha_i - \epsilon)\};$$

$$s(0) = \lim_{\epsilon \to 0} \{s(0 + \epsilon)\};$$

$$\alpha_i = i\text{-th switching angle};$$

$$N = \text{number of switching angles } \alpha_i \text{ in the definition range of } \alpha_i;$$
(B.5)

The term s(0) in A_0 and the term $(-1)^{s(0)}$ in A_0 , A_k and B_k are with respect to the start value s(0) of s, which might be different (e.g. s(0)=0 or

s(0) = -1) than those assumed in figure B.1 (s(0) = 1).

Inserting eqn. (B.4) in eqn. (B.1) results in eqn. (B.6), which describes the general 3-level VSI switching function in dependancy on the individual switching angles α_i .

$$s = \frac{1}{2\pi} \left(s(0) \cdot 2\pi + (-1)^{s(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \alpha_{i} \right) +$$

$$+ (-1)^{s(0)} \sum_{K} \frac{1}{k\pi} \left\{ \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i} \right) \cdot \cos k\omega t - \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i} \right) \cdot \sin k\omega t \right\}$$
with $k \in K = 1, 2, 3, \dots \infty$ and $0 \le \alpha_{i} \le 2\pi$;

With the trigonometric theorem ([52])

$$A \cdot \cos x + B \cdot \sin x = \sqrt{A^2 + B^2} \cdot \sin(x + \operatorname{atan}(A/B))$$

eqn. (B.6) can also be written as eqn. (B.7).

$$s = \frac{1}{2\pi} \left(s(0) \cdot 2\pi + (-1)^{s(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \alpha_{i} \right) +$$

$$+ \sum_{K} S_{k} \cdot \sin(k\omega t + \phi_{S_{k}})$$
with $k \in K = 1, 2, 3, ... \infty$ and $0 \le \alpha_{i} \le 2\pi$;
$$S_{k} = \frac{1}{\pi k} \sqrt{\left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i} \right)^{2} + \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i} \right)^{2}};$$

$$\phi_{S_{k}} = \operatorname{atan} \left(\frac{(-1)^{s(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i}}{\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i}} \right);$$
(B.7)

B.1.3 3-level VSI switching functions with a symmetry to half of a period

A 3-level VSI switching function s has a symmetry to half of its period (figure B.2), if the following condition is fulfilled:



$$s(\omega t - \pi) = -s(\omega t) \tag{B.8}$$

figure B.2: 3-level VSI switching function s with a symmetry to half of a period

Then, the fourier coefficients A_0 , A_k and B_k are determined in a most general form according to eqn. (B.9).

$$A_{0} = 0;$$

$$A_{k} = (-1)^{s(0)} \frac{2}{k\pi} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i};$$

$$B_{k} = -(-1)^{s(0)} \frac{2}{k\pi} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i};$$
with $k \in K = 1, 3, 5, ... \infty$ and $0 \le \alpha_{i} \le \pi;$
(B.9)

From eqn. (B.9) it is evident that, compared with the 3-level VSI switching functions with no symmetry at all, no DC-component and exclusively odd numbered harmonic orders k will be present in s.

Inserting eqn. (B.9) in eqn. (B.1) results in eqn. (B.10), which describes the general 3-level VSI switching function with a symmetry to half of the pe-

riod in dependancy on the individual switching angles α_i .

$$s = (-1)^{s(0)} \sum_{K} \frac{2}{k\pi} \left\{ \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i} \right) \cdot \cos k\omega t - \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i} \right) \cdot \sin k\omega t \right\}$$
with $k \in K = 1, 3, 5, \dots \infty$ and $0 \le \alpha_{i} \le \pi$;
$$(B.10)$$

With the trigonometric theorem ([52])

$$A \cdot \cos x + B \cdot \sin x = \sqrt{A^2 + B^2} \cdot \sin(x + \operatorname{atan}(A/B))$$

eqn. (B.10) can also be written as eqn. (B.11).

$$s = \sum_{K} S_{k} \cdot \sin(k\omega t + \phi_{S_{k}})$$
(B.11)
with $k \in K = 1,3,5,...\infty$ and $0 \le \alpha_{i} \le \pi$;
$$S_{k} = \frac{2}{\pi k} \sqrt{\left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i}\right)^{2} + \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i}\right)^{2}}$$
$$\phi_{S_{k}} = \operatorname{atan} \left(\frac{(-1)^{s(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i}}{(-(-1)^{s(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i}}\right);$$

B.1.4 3-level VSI switching functions with a symmetry to a quarter of a period

For a 3-level VSI switching functions s with a symmetry to a quarter of its period, the calculation of its fourier row can further be simplified by specific symmetry conditions. Hereby it has to be distinguished between switching functions s with a cosinusoidal fundamental component and those with a sinusoidal fundamental component.

a) Cosinusoidal fundamental component

For a 3-level VSI switching functions s with a symmetry to a quarter of its period and a cosinusoidal fundamental component (figure B.3), the follow-



figure B.3: 3-level VSI switching function s with a symmetry to a quarter of a period and a cosinusoidal fundamental component

With that, the fourier coefficients A_0 , A_k and B_k are determined in a most general form according to eqn. (B.13).

 $A_{0} = 0;$ $A_{k} = (-1)^{s(0)} \frac{4}{k\pi} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i};$ $B_{k} = 0;$ with $k \in K = 1, 3, 5, ... \infty$ and $0 \le \alpha_{i} \le \pi/2;$ (B.13)

From eqn. (B.13) it is evident that for switching functions with a symmetry to a quarter of a period and a cosinusoidal fundamental component, all fourier coefficients B_k will equal to 0. Hence, the sinusoidal components $\sin k\omega t$ in eqn. (B.1) will not contribute to the fourier row of s.

Inserting eqn. (B.13) in eqn. (B.1) results in eqn. (B.14), which describes the 3-level VSI switching function with a symmetry to a quarter of a period and a cosinusoidal fundamental component in dependancy on the individual switching angles α_i .

$$s = (-1)^{s(0)} \sum_{K} \frac{4}{k\pi} \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i} \right) \cdot \cos k\omega t \qquad (B.14)$$

with $k \in K = 1, 3, 5, \dots \infty$ and $0 \le \alpha_{i} \le \pi/2$;

b) Sinusoidal fundamental component

For a 3-level VSI switching functions s with a symmetry to a quarter of its period and a sinusoidal fundamental component (figure B.4), the following two conditions have to be fulfilled in the interval $[-\pi,\pi]$:

$$s(\omega t - \pi) = -s(\omega t)$$
 and $s(\omega t) = -s(-\omega t)$ (B.15)



figure B.4: 3-level VSI switching function s with a symmetry to a quarter of a period and a sinusoidal fundamental component

With that, the fourier coefficients A_0 , A_k and B_k are determined in a most general form according to eqn. (B.16).

 $A_{0} = 0; (B.16)$ $A_{k} = 0; (B.16)$ $B_{k} = -(-1)^{s(0)} \frac{4}{k\pi} \sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i}; (B.16)$ with $k \in K = 1, 3, 5, \dots \infty$ and $0 \le \alpha_{i} \le \pi/2;$

From eqn. (B.16) it is evident that for switching functions with a symmetry

- 351 -

to a quarter of a period and a sinusoidal fundamental component, all fourier coefficients A_k will equal to 0. Hence, the cosinusoidal components $\cos k\omega t$ in eqn. (B.1) will not contribute to the fourier row of s.

Inserting eqn. (B.16) in eqn. (B.1) results in eqn. (B.17), which describes the 3-level VSI switching function with a symmetry to a quarter of a period and a sinusoidal fundamental component in dependancy on the individual switching angles α_i .

$$s = -(-1)^{s(0)} \sum_{K} \frac{4}{k\pi} \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \cos k\alpha_{i} \right) \cdot \sin k\omega t \quad (B.17)$$

with $k \in K = 1, 3, 5, \dots \infty$ and $0 \le \alpha_{i} \le \pi/2$;

B.2 FFM switching functions

This chapter introduces the graphical generation and a fourier row description of general 3-level VSI FFM switching functions, basing on two phasedisplaced 2-level VSI FFM pulse patterns. Besides the FFM switching functions with a symmetry to a quarter of a period, also those for the two DCside balancing control methods (type I and type II) are presented. Hereby, all graphical and mathematical representations of the switching functions are with respect to a cosinusoidal fundamental component as it is assumed throughout this thesis.

The fourier row of the 3-level VSI FFM switching functions are given in dependancy on both the NP-angle β and the correction angle γ , which is the control variable for the DC-side balance control schemes.

The graphical generation method might not only be helpful for mathematical analyses but also might show up an easy way for the generation of the pulse patterns in simulator and hardware implementations. This will especially prove right for the modified switching functions suitable for the two DC-side balance control schemes.

B.2.1 3-level VSI FFM switching function

a) Graphical generation

The most simple 3-level VSI switching function s, which results from FFM modulation, always can be represented by half the sum of two phase-displaced 2-level VSI FFM switching functions s_{IFFM} and s_{IIFFM} (eqn. (B.18) and figure B.5):

$$s_{FFM} = \frac{1}{2} \cdot (s_{IFFM} + s_{IIFFM}) \tag{B.18}$$

Each 2-level VSI FFM switching function s_{IFFM} or s_{IIFFM} in its turn can be generated with a pure sinusoidal control signal cs_I or cs_{II} and a constant carrier signal c_I or c_{II} according to the following convention:

$$s_{IFFM/IIFFM} = \operatorname{sgn}(cs_{I/II} - c_{I/II})$$
(B.19)

The individual quantities in eqn. (B.19) can be described by

$$cs_{I} = \cos(\omega t - \beta) \quad ; \quad cs_{II} = \cos(\omega t + \beta) \quad (B.20)$$

$$c_{I} = 0; \quad c_{II} = 0$$

Herein, the phase displacement β is denoted the NP-angle of the 3-level VSI FFM pulse pattern.

The statements mentioned above can graphically be verified in figure B.5 for a 3-level VSI FFM pulse pattern.



figure B.5: Graphical generation principle of a 3-level VSI FFM switching function s_{FFM}

b) Mathematical representation

For analysis purposes, a mathematical representation of the switching functions might be of great value. A description by means of a fourier row seems to be the most suited in the field of power electronics. Hereby, the fourier rows for the individual 2-level VSI FFM switching functions s_{IFFM} and s_{IIFFM} result to eqn. (B.21).

$$s_{IFFM} = \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cdot \cos[k(\omega t - \beta)]$$

$$s_{IIFFM} = \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cdot \cos[k(\omega t + \beta)]$$

$$k \in K = 1,3,5,7,...; \quad \beta \le \pi/2$$
(B.21)

With eqn. (B.18), eqn. (B.21) and the trigonometric theorem ([52])

$$\cos x + \cos y = 2\cos\frac{x+y}{2}\cos\frac{x-y}{2}$$

the fourier row for the 3-level VSI FFM switching function s_{FFM} can be calculated to eqn. (B.22).

$$s_{FFM} = \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cos k\beta \cdot \cos k\omega t$$

$$k \in K = 1, 3, 5, 7, \dots; \quad \beta \le \pi/2$$
(B.22)

From eqn. (B.22) it is evident that with an appropriate choice of the NP-angle β , particular harmonics can be eliminated ($\cos k\beta = 0$) or minimized ($\cos k\beta \rightarrow min$). Further it is possible to control the modulation index m(=4/ $\pi \cdot \cos \beta$) in a wide range between $m=4/\pi$ ($\beta=0$) and m=0($\beta=\pi/2$).

For sure, eqn. (B.22) can also easily be verified by eqn. (B.14), representing the general fourier row for a 3-level VSI switching function with a symmetry to a quarter of a period and a cosinusoidal fundamental component. Hereby, according to figure B.5, the number of switching angles N in a quarter of a period equals to N=1 and the unique switching angle α_1 results to

 $\alpha_1 = \pi/2 - \beta$.

The switching function values s(0) and $s(\alpha_1)$ (eqn. (B.5)) are determined to

$$s(0) = s_{FFM}(0) = 1;$$
 $s(\alpha_1) = s_{FFM}(\alpha_1) = 1.$

B.2.2 Modified 3-level VSI FFM switching function for the DC-side balance control of type I

a) Graphical generation

Also 3-level VSI FFM pulse patterns suitable for the DC-side balance control of type I can be generated with the help of two phase-displaced modified 2-level VSI FFM pulse patterns (eqn. (B.18)).

Hereby, the control signals cs_I and cs_{II} are the same as for the unmodified FFM pulse pattern (appendix B.2.1), while the carrier signals c_I and c_{II} now take on a DC-value unequal to 0. This is manifested in eqn. (B.23) and graphically shown in figure B.6.

 $c_{S_{I}} = \cos(\omega t - \beta) ; \quad c_{S_{II}} = \cos(\omega t + \beta)$ $c_{I} = const = \sin\gamma; \quad c_{II} = const = \sin\gamma$ $s_{IFFM/IIFFM} = sgn(c_{S_{I/II}} - c_{I/II})$ $s_{FFM} = \frac{1}{2} \cdot (s_{IFFM} + s_{IIFFM})$ (B.23)



figure B.6: Graphical generation principle of a 3-level VSI FFM switching function s_{FFM} for DC-side balance control of type I

According to eqn. (B.23), the NP-angle β and the DC-side balance control angle γ can be adjusted independently.

It can be seen in figure B.6 that the DC-components in c_I and c_{II} yield a phase-displacement γ of the switching instants of s_{IFFM} and s_{IIFFM} in opposite directions. This causes the negative blocks of both s_{IFFM} and s_{IIFFM} to become larger than the positive blocks, which corresponds to a negative DC-component in the two switching functions.

As a consequence also the resulting 3-level VSI pulse pattern s_{FFM} , being half the sum of s_{IFFM} and s_{IIFFM} , will show up a negative DC-component, which is represented by a larger negative and a smaller positive block. Further it is obvious from figure B.6 that in case of a negative DC reference value for c_I and c_{II} , the opposite, namely a larger positive and a smaller negative block for s_{FFM} would be achieved.

With regard to the NP-angles of s_{FFM} , it can clearly be seen in figure B.6 that their length (2β) has not been influenced by the modification of the carrier signals. However, this does not prove right for the location of the NP-angles, which now, compared to the unmodified 3-level VSI FFM pulse pattern in figure B.5, are phase-displaced in opposite directions by the DC-side balance control angle γ .

b) Mathematical representation

The fourier rows for the individual 2-level VSI FFM switching functions generated with the control and carrier signals according to eqn. (B.23) result to eqn. (B.24).

$$s_{IFFM} = -\frac{2\gamma}{\pi} + \sum_{K} \frac{4}{\pi k} \left(\sin k \frac{\pi}{2} \cos k\gamma - \cos k \frac{\pi}{2} \sin k\gamma \right) \cos \left[k(\omega t - \beta) \right] (B.24)$$

$$s_{IIFFM} = -\frac{2\gamma}{\pi} + \sum_{K} \frac{4}{\pi k} \left(\sin k \frac{\pi}{2} \cos k\gamma - \cos k \frac{\pi}{2} \sin k\gamma \right) \cos \left[k(\omega t + \beta) \right]$$

$$k \in K = 1,2,3,4,...; \qquad \beta \le \pi/2; \qquad \gamma < \pi/2 - \beta;$$

The restriction $\gamma < \pi/2 - \beta$ ensures, that the resulting 3-level VSI FFM pulse pattern s_{FFM} contributes with both positive and negative pulses. If $\gamma < \pi/2 - \beta$ is not fulfilled either exclusively positive or exclusively negative pulses will be apparent in s_{FFM} .

With eqn. (B.23),

 $s_{FFM} = 1/2 \cdot (s_{IFFM} + s_{IIFFM})$

eqn. (B.24) and the trigonometric theorem ([52])

$$\cos x + \cos y = 2\cos\frac{x+y}{2}\cos\frac{x-y}{2}$$

the fourier row for the 3-level VSI FFM switching function s_{FFM} will result in eqn. (B.25).

$$s_{FFM} = -\frac{2\gamma}{\pi} + \sum_{K} \frac{4}{\pi k} \left(\sin k \frac{\pi}{2} \cos k\gamma - \cos k \frac{\pi}{2} \sin k\gamma \right) \cos k\beta \cdot \cos k\omega t \quad (B.25)$$

$$k \in K = 1, 2, 3, 4, \dots; \qquad \beta \le \pi/2; \qquad \gamma < \pi/2 - \beta;$$

It can clearly be seen in eqn. (B.25), that s_{FFM} now shows up a DC-component proportional to γ . However, these DC-components constitute a zero sequence system and will therefore not cause any DC-components to arise in the AC-side currents.

Further also all even numbered harmonics will be present in s_{FFM} , which are capable to control a DC-side unbalance to 0, at least for an operation mode with an active power exchange. The phase-displacement of these even numbered harmonics with respect to the fundamental component is either 0 or π as can clearly be seen in eqn. (B.25).

For sure, eqn. (B.25) can also easily be verified by eqn. (B.6), representing the general fourier row for a 3-level VSI switching function with no symmetry. Hereby, according to figure B.6, the number of switching angles N in the whole period equals to N=4 and the individual switching angles α_i result to

$$\alpha_{1/2} = \pi/2 \mp \beta - \gamma;$$
 $\alpha_{3/4} = 3\pi/2 \mp \beta + \gamma.$

The switching function values s(0) and $s(\alpha_i)$ (eqn. (B.5)) are determined to

$$s(0) = s_{FFM}(0) = 1; \ s(\alpha_{1/4}) = s_{FFM}(\alpha_{1/4}) = 1; \ s(\alpha_{2/3}) = s_{FFM}(\alpha_{2/3}) = -1.$$

B.2.3 Modified 3-level VSI FFM switching function for the DC-side balance control of type II

a) Graphical generation

Also 3-level VSI FFM pulse patterns suitable for the DC-side balance control of type II can be generated with the help of two phase-displaced modified 2-level VSI FFM pulse patterns (eqn. (B.18)). Hereby, the control signals cs_I and cs_{II} are the same as for the unmodified FFM pulse pattern (appendix B.2.1). The carrier signals c_I and c_{II} however are now described by two opposite signed DC-values, which is mathematically summarized in eqn. (B.26) and graphically shown in figure B.7.

$$c_{S_{I}} = \cos(\omega t - \beta) ; \quad c_{S_{II}} = \cos(\omega t + \beta)$$

$$c_{I} = const = \sin\gamma; \quad c_{II} = -const = -\sin\gamma$$

$$s_{IFFM/IIFFM} = sgn(c_{S_{I/II}} - c_{I/II})$$

$$s_{FFM} = \frac{1}{2} \cdot (s_{IFFM} + s_{IIFFM})$$
(B.26)



figure B.7: Graphical generation principle of a 3-level VSI FFM switching function s_{FFM} for DC-side balance control of type II

Here again, the NP-angle β and the DC-side balance control angle γ can be adjusted independently.

The 2-level VSI FFM switching functions s_{IFFM} and s_{IIFFM} , resulting from eqn. (B.26) are also graphically shown in figure B.7.

As could be expected, the two identical but opposite signed DC-values for c_I and c_{II} will cause identical but opposite signed DC-components to arise in s_{IFFM} and s_{IIFFM} .

Therefore the resulting 3-level VSI FFM pulse pattern, which is half the sum of s_{IFFM} and s_{IIFFM} , will not show up a DC-component, which means that the pulse lengths of the positive and negative blocks are equal.

However, compared to the unmodified FFM modulation function (appendix B.2.1), the positive and negative blocks are phase-displaced in opposite directions, which yields unequal NP-angles, as can clearly be seen in figure B.7.

b) Mathematical representation

The fourier rows for the individual 2-level VSI FFM switching functions, generated with the control and carrier signals according to eqn. (B.26), are given in eqn. (B.27).

$$s_{IFFM} = -\frac{2\gamma}{\pi} + \sum_{K} \frac{4}{\pi k} \left(\sin k \frac{\pi}{2} \cos k\gamma - \cos k \frac{\pi}{2} \sin k\gamma \right) \cos \left[k(\omega t - \beta) \right] (B.27)$$

$$s_{IIFFM} = +\frac{2\gamma}{\pi} + \sum_{K} \frac{4}{\pi k} \left(\sin k \frac{\pi}{2} \cos k\gamma + \cos k \frac{\pi}{2} \sin k\gamma \right) \cos \left[k(\omega t + \beta) \right]$$

$$k \in K = 1, 2, 3, 4, \dots; \qquad \beta \le \pi/2; \qquad \gamma < \beta;$$

The restriction $\gamma < \beta$ ensures, that none of the NP-angles of the resulting 3level VSI FFM pulse pattern s_{FFM} will shrink to 0, which would coincide with the forbidden transition from $s_{FFM}=1$ to $s_{FFM}=-1$ or vice versa.

With eqn. (B.26),

 $s_{FFM} = 1/2 \cdot (s_{IFFM} + s_{IIFFM}),$

eqn. (B.27) and the trigonometric theorems ([52])

$$\cos x + \cos y = 2\cos\frac{x+y}{2}\cos\frac{x-y}{2} \text{ and}$$
$$\cos x - \cos y = -2\sin\frac{x+y}{2}\sin\frac{x-y}{2}$$

the fourier row for the 3-level VSI FFM switching function s_{FFM} can be calculated to eqn. (B.28).

It is confirmed in eqn. (B.28), that the resulting 3-level VSI FFM pulse pattern s_{FFM} has no DC-component as mentioned yet in the previous subchapter a).

However, also the pulse patterns suitable for the DC-side balance control of type II contribute with even numbered harmonics, which are the driving
$$s_{FFM} = \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cos k \gamma \cos k \beta \cdot \cos k \omega t -$$

$$-\sum_{K} \frac{4}{\pi k} \cos k \frac{\pi}{2} \sin k \gamma \sin k \beta \cdot \sin k \omega t$$

$$k \in K = 1, 2, 3, 4, \dots; \quad \beta \le \pi/2; \quad \gamma < \beta;$$
(B.28)

force for the DC-side balancing. These even numbered harmonics show up a phase-displacement of $\pm \pi/2$ with respect to the fundamental component, in opposite to a phase-displacement of 0 or π for the pulse patterns of the DC-side balance control of type I.

For sure, also eqn. (B.28) can easily be verified by eqn. (B.6), representing the general fourier row for a 3-level VSI switching function with no symmetry. Hereby, according to figure B.7, the number of switching angles N in the whole period equals to N=4 and the individual switching angles α_i result to

$$\alpha_{1/2} = \pi/2 \mp (\beta - \gamma);$$
 $\alpha_{3/4} = 3\pi/2 \mp (\beta + \gamma).$

The switching function values s(0) and $s(\alpha_i)$ (eqn. (B.5)) are determined to

 $s(0) = s_{FFM}(0) = 1; \ s(\alpha_{1/4}) = s_{FFM}(\alpha_{1/4}) = 1; \ s(\alpha_{2/3}) = s_{FFM}(\alpha_{2/3}) = -1.$

B.3 PWM switching functions

The chapter to come introduces the graphical generation and the fourier row representations of those 3-level VSI PWM switching functions, which can be decomposed in a number of N 3-level VSI FFM switching functions. This decomposition can be performed for all PWM switching functions having a symmetry to a quarter of a period and also for their modified representatives suitable for the two DC-side balance control methods (type I and type II). Hereby, all graphical and mathematical representations of the switching functions are with respect to a cosinusoidal fundamental component as it is assumed throughout this thesis.

The fourier rows of the 3-level VSI PWM switching functions are given in dependency on their switching frequency $f_s = N$, the particular N NP-angles β_i of the individual N 3-level VSI FFM pulse patterns and the DC-side balance control angle γ .

Especially for these PWM pulse patterns, the graphical generation method might not only be helpful for mathematical analyses but also might show up

an easy way for the generation of the pulse patterns in software simulator and hardware implementations. This will especially prove right for the modified switching functions suitable for the two DC-side balance control schemes of type I and type II.

B.3.1 3-level VSI PWM switching functions with a symmetry to a quarter of a period

a) Graphical generation

Each 3-level VSI PWM pulse pattern s_{PWM} with a symmetry to a quarter of a period and a switching frequency $f_s = N$ can be decomposed in a sum of N 3-level VSI FFM switching functions with N different NP-angles β_i (eqn. (B.29)).

$$s_{PWM} = (-1)^{s_{PWM}(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s_{FFMi}$$
(B.29)

This generation convention can e.g. be derived from eqn. (B.14),

$$s = (-1)^{s(0)} \sum_{K} \frac{4}{k\pi} \left(\sum_{i=1}^{N} (-1)^{i} \cdot s(\alpha_{i}) \cdot \sin k\alpha_{i} \right) \cdot \cos k\omega t$$

$$k \in K = 1, 3, 5, \dots \infty \text{ and } 0 \le \alpha_{i} \le \pi/2;$$

which describes the general fourier row of a 3-level VSI PWM pulse pattern with a symmetry to a quarter of a period and a cosinusoidal fundamental component.

Herein, the N different switching angles α_i can be expressed by the N particular NP-angles β_i of N individual 3-level VSI FFM switching functions s_{FFMi} according to

$$\alpha_i = \pi/2 - \beta_i$$
.

Further it has to be taken into account, that the N individual 3-level VSI FFM switching functions s_{FFMi} contribute with an alternating sign $(-1)^i$ to the sum term in eqn. (B.29).

The graphical verification of the above mentioned statements is presented in figure B.8, where N is chosen to be N=3.

Having a closer look at figure B.8, it can further be seen that it is a good idea to choose the values of the individual NP-angles β_i in descending order, i.e



figure B.8: Graphical generation principle of a 3-level VSI PWM switching function with a symmetry to a quarter of a period by means of N (here: N=3) 3-level VSI FFM pulse patterns

 β_1 contributes with the largest value and β_N with the smallest. With that the index *i* of α_i and β_i coincides and in addition only positive/negative pulses appear in the positive/negative fundamental half-wave of the resulting switching function s_{PWM} as it is desirable at least for an optimized pulse pattern.

Presuming a cosinusoidal fundamental component, the start value $s_{PWM}(0)$ equals $s_{PWM}(0)=1$, if N is an odd number, while $s_{PWM}(0)$ equals $s_{PWM}(0)=0$, if N is an even number. This also can be verified in figure B.8.

Finally it should be noted, that the switching frequency f_s of the resulting pulse pattern s_{PWM} and also of the individual 3-level VSI valves coincides with the number N of individual 3-level VSI FFM switching functions s_{FFMi} . This fact is furthermore evident from figure B.8.

b) Mathematical representation

A mathematical representation of s_{PWM} in dependency on the switching frequency $f_s = N$ and the N particular NP-angles β_i of the N 3-level VSI FFM switching functions s_{FFMi} can now easily be calculated.

For that purpose, the individual 3-level VSI FFM switching functions s_{FFMi} are described by their general fourier, which is given by eqn. (B.22) and for clearness reasons once more presented below:

$$s_{FFMi} = \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cos k \beta_i \cdot \cos k \omega t$$
(B.30)

Inserting eqn. (B.30) in the above derived generation convention eqn. (B.29), yields eqn. (B.31).

$$s_{PWM} = (-1)^{s_{PWM}(0)} \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \left(\sum_{i=1}^{N} (-1)^{i} \cdot \cos k \beta_{i} \right) \cdot \cos k \omega t \quad (B.31)$$

$$k \in K = 1, 3, 5, 7, \dots; \qquad \beta_{i} \le \pi/2;$$

Eqn. (B.31) describes the 3-level VSI PWM switching function s_{PWM} with a symmetry to a quarter of a period in dependency on the switching frequency $f_s = N$ and the N particular NP-angles β_i of the N 3-level VSI FFM pulse patterns s_{FFMi} .

For sure, eqn. (B.31) can also be verified with eqn. (B.14), representing the general fourier row for a 3-level VSI switching function with a symmetry to a quarter of a period and a cosinusoidal fundamental component. Hereby, according to figure B.8, the individual switching angles α_i are given to

$$\alpha_i = \pi/2 - \beta_i; \quad i = 1, 2, ..., N.$$

The switching function values s(0) and $s(\alpha_i)$ (eqn. (B.5)) are determined to

$$s(0) = s_{PWM}(0) = 1$$
 (N = odd) or $s(0) = s_{PWM}(0) = 0$ (N = even)
 $s(\alpha_i) = s_{PWM}(\alpha_i) = 1.$

B.3.2 Modified 3-level VSI PWM switching function for DC-side balance control of type I

a) Graphical generation

Also 3-level VSI PWM switching functions s_{PWM} suitable for the DC-side



balance control of type I can be generated by a number of N modified 3level VSI FFM switching functions s_{FFMi} (figure B.9).

figure B.9: Graphical generation principle of a 3-level VSI PWM switching function suitable for DC-side balance control of type I by means of N (here:N=3) modified 3-level VSI FFM pulse patterns

This can be performed in an equivalent way as described in appendix B.3.1 (eqn. (B.29)) according to

$$s_{PWM} = (-1)^{s_{PWM}(0)} \sum_{i=1}^{N} (-1)^{i} \cdot s_{FFMi}$$
(B.32)

and is shown in figure B.9 for a modified 3-level VSI PWM pulse pattern s_{PWM} with N=3. Hereby, the NP-angles β_i are the same as those for the 3-level VSI FFM switching functions s_{FFMi} in figure B.8 (appendix B.3.1).

It can be seen in figure B.9 that the common DC-side balance control angle γ for the particular s_{FFMi} alternately changes its sign. Hence, also their DC-

components alternately have a positive or a negative value. This ensures that all positive and all corresponding negative pulses of the resulting pulse pattern s_{PWM} contribute with different lengths.

b) Mathematical representation

A mathematical representation of s_{PWM} in dependency on the switching frequency $f_s = N$, the N particular NP-angles β_i of the N 3-level VSI FFM switching functions s_{FFMi} and the DC-side balance control angle γ can now easily be calculated.

For that purpose, the individual 3-level VSI FFM switching functions s_{FFMi} with their alternating signed DC-side balance control angle γ are described by their general fourier (eqn. (B.25)). With

 $\cos[-k(-1)^i \cdot \gamma] = \cos k\gamma$ and $\sin[-k(-1)^i \cdot \gamma] = -(-1)^i \sin k\gamma$

this results to eqn. (B.33).

$$s_{FFMi} = \frac{2 \cdot (-1)^{i} \cdot \gamma}{\pi} +$$

$$+ \sum_{K} \frac{4}{\pi k} \left(\sin k \frac{\pi}{2} \cos k \gamma + (-1)^{i} \cos k \frac{\pi}{2} \sin k \gamma \right) \cos k \beta_{i} \cdot \cos k \omega t$$

$$k \in K = 1, 2, 3, 4, \dots; \qquad \beta_{i} \le \pi/2; \qquad \gamma < \pi/2 - \beta_{i};$$
(B.33)

Inserting eqn. (B.33) in the generation convention (eqn. (B.32)) yields eqn. (B.34).

$$s_{PWM} = (-1)^{s_{PWM}(0)} N \frac{2\gamma}{\pi} +$$

$$+ (-1)^{s_{PWM}(0)} \sum_{K} \frac{4}{\pi k} \sum_{i=1}^{N} \left((-1)^{i} \sin k \frac{\pi}{2} \cos k\gamma + \cos k \frac{\pi}{2} \sin k\gamma \right) \cos k\beta_{i} \cdot \cos k\omega t$$
with
$$k \in K = 1, 2, 3, 4, ...; \quad \beta_{i} \le \pi/2, \ i = 1, 2, ..., N;$$

$$\gamma < min \left(\frac{\pi}{2} - \beta_{i} \right), \ i = 1, 2, ..., N \text{ and } \gamma < \frac{min |\beta_{i+1} - \beta_{i}|}{2}, \ i = 1, 2, ..., N-1$$

Eqn. (B.34) describes the 3-level VSI PWM switching function s_{PWM} suitable for the DC-side balance control of type I in dependency on the switching frequency $f_s = N$, the N particular NP-angles β_i of the N 3-level VSI FFM pulse patterns s_{FFMi} and the DC-side balance control angle γ .

The restrictions for the DC-side balance control angle γ in eqn. (B.34) ensure, that the resulting 3-level VSI PWM pulse pattern s_{PWM} contributes with the same number of positive and negative pulses, which is desirable with respect to the switching frequency for each 3-level VSI valve.

In case that these restrictions for γ are not fulfilled, the sum of the particular s_{FFMi} might in addition result in values $s_{PWM} = 2$ or $s_{PWM} = -2$, which from a logical and technical point of view does not make any sense.

For sure, eqn. (B.34) can also be achieved with eqn. (B.6), representing the general fourier row for a 3-level VSI switching function with no symmetry at all. Hereby, according to figure B.9, the individual switching angles α_i are given to

$$\alpha_{i} = \pi/2 - \beta_{i} + (-1)^{i} \cdot \gamma; \qquad \alpha_{N+i} = \pi/2 + \beta_{N-i+1} - (-1)^{N+i} \cdot \gamma; \alpha_{2N+i} = 3\pi/2 - \beta_{i} - (-1)^{2N+i} \cdot \gamma; \qquad \alpha_{3N+i} = 3\pi/2 + \beta_{N-i+1} + (-1)^{3N+i} \cdot \gamma; i = 1, 2, ..., N.$$

The switching function values s(0) and $s(\alpha_i)$ (eqn. (B.5)) are determined to

$$s(0) = s_{PWM}(0) = 1 \ (N = \text{odd}) \text{ or } s(0) = s_{PWM}(0) = 0 \ (N = \text{even})$$

$$s(\alpha_i) = s_{PWM}(\alpha_i) = 1; \qquad s(\alpha_{N+i}) = s_{PWM}(\alpha_{N+i}) = -1;$$

$$s(\alpha_{2N+i}) = s_{PWM}(\alpha_{2N+i}) = -1; \qquad s(\alpha_{3N+i}) = s_{PWM}(\alpha_{3N+i}) = 1.$$

B.3.3 Modified 3-level VSI PWM switching function for DC-side balance control of type II

a) Graphical generation

Also a 3-level VSI PWM switching function s_{PWM} suitable for the DC-side balance control of type II can be generated by a number of N modified 3-level VSI FFM switching functions s_{FFMi} .

Here again, this can be performed in an equivalent way as described in the previous chapters and is shown in figure B.10 for a modified 3-level VSI PWM pulse pattern s_{PWM} with N=3. Hereby, the NP-angles β_i are the same as those for the 3-level VSI FFM switching functions s_{FFMi} in figure B.8.

It can be seen in figure B.10 that the common DC-side balance control angle γ for the particular s_{FFMi} alternately changes its sign. This ensures that the corresponding NP-angles in the two half-periods of the resulting pulse pattern s contribute with different lengths.



figure B.10: Graphical generation principle of a 3-level VSI PWM switching function suitable for DC-side balance-control of type II by means of N (here:N=3) modified 3-level VSI FFM pulse patterns

b) Mathematical representation

A mathematical representation of s_{PWM} in dependency on the switching frequency $f_s = N$, the N particular NP-angles β_i of the N 3-level VSI FFM switching functions s_{FFMi} and the DC-side balance control angle γ can now easily be calculated.

For that purpose, the individual 3-level VSI FFM switching functions s_{FFMi} with their alternating sign for the DC-side balance control angle γ are described by their general fourier (eqn. (B.28)). With

 $\cos[-k(-1)^{i}\gamma] = \cos k\gamma$ and $\sin[-k(-1)^{i}\gamma] = -(-1)^{i}\sin k\gamma$ this results to eqn (B 35):

this results to eqn. (B.35):

$$s_{FFMi} = \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cos k \gamma \cos k \beta_{i} \cdot \cos k \omega t +$$

$$+ \sum_{K} \frac{4}{\pi k} \cos k \frac{\pi}{2} (-1)^{i} \sin k \gamma \sin k \beta_{i} \cdot \sin k \omega t$$

$$k \in K = 1, 2, 3, 4, \dots; \qquad \beta_{i} \le \pi/2; \qquad \gamma < \beta_{i};$$
(B.35)

Inserting eqn. (B.35) in the generation convention (eqn. (B.29)) yields eqn. (B.36).

$$(B.36)$$

$$s_{PWM} = (-1)^{s_{PWM}(0)} \left\{ \sum_{K} \frac{4}{\pi k} \sin k \frac{\pi}{2} \cos k \gamma \left(\sum_{i=1}^{N} (-1)^{i} \cos k \beta_{i} \right) \cdot \cos k \omega t + \sum_{K} \frac{4}{\pi k} \cos k \frac{\pi}{2} \sin k \gamma \left(\sum_{i=1}^{N} \sin k \beta_{i} \right) \cdot \sin k \omega t \right\}$$

$$k \in K = 1, 2, 3, 4, \dots; \quad \beta_{i} \le \pi/2, \ i = 1, 2, \dots, N;$$

$$\gamma < \min(\beta_{i}), \ i = 1, 2, \dots, N \text{ and}$$

$$\gamma < \frac{\min|\beta_{i+1} - \beta_{i}|}{2}, \ i = 1, 2, \dots, N-1$$

Eqn. (B.36) describes the 3-level VSI PWM switching function s_{PWM} suitable for the DC-side balance control of type II in dependency on the switching frequency $f_s = N$, the N particular NP-angles β_i of the N 3-level VSI FFM pulse patterns s_{FFMi} and the DC-side balance control angle γ .

On one hand, the restrictions for the DC-side balance control angle γ in eqn. (B.36) ensure that none of the NP-angles of the resulting 3-level VSI PWM pulse pattern s_{PWM} will shrink to 0, which could coincide with the forbidden transition from $s_{PWM}=1$ to $s_{PWM}=-1$ or vice versa. On the other hand, it is guaranteed that exclusively positive/negative pulses are apparent in the positive/negative half wave of the fundamental component of s_{PWM} , which is desirable with respect to the modulation index m.

In case that these restrictions for γ are not fulfilled, the sum of the particular s_{FFMi} might in addition result in values $s_{PWM} = 2$ or $s_{PWM} = -2$, which from a logical and technical point of view does not make any sense.

For sure, eqn. (B.36) can also be achieved with eqn. (B.6), representing the general fourier row for a 3-level VSI switching function with no symmetry

at all. Hereby, according to figure B.10, the individual switching angles α_i are given to

$$\begin{aligned} \alpha_{i} = \pi/2 - \beta_{i} - (-1)^{i} \cdot \gamma; & \alpha_{N+i} = \pi/2 + \beta_{N-i+1} - (-1)^{N+i} \cdot \gamma; \\ \alpha_{2N+i} = 3\pi/2 - \beta_{i} + (-1)^{2N+i} \cdot \gamma; & \alpha_{3N+i} = 3\pi/2 + \beta_{N-i+1} + (-1)^{3N+i} \cdot \gamma. \\ i = 1, 2, \dots, N. \end{aligned}$$

The switching function values s(0) and $s(\alpha_i)$ (eqn. (B.5)) are determined to

$$s(0) = s_{PWM}(0) = 1 \ (N = \text{odd}) \text{ or } s(0) = s_{PWM}(0) = 0 \ (N = \text{even})$$

$$s(\alpha_i) = s_{PWM}(\alpha_i) = 1; \qquad s(\alpha_{N+i}) = s_{PWM}(\alpha_{N+i}) = -1;$$

$$s(\alpha_{2N+i}) = s_{PWM}(\alpha_{2N+i}) = -1; \qquad s(\alpha_{3N+i}) = s_{PWM}(\alpha_{3N+i}) = 1.$$

Appendix C

Coordinate transforms

C.1 The alpha/beta transform

The alpha/beta (α/β) transform originates from the theory of electrical ACmachines but is also very helpful for general 3-phase systems ([53]). Compared to the 3-phase representation, this transformation into a rotating phasor simplifies the mathematical analysis and further provides an easier access for the understanding of the system behaviour.

C.1.1 Transformation from 3-phase to alpha/beta representation

Any three phase system x_{ph} (voltages, currents), either symmetrical or asymmetrical, can be transformed into a rotating phasor \dot{x} , according to eqn. (C.1) and figure C.1:

$$\dot{\vec{x}} = x_{\alpha} + j \cdot x_{\beta} = \frac{2}{3} \cdot (x_a \cdot e^{j0} + x_b \cdot e^{j2\pi/3} + x_c \cdot e^{-j2\pi/3})$$
(C.1)



figure C.1: transformation of a 3-phase system x_{ph} into a rotating phasor \dot{x}

In case of a pure sinusoidal, symmetrical 3-phase system x_{ph} with an angular frequency ω , the rotating phasor \vec{x} will describe a circle around its origin with the angular velocity ω . Further, the factor 2/3 in eqn. (C.1) ensures that the rotating phasor \vec{x} has the same amplitude as the individual symmetrical 3-phase quantities x_a , x_b , x_c . For an invariant transformation with re-

spect to the powers, the factor 2/3 has to be replaced by $\sqrt{2/3}$.

Due to the transformation rule eqn. (C.1), the zero sequence system x_{zero} of x_{ph} will be eliminated in \dot{x} . This does not imply a severe drawback, since usually x_{zero} will ineffectively drop over the secondary transformer starpoint *SP* and the DC-side midpoint *NP* of the 3-level VSI and will therefore not be of major interest. However, for a unique transformation from the α/β plane back to the 3-phase quantities, x_{zero} must be known and is defined by eqn. (C.2):

$$x_{zero} = 1/3 \cdot (x_a + x_b + x_c)$$
 (C.2)

With

$$e^{\pm j2\pi/3} = \cos(2\pi/3) \pm j \cdot \sin(2\pi/3) = -1/2 \pm j \cdot \sqrt{3/2},$$
 (C.3)

eqn. (C.1) and eqn. (C.2) can be summarized written in matrix notation to eqn. (C.4).

$\begin{bmatrix} x_{\alpha} \end{bmatrix}$		2/3 -1/3	-1/3	$\begin{bmatrix} x_a \end{bmatrix}$	
x _β	=	0 1/√3	-1/√3	x_b .	(C.4
xzero		[1/3 1/3	1/3]	$\begin{bmatrix} x_c \end{bmatrix}$	

C.1.2 Transformation from alpha/beta to 3-phase representation

The transformation from the rotating phasor \dot{x} back to the 3-phase quantities x_a , x_b , x_c is given by the following equations:

$x_a = Re(\vec{x} \cdot e^{j0}) + x_{zero}$	(C.5)
$x_b = Re(\vec{x} \cdot e^{-j2\pi/3}) + x_{zero}$	
$x_c = Re(\vec{x} \cdot e^{j2\pi/3}) + x_{zero}$	

The components $Re(\vec{x} \cdot e^{j0})$, $Re(\vec{x} \cdot e^{-j2\pi/3})$ and $Re(\vec{x} \cdot e^{j2\pi/3})$ can be interpreted as the projections of the rotating phasor \vec{x} onto the (symmetrical) axes e^{j0} , $e^{-j2\pi/3}$ and $e^{j2\pi/3}$ respectively, which yields the zero sequence free parts of the 3-phase quantities x_a , x_b and x_c . This is also graphically shown in figure C.2.

With eqn. (C.3) and $\dot{x} = x_{\alpha} + j \cdot x_{\beta}$, eqn. (C.5) can also be represented in matrix convention according to eqn. (C.6).



figure C.2: transformation of the rotating phasor \dot{x} into the zero sequence free 3-phase quantities

$\begin{bmatrix} x_a \\ x_b \end{bmatrix} =$	1 -1/2	0 √3/2	1 1	$\begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix}$	(C.6)
x_{c}	-1/2	-√3/2	1	xzero	

C.2 The *d/q* transform

Each rotating phasor \hat{x} can be transformed into a coordinate system, whose orthogonal axes d and q rotate with the same or another angular velocity than the fundamental component of the rotating phasor itself. In case that both angular velocities coincide, the fundamental component of the rotating phasor \hat{x} will stand still in the new rotating coordinate system and its projections onto the d and q axis will constitute DC-components.

The major advantage of the d/q transform becomes evident when designing a control scheme. In comparison to time varying quantities as input variables to a controller, their representations by means of phasor DC-components yields a much better control performance.

C.2.1 Transformation from alpha/beta to d/q representation

The mathematical relationship for the transformation of a rotating phasor \dot{x} into a phasor \underline{x} in a coordinate system rotating with an angular velocity $k\omega_1$ is given by eqn. (C.7). Hereby, ω_1 denotes the fundamental angular fre-

$$\underline{x} = x_d + j \cdot x_q = \overset{\flat}{x} \cdot e^{-jk\omega_1 t}$$
(C.7)

quency of the AC-system and k may represent any positive or negative number. Eqn. (C.7) can graphically be verified in figure C.3.



figure C.3: transformation of a rotating phasor \dot{x} into a phasor \underline{x} in a coordinate system rotating with an angular velocity $k\omega_1$

In case that k equals k=1, the AC-side quantities with fundamental angular frequency ω_1 will constitute DC-quantities in the d/q plane. In general, for any value of k, all rotating phasors (and corresponding 3-phase quantities) with angular frequencies $k\omega_1$ will be transformed to DC-quantities in the d/ q plane.

With $e^{-jk\omega_1 t} = \cos k\omega_1 t - j \cdot \sin k\omega_1 t$ and $\dot{x} = x_{\alpha} + j \cdot x_{\beta}$, eqn. (C.7) can also be written in matrix notation according to eqn. (C.8).



Finally it should be noted that in this thesis two different angular velocities $k\omega_1$ will be used for the rotating coordinate system, namely $k\omega_1 = \omega_1$ (k=1) and $k\omega_1 = -2\omega_1$ (k=-2). While $k\omega_1 = \omega_1$ is suitable for investigations concerning the control of the AC-side currents i_{ph} and the total DC-side voltage u_{Dsum} , $k\omega_1 = -2\omega_1$ constitutes the right choice for studies with respect to the DC-side balance (u_{Ddiff}) and its control.

In order to distinguish between the phasors and their d/q-components in these two different coordinate systems, the following notation will be used:

$\bar{x} = \bar{x}$	$x_d = x_d', x_q = x_q'$	if	$k\omega_1 = \omega_1 \ (k=1)$	(C.9)
$\underline{x} = \underline{x}^{"}$	$x_d = x_d$ ", $x_q = x_q$ "	if	$k\omega_1 = -2\omega_1 \ (k=-2)$	(C.10)

With that eqn. (C.8) results to eqn. (C.11) and eqn. (C.12).

$$\begin{bmatrix} x_{d} \\ x_{q} \end{bmatrix} = \begin{bmatrix} \cos \omega_{1} t & \sin \omega_{1} t \\ -\sin \omega_{1} t & \cos \omega_{1} t \end{bmatrix} \cdot \begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix}$$
(C.11)
$$\begin{bmatrix} x_{d} \\ x_{q} \end{bmatrix} = \begin{bmatrix} \cos 2\omega_{1} t & -\sin 2\omega_{1} t \\ \sin 2\omega_{1} t & \cos 2\omega_{1} t \end{bmatrix} \cdot \begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix}$$
(C.12)

C.2.2 Transformation from d/q to alpha/beta representation

The transformation from the phasor \underline{x} back to the rotating phasor \hat{x} can be calculated with the following eqn. (C.13):

$$\dot{\tilde{x}} = x_{\alpha} + j \cdot x_{\beta} = \underline{x} \cdot e^{jk\omega_{1}t}$$
(C.13)

Also here, with $e^{jk\omega_1 t} = \cos k\omega_1 t + j \cdot \sin k\omega_1 t$ and $\underline{x} = x_d + j \cdot x_q$, eqn. (C.13) can be expressed in matrix convention, which yields eqn. (C.14).

$$\begin{bmatrix} x_{\alpha} \\ x_{\beta} \end{bmatrix} = \begin{bmatrix} \cos k\omega_{1}t & -\sin k\omega_{1}t \\ \sin k\omega_{1}t & \cos k\omega_{1}t \end{bmatrix} \cdot \begin{bmatrix} x_{d} \\ x_{q} \end{bmatrix}$$
(C.14)

Note, that the derivative of a rotating phasor $d\dot{x}/dt$ results to eqn. (C.15).

$$\frac{d\dot{x}}{dt} = \frac{dx_{\alpha}}{dt} + j \cdot \frac{dx_{\beta}}{dt} = \left(\frac{dx}{dt} + jk\omega_1 \underline{x}\right) \cdot e^{jk\omega_1 t}$$
(C.15)

Herein it must not be forgotten to take into account the partial derivatives of both the phasor \underline{x} and the rotating unity phasor $e^{jk\omega_1 t}$. The notation in matrix convention is finally given in eqn. (C.16).

$$\begin{bmatrix} \frac{dx_{\alpha}}{dt} \\ \frac{dx_{\beta}}{dt} \end{bmatrix} = \begin{bmatrix} \cos k\omega_1 t - \sin k\omega_1 t \\ \sin k\omega_1 t & \cos k\omega_1 t \end{bmatrix} \cdot \begin{bmatrix} \frac{dx_d}{dt} - k\omega_1 i_q \\ \frac{dx_q}{dt} + k\omega_1 i_d \end{bmatrix}$$
(C.16)

Appendix D

The dynamic phasor equations of the system

This chapter presents the transformation of the 3-level VSI system equations from the 3-phase-plane into the rotating d/q-plane. The hereby achieved dynamic phasor equations will then comprehensively be written in state-space notation, which finally will be followed by the linearization of the system.

D.1 3-phase to d/q transformation

In order to study the dynamic system behaviour and to derive suitable control schemes, it is advisable to represent the system equations by means of phasors in the d/q plane.

The physical model, serving as a basis for the derivation of the 3-phase equations is given in figure D.1 and shows up slight modifications compared to those introduced in chapter 2 (figure 2.3). The remote generator voltages u_{Gph} , which usually are not known at the site of the 3-level VSI, and also the varying and hardly measurable AC-system impedance $(r_L \text{ and } l_L)$ are not taken into account in figure D.1.



figure D.1: model of the 3-level VSI connected to an AC-system for studies concerning dynamic system behaviour

It can be assumed that changes in these two quantities will be reflected to the AC-system voltages u_{Lph} at the primary terminals of the converter transformer, which in its turn are easy accessible for measurement. Hence, the

AC-system voltages u_{Lph} can be seen as dynamic disturbance variables, representing transients in the AC-system. With that, the model presented in figure D.1 will serve as a good basis for the investigations to come.

D.1.1 AC-side equations

With Kirchhoff laws, the AC-side equations of the model in figure D.1 are given by eqn. (D.1):

u _{La}		u _{SP}		i _a		di _a /dt		ua	
u _{Lb}	+	u _{SP}	= <i>r</i>	i _b	+ l	di _b /dt	+	u _b	(D.1)
u_{Lc}		u _{SP}		i _c		di _c /dt		u _c	

Representing the 3-level VSI output voltages $u_{a,b,c}$ by the switching functions and the DC-side voltages according to eqn. (2.10) of chapter 2.4.1 results to eqn. (D.2):

$$\begin{bmatrix} u_{La} \\ u_{Lb} \\ u_{Lc} \end{bmatrix} + \begin{bmatrix} u_{SP} \\ u_{SP} \\ u_{SP} \end{bmatrix} = r \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + l \begin{bmatrix} di_a/dt \\ di_b/dt \\ di_c/dt \end{bmatrix} + \frac{1}{2} \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} u_{Dsum} + \frac{1}{2} \begin{bmatrix} s_a^2 \\ s_b^2 \\ s_c^2 \end{bmatrix} u_{Ddiff} \quad (D.2)$$

It should be noted at this point, that $u_{a,b,c}$ for sure also can be described in dependency on the absolute value of the switching functions $|s_{pk}|$ instead of its squared values s_{pk}^2 , as discussed in detail in chapter 2.4.1. Multiplying both sides of eqn. (D.2) with the 3-phase to α/β transformation matrix (eqn. (C.4) in appendix C.1.1) yields the α/β description of the system:

$\left[\right]$	<i>u_{Lα}</i>	–	0	-		i _α	1	di _α	/dt		sα	" <u>1</u>	$\int s^2 \alpha$		(D 3)
u	u _{Lβ} Lzero	т	u _{SP}	-	1	ι _β 0	Τι		/at) _	12	s _β s _{zero}	^u _{Dsum} +2	s ² β s ² zero	^u Ddiff	(D.3)

Herein, the third equation is exclusively with respect to the zero sequence systems, which ineffectively drop over the secondary transformer starpoint SP and the DC-side neutral point NP and will therefore be neglected from now on.

Further it should be emphasized, that s_{α}^2 and s_{β}^2 are denoted the α and β component of the squared switching functions s_{ph}^2 . They have to

be distinguished from the squared α and β components of the (unsquared) switching functions s_{ph} , which would be written to s_{α}^2 and s_{β}^2 .

With the help of the α/β to d/q transformation matrices (eqn. (C.14) and eqn. (C.16) in appendix C.2.2), the systems equations can finally be transformed from the still-standing α/β plane into the rotating d/q plane, the result of which is given in eqn. (D.4).

$$\begin{bmatrix} u_{Ld} \\ u_{Lq} \end{bmatrix} = r \begin{bmatrix} i_d \\ i_q \end{bmatrix} + l \begin{bmatrix} di_d / dt - k\omega_1 i_q \\ di_q / dt + k\omega_1 i_d \end{bmatrix} + \frac{1}{2} \begin{bmatrix} s_d \\ s_q \end{bmatrix} u_{Dsum} + \frac{1}{2} \begin{bmatrix} s^2_d \\ s^2_q \end{bmatrix} u_{Ddiff} \quad (D.4)$$

Here again, s_d^2 and s_q^2 are representing the d and the q component of the squared switching functions s_{ph}^2 and must not be taken for the squared d and q components of the (unsquared) switching functions s_{ph} , which would be written to s_d^2 and s_q^2 .

More, it should be noted that in eqn. (D.4) the angular velocity $k\omega_1$ of the rotating d/q plane is assumed to be variable. This is due to the fact that the further studies will distinguish between two different values for $k\omega_1$.

For investigations concerning the control of the AC-side currents (i_d, i_q) and the total DC-side voltage (u_{Dsum}) , a d/q -plane which rotates with the AC-system fundamental frequency (k=1) should be chosen. This is also well known yet from the 2-level VSI.

However, focusing on a self-balancing analysis of the two DC-side voltages and appropriate DC-side balancing control schemes, the d/q plane preferably rotates with $-2\omega_1$ (k=-2), which will be discussed more in detail in appendix E.2.1.

Hence it is advisable at this point to represent the AC-side phasor equation in a most general form with respect to the chosen d/q-plane.

D.1.2 DC-side equations

In this thesis, the sum u_{Dsum} and the difference u_{Ddiff} of the two DC-side voltages u_{D1} and u_{D2} are not assumed to be constant but to depend on the AC-side quantities, which, according to eqn. (2.36) and eqn. (2.37) in chapter 2.4.3, can be written to eqn. (D.5) and eqn. (D.6).

In order to express the right sides of eqn. (D.5) and eqn. (D.6) by means of phasor quantities, the active power balance on the AC- and the DC-side of the 3-level VSI will be of great help. This active power balance in phasor notation is given by eqn. (D.7).

$$c \cdot \frac{du_{Dsum}}{dt} = i_{D1} - i_{D2} + 2i_D = \sum_{ph = a,b,c} i_{ph} \cdot s_{ph} + 2i_D$$
(D.5)

$$c \cdot \frac{du_{Ddiff}}{dt} = i_{D1} + i_{D2} = \sum_{ph = a,b,c} i_{ph} \cdot s_{ph}^2$$
 (D.6)

$$\frac{3}{2} \cdot Re(\underline{u} \cdot \underline{i}^*) = i_{D1} \cdot u_{D1} - i_{D2} \cdot u_{D2}$$
(D.7)

Herein \underline{u} denotes the 3-level VSI output voltage phasor and i^* the conjugated complex AC-side current phasor. With

$$\begin{split} \underline{u} &= \frac{1}{2} \cdot \underline{s} \cdot u_{Dsum} + \frac{1}{2} \cdot \underline{s}^2 \cdot u_{Ddiff} \\ &= \frac{1}{2} \cdot (s_d + js_q) \cdot (u_{D1} + u_{D2}) + \frac{1}{2} \cdot (s_d^2 + js_q^2) \cdot (u_{D1} - u_{D2}) \end{split}$$

and

$$i^* = i_d - ji_q$$

eqn. (D.7) yields eqn. (D.8) for the active power on the AC-side.

$$\frac{3}{2} \cdot Re(\underline{u} \cdot \underline{i}^*) = \frac{3}{4} [(s_d + s_d^2) \cdot \underline{i}_d + (s_q + s_q^2) \cdot \underline{i}_q] \cdot u_{D1}^-$$
(D.8)
$$-\frac{3}{4} [(s_d^2 - s_d) \cdot \underline{i}_d + (s_q^2 - s_q) \cdot \underline{i}_q] \cdot u_{D2}$$

Comparing eqn. (D.8) with the active power on the DC-side (right side of eqn. (D.7)), results in the following expressions for the DC-side currents i_{D1} and i_{D2} :

$$i_{D1} = \frac{3}{4} [(s_d + s_d^2) \cdot i_d + (s_q + s_q^2) \cdot i_q]$$
(D.9)

$$i_{D2} = \frac{3}{4} [(s_d^2 - s_d) \cdot i_d + (s_q^2 - s_q) \cdot i_q]$$
(D.10)

Finally, by inserting eqn. (D.9) and eqn. (D.10) in eqn. (D.5) and eqn. (D.6), the desired 3-level VSI DC-side equations in phasor notation are achieved (eqn. (D.11), eqn. (D.12)).

$$c \cdot \frac{du_{Dsum}}{dt} = \frac{3}{2} \cdot (s_d \cdot i_d + s_q \cdot i_q) + 2i_D \tag{D.11}$$

$$c \cdot \frac{du_{Ddiff}}{dt} = \frac{3}{2} \cdot (s_d^2 \cdot i_d + s_q^2 \cdot i_q) \tag{D.12}$$

D.2 State-space representation and linearization

D.2.1 State-space representation

The system equations on the AC- and the DC-side, as given by eqn. (D.4) and eqn. (D.11), eqn. (D.12), can be summarized in the state-space representation, which generally is described by eqn. (D.13).

$$\frac{dx}{dt} = A \cdot x + B \cdot u \tag{D.13}$$

Herein, x denotes the state variable vector, A the system matrix, B the input matrix and u the input variable vector. For more detailed informations concerning state-space theory, the reader is referred to the well known literature (e.g. [75]).

Applying eqn. (D.13) to eqn. (D.4), eqn. (D.11) and eqn. (D.12) yields the state space representation of the investigated system (3-level VSI connected in shunt to the AC-system) according to eqn. (D.14).

$\frac{d}{dt}$	$egin{array}{c} i_d \ i_q \ u_{Dsum} \ u_{Ddiff} \end{array}$	=	$\begin{bmatrix} -\frac{r}{l} \\ -k\omega_1 \\ \frac{3s_d}{2c} \\ \frac{3s^2_d}{2c} \end{bmatrix}$	$k\omega_{1}$ $-\frac{r}{l}$ $\frac{3s_{q}}{2c}$ $\frac{3s^{2}q}{2c}$	$ \frac{s_d}{2l} \\ \frac{s_q}{2l} \\ 0 \\ 0 $	$\begin{bmatrix} s^2_d \\ 2l \\ s^2_q \\ 2l \end{bmatrix}$	$\begin{bmatrix} i_d \\ i_q \\ u_{Dsum} \\ u_{Ddiff} \end{bmatrix} + \begin{bmatrix} \frac{1}{l} & 0 & 0 \\ 0 & \frac{1}{l} & 0 \\ 0 & 0 & \frac{2}{c} \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} u_{Ld} \\ u_{Lq} \\ i_D \end{bmatrix} $ (D.14)
----------------	---	---	--	---	--	--	--

Obviously, the state variable vector x consists of the AC-side current phasor components i_d and i_q and both the sum and the difference u_{Dsum} and u_{Ddiff} of the two DC-side voltages. Simultaneously, these quantities constitute the system variables to be controlled.

The input vector u is represented by the AC-system voltage phasor components u_{Ld} and u_{Lq} as well as by the DC-side load current i_D , which all three can here be seen as the disturbance variables of the system.

The control of the state variables will be achieved via the switching function phasor components s_d and s_q , which therefore will be denoted the control variables of the system. It should be noted that s_d and s_q (together with u_{Dsum}) uniquely determine both the amplitude and the

phase-displacement (the angle ϕ_u) of the 3-level VSI output voltage fundamental and with that any 3-level VSI operation mode.

The phasor components s_d^2 and s_q^2 , which are known to correspond to the squared switching functions, do not constitute independent control variables, since they exclusively are determined by the switching functions itself. Hence, any changes in s_d^2 or s_q^2 will be achieved by appropriate changes in s_d and s_q .

D.2.2 Linearization

The solution of eqn. (D.14) with conventional analytical methods (e.g. [75]) is not possible, since the matrix elements of A are not constant due to the time variant switching function phasor components s_d , s_a , s_a^2 , $and s_a^2$.

By linearizing the system in a specific operation point, this will be subject to change and studies concerning the dynamic system behaviour will then be possible, e.g. in the Laplace domain.

For that purpose, the individual time varying system quantities in eqn. (D.14) will be replaced by its steady-state operation point values, indicated by the index '0', and a deviation around this steady-state value, marked by the ' Δ ' operator. This is summarized in eqn. (D.15).

$i_d = I_{d0} + \Delta i_d;$	$i_q = I_{q0} + \Delta i_q;$	(D.15)
$u_{Dsum} = U_{Dsum0} + \Delta u_{Dsum};$	$u_{Ddiff} = U_{Ddiff0} + \Delta u_{Ddiff};$	
$s_d = S_{d0} + \Delta s_d;$	$s_q = S_{q0} + \Delta s_q;$	
$s_{d}^{2} = S_{d0}^{2} + \Delta s_{d}^{2};$	$s_{q}^{2} = S_{q0}^{2} + \Delta s_{q}^{2};$	
$u_{Ld} = U_{Ld0} + \Delta u_{Ld}; u_{Lq} =$	$U_{Lq0} + \Delta u_{Lq}; i_D = I_{D0} + \Delta i_D;$	

The steady-state operation points of the individual phasor quantities in eqn. (D.15) are written in uppercase letters, since they constitute DC-components. It should be recalled in mind that these DC-components, depending on the parameter k of the d/q transform, will correspond to an oscillation in the 3-phase plane with an angular frequency $k\omega_1$. Hence, only if in the 3-phase plane these quantities show up an oscillation with this angular frequency $k\omega_1$, their operation point value will be unequal to 0, otherwise it will equal to 0.

With the given operation points (eqn. (D.15)), the system's steady state equations can be described according to eqn. (D.16).

$$\begin{bmatrix} 0\\0\\0\\0\\0\end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & k\omega_{1} & -\frac{S_{d0}}{2l} & -\frac{S^{2}_{d0}}{2l} \\ -k\omega_{1} & -\frac{r}{l} & -\frac{S_{q0}}{2l} & -\frac{S^{2}_{q0}}{2l} \\ \frac{3S_{d0}}{2c} & \frac{3S_{q0}}{2c} & 0 & 0 \\ \frac{3S^{2}_{d0}}{2c} & \frac{3S^{2}_{q0}}{2c} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_{d0}\\I_{q0}\\U_{Dsum0}\\U_{Ddiff0}\end{bmatrix} + \begin{bmatrix} \frac{1}{l} & 0 & 0 \\ 0 & \frac{1}{l} & 0 \\ 0 & 0 & \frac{2}{c} \\ 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} U_{Ld0}\\U_{Lq0}\\I_{D0}\end{bmatrix}$$
(D.16)

Finally, inserting the operation points (eqn. (D.15)) in the state-space equations (eqn. (D.14)) and applying eqn. (D.16) yields the linearized system equations in its most general form (eqn. (D.17)). Hereby all product terms of two ' Δ ' quantities are neglected.

$$\frac{d}{dt}\begin{bmatrix} \Delta i_{d} \\ \Delta i_{q} \\ \Delta u_{Dsum} \\ \Delta u_{Ddiff} \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & k\omega_{1} & -\frac{S_{d0}}{2l} & -\frac{S^{2}_{d0}}{2l} \\ -k\omega_{1} & -\frac{r}{l} & -\frac{S_{q0}}{2l} & -\frac{S^{2}_{q0}}{2l} \\ \frac{3S_{d0}}{2c} & \frac{3S_{q0}}{2c} & 0 & 0 \\ \frac{3S^{2}_{d0}}{2c} & \frac{3S^{2}_{q0}}{2c} & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d} \\ \Delta i_{q} \\ \Delta u_{Dsum} \\ \Delta u_{Ddiff} \end{bmatrix} +$$
(D.17)
$$+ \begin{bmatrix} \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 & -\frac{U_{Ddiff0}}{2l} & 0 \\ 0 & \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 & -\frac{U_{Ddiff0}}{2l} \\ 0 & 0 & \frac{2}{c} & \frac{3I_{d0}}{2c} & \frac{3I_{q0}}{2c} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{3I_{d0}}{2c} & \frac{3I_{q0}}{2c} \end{bmatrix} \cdot \begin{bmatrix} \Delta u_{Ld} \\ \Delta u_{Lq} \\ \Delta s_{d} \\ \Delta s_{q} \\ \Delta s^{2}_{q} \end{bmatrix}$$

Appendix E

Transfer functions of the system

This chapter presents the derivation of the phasor transfer functions in the Laplace domain, necessary for both investigations concerning

- appropriate control schemes and
- the assessment of the 3-level VSI DC-side self-balancing abilities.

Hereby, two different d/q frames, rotating with an angular velocity ω_1 and with an angular velocity $-2\omega_1$, have been used. In order to distinguish between the d/q-phasor components in these two different coordinate systems, the following notation will be used (see also appendix C.2.1):

 $\begin{array}{cccc} \underline{x} = \underline{x}' & x_d = x_d', \, x_q = x_q' & \text{if } k\omega_1 = \omega_1 \, (k=1) \\ \underline{x} = \underline{x}'' & x_d = x_d'', \, x_q = x_q'' & \text{if } k\omega_1 = -2\omega_1 \, (k=-2) \end{array}$

E.1 Transfer functions for the control of fundamental components

E.1.1 Linearized state-space equations in a d/q frame rotating with an angular velocity ω_1

Usually, in VSI transmission applications, the fundamental components of the AC-side currents constitute the main variables to be controlled. In order that these quantities appear as DC-components in the d/q-plane, the phasor coordinate system has to rotate with the fundamental angular velocity ω_1 (k=1, appendix C.2.1).

Then, the steady-state operation points S^2_{d0} ' and S^2_{q0} ' of the squared switching functions s^2_{ph} usually will equal to 0. This is due to the fact that s^2_{ph} for symmetrical operation conditions will not show up a component with fundamental frequency f_1 (chapter 4.3.1, (eqn. (4.2)). Except of a DC-component (zero sequence system), a negative sequence 2nd harmonic constitutes the fundamental component of s^2_{ph} . Hence, only if the phasor coordinate system would rotate with an angular velocity $-2\omega_1$ (k=-2), the operation points S^2_{d0} " and S^2_{q0} " would result to DC-components unequal to 0.

Assuming symmetrical operation conditions on both the AC- and the DCside $(U_{Ddiff0} = 0)$ and switching functions with at least a symmetry to half of a period, the individual system quantities can be described by eqn. (E.1) (see also eqn. (D.15)).

$$i_{d}' = I_{d0}' + \Delta i_{d}'; \qquad i_{q}' = I_{q0}' + \Delta i_{q}'; \qquad (E.1)$$

$$u_{Dsum} = U_{Dsum0} + \Delta u_{Dsum}; \qquad u_{Ddiff} = 0 + \Delta u_{Ddiff} ; \qquad (E.1)$$

$$s_{d}' = S_{d0}' + \Delta s_{d}'; \qquad s_{q}' = S_{q0}' + \Delta s_{q}'; \qquad (E.1)$$

$$s_{d}' = U_{d0}' + \Delta s_{d}'; \qquad s_{q}' = 0 + \Delta s_{q}'; \qquad (E.1)$$

$$u_{Ld}' = U_{Ld0}' + \Delta u_{Ld}'; \qquad u_{Lq}' = U_{Lq0}' + \Delta u_{Lq}'; \qquad i_{D} = I_{D0} + \Delta i_{D};$$

With that, the linearized system equations in its most general form (eqn. (D.17)) can be written to eqn. (E.2).

-

$$\frac{d}{dt} \begin{bmatrix} \Delta i_{d'} \\ \Delta i_{q'} \\ \Delta u_{Dsum} \\ \Delta u_{Ddiff} \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & \omega_{1} & -\frac{S_{d0'}}{2l} & 0 \\ -\omega_{1} & -\frac{r}{l} & -\frac{S_{q0'}}{2l} & 0 \\ \frac{3S_{d0'}}{2c} & \frac{3S_{q0'}}{2c} & 0 & 0 \\ \frac{3S_{d0'}}{2c} & \frac{3S_{q0'}}{2c} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d'} \\ \Delta i_{q'} \\ \Delta u_{Dsum} \\ \Delta u_{Ddiff} \end{bmatrix} +$$

$$+ \begin{bmatrix} \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 & 0 & 0 \\ 0 & \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 & 0 \\ 0 & 0 & \frac{2}{c} & \frac{3I_{d0'}}{2c} & \frac{3I_{q0'}}{2c} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{3I_{d0'}}{2c} & \frac{3I_{q0'}}{2c} \end{bmatrix} \cdot \begin{bmatrix} \Delta u_{Ld'} \\ \Delta u_{Lq'} \\ \Delta s_{d'} \\ \Delta s_{q'} \\ \Delta s_{q'} \\ \Delta s_{q'} \end{bmatrix}$$
(E.2)

Herein it is evident that in this d/q plane (rotating with ω_1), the state variable Δu_{Ddiff} is linearly independent on the other state variables $\Delta i_d'$, $\Delta i_q'$ and Δu_{Dsum} . With that the equation for Δu_{Ddiff} is absolutely decoupled from the other three equations, which also indicates, that the choice of this d/q-plane (rotating with ω_1) will not be very well suited for investigations concerning the DC-side voltage balance. For that purpose, another d/q-plane rotating with $-2\omega_1$, constitutes the right choice (appendix E.2).

According to the statements above, eqn. (E.2) can therefore be simplified, which finally results to eqn. (E.3).

$$\frac{d}{dt} \begin{bmatrix} \Delta i_{d} \\ \Delta i_{q} \\ \Delta u_{Dsum} \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & \omega_{1} & -\frac{S_{d0}}{2l} \\ -\omega_{1} & -\frac{r}{l} & -\frac{S_{q0}}{2l} \\ \frac{3}{2}\frac{S_{d0}}{c} & \frac{3}{2}\frac{S_{q0}}{c} & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d} \\ \Delta i_{q} \\ \Delta u_{Dsum} \end{bmatrix} + \begin{bmatrix} \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 \\ 0 & \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} \\ 0 & 0 & \frac{2}{c} & \frac{3}{2}\frac{I_{d0}}{c} & \frac{3}{2}\frac{I_{q0}}{c} \end{bmatrix} \cdot \begin{bmatrix} \Delta u_{Ld} \\ \Delta u_{Lq} \\ \Delta u_{Dsum} \end{bmatrix} (E.3)$$
$$\frac{d}{dt} \Delta u_{Ddiff} = \frac{3I_{d0}}{2} \cdot \Delta s^{2}_{d} + \frac{3I_{q0}}{2} \cdot \Delta s^{2}_{q}$$

E.1.2 Transformation into the Laplace domain

The linearized system equations eqn. (E.3) can now be transformed into the Laplace domain in order to calculate the desirable transfer functions. Since all quantities are given in [p.u.] representation, the same has to be true for the Laplace operator s, as defined in appendix A.1.4.

In a first step, this transformation yields eqn. (E.4).

$$s \begin{bmatrix} \Delta i_{d}'(s) \\ \Delta i_{q}'(s) \\ \Delta u_{Dsum}(s) \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & \omega_{1} & -\frac{S_{d0}'}{2l} \\ -\omega_{1} & -\frac{r}{l} & -\frac{S_{q0}'}{2l} \\ \frac{3S_{d0}'}{2} & \frac{3S_{q0}'}{2} & \frac{3S_{q0}'}{2} & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d}'(s) \\ \Delta i_{q}'(s) \\ \Delta u_{Dsum}(s) \end{bmatrix} +$$

$$+ \begin{bmatrix} \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 \\ 0 & \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} \\ 0 & 0 & \frac{2}{c} & \frac{3I_{d0}'}{2} & \frac{3I_{q0}'}{2} \end{bmatrix} \cdot \begin{bmatrix} \Delta u_{Ld}'(s) \\ \Delta u_{Lq}'(s) \\ \Delta s_{d}'(s) \\ \Delta s_{q}'(s) \end{bmatrix}$$

$$s \Delta u_{Ddiff}(s) = \frac{3I_{d0}'}{2} \cdot \Delta s^{2}{}_{d}'(s) + \frac{3I_{q0}'}{2} \cdot \Delta s^{2}{}_{q}'(s)$$

$$(E.4)$$

Rewriting eqn. (E.4) in a more suitable form finally results to eqn. (E.5).

Eqn. (E.5) describes the relationship between the 3-level VSI variables to be controlled, $(\Delta i_d'(s), \Delta i_q'(s) \text{ and } \Delta u_{Dsum}(s) (\Delta u_{Ddiff}(s)))$, and both the control $(\Delta s_d'(s), \Delta s_q'(s))$ and disturbance variables $(\Delta u_{Ld}'(s), \Delta u_{Lq}'(s), \Delta i_D(s))$.

$$\begin{bmatrix} \left(s + \frac{r}{l}\right) & -\omega_{1} & \frac{S_{d0}}{2l} \\ \omega_{1} & \left(s + \frac{r}{l}\right) & \frac{S_{q0}}{2l} \\ -\frac{3S_{d0}}{2} & \frac{-3S_{q0}}{2c} & s \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d}'(s) \\ \Delta i_{q}'(s) \\ -\Delta u_{Dsum}(s) \end{bmatrix} = \begin{bmatrix} \frac{1}{l} \Delta u_{Ld}'(s) - \frac{U_{Dsum0}}{2l} \Delta s_{d}'(s) \\ \frac{1}{l} \Delta u_{Lq}'(s) - \frac{U_{Dsum0}}{2l} \Delta s_{q}'(s) \\ \frac{2}{c} \Delta i_{D}(s) + \frac{3I_{d0}'}{2c} \Delta s_{d}'(s) + \frac{3I_{q0}'}{2c} \Delta s_{q}'(s) \end{bmatrix}$$
(E.5)
$$\Delta u_{Ddiff}(s) = \frac{3I_{d0}'}{2sc} \cdot \Delta s_{d}'(s) + \frac{3I_{q0}'}{2sc} \cdot \Delta s_{q}'(s)$$

For some investigations it might be more convenient to express the control variables $\Delta s_{d'}(s)$ and $\Delta s_{q'}(s)$ by related quantities, namely the modulation index *m* of the switching functions and their phase-displacement ϕ_u with respect to the AC-system voltage phasor $\underline{\mu}_{L'}$.

For that purpose, the switching functions s_{ph} are approximated by their fundamental component, which in phasor notation can be written to eqn. (E.6).

$$\underline{s} = s_d' + j \cdot s_q' = m \cdot \cos \phi_u + j \cdot m \cdot \sin \phi_u \approx m + j \cdot m \cdot \phi_u$$
(E.6)

With $m = M_0 + \Delta m$ and $\phi_u = \Phi_{u0} + \Delta \phi_u$, eqn. (E.6) results to eqn. (E.7).

$$(S_{d0}'+\Delta s_{d}')+j\cdot(S_{q0}'+\Delta s_{q}')\approx (M_{0}+\Delta m)+j\cdot(M_{0}+\Delta m)\cdot(\Phi_{u0}+\Delta\phi_{u}) \quad (E.7)$$

Evaluating the right side of eqn. (E.7), hereby neglecting the very small term $\Delta m \cdot \Delta \phi_u$, and finally comparing the real and the imaginary parts on both sides results in the desired relationships presented in eqn. (E.8).

$$S_{d0}' = M_0; \qquad S_{q0}' = M_0 \cdot \Phi_{u0}; \qquad (E.8)$$
$$\Delta s_d' = \Delta m; \qquad \Delta s_q' = \Delta m \cdot \Phi_{u0} + \Delta \phi_u \cdot M_0$$

With that, eqn. (E.5) can now be rewritten into the form of eqn. (E.9).

Г

$$\begin{bmatrix} \left(s + \frac{r}{l}\right) & -\omega_{1} & \frac{M_{0}}{2l} \\ \omega_{1} & \left(s + \frac{r}{l}\right) & \frac{M_{0}\Phi_{u0}}{2l} \\ -\frac{3M_{0}}{2} & -\frac{3M_{0}\Phi_{u0}}{c} & s \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d}'(s) \\ \Delta i_{q}'(s) \\ \Delta u_{Dsum}(s) \end{bmatrix} = \begin{bmatrix} \frac{\Delta u_{Ld}'(s) - U_{Dsum0}\Delta m(s)}{l} \\ \frac{1}{l}\Delta u_{Lq}'(s) - \frac{U_{Dsum0}\Phi_{u0}}{2l}\Delta m(s) - \frac{U_{Dsum0}M_{0}}{2l}\Delta \phi_{u}(s) \\ \frac{2}{c}\Delta i_{D}(s) + \frac{3(I_{d0}' + \Phi_{u0}I_{q0}')}{2c}\Delta m(s) + \frac{3I_{q0}'M_{0}}{2c}\Delta \phi_{u}(s) \end{bmatrix}$$

$$\Delta u_{Ddiff}(s) = \frac{3I_{d0}'}{2sc} \cdot \Delta s^{2}_{d}'(s) + \frac{3I_{q0}'}{2sc} \cdot \Delta s^{2}_{q}'(s)$$

E.1.3 Calculation of the transfer functions

The upper matrix equation in eqn. (E.5) and eqn. (E.9) are written in the form $A \cdot x = u$ where e.g. A, x, u in eqn. (E.5) coincide with

$$A = \begin{bmatrix} \left(s + \frac{r}{l}\right) & -\omega_{1} & \frac{S_{d0}}{2l} \\ \omega_{1} & \left(s + \frac{r}{l}\right) & \frac{S_{q0}}{2l} \\ -\frac{3S_{d0}}{2c} & -\frac{3S_{q0}}{2c} & s \end{bmatrix}; x = \begin{bmatrix} \Delta i_{d}'(s) \\ \Delta i_{q}'(s) \\ \Delta u_{Dsum}(s) \end{bmatrix}; u = \begin{bmatrix} \frac{1}{l} \Delta u_{Ld}'(s) - \frac{U_{Dsum0}}{2l} \Delta s_{d}'(s) \\ -\frac{1}{l} \Delta u_{Lq}'(s) - \frac{U_{Dsum0}}{2l} \Delta s_{q}'(s) \\ -\frac{2}{c} \Delta i_{D}(s) + \frac{3I_{d0}'}{2c} \Delta s_{d}'(s) + \frac{3I_{q0}'}{2c} \Delta s_{q}'(s) \end{bmatrix}.$$

This type of matrix equation can be solved for the vector x according to $x = A^{-1} \cdot u$, which was performed for eqn. (E.5) and eqn. (E.9) with the symbolic calculation tools of the simulation program MATLAB.

This results in the transfer functions for $\Delta i_d'(s)$, $\Delta i_q'(s)$ and $\Delta u_{Dsum}(s)$ in dependancy on both the disturbance variables ($\Delta u_{Ld'}(s)$, $\Delta u_{Lq'}(s)$, $\Delta i_D(s)$) and the control variables ($\Delta s_d'(s)$, $\Delta s_q'(s)$) or $\Delta \phi_u(s)$, $\Delta m(s)$). The equations are presented in table 1 - table 3 (eqn. (E.10) - eqn. (E.15)).

These transfer functions in its most general form do not look very inviting for further discussions. However, they can be simplified by assuming the ohmic part r to equal to r=0, which in a first approximation is quite good fulfilled in a high power system.

These simplified transfer functions are presented in table 4 - table 6 (eqn. (E.16) - eqn. (E.21)).

The transfer functions in dependancy on the control variables $\Delta \phi_u(s)$ and $\Delta m(s)$ will be the basis for the discussions concerning the control of a 3-level VSI SVC in chapter 9.

















E.2 Transfer functions for the control of the DC-side balance

E.2.1 Linearized state-space equations in a d/q frame rotating with an angular velocity $-2\omega_1$

As could be seen in the previous chapter, transforming the system equations in a d/q frame rotating with an angular frequency ω_1 (k=1, appendix C.2.1) is not very well suited for investigations concerning the 3-level VSI DC-side balance and its control.

It was also mentioned that for that purpose a d/q frame rotating with an angular velocity $-2\omega_1$ (k=-2, appendix C.2.1) constitutes the right choice. It should be recalled in mind that a DC-component in this coordinate system corresponds to a negative sequence 2nd harmonic in the 3-phase plane.

Regarding the squared switching functions s_{ph}^2 , it was shown in chapter 4.3.1, eqn. (4.2) that their fundamental component coincides with a negative sequence 2nd harmonic. Hence, only if the phasor coordinate system will rotate with an angular velocity $-2\omega_1$ (k=-2), the steady-state operation points S_{d0}^2 and S_{q0}^2 of s_{ph}^2 will result to DC-components unequal to 0.

On the other side, the steady-state operation points S_{d0} " and S_{q0} " of the switching function phasor components s_d " and s_q " will now equal to 0, since for a pulse pattern symmetry to at least half of a period, no negative sequence 2nd harmonic will be present in the switching functions.

Further, it can be presumed without restriction of the general validity that the two DC-side voltages u_{D1} and u_{D2} are balanced, e.g. $U_{Ddiff0}=0$, since the dynamics of u_{Ddiff} will still be taken into account by its deviations Δu_{Ddiff} from U_{Ddiff0} .

With that, also the operation points of the AC-side current phasor components I_{d0} " and I_{q0} " will now equal to 0. This is due to the fact that in case of a balanced DC-side ($U_{Ddiff0}=0$), no negative sequence 2nd harmonics will be present in the AC-side currents i_{ph} , as clearly shown in the harmonic analysis in chapter 4.3.3.

Hence, the individual system quantities can be described by eqn. (E.22) (see also eqn. (D.15)).

With that the linearized system equations in its most general form (eqn.

$$i_{d}^{"} = 0 + \Delta i_{d}^{"}; \qquad i_{q}^{"} = 0 + \Delta i_{q}^{"}; \qquad (E.22)$$

$$u_{Dsum} = U_{Dsum0} + \Delta u_{Dsum}; \qquad u_{Ddiff} = 0 + \Delta u_{Ddiff} ;$$

$$s_{d}^{"} = 0 + \Delta s_{d}^{"}; \qquad s_{q}^{"} = 0 + \Delta s_{q}^{"};$$

$$s_{d}^{2} = S^{2}_{d0}^{0} + \Delta s^{2}_{d}^{"}; \qquad s_{q}^{2}^{"} = S^{2}_{q0}^{0} + \Delta s^{2}_{q}^{"};$$

$$u_{Ld}^{"} = 0 + \Delta u_{Ld}^{"}; \qquad u_{Lq}^{"} = 0 + \Delta u_{Lq}^{"}; \qquad i_{D} = I_{D0} + \Delta i_{D};$$

(D.17)) can be written to eqn. (E.23).

Herein it is evident that in a d/q plane rotating with $-2\omega_1$, the state variable Δu_{Dsum} does not show any dependancy on the other state variables Δi_d ", Δi_q " and Δu_{Ddiff} . Δu_{Dsum} exclusively is a function of Δi_D . With that the equation for Δu_{Dsum} is absolutely decoupled from the other three equations.

It should further be mentioned that as a consequence also the DC-side source/sink current Δi_D will no longer have an influence on Δi_d , Δi_q and Δu_{Ddiff} . Especially the independence on Δu_{Ddiff} indicates that Δi_D will not have any impact on an arising unbalance and will not at all be capable to serve as a control variable for a DC-side balance controller. Hence, eqn. (E.23) can be simplified to eqn. (E.24).

Herein, the differential equation for Δu_{Dsum} is in fact included, however only in order to complete the picture, but not for further investigations.

$$\frac{d}{dt} \begin{bmatrix} \Delta i_{a}^{"} \\ \Delta i_{q}^{"} \\ \Delta u_{Ddiff} \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & -2\omega_{1} & -\frac{S^{2}_{d0}^{"}}{2l} \\ 2\omega_{1} & -\frac{r}{l} & -\frac{S^{2}_{q0}^{"}}{2l} \\ 2\omega_{1} & \frac{r}{l} & -\frac{S^{2}_{q0}^{"}}{2l} \\ \frac{3}{2} \frac{S^{2}_{d0}^{"}}{2} & \frac{3}{2} \frac{S^{2}_{q0}^{"}}{c} & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{a}^{"} \\ \Delta i_{q}^{"} \\ \Delta u_{Ddiff} \end{bmatrix} + (E.24) \\
+ \begin{bmatrix} \frac{1}{l} & 0 & -\frac{U_{Dsum0}}{2l} & 0 \\ 0 & \frac{1}{l} & 0 & -\frac{U_{Dsum0}}{2l} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta u_{La}^{"} \\ \Delta u_{Lq}^{"} \\ \Delta s_{d}^{"} \\ \Delta s_{q}^{"} \end{bmatrix} \\
\left(\frac{d}{dt} \Delta u_{Dsum} = \frac{2}{c} \cdot \Delta i_{D} \right) \quad (\text{optional})$$

E.2.2 Transformation into the Laplace domain

The linearized system equations eqn. (E.24) can now be transformed into the Laplace domain in order to calculate the desirable phasor transfer functions. In a first step, this transformation yields eqn. (E.25).

$$s \begin{bmatrix} \Delta i_{d}^{"}(s) \\ \Delta i_{q}^{"}(s) \\ \Delta u_{Ddiff}(s) \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & -2\omega_{1} & \frac{S^{2}_{d0}^{"}}{2l} \\ 2\omega_{1} & -\frac{r}{l} & -\frac{S^{2}_{q0}^{"}}{2l} \\ \frac{3S^{2}_{d0}^{"}}{c} & \frac{3S^{2}_{q0}^{"}}{2} \\ \frac{3S^{2}_{d0}^{"}}{c} & \frac{3S^{2}_{q0}^{"}}{2} \\ 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d}^{"}(s) \\ \Delta i_{q}^{"}(s) \\ \Delta u_{Ddiff}(s) \end{bmatrix} +$$

$$+ \begin{bmatrix} \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} & 0 \\ 0 & \frac{1}{l} & 0 & 0 & -\frac{U_{Dsum0}}{2l} \\ 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} \Delta u_{Ld}^{"}(s) \\ \Delta u_{Lq}^{"}(s) \\ \Delta i_{D}(s) \\ \Delta s_{d}^{"}(s) \\ \Delta s_{q}^{"}(s) \end{bmatrix}$$

$$\left(s\Delta u_{Dsum}(s) = \frac{2}{c} \cdot \Delta i_{D}(s) \right) \text{(optional)}$$

$$(E.25)$$

Rewriting eqn. (E.25) in a form which is suitable for the calculation of the phasor transfer functions results in eqn. (E.26).
$$\begin{pmatrix} \left(s+\frac{r}{l}\right) & 2\omega_{1} & \frac{S^{2}_{d0}}{2l} \\ -2\omega_{1} & \left(s+\frac{r}{l}\right) & \frac{S^{2}_{q0}}{2l} \\ -\frac{3}{2}\frac{S^{2}_{d0}}{c} & -\frac{3}{2}\frac{S^{2}_{q0}}{c} & s \\ \end{bmatrix} \cdot \begin{bmatrix} \Delta i_{d}^{"}(s) \\ \Delta i_{q}^{"}(s) \\ \Delta u_{Ddiff}(s) \end{bmatrix} = \begin{bmatrix} \frac{1}{l}\Delta u_{Ld}^{"}(s) - \frac{U_{Dsum0}}{2l}\Delta s_{d}^{"}(s) \\ \frac{1}{l}\Delta u_{Lq}^{"}(s) - \frac{U_{Dsum0}}{2l}\Delta s_{q}^{"}(s) \\ 0 \end{bmatrix}$$
(E.26)
$$\left(\Delta u_{Dsum}(s) = \frac{2}{sc} \cdot \Delta i_{D}(s)\right) \text{ (optional)}$$

E.2.3 Calculation of the transfer functions

As it proved right yet for eqn. (E.5) and eqn. (E.9) in appendix E.1.2, also the upper matrix equation in eqn. (E.26) is written in the form $A \cdot x = u$.

Hence, it can be solved for the vector x according to $x = A^{-1} \cdot u$, which was performed with the symbolic calculation tools of the simulation program MATLAB.

This results in the transfer functions for $\Delta i_d''(s)$, $\Delta i_q''(s)$ and $\Delta u_{Ddiff}(s)$ in dependancy on both the disturbance variables ($\Delta u_{Ld}''(s)$, $\Delta u_{Lq}''(s)$) and the control variables ($\Delta s_d''(s)$ and $\Delta s_q''(s)$). The equations are presented in table 7 - table 9.







E.3 Transfer functions for DC-side self-balancing analysis

E.3.1 State-space equations in a d/q frame rotating with an angular velocity $-2\omega_1$

In order to study the DC-side self-balancing attributes of the 3-level VSI, the dynamic phasor equations transformed in a d/q frame rotating with an angular velocity $-2\omega_1$ (k=-2, appendix C.2.1) again are of great help.

However, in comparison to the investigations concerning the DC-side balance control, the assumptions made with respect to the particular steadystate operation points, control and disturbance variables will change for selfbalancing studies.

This is explained by the fact that the expression 'self-balancing' describes the ability of the 3-level VSI to counteract to a given DC-side unbalance $U_{Ddiff0} \neq 0$ without any additional control measure (modifications in the control variables s_{ph}) and without any influence of other potential unbalance sources (u_{Lph}) . Hence all dynamic deviations Δs_d ", Δs_q ", Δs_2^2 ", Δs^2_q ", Δu_{Ld} ", Δu_{Lq} " and Δi_D will be set to 0. With that it is ensured, that exclusively the influence of the 3-level VSI topology itself is taken into account.

When investigating the 3-level VSI self-balancing behaviour, the most important presumption is evidently an existing unbalance $U_{Ddiff0} \neq 0$, against which the 3-level VSI might counteract. This unbalance U_{Ddiff0} in its turn will generate even numbered AC-side current harmonics as clearly shown in the harmonic analysis in chapter 7.3. Therefore, their steady-state operation points I_{d0} " and I_{q0} " will also be unequal to 0 in a d/q frame rotating with an angular velocity $-2\omega_1$.

The switching functions are supposed to constitute symmetrical 3-phase systems with at least a symmetry to half of a period. Then, in a d/q frame rotating with an angular velocity $-2\omega_1$, their steady-state operation points $S_{d0}^{"}$ and $S_{q0}^{"}$ will equal to 0, as discussed yet in appendix E.2.1.

Since it is presumed that all potential unbalance sources will have no influence, the operation points U_{Ld0} " and U_{Lq0} " of the AC-system voltage phasor components as well will equal to 0 in the chosen d/q frame.

Finally, the total DC-side voltage u_{Dsum} and the DC-side source/sink current i_D may take on any values for their operation points U_{Dsum0} and I_{D0} .

The explanations made so far can be summarized in eqn. (E.33) (see also eqn. (D.15)).

$$i_{d}^{"} = I_{d0}^{"} + \Delta i_{d}^{"}; \qquad i_{q}^{"} = I_{q0}^{"} + \Delta i_{q}^{"}; \qquad (E.33)$$

$$u_{Dsum} = U_{Dsum0} + 0 \qquad ; \qquad u_{Ddiff} = U_{Ddiff0} + \Delta u_{Ddiff}; \qquad s_{d}^{"} = 0 + 0; \qquad s_{q}^{"} = 0 + 0; \qquad s_{q}^{"} = 0 + 0; \qquad s_{q}^{2} = S_{q0}^{2} + 0; \qquad s_{q}^{2} = S_{q0}^{2} + 0; \qquad u_{Ld}^{"} = 0 + 0; \qquad i_{D} = I_{D0} + 0;$$

Inserting eqn. (E.33) in the general state-space equations (eqn. (D.14), appendix D.2.1) yields eqn. (E.34), which constitutes a good basis for further investigations concerning the 3-level VSI self-balancing behaviour.

$\frac{d}{dt} \begin{bmatrix} i_d^{"} \\ i_q^{"} \\ u_{Dsum} \\ u_{Ddiff} \end{bmatrix} =$	$\begin{bmatrix} \frac{r}{l} \\ 2\omega_1 \\ 0 \\ \frac{3}{2} \frac{S^2_{d0}}{c} \end{bmatrix} \frac{r}{2}$	$-2\omega_1 0$ $-\frac{r}{l} 0$ $0 0$ $\frac{3}{2}\frac{S^2_{q0}}{c} 0$	$ \frac{S^2_{d0}}{2l} \\ \frac{S^2_{q0}}{2l} \\ 0 \\ 0 $	$ \begin{bmatrix} i_d^{"} \\ i_q^{"} \\ u_{Dsum} \\ u_{Ddiff} \end{bmatrix} + $	$\begin{bmatrix} \frac{1}{l} & 0 & 0 \\ 0 & \frac{1}{l} & 0 \\ 0 & 0 & \frac{2}{c} \\ 0 & 0 & 0 \end{bmatrix}$	$\begin{bmatrix} 0\\0\\I_{D0}\end{bmatrix}$	(E.34)
--	---	---	--	---	--	---	--------

It is evident in eqn. (E.34) that the differential equation for u_{Dsum} is completely decoupled from the other equations and will therefore have no influence on the 3-level VSI self-balancing behaviour, which completely will be described by the equations for i_d , i_q and u_{Ddiff} . Hence, the equation for u_{Dsum} will be neglected from now on, which finally results to eqn. (E.35).

$\frac{d}{dt}\begin{bmatrix} i_{d}''\\ i_{q}''\\ u_{Ddiff} \end{bmatrix} = \begin{bmatrix} -\frac{r}{l} & -2\omega_{1} & -\frac{r}{l} \\ 2\omega_{1} & -\frac{r}{l} & -\frac{r}{l} \\ \frac{3}{2}\frac{S^{2}_{d}0''}{c} & \frac{3}{2}\frac{S^{2}_{q}0''}{c} \end{bmatrix}$	$ \begin{bmatrix} S^{2}_{d0} \\ 2l \\ S^{2}_{q0} \\ \hline 2l \\ 0 \end{bmatrix} \cdot \begin{bmatrix} i_{d} \\ i_{q} \\ u_{Ddiff} \end{bmatrix} $	(E.35)
--	--	--------

E.3.2 Transformation into the Laplace domain

In order to calculate the transfer functions in a convenient way, the statespace equations will now be transformed into the Laplace domain.

Hereby, it has to be recalled in mind that the state variables i_d ", i_q " and u_{Ddiff} show up initial values (their operation points I_{d0} ", I_{q0} ", U_{Ddiff0}) at

t=0, which has to be taken into account when transforming the derivative of a time domain quantity into the Laplace domain.

Hence, in the Laplace domain, eqn. (E.35) results to eqn. (E.36).

$$s\begin{bmatrix}i_{d}"(s)\\u_{Ddiff}(s)\end{bmatrix} - \begin{bmatrix}I_{d0"}\\U_{Ddiff0}\end{bmatrix} = \begin{bmatrix}-\frac{r}{l} & -2\omega_{1} & -\frac{S^{2}_{d0"}}{2l}\\2\omega_{1} & -\frac{r}{l} & -\frac{S^{2}_{q0"}}{2l}\\\frac{3}{2}\frac{S^{2}_{d0"}}{c} & \frac{3}{2}\frac{S^{2}_{q0"}}{c} & 0\end{bmatrix} \cdot \begin{bmatrix}i_{d}"(s)\\u_{Ddiff}(s)\end{bmatrix}$$
(E.36)

Finally, rewriting eqn. (E.36) yields eqn. (E.37), which can now be solved for the transfer functions for $i_d''(s)$, $i_a''(s)$ and $u_{Ddiff}(s)$.

	$\begin{bmatrix} \left(s + \frac{r}{l}\right) \\ -2\omega_1 \\ -\frac{3}{2}\frac{S^2_{d0}}{c} \end{bmatrix} = -\frac{3}{2}\frac{S^2_{d0}}{c} = -\frac{1}{2}\frac{S^2_{d0}}{c} = -\frac{1}{2}S^2_$	$\frac{2\omega_1}{\left(s+\frac{r}{l}\right)}$ $\frac{3\frac{S^2q^0}{c}}{\frac{s^2}{c}}$	$\frac{S_{d0}^{2}}{2l}$ $\frac{S_{q0}^{2}}{2l}$ s	$ \begin{bmatrix} i_d''(s) \\ i_q''(s) \\ u_{Ddiff}(s) \end{bmatrix} = \begin{bmatrix} \\ \\ \end{bmatrix} $	$I_{d0}"$ $I_{q0}"$ U_{Ddiff0}		(E.37)
--	--	--	---	--	----------------------------------	--	--------

E.3.3 Calculation of the transfer functions

Since eqn. (E.37) is written in the form $A \cdot x = u$, it can be solved for the vector x ($x = [i_d''(s), i_q''(s), u_{Ddiff}(s)]$) according to $x = A^{-1} \cdot u$. Here again this was performed with the symbolic calculation tools of the simulation program MATLAB.

In addition each of the three achieved equations for the quantities $i_d"(s)$, $i_q"(s)$ and $u_{Ddiff}(s)$ was exclusively expressed in dependancy on its corresponding initial value $I_{d0}"$, $I_{q0}"$, U_{Ddiff0} , which constitutes a more convenient representation for the discussions in chapter 7.4.

The resulting equations are given in table 10.



References

- Hingorani N. G.: FACTS Flexible AC Transmission System, EPRI workshop Flexible AC Transmission System (FACTS), Cincinnati, Ohio, USA, 1990
- [2] Douglas J.: The delivery system of the Future, EPRI Journal, pp. 5-11, October-November 1992
- [3] Hingorani N. G.: Flexible AC Transmission, IEEE Spectrum, pp. 40-45, April 1993
- [4] Hingorani N. G., Stahlkopf K. E.: High power electronics, Scientific American, pp. 2-9, November 1993
- [5] Taylor G.: Flexible AC Transmission Systems (FACTS) Broadening the opportunities for Transmission management, Power in the Gulf Conference, Dubai, 1996
- [6] Stahlkopf K. E., Wilhelm M. R.: Tighter controls for busier systems, IEEE Spectrum, pp. 48-52, April 1997
- [7] Christl N. et al.: Advanced series compensation with variable impedance, EPRI workshop Flexible AC Transmission System (FACTS), Cincinnati, Ohio, USA, 1990
- [8] Wüest D.: Untersuchung eines statischen Blindleistungskompensators mit selbstgeführtem Stromrichter bei niedriger Schaltfrequenz, Ph. D. thesis no. 9183, Swiss Federal Institute of Technology, Zurich, Switzerland, 1990
- [9] Gyugyi L.: Solid state synchronous voltage sources for dynamic compensation and real-time control of AC transmission lines, IEEE Special Publication
- [10] Gyugyi L.: Solid-State Control of AC-power transmission, EPRI workshop Flexible AC Transmission System (FACTS), Cincinnati, Ohio, USA, 1990
- [11] Breuer G. D.: Flexible AC Transmission scoping studies, EPRI workshop Flexible AC Transmission System (FACTS), Cincinnati, Ohio, USA, 1990
- [12] Casazza J. A., Lekang D. J.: New FACTS technology its potential impact on transmission system utilization, EPRI workshop Flexible AC Transmission System (FACTS), Cincinnati, Ohio, USA, 1990
- [13] Ramey D. et al.: Use of FACTS power flow controllers to enhance transmission transfer limits, American Power Conference, 1994

- [14] McGillis D. T. et al.: An investigation into the realities of FACTS devices, 6th International AC and DC Transmission conference, pp. 252-257, London, United Kingdom, 1996
- [15] Besanger Y. et al.: Improvement of power system performance by inserting FACTS devices, 6th International AC and DC Transmission conference, pp. 263-268, London, United Kingdom, 1996
- [16] Nelson R. J. et al.: Transient stability enhancement with FACTS controllers, 6th International AC and DC Transmission conference, pp. 269-274, London, United Kingdom, 1996
- [17] Mihalic R. et al.: Improvement of transient stability using Unified Power Flow Controller, IEEE Transactions on Power Delivery, pp. 485-492, vol.11, no.1, 1996
- [18] Pilotto L. A. S., et al.: Determination of needed FACTS controllers that increase asset utilization of power systems, IEEE Transactions on Power Delivery, pp. 364-371, vol.12, no.1, 1997
- [19] Mori Sh. et al.: Development of a large Static Var Generator using selfcommutated inverters for improving power system stability, IEEE Transactions on Power Systems, pp. 371-377, vol.8, no.1, 1993
- [20] Schauder C. et al.: Development of a 100 MVar static condenser for voltage control of transmission systems, IEEE Transactions on Power Delivery, pp. 1486-1496, vol.10, no.3, 1995
- [21] Ichikawa F. et. al.: Operating experience of a 50 MVA self-commutated SVC at the Shin-Shinano substation, International Power Electronics Conference IPEC-Yokohama '95, pp. 597-602, Yokohama, Japan, 1995
- [22] Iizuka A. et al.: Self-commutated Static Var Generator at Shintakatsuka substation, International Power Electronics Conference IPEC-Yokohama '95, pp. 609-614, Yokohama, Japan, 1995
- [23] Kimura N., et al.: Improving stability of power system by forced commutation Static Var Compensator, European Power Electronics conference (EPE'91), pp.1-6, Brighton, United Kingdom, 1991
- [24] Larsen E. et al.: Benefits of GTO-based compensation systems for electric utility applications, IEEE Transactions on Power Delivery, pp. 2056-2064, vol.7, no.4, 1992
- [25] Hammad A. E.: Comparing the voltage control capabilities of present and future Var compensating techniques in transmission systems, IEEE Transactions on Power Delivery, pp. 475-484, vol.11, no.1, 1996
- [26] Nelson R. J.: Transmission power flow control: electronic versus electromagnetic alternatives for steady-state operation, IEEE Transactions on Power Delivery, pp. 1678-1684, vol.9, no.3, 1994

- [27] Nelson R. J., et al.: Transmission series power flow control, IEEE Transactions on Power Delivery, pp. 504-510, vol.10, no.1, 1995
- [28] Gyugyi L. et al.: The Unified Power Controller: a new approach to power transmission control, IEEE Transactions on Power Delivery, pp. 1085-1097, vol.10, no.2, 1995
- [29] Gyugyi L. et al.: Static synchronous series compensator: a solid-state approach to the series compensation of transmission lines, IEEE Transactions on Power Delivery, pp. 406-417, vol.12, no.1, 1997
- [30] Lindberg A.: PWM and control of two and three level high power Voltage Source Converters, Licentiate thesis TRITA-EHE 9501, Royal Institute of technology, Stockholm, Sweden, 1995
- [31] Ekanayake J.B., Jenkins N.: Performance of a three-level Advanced Static VAr Compensator, IEEE/KTH Stockholm Power Tech Conference, pp. 136-141, Stockholm, Sweden, 1995
- [32] Ekanayake J.B., Jenkins N.: A three-level Advanced Static VAr Compensator, IEEE Transactions on Power Delivery, vol.11, no.1, pp. 540-545, 1996
- [33] Stemmler H.: Scriptum Einführung in die Leistungselektronik, edition winter term 96, Chair of power electronics and electrometrology, Swiss Federal Institute of Technology, Zurich, Switzerland
- [34] Stemmler H.: Scriptum Leistungselektronische Systeme, Part 2, edition summer term 97, Chair of power electronics and electrometrology, Swiss Federal Institute of Technology, Zurich, Switzerland
- [35] Meyer M.: Leistungselektronik, Springer Verlag, Berlin, ISBN 3-540-52460-6, 1990
- [36] Steimer P. K. et al.: State-of-the-art verification of the hard driven GTO inverter development for a 100MVA Intertie, IEEE Power Electronics Specialists Conference (PESC), pp. 1401-1407, 1996
- [37] Jenni F., Wüest D.: Steuerverfahren für selbstgeführte Stromrichter, VDF Teubner, ISBN 3-519-06176-7, 1995
- [38] Carocci F., Zurlo L.: Regelung eines 3-Punkt-WR am Netz mit PSR II, diploma work LEM 9501, Chair of Power Electronics and Electrometrology, Swiss Federal Institute of Technology, Zurich, Switzerland, 1995
- [39] Neumann, K.: Operations research Verfahren, Vol.1, Carl Hanser Verlag, Munich, Vienna, 1975
- [40] Hoft R.G., Patel H.S.: Generalized techniques of harmonic elimination and voltage control in thyristor inverters, Part I, Harmonic elimination, IEEE Transactions on Industrial Applications, Vol. IA-9, pp. 310-317, 1973

- [41] Matlab User Manuals, The Math Works Inc., Natick, Mass. 01760, USA, 1992
- [42] Stemmler H.: Steuerverfahren für ein- und mehrpulsige Unterschwingungswechselrichter zur Speisung von Kurzschlussläufern, Ph. D. thesis, Rheinisch-Westfälische Technische Hochschule Aachen, 1970
- [43] Schönung, A., Stemmler H.: Static frequency changers with subharmonic control in conjunction with reversible variable speed AC-drives, Brown Boveri Review, August, September 1964
- [44] Steinke J. K.: Switching frequency optimal PWM control of a threelevel Inverter, IEEE Transactions on Power Electronics, pp. 487-496, vol.7, no.3, 1992
- [45] Guggenbach P.: Versetzte Taktung von zwei Wechselrichtern zur Speisung einer Induktionsmaschine mit offener Wicklung, Ph.D. Thesis 12104, Swiss Federal Institute of Technology, Zurich, Switzerland, 1997
- [46] CIGRE/IEEE: Guide for planning DC links terminating at AC-system locations having low short-circuit capacities, part 1, 1991
- [47] Thallam R. S.: Review of the design and performance features of HVDC systems connected to low short circuit ratio AC systems, IEEE Transactions on Power Delivery, vol.7, no.4, pp. 2065-2073, 1992
- [48] Lindberg A., Lindberg L.: Inner current loop for large voltage source Converters operating at low switching frequency, Power Electronics and Variable-speed Drives Conference (PEVD'94), pp. 217-222, 1994
- [49] Lindberg L.: Voltage source forced commutated converters for high power transmission applications, Licentiate thesis TRITA-EHE-Nr 3, Royal Institute of Technology, Stockholm, Sweden, 1990
- [50] Povh, D.: Einsatz der FACTS-Geräte in Hochspannungsnetzen, Talk at the FACTS seminary, Chair of power electronics and electrometrology, Swiss Federal Institute of Technology, Zurich, Switzerland, 1997
- [51] Jiang Y., Ekström Å.: General analysis of harmonic transfer through converters, IEEE Transactions on Power Electronics, vol.12, no.2, pp. 287-293, 1997
- [52] Bronstein I. N., Semendjajew K.A.: Taschenbuch der Mathematik, Verlag Harri Deutsch, 1981
- [53] Kovacs K. P.: Symmetrische Komponenten in Wechselstrommaschinen, Birkhäuser Verlag Basel und Stuttgart, 1962
- [54] Miller, T. J. E.: Reactive power control in electric systems, John Wiley & Sons, 1982
- [55] Gander W., Hrebicek J.: Solving problems in scientific computing using Maple and MATLAB, pp. 299-311, Springer Verlag, 2nd edition, 1995

- [56] Waldvogel J.: Circuits in power electronics, research report no. 94-13, chair for applied mathematics, Swiss Federal Institute of Technology, Zurich, Switzerland, 1994
- [57] Scheuer G., Stemmler H.: Analysis of a 3-level VSI Neutral-point-control for fundamental frequency modulated SVC-applications, 6th International AC and DC Transmission conference, pp. 303-310, London, United Kingdom, 1996
- [58] Föllinger O.: Laplace- und Fourier-Transformation, AEG-Telefunken AG, 3rd edition, 1982, ISBN 3-87087-125-3
- [59] Ekström Å.: Calculation of transfer functions for a forced-commutated Voltage Source Converter, IEEE Power Electronics Specialists Conference (PESC), pp. 330-337, Boston-MA, USA, 1991
- [60] Jiang Y., Ekström Å.: Study of the interaction oscillation between the AC-system and the forced-commutated Voltage Source Converter, First International Power Electronics and Motion Control Conference (IPEMC'94), pp. 1050-1055, Beijing, China, 1994
- [61] De Oliveira M. M., Jiang Y., Ekström Å.: Performance of conventional and advanced Static Var Compensators at low frequency resonance conditions, IEEE/KTH Stockholm Power Tech Conference, pp. 161-166, Stockholm, Sweden, 1995
- [62] De Oliveira M. M.: Theoretical analysis and real time simulator studies of an advanced Static Var Compensator, Licentiate thesis TRITA-EHE 9602, Royal Institute of Technology, Stockholm, Sweden, 1996
- [63] Klaver H. L.: Control of the Neutral point of a three-level -inverter, European Power Electronics conference (EPE'91), pp. 3-278 - 3-281, 1991
- [64] Matsui M.: Static Var Compensator using neutral-point-clamped PWM Inverter and its control scheme, International Power Electronics Conference IPEC-Yokohama '95, pp. 488-493, Yokohama, Japan, 1995
- [65] Tamai S. et al.: 3 Level GTO converter-inverter pair system for large capacity induction motor drive, European Power Electronics conference (EPE'93), pp. 45-50, 1993
- [66] Ekström Å.: Theoretical analysis and simulation of forced commutated Voltage Source Converters for FACTS applications, EPRI workshop Flexible AC Transmission System (FACTS), Cincinnati, Ohio, USA, 1990
- [67] De Oliveira M. M., Ekström Å.: Transfer function for a Voltage Source Converter operating as an SVC, 2nd Brazilian power electronics conference (COBEP 93), pp. 167-172, Uberlandia-MG, Brazil, 1993

- [68] Jiang Y.: Investigating behaviours of forced-commutated VSC as an SVC at abnormal system conditions, Licentiate thesis TRITA-EHE 9406, Royal Institute of Technology, Stockholm, Sweden, 1994
- [69] Jiang Y., Ekström Å.: Applying PWM to control overcurrents at unbalanced faults of forced-commutated VSCs used as Static Var Compensators, proceedings IEEE/KTH Stockholm Power Tech Conference, pp. 167-172, Stockholm, Sweden, 1995
- [70] Schauder C., Metha H.: Vector analysis and control of Advanced Static Var Compensators, 5th International AC and DC Transmission conference, pp. 266-272, London, United Kingdom, 1991
- [71] Unbehauen H.: Regelungstechnik I, Lineare kontinuierliche Regelsysteme, Vieweg, 7th edition, 1992, ISBN 3-528-63332-8
- [72] Stemmler H., Omlin A.: Converter controlled fixed frequency variable speed motor/generator, International Power Electronics Conference IPEC-Yokohama '95, pp. 170-176, Yokohama, Japan, 1995
- [73] Omlin A.: Untersuchung der unter/übersynchronen Kaskade mit einem Spannungszwischenkreis-Umrichter, Diss. ETH Nr. 12203, Chair of Power Electronics and Electrometrology, Swiss Federal Institute of Technology Zurich, 1997
- [74] Thanh-Nam Le: Kompensation schnell veränderlicher Blindströme eines Drehstromverbrauchers, etzArchiv Band 11, pp.249-253, 1989
- [75] Föllinger O.: Regelungstechnik, AEG-Telefunken AG, 3rd edition, 1980, ISBN 3-87087-116-4

List of symbols

Instantaneous/amplitude values

x	instantaneous value of the quantity x(t) in physical units
х	Amplitude value of a pure sinusoidal AC-quantity x(t) or average value of a time varying DC-quantity x(t) in physi- cal units
x	instantaneous value of the quantity $x(t)$ in [p.u.]
X	Amplitude value of a pure sinusoidal AC-quantity $x(t)$ or average value of a time varying DC-quantity $x(t)$ in [p.u.]

Electrical AC-side quantities ([p.u.] notation)

u _{Gph}	AC-system generator voltages, $ph = a,b,c$
u _{SP}	zero sequence voltage at the generator voltage starpoint or the secondary transformer starpoint
u _{Lph}	AC-system voltages at the primary side of the inverter transformer, $ph = a,b,c$
u _{Zph}	AC-side load voltages, $ph = a,b,c$
u _{ph}	3-level VSI output voltages, $ph = a,b,c$
U _{phsum}	3-level VSI output voltages generated by the sum of the two DC-side voltages u_{D1} and u_{D2} and the switching functions s_{ph} , $ph = a,b,c$
U _{phdiff}	3-level VSI output voltages generated by the difference of the two DC-side voltages u_{D1} and u_{D2} and the squared switching functions s_{ph}^2 , $ph = a,b,c$
i _{ph}	AC-side currents, $ph = a,b,c$
i _{phsum}	AC-side currents generated by u_{phsum} , $ph = a,b,c$
İ _{phdiff}	AC-side currents generated by u_{phdiff} , $ph = a,b,c$
I _{phpeak}	peak-values of the AC-side currents i_{ph}
S _{VSI}	nominal apparent power of the 3-level VSI
S _{ph-VSI}	apparent power of one 3-level VSI leg

2- or 3-level VSI DC-side quantities ([p.u.] notation)

u _D	2-level VSI DC-side voltage
u _{D1} , u _{D2}	upper (u_{D1}) and lower (u_{D2}) 3-level VSI DC-side voltage
u _{Dsum}	sum of the two 3-level VSI DC-side voltages u_{D1} and u_{D2}
u _{Ddiff}	difference of the two 3-level VSI DC-side voltages u_{D1} and u_{D2}
$\Delta \hat{u}_D$	peak-value of the harmonic voltage stress of the 2-level VSI DC-side voltage u_D
$\Delta \hat{u}_{D1/D2}$	peak-value of the harmonic voltage stress of the 3-level VSI DC-side voltages u_{D1} and u_{D2}
i _{D1} , i _{D2}	upper (i_{D1}) and lower (i_{D2}) 3-level VSI DC-side current
i _{Ddiff}	difference of i_{D1} and i_{D2} (= $i_{D1} - i_{D2}$)
<i>i</i> ₀	3-level VSI NP-current
<i>i</i> _{0_<i>i</i>_{<i>a</i>1}}	NP-current generated by the AC-side current fundamental i_{a1} of phase a
i _{0_i_{ph1}}	NP-current generated by all 3 AC-side current fundamen- tals i_{ph1}
<i>i</i> _{0_<i>i</i>_{a2}}	NP-current generated by the AC-side current neg. seq. 2nd harmonic i_{a2} of phase a
i _{0_i_{ph2}}	NP-current generated by all 3 AC-side current neg. seq. 2nd harmonics i_{ph2}
$I_{0DC_i_{nh}}$	NP-current DC-component caused by $i_{0_{i_{phl}}}$
$I_{0DC_{i_{nh2}}}$	NP-current DC-component caused by $i_{0_{-}i_{ph2}}$
$I_{0DC_{i_{nbl}+2}}$	NP-current DC-component caused by $i_{0_{-i_{phl}}}$ and $i_{0_{-i_{ph2}}}$
I _{ODC}	DC-component of the NP-current i_0 , including $I_{0DC_{-i_{phl+2}}}$ and the contributions of all higher ordered even and odd numbered AC-side current harmonics
i _D	DC-side load current from an energy source or sink

Electrical components ([p.u.] notation)

z	impedance
r	resistance of the inverter transformer (incl. the 3-level VSI losses)
r _L	resistance of the AC-system lines
r _{tot}	total resistance $r+r_L$ of the 3-level VSI- and the AC-system lines
l	stray inductance of the inverter transformer
l_L	inductance of the AC-system lines
l _{tot}	total inductance $l+l_L$ of the 3-level VSI- and the AC-system lines
с	individual 2- or 3-level VSI DC-side capacitance
c _{tot}	total installed 3-level VSI DC-side capacitance

Switching functions and related quantities

S	general 2- or 3-level VSI switching function
Sph	3-phase 2- or 3-level VSI switching functions, $ph = a,b,c$
s _{ph}	absolute value of the 3-phase 3-level VSI switching func- tions, $ph = a,b,c$
s ² _{ph}	squared 3-phase 3-level VSI switching functions, ph = a,b,c
S _{IFFM/IIFFM}	2-level VSI FFM switching functions used for the genera- tion of a 3-level VSI FFM switching function
S _{FFM}	3-level VSI FFM switching function
S _{FFMi}	<i>i</i> -th 3-level VSI FFM switching function used for the generation of a 3-level VSI PWM switching function
S _{PWM}	3-level VSI PWM switching function
c _I , c _{II}	carrier signals used for the generation of the 2-level VSI FFM switching functions <i>s</i> _{IFFM/IIFFM}

 cs_I, cs_{II}

- 413 -

cs _{ph}	pure sinusoidal 3-phase control signals used for the gener- ation of carrier based PWM switching functions
cs ₀	zero sequence component superimposed to cs _{ph}
CS _{ph+0}	3-phase control signals with superposition of the zero sequence component cs_0 for the generation of carrier based PWM switching functions
$c1_{ph}, c2_{ph}$	3-phase carrier signals for the generation of carrier based 3-level VSI PWM switching functions, $ph = a,b,c$
c _{ph}	3-phase carrier signals for the generation of carrier based 2-level VSI PWM switching functions, $ph = a,b,c$
m	modulation index of the switching functions s_{ph} (identical in all 3 phases)
m _{ph}	modulation indices of each individual 3-phase switching function s_{ph} , $ph = a,b,c$
Ν	number of switching angles in either a quarter, a half or in one period of a pulse pattern

Angles, frequencies and angular frequencies

D_{ph}	angles between the individual 3-phase quantities a, b and c
φ _u	angle between the 3-level VSI output voltages u_{ph} and the AC-system voltages u_{Lph}
α,	<i>i</i> -th switching angle of the switching functions s or s_{ph}
β	NP-angle of a 3-level VSI FFM switching function
β _i	i-th NP-angle of a general 3-level VSI switching function
γ	DC-side balance control angle
$\phi_{S_k}, \phi_{S_{phk}}$	phase-displacement of the k-th switching function har- monic s_k or s_{phk}
f	frequency
ω	angular frequency, $\omega = 2\pi \cdot f$

fundamental frequency
fundamental angular frequency
frequency of the 2nd harmonic
angular frequency of the 2nd harmonic
resonance frequency of the VSI
resonance angular frequency of the VSI
3dB cut-off frequency of a low-pass filter
3dB cut-off angular frequency of a low-pass filter
switching frequency of the general switching function s (f_s) or the 3-phase switching functions s_{ph} $(f_{s_{ph}})$
carrier frequency for carrier based PWM

Time and time constants

t	time in [rad]
$\tau_c, \tau_{c_{tot}}$	2- or 3-level VSI DC-side capacitor time constants in [msec]
$\tau_{cAC}, \tau_{c_{tat}AC}$	AC-side capacitor time constants in [msec]
τ _{bal}	balancing time constant of the two 3-level VSI DC-side voltages u_{D1} and u_{D2} in [sec]

Rotating phasor quantities

uL	rotating phasor of the AC-system voltages u_{Lph}
$u_{L\alpha}, u_{L\beta}$	α - and β - component of the rotating phasor $\dot{\vec{u}}_L$
<i>u</i> _{Lzero}	zero sequence component of the AC-system voltages u_{Lph}
ì	rotating phasor of the AC-side currents i_{ph}
i _α , i _β	α - and β -component of the rotating phasor i
S	rotating phasor of the switching functions s_{ph}
s _α , s _β	α -and β -component of the rotating phasor \dot{s}
Szero	zero sequence component of the switching functions s_{ph}
\vec{s}^2	rotating phasor of the squared switching functions s^2_{ph}

$s^2_{\alpha}, s^2_{\beta}$	α -and β -component of the rotating phasor $\vec{s^2}$
s ² zero	zero sequence component of the squared switching functions s_{ph}^2

Phasor quantities

<u><u>u</u>_L</u>	phasor of the AC-system voltages u_{Lph} , d/q frame rotating with an angular velocity $k\omega_1$
$u_{Ld}^{}, u_{Lq}^{}$	d and q component of the phasor \underline{u}_L , d/q frame rotating with an angular velocity $k\omega_1$
<u>u</u> _'	phasor of the AC-system voltages u_{Lph} , d/q frame rotating with an angular velocity ω_1
u_{Ld}', u_{Lq}'	d and q component of the phasor \underline{u}_L ', d/q frame rotating with an angular velocity ω_1
<u>u</u> _"	phasor of the AC-system voltages u_{Lph} , d/q frame rotating with an angular velocity $-2\omega_1$
u_{Ld} ", u_{Lq} "	d and q component of the phasor \underline{u}_L ", d/q frame rotating with an angular velocity $-2\omega_1$
Щ	phasor of the 3-level VSI output voltages u_{ph} , d/q frame rotating with an angular velocity $k\omega_1$
<u>u</u> '	phasor of the 3-level VSI output voltages u_{ph} , d/q frame rotating with an angular velocity ω_1
i	phasor of the AC-side currents i_{ph} , d/q frame rotating with an angular velocity $k\omega_1$
i_d, i_q	d and q component of the phasor <i>i</i> , d/q frame rotating with an angular velocity $k\omega_1$
<u>į</u>	phasor of the AC-side currents i_{ph} , d/q frame rotating with an angular velocity ω_1
i_d', i_q'	d and q component of the phasor i' , d/q frame rotating with an angular velocity ω_1
<i>i</i> "	phasor of the AC-side currents i_{ph} , d/q frame rotating with an angular velocity $-2\omega_1$
i_{d} ", i_{q} "	d and q component of the phasor $i^{"}$, d/q frame rotating with an angular velocity $-2\omega_1$

2	phasor of the switching functions s_{ph} , d/q frame rotating with an angular velocity $k\omega_1$
s _d , s _q	d and q component of the phasor s, d/q frame rotating with an angular velocity $k\omega_1$
<u>s</u> '	phasor of the switching functions s_{ph} , d/q frame rotating with an angular velocity ω_1
s_d , s_q	d and q component of the phasor $\underline{s}',$ d/q frame rotating with an angular velocity ω_1
<u>s</u> "	phasor of the switching functions s_{ph} , d/q frame rotating with an angular velocity $-2\omega_1$
s_d ", s_q "	d and q component of the phasor $\underline{s}^{\prime\prime},$ d/q frame rotating with an angular velocity $-2\omega_1$
$\underline{s^2}$	phasor of the squared switching functions s_{ph}^2 , d/q frame rotating with an angular velocity $k\omega_1$
s_{d}^{2}, s_{q}^{2}	d and q component of the phasor $\underline{s^2}$, d/q frame rotating with an angular velocity $k\omega_1$
$\underline{s^{2'}}$	phasor of the squared switching functions s_{ph}^2 , d/q frame rotating with an angular velocity ω_1
s_{d}^{2}, s_{q}^{2}	d and q component of the phasor $\underline{s^{2'}}$, d/q frame rotating with an angular velocity ω_1
<u>s²"</u>	phasor of the squared switching functions $s^2{}_{ph}$, d/q frame rotating with an angular velocity $-2\omega_1$
s_{d}^{2} , s_{q}^{2}	d and q component of the phasor $\underline{s^{2"}}$, d/q frame rotating with an angular velocity $-2\omega_1$

Linearized phasor quantities

U_{Ld0}, U_{Lq0}	steady-state operation points of u_{Ld} and u_{Lq}
$\Delta u_{Ld}, \Delta u_{Lq}$	deviations of u_{Ld} and u_{Lq} from the steady-state operation points U_{Ld0} and U_{Lq0}
U_{Ld0}', U_{Lq0}'	steady-state operation points of u_{Ld} and u_{Lq}
$\Delta u_{Ld}', \Delta u_{Lq}'$	deviations of u_{Ld}' and u_{Lq}' from the steady-state opera- tion points U_{Ld0}' and U_{Lq0}'
U_{Ld0} ", U_{Lq0} "	steady-state operation points of u_{Ld} " and u_{Lq} "

Δu_{Ld} ", Δu_{Lq} "	deviations of u_{Ld} " and u_{Lq} " from the steady-state opera- tion points U_{Ld0} " and U_{Lq0} "
I_{d0}, I_{q0}	steady-state operation points of i_d and i_q
$\Delta i_d, \Delta i_q$	deviations of i_d and i_q from the steady-state operation points I_{d0} and I_{q0}
I _{d0} ', I _{q0} '	steady-state operation points of i_d and i_q
$\Delta i_d', \Delta i_q'$	deviations of i_d and i_q from the steady-state operation points I_{d0} and I_{q0}
I _{d0} ", I _{q0} "	steady-state operation points of i_d " and i_q "
Δi_d ", Δi_q "	deviations of i_d " and i_q " from the steady-state operation points I_{d0} " and I_{q0} "
S_{d0}, S_{q0}	steady-state operation points of s_d and s_q
$\Delta s_d, \Delta s_q$	deviations of s_d and s_q from the steady-state operation points S_{d0} and S_{q0}
S_{d0}', S_{q0}'	steady-state operation points of s_d and s_q
$\Delta s_d', \Delta s_q'$	deviations of s_d' and s_q' from the steady-state operation points S_{d0}' and S_{q0}'
S_{d0} ", S_{q0} "	steady-state operation points of s_d and s_q .
Δs_d ", Δs_q "	deviations of s_d " and s_q " from the steady-state operation points S_{d0} " and S_{q0} "
S^2_{d0}, S^2_{q0}	steady-state operation points of s_d^2 and s_q^2
Δs_d^2 , Δs_q^2	deviations of s_d^2 and s_q^2 from the steady-state operation points S_{d0}^2 and S_{q0}^2
S^2_{d0}', S^2_{q0}'	steady-state operation points of s_d^2 and s_q^2
Δs^2_d ', Δs^2_q '	deviations of s_{d}^{2} and s_{q}^{2} from the steady-state operation points S_{d0}^{2} and S_{q0}^{2}
S^2_{d0} ", S^2_{q0} "	steady-state operation points of s_d^2 and s_q^2
Δs^2_d ", Δs^2_q "	deviations of s_d^2 " and s_q^2 " from the steady-state opera- tion points S_{d0}^2 " and S_{q0}^2 "
Φ_{u0}	steady-state operation point for the angle ϕ_u
Δφ _u	deviations of the angle φ_{u} from the steady-state operation point Φ_{u0}

<i>M</i> ₀	steady-state operation point for the modulation index m of the switching functions s_{ph}
Δm	deviations of the modulation index m from the steady- state operation point M_0
U _{Dsum0}	steady-state operation point of u_{Dsum}
Δu_{Dsum}	deviations of u_{Dsum} from the steady-state operation point U_{Dsum0}
U_{Ddiff0}	steady-state operation point of u_{Ddiff}
Δu_{Ddiff}	deviations of u_{Ddiff} from the steady-state operation point U_{Ddiff0}
<i>I</i> _{D0}	steady-state operation point of the 3-level VSI DC-side load current i_D
Δi_D	deviations of the 3-level VSI DC-side load current i_D from the steady-state operation point I_{D0}

Indices

k, l, p	harmonic orders
i, j, n	running indices
pos	positive sequence component
neg	negative sequence component
zero	zero sequence component
max	maximum value
ref	reference value
refpos	reference value for a fundamental positive sequence quan- tity
refneg	reference value for a fundamental negative sequence quantity
fil	filtered quantity
aux	auxiliary variable

Miscellaneous quantities

SCR	Short Circuit Ratio
corr _i	correction factor for the worst case harmonic distortion of the AC-side currents with respect to a specific AC-system strength
corr _{uL}	correction factor for the worst case harmonic distortion of the AC-system voltages with respect to a specific AC-sys- tem strength
Δh_{ev}	correction factor; contribution of higher ordered even numbered harmonics of s_{ph} to a DC-component in the NP-current i_0
I _{q0crit}	critical (capacitive) operation point for the DC-side bal- ance control scheme of type II
THD _i	total harmonic distortion of the AC-side currents i_{ph}
THD _{uL}	total harmonic distortion of the AC-system voltages u_{Lph}

Abbreviations

FFM	Fundamental Frequency Modulation
PWM	Pulse Width Modulation
VSI	Voltage Source Inverter
SVC	<u>Static Var Compensator</u>
NP	Neutral Point
SP	Secondary transformer starPoint
SCR	Short Circuit Ratio
IGBT	Insulated Gate Bipolar Transistor
GTO	Gate Turn-Off Thyristor
THD	Total Harmonic Distortion

Leer - Vide - Empty

Curriculum vitae

16. 8. 1962	Born in Ludwigshafen/Rhein, Germany
1969 - 1973	Primary school in Ludwigshafen/Rhein, Germany
1973 - 1982	Scientific Grammar school in Ludwigshafen/Rhein, Germany
1982	Mechanical and electrical laboratory course at Siemens AG in Mannheim, Germany
1982 - 1989	Diploma course in electrical engineering at the Technical University of Karlsruhe, Germany
November 1989	Diploma degree in electrical engineering of the Technical University of Karlsruhe, Germany
1983 - 1988	Part-time employment at Siemens AG in Mannheim and Karlsruhe, Germany
1984 - 1987	Part-time employment at the Institute for Automation and Robotics of the Technical University of Karlsruhe, Germany
since 1990	Research and teaching assistant at the Chair of Power Electronics and Electrometrology of the Swiss Federal Institute of Technology Zurich, Switzerland

Leer - Vide - Empty

Lebenslauf

16. 8. 1962	Geboren in Ludwigshafen am Rhein, Deutschland
1969 - 1973	Grundschule in Ludwigshafen am Rhein
1973 - 1982	staatliches, naturwissenschaftliches Gymnasium in Ludwigshafen am Rhein
Juni 1982	Allgemeine Hochschulreife (Abitur)
Juli - September 1982	Praktikum bei der Firma Siemens AG in Mannheim
1982 - 1989	Studium der Elektrotechnik an der Technischen Hochschule in Karlsruhe
November 1989	Abschluss in Elektrotechnik mit Diplom als Dipl. Ing. TH
1983 - 1988	Werksstudententätigkeiten bei der Firma Siemens AG in Mannheim und Karlsruhe
1984 - 1987	Hilfswissenschaftler am Institut für Prozess- rechentechnik und Robotik der Universität Karls- ruhe
seit 1990	Assistent für Forschung und Lehre an der Professur für Leistungselektronik und Messtechnik der ETH Zürich