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Analysis and Multi-Objective Optimization of Multi-Cell DC/DC and AC/DC Converter Systems

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Für Angela

"An experiment is a question which science poses to Nature, and a measurement is the recording of Nature's answer."

Max Planck

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Zurich, April 2016
Matthias Kasper

Contents

Kurzfassung

Hinter vielen globalen Megatrends, die unser Leben als Individuen und als Gesellschaft in vielen verschiedenen Bereichen beeinflussen, steht die Leistungselektronik als eine der Schlüsseltechnologien, die diese Trends ermöglichen. Prominente Beispiele sind hierbei die sukzessive Umstellung der Energieversorgung von konventionellen, fossilen Energieträgern auf erneuerbare Energiequellen, die Reduktion der ausgestossenen Treibhausgase durch Elektrifizierung der Mobilität und der Trend in der Informationstechnolgie zu cloud-basierten Anwendungen, die auch durch die Entwicklung von kostengünstigen, effizienten und kompakten leistungselektronischen Konvertersystemen ermöglicht werden. Um die zukünftigen Anforderungen an die Leistungselektronik erfüllen zu können, ist es daher wichtig, dass neue Wege zur Entwicklung von leistungselektronischen Systemen mit erhöhter Effizienz, Leistungsdichte und Zuverlässigkeit aufgezeigt werden.

Das Studium der Fachliteratur zeigt, dass die Fortschritte bei der Entwicklung von leistungselektronischen Systemen hauptsächlich entweder durch Weiterentwicklungen auf Ebene der Komponenten zustande kommen, oder auf der modifizierten Steuerung und Regelung bekannter Schaltungstopologien basieren. Diese beiden Ansätze sind evolutionärer Natur und versprechen daher auf absehbare Zeit nur schrittweise Verbesserungen gegenüber heutigen Konzepten.

Ein vielversprechender und grundlegend anderer Ansatz, um die zukünftigen Anforderungen an leistungselektronische Systeme zu erfüllen, ist die Entwicklung von Multizellen-Konvertersystemen, bei denen mehrere Teilsysteme (Zellen) in einem Verbund zusammenarbeiten. Bezüglich der Performancekriterien (z.B. Effizienz und Leistungsdichte) des Gesamtsystems ergeben sich hierbei Vorteile, da die einzelnen Zellen mit geringerer Leistung und daher mit geringerer Spannung und/oder geringeren Strömen arbeiten können, als ein entsprechendes Einzellenkonvertersystem. Die Entwicklung von Multizellenkonvertern eröffnet darüber hinaus neue Freiheitsgrade z.B. hinsichtlich der Zellenzahl und Koordination der Regelung der einzelnen Zellen im Kontext des Gesamtsystems. Es liegt allerdings bisher keine systematische Beschreibung aller Betriebskonzepte und Designmöglichkeiten von Multizellenkonvertern vor, welche jedoch für eine umfassende Mehrkriterien-Optimierung bzw. einen daraus resultierenden aussagekräftigen Vergleich mit derzeitigen Lösungen eine zwingende Voraussetzung darstellt.

Der Schwerpunkt der Dissertation liegt daher auf der umfassenden

Analyse und Beschreibung von Multizellensystemen für verschiedene Hauptanwendungsbereiche leistungselektronischer Konverter, wobei jeweils mittels Mehrkriterien-Optimierung einerseits ein neues System erstellt und andererseits z.B. hinsichtlich Effizienz und Leistungsdichte vorhandene Lösungen vergleichend gegenübergestellt werden. Hierzu werden in einem ersten Schritt in **Kapitel 2** die Vorteile von Multizellensystemen gegenüber Einzellenkonvertern auf Basis von Skalierungsgesetzen und theoretischen Modellen aufgezeigt.

Anschliessend werden für die Anwendung bei photovoltaischen Energiesystemen in **Kapitel 3**, für die Entwicklung eines hocheffizienten Netzteils für Datenzentren in **Kapitel 4** und für die Entwicklung einer Hilfsenergieversorgung mit hohem Spannungsübersetzungsverhältnis in **Kapitel 5** verschiedene Lösungsansätze mit Multizellenkonvertern analysiert. Hierbei werden jeweils auf Basis analytischer Beschreibungen und Simulationen umfassende Optimierungen durchgeführt. Ausserdem wird die Abhängigkeit zwischen den Zielgrössen Leistungsdichte und Effizienz bzw. der bei einem Design zwischen diesen Performanceindikatoren zu schliessende Kompromiss geklärt. Die Ergebnisse der Optimierungen werden jeweils durch Messungen an Laborprototypen verifiziert. Darüber hinaus werden auch die Freiheitsgrade in der Regelung bzw. im Zusammenspiel der einzelnen Zellen zu Etablierung der Gesamtfunktion analysiert und gegenüber konventionellen Lösungen evaluiert.

Abschliessend werden in **Kapitel 6** die wichtigsten Ergebnisse dieser Arbeit zusammengefasst und mögliche zukünftige Forschungsthemen kurz diskutiert.

Abstract

One of the key enabling technologies behind many global megatrends, which are affecting our lives as individuals and as a society in many different areas, is power electronics. Prominent examples are the shift from conventional energy sources to renewable energy sources, the reduction of greenhouse gas emissions due to the electrification of mobility, and the trend towards cloud-computing in the information technology area, which are all based on the development of cost-effective, efficient and compact power electronic systems. In order to fulfill future requirements for power electronic systems, it is therefore of great importance to identify new ways to develop systems with higher efficiency, power density, and reliability.

The analysis of relevant literature reveals, that improvements of power electronic systems are to a great extent either based on the improvements of specific components or on the modification of known control algorithms and/or topologies. These improvement processes, however, are of evolutionary nature and are not going to provide significant steps of performance improvements compared to today's solutions for the foreseeable future.

A very promising and fundamentally different approach, in order to fulfill the future demands for power electronic systems, is the development of multi-cell converter systems consisting of multiple converter cells connected together. Several advantages are obtained with respect to different performance criteria (e.g. efficiency and power density) of the full system by employing multiple converter cells with lower power rating that share the voltage and/or the current. The development of multi-cell converter systems creates new degrees of freedom regarding e.g. the number of employed cells and the control of the individual cells of the multi-cell system. Until now there has not been a comprehensive analysis and investigation of possible modulation schemes and converter designs of multi-cell systems, which clearly indicates the mandatory requirement for a multi-objective optimization and a comprehensive comparison to state-of-the-art solutions.

The main focus of this thesis is thus set on the comprehensive analysis and description of multi-cell converter systems for different application areas. For each specific application a multi-objective optimization is performed for novel multi-cell converter solutions and compared to state-of-the-art solutions with respect to e.g. the achievable efficiency and power density. In a first step, different fundamental scaling laws

and theoretical models are derived in **Chapter 2**, which reveal the advantages of multi-cell systems compared to single-cell systems.

Consequently, different multi-cell converter solutions are analyzed for photovoltaic energy systems in **Chapter 3**, for the development of a high efficiency telecom power suppy in **Chapter 4**, and for the development of an auxiliary power supply with high voltage conversion ratio in **Chapter 5**. Based on analytical descriptions of the converters and simulations, comprehensive multi-objective optimizations are performed, which identify the trade-off between the achievable power-density and efficiency. The results of the optimizations are then verified by measurements on hardware demonstrators. Furthermore, the additional degree of freedom in the control of the multi-cell system by controlling the individual cells is investigated and compared to conventional solutions.

Finally, **Chapter 6** summarizes and concludes the main achievements of the thesis and presents an outlook on possible future research work.

1 Introduction

Our future as a society, but also as individuals is to a great extent shaped by fundamental global trends that have a far-reaching impact on different aspects of our lives [1, 2]. These *megatrends* are major shifts of economic, social and environmental conditions which are happening on a global scale and affect economies, businesses, societies, cultures, and individuals. For many of these megatrends power electronics is a key enabling technology and/or a mandatory prerequisite for the ongoing development of these trends. The most important megatrends among those are:

- *Changing demographics*: Besides the trend of a growing and aging society, the increasing urbanization is posing a problem to existing cities. They have to cope with a growing population, which also implies the extension and adaptation of the public transport infrastructure. This requires the wide-spread application of power electronics in subway trains, electric buses and/or light-rail transit systems.
- *Scarcity of resources*: The dwindling supplies of fossil fuels in combination with a soaring energy demand in emerging countries is urging to shift the power generation to renewable energy sources, such as photovoltaics, wind power and wave power. The grid integration of renewable energy sources on a large scale, however, can only be achieved by employing power electronics in so-called smart grids.
- *Climate change*: The increasing concentration of greenhouse gases in the atmosphere is the main driver of rising temperatures. Among

the greenhouse gases, CO_2 is the most important gas with a concentration influenced to a great extent by mankind. Here, power electronics is the key technology to make a valuable contribution to reduce the CO_2 footprint of humans. In this context, especially the electrification of mobility, with the development of hybrid and fully electric vehicles, electric buses and more electric aircraft, has experienced a strong growth in past years.

- *Technological breakthroughs*: The importance of technology in our lives will increase since innovation cycles become shorter and new technologies are being adopted faster. One major technological trend is the Internet-of-Things which is a mix of the internet, mobile devices, data analytics and cloud computing. This has initiated a tremendous growth of data centers around the world, which has triggered the power electronic research for highly efficient power supplies for data centers.

Since power electronics is behind many important global megatrends, further and continuous improvements of power electronic systems are a mandatory prerequisite to guarantee the advancement of these trends.

1.1 Drivers of Performance Improvements in Power Electronic Systems

The development of power electronic converter systems towards more efficient, compact and cost effective systems is nowadays to a large extent driven by the performance improvement of power electronic components and/or by a higher level of integration [3]. These improvement processes primarily focus on semiconductors (e.g development of the insulated-gate bipolar transistor (IGBT) [4] or the super-junction MOSFET [5]), magnetic materials, capacitors, heat-sinks, sensor ICs, chip embedding in printed circuit boards (PCB), and new packaging options. However, they evolve only over longer periods of time that often span decades; the development and market introduction of wide-bandgap semiconductors, which started about two decades ago, could serve as an example here. Another way of improving the performance of power electronic systems is the development of new topologies, which is able to shift the system performance (e.g. efficiency, power density and system cost) to

(a) (b) (c)

Fig. 1.1: Application areas of multi-cell converters which are adressed in this thesis: (a) mitigation of the partial shading problem in photovoltaic systems, (b) design of a highly efficient single-phase telecom rectifier supply, and (b) desgin of an auxiliary power supply with a high voltage conversion ratio as found in e.g. railway applications.

new levels in a much shorter time. However, many newly developed topologies are based on adding components to standard topologies [6], which improves individual performance aspects of the basic system but also leads to a higher system complexity and often reduced reliability, since the failure rate increases with increasing component count [7].

In contrast to the development of new technologies and entirely new topologies, this thesis proposes a new path towards improved system performance by employing existing and well-known topologies as building blocks (i.e. converter cells) in multi-cell converter systems where the cell terminals are connected in series or in parallel. The multi-cell systems are then optimized by the methodology of a multi-objective optimization to reveal the achievable performance trade-off of the entire system between the efficiency and the power density. This is done by mapping the design space, which contains all degrees of freedom in the design of a multi-cell system, into the performance space by means of mathematical system and components models.

1.2 Multi-Cell Converter Approach

The first literature references of multi-cell converters date back more than 40 years to the 1970s [8, 9]. In the subsequent decades, multi-cell converters have been established primarily in medium- to high-voltage high-power applications such as traction applications [10–14], offshore wind energy systems [15, 16], and in Solid-State Transformers (SSTs) [17–19]. For these applications with high operating voltages like interfacing a medium voltage grid of 10 kV, the lack of suit-

able power semiconductors with sufficient blocking voltage (typically limited to 6.5 kV) necessitates the application of multi-cell or multi-level topologies where the operating voltage is shared among many in series connected semiconductor devices [20]. Here, the cascaded H-bridge (CHB) topology has gained significant interest and has been used in a wide range of applications, e.g., in smart grid applications / SSTs [18, 19], STATCOMs [21, 22], medium voltage drives [23, 24], and railway applications [11–14]. Additional advantages are obtained due to the multi-level voltage waveform, including reduced harmonic distortion and lower electromagnetic interference.

The focus of this thesis, however, is on the application of multi-cell topologies in the power range of up to a few Kilowatts with semiconductors with a voltage rating of up to 1 kV with the goal of demonstrating the benefits of the multi-cell approach in this power and voltage range. In order to show the versatility of the multi-cell converter concept, a broad range of different applications is covered in this thesis. The analyzed applications consist of photovoltaic energy systems, where the multi-cell approach allows to mitigate the unfavorable effects of partial shading, the development of a highly efficient single-phase telecom rectifier system, and an auxiliary supply for high voltage conversion ratio (cf. **Fig. 1.1**).

1.3 Goals and Contributions of the Thesis

The objective of this thesis is to comprehensively analyze, develop and optimize multi-cell converter solutions for different applications by considering suitable converter topologies and control schemes. The results are verified with simulations and/or measurements of hardware prototypes. The main contributions of the thesis are given in the following:

- The thesis presents a *comprehensive analysis of scaling laws of multi-cell systems* that reveal the dependency of different performance and operating aspects of multi-cell systems on the number of employed cells. The scaling laws allow to predict certain fundamental performance trends inherent to the multi-cell approach.
- For *various applications*, ranging from DC/DC to AC/DC conversion, different multi-cell converter concepts are analyzed in detail. This includes the identification of suitable multi-cell topologies,

the design, the multi-objective optimization, and the implementation of hardware demonstrators for each type of application.

- The *multi-objective optimization* of each multi-cell converter system employs detailed and comprehensive system and component models in the electric, magnetic and thermal domain.
- The additional degrees of freedom in the operation of a multi-cell converter system are investigated and a *novel 4D-interleaving control concept* is introduced, which allows to improve the system performance (i.e. efficiency and power density) even further.
- A *novel scalable multi-cell converter topology* for the application as auxiliary supply with a high step-down ratio is proposed.
- A *detailed analysis of the soft-switching behavior* of power MOSFETs and of the losses associated with incomplete soft-switching is provided.

1.4 Outline of the Thesis

The main goal of this thesis is to provide the reader with a fundamental understanding of the multi-cell approach by presenting general scaling laws common to all multi-cell converter systems, and a selection of applications where specific multi-cell converter solutions are analyzed and optimized in detail.

In order to provide an introduction and to give a motivation to investigate the multi-cell converter approach in detail, fundamental scaling laws of multi-cell systems are presented in **Chapter 2**. Different types of multi-cell systems are introduced and the effects of series- and parallel-interleaving of the converter cells are discussed with the example of boost converters.

In **Chapter 3** the problem of partial shading in PV-systems is discussed and four different DC/DC multi-cell converter solutions are analyzed in detail and optimized by means of multi-objective optimizations. The presented solutions include full-power and partial-power conversion in series- and parallel-interleaved multi-cell systems. Where applicable, the optimization results are validated with hardware demonstrators.

As an example for a multi-cell converter for AC/DC conversion, the application of a telecom rectifier power supply module is presented and analyzed in **Chapter 4**. The system is investigated regarding the

implications of the multi-cell approach for AC/DC conversion and then optimized with the aim of achieving a high conversion efficiency. In addition, a highly efficient prototype in combination with measurement results is presented.

Another application for multi-cell converters is the DC/DC conversion with low power but high conversion ratios, which is analyzed in **Chapter 5**. Here, a scalable auxiliary power supply topology is introduced and analytically described. Furthermore, a prototype verifying the derived models is presented.

Finally, the thesis concludes in **Chapter 6** with a summary and gives an outlook on subjects of future research related to different aspects of multi-cell systems.

1.5 List of Publications

Different parts of the research findings presented in this dissertation and of other research projects carried out in parallel have already been published or will be published in international scientific journals, conference proceedings, workshops, and/or have been protected by multi-national patents. The publications developed in the course of this Ph.D. thesis are listed below.

Journal Papers

- M. Kasper, D. Bortis, and J. W. Kolar, "Design of String Current Diverters for Balancing Local Asymmetries," *IEEE Trans. Power Electron.*, *submitted for review.*
- M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Design of a Highly Efficient (97.7%) and Super-Compact (2.2kW/dm^3) Isolated AC/DC Telecom Power Supply Module Based on the Multi-Cell ISOP Converter Approach," *IEEE Trans. Power Electron.*, *early access.*
  DOI: 10.1109/TPEL.2016.2633334
- M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of Power MOSFETs Revisited," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
  DOI: 10.1109/TPEL.2016.2574998

- M. Kasper, D. Bortis and J. W. Kolar, "Classification and Comparative Evaluation of PV Panel-Integrated DC/DC Converter Concepts," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2511–2526, May 2014.
  DOI: 10.1109/TPEL.2013.2273399

Conference Papers

- M. Kasper, M. Antivachis, D. Bortis, and J. W. Kolar, "4D-Interleaving of Isolated ISOP Multi-Cell Converter Systems for Single Phase AC/DC Conversion," in *Proc. of the Int. Conf. on Power Conversion and Intelligent Motion (PCIM)*, 2016.
- M. Kasper, C. W. Cheng, D. Bortis, G. Deboy, and J. W. Kolar, "Hardware Verification of a Hyper-Efficient (98%) and Super-Compact (2.2kW/dm^3) Isolated AC/DC Telecom Power Supply Module Based on Multi-Cell Converter Approach," in *Proc. of the IEEE Applied Power Electronics Conference (APEC)*, 2015.
  DOI: 10.1109/APEC.2015.7104333
  Honor: Best Presentation Award
- M. Kasper, D. Bortis, G. Deboy, and J. W. Kolar, "Hyper-Efficient (98%) and Super-Compact (3.3kW/dm^3) Isolated AC/DC Telecom Power Supply Module Based on Multi-Cell Converter Approach," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, 2014.
  DOI: 10.1109/ECCE.2014.6953388
- M. Kasper, S. Herden, D. Bortis, and J. W. Kolar, "Impact of PV String Shading Conditions on Panel Voltage Equalizing Converters and Optimization of a Single Converter System with Overcurrent Protection," in *Proc. of the 16th IEEE European Conference on Power Electronics and Applications (EPE-ECCE Europe)*, 2014.
  DOI: 10.1109/EPE.2014.6910859
- M. Kasper, D. Bortis, and J. W. Kolar, "Scaling and Balancing of Multi-Cell Converters," in *Proc. of the International Power Electronics Conference (IPEC-ECCE Asia)*, 2014.
  DOI: 10.1109/IPEC.2014.6869875
- M. Kasper, D. Bortis, and J. W. Kolar, "Novel High Voltage Conversion Ratio "Rainstick" DC/DC Converters," in *Proc. of*

the Energy Conversion Congress and Exposition (ECCE USA), 2013.
DOI: 10.1109/ECCE.2013.6646783

- M. Kasper, M. Ritz, D. Bortis, and J. W. Kolar, "PV Panel-Integrated High Step-Up High Efficiency Isolated GaN DC-DC Boost Converter," in *Proc. 35th IEEE Int. Telecommunications Energy Conf. (INTELEC)*, 2013.
- M. Kasper, D. Bortis, T. Friedli, and J. W. Kolar, "Classification and Comparative Evaluation of PV Panel-Integrated DC–DC Converter Concepts," in *Proc. of the 15th IEEE Int. Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012.
DOI: 10.1109/EPEPEMC.2012.6397403

Workshop

- M. Kasper, G. Deboy, and J. W. Kolar, "98.5% / 1.5kW/dm^3 Multi-Cell Telecom Rectifier Module (230VAC/48VDC) - Breaking the Pareto Limit of Conventional Converter Approaches ," *ECPE Workshop "Advanced Multi-Cell / Multi-Level Power Converters"*, Toulouse, France, July 1-2, 2014.

Patents

- M. Kasper, C.W. Chen, and J. W. Kolar, "Switching Frequency Modulation in a Switched-Mode Power Supply," United States Patent Application No. 15/294,552, filed on Oct. 14, 2016.
- M. Kasper, G. Deboy, and J. W. Kolar, "Power Converter with a Snubber Circuit," United States Patent Application No. 15/049,725, filed on Feb. 22, 2016.
- M. Kasper, G. Deboy, and J. W. Kolar, "Multi-Cell Power Conversion Method with Failure Detection and Multi-Cell Power Converter," United States Patent Application No. 14/638,517, filed on March 4, 2015.
- M. Kasper, G. Deboy, and J. W. Kolar, "Multi-Cell Power Conversion Method and Multi-Cell Power Converter (4),"
  - German Patent Application No. 102015115042.5, filed on Sept. 8, 2015.

  - United States Patent Application No. 14/479,987, filed on Sept. 8, 2014.

- M. Kasper, G. Deboy, and J. W. Kolar, "Multi-Cell Power Conversion Method and Multi-Cell Power Converter (3),"
  - German Patent Application No. 102015115041.7, filed on Sept. 8, 2015.
  - United States Patent Application No. 14/479,904, filed on Sept. 8, 2014.

- M. Kasper, G. Deboy, and J. W. Kolar, "Multi-Cell Power Conversion Method and Multi-Cell Power Converter (2),"
  - German Patent Application No. 102015115069.7, filed on Sept. 8, 2015.
  - United States Patent Application No. 14/479,854, filed on Sept. 8, 2014.

- M. Kasper, G. Deboy, and J. W. Kolar, "Multi-Cell Power Conversion Method and Multi-Cell Power Converter (1),"
  - German Patent Application No. 102015115037.9, filed on Sept. 8, 2015.
  - United States Patent Application No. 14/479,711, filed on Sept. 8, 2014.

- D. Bortis, M. Kasper, and J. W. Kolar, "Vorrichtung zur Gleichspannungswandlung für hohe Übersetzungsverhältnisse (DC/DC Converter for Converting High Input Voltage Into Low Output Voltage)," Swiss Patent Application No. CH 707447A2, filed on Jan. 15, 2013, published on July 15, 2014.

2

Fundamental Scaling Laws of Multi-Cell Converters

In order to provide a basis for an in-depth analysis of multi-cell systems for the different applications in the next chapters, this chapter first introduces fundamental scaling laws of power electronic converters. Subsequently, the benefits of multi-cell converter systems are discussed in detail with the examples of parallel and series connected multi-cell boost converters in comparison to a single-cell boost converter system. In a third step, the challenges associated with multi-cell converter system realizations are addressed.

2.1 Basic Scaling Laws of Power Electronic Converters

Multi-cell topologies can in general be classified as converter systems consisting of two or more subsystems that are connected in one of the following configurations: input-series output-parallel (ISOP), input-series output-series (ISOS), input-parallel output-series (IPOS) or input-parallel output-parallel (IPOP) [25] (cf. **Fig. 2.1**). For the case of distributed sources or loads, only terminals of one side of the cells might be connected in a parallel or series while the terminals of the other side are connected individually to the distributed sources or loads, respectively. This is the case for PV system, where each PV panel constitutes an individual power source, and for battery systems, where each converter cell is connected to one or more battery cells.

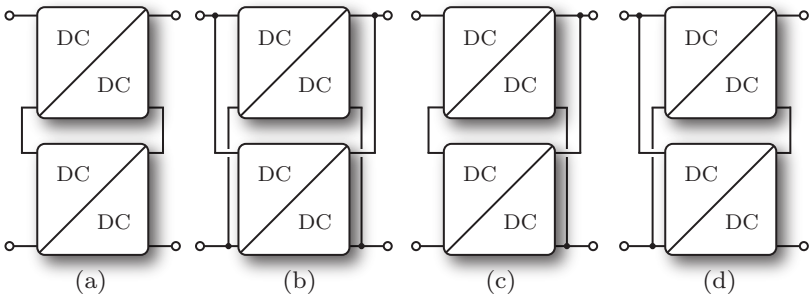

Fig. 2.1: Overview of different multi-cell converter configurations: (a) input-series output-series (ISOS), (b) input-parallel output-parallel (IPOP), (c) input-series output-parallel (ISOP), and (d) input-parallel output-series (IPOS) connection of the converter terminals.

The different types of configurations allow to either share the current between the converter cells with parallel connected terminals or distribute the voltage between the converter cells with series connected terminals. As a result of splitting either the current or the voltage among the converter cells, the system power is also split in such way that each cell transfers only a fraction of the total power.

The concept of splitting the overall system into smaller subsystems with relatively low power rating leads to benefits that can be leveraged to improve one or more performance criteria (e.g. efficiency and power density) of the overall system.

As derived in **Appendix A**, the volume V of a power electronic system with output power P scales compared to a reference system (V_0, P_0) with

$$\frac{V}{V_0} = \left(\frac{P}{P_0}\right)^{3/2} \tag{2.1}$$

under the assumption of a constant efficiency (i.e. $\eta = \eta_0$). This is visualized in **Fig. 2.2(a)**. The total volume of a multi-cell system V_{MC}, where the power P_0 is split among a number N of converter cells, i.e. $P = P_0/N$, can be derived as

$$V_{\mathrm{MC}} = N \cdot V_0 \left(\frac{P_0}{N \cdot P_0}\right)^{3/2} = N^{-1/2} \cdot V_0. \tag{2.2}$$

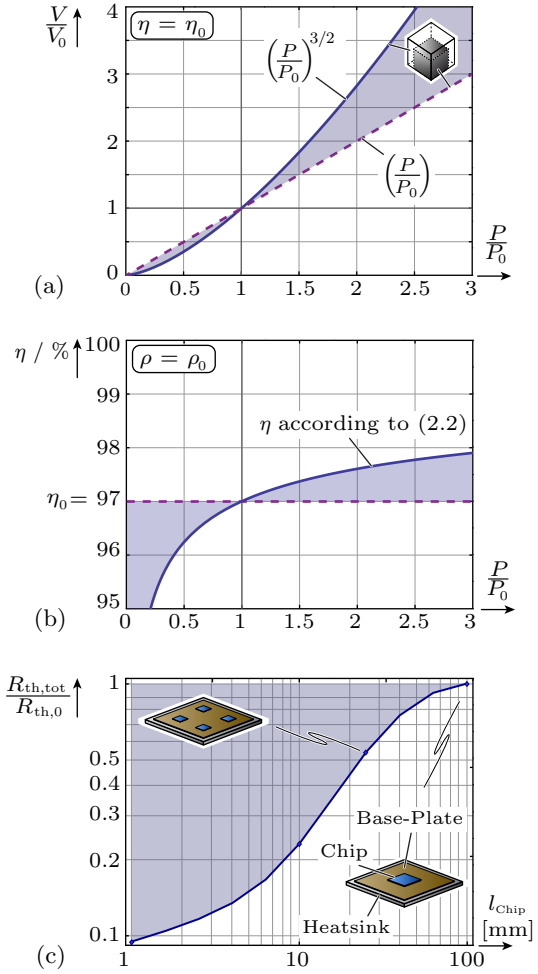

Fig. 2.2: General scaling laws of power electronic converters: (a) scaling of converter volume V with the converter power P at a constant conversion efficiency η and (b) required scaling of converter efficiency with the converter power at a constant power density ρ, both under the assumption of a constant heat dissipation per converter surface area; (c) reduction of the total thermal resistance of semiconductors by distributing the total chip area to multiple chips with shorter edge lengths l_{Chip}.

As a result, the total boxed volume of multi-cell converters scales advantageously compared to a single converter with the same total power rating as the multi-cell converter. By splitting the power into e.g. three subsystem, with a power of each cell of $P = P_0/3$, the total volume of the multi-cell system is reduced to $V_{\mathrm{MC}} \approx 0.58 \cdot V_0$. In other words, the power density ($\rho = P/V$) of multi-cell systems increases with the number of cells by

$$\rho = N^{1/2} \cdot \rho_0 \ . \tag{2.3}$$

With a similar approach (cf. **Appendix A**), assuming a constant power density (i.e. $\rho = P/V = \rho_0 = P_0/V_0$), it can be found that the necessary efficiency η of a converter system scales with the rated system output power P by

$$\eta = \frac{\eta_0 \cdot \left(\frac{P}{P_0}\right)^{1/3}}{1 + \eta_0 \cdot \left(\left(\frac{P}{P_0}\right)^{1/3} - 1\right)} \tag{2.4}$$

since only a fixed amount of losses (dissipated as heat) can be extracted per surface area. This relationship is depicted for $\eta_0 = 97\%$ in **Fig. 2.2(b)** and shows that, for example, doubling the system power ($P = 2 \cdot P_0$) while keeping the same power density requires to increase the efficiency to $\eta = 97.6\%$.

By splitting the system into lower rated subsystems due to parallel- or series-interleaving, the semiconductor ratings can be reduced, resulting in a smaller silicon area of the employed chips. Due to the better heat-spreading of smaller chips on a (comparably large) base-plate, the total thermal resistance $R_{\mathrm{th,tot}}$ of the lower-rated chips reduces compared to the thermal resistance $R_{\mathrm{th},0}$ of the full-rated power semiconductor, as shown in **Fig. 2.2(c)**. The values were determined with FEM simulations for a chip structure based on a TO-247 package with 350 µm thick silicon, 2 mm thick copper base-plate, 40 µm thick phase-change material ($\lambda = 0.3474\,\mathrm{W/(m \cdot K)}$) and a 5 mm thick heat-sink connected to a reference temperature of $T_{\mathrm{amb}} = 40\,^{\circ}\mathrm{C}$. The copper area of the base plate was chosen to be ten times larger than the silicon area. As the thermal resistance decreases with decreasing chip edge length, the overall heat-sink volume can be decreased by applying the multi-cell approach.

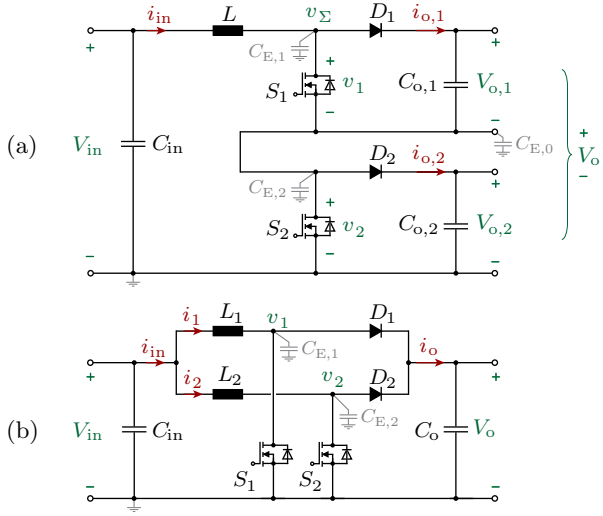

Fig. 2.3: Multi-cell converter realizations of a DC/DC boost converter: (a) series interleaving of two boost stages and (b) parallel interleaving of two boost stages.

As a result of the above mentioned fundamental scaling laws, which are independent of the employed converter topology, the multi-cell approach offers advantages in terms of converter efficiency and/or power density and potentially also costs since lower rated semiconductors and/or smaller heat-sinks can be employed.

2.2 Multi-Cell Boost Converters

In this section, the operation and the scaling benefits of series-interleaved and parallel-interleaved multi-cell converters are described using the example of DC/DC boost converters as shown in **Fig. 2.3**.

2.2.1 Series-Interleaved Boost Converters

In the series-interleaved boost converter (cf. **Fig. 2.3(a)**), with N_s series connected converter cells, the total output voltage V_o is shared among the output capacitors $C_{o,1}, C_{o,2} ... C_{o,Ns}$ of the individual converter cells, such that $V_{o,i} = V_o/N_s$. The system is advantageously

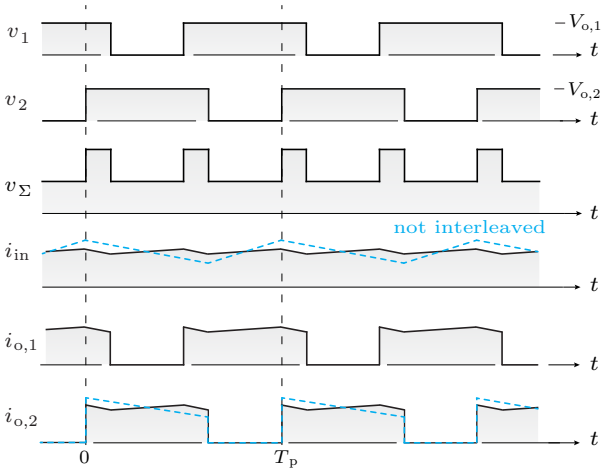

Fig. 2.4: Schematic waveforms of the operation of two series-interleaved DC/DC boost converters. Dashed lines denote the waveforms for operation without phase shift, i.e. non-interleaved operation.

operated with a phase-shifted (interleaved) modulation scheme with a phase shift of $\delta = 2\pi/N_s$ [26] as shown in **Fig. 2.4**. This results in an effective switching frequency of the total switch node voltage $v_\Sigma = \sum_{i=1}^{N} v_i$ of $f_{sw,eff} = N_s \cdot f_{sw}$ with f_{sw} being the switching frequency of one converter cell. Hence, the peak-to-peak current ripple Δi_{in} of the input current i_{in} can be calculated in dependency on the modulation index $M = V_{in}/V_o$ by introducing an effective modulation index $M_{eff} = (M \text{ modulo } 1/N_s)$ as

$$\Delta i_{in} = \frac{V_o}{L \cdot f_{sw}} \cdot M_{eff} \left(M_{eff} - \frac{1}{N_s} \right) . \tag{2.5}$$

The maximum value of Δi_{in} can be found for $M_{eff} = 0.5/N_s$ as

$$\Delta i_{in,max} = \frac{V_o}{4 N_s^2 f_{sw} L} \tag{2.6}$$

yielding a $\propto 1/N_s^2$ decrease of the ripple amplitude in dependency of the number of converter cells.

Furthermore, the harmonic spectrum of the multi-cell converter voltage v_Σ can be derived from a single converter system by considering only

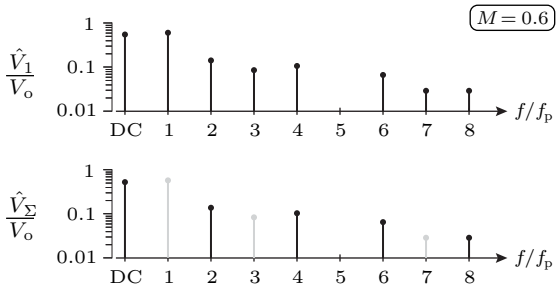

Fig. 2.5: Comparison of the harmonic spectrum of the switch node voltage V_1 of a single boost converter (top) with the harmonic spectrum of two series-interleaved boost converters (bottom) at a modulation index of $M = 0.6$. Harmonics shown in grey are canceled in the spectrum of the interleaved converters.

the harmonics with orders that are multiples of the number of cells N_s, as visualized in **Fig. 2.5**.

Semiconductors

The losses caused by semiconductors can be divided into conduction and switching losses and their dependency on the number of converter cells is described in the following.

Conduction Losses

For standard MOSFETs (i.e. not super-junction MOSFETs) the fundamental relation between the blocking voltage V_{DS} and the lowest achievable on-state resistance $R_{DS,on}$ of a device is determined by the so-called silicon limit [28], which can be expressed for a given semiconductor area A_{Si} as

$$R_{DS,on,(1)} \cdot A_{Si} = 8.3 \cdot 10^{-9} \cdot V_{DS}^{2.5}[\Omega\mathrm{cm}^2] = k_{Si} \cdot V_{DS}^{2.5}[\Omega\mathrm{cm}^2] \; . \quad (2.7)$$

This relation holds true for MOSFETs where the $R_{DS,on}$ is mainly influenced by the resistance of the drift region of the device, i.e. only for devices with blocking voltages larger than around 50 V [29]. In the multi-cell system with series-interleaved boost converters, the required blocking voltage of $V_{DS} = V_o$ is equally shared by N_s series connected

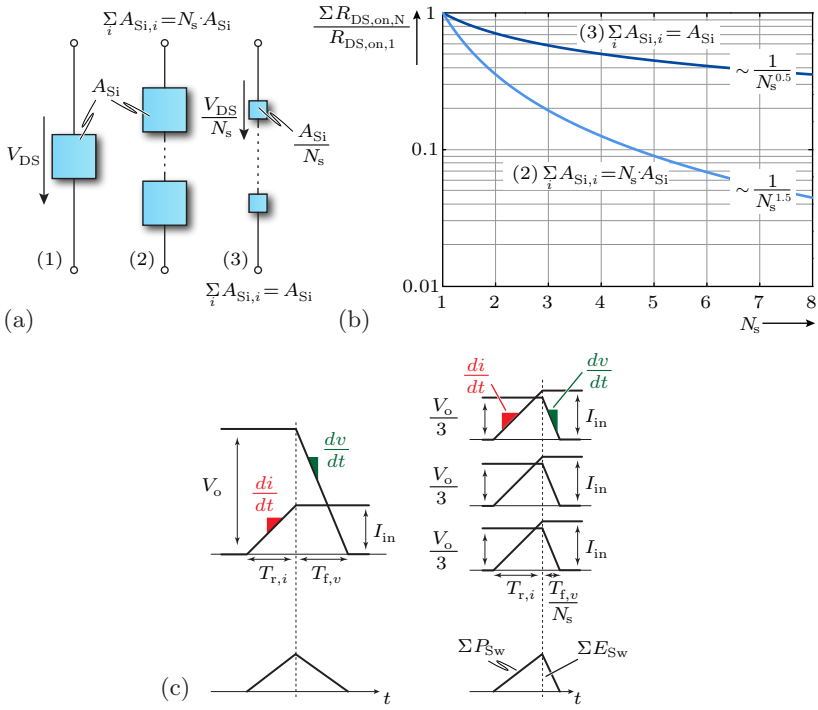

Fig. 2.6: Scaling laws of conduction and switching losses for series-interleaved boost converters: (a) replacing a single semiconductor with a blocking voltage of V_DS (1) with N_s semiconductors with blocking voltages of $V_\mathrm{DS}/N_\mathrm{s}$, where each has either the same silicon area A_Si as the full-rated semiconductor (2), or where the total chip area is equal to A_Si (3); (b) improvement of the total $R_\mathrm{DS,on}$ for scenarios (2) and (3) with the number of series connected semiconductors and/or converter cells; (c) reduction of switching losses in a series-interleaved multi-cell system with the same $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ as the single converter system [27].

switches, i.e. each switch has to be capable of blocking a voltage of $V_\mathrm{DS}/N_\mathrm{s}$, as shown in **Fig. 2.6(a)**. Now, it can either be assumed that the chip area of each semiconductor is equal to the chip area of the full-rated switch (i.e. N_s devices with A_Si, (2) in **Fig. 2.6(a)**) or that the total chip area A_Si is equally distributed among the semiconductors (i.e. N_s devices with $A_\mathrm{Si}/N_\mathrm{s}$, (3) in **Fig. 2.6(a)**). For option (2) the

total resistance can be calculated as

$$\begin{aligned} R_{\mathrm{DS,on,N,(2)}} &= N_\mathrm{s} \cdot \frac{1}{A_\mathrm{Si}} \cdot k_\mathrm{Si} \cdot \left(\frac{V_\mathrm{DS}}{N_\mathrm{s}}\right)^{2.5} [\Omega\mathrm{cm}^2] \\ &= \frac{1}{\sqrt{N_\mathrm{s}} \cdot N_\mathrm{s}} \cdot \frac{1}{A_\mathrm{Si}} \cdot k_\mathrm{Si} \cdot V_\mathrm{DS}^{2.5} [\Omega\mathrm{cm}^2] \end{aligned} \tag{2.8}$$

whereas the total resistance of option (3) equals

$$\begin{aligned} R_{\mathrm{DS,on,N,(3)}} &= N_\mathrm{s} \cdot \frac{N_\mathrm{s}}{A_\mathrm{Si}} \cdot k_\mathrm{Si} \cdot \left(\frac{V_\mathrm{DS}}{N_\mathrm{s}}\right)^{2.5} [\Omega\mathrm{cm}^2] \\ &= \frac{1}{\sqrt{N_\mathrm{s}}} \cdot \frac{1}{A_\mathrm{Si}} \cdot k_\mathrm{Si} \cdot V_\mathrm{DS}^{2.5} [\Omega\mathrm{cm}^2] \ . \end{aligned} \tag{2.9}$$

Both equations can be interpreted as a shift of the silicon limit towards lower specific on-state resistances [30], which can be expressed as

$$R_{\mathrm{DS,on,N,(2)}} = \frac{R_{\mathrm{DS,on,(1)}}}{\sqrt{N_\mathrm{s}} \cdot N_\mathrm{s}} \text{ and } R_{\mathrm{DS,on,N,(3)}} = \frac{R_{\mathrm{DS,on,(1)}}}{\sqrt{N_\mathrm{s}}} \ . \tag{2.10}$$

This relationship is visualized in **Fig. 2.6(b)**. The fundamental limits of wide bandgap materials such as GaN and SiC can be shifted in the same manner, since their on-state resistance for a given semiconductor area also increases more than quadratically with the break-down voltage (i.e. $R_{\mathrm{DS,on,GaN}} \propto V_\mathrm{DS}^{2.5}$ and $R_{\mathrm{DS,on,6H\text{-}SiC}} \propto V_\mathrm{DS}^{2.6}$) [31].

Switching Losses (Option 1)

The first option of calculating switching losses considers the overlapping of the current through the transistor and the voltage across the transistor during the switching transition (mainly applicable to circuits with IGBTs). The switching losses of N_s series connected switches can be compared to a single switch with full blocking voltage by assuming equal rates of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ for all switches [27]. The switching losses of the single full-rated switch are

$$P_{\mathrm{Sw,loss,1}} = E_\mathrm{sw} \cdot f_{\mathrm{sw,1}} = \frac{(T_{\mathrm{r},i} + T_{\mathrm{f},v})}{2} \cdot I_\mathrm{in} \cdot V_\mathrm{DC} \cdot f_{\mathrm{sw,1}} \ . \tag{2.11}$$

As can be seen from (2.6), the switching frequency of a system with N_s cells can be scaled by $1/N_\mathrm{s}^2$ while keeping the same current ripple amplitude for a certain inductance. Since the voltage across one switch

is equal to $V_\mathrm{o}/N_\mathrm{s}$ and the same $\mathrm{d}v/\mathrm{d}t$ is assumed, time $T_{\mathrm{f},v}$ decreases by a factor of $1/N_\mathrm{s}$. Thus, the overall switching losses of N_s series connected switches become

$$\begin{aligned} P_{\mathrm{Sw,loss,Ns}} &= N_\mathrm{s} \cdot E_{\mathrm{sw,cell}} \cdot \frac{f_{\mathrm{sw},1}}{N_\mathrm{s}^2} \\ &= N_\mathrm{s} \cdot \frac{1}{2} \cdot \left(T_{\mathrm{r},i} + \frac{T_{\mathrm{f},v}}{N_\mathrm{s}} \right) \cdot I_\mathrm{in} \cdot \frac{V_\mathrm{o}}{N_\mathrm{s}} \cdot \frac{f_{\mathrm{sw},1}}{N_\mathrm{s}^2} \\ &= \frac{1}{2N_\mathrm{s}^2} \cdot \left(T_{\mathrm{r},i} + \frac{T_{\mathrm{f},v}}{N_\mathrm{s}} \right) \cdot I_\mathrm{in} \cdot V_\mathrm{o} \cdot f_{\mathrm{sw},1} \ . \end{aligned} \tag{2.12}$$

Neglecting $T_{\mathrm{f},v}/N$ (compared to $T_{\mathrm{r},i}$) in a first step or assuming low values of $T_{\mathrm{r},i}$ (i.e. low values of the input current I_in), an improvement of the switching losses of

$$P_{\mathrm{Sw,loss,Ns}} \approx \frac{P_{\mathrm{Sw,loss},1}}{N_\mathrm{s}^2} ... \frac{P_{\mathrm{Sw,loss},1}}{N_\mathrm{s}^3} \tag{2.13}$$

can be found.

Switching Losses (Option 2)

The second option of calculating switching losses considers the energy stored in the parasitic capacitances of the transistor and the diode of a half-bridge. The energy stored in a parasitic non-linear capacitance ($C_{\mathrm{T,oss}}$ or $C_{\mathrm{D,oss}}$) can be calculated by introducing an energy-equivalent capacitance

$$C_{\mathrm{oss,E,eq}}(V_\mathrm{DS}) = \frac{2 \cdot E_\mathrm{oss}(V_\mathrm{DS})}{V_\mathrm{DS}^2} = \frac{2 \int_0^{V_\mathrm{DS}} v \cdot C_\mathrm{oss}(v)\mathrm{d}v}{V_\mathrm{DS}^2} \ ; \tag{2.14}$$

furthermore, a charge-equivalent capacitance

$$C_{\mathrm{oss,Q,eq}}(V_\mathrm{DS}) = \frac{Q_\mathrm{oss}(V_\mathrm{DS})}{V_\mathrm{DS}} = \frac{\int_0^{V_\mathrm{DS}} C_\mathrm{oss}(v)\mathrm{d}v}{V_\mathrm{DS}} \tag{2.15}$$

can be defined for the switch and the diode. This allows to calculate the energy $E_{\mathrm{on},1}$ lost per switching cycle in a system with only one converter cell (i.e. $N_\mathrm{s} = 1$) to be

$$\begin{aligned} E_{\mathrm{on},1} = & \frac{1}{2} \cdot C_{\mathrm{T,oss,E,eq},1}(V_\mathrm{o}) \cdot V_\mathrm{o}^2 \\ & - \frac{1}{2} \cdot C_{\mathrm{D,oss,E,eq},1}(V_\mathrm{o}) \cdot V_\mathrm{o}^2 \\ & + C_{\mathrm{D,oss,Q,eq},1}(V_\mathrm{o}) \cdot V_\mathrm{o}^2 \end{aligned} \tag{2.16}$$

(cf. [32]) since the turn-off transition of the MOSFET can be regarded as loss-less (ZVS) and thus $E_{\mathrm{off},1} = 0$. The above equation can be simplified, since the contribution of $C_{\mathrm{D,oss,E,eq},1}$ is typically small compared to the other terms and thus negligible, such that

$$E_{\mathrm{on},1} = \frac{1}{2} \cdot C_{\mathrm{eff},1}(V_\mathrm{o}) \cdot V_\mathrm{o}^2 \tag{2.17}$$

by introducing an effective capacitance

$$C_{\mathrm{eff},1}(V_\mathrm{o}) = C_{\mathrm{T,oss,E,eq},1}(V_\mathrm{o}) + 2 \cdot C_{\mathrm{D,oss,Q,eq},1}(V_\mathrm{o}) \ . \tag{2.18}$$

Hence, the switching losses for a single cell system are

$$P_{\mathrm{Sw,loss},1} = E_{\mathrm{on},1} \cdot f_{\mathrm{sw},1} = \frac{1}{2} \cdot C_{\mathrm{eff},1}(V_\mathrm{o}) \cdot V_\mathrm{o}^2 \cdot f_{\mathrm{sw},1} \ . \tag{2.19}$$

In a system with N_s converter cells, the voltage across each switch is only $V_\mathrm{o}/N_\mathrm{s}$ and the switching frequency of each cell is $f_{\mathrm{sw},1}/N_\mathrm{s}^2$ for the same current ripple (cf. (2.6)). Thus, in the same manner as before, the power dissipated in the switches of a multi-cell system can be calculated as

$$\begin{aligned} P_{\mathrm{Sw,loss,Ns}} &= N_\mathrm{s} \cdot E_{\mathrm{on,N}} \cdot \frac{f_{\mathrm{sw},1}}{N_\mathrm{s}^2} \\ &= \frac{1}{N_\mathrm{s}} \cdot \frac{1}{2} \cdot C_{\mathrm{eff,Ns}}(V_\mathrm{o}/N_\mathrm{s}) \left(\frac{V_\mathrm{o}}{N_\mathrm{s}}\right)^2 f_{\mathrm{sw},1} \\ &= \frac{1}{2N_\mathrm{s}^3} \cdot C_{\mathrm{eff,Ns}}(V_\mathrm{o}/N_\mathrm{s}) \cdot V_\mathrm{o}^2 \cdot f_{\mathrm{sw},1} \end{aligned} \tag{2.20}$$

and/or

$$P_{\mathrm{Sw,loss,Ns}} = \frac{1}{N_\mathrm{s}^3} \cdot \frac{C_{\mathrm{eff,Ns}}(V_\mathrm{o}/N_\mathrm{s})}{C_{\mathrm{eff},1}(V_\mathrm{o})} \cdot P_{\mathrm{Sw,loss},1} \ . \tag{2.21}$$

Depending on how the values of the effective capacitances of the employed low voltage switches (i.e. at $V_\mathrm{DS} = V_\mathrm{o}/N_\mathrm{s}$) compare to those of the higher voltage switch (i.e. at $V_\mathrm{DS} = V_\mathrm{o}$), a significant improvement of the switching losses can be achieved in the multi-cell system.

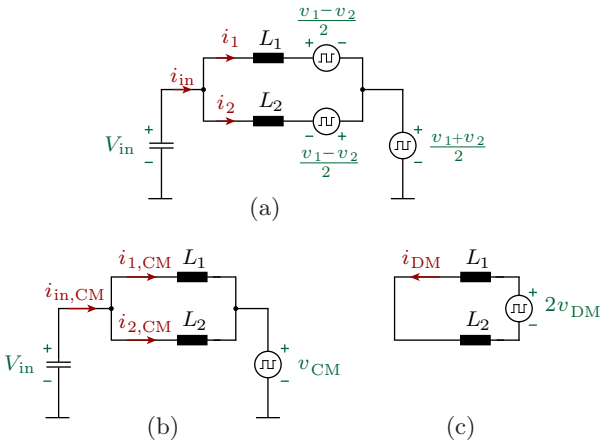

Fig. 2.7: Equivalent circuit diagram of two parallel-interleaved boost converters: (a) replacement of switch node voltages with rectangular voltage sources and splitting into (b) common-mode and (d) differential-mode equivalent circuits.

2.2.2 Parallel-Interleaved Boost Converters

In the parallel-interleaved boost converter (cf. **Fig. 2.3(b)**) with N_p parallel connected boost converters, the DC value of the input current I_in of the system is equally shared among the converter cells, i.e. average input current values of $I_1 = I_2 = ... = I_{\text{N}\text{p}} = I_\text{in}/N_\text{p}$ occur. The operation of the individual converter cells is phase-shifted with the same phase shift of $\delta = 2\pi/N_\text{p}$ as for the series interleaved system. This mode of operation allows to derive the equivalent circuit of **Fig. 2.7(a)** for a system with two parallel-interleaved boost converters. In this circuit the switches are replaced by rectangular voltage sources in order to accurately model the influence of the switch node voltages v_1 and v_2 on the input currents i_in, i_1 and i_2. The rectangular voltage sources can be divided into a common-mode voltage component (cf. **Fig. 2.7(b)**)

$$v_\text{CM} = \frac{v_1 + v_2}{2} \tag{2.22}$$

and a differential-mode voltage component [33] (cf. **Fig. 2.7(c)**)

$$u_\text{DM} = \frac{v_1 - v_2}{2} \ . \tag{2.23}$$

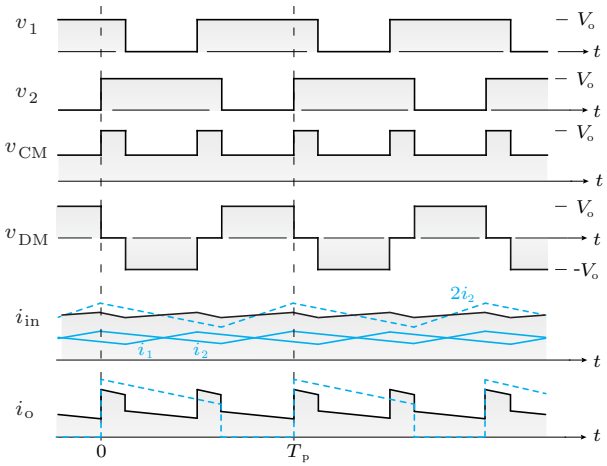

Fig. 2.8: Schematic waveforms of the operation of two parallel-interleaved phase-shifted boost converters. Dashed lines denote the waveforms for operation without phase shift.

Based on these equivalent circuits it can be concluded, that the input current of the system i_{in} is only influenced by the common-mode voltage component v_{CM} (hence $i_{in} = i_{in,CM}$), whereas the current i_{DM}, driven by the differential-mode voltage component v_{DM}, circulates only between the boost stages and does not contribute to the power transfer from the source to the load. The schematic waveform of those quantities (cf. **Fig. 2.8**) illustrates the similarity between the common-mode voltage v_{CM} of the parallel-interleaved boost converters and the voltage v_Σ of the series-interleaved boost converters of **Fig. 2.4**. Both exhibit an effective switching frequency of $f_{sw,eff} = N_p \cdot f_{sw}$ or $f_{sw,eff} = N_s \cdot f_{sw}$, respectively.

The harmonic spectrum of multiple parallel-interleaved boost converters can also be derived from the harmonic spectrum of a single boost converter. The spectrum of the common-mode voltage v_{CM} is basically identical to the spectrum of the single converter but contains only harmonics with orders that are multiples of the cell number N_p, as shown in **Fig. 2.9**. The spectrum of the differential-mode voltage v_{DM} contains the remaining harmonics, i.e. those harmonics of the original spectrum that are not present in the spectrum of v_{CM}. It is important

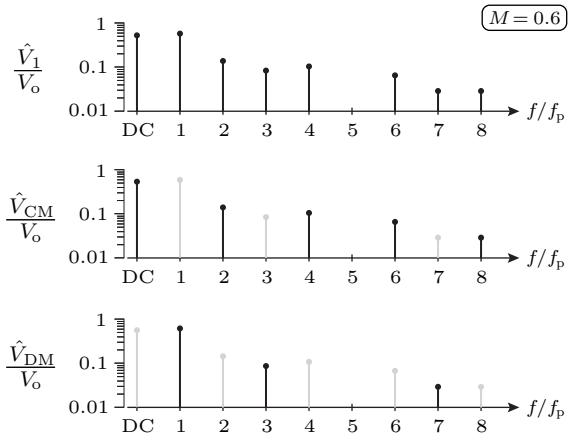

Fig. 2.9: Comparison of the harmonic spectrum of a single boost converter (top) to the common-mode voltage spectrum (middle) and the differential-mode voltage spectrum (bottom) of two parallel-interleaved boost converters.

to note, that the common-mode voltage exhibits the same spectrum as the voltage u_Σ of the series-interleaved boost converters for the same number of converter cells.

Stored Energy and Converter Volume

The peak-to-peak current ripple of the inductor current in any of the parallel interleaved boost stages can be calculated for a given modulation index $M = V_{in}/V_o$ as

$$\Delta i_i = \frac{V_o \cdot M \cdot (1 - M)}{f_{sw} \cdot L} \tag{2.24}$$

whereas the DC value of the inductor current equals

$$I_i = \frac{I_{in}}{N_p} \tag{2.25}$$

under the assumption of equal power sharing between the parallel boost stages. The total peak energy stored in the inductors of a system with N_p parallel-interleaved boost converters is

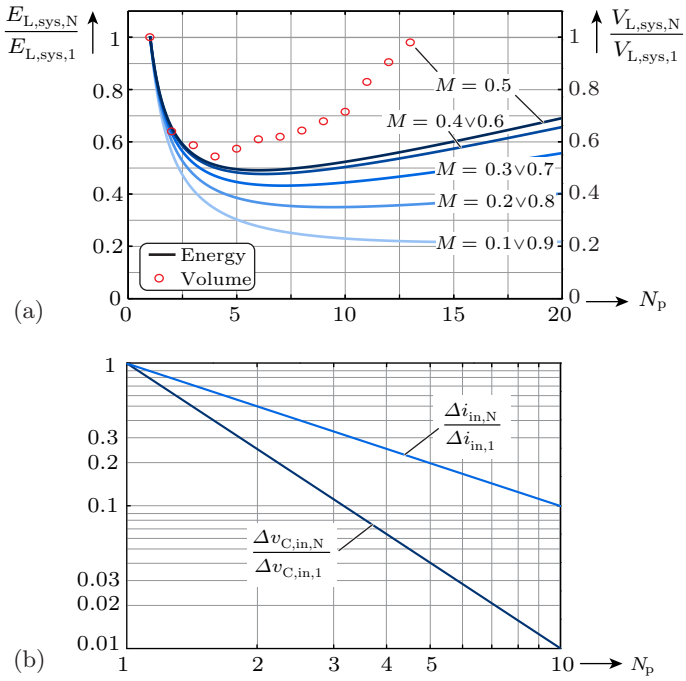

Fig. 2.10: Scaling laws of parallel-interleaved boost converters. (a) Dependency of the normalized total peak energy stored in the inductors ($E_{\mathrm{L,sys,N}}/E_{\mathrm{L,sys,1}}$) with the number of converter cells and the modulation index. The total normalized inductor volume ($V_{\mathrm{L,sys,N}}/V_{\mathrm{L,sys,1}}$) of parallel-interleaved boost converters is shown for $M = 0.5$ for efficiency-constrained designs with N87 core material and litz wires (cf. [34]). It should be noted, that the resulting characteristic under the chosen efficiency constraint is largely frequency independent. (b) Reduction of the normalized system input current ripple and normalized input voltage ripple with the number of converter cells.

$$E_{\mathrm{L,sys,N}} = N_\mathrm{p} \cdot \frac{1}{2} \cdot L \cdot \left(I_i + \frac{\Delta i_i}{2} \right)^2 . \tag{2.26}$$

The energy stored in a system with interleaved boost converters can now be compared to the energy in a single boost converter system as depicted in **Fig. 2.10(a)** for $V_\mathrm{o} = 400\,\mathrm{V}$, $L = 200\,\mu\mathrm{H}$, $f_\mathrm{sw} = 100\,\mathrm{kHz}$

and $I_{\mathrm{in}} = 15\,\mathrm{A}$. It has to be pointed out that for this and the following considerations the inductance L of each converter cell is equal to the inductance of a single boost converter (i.e. resulting in an increased relative ripple of the inductor currents since the average current in each inductor decreases but the peak-to-peak current ripple stays the same). The result shows that for each modulation index an optimum number of parallel-interleaved boost converters can be found where the total peak energy is minimized. The relation between stored energy in inductive components and their corresponding volume has been studied in [34] where it was shown that the inductor volume is largely proportional to the stored energy as long as low-frequency losses dominate compared to high-frequency losses. The total inductor volume of parallel-interleaved boost converters with efficiency-constrained inductor designs is also shown in **Fig. 2.10(a)** for a modulation index of $M = 0.5$. Thus, for a fixed switching frequency, minimizing the total energy also minimizes the overall inductor volume until high frequency losses predominate.

The peak-to-peak current ripple of the input current can be derived for a given number of parallel boost converters N_{p} and an effective modulation index $M_{\mathrm{eff}} = (M \text{ modulo } 1/N_{\mathrm{p}})$ as

$$\Delta i_{\mathrm{in}} = \frac{V_{\mathrm{o}} \cdot N_{\mathrm{p}}}{f_{\mathrm{sw}} \cdot L} \cdot M_{\mathrm{eff}} \left(\frac{1}{N_{\mathrm{p}}} - M_{\mathrm{eff}} \right) \tag{2.27}$$

with a maximum value at $M_{\mathrm{eff}} = 0.5/N_{\mathrm{p}}$ of

$$\Delta i_{\mathrm{in,max}} = \frac{V_{\mathrm{o}}}{4 f_{\mathrm{sw}} N_{\mathrm{p}} L} \ . \tag{2.28}$$

The ripple of the input current introduces a voltage ripple on the input capacitor C_{in}, which can be calculated with the relation of $v = \int i \mathrm{d}t / C$ as

$$\Delta v_{\mathrm{C,in,max}} = \frac{\Delta i_{\mathrm{in,max}}}{8 N_{\mathrm{p}} f_{\mathrm{sw}} C_{\mathrm{in}}} = \frac{V_{\mathrm{o}}}{32 N_{\mathrm{p}}^2 f_{\mathrm{sw}}^2 C_{\mathrm{in}} L} \tag{2.29}$$

(assuming a constant average current drawn from the voltage source, which is powering the converter system). These scaling laws are shown in **Fig. 2.10(b)** normalized to the values of a single boost converter system.

Please note, that another approach of the parallel interleaving is to scale the inductance L of each parallel cell by $L = N_{\mathrm{p}} L_0$. This does

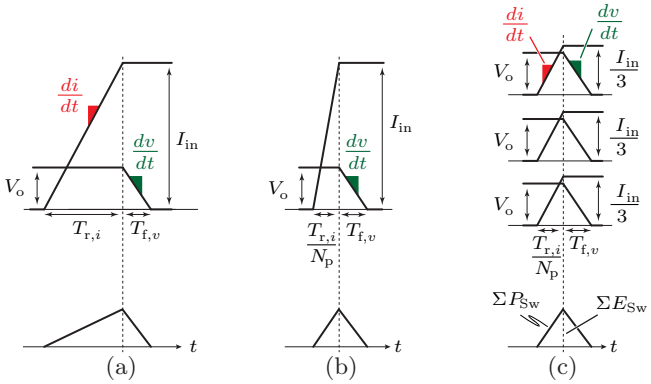

Fig. 2.11: Comparison of switching losses between a single boost converter (a) and parallel-interleaved boost convertes (c) for the same rates of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. The single boost converter can only reach the same level of switching losses as the parallel-interleaved converter, if the rate of $\mathrm{d}i/\mathrm{d}t$ is increased by a factor of N_p (b).

not lead to a reduction of the stored energy in the system like in (2.26), but reduces the total input current ripple by a factor of $1/N_\mathrm{p}^2$ instead of just $1/N_\mathrm{p}$ like in (2.28).

Switching Losses (Option 1)

The switching losses can be calculated by considering the overlap of voltages and currents of the switches of the multi-cell converter, as shown in **Fig. 2.11**. Based on the result of (2.28) the switching frequency of each stage can be reduced by a factor of $1/N_\mathrm{p}$ compared to the switching frequency of a single boost converter to obtain the same peak-to-peak amplitude of the input current. By assuming the same rates of $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ as in the single converter system the switching losses can be found to be

$$\begin{aligned} P_{\mathrm{Sw,loss,Np}} &= N_\mathrm{p} \cdot E_{\mathrm{sw,cell}} \cdot \frac{f_{\mathrm{sw},1}}{N_\mathrm{p}} \\ &= N_\mathrm{p} \cdot \frac{1}{2} \cdot \left(\frac{T_{\mathrm{r},i}}{N_\mathrm{p}} + T_{\mathrm{f},v} \right) \cdot \frac{I_\mathrm{in}}{N_\mathrm{p}} \cdot V_\mathrm{o} \cdot \frac{f_{\mathrm{sw},1}}{N_\mathrm{p}} \\ &= \frac{1}{2N_\mathrm{p}} \cdot \left(\frac{T_{\mathrm{r},i}}{N_\mathrm{p}} + T_{\mathrm{f},v} \right) \cdot I_\mathrm{in} \cdot V_\mathrm{o} \cdot f_{\mathrm{sw},1} \,. \end{aligned} \tag{2.30}$$

An upper boundary of the switching loss reduction can be found for low output voltage values, i.e. negligible times $T_{\mathrm{f},v}$, thus the switching loss reduction lies in the range of

$$P_{\mathrm{Sw,loss,Np}} = \frac{P_{\mathrm{Sw,loss,1}}}{N_{\mathrm{p}}} \ldots \frac{P_{\mathrm{Sw,loss,1}}}{N_{\mathrm{p}}^2} \ . \tag{2.31}$$

Switching Losses (Option 2)

The calculation of the switching losses based on the energy stored in the parasitic transistor and diode capacitances yields for the system with parallel-interleaved boost converters

$$\begin{aligned} P_{\mathrm{Sw,loss,Np}} &= N_{\mathrm{p}} \cdot E_{\mathrm{on,Np}} \cdot \frac{f_{\mathrm{sw,1}}}{N_{\mathrm{p}}} \\ &= \frac{1}{2} \cdot C_{\mathrm{eff,Np}}(V_{\mathrm{o}}) \cdot V_{\mathrm{o}}^2 \cdot f_{\mathrm{sw,1}} \end{aligned} \tag{2.32}$$

and/or

$$P_{\mathrm{Sw,loss,Np}} = \frac{C_{\mathrm{eff,Np}}(V_{\mathrm{o}})}{C_{\mathrm{eff,1}}(V_{\mathrm{o}})} \cdot P_{\mathrm{Sw,loss,1}} \ . \tag{2.33}$$

Since the switches and diodes in the parallel-interleaved boost converters have to be rated for the same voltage but for a lower current than the switch in the single boost converter, the employed silicon area can be smaller and thus also the parasitic capacitances will be smaller and the capacitive switching losses will decrease.

2.3 Challenges of Multi-Cell Systems

The scaling laws, that were derived in the section above, clearly demonstrate the theoretical benefits of a multi-cell converter in comparison to a single converter counterpart. In a practical setup, however, there are limiting factors that constrain the number of employed cells within a multi-cell system, and the system performance would decrease if the number of cells was increased beyond an optimal number of converter cells. These limiting factors and challenges of multi-cell systems are described in the following.

2.3.1 Constant Offset Penalties

By increasing the number of cells in order to benefit from the scaling laws, each additional cell comes with a penalty to the overall systems performance. The main contributors are:

- *Control & Communication*: Each converter cell requires a control unit which typically consists of a DSP and/or an FPGA, analog electronics to measure control variables such as currents and voltages, and other auxiliary ICs. Furthermore, the communication to other cells has to be established, which necessitates isolation ICs to transmit signals beyond isolation barriers and/or optical data links. All of these components have a power consumption which is almost independent of the power level of the converter. This decreases the system efficiency, especially at low load operation. In addition, the required volume for the control and communication deteriorates the power density of the converter.
- *MOSFET package & PCB resistance*: For the case of series connected MOSFETs, the total $R_{\mathrm{DS,on,N}}$ of the series connected cells is not only dependent on the resistance of the chip itself, but also on the package resistance and the interconnecting PCB traces, summarized into R_{pack}. Thus, (2.9) can be extended to

$$R_{\mathrm{DS,on,N,(3)}} = \frac{1}{\sqrt{N_{\mathrm{s}}}} \cdot \frac{1}{A_{\mathrm{Si}}} \cdot k_{\mathrm{Si}} \cdot V_{\mathrm{DS}}^{2.5} [\Omega \mathrm{cm}^2] + N_{\mathrm{s}} \cdot R_{\mathrm{pack}} \ . \quad (2.34)$$

  Consequently, an optimum number $N_{\mathrm{s,opt}}$ of series connected devices with the lowest resulting total $R_{\mathrm{DS,on,N}}$ can be found as

$$N_{\mathrm{s,opt}} = 2\sqrt{2} \left(\frac{A_{\mathrm{Si}} R_{\mathrm{pack}}}{k_{\mathrm{Si}} V_{\mathrm{DS}}^{2.5}} \right) \ . \quad (2.35)$$

  Increasing the number of cells beyond this optimal number does no longer result in a lower value of the total on-resistance.

2.3.2 Common-Mode Currents

The parasitic ground capacitances at the switch-nodes of the converters are a source for unwanted common-mode currents which necessitate the application of common-mode filters, e.g. in PFC boost rectifiers, that substantially increase the volume of the converter. The voltage

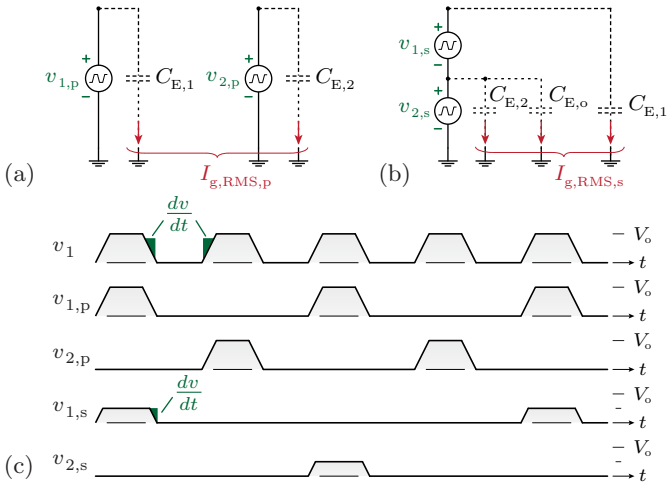

Fig. 2.12: Equivalent circuit models for ground currents of (a) the parallel-interleaved boost converter and (b) the series-interleaved boost converter. The waveforms of the switch-node voltages of the parallel-interleaved system ($v_{1,p}$, $u_{2,p}$) and series-interleaved system ($v_{1,s}$, $v_{2,s}$) are compared to those of a single boost converter (v_1) in (c) under the assumption of same dv/dt in all systems.

of the switch-node can be modeled with a trapezoidal wave voltage source that exhibits a certain $\mathrm{d}v/\mathrm{d}t$, as shown in **Fig. 2.12(a)** for the parallel-interleaved boost converter and in **Fig. 2.12(b)** for the series-interleaved boost converter with parasitic capacitances as defined in **Fig. 2.3**. A comparison of the voltage waveforms between the single boost converter (v_1), the parallel-interleaved ($v_{1,p}$, $v_{2,p}$) and the series-interleaved boost converter ($v_{1,s}$, $v_{2,s}$) is depicted in **Fig. 2.12(c)**. Based on the fundamental relationship of $I_C = C \cdot \mathrm{d}v/\mathrm{d}t$, the RMS value of the ground current of a single boost converter system through capacitance C_E can be calculated as

$$I_{g,RMS,1} = \sqrt{2k} \cdot C_E \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \text{ with } k = \frac{V_o \cdot f_{sw}}{\frac{\mathrm{d}v}{\mathrm{d}t}} \,. \tag{2.36}$$

The switching frequency of the parallel-interleaved boost converters can be reduced by a factor of 1/2 (for $N_p = 2$) for an equal total input current ripple amplitude (cf. (2.28)) leading to

$$k_\mathrm{p} = \frac{V_\mathrm{o} \cdot f_\mathrm{sw}}{\frac{\mathrm{d}v}{\mathrm{d}t} \cdot 2} = \frac{k}{2} \ . \tag{2.37}$$

Under the assumption of $C_{\mathrm{E},1} = C_{\mathrm{E},2} = C_\mathrm{E}$ the RMS value of the ground current can be found as

$$I_{\mathrm{g,RMS,p}} = \sqrt{2} \cdot \sqrt{2k_\mathrm{p}} \cdot C_\mathrm{E} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} = \sqrt{2k} \cdot C_\mathrm{E} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \ . \tag{2.38}$$

For the series-interleaved system, the switching frequency can be reduced by 1/4 (for $N_\mathrm{s} = 2$) for an equal input current ripple amplitude (cf. (2.6)) and in combination with a voltage amplitude of only $V_\mathrm{o}/2$ for each equivalent source results

$$k_\mathrm{s} = \frac{\frac{V}{2} \cdot f_\mathrm{sw}}{\frac{\mathrm{d}v}{\mathrm{d}t} \cdot 4} = \frac{k}{8} \ . \tag{2.39}$$

By superposition and again assuming $C_{\mathrm{E},1} = C_{\mathrm{E},2} = C_\mathrm{E}$ the equation for the ground current yields

$$\begin{aligned} I_{\mathrm{g,RMS,s}} &= \sqrt{2k_\mathrm{s} \cdot \left((C_{\mathrm{E,o}} + 2C_\mathrm{E}) \frac{\mathrm{d}u}{\mathrm{d}t} \right)^2 + 2k_\mathrm{s} \cdot \left(C_\mathrm{E} \frac{\mathrm{d}u}{\mathrm{d}t} \right)^2} \\ &= \frac{1}{2} \cdot \sqrt{k} \cdot \sqrt{(C_{\mathrm{E,o}} + 2 \cdot C_\mathrm{E})^2 + C_\mathrm{E}^2} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \end{aligned} \tag{2.40}$$

with $C_{\mathrm{E,o}}$ denoting the capacitance of the entire "upper" converter cell to ground. By relating the ground currents of multi-cell systems to the single boost converter it can be found that

$$\frac{I_{\mathrm{g,RMS,p}}}{I_{\mathrm{g,RMS,1}}} = 1 \tag{2.41}$$

$$\frac{I_{\mathrm{g,RMS,s}}}{I_{\mathrm{g,RMS,1}}} = \frac{1}{2\sqrt{2}} \sqrt{\left(2 + \frac{C_{\mathrm{E,o}}}{C_\mathrm{E}} \right)^2 + 1} \ . \tag{2.42}$$

This means that the RMS ground current of the series-interleaved system can only reach the same value as the parallel-interleaved system (and thus as the single boost converter) if $C_{\mathrm{E,o}} = (\sqrt{7}-2) \cdot C_\mathrm{E} \approx 0.64 \cdot C_\mathrm{E}$ (considering the series interleaving of the two cells). This is rather unlikely, since capacitance $C_{\mathrm{E,o}}$ is the capacitance of the entire "upper" converter cell to ground, which is amongst others defined by the physical size of the entire converter cell. Thus, the series-interleaved boost converter system will potentially exhibit larger RMS ground currents than the single and the parallel interleaved systems.

2.3.3 Reliability

A common argument, which is often raised in the context of multi-cell converters, addresses the reliability of the entire system. As the system is constructed of several converter cells, the total number of employed components is increased compared to an equivalent single-stage converter system. This increases the probability of a failure of a component. However, in contrast to the single converter system, the failure of a single component is not necessarily leading to a failure of the entire multi-cell system since only one cell is affected. Depending on the operation of the multi-cell system, it might still be functional at a reduced power and/or voltage level. This might require that the failed cell goes into a predefined state in case of failure, i.e. open or short circuit state. It furthermore has to notify the master cell about the occurrence of the failure such that the control loops in the master cell can be adapted to the new number of active cells.

The simplest and most effective way to increase the reliability of the multi-cell system is achieved by introducing redundancy by means of additional standby cells [27]. For an assumed failure in time (1FIT = $1/10^9 h$) rate λ_{cell} of a single converter cell, the mean time to failure ($MTTF_{\text{sys}}$) for the entire system with N_{cells} can be derived as

$$MTTF_{\text{sys}} = \frac{1}{N_{\text{cells}} \lambda_{\text{cell}}} \ . \tag{2.43}$$

The addition of k_{red} redundant cells allows to achieve a redundancy, where the system is operational as long as at least N_{cells} cells are functional out of $N_{\text{cells}} + k_{\text{red}}$ total cells [35]. For the case, that the redundant cells are just in standby, the total system mean time to failure has increased to

$$MTTF_{\text{sys}} = \frac{k_{\text{red}} + 1}{N_{\text{cells}} \lambda_{\text{cells}}} \ . \tag{2.44}$$

The additional cost to achieve redundancy is only a fraction of the entire system cost whereas a single converter system doubles in cost if it is made redundant.

2.3.4 Transformers and Electrolytic Capacitors

In any application that requires a certain energy storage, either because it has to fulfill a given hold-up time requirement or because it has to

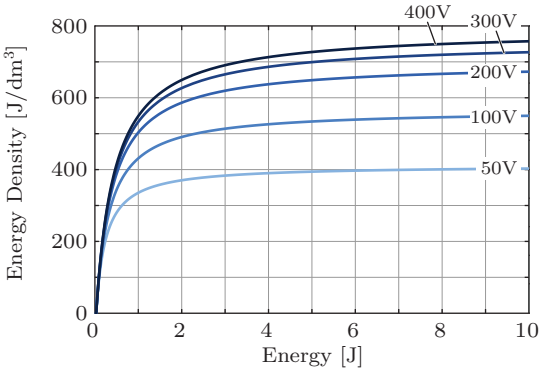

Fig. 2.13: Fitted energy density function for electrolytic capacitors of three different manufacturers (Panasonic, Rubycon, EPCOS) in dependency of the voltage and the stored energy. Due to the splitting of the DC-link into multiple low voltage DC-links in series-connected multi-cell converters, the total energy is stored at lower voltages which results in a larger total capacitor volume.

buffer a pulsating power flow such as in single-phase grid applications, typically electrolytic capacitors are employed. This is mainly due to the fact, that this technology provides the highest energy density among the available capacitors technologies. The required energy storage is independent of the system topology and applies to both single-cell converter systems and multi-cell systems. The only difference is, however, that in series connected multi-cell systems, the energy is stored at lower voltage levels, since the total DC-link voltage is split into multiple low voltage DC-links. This results in a larger volume as the energy density decreases for electrolytic capacitors with lower voltage. This is shown by a fitted energy density function for more than 500 electrolytic capacitors of three different manufactures (Panasonic, Rubycon, EPCOS) in **Fig. 2.13**. The fitting function for the volume (in m^3) of the capacitors in dependency of the voltage rating V_{rat} (in V) and the capacitance value C_{val} (in F) is given as

$$\mathrm{Vol}_{\mathrm{C,elco}} = k_1 + k_2 \cdot C_{\mathrm{val}} \cdot V_{\mathrm{rat}} + k_3 \cdot C_{\mathrm{val}} \cdot V_{\mathrm{rat}}^2 \tag{2.45}$$

where $k_1 = 5.41 \cdot 10^{-7}\,\mathrm{m}^3$, $k_2 = 3.33 \cdot 10^{-5}\,\mathrm{m}^3/(\mathrm{F} \cdot \mathrm{V})$, and $k_3 = 5.5 \cdot 10^{-7}\,\mathrm{m}^3/(\mathrm{F} \cdot \mathrm{V}^2)$.

In multi-cell systems, where the terminals on one side of the cells are connected in series and the terminals on the other side are connected in parallel (e.g. ISOP or IPOS topologies), the employment of transformers is mandatory. The required area product (multiplication of winding area A_W and core area A_C) of a transformer can be derived as [36]

$$A_\mathrm{W} A_\mathrm{C} = \frac{\sqrt{2}}{\pi k_\mathrm{W} J_\mathrm{rms} \hat{B}} \frac{S}{f} \ . \tag{2.46}$$

The area product is proportional to the fourth power of the characteristic edge length of the transformer, as is accordingly also the (apparent) power of the transformer

$$A_\mathrm{W} A_\mathrm{C} \sim L^4 \sim S \ . \tag{2.47}$$

By taking into account, that the volume of a transformer is only proportional to the cubic function of the linear dimension

$$\mathrm{Vol_T} \sim L^3 \sim S^{\frac{3}{4}} \tag{2.48}$$

the volume of a transformer scales in relation to a reference design ($\mathrm{Vol_T^*}$, S^*) with

$$\mathrm{Vol_T} = \mathrm{Vol_T^*} \left(\frac{S}{S^*} \right)^{\frac{3}{4}} \ . \tag{2.49}$$

In multi-cell converters, the power rating of the employed transformers can be reduced with the number of cells N_cells by the factor $S = S^*/N_\mathrm{cells}$, as either the voltage rating is reduced in the series interleaved connection or the current rating is reduced in the parallel interleaved connection. Consequently, the total transformer volume in multi-cell converters scales with the number of cells compared to a single converter system by

$$\mathrm{Vol_{T,MC}} = N_\mathrm{cells} \mathrm{Vol_T^*} \left(\frac{1}{N_\mathrm{cells}} \right)^{\frac{3}{4}} = N_\mathrm{cells}^{\frac{1}{4}} \mathrm{Vol_T^*} \ . \tag{2.50}$$

This means, that the total transformer volume in multi-cell systems increases (slightly) with an increasing number of cells.

Please note that these are only fundamental considerations of transformer scaling laws that do not take into account practical considerations, e.g. the required isolation distance between the primary and

secondary winding or the applied switching frequencies of the multi-cell and single-cell systems or thermal limitations.

2.3.5 Balancing and Control of Multi-Cell Converters

The balancing of currents and/or voltages is an important issue in multi-cell converter systems as the design of the converter cells relies on an equal current and/or voltage sharing among the cells, such that the overall system power is equally distributed. Thus, any conditions that lead to a violation of the power sharing might cause an overloading and ultimately a destruction of individual converter cells, possibly resulting in a system failure. Therefore, current and/or voltage sharing among the converter cells has to be guaranteed for steady state condition and transients. Also, the influence of component mismatches, such as slightly different inductance values of parallel connected converter cells, on the balancing of the system needs to be addressed.

The operation of multi-cell systems with common-duty-ratio control, where all converter cells are operated with the same duty cycle, relies on the natural balancing capabilities of a multi-cell topology and is thus only feasible for IPOS and ISOP systems [25, 37, 38]. For those topologies any component mismatch leads to slightly unequal sharing conditions, but not to a runaway situation.

In general, ISOS and IPOP are considered to have no natural balancing mechanism and thus require additional control means to guarantee a balanced operation (even though for the ISOS converter some weak balancing mechanisms could also be found [39]). For the IPOP converter it is sufficient to control the output current to be equally shared, as the input current will then also be equally shared [40]. Different control schemes such as droop methods and active control concepts have been published and reviewed in literature [41–44]. For ISOS converter structures it was found that controlling the output voltage sharing does not ensure input voltage sharing due to the presence of a right-half-plane pole and thus control efforts should focus on input voltage sharing [45].

2.3.6 Impedance of the Commutation Loops

In each converter cell of the multi-cell converter the switches and the attached DC-link capacitor create a commutation loop, which is shown for

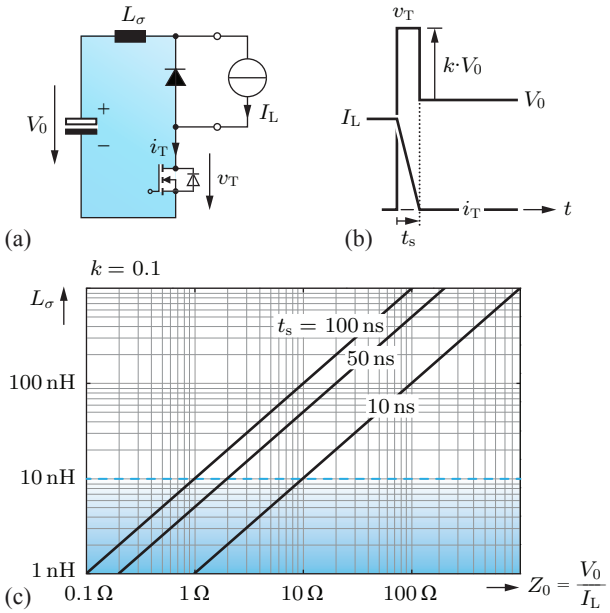

Fig. 2.14: Influence of the parasitic commutation loop inductance on the overvoltage during switching transients: (a) commutation loop formed by a DC-link capacitor, a transistor, and a freewheeling diode; parasitic loop inductance L_σ; (b) the turn-off transition of the transistor causes a voltage overshoot of kV_0 of the transistor voltage v_T during the time t_s of the switching transient; (c) maximum allowed loop inductance L_σ for different impedance values $Z_0 = V_0/I_L$ of the converter cell and different values of the transition time t_s such that the voltage overshoot is limited to 10% of the DC-link voltage V_0 (i.e. $k = 0.1$).

the simplified case of a unidirectional half-bridge with the load modeled as constant current source I_L in **Fig. 2.14(a)**. The commutation loop contains an inductance L_σ which represents all parasitic inductances of the commutation loop, i.e. inductances due to the semiconductor packages, the PCB or the capacitor leads. At the turn-off of the MOSFET the parasitic inductance L_σ causes an overvoltage Δv_0, depending on the duration of the switching transition t_s and the load current level I_L,

$$\Delta v_0 = L_\sigma \cdot \frac{I_L}{t_s} \leq k \cdot V_0 \ . \tag{2.51}$$

The overvoltage is related to the capacitor voltage V_0 such that a constraint for a maximum permissible overvoltage $k \cdot V_0$ is given, as visualized in **Fig. 2.14(b)**. By introducing the impedance $Z_0 = V_0/I_\mathrm{L}$ this inequality can be rearranged to [30]

$$Z_0 = \frac{V_0}{I_\mathrm{L}} \geq \frac{L_\sigma}{k \cdot t_\mathrm{s}} \ . \tag{2.52}$$

Thus, for a given impedance of the converter cell, the parasitic loop inductance has to be lower than a specific value, which is visualizied for a relative overvoltage of 10% (i.e. $k = 0.1$) and different switching transition durations t_s in **Fig. 2.14(c)**. By paralleling converter cells, the current I_L is split up among the converter cells, thus their impedance is increased by

$$Z_{0,\mathrm{par}} = \frac{V_0 \cdot N}{I_\mathrm{L}} = N \cdot Z_0 \tag{2.53}$$

while connecting converter cells in series distributes the voltage among the converter cells and thus decreases the impedance by

$$Z_{0,\mathrm{ser}} = \frac{V_0}{I_\mathrm{L} \cdot N} = \frac{Z_0}{N} \ . \tag{2.54}$$

As a result, it is especially important for series connected converter cells to keep the parasitic loop inductance limited to small values, for example by using lead-less semiconductor packages, in order to avoid transient over-voltages at the switches.

2.4 Summary and Conclusion

Based on the investigation of the scaling laws it can be summarized that both the series-interleaved as well as the parallel-interleaved approach offer considerable advantages in terms of reduced

- *conduction losses*: The use of low-voltage semiconductors in series-connected converter cells effectively shifts the silicon limit towards lower specific on-state resistances which is due to the scaling of the specific on-state resistance with the blocking voltage by $R_\mathrm{DS,on} \propto V_\mathrm{DS}^{2.5}$. This leads to the effect that N_cells in series connected semiconductors with a blocking voltage of $V_\mathrm{DC}/N_\mathrm{cells}$ have a lower total $R_\mathrm{DS,on}$ than a single semiconductor with a blocking

voltage of V_{DC}. For the case of equal total chip areas, a reduction of the total $R_{\mathrm{DS,on}}$ by a factor of $1/\sqrt{N_{\mathrm{cells}}}$ can be achieved;

- *current and voltage ripple*: By interleaving the operation of the converter cells, the effective switching frequency of the system is a multiple of the switching frequency of a single converter cell [46]. In combination with the reduced voltage levels of the cells (in series interleaving) or increased boost inductance (in parallel interleaving for equal total stored energy), the current ripple reduces by $1/N_{\mathrm{cells}}^2$;
- *switching losses*: By splitting the system into low power cells with low voltage and/or low current, the total switching losses reduce with $1/N_{\mathrm{cells}}^2$ for the case of equal current ripples (under the assumption of equal $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ rates of the multi-cell system and the single-cell system and that the switching losses are defined by the overlapping of voltage and current during the switching transition). For the case of equal switching losses, the effective switching frequency in the multi-cell system can be a factor of N_{cells} higher than in the single-cell system;
- *heatsink volumes*: The reduction of the total switching and conduction losses combined with the distribution of the losses among several semiconductors leads to smaller heatsinks or even completely eliminates the need for heatsinks;
- *magnetic component volumes*: The parallel interleaving of converter cells leads to a reduction of the total energy stored in the inductors which correlates with a reduction of the total inductor volume for the same current ripple.

The above mentioned benefits are summarized in **Tab. 2.1** and can be leveraged in different ways. In **Tab. 2.1** the multi-cell systems are designed for the same switching losses and the same stored energy as the single-cell system, which results in a strong reduction of the current ripple (i.e. $1/N_{\mathrm{cells}}^2$). Another possible design might be to operate the multi-cell systems with the same effective switching frequency of $f_{\mathrm{sw,0}}$ as the single-cell system (i.e. each cell operates with $f_{\mathrm{sw,0}}/N_{\mathrm{cells}}$). This leads to reduced switching losses of $P_{\mathrm{sw,0}}/N_{\mathrm{cells}}$ as well as a reduced current ripple of $\Delta I_0/N_{\mathrm{cells}}$. Consequently, if the systems are designed for the same current ripple of ΔI_0, a reduction of the switching losses in the multi-cell systems by a factor of $1/N_{\mathrm{cells}}^2$ can be gained.

Furthermore, since standard components with lower voltage and/or current ratings can be employed, the costs for a multi-cell system very likely also decreases.

Different challenges in the design of a multi-cell system include the control and balancing of the cells voltages and/or currents, and other factors that adversely affect the performance of the system with increasing number of cells. As a consequence, for every multi-cell system the number of employed cells is an important optimization parameter.

Tab. 2.1: Scaling laws of multi-cell systems with N_{cells} cells in comparison to a single-cell system. In the parallel interleaved multi-cell system, each converter cell has an inductor with the inductance specified in this table, and the current ripple is the total ripple of the current of the entire multi-cell system. The stored energy is the total energy stored in the inductors of each system and is calculated by considering only the average current through the inductors, i.e. neglecting the current ripple. Furthermore, it is assumed that the cells in the multi-cell systems are operated interleaved to each other with the optimal phase shift of $\delta = 2\pi/N_{\text{cells}}$.

System	**Sw. Freq. per Cell**	**Effective Sw. Freq.**	**Switching Losses**	**Current Ripple**	**Inductance**	**Stored Energy**
Single-Cell	$f_{\text{sw},0}$	$f_{\text{sw},0}$	$P_{\text{sw},0}$	ΔI_0	L_0	$E_{\text{L},0}$
Multi-Cell (Series)	$f_{\text{sw},0}$	$N_{\text{cells}} \cdot f_{\text{sw},0}$	$P_{\text{sw},0}$	$\Delta I_0 / N_{\text{cells}}^2$	L_0	$E_{\text{L},0}$
Multi-Cell (Parallel)	$f_{\text{sw},0}$	$N_{\text{cells}} \cdot f_{\text{sw},0}$	$P_{\text{sw},0}$	$\Delta I_0 / N_{\text{cells}}^2$	$N_{\text{cells}} \cdot L_0$	$E_{\text{L},0}$

3

Multi-Cell Photovoltaic Energy Systems

RENEWABLE energy sources, including hydro power, wind power etc., are gaining an increasing share of the global electricity generation and have reached a share of 19.3% in 2009 [47]. Among these, especially the photovoltaic (PV) technology has been in the focus of many governments and, due to substantial subsidies, a steep rise in the number of installations in those countries has resulted. In some countries, e.g. in Germany, the electricity generated by PV systems already amounts to 30% of the overall electricity generation during some days with a record high of almost 50% in 2012 [48]. With the ongoing trend of declining PV panel prices from $\$4.90/\mathrm{W_{pk}}$ in 1998 to $\$1.28/\mathrm{W_{pk}}$ in 2011 [49], the rate of growth of new PV system installations is expected to remain on a high level and to compensate for diminishing subsidies in the future.

In state-of-the-art PV system installations for residential as well as commercial or utility-scale application, PV panels are connected in series so that the panel output voltages, usually in the range of 15 to 45 V, add up to a voltage of at least around 400 V which is required (in Europe) to feed power into the public grid by means of a central DC/AC converter. Due to this series connection, the output current of all panels is equal to the string current. The current generation of a PV panel, however, is proportionally dependent on the irradiance level. If all PV panels in a string receive the same level of irradiance, the whole string of panels has only one global Maximum Power Point (gMPP) and all panels contribute to the total power of the string (cf. **Fig. 3.1(a)**). In contrast, if the PV panels in a string are subject to different levels of irradiance, e.g. due to local shading of some panels, the output

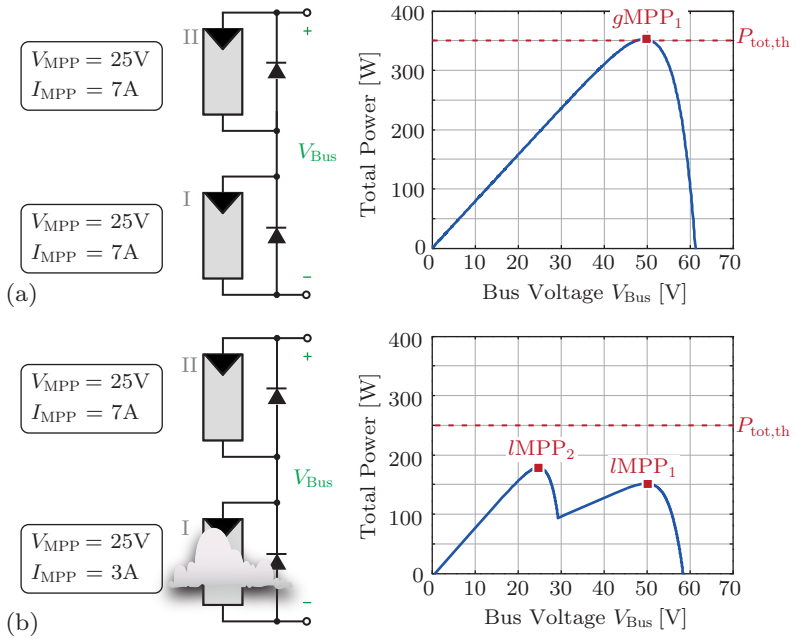

Fig. 3.1: Impact of shading on a simplified PV string formed by only two PV panels: (a) Output power of the PV string with only unshaded panels receiving equal irradiance and (b) with one shaded panel (plotted vs. the total bus voltage V_{Bus}). In the case of unequal irradiance levels, multiple local MPPs (lMPP) are formed by the string but none of them provides the full amount of power $P_{\text{tot,th}}$, available from the PV panels in total.

currents are unequal and the string shows multiple local MPPs (lMPP) as visualized in **Fig. 3.1(b)**. In that case, the panels generating less current than the string current will get reverse biased and their internal bypass diodes will conduct the string current and consequently they will be shorted out, i.e. their power can not be harvested. Alternatively, the string current, which is controlled by the central inverter, can be lowered so that the shaded panels are not bypassed. But then the unshaded panels will not be operating at their MPP. In both scenarios, not all of the theoretically available power $P_{\text{tot,th}}$ of a PV string with N PV panels, which is the sum of MPPs of all PV panels

$$P_{\mathrm{tot,th}} = \sum_{i=1}^{N} P_{\mathrm{MPP,i}} \ , \tag{3.1}$$

can be harvested. This problem of unequal current generation of series-connected PV panels within a string - often referred to as mismatch - is not only caused by shading but also by other factors such as different orientation of PV panels, dirt or dust on panels, different panel manufacturers, unequal aging etc. Especially building-integrated PV modules are prone to orientation mismatch and partial shading.

By equipping each PV panel with a DC/DC converter, the panels can be operated independent from each other in their individual MPPs and the aforementioned problems can be mitigated. Those module integrated converters (MICs) allow to harvest the theoretically available string power $P_{\mathrm{tot,th}}$. However, some reduction of the power generation due to the finite efficiency of the DC/DC converters has to be accepted.

In this thesis, only the concept of distributed DC/DC converters with a central grid-connected DC/AC converter is considered. Module-level DC/AC converters (typically referred to as micro-inverters [50,51]) are not in the scope of this thesis due to a number of disadvantages inherent to this concept. Since the whole DC/AC conversion has to be performed, a two-stage concept is typically employed with a step-up DC/DC converter and a DC/AC inverter with a grid filter. In addition, the power pulsation with twice the grid frequency needs to be filtered/buffered within the module by employing either electrolytic capacitors or a power pulsation buffer concept [52]. Since all of this has to be integrated into each PV module, the overall installation effort increases whereas the reliability and lifetime decreases as all components are exposed to the varying temperatures of the PV modules during the day and night cycles but also over the course of the seasons. In addition, the efficiency of this concept is typically lower compared to concepts with a central DC/AC converter.

3.1 Classification of DC/DC Converter Topologies for PV-Panel Integration

Possible DC/DC converter topologies for PV panel integration can be classified into the two groups of full-power and partial-power converters

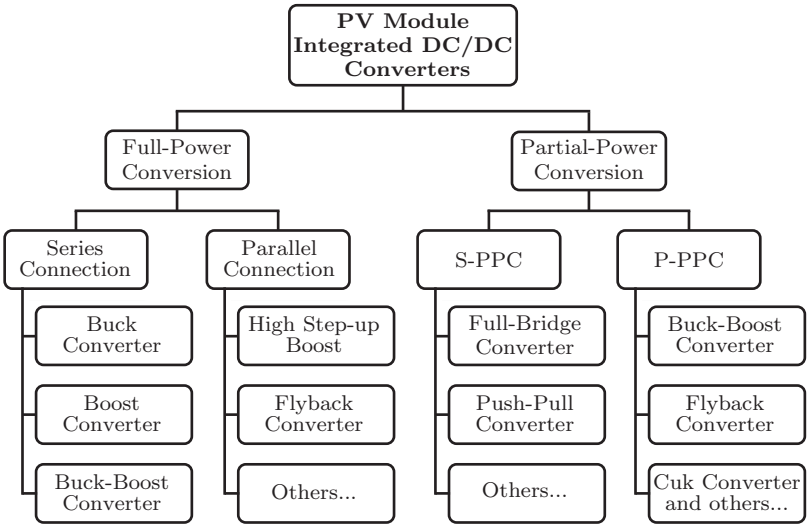

Fig. 3.2: Classification of PV module-integrated DC/DC converter concepts into full-power and partial-power processing converters, each with subcategories of series and parallel connection.

as shown in **Fig. 3.2** and in their basic form in **Fig. 3.3**. In a full-power converter the whole amount of panel power is processed by the converter, whereas in a partial-power converter only a fraction of the panel power has to be converted. The full-power converter concepts can be further divided into series (S-FPC) and parallel connected concepts (P-FPC) [53].

In a similar way, the partial-power converter category contains the subcategories of Series-connected Partial-Power Converters (S-PPC), which add or subtract a voltage in series to the panel output voltage, and Parallel-connected Partial-Power Converters (P-PPC) which equalize the PV panel voltages. The P-PPC concept is also known as "energy shuffler" or "current diverter" concept [54].

Common to all PPCs is the possibility to compensate the mismatch between the PV panels by processing only a fraction of the full panel power. Hence, the total efficiency η_{tot} of the mismatch compensation depends only to a certain extent on the converter efficiency η_{conv} itself [55], [56]. The PPCs are characterized by a splitting of the power

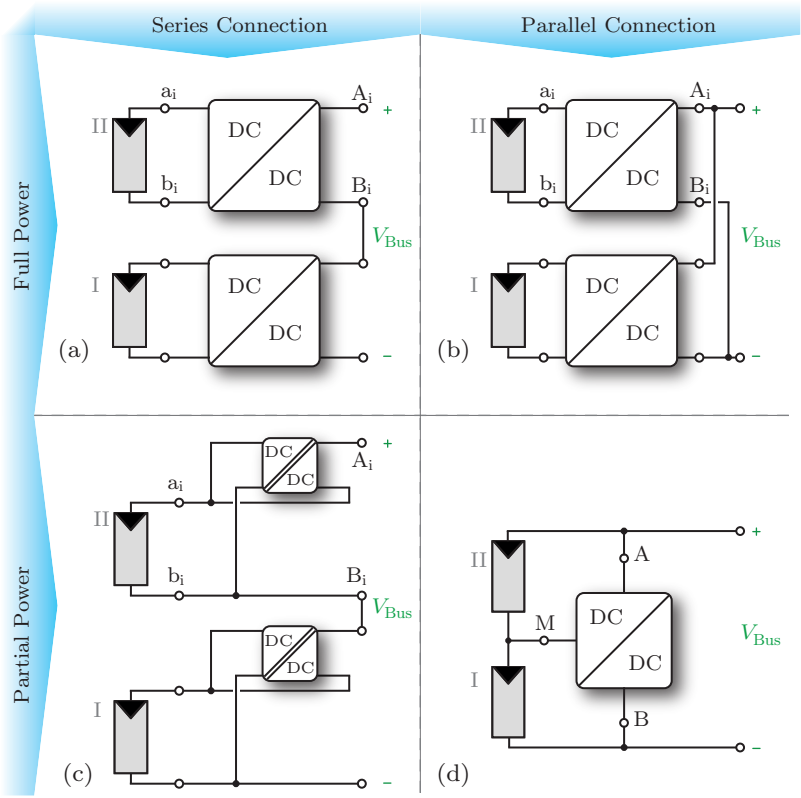

Fig. 3.3: Possible multi-cell structures with DC/DC converters ensuring MPP operation of the individual PV panels, divided into full and partial-power concepts with either series or parallel connection: (a) series-connected full-power converter (S-FPC), (b) parallel-connected full-power converters (S-PPC), (c) series-connected partial-power converters (P-FPC), and (d) parallel-connected partial-power converter (P-PPC).

conditioning into two power flow paths (cf. **Fig. 3.4**) [57], [58]. If one of the paths is highly efficient, e.g. direct power flow from the source to the load with $\eta \approx 1$, then the effective conversion efficiency is increased. The ratio of the power P_c, which is processed by the PPC, to the total power P_{PV}, taken from the PV panel, determines the influence of the PPC efficiency on the total efficiency

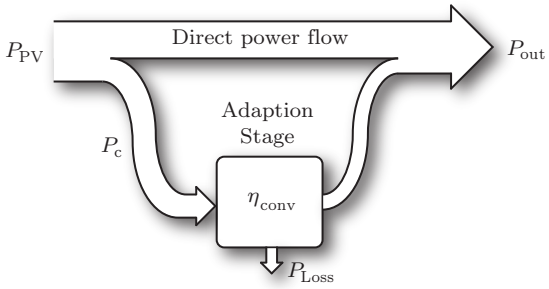

Fig. 3.4: Splitting of the power flow into two parallel power flow paths as given for PPCs. The direct path transfers power from the PV panel to the output without any conversion stage. Only a fraction P_{c} of the panel output power P_{PV} is processed by a voltage (or current) adaption stage with efficiency η_{conv}.

$$\eta_{\mathrm{tot}} = 1 - \frac{P_{\mathrm{c}}}{P_{\mathrm{PV}}} \left(1 - \eta_{\mathrm{conv}}\right). \tag{3.2}$$

This means, if less power is processed by the PPC, a higher system efficiency is achieved. Thus, in the ideal case with no mismatch, the PPC does not have to process any power and the total efficiency approaches 100% (neglecting load independent converter losses e.g. due to control electronics). Furthermore, the PPC can be optimized for a high part-load efficiency, since it will only process large fractions of the PV panel power if high conversion ratios are required, which typically only happens at severe mismatch conditions.

3.2 Series-Connected Full-Power MIC

For series-connected full-power conversion (**Fig. 3.3(a)**) either buck, boost or buck-boost converters can be used [59]. Other topologies like e.g. the Ćuk or SEPIC converter are not considered here due to their higher system complexity. When the PV panels are equipped with buck converters, the output voltage of shaded panels can only be stepped down in order to increase their output current until it matches the current of the unshaded panels (cf. **Fig. 3.5(a)**). Vice versa, if boost converters are employed, the output voltage of unshaded PV panels can be increased in order to lower the output current until it matches the MPP current of the shaded panels (cf. **Fig. 3.5(b)**). The greatest flexibility is given with buck-boost converters (cf. **Fig. 3.5(c)**) where any string current value can be matched by the output currents of the converters.

These three different concepts also have different implications on the number of PV panels per string which are required in order to reach a given bus voltage V_{Bus} of e.g. 400 V despite different levels of irradiance. In a string where all panels are equipped with buck converters, the string voltage may drop below 400 V if panels are shaded, since the adaption to match the current of the unshaded panels is achieved by lowering the voltage of shaded panels. Thus a minimum number of panels per string is required to guarantee the generation of the bus voltage up to a certain degree of shading. The upper limit of the number of PV panels with a buck converter in a string depends on the maximum output current rating of the converters.

With boost converters, the string voltage is prone to exceed the level of 400 V during shading, since unshaded panels increase their output voltage to reach the lower current level of shaded panels. Thus, a maximum number of PV panels per string can be defined for a certain degree of shading. Furthermore, the lower limit of PV panels with boost converters in each string depends on the maximum output voltage rating of the converters.

Buck-boost converters allow to keep the bus voltage constant, since any level of string current can be set. Thus, the upper limit of PV panels per string for the buck-boost converter concept depends on the maximum output current rating and the lower limit depends on the maximum output voltage rating of the buck-boost converters. In **Tab. 3.1** the equations for the maximum and minimum numbers of PV panels

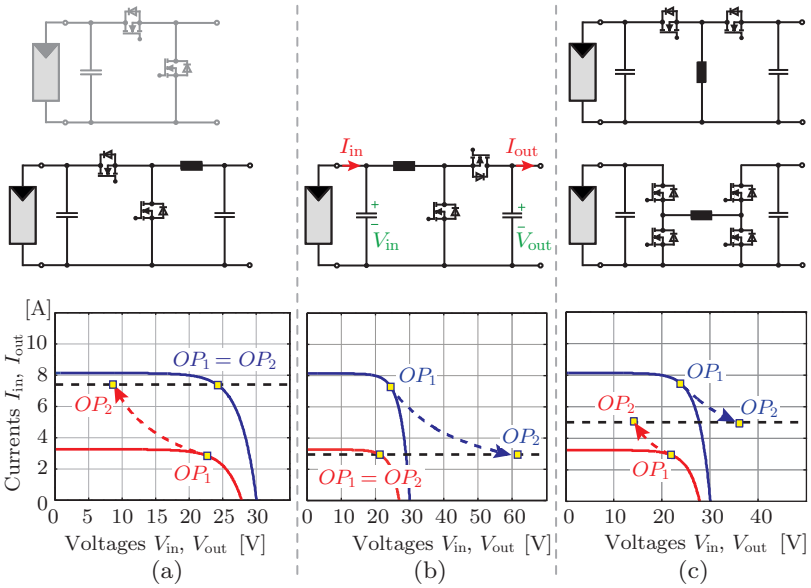

Fig. 3.5: Working principles of full-power converters for a series connection of shaded (red) and unshaded (blue) panels: (a) buck converter, (b) boost converter and (c) buck-boost converter. OP_1: converter input (V_{in}, I_{in}) related to MPP of a PV panel. OP_2: operating point characterizing the converter output (V_{out}, I_{out}). The first converter of (a) (cf. step inverter in [60]), here shown in grey, can either connect the converter output to the PV panel output or bypass the PV panel. The string voltage of a PV string equipped with this converter type exhibits voltage steps and thus an *LC* filter (not shown) needs to be connected to the string.

per string are given for the three different full-power converter topologies under the assumption that all PV panels should be able to feed power into the string under a given shading condition which can be expressed as $\Delta = \frac{P_{PV,unsh}}{P_{PV,sh}}$. An example of those limitations is depicted in **Fig. 3.6**. For this scenario, in case only boost converters are used, the number of panels per PV string has to be in the range of 6 to 11; if all PV panels are equipped with buck converters only, the number of panels has to be between 25 and 32. So, if either only buck or boost converters are chosen, there is no possibility to have between 12 and 24 PV panels in the string. However, with buck-boost converters, any number of PV

Tab. 3.1: Maximum, resp. minimum number of PV panels per string for different MIC topologies, where $I_{\mathrm{out,max}}$ denotes the maximum output current of the converter, V_{MPP} the PV panel voltage in a typical MPP, Δ the fraction $\frac{P_{\mathrm{PV,unsh}}}{P_{\mathrm{PV,sh}}}$ and $P_{\mathrm{PV,max}}$ the maximum output power of the PV panel.

Type	**Max. nr. of PV panels**	**Min. nr. of PV panels**
Buck	$\frac{V_{\mathrm{Bus}}}{P_{\mathrm{PV,max}}} I_{\mathrm{out,max}}$	$\left(\frac{V_{\mathrm{Bus}}}{V_{\mathrm{MPP}}} - 1\right)\Delta + 1$
Boost	$\frac{V_{\mathrm{Bus}} + (\Delta - 1) V_{\mathrm{MPP}}}{\Delta \cdot V_{\mathrm{MPP}}}$	$\left(\frac{V_{\mathrm{Bus}}}{V_{\mathrm{out,max}}} - 1\right)\Delta + 1$
Buck-boost	$\frac{V_{\mathrm{Bus}}}{P_{\mathrm{PV,max}}} I_{\mathrm{out,max}}$	$\left(\frac{V_{\mathrm{Bus}}}{V_{\mathrm{out,max}}} - 1\right)\Delta + 1$

panels between 6 and 32 can be connected in series. Thus, based on the limitations which buck as well as boost converter topologies imply on the number of panels in a PV string, the buck-boost concept is chosen for further consideration. Since MICs in general target residential applications, which are more susceptible to shading than industrial applications, the flexibility provided by buck-boost converters is not only advantageous for the design of a PV system regarding shading, but also allows to fully utilize the available space on a rooftop by setting up multiple PV strings with different lengths.

The global irradiance consists of at least one quarter to one third of indirect irradiance, i.e. diffuse irradiance and reflected irradiance. Therefore, the maximum shading condition Δ_{max}, up to which all PV panels should be able to operate in their MPP, is around $\Delta_{\mathrm{max}} = 3...4$. Furthermore, in order to set up a PV system with the greatest flexibility in the number of PV panels per string, the maximum number of PV panels N_{max} should be equal to $(2 \cdot N_{\mathrm{min}})$. This allows, for example, to split up a string with more panels than N_{max} into two strings with at least N_{min} panels. Based on that, the required maximum output current can be calculated with the formulas for the minimum and maximum converters in a PV string with buck-boost converter (cf. **Tab. 3.1**) as

$$I_{\mathrm{out,max}} = \frac{2 \cdot P_{\mathrm{Pv,max}} (V_{\mathrm{out,max}} + V_{\mathrm{Bus}} \cdot \Delta_{\mathrm{max}} - V_{\mathrm{out,max}} \cdot \Delta_{\mathrm{max}})}{V_{\mathrm{Bus}} \cdot V_{\mathrm{out,max}}} \,. \tag{3.3}$$

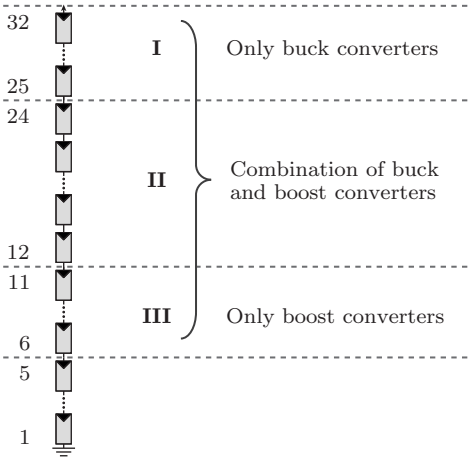

Fig. 3.6: Example of maximum and minimum number of PV panels per string when either only buck converters (**I**) or only boost converters (**III**) are used. The buck-boost converters are combining those two regions and are extending it to the previously unreachable area **II**. (Numbers used for this example: $V_{\mathrm{Bus}} = 400\,\mathrm{V}$, $V_{\mathrm{MPP}} = 25\,\mathrm{V}$, $P_{\mathrm{PV,max}} = 250\,\mathrm{W}$, $\Delta = 1.5$, $I_{\mathrm{out,max}} = 20\,\mathrm{A}$, $V_{\mathrm{out,max}} = 100\,\mathrm{V}$.)

3.2.1 Converter Dimensioning and Optimization

As a result of the evaluation process of **Sec. 3.1**, the full power buck-boost converter concept is selected as the best suited MIC concept for

Tab. 3.2: Specifications of series-connected DC/DC converters for PV panel integration.

Parameter	Variable	Value
Max. converter power	P_{conv}	275 W
Input voltage	V_{in}	15 V...45 V
Max. input current	$I_{\mathrm{in,max}}$	10 A
Output voltage	V_{out}	10 V...100 V
Max. output current	$I_{\mathrm{out,max}}$	20 A
Ambient temperature	T_{amb}	−20°C...+80°C
Bus voltage	V_{Bus}	400 V

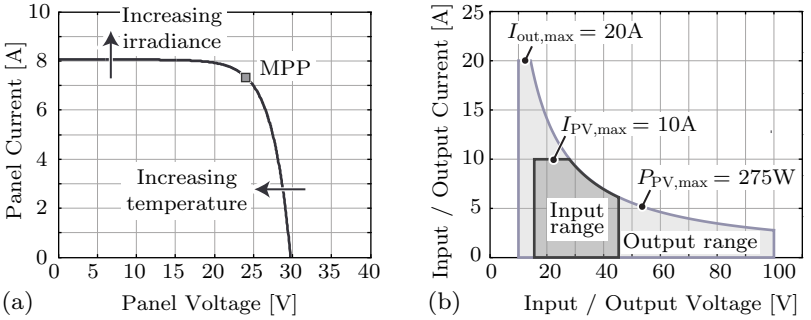

Fig. 3.7: (a) Influence of temperature and irradiance variation on the electrical characteristic of a PV panel and (b) derived input and output specifications of the series-connected PV panel-integrated converter.

series-connected PV panels due to its high flexibility in the number of PV panels per string.

Before the buck-boost converter can be analyzed in detail, the converter specifications have to be defined. The converter input operating range depends on the electrical output characteristic of the PV panel, i.e. dependency of the output current on the output voltage of a PV panel. This characteristic changes with temperature and irradiance level (cf. **Fig. 3.7(a)**) but also depends on the type of PV panel (e.g. polycristalline or monocristalline). In order to cope with these variations, a converter input operating range can be defined as shown in **Fig. 3.7(b)**. The converter output specifications can be derived based on the considerations of the maximum and minimum number of PV panels per string as described in the previous section. With the converter specifications as summarized in **Tab. 3.2** a very high degree of flexibility regarding the arrangement of PV panels within strings is provided as a minimum number of $N_{\text{min}} = 13$ and a maximum number of $N_{\text{max}} = 29$ PV panels can be connected in a string. Furthermore, the system is able to operate all PV panels in their individual MPPs even under severe mismatch conditions up to $\Delta = 4$.

3.2.2 Choice of Converter Topology

The buck-boost converter can be realized by either a 2-switch topology or a 4-switch topology as shown in **Fig. 3.5(c)**. These two converter

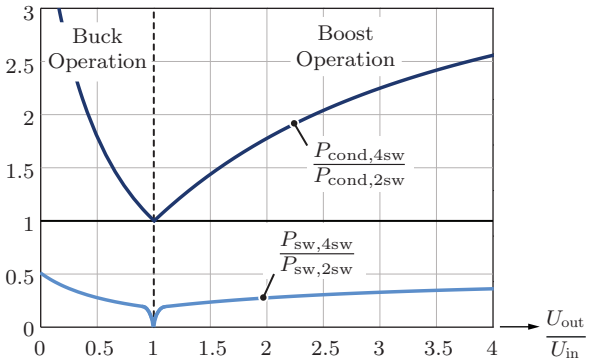

Fig. 3.8: Relation of semiconductor losses, i.e. conduction losses P_{cond} and switching losses P_{sw}, between the 4-switch and the 2-switch buck-boost converter under the assumption that the same total silicon area is used for both converter designs.

topologies are compared to each other regarding their switching and conduction losses, under the assumption that the same total silicon area A_{Si} and the same switching frequency is used for both converter topologies. As a result, the conduction losses and switching losses of the converters can be set in relation. For reasons of simplification, it is also assumed that the 4-switch and the 2-switch buck-boost converter comprise the same kind of switches with a specific technology-dependent on-state resistance $R^*_{\text{DS(on)}} = R_{\text{DS(on)}} \cdot A_{\text{Si}}$ [55].

Since the 4-switch converter is either working in buck or boost mode, with only one bridge-leg being switched, the conduction losses can be obtained in dependence of the transfer ratio $T_{\text{R}} = V_2/V_1$ as

$$P_{\text{cond,4sw}} = \begin{cases} 2 \cdot \frac{R^*_{\text{DS(on)}} \cdot 4}{A_{\text{Si}}} \cdot \left(\frac{P}{T_{\text{R}} \cdot V_1}\right)^2, & \text{if } T_{\text{R}} \leq 1 \text{ (buck mode)} \\ 2 \cdot \frac{R^*_{\text{DS(on)}} \cdot 4}{A_{\text{Si}}} \cdot \left(\frac{P}{V_1}\right)^2, & \text{if } T_{\text{R}} > 1 \text{ (boost mode)} \end{cases} . \tag{3.4}$$

The conduction losses of the 2-switch buck-boost converter can be expressed in a similar way by

$$P_{\text{cond,2sw}} = \frac{R^*_{\text{DS(on)}} \cdot 2}{A_{\text{Si}}} \cdot \left(\frac{P \cdot (1 + T_{\text{R}})}{T_{\text{R}} V_1}\right)^2 . \tag{3.5}$$

For the calculation of the switching losses it can be assumed that only the capacitances C_{oss} of the transistors determine the switching losses during the turn-on operation while the contribution of the junction capacitances and the reverse recovery current of the diodes as well as other parasitic capacitances are neglected. By taking into account the voltage dependency of $C_{\mathrm{oss}}(V_{\mathrm{DS}})$ the loss of energy can be expressed as (cf. [61])

$$E_{\mathrm{S,turn\text{-}on}} = \frac{2}{3} C_{\mathrm{oss,ref}} \sqrt{V_{\mathrm{DS,ref}}} V_{\mathrm{DS}}^{(3/2)} \ . \tag{3.6}$$

Furthermore, the 4-switch buck-boost converter can operate in pass-through mode if the voltage transfer ratio T_F is equal to one. Hence, the switching losses of the 4-switch converter are given by

$$P_{\mathrm{sw,4sw}} = \begin{cases} \frac{2}{3} C^*_{\mathrm{oss,ref}} \frac{A_{\mathrm{Si}}}{4} \sqrt{V_{\mathrm{DS,ref}}} V_1^{(3/2)} f_{\mathrm{sw}}, & \text{if } T_{\mathrm{R}} < 1 \text{ (buck mode)} \\ 0, & \text{if } T_{\mathrm{R}} = 1 \\ \frac{2}{3} C^*_{\mathrm{oss,ref}} \frac{A_{\mathrm{Si}}}{4} \sqrt{V_{\mathrm{DS,ref}}} (T_{\mathrm{R}} V_1)^{(3/2)} f_{\mathrm{sw}}, & \text{if } T_F > 1 \text{ (boost mode)} \end{cases} \tag{3.7}$$

and for the 2-switch converter by

$$P_{\mathrm{sw,2sw}} = \frac{2}{3} C^*_{\mathrm{oss,ref}} \frac{A_{\mathrm{Si}}}{2} \sqrt{V_{\mathrm{DS,ref}}} \left(\frac{V_1}{1 - \frac{T_{\mathrm{R}}}{1+T_{\mathrm{R}}}} \right)^{(3/2)} f_{\mathrm{sw}} \ . \tag{3.8}$$

The values $R^*_{\mathrm{DS(on)}}$ and $C^*_{\mathrm{oss,ref}}$ define a Figure of Merit (FOM) (see (34) in [62]) which denotes a technology limit

$$\mathrm{FOM}_{\eta\rho 1} = \frac{1}{\sqrt{R^*_{\mathrm{DS(on)}} C^*_{\mathrm{OSS,ref}}}} \ . \tag{3.9}$$

The above calculated semiconductor losses of the 2-switch converter in relation to the 4-switch converter are shown in **Fig. 3.8**. It is revealed that the 4-switch converter features lower switching losses but larger conduction losses in the whole operating range. However, in this comparison only the conduction losses in the semiconductors have been considered. Since the inductor current in the 2-switch converter is larger than in the 4-switch converter, the ohmic losses of the inductor and of the PCB tracks of the 2-switch converter will probably be higher than the ones of the 4-switch converter and the difference of the conduction losses will decrease.

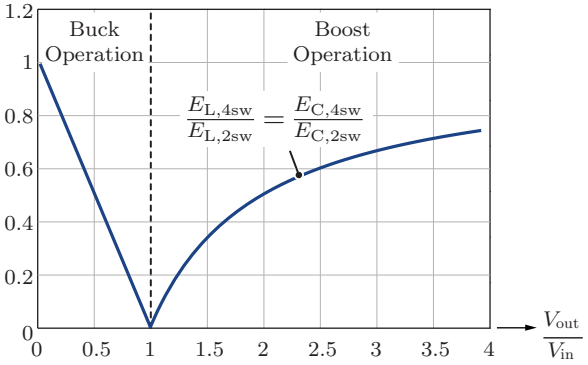

Fig. 3.9: Relation of the energy stored in the inductors and/or capacitors of the 2-switch and the 4-switch buck-boost converter under the assumption of a certain equal relative current and/or voltage ripple $\varepsilon_{\mathrm{vC}} = \varepsilon_{\mathrm{iL}}$.

Furthermore, the relative volume of the passive components can be compared between the two converter types by assessing the stored energy in the inductor and capacitors. With the introduction of tolerable relative voltage and current ripples, $\varepsilon_{\mathrm{vC}} = \Delta v_{\mathrm{C}}/V_{\mathrm{C}}$ and $\varepsilon_{\mathrm{iL}} = \Delta i_L/I_L$ respectively (V_{C} and I_{L} denominate rated values of the capacitor voltage and inductor current resp.), the energy stored in the input and output capacitors (which is related to the physical capacitor volume, see section 5 in [63]) can be expressed for the 4-switch converter as

$$E_{\mathrm{C,4sw}} = \begin{cases} \frac{1}{4}(1-T_{\mathrm{R}})\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{\mathrm{vC}}}{2}\right)^2}{\frac{\varepsilon_{\mathrm{vC}}}{2}}, & \text{if } T_{\mathrm{R}} \leq 1 \text{ (buck mode)} \\ \frac{1}{4}\frac{T_{\mathrm{R}}-1}{T_{\mathrm{R}}}\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{\mathrm{vC}}}{2}\right)^2}{\frac{\varepsilon_{\mathrm{vC}}}{2}}, & \text{if } T_{\mathrm{R}} > 1 \text{ (boost mode)} \end{cases} . \tag{3.10}$$

and for the 2-switch converter as

$$E_{\mathrm{C,2sw}} = \frac{1}{4}\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{\mathrm{vC}}}{2}\right)^2}{\frac{\varepsilon_{\mathrm{vC}}}{2}} . \tag{3.11}$$

In an analogous fashion, the equations for the stored energy in the inductor (which is again related to the component volume [63]) can be expressed for the 4-switch converter as

$$E_{\mathrm{L,4sw}} = \begin{cases} \frac{1}{4}(1-T_{\mathrm{R}})\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{\mathrm{iL}}}{2}\right)^2}{\frac{\varepsilon_{\mathrm{iL}}}{2}}, & \text{if } T_{\mathrm{R}} \leq 1 \text{ (buck mode)} \\ \frac{1}{4}\frac{T_{\mathrm{R}}-1}{T_{\mathrm{R}}}\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{\mathrm{iL}}}{2}\right)^2}{\frac{\varepsilon_{\mathrm{iL}}}{2}}, & \text{if } T_{\mathrm{R}} > 1 \text{ (boost mode)} \end{cases} \tag{3.12}$$

and for the 2-switch converter as

$$E_{\mathrm{L,2sw}} = \frac{1}{4}\frac{P}{f_{\mathrm{sw}}}\frac{\left(1+\frac{\varepsilon_{\mathrm{iL}}}{2}\right)^2}{\frac{\varepsilon_{\mathrm{iL}}}{2}} \ . \tag{3.13}$$

The energy storage requirements of both converter topologies can now be directly related, which yields

$$\frac{E_{\mathrm{L,4sw}}}{E_{\mathrm{L,2sw}}} = \frac{E_{\mathrm{C,4sw}}}{E_{\mathrm{C,2sw}}} = \begin{cases} (1-T_{\mathrm{R}}), & \text{if } T_{\mathrm{R}} \leq 1 \text{ (buck mode)} \\ \frac{T_{\mathrm{R}}-1}{T_{\mathrm{R}}}, & \text{if } T_{\mathrm{R}} > 1 \text{ (boost mode)} \end{cases} \tag{3.14}$$

as shown in **Fig. 3.9**. The comparison of semiconductor losses as well as the ratio of the stored energies and/or volumes of passive components indicates benefits for the 4-switch topology, which accordingly is selected for further dimensioning and optimization. In addition, with a special modulation scheme, the 4-switch converter can also be operated in a soft-switching mode [64] which results in lower switching losses. However, this modulation scheme induces higher RMS values of the inductor current and an increased complexity in the control scheme and thus is not considered in this thesis.

3.2.3 Converter Modeling and Optimization Routine

In this section the general converter optimization procedure is described and the results for a converter realization with Si MOSFETs with a switching frequency of 100 kHz and a converter with GaN FETs with a switching frequency of 400 kHz are shown.

For a comprehensive and meaningful characterisation of the converter, the trade-off between efficiency and power density can be visualized by means of a η-ρ-Pareto front. For calculating the η-ρ-Pareto front, the volume of the employed components and their losses must be identified for each design, as shown in the design procedure of **Fig. 3.11**. The main losses can be categorized into:

- Switching losses (P_{semi}) of MOSFETs including gate drive losses.

- DC, skin effect and proximity effect winding losses (P_{DC}, P_{sk} and P_{pr}) and core losses (P_{core}) of the inductor.
- Ohmic losses of the PCB tracks (P_{PCB}) and conduction losses due to the on-state resistance of the MOSFETs ($P_{\mathrm{Rds,on}}$).
- Constant losses (P_{const}), i.e. power consumption of the auxiliary supply for the DSP, current and voltage sensors and other peripheral electronics.

Switching Losses ($P_{\mathbf{semi}}$)

The choice of input side switches (i.e. at the side which is connected to the PV panel) is based on the required blocking voltage, which is defined by the upper limit $V_{\mathrm{in,max}}$ of the converter input voltage range, cf. **Fig. 3.7**. Thus, MOSFETs with a blocking voltage capability of at least 60 V are required for the input side and MOSFETs with a voltage rating of around 150 V are sufficient for the output side. Resulting from the wide operating range, the output side switches virtually have to cope with a power of $V_{\mathrm{out,max}} \cdot I_{\mathrm{out,max}} = 2\,\mathrm{kW}$.

The switching losses of the MOSFETs strongly depend on the specific PCB layout which has to be optimized with regard to parasitic inductances in the commutation paths. This is in particular the case for low load impedances, i.e. for operating points with low voltage and high current as possibly occurring in buck operation. In combination with different gate drives and variations of the gate resistance, an accurate analytical modeling of the switching losses becomes very challenging. Thus, switching loss measurements have been conducted with a small set of suitable switches from different manufacturers and, where applicable, LTSPICE simulations have been performed to build up a loss database containing the energy loss E_{semi} occuring within a switching period, depending on the switched current and voltage for a certain junction temperature.

Inductor Design and Losses ($P_{\mathbf{DC}}$, $P_{\mathbf{pr}}$, $P_{\mathbf{sk}}$ and $P_{\mathbf{core}}$)

The converter is designed to work in Continuous Conduction Mode (CCM) and thus shows a DC inductor current with superimposed switching frequency-dependent ripple. The value of the inductor is chosen considering a limitation of the current ripple to a maximum of $\pm 3\,\mathrm{A}$ which is equal to $\pm 30\%$ of the maximum input current $I_{\mathrm{in,max}}$. As shown in

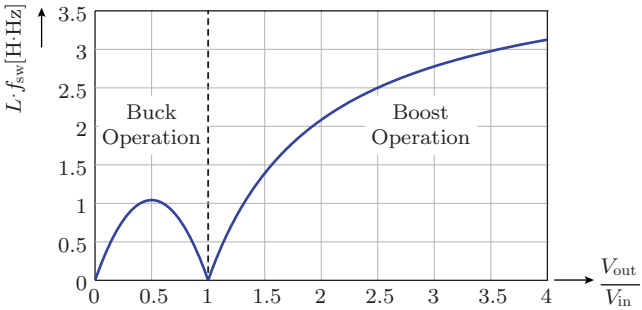

Fig. 3.10: Normalized inductance value in dependency of the output to input voltage ratio for an operating point of $V_{in} = 25\,V$ and a maximum current ripple of $\pm 30\%$ of $I_{in,max}$.

Fig. 3.10, the worst-case requirement to maintain this limit is given by the highest boost ratio operating point, i.e. for $V_{out,max} = 100\,V$. Moreover, an inductor design is only valid, if the maximum flux density B_{pk} in the core with cross section A_c is well below the saturation flux density of the core material. The peak flux density can be calculated as

$$B_{pk} = \frac{L \cdot I_{pk}}{N \cdot A_c} \ , \tag{3.15}$$

where N is the number of turns and I_{pk} is the peak current which can be determined as the sum of the maximum average current according to (3.3) and the ripple current.

The core losses of the inductor can be calculated for non-sinusoidal flux waveforms with the improved Generalized Steinmetz Equation (iGSE) [65] which yields the power loss per unit volume,

$$P_{V,core} = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt \ , \tag{3.16}$$

with ΔB being the peak-to-peak flux density and

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \ , \tag{3.17}$$

where α, β and k are material parameters that can be deduced from manufacturer's data sheets of a core material by curve fitting. Accord-

ing to [66], these parameters have to be adapted to take the DC-bias into account. Furthermore, (3.16) can be simplified for piece-wise linear flux density waveforms as present in the converter [67].

The winding losses are caused by the conduction losses of the DC inductor current and by eddy currents which increase with increasing frequency. The eddy currents lead to skin effect and proximity effect losses which can be determined by means of FEM simulations for a specific core design or by analytical approximations as summarized in [68].

Capacitor Selection

Similar to the current ripple criterion for the inductor value, a voltage ripple criterion has to be defined for the input and output capacitors. In [69] it was shown, that the voltage ripple at the PV panel should be kept below 8.5% of the MPP voltage in order to extract 98% of the available panel power. This statement mainly focuses on MPP trackers which periodically change the converter input voltage in order to track the MPP of the PV panel. The voltage ripple which is caused by the switching transients should be kept to a minimum in order to not influence the MPP tracker. Thus, the maximum relative peak-to-peak voltage ripple at the input and output is limited to around 2%, which yields $C_{\mathrm{in}} \cdot f_{\mathrm{sw}} \approx 7\,\mathrm{F} \cdot \mathrm{Hz}$ and $C_{\mathrm{out}} \cdot f_{\mathrm{sw}} \approx 4.5\,\mathrm{F} \cdot \mathrm{Hz}$.

3.2.4 Optimization Results and Experimental Verification

In this section, the optimization results for two semiconductor technologies, i.e. Si and GaN, are shown and experimentally verified by prototypes. First, the GaN technology is described and the differences to Si and SiC are pointed out. Furthermore, different ways of measuring a converter efficiency are compared and the measurement setup, which was finally used for the measurements of the prototypes, is described. In addition, the control schemes of the converter as well as the PV system, composed of multiple PV panels with integrated DC/DC converters and the subsequent inverter, are presented.

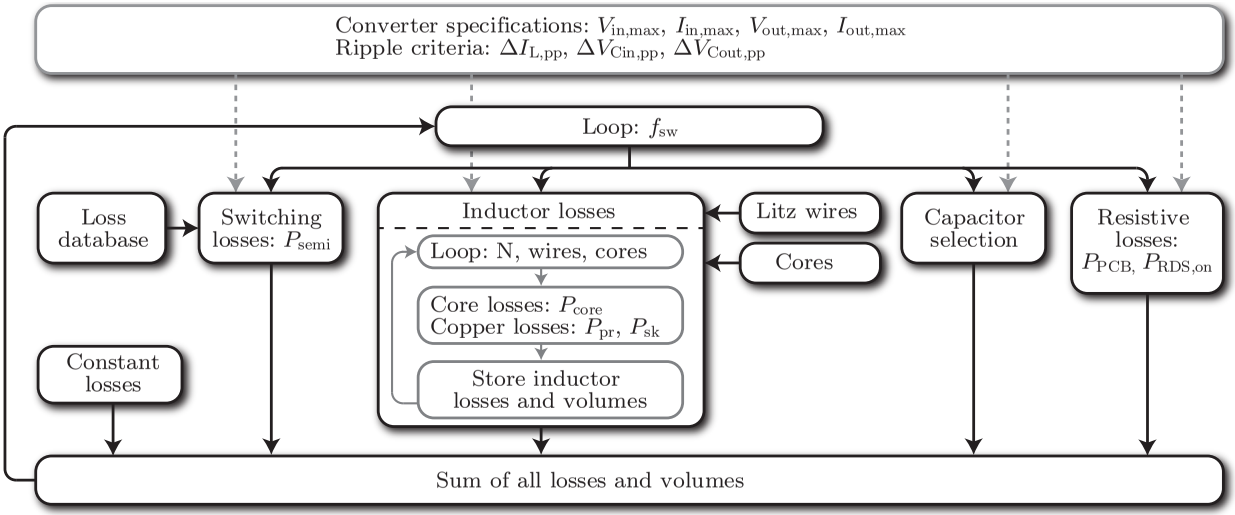

Fig. 3.11: η-ρ-Pareto optimization algorithm for the 4-switch buck-boost converter: A loop over a range of switching frequencies is executed and for each switching frequency a converter design is calculated based on the converter specifications and ripple criteria. This includes the design of the main inductor which is executed in an inner loop to minimize the losses where all available core sizes are considered. As a result of the optimization, all converter losses and converter volumes are stored in order to determine the feasible efficiency vs. power density performance space.

GaN Transistor Technology

For the past 30 years, after its first appearance in 1976 as an alternative to bipolar transistors, the Si MOSFET has dominated the area of switching power conversion in the low power range due to its advantageous properties as an unipolar device, no threshold voltage in forward direction, easy controllability of the switching speed via gate resistances, lack of tail currents, ruggedness and fast switching speeds [29]. But, since the development of superjunction MOSFETs [5] and the related overcoming of the silicon limit, the rate of improvement has slowed down. However, with the recent introduction of enhancement-mode Gallium-Nitride-on-Silicon transistors, the switching Figure of Merit ($R_{\mathrm{DS,on}} \cdot Q_{\mathrm{GD}}$) has been significantly improved by a factor of six for 200 V devices and by a factor of two to three for 40 V and 100 V devices [70]. The major benefits of GaN FETs arise from the physical properties of Gallium Nitride as a wide band-gap material like Silicon Carbide (SiC). Wide band-gap materials posses a higher critical electric field strength than silicon which allows to manufacture devices with a lower on-state resistance $R_{\mathrm{DS,on}}$ at a given maximum blocking voltage capability. A distinctive feature of GaN in combination with an AlGaN layer is the formation of a two-dimensional electron gas (2DEG) with unusually high electron mobility that facilitates even smaller devices for a certain on-resistance and maximum operating voltage than realizable with SiC [70]. The maximum allowable operating voltage of this type of devices is not defined by an avalanche break-down mechanism as for a pn-junction, a metal-semiconductor contact (Schottky barrier) or metal-oxide-semiconductor but by a subthreshold leakage (STL) current that increases with increasing drain-source voltage [71], [72]. Furthermore, due to the pure lateral structure of GaN FETs, no parasitic pn-diode is inherently present as given for vertical Si MOSFET structures. However, a reverse biased GaN FET operates in a similar manner as a body diode but due to a different mechanism [70]. Thus, for reverse conduction, no minority carriers are involved so that no reverse recovery losses are generated. These advantages enable the design of converter systems with higher switching frequencies at the same efficiency, which leads to reduced volumes of passive components and thus to an overall increase in power density.

As a drawback, the recent generation of GaN FETs is not avalanche rated, thus special care has to be taken to prevent transient overvoltages. Moreover, the gate-source voltage must not exceed an upper limit

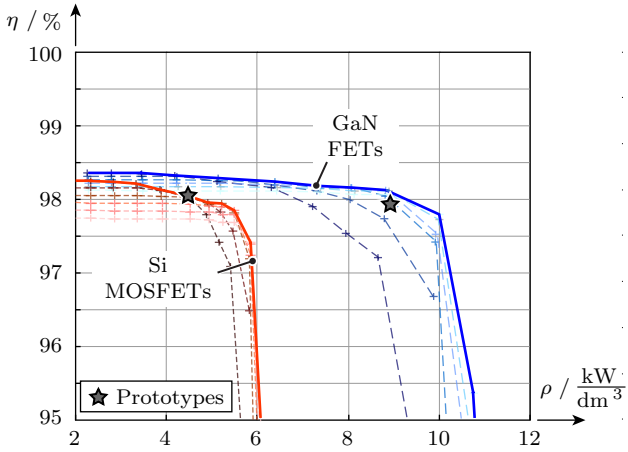

Fig. 3.12: Results of the η-ρ-Pareto optimization for a 4-switch buck-boost converter with either Si MOSFETs or GaN FETs. The efficiency is calculated as mean value of two operating points, i.e. at an input voltage of 30 V and an output voltage of 20 V and/or 40 V with an input power of 200 W. Solid lines represent the Pareto fronts of each semiconductor technology whereas the dashed lines are results for specific switching frequencies (20 kHz...500 kHz). The power density is calculated based on the sum of all component boxed volumes.

of 6 V which requires the application of gate drives with voltage clamping. Because of a rather low threshold voltage of around $V_{\mathrm{GS,th}} = 1.6\,\mathrm{V}$, the gate to source path needs to be designed for minimum inductance in order to prevent an erroneous turn-on of the switch in case of fast switching transients in rectifier operation.

Optimization Results and Prototype Realizations

The results of the η-ρ-Pareto optimization of the buck-boost converter are comparatively shown for both semiconductor technologies, i.e. Si MOSFETs and GaN FETs, in **Fig. 3.12**. In order to ensure a fair comparison, the efficiency shown in the graph is calculated as a mean value of the efficiencies given for boost operation ($V_{\mathrm{in}} = 30\,\mathrm{V}$, $V_{\mathrm{out}} = 40\,\mathrm{V}$) and buck operation ($V_{\mathrm{in}} = 30\,\mathrm{V}$, $V_{\mathrm{out}} = 20\,\mathrm{V}$) at an input power of 200 W. The advantages of lower switching losses of GaN FETs in comparison to Si MOSFETs can be leveraged in two dimensions: a

converter system can be realized with a higher power density at the same efficiency or with a higher efficiency at the same power density compared to the Si-based system.

Based on the results of the Pareto optimization two converter designs with different switching frequencies but same efficiency have been selected for realization as prototypes (cf. **Fig. 3.12**).

The Si MOSFET based converter prototype (**Fig. 3.13(a)**) operates at a switching frequency of 100 kHz. The main inductor ($L \approx 30\,\mu H$) of the converter is realized using an N87 ETD34 ferrite core.

For the second prototype (**Fig. 3.13(b)**) GaN FETs have been selected as input and output side switches in combinations with the recommended half-bridge gate driver IC LM5113 / TI for GaN FETs. Since the switches and the gate drives are only rated for 100 V, the boost operation range is limited to a maximum output voltage of around 70 V. The prototype features a main inductance of 7 µH consisting of an EFD25 core, also made of N87 ferrite material. Consequently the inductor volume is decreased from 22.6 cm^3 to 8.7 cm^3 ($\approx -62\%$).

Efficiency Measurement Setup

For highly accurate efficiency measurements of converters with losses in the lower Watt range, a special measurement setup is required. In general, there are basically three possibilities how efficiency measurements can be performed:

- Measurement of input and output using a power analyzer.
- Separate measurements of input and output voltages and currents, which allows a high accuracy in case of DC quantities.
- Calorimetric measurements, i.e. the direct measurement of the losses in combination with the measurement of the input or output power.

Using a power analyzer is the most convenient way and therefore usually the first choice. However, measurements of a DC/DC converter for a typical operating point of a PV module, even with a high performance power anaylzer such as the WT3000 / Yokogawa, lead to an efficiency accuracy of only $\pm$ 0.18%. This would mean, that a measurement result of e.g. 98.5% would only indicate that the actual value is in between 98.32% and 98.68%.

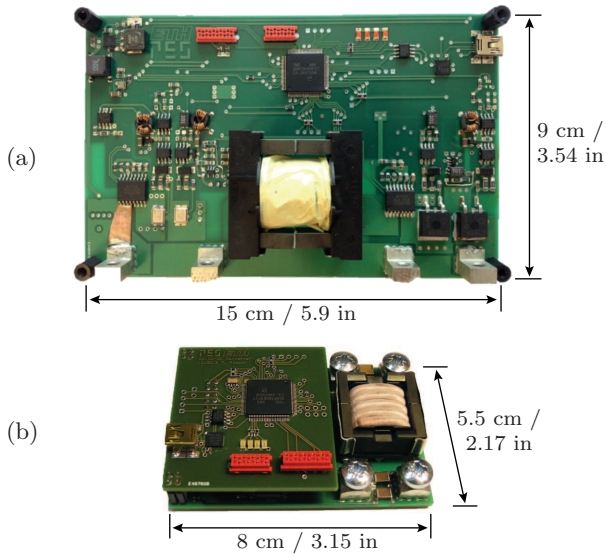

Fig. 3.13: PV panel-integrated buck-boost converter prototypes: (a) Prototype with Si MOSFETs (input side: BSB028N06NN3 / Infineon in Can-Pak package, output side: IPB072N15N3 / Infineon in D2Pak package) and 100 kHz switching frequency, and (b) prototype with GaN FETs (EPC2001 / EPC) and 400 kHz switching frequency.

With calorimetric methods, the efficiency is determined by measuring the dissipated heat [55]. However, this method requires special equipment such as a calorimetric chamber and for each measurement some time has to be allowed until a thermal steady state has been reached. Thus, this method is not suitable, especially for measurements of several different operating points.

Consequently, the efficiency measurements have been performed by separately measuring input and output voltages and currents as shown in **Fig. 3.14**. The setup consists of a Solar Array Simulator (E4360 / Agilent) as power source, two calibrated measurement shunts (1282 / Burster) and four high-precision voltmeters (34410A / Agilent) for the measurement of the converter input and output voltage and the voltage across the shunt resistors for precise current measurements and an electronic load (63202 / Chroma). The voltmeters are synchronously triggered by a function generator (33220A / Agilent) in order to mea-

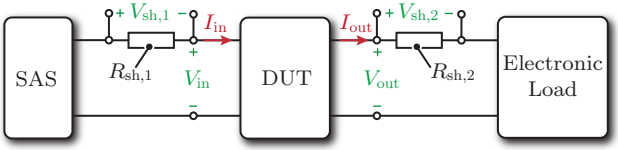

Fig. 3.14: High precision efficiency measurement setup comprising a solar array simulator (SAS), the converter as device under test (DUT), an electronic load, highly accurate voltmeters and shunt resistors for current measurements.

sure all values at the same point in time. All devices are centrally controlled by a computer via MATLAB. The converter efficiency can thus be calculated as

$$\eta_{\mathrm{Conv}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}} I_{\mathrm{in}}} = \frac{V_{\mathrm{out}} \frac{V_{\mathrm{sh,2}}}{R_{\mathrm{sh,2}}}}{V_{\mathrm{in}} \frac{V_{\mathrm{sh,1}}}{R_{\mathrm{sh,1}}}} \ . \tag{3.18}$$

The accuracy of this method for a typical operating point is $\pm\, 0.05\%$, i.e. over three times more accurate than a measurement using a power analyzer.

Experimental Results

The efficiency measurements have been performed at a fixed input voltage of $V_{\mathrm{in}} = 30\,\mathrm{V}$ and for different output voltages and input power levels. The results for the Si and GaN converters are depicted in **Fig. 3.15(a)** for buck operation with output voltages of 20 V and 25 V as a function of the input power. In a similar way, the results for boost operation are depicted in **Fig. 3.15(b)** for both converter prototypes for output voltages of $V_{\mathrm{out}} = 35\,\mathrm{V}$ and $V_{\mathrm{out}} = 40\,\mathrm{V}$ for different input power values.

A comparison of measured efficiency values of both converter prototypes together with results for a commercial converter for PV panel integration, which employs the same 4-switch buck-boost topology as the prototypes, is depicted in **Fig. 3.16**. In addition, the measured efficiency of the GaN converter for 100 kHz switching frequency is also shown. Due to the lower switching frequency and in order to mainly compare the semiconductor devices, the main inductor of the Si converter was used in the GaN converter for this measurement. The results show, that the GaN converter has higher conduction losses, since the

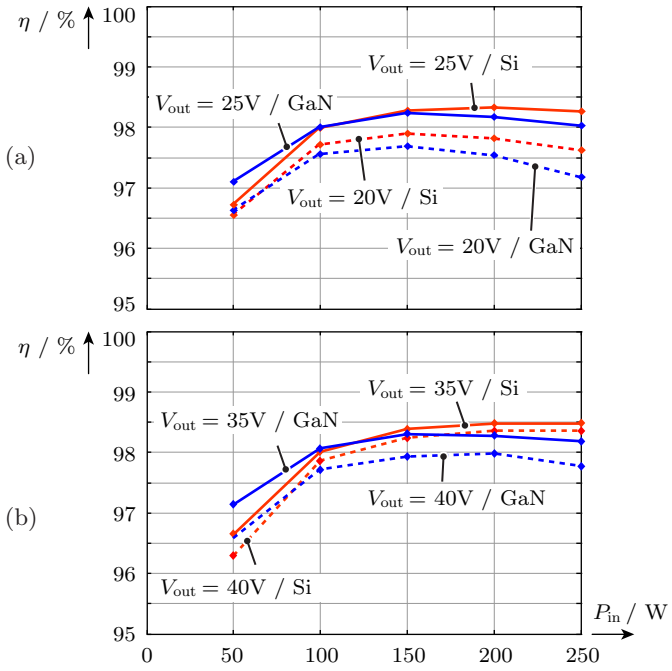

Fig. 3.15: Efficiency measurement results of the Si converter prototype ($f_{sw} = 100\,\text{kHz}$) and the GaN prototype ($f_{sw} = 400\,\text{kHz}$): (a) buck operation at 30 V input voltage and output voltages of 20 V and 25 V for different levels of input power P_{in} and (b) boost operation at 30 V input voltage and for output voltages of 35 V and 40 V for the same levels of input power P_{in}.

efficiency in buck mode (with decreasing output voltage and thus rising output current) drops below the efficiency of the Si converter for the same switching frequency (100 kHz). This is due to the fact, that, according to the data sheets, the total $R_{DS(on),max}$ value of the switches in the Si converter is only 10 mΩ, whereas in the GaN converter the total value is 14 mΩ (+40%). Furthermore, since the chip area of the GaN switches is very small, the PCB copper traces are in general somewhat shorter but also less wide and therefore they very likely lead to higher PCB conduction losses. If the GaN converter is operated at a switching frequency of 400 kHz, then, besides four times higher switching losses, also higher inductor losses occur.

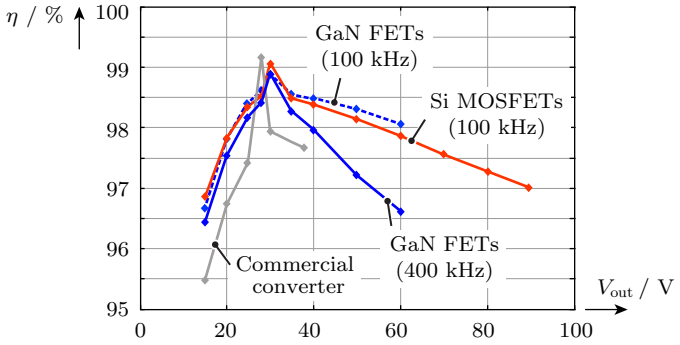

Fig. 3.16: Efficiency measurement results of the Si converter prototype with a switching frequency of 100 kHz and the GaN converter with a switching frequency of 400 kHz and also with 100 kHz in comparison to a commercial PV panel-integrated buck-boost converter. The measurements were performed with an input voltage V_{in} of 30 V and an input power P_{in} of 200 W.

3.2.5 Control of Converter and PV System

The PV panel exhibits one operating point ($V_{PV,MPP}$, $I_{PV,MPP}$) that results in a maximum panel output power at a certain irradiance and temperature. The panel-integrated converter thus needs to constantly track this operating point as it changes during the course of the day due to the moving sun, shadows, e.g. caused by passing clouds, and changing panel temperature. In literature, many MPP tracking algorithms have been proposed and comparatively evaluated [73]. It was found, that the perturb and observe (P&O) method provides a good performance with low complexity and is thus selected for implementation in the prototypes. The controller consists of a cascaded structure where the outer loop comprises the MPP tracker that multiplies the measured values of panel voltage and current to determine the panel output power (cf. **Fig. 3.17**). The inner loop controls the panel current which receives reference values from the MPP tracker. The MPP tracker constantly varies the current reference value and the direction of perturbation is based on the previous step and the corresponding change in panel power. The current controller has to be comparably fast in order to decouple the control loops. The transfer function of the converter changes as the converter operation moves from buck to boost mode or vice versa, which has to be considered in the design of the

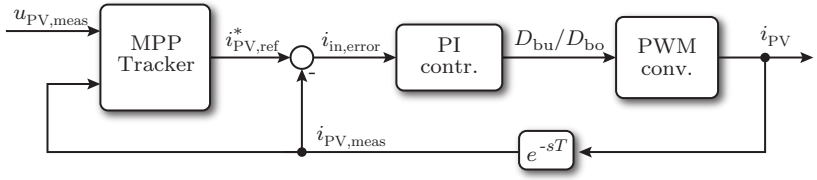

Fig. 3.17: Cascaded converter control with the MPP tracker as (slow) outer control loop and the PV current controller as (fast) inner control loop.

current controller. The small-signal transfer function of the duty cycle to the PV panel current can be found using the state-space averaging approach [74] for the buck converter with a stationary duty cycle D_{bu} as

$$G_{\mathrm{id,buck}}(s) = \frac{I_0 \cdot L \cdot C \cdot s^2 + C \cdot D_{\mathrm{bu}} \cdot V_{\mathrm{PV}} \cdot s + I_0}{C \cdot L \cdot s^2 + 1} \tag{3.19}$$

and for the boost converter with a duty cycle D_{bo} as

$$G_{\mathrm{id,boost}}(s) = \frac{(1 - D_{\mathrm{bo}})I_0 + C \cdot V_{\mathrm{PV}} \cdot s}{(1 - D_{\mathrm{bo}})^2 + C \cdot L \cdot s^2} \tag{3.20}$$

where I_0 denotes the converter output current i.e. the string current. The string current is controlled by the central (string) inverter and thus exhibits slower dynamics. The transition from buck to boost mode and vice-versa is implemented as described in [75]. When the output voltage is equal to input voltage, a so-called pass-through mode can be activated where only the upper switches of each bridge-leg are turned on, which allows to mitigate any switching losses by connecting the converter input via the inductor with the converter output. However, in this case the controllability is lost as the MPP tracker can no longer determine whether the panel is operated in its MPP. One method to overcome this problem is to periodically leave the pass-through mode and to sweep through a certain range of operating points in order to determine whether other operating points can deliver more power [76].

The control of the full system does not require any communication between the individual PV panel-integrated converters or between the panel-integrated converters and the central DC/AC grid converter. Each panel-integrated converter can track the MPP of the attached PV panel as described above. As a consequence, the converter output

voltage is not controlled by the panel-integrated converter but its value depends on the output power of the attached PV panel and the string current, which is common for all converters. Thus, the central DC/AC inverter can control the bus voltage V_{Bus} by adapting the string current I_{str}. The steady-state output voltages of the converters can be calculated for a system with N PV panels as

$$V_{\mathrm{out},i} = \frac{P_{\mathrm{PV},i}}{I_{\mathrm{str}}} = \frac{P_{\mathrm{PV},i} \cdot V_{\mathrm{Bus}}}{P_{\mathrm{PV,tot}}} = \frac{P_{\mathrm{PV},i} \cdot V_{\mathrm{Bus}}}{\sum_{j=1}^{N} P_{\mathrm{PV},j}},\ i \in \{1, 2, ..., N\}\ . \tag{3.21}$$

An example of a PV system with only two PV panels with buck-boost converters and a bus voltage of only 120 V is depicted in **Fig. 3.18**. For extreme irradiance differences between the panels (e.g. due to unequal shading), the converter output voltage of the panel with the highest output power might reach the upper limit. In that case, this converter has to deliberately move the operating point out of the MPP to reduce the input power until the output voltage is no longer at the maximum value. To overcome this problem, additional communication between the panels or the implementation of a supervisory control circuit are necessary [77].

3.2.6 Summary

For the class of series-connected full-power PV module integrated converters, the buck-boost converter topology is identified as the most promising concept for PV panel integration due to the great flexibility it provides with regard to the number of panels per PV string for a fixed DC bus voltage. An optimization and modeling procedure is described in detail, which allows to obtain an efficiency / power densitiy (η-ρ) Pareto front. Based on the results of the analytical modeling, two prototypes of the full-power processing buck-boost concept are realized for a rated power of 275 W and an input/output voltage range of $V_{\mathrm{in}} = 15...45\,\mathrm{V}$ and $V_{\mathrm{out}} = 12.5...100\,\mathrm{V}$ with either Si MOSFETs with a switching frequency of 100 kHz or GaN FETs with a switching frequency of 400 kHz. Both converters feature efficiencies of up to 98.5% in switch-mode operation and 99% in pass-through operation.

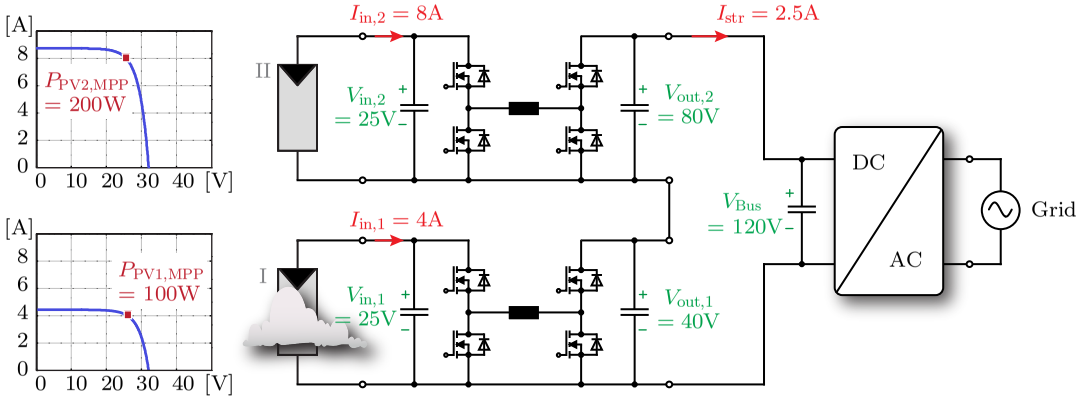

Fig. 3.18: Example of a PV system which employs for reason of simplification only two PV panels with integrated buck-boost converters and generates accordingly a low bus voltage V_{Bus} of only 120 V. Each converter tracks the MPP of the attached PV panel and the central DC/AC converter controls the bus voltage with a reference value of 120 V. The converter output voltages $V_{\mathrm{out},1}$ and $V_{\mathrm{out},2}$ reach a steady-state value according to (3.21).

3.3 Parallel-Connected Full-Power MIC

In this section, the approach of the parallel-connected full-power PV-panel integrated converters is investigated where every PV panel is equipped with a DC/DC converter and the converter outputs are connected in parallel, i.e. to the DC-bus at the central DC/AC converter input, as shown in **Fig. 3.19**. This requires the use of an appropriate DC/DC converter topology with high step-up ratio and, at the same time, also a high conversion efficiency.

At first, different topologies that meet these requirements are identified and evaluated and the most suitable concept is selected for an in-depth analysis and optimization. The η-ρ (efficiency/power density) Pareto optimization and the corresponding results are presented subsequently. Based on the optimization outcome, a prototype employing only GaN switches is assembled and the measurement results are shown afterwards.

3.3.1 Classification of High Step-Up Topologies

In literature, several converter topologies have been proposed with both high step-up ratios and high efficiency. Those topologies can be classified into two main categories of isolated and non-isolated concepts. Depending on the country where the PV system is installed, it might be necessary to include an isolation stage in the PV panel integrated

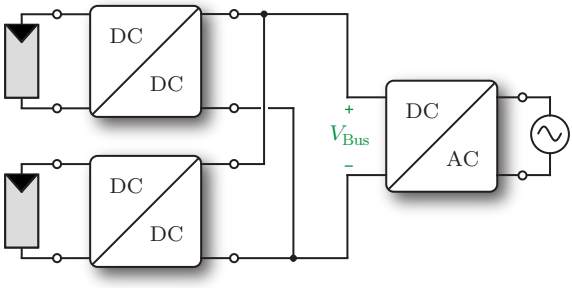

Fig. 3.19: Simplified PV system consisting of two PV panels with high step-up panel-integrated DC/DC converters and a central DC/AC converter. Each PV panel output voltage is stepped-up to reach the level of the bus voltage V_{Bus} of the central DC/AC converter.

DC/DC converters. However, the criteria for selecting the best suited concept for PV panel integration are common to both categories: high conversion efficiency both at full and part load, easy controllability, high power density and low part count for reduced costs as well as a long system lifetime.

Non-isolated Topologies

Non-isolated high step-up converters are usually either boost converters with coupled inductors (**Fig. 3.20(a)**) [78–81] or boost converters combined with a flyback converter [82–84] (**Fig. 3.20(b)**). A high conversion efficiency can be achieved with soft-switching if additional circuits are added to these basic concepts. The converters are extensions of the conventional boost converter structure, in which large duty cycles would occur at high conversion ratios. As a consequence, the conventional boost converter would suffer from low efficiency due to high switching losses resulting from hard switching at high voltage and from the reverse recovery effect of the diode. Additionally, since the voltage conversion ratio of the boost converter is a non-linear function of the duty cycle, large duty cycles would also have a negative effect on the control dynamics.

High conversion ratios can also be achieved with voltage multiplier topologies, such as e.g. switched-capacitor converters [85, 86]. A drawback of these topologies is the limited controllability of the output voltage, which is usually an integer multiple of the input voltage and thus not continuously adjustable. This controllability would only be given for a more complex hybrid combination of a switched-capacitor and an inductor-based converter [87].

Isolated Topologies

Isolated DC/DC converter topologies usually employ a high frequency transformer. A transformer is inherently well suited for the application in converters with a high voltage conversion ratio, as the step-up ratio can be set with the turns ratio. The topologies with a transformer can work with either unidirectional core excitation, as e.g. given for flyback or forward converter, or with bidirectional core excitation (push-pull, half-bridge or full-bridge converter). Since the former category exhibits phases within a switching period, where no power is transferred to the load, their power density and efficiency are lower compared to the lat-

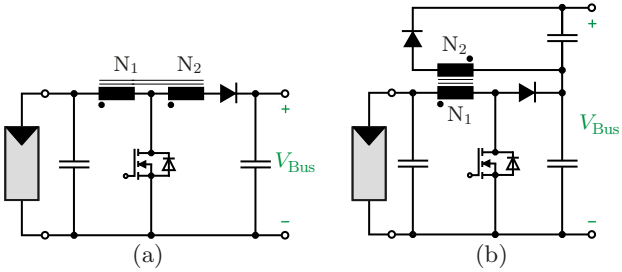

Fig. 3.20: Non-isolated high step-up converter topologies: (a) boost converter with tapped inductor and (b) boost-flyback topology.

ter category and thus are not considered further. For reduced switching losses and component stresses either additional auxiliary circuits, e.g. snubber circuits, can be used or topologies with an inherent ZVS/ZCS capability, such as the resonant half-bridge and full-bridge converters can be selected [88]. The series resonant converter (SRC) is especially well suited for applications with high output voltage and high efficiency at part-load operation [74] and is therefore selected for further consideration (cf. **Fig. 3.21(a)**). As the input voltage needs to be stepped up, the SRC is advantageously equipped with a full-bridge inverter and a voltage doubler as rectification circuit, in order to reach the highest voltage transfer ratio at a given transformer turns ratio.

In combination with MOSFETs, it is preferable to operate the SRC above resonance [89] as this allows utilizing the resonant current at the switching instant to achieve ZVS.

Selection of Topology

From the aforementioned classification of topologies, the SRC offers the advantages of high efficiency, as it can operate without (low) switching losses due to ZVS, and a high power density because of its bidirectional core excitation. However, the switching frequency has to be adjusted in order to vary the voltage transfer ratio of the converter such that the varying PV panel voltage is stepped-up to a fixed output voltage level.

Based on the SRC circuit depicted in **Fig. 3.21(a)** the equivalent circuit for the fundamental harmonics analysis (FHA) can be derived, as visualized in **Fig. 3.21(b)**. The resonant network reacts mainly to the first harmonic of the square wave voltage produced by the full-bridge

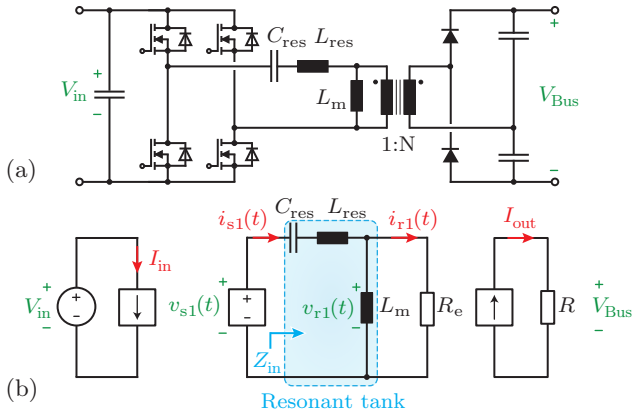

Fig. 3.21: (a) Series resonant converter topology and (b) equivalent circuit which models the fundamental frequency behavior.

switch network, thus higher harmonics can be neglected in the analysis allowing the use of the FHA method [74]. Hence, the input voltage of the resonant tank $v_{s1}(t)$ equals the first harmonic of the square wave voltage, i.e.

$$v_{s1}(t) = \frac{4V_{in}}{\pi} \sin(\omega_s t) \ , \tag{3.22}$$

where ω_s is determined by the switching frequency $\omega_s = 2\pi f_s$. The average value of the input current I_{in} can be obtained by averaging the absolute value of the current $i_{s1}(t)$, which is drawn by the resonant tank, over half a switching period. This yields

$$I_{in} = \frac{2\hat{I}_{s1}}{\pi} \cos(\phi_s) \ , \tag{3.23}$$

where $\hat{I}_{s1}$ is the amplitude of the first harmonic of the sinusoidal resonant current $i_{s1}(t)$ and ϕ_s is the phase angle with respect to the voltage $v_{s1}(t)$.

The rectifier network can also be analyzed with the FHA method if it is again assumed that the resonant tank has a negligible response to higher harmonics. Thus, the voltage $v_{r1}(t)$ (on the primary side of the transformer) is the first harmonic of the square wave voltage that

is impressed by the rectified current. This yields for a voltage doubler configuration

$$v_{\mathrm{r1}}(t) = \frac{2V_{\mathrm{Bus}}}{N\pi}\sin(\omega_{\mathrm{s}}t - \phi_{\mathrm{s}}) \ , \tag{3.24}$$

where N is the transformer turns ratio. The voltage $v_{\mathrm{r1}}(t)$ is in phase with the resonant tank output current

$$i_{\mathrm{r1}}(t) = \hat{I}_{\mathrm{r1}}\sin(\omega_{\mathrm{s}}t - \phi_{\mathrm{s}}) \ , \tag{3.25}$$

where $\hat{I}_{\mathrm{r1}}$ is the peak value of the sinusoidal current at fundamental frequency. Based on that, the value of the DC output current I_{out} can be obtained by averaging the rectified resonant tank output current $|i_{\mathrm{r1}}(t)|$ over half a switching period, which results in

$$I_{\mathrm{out}} = \frac{1}{N\pi}I_{\mathrm{r1}} \ . \tag{3.26}$$

Furthermore, the equivalent load resistance R_{eq} on the primary side of the transformer can be calculated as

$$R_{\mathrm{eq}} = \frac{v_{\mathrm{r1}}(t)}{i_{\mathrm{r1}}(t)} = R\frac{2}{N^2\pi^2} \ . \tag{3.27}$$

With the result for R_{eq}, the input impedance of the resonant tank can be derived as

$$Z_{\mathrm{in}}(s) = sL_{\mathrm{res}} + \frac{1}{sC_{\mathrm{res}}} + (R_{\mathrm{eq}}||sL_{\mathrm{m}}) \ . \tag{3.28}$$

Based on that, the voltage gain of the resonant tank can be derived as

$$G_{\mathrm{res}}(s) = \left|\frac{(R_{\mathrm{eq}}||sL_{\mathrm{m}})}{Z_{\mathrm{in}}(s)}\right| \ , \tag{3.29}$$

which varies with the switching frequency. The resonant tank exhibits two resonance frequencies given as

$$f_{\mathrm{res},1} = \frac{1}{2\pi\sqrt{L_{\mathrm{res}}C_{\mathrm{res}}}} \ , \ f_{\mathrm{res},2} = \frac{1}{2\pi\sqrt{(L_{\mathrm{res}}+L_{\mathrm{m}})C_{\mathrm{res}}}} \ , \tag{3.30}$$

and the gain of the resonant tank equals one, if operated at $f_{\mathrm{res},1}$. If it is assumed that the leakage inductance L_σ of the transformer, which usually has a value below one or two percent of the value of the magnetizing inductance L_{m}, is utilized as resonance inductance L_{res} then the

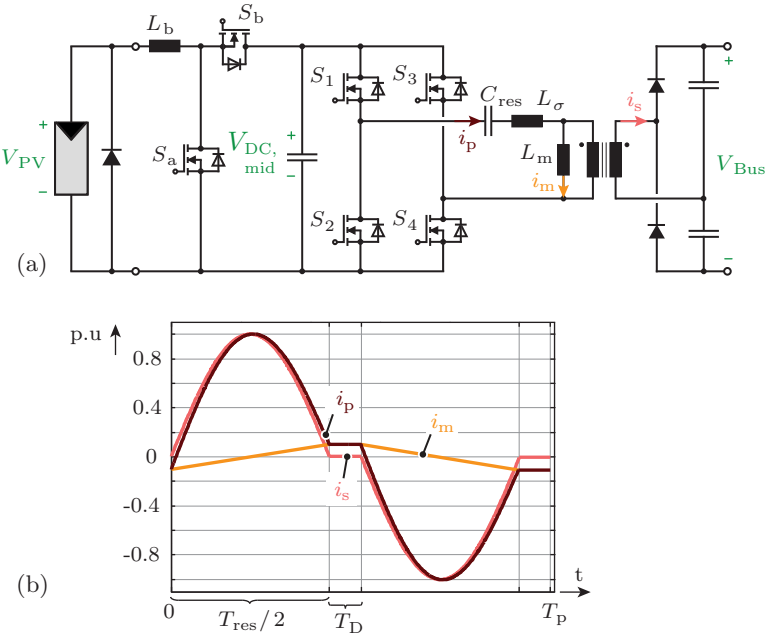

Fig. 3.22: Proposed converter topology: (a) two-stage converter consisting of a boost converter and a SRC and (b) characteristic waveforms of the SRC. The SRC is operated in the HC-DCM which utilizes the magnetizing current i_m for ZVS during dead-time T_D and features a constant voltage transfer ratio.

frequencies $f_{res,1}$ and $f_{res,2}$ differ by a factor of around ten, according to (3.30). The transfer ratio of V_{in} to V_{Bus} for $f_{sw} \neq f_{res,1}$ does not only depend on the switching frequency, but also on the power level. Thus, if one wants to cover the total PV panel voltage range ($V_{PV} = 15...45\,V$) at all power levels, the transformer design becomes challenging. To account for that, in [90] the leakage inductance was chosen to be in the same order of magnitude as the magnetizing inductance, thus requiring a transformer design with dedicated windings to achieve a high leakage inductance. If, in contrast, the magnetizing inductance is reduced, e.g. by introducing an airgap in the main magnetic path, the magnetizing current will increase and cause higher conduction losses.

From the considerations above, it can be seen that the voltage trans-

fer ratio of V_{in} to V_{Bus} is only constant, if the SRC is operated at resonance frequency $f_{\text{sw}} = f_{\text{res},1}$. At this operating point, the transfer ratio is independent of the load current. Therefore, in this thesis a two-stage topology is proposed, which consists of a boost converter and a SRC as shown in **Fig. 3.22(a)**. The boost converter steps the changing PV voltage V_{PV} to an intermediate constant voltage bus $V_{\text{DC,mid}}$. The SRC converter is operated at $f_{\text{res},1}$ in half-cycle discontinuous conduction mode (HC-DCM) [91] as shown in **Fig. 3.22(b)**. This enables a very efficient voltage conversion from the intermediate bus voltage $V_{\text{DC,mid}}$ to the high voltage bus V_{Bus} by utilizing the transformer leakage inductance as resonance inductance and the magnetizing current in combination with the parasitic output capacitances of the full-bridge MOSFETs for ZVS switching. The duration of the square wave pulses of the full-bridge are equal to the time required for the resonant current to complete one half wave, i.e. $T_{\text{res}}/2$. Between the square wave pulses a dead-time T_{D} is introduced, during which the remaining magnetizing current charges/discharges the parasitic capacitances of the MOSFETs in such way that ZVS is achieved before the full-bridge switches turn on for the next half cycle. As only the magnetizing current is used for ZVS, the SRC can operate without switching losses independent of the transferred power.

The concept of applying two converter stages simplifies the design and the control of the system. The bridge legs of the SRC are operated at a fixed switching frequency with 50% duty cycle and 180 ° phase shift. Since the output voltage V_{Bus} is controlled by the central DC/AC converter, the voltage of the intermediate DC bus $V_{\text{DC,mid}}$ is also constant. Thus, the boost stage can perform Maximum Power Point (MPP) tracking of the PV panel by proper variation of the duty cycle D_{boost} of switch S_{a}.

3.3.2 Converter Optimization

The degrees of freedom in the design of the converter (specifications in **Tab. 3.3**) are the level of the intermediate bus voltage $V_{\text{DC,mid}}$, the resonance frequency f_{res} of the SRC, and the switching frequency $f_{\text{sw,boost}}$.

Tab. 3.3: Specifications of the PV panel integrated high-step up boost converter.

Parameter	Variable	Value
Max. converter power	P_{conv}	275 W
Max. input voltage	$V_{\mathrm{PV,max}}$	45 V
Min. input voltage	$V_{\mathrm{PV,min}}$	15 V
Max. input current	$I_{\mathrm{PV,max}}$	10 A
Bus voltage	V_{Bus}	400 V
Min. ambient temperature	T_{min}	−20°C
Max. ambient temperature	T_{max}	80°C

Choice of the Value of $V_{\mathrm{DC,mid}}$

In contrast to the SRC stage operating in ZVS at all times, the boost stage creates switching losses since it operates in continuous conduction mode. The switching losses of the boost converter are influenced by the input current as well as by the voltage $V_{\mathrm{DC,mid}}$ and increases with increasing values of both. As the input current is determined by the MPP of the PV panel and thus cannot be altered, it is preferable to select a value of $V_{\mathrm{DC,mid}}$ which is as low as possible, i.e. slightly above the maximum converter input voltage to keep the duty cycle in a reasonable range with good controllability and efficiency. Based on this, an intermediate bus voltage level of $V_{\mathrm{DC,mid}} = 50\,\mathrm{V}$ is chosen. Thus, the duty cycle of the boost converter varies in the range of $D_{\mathrm{boost}} = 0.1...0.7$ for input voltages in the range of $V_{\mathrm{PV}} = 15...45\,\mathrm{V}$.

Optimization Procedure of Boost Stage

The losses of the boost stage comprise inductor losses and semiconductor switching and conduction losses. Regarding the inductor L_{b}, different values for the peak-to-peak current ripple $\Delta I_{\mathrm{L,max}} = [20\%...100\%]$ of the maximum average value of the inductor current $I_{\mathrm{in,max}}$ have been used for the following optimization. Based on that, a value of $\Delta I_{\mathrm{L,max}} = 60\%$ of $I_{\mathrm{in,max}}$ has been selected. The maximum inductor current ripple occurs for $D_{\mathrm{boost}} = 0.5$ which is given at $V_{\mathrm{PV}} = 25\,\mathrm{V}$. For the product of inductance and switching frequency this yields a value of

$$L_\mathrm{b} f_\mathrm{sw} = \frac{V_\mathrm{DC,mid}}{4\Delta I_\mathrm{L,max} I_\mathrm{in,max}} \approx 2.1\,\mathrm{H}\cdot\mathrm{Hz}\ . \tag{3.31}$$

Furthermore, the maximum flux density in the core has to be kept well below the saturation flux density, i.e.

$$B_\mathrm{sat} > B_\mathrm{max} = \frac{L_\mathrm{b}\hat{I}_\mathrm{L}}{N_\mathrm{Ind}\cdot A_\mathrm{c,min}}\ , \tag{3.32}$$

with N_ind being the number of turns, $A_\mathrm{c,min}$ the minimum core cross section and $\hat{I}_\mathrm{L}$ the peak value of the inductor current.

The inductor losses comprise core losses and winding losses. The core losses can be calculated using the improved Generalized Steinmetz Equation (iGSE), as already introduced in (3.16).

The winding losses are caused by the DC inductor current and by eddy current losses, which increase with increasing frequency. The eddy currents contribute to skin and proximity effect losses, which can be analytically approximated according to [68]. Harmonics up the 10th order are considered in the calculations.

For the boost and the synchronous rectification switch Gallium Nitrid (GaN) FETs from EPC (EPC2001) are selected, since they feature lower switching losses compared to Silicon MOSFETs at a given switching frequency. As the switching losses are strongly influenced by parasitic inductances of the circuit layout, a layout similar to the one already successfully tested in **Sec. 3.2.4** has been taken as a reference and the losses have been validated with LTSpice simulations of the manufacturer's switch models. Furthermore, the on-state resistance $R_\mathrm{DS,on}$ of the switches and the resistance of the PCB traces account for conduction losses.

Optimization Procedure of the SRC

Since the SRC is operated with ZVS, the main loss contributors are transformer losses and conduction losses in both the switches and the PCB traces.

The transformer needs to be designed for a turns ratio of $N_\mathrm{sec}/N_\mathrm{prim} = 4$ because the voltage needs to be stepped up from $V_\mathrm{DC,mid} = 50\,\mathrm{V}$ to half the value of $V_\mathrm{Bus} = 400\,\mathrm{V}$ since a voltage doubler is used for the rectification. As a first approximation, disregarding the magnetizing

current $i_{\mathrm{m}}(t)$ and the dead-time T_{D}, the peak value of the primary current $\hat{I}_{\mathrm{p}}$ can be calculated for a given PV panel power P_{PV} as

$$\hat{I}_{\mathrm{p}} = \frac{\pi \cdot P_{\mathrm{PV}}}{2 \cdot V_{\mathrm{DC,mid}}} \ . \tag{3.33}$$

and the RMS value as

$$I_{\mathrm{p,rms}} = \frac{\hat{I}_{\mathrm{p}}}{\sqrt{2}} = \frac{\sqrt{2}\pi \cdot P_{\mathrm{PV}}}{4 \cdot V_{\mathrm{DC,mid}}} \ . \tag{3.34}$$

As the current exhibits a sinusoidal waveform, the winding losses can be calculated by using only the fundamental frequency for the calculation of the AC resistance of the windings, taking proximity and skin effect into account.

The core losses can be assessed with the iGSE by first considering the flux linkage Ψ_{p} in the transformer, which exhibits in a first approximation (i.e. neglecting the dead time T_{D}) a triangular waveform with a peak value of $\hat{\Psi}_{\mathrm{p}}$ on the primary side, i.e.

$$\hat{\Psi}_{\mathrm{p}} = \frac{V_{\mathrm{DC,mid}}}{4 \cdot f_{\mathrm{sw}}} \ . \tag{3.35}$$

Depending on the flux linkage, the flux density in the core can be calculated as

$$B = \frac{\Psi_{\mathrm{p}}}{N_{\mathrm{p}} \cdot A_{\mathrm{c,min}}} \ , \tag{3.36}$$

with a peak value that has to be well below the saturation flux density

$$B_{\mathrm{sat}} > B_{\mathrm{max}} = \frac{\hat{\Psi}_{\mathrm{p}}}{N_{\mathrm{p}} \cdot A_{\mathrm{c,min}}} \ . \tag{3.37}$$

For the switches of full-bridge stage also GaN FETs from EPC (EPC2001) are selected due to a lower parasitic capacitance $C_{\mathrm{oss}}(V_{\mathrm{DS}})$ compared to Si MOSFETs with similar voltage rating and on-state resistance $R_{\mathrm{DS,on}}$. This allows to minimize the dead-time T_{D} which is required to charge/discharge the capacitances $C_{\mathrm{OSS}}(V_{\mathrm{DS}})$ of all switches.

Optimization Results

For different core types (ETD and EFD cores) made of N87 Siferrite material and a selection of Rupalit litz wires the inductor and transformer

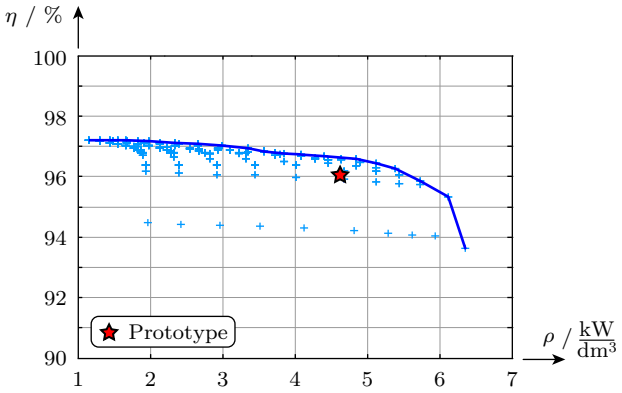

Fig. 3.23: Optimization results for an operating point of $P_{\mathrm{PV}} = 250\,\mathrm{W}$ and $V_{\mathrm{PV}} = 30\,\mathrm{V}$ visualized as efficiency/power density (η-ρ) Pareto plot. Each marker represents one combination of an inductor core size and transformer core size.

losses have been calculated for an operating point of $P_{\mathrm{PV}} = 250\,\mathrm{W}$ and $V_{\mathrm{PV}} = 30\,\mathrm{V}$ for different switching frequencies of the boost stage and different resonance frequencies of the SRC stage. Since several combinations of inductor and transformer designs exist, an efficiency/power density (η-ρ) Pareto plot (**Fig. 3.23**) is created, which visualizes the achievable trade-off between the converter efficiency and volume for all possible combinations at the selected operating point. For calculating the total converter volume, boxed volumes of the main components, i.e. the inductor, the transformer and PCB have been considered.

3.3.3 Prototype and Experimental Results

Based on the optimization results, a converter prototype has been assembled, shown in **Fig. 3.24(a)**. The switching frequency of the boost stage is set to an optimized value of $f_{\mathrm{sw,boost}} = 210\,\mathrm{kHz}$ and the inductor consists of an EFD25 core with an inductance of $L_{\mathrm{b}} \approx 10\,\mu\mathrm{H}$ i.e. $N = 7$ turns (420 strands with 71 µm diameter) and an air gap of $l_{\mathrm{gap}} = 0.76\,\mathrm{mm}$.

The transformer of the SRC is composed of an ETD34 core with $N_{\mathrm{p}} = 9$ primary turns (420 strands with 71 µm diameter) and $N_{\mathrm{s}} = 36$ secondary turns (120 strands with 71 µm diameter) and is operated at a

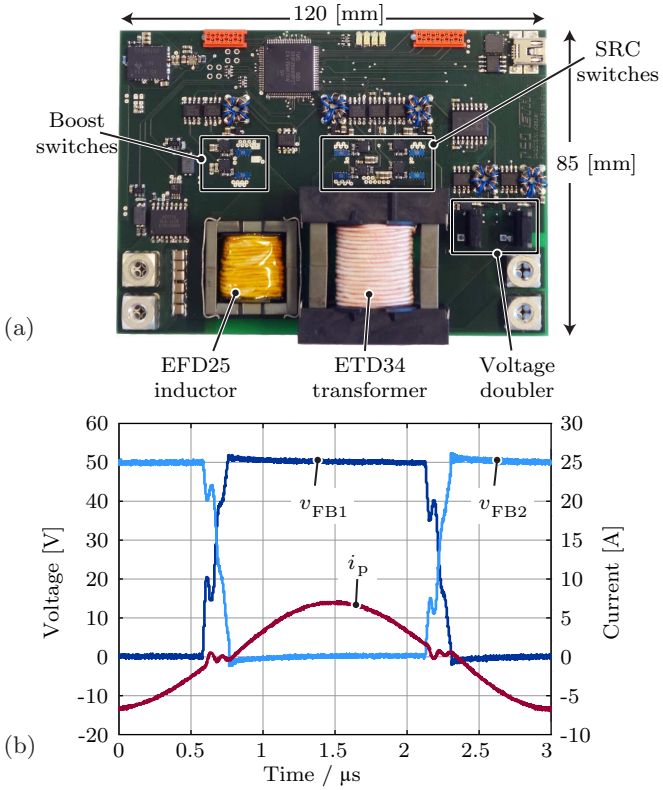

Fig. 3.24: (a) Prototype of the high step-up boost converter comprising a boost stage, an isolated SRC stage and a voltage doubler rectifier. (b) Measured waveforms of the converter prototype showing the output voltage of both bridge-legs (v_{FB1} and v_{FB2}) of the full-bridge and the transformer current i_p on the primary side at an operating point of $P_{PV} = 200\,W$, $V_{DC,mid} = 50\,V$ and $V_{Bus} = 400\,V$.

resonance frequency of $f_{res} = 350\,kHz$. In order to limit the influence of the dead time T_D on the RMS value of the transformer current, its value is limited to 10% of the resonance period. This requires a magnetizing inductance of $L_m \approx 60\,\mu H$ and thus a total air gap of $l_{gap} = 0.1\,mm$ in the transformer core. With a leakage inductance of $L_\sigma \approx 380\,nH$ the resonance capacitance has to be $C_m \approx 484\,nF$ in order to tune the resonance circuit to the desired resonance frequency.

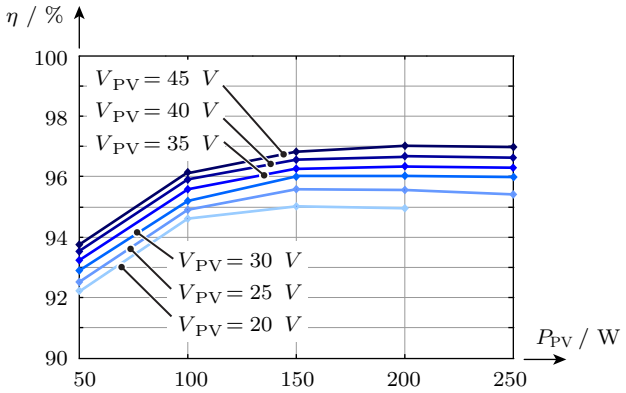

Fig. 3.25: Measured efficiency of the prototype for different levels of input voltage V_{PV} and different levels of converter input power P_{PV}.

The voltage doubler rectifier circuit consists of SiC diodes from Cree (C3D02060E).

The measurement results shown in **Fig. 3.24** verify the operation of the SRC in HC-DCM. After each resonant half-wave of the primary current i_p, the magnetizing current charges/discharges the parasitic capacitances of the GaN FETs in the full-bridge as can be seen with the bridge-leg voltages v_{FB1} and v_{FB2}. Thus, no switching losses are generated in the full-bridge switches of the SRC.

The converter efficiency has been measured for different input voltages V_{PV} at different levels of input power P_{PV} and the results are visualized in **Fig. 3.25(b)**. The converter efficiency increases with increasing input voltage V_{PV} as the conduction and switching losses of the boost stage decrease with decreasing input current i.e. increasing input voltage at a given power level. A peak efficiency of around 97% is achieved at the operating point with an input voltage of $V_{PV} = 45\,\text{V}$ and an input power of $P_{PV} = 200\,\text{W}$.

3.3.4 Improving Part-Load Efficiency

For operation of the SRC in HC-DCM, the magnetizing flux causes core losses independent of the transferred power. At low levels of the input power P_{PV}, these constant losses constitute a relatively large part of the total losses since other loss contributions, such as e.g. conduction

losses and switching losses of the boost stage, decrease with decreasing input power. Hence, in order to improve the part-load efficiency of the converter, the modulation scheme of the SRC can be slightly changed as shown in **Fig. 3.26** by introducing a free-wheeling state for the magnetizing current during time T_{FW}. This half-cycle skipping (HCS) mode reduces the frequency at which resonant half wave pulses are processed by the SRC and thus also the frequency at which the magnetizing flux changes, which results in lower core losses. This principle of operation is comparable to the line cycle skipping (LCS) method of PFC boost converters, which achieves an almost flat efficiency curve over the transferred power [92]. One disadvantage, however, are increased peak and RMS values of the resonant current, giving rise to higher winding losses in the transformer. Thus, an optimal free-wheeling time T_{FW} can be found for each power level with the lowest converter losses.

The efficiency measurement results for the prototype at low power operation at an input voltage of $V_{\mathrm{PV}} = 35\,\mathrm{V}$ are shown in **Fig. 3.27** for the case of HCS operation in comparison to normal HC-DCM operation.

3.3.5 Summary

The two-stage converter concept employing a boost stage and a series resonant converter (SRC) stage is identified as the best suited concept

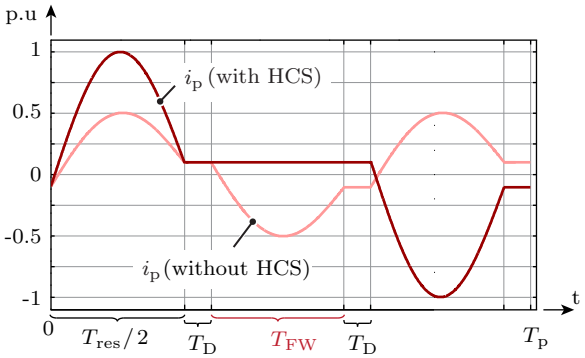

Fig. 3.26: Operating principle of the half-cycle skipping (HCS) mode. In comparison to the normal HC-DCM operation, a free-wheeling state for the magnetizing current during time T_{FW} is introduced.

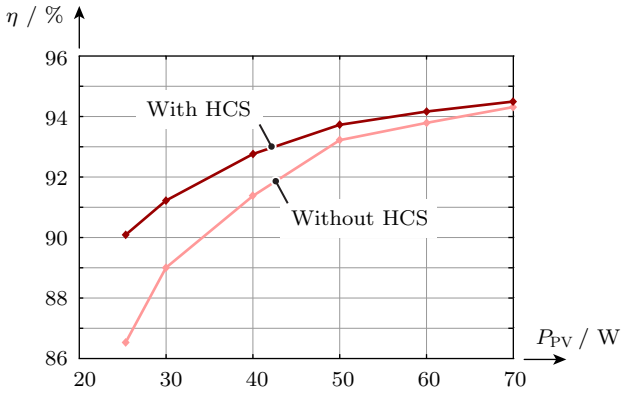

Fig. 3.27: Comparison between the measured efficiency of the prototype in half-cycle skipping (HCS) mode and in normal HC-DCM for an input voltage of $V_{\mathrm{PV}} = 35\,\mathrm{V}$ at low levels of converter input power P_{PV}.

for the class of parallel-connected full-power PV module integrated converters. The boost stage is required for the adaption of the temperature dependent PV panel output voltage of $V_{\mathrm{PV}} = 15...45\,\mathrm{V}$ to an intermediate constant bus voltage of $V_{\mathrm{DC,mid}} = 50\,\mathrm{V}$ and for tracking the MPP of the PV panel. The high step-up conversion to a converter output voltage of $V_{\mathrm{Bus}} = 400\,\mathrm{V}$ is accomplished by the second isolated stage i.e. the SRC operated in HC-DCM, where the magnetizing current of the transformer is utilized to achieve soft-switching. Based on the results of an efficiency/power density (η-ρ) Pareto optimization, a prototype has been assembled employing only wide band-gap semiconductor devices such as GaN FET switches and SiC diodes. Measurement results verify the operation of the SRC in HC-DCM and also show that a peak converter efficiency slightly above 97% could be achieved at a power level of $P_{\mathrm{PV}} = 200\,\mathrm{W}$ and an input voltage of $V_{\mathrm{PV}} = 35\,\mathrm{V}$. The efficiency at part load operation can be improved by operating the SRC in half-cycle skipping (HCS) mode which reduces the core losses of the transformer at the expense of slightly higher conduction losses.

3.4 Parallel-Connected Partial-Power MIC

The concept of the parallel connected partial-power converter (P-PPC) for PV panels has been the focus of several research papers [54, 93–102]. Even though the PV panels are still connected in series, the voltages of the panels are equalized by the P-PPCs and therefore act like a "virtual parallel" connection. Many of these topologies have been known for more than two decades from battery equalization circuits, where the state of charge of series connected battery cells is equalized in order to prevent unequal aging of the batteries [93, 94]. However, this "virtual

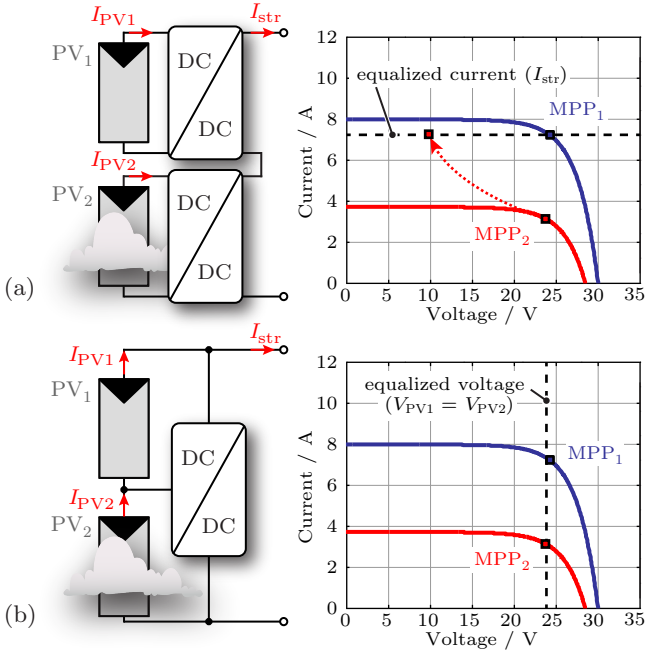

Fig. 3.28: Comparison of different PV panel-integrated DC/DC converter concepts for a simplified system with two PV panels receiving different levels of irradiance: (a) the series-connected full-power converter concept adjusts the maximum power points MPP_1 and MPP_2 of the PV panels to a common string current I_{str}; (b) the parallel-connected partial-power concept equalizes all PV panel voltages such that the panel voltages are equal or close to the MPP voltages.

parallel" connection of battery cells cannot only be used for battery systems but can also be applied to PV panels [54, 96, 97] or on substring level to strings of PV cells within a PV panel. [98–102].

In contrast to the cited literature references, which are mainly focusing either on the theoretical analysis of different balancing topologies or on advanced control schemes, this thesis provides an analytical background of both the operation of the proposed converter concept and the operation of the whole PV system. A novel contribution is hereby the analysis of the impact of different shading scenarios of a PV string on the operating points of the balancing converters. Furthermore, a two-level overcurrent protection concept is introduced and the adjustment of the operating points of each balancing converter of a PV string installation is explained if an overcurrent exceeds the safe operating limits. This constitutes the basis for a converter optimization which is used for designing a set of converter prototypes which are finally tested in string operation with different shading scenarios.

3.4.1 Operating Principle

In order to extract the maximum amount of power from a string of PV panels, each PV panel has to be operated at its maximum power point (MPP). On the one hand, this can be achieved with full-power DC/DC converters on each PV panel that adjust the PV panel current I_{PV} to the string current I_{str}, as shown for the series connected full-power converter in **Fig. 3.28(a)** (cf. **Sec. 3.2**). On the other hand, instead of adjusting all PV panels to the same current, they can also be operated with the same panel voltage by means of partial-power balancing and/or panel voltage equalization converters, since the voltage of the MPP of a panel is barely affected by the level of received irradiance, as visualized in **Fig. 3.28(b)**. In contrast to full-power converters, however, the partial-power balancing converters cannot track the MPPs of the PV panels; the overall MPP tracking of the whole string in this case is performed by the central inverter. Furthermore, due to the series connection of the PV panels in the balancing converter concept, the voltage of the string is given by the addition of the individual PV panel voltages. Thus, paralleling multiple strings is only feasible if all strings contain the same number of PV panels of the same type which have equal temperatures. Those limitations regarding the flexibility of the system design, however, are in many cases outweighed by a lower complexity

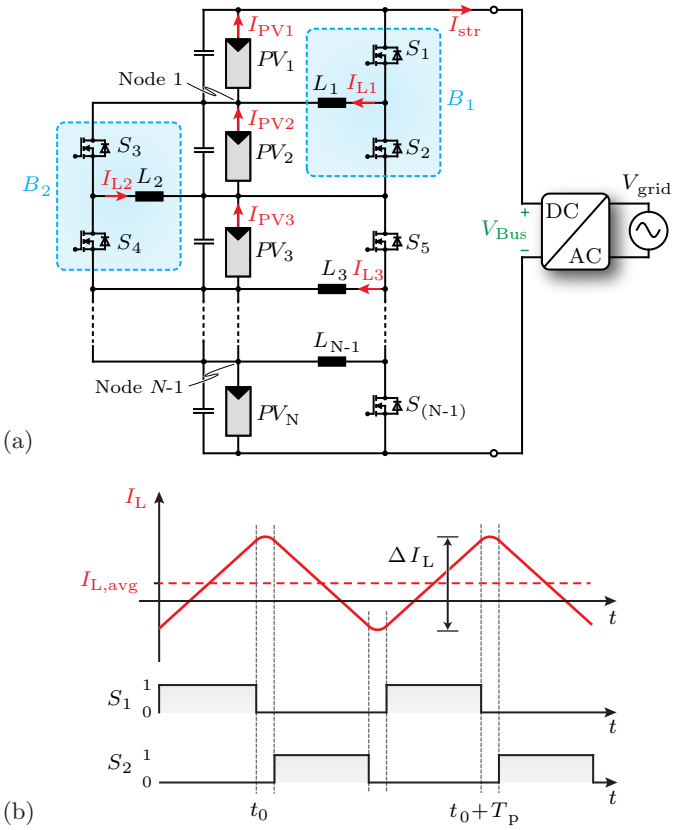

Fig. 3.29: Analyzed PV system with balancing circuits: (a) circuit diagram showing a PV string with N PV panels (PV_1,...,PV_N), $N-1$ balancing converters (B_1,...,$B_{(N-1)}$) and a grid connected DC/AC converter and (b) characteristic inductor current waveform and gate signals of one balancing converter.

in the control, lower component count, and higher efficiency of the balancing converters, since they convert only a small part of the panel power, defined by the differences of the actual PV panel current values.

The balancing converters denoted as B_1, B_2 in **Fig. 3.29(a)**, are inverting buck-boost DC/DC converters, each connected around two adjacent PV panels. This means that a PV string consisting of N PV

panels requires $(N-1)$ balancing converters, i.e. $(2 \cdot (N-1))$ switches and $(N-1)$ inductive components in total.

The balancing converters do not require any closed loop control since the switches of each buck-boost converter can be controlled by a simple PWM signal with a fixed duty cycle of 50% in case of normal operation without over-current. Furthermore, the balancing converters operate independent of each other and neither require any communication or synchronization with neighboring converters nor with the central inverter.

The waveforms of the gate signals and the inductor current are shown in **Fig. 3.29(b)** for one balancing converter. The triangular current of the inductor can be utilized in combination with the parasitic drain-source capacitances of the MOSFETs to achieve zero-voltage switching (ZVS) (cf. **Appendix C**), as the current direction reverses during each conduction interval. In order to maintain ZVS operation over the whole PV panel voltage range, the switching frequency is linearly adjusted with the PV panel voltage by means of a voltage controlled oscillator (VCO). This results in a constant peak-to-peak current ripple ΔI_{L} of the inductor current I_{L}.

Panel-Level vs. Sub-String Level Equalization

In recent publications, a voltage equalization on sub-string level of the PV panels has been proposed [98–102]. This is motivated by the fact, that a PV panel usually consists of two or three strings of series connected PV cells, so-called sub-strings. They are equipped with bypass diodes, as depicted in **Fig. 3.30(a)** for a PV panel with two sub-strings. Thus, if equalization modules are connected around the sub-strings, each sub-string can be operated at its MPP. In contrast, the equalization on PV panel level only regulates the terminal voltage V_{PV} of the PV panel and not the voltages of the sub-strings. The current through the sub-strings is equal to the PV panel current which is drawn from the terminals of the PV panel. The whole system, consisting of the PV panels with balancing converters and the central DC/AC converter, is driven by the MPP tracker of the central DC/AC converter to strive for maximum output power. Thus, the currents within the PV panels will adjust to the value that still yields the required PV panel voltage, which is the voltage applied to the PV panel by the balancing converters.

As a result, in a partially shaded PV panel, the output power of the unshaded sub-strings will be below their MPP, since the shaded

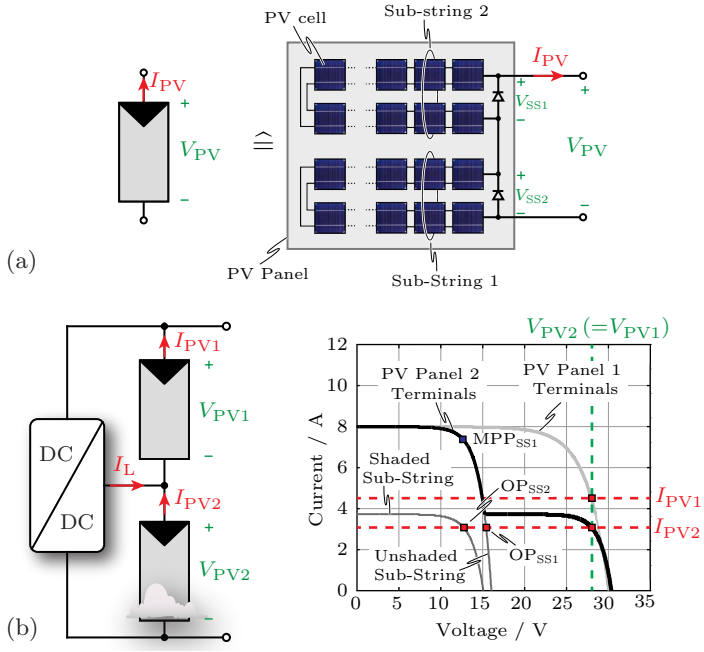

Fig. 3.30: Issue of partial shading of a PV panel: (a) structure of a standard crystalline Si PV panel with two internal strings (i.e. sub-strings) of PV cells with bypass diodes; (b) simplified system with a voltage balancer around an unshaded PV panel (PV panel 1) and a partially shaded PV panel (PV panel 2) and the corresponding current/voltage diagram of the partially shaded PV panel with the operating points of the unshaded and shaded sub-string, OP_{SS1} and OP_{SS2}, respectively.

sub-string dictates the current level. This is visualized in **Fig. 3.30(b)** for a PV string with two PV panels and one balancing converter, where the upper panel is unshaded and the lower panel is partially shaded. The panel voltage V_{PV2} is equal to the voltage of the upper PV panel V_{PV1} as a result of the equalization process. The current I_{PV2} of the partially shaded panel is therefore given by the intersection of the PV panel terminal characteristics and the impressed voltage V_{PV2} and is conducted by both sub-strings.

In practice, however, only few PV panels, namely these at the border of shaded and unshaded areas, will be partially shaded. Thus, the

benefit of sub-string level equalization circuits compared to panel level balancing converters is in most cases outweighed by higher system costs resulting from the increased part count.

3.4.2 Analytical Description

In this section, the operation of a PV string with balancing converters is analytically described in order to determine the influence of different shading conditions on the operation of the converters. In case of any mismatch between the PV panels within a string, the currents in the inductors of the balancing converters exhibit DC values $I_{\mathrm{L1}}, ..., I_{\mathrm{L(N\text{-}1)}}$ (cf. **Fig. 3.29(a)**). The values of these DC currents can be calculated depending on the values of the PV panel currents $(I_{\mathrm{PV1}}, ..., I_{\mathrm{PV(N)}})$, i.e. preferably the MPP currents of the PV panels, as long as a duty cycle of 50% is maintained and also by taking into consideration that no DC current can flow through the capacitors. The current direction is inherited from **Fig. 3.29(a)** and, based on Kirchoff's current law, the equations for the $(N-1)$ nodes between each pair of adjacent PV panels can be written as

$$\begin{aligned}
&\text{Node 1:} && I_{\mathrm{PV2}} - I_{\mathrm{PV1}} + I_{\mathrm{L1}} - \frac{1}{2}\cdot I_{\mathrm{L2}} = 0 \\
&\text{Node 2:} && I_{\mathrm{PV3}} - I_{\mathrm{PV2}} + I_{\mathrm{L2}} - \frac{1}{2}\cdot I_{\mathrm{L1}} - \frac{1}{2}\cdot I_{\mathrm{L3}} = 0 \\
& && \vdots \\
&\text{Node N-2:} && I_{\mathrm{PV(N\text{-}1)}} - I_{\mathrm{PV(N\text{-}2)}} + I_{\mathrm{L(N\text{-}2)}} - \frac{1}{2}\cdot I_{\mathrm{L(N)}} - \frac{1}{2}\cdot I_{\mathrm{L(N\text{-}3)}} = 0 \\
&\text{Node N-1:} && I_{\mathrm{PV(N)}} - I_{\mathrm{PV(N\text{-}1)}} + I_{\mathrm{L(N\text{-}1)}} - \frac{1}{2}\cdot I_{\mathrm{L(N\text{-}2)}} = 0 \ .
\end{aligned} \tag{3.38}$$

This can also be expressed in matrix form as

$$\begin{bmatrix} 1 & -\frac{1}{2} & 0 & & \cdots & 0 & 0 \\ -\frac{1}{2} & 1 & -\frac{1}{2} & 0 & & & 0 \\ 0 & -\frac{1}{2} & 1 & -\frac{1}{2} & 0 & & \vdots \\ & \ddots & \ddots & \ddots & \ddots & \ddots & \\ \vdots & & 0 & -\frac{1}{2} & 1 & -\frac{1}{2} & 0 \\ 0 & & & 0 & -\frac{1}{2} & 1 & -\frac{1}{2} \\ 0 & 0 & \cdots & & 0 & -\frac{1}{2} & 1 \end{bmatrix} \times \begin{bmatrix} I_{\mathrm{L1}} \\ I_{\mathrm{L2}} \\ I_{\mathrm{L3}} \\ \vdots \\ I_{\mathrm{L(N\text{-}1)}} \end{bmatrix}$$

$$= \begin{bmatrix} I_{\mathrm{PV2}} - I_{\mathrm{PV1}} \\ I_{\mathrm{PV3}} - I_{\mathrm{PV2}} \\ I_{\mathrm{PV4}} - I_{\mathrm{PV3}} \\ \vdots \\ I_{\mathrm{PV(N)}} - I_{\mathrm{PV(N\text{-}1)}} \end{bmatrix} \tag{3.39}$$

By applying mathematical reformulation, the average inductor current $I_{\mathrm{L,n}}$ of one balancing converter can be expressed in a summation of the PV panel currents as

$$I_{\mathrm{L,n}} = 2 \cdot \left(\sum_{i=1}^{n} \frac{N-n}{N} \cdot I_{\mathrm{PV,i}} - \sum_{i=n+1}^{N} \frac{n}{N} \cdot I_{\mathrm{PV,i}} \right) . \tag{3.40}$$

The DC string current I_{str}, that is drawn by the central inverter, can be calculated as

$$I_{\mathrm{str}} = \frac{\sum_{i=1}^{N} I_{\mathrm{PV,i}}}{N} . \tag{3.41}$$

Based on the DC string current I_{str}, the DC currents in the inductors (cf. (3.40)) can be expressed by a simple equation in only one summation as

$$I_{\mathrm{L,n}} = 2 \cdot \left(\sum_{i=1}^{n} \Delta I_{\mathrm{i}} \right) \tag{3.42}$$

where $\Delta I_{\mathrm{i}} = I_{\mathrm{PV,i}} - I_{\mathrm{str}}$ is the difference between the PV panel current and the string current.

Based on (3.40) or (3.42), the average value of the inductor current in each balancing module can be calculated for different shading scenarios. In **Fig. 3.31** two shading scenarios are depicted for a string with 10 PV

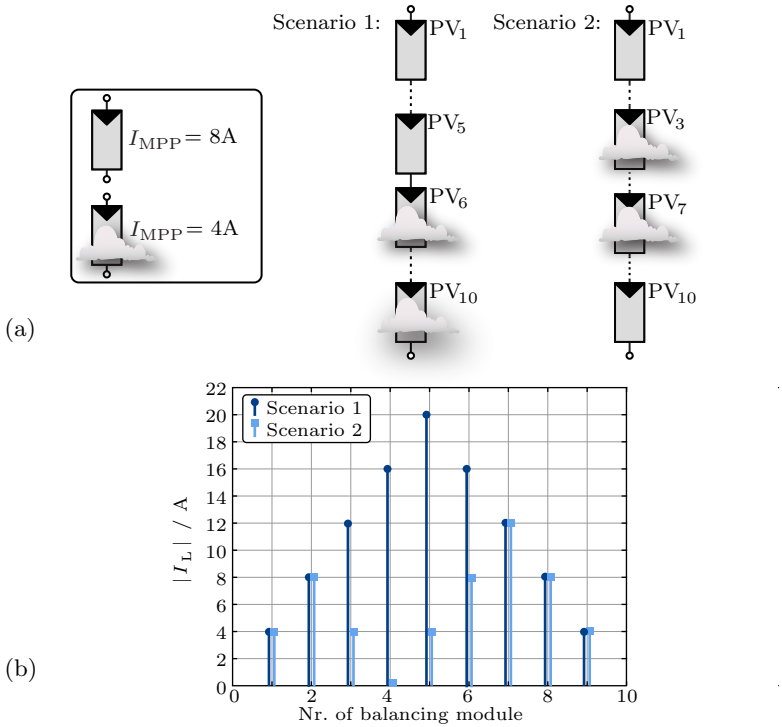

Fig. 3.31: Impact of different shading scenarios on average current values of inductors in balancing converters: (a) PV string with $N = 10$ PV panels and two different shading scenarios. In both scenarios the same number of panels are shaded, but the shaded panels are located at different positions within the PV string: In scenario 1 the shaded panels are placed at the bottom of the string, whereas in scenario 2 the shaded panels are placed at the center of the string. (b) Average inductor current values I_{L} of balancing modules for both scenarios.

panels and 9 balancing modules. In both scenarios, the same numbers of shaded and unshaded panels is assumed (i.e. 4 shaded and 6 unshaded panels). Furthermore, it is assumed that all panels are operated at their MPP where the unshaded panels deliver $I_{\mathrm{MPP,unsh}} = 8\,\mathrm{A}$ and the shaded panels provide $I_{\mathrm{MPP,sh}} = 4\,\mathrm{A}$. In scenario 1, the shaded panels are placed at the end of the string, whereas in scenario 2 the shaded panels are located at the center of the string. The resulting average inductor

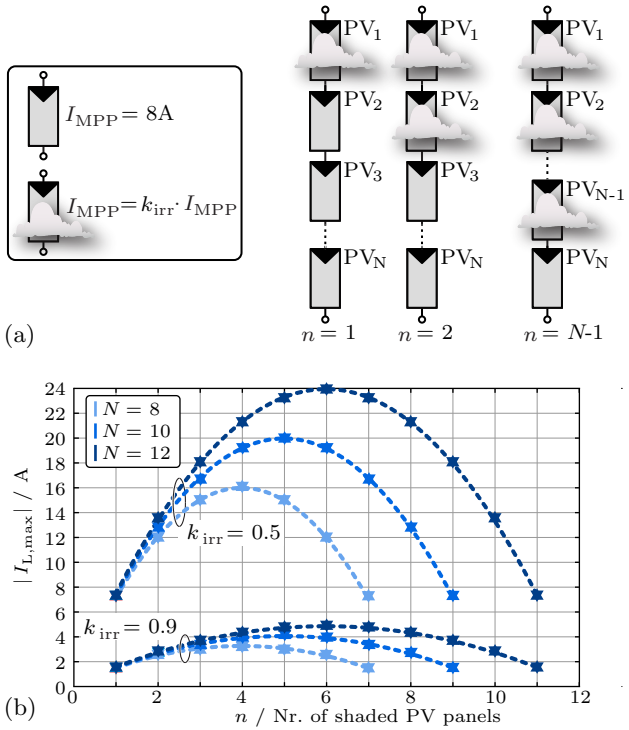

Fig. 3.32: The maximum worst-case DC inductor current that occurs in the balancing converter with an adjacent shaded and unshaded PV panel for shading scenarios, where the string is divided into a shaded and an unshaded section. The DC inductor current of this balancing module increases when 1) the string gets longer, 2) the amount of shaded and unshaded PV panels is balanced, and 3) the ratio of irradiance k_{irr} decreases.

current values in each balancing module are visualized for both scenarios in **Fig. 3.31(b)**. The largest average value that appears in scenario 1 amounts to $I_{L,max} = 20\,A$, whereas the largest value in scenario 2 is only $I_{L,max} = 12\,A$ and thus only 60% of the value of scenario 1. This aspect has not been discussed in the literature so far and constitutes an important point in the course of the converter design and selection of a proper protection concept in order to prevent overloading of balancing converters in a PV system in certain shading situations.

The most critical operation in matters of shading situations of a PV panel string is a two-part distribution of the shaded and the unshaded PV panels, given that there is then just one balancing module in the total string with an adjacent shaded and unshaded PV panel. Then, the DC inductor current of this balancing module carries the maximum DC inductor current. For an analytical derivation of the maximum DC value of the inductor current the DC string current I_{str} is expressed depending on the amount of shaded PV panels n, a ratio of irradiance k_{irr}, and the PV panel current I_{PV} of unshaded panels in their MPP

$$I_{\mathrm{str}} = \frac{I_{\mathrm{PV}} \cdot (N - n) + k_{\mathrm{irr}} \cdot I_{\mathrm{PV}} \cdot n}{N} \ . \tag{3.43}$$

Inserting (3.43) in (3.42) and differentiating with respect to n yields a maximum DC inductor current at $n = \frac{N}{2}$ which equals

$$I_{\mathrm{L,max}}\Big|_{n=\frac{N}{2}} = \frac{1}{2} \cdot (1 - k_{\mathrm{irr}}) \cdot N \cdot I_{\mathrm{PV}} \ . \tag{3.44}$$

Based on (3.42) the maximum DC inductor currents for n shaded PV panels are illustrated in **Fig. 3.32** where the combination of $k_{\mathrm{irr}} = 0.5$, $N = 10$ and $n = 5$ corresponds to scenario 1 of **Fig. 3.31**.

The DC current of an inductor also influences the RMS current values in the switches of a balancing module and thus the conduction losses. The RMS current value of a switch can be expressed as a function of the peak-to-peak inductor current ripple ΔI_{L} and of the average inductor current I_{L}, by

$$I_{\mathrm{sw,rms}} = \frac{1}{2}\sqrt{2 \cdot I_{\mathrm{L}}^2 + \frac{1}{6}\Delta I_{\mathrm{L}}^2} \ . \tag{3.45}$$

Furthermore, the efficiency of a PV system with N PV panels and $N - 1$ balancing converters can be calculated by taking into account the power generated by the PV panels $(P_{\mathrm{PV,1}}, ..., P_{\mathrm{PV,N}})$ and the losses in the balancing converters $(P_{\mathrm{Loss,1}}, ..., P_{\mathrm{Loss,N\text{-}1}})$, which results in

$$\eta_{\mathrm{Sys}} = \frac{\sum_{i=1}^{N} P_{\mathrm{PV,i}} - \sum_{i=1}^{N-1} P_{\mathrm{Loss,i}}}{\sum_{i=1}^{N} P_{\mathrm{PV,i}}} \ . \tag{3.46}$$

3.4.3 Over-Current Protection

The currents in the balancing modules might exceed the limit of the safe operating area as a result of unfavorable shading scenarios, meaning the balancing module drops out of ZVS due to a large DC current. The large DC current might furthermore lead to either the saturation of the inductor and/or to the thermal destruction of the MOSFETs caused by the switching losses. Therefore, a two-level protection concept is used in order to counteract high DC inductor current values and guarantee safe operation. In a first step, the balancing module is kept in the safe operating area by adjusting the duty cycle within the balancing module. In a second step, in case a situation with either very fast changes of the operating points of the PV panels occurs or when the irradiance levels of the PV panels are severely different, the balancing module is bypassed by turning off the MOSFETs. The protection methods are described in more detail in the following paragraphs.

The balancing module loses ZVS when the DC value of the inductor current exceeds half of the peak-to-peak inductor current ΔI_{L}. Thus, the duty cycle adjustment is initiated as soon as the measured DC value of the inductor current exceeds a predefined value. The direction of the duty cycle adjustment is given by the sign of the DC current. The duty cycle is changed until the DC current is below the limit. This allows to operate the PV panels in operating points with different voltages and therefore smaller differences in the PV currents, as shown in **Fig. 3.33**. As a drawback of this protection measure, however, the PV panels are moved out of their MPP and operate at a sub-optimal operating point. Since the shading situation might change over time, the controller is constantly trying to bring back the duty cycle ratio to the initial value of 50 %.

In case the duty cycle modification cannot provide safe operation and the DC inductor current exceeds a defined limit, the second level of the protection concept is activated and the balancing module is turned off. By turning off a balancing module, the string of PV panels is divided into two parts that are independently balanced by the remaining converters. Thus, the string contains two MPPs and the central inverter tracks the MPP with the highest power. A restart of the turned-off balancing module can be attempted once the voltages of the adjacent panels are in close vicinity.

A more detailed analysis of the output power of a PV string with power limited balancing converters is provided in **Appendix B**.

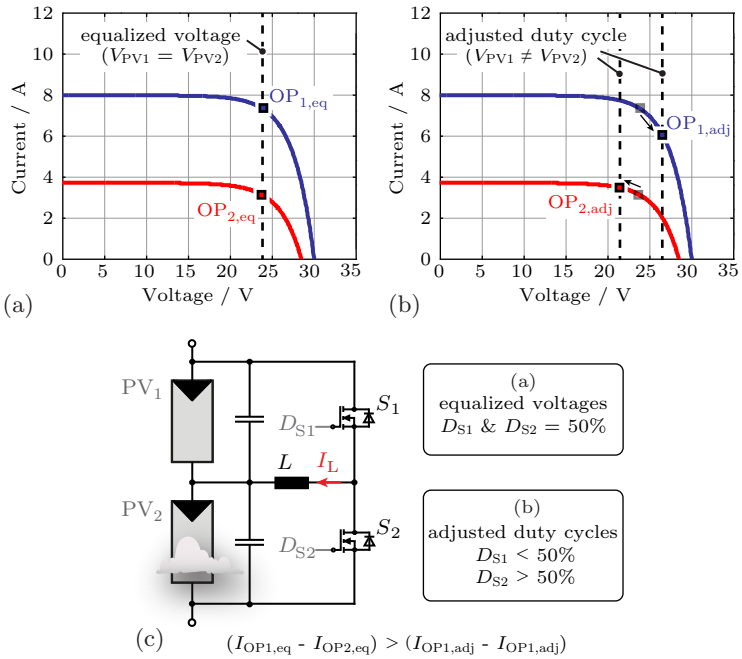

Fig. 3.33: Operating points of (a) two PV panels with equalized voltages and (b) unequalized voltages due to duty cycle adjustment. The duty cycle adjustment keeps the balancing converter in the safe operating area with ZVS since the DC inductor current I_L is decreased by the adjustment.

3.4.4 Balancing Converter Optimization and Realization

In this section the optimization procedure and design of the balancing converter prototype are explained. The balancing converter specifications do not only depend on the electrical characteristics of the PV panels but also on the expected shading scenarios, i.e. the difference between the generated panel currents within a string. Since worst case scenarios can result in high average inductor current values, as described and depicted in **Sec. 3.4.2**, the design of the converter has to be limited to reasonable shading scenarios. With larger values of the maximum average inductor current, the balancing converter can work in a wider range of shading conditions without reaching the limits at which the

protection circuits are activated. This, however, leads to larger constant losses due to the larger peak-to-peak current ripple in the inductor and larger RMS current values in the MOSFETs. Thus, as a result of this trade-off, the maximum average inductor current up to which the switches can operate in ZVS is set to $I_{\mathrm{L,max}} = 5\,\mathrm{A}$ for the prototype. In order to achieve ZVS, the amplitude of the peak-to-peak inductor current ripple ΔI_{L} has to be twice the maximum average inductor current $I_{\mathrm{L,max}}$, i.e. $\Delta I_{\mathrm{L}} = 10\,\mathrm{A}$. The switching frequency is linearly adjusted to the PV panel voltage by a voltage controlled oscillator (VCO) that senses the voltage across both PV panels. This yields constant volt-seconds $\lambda_{\mathrm{L}} = V_{\mathrm{PV}}/(2 \cdot f_{\mathrm{sw}})$ which are applied across the main inductor of a balancing module during a switching state and thus, also yields a constant inductor current ripple ΔI_{L} for all PV panel voltages. Hence,

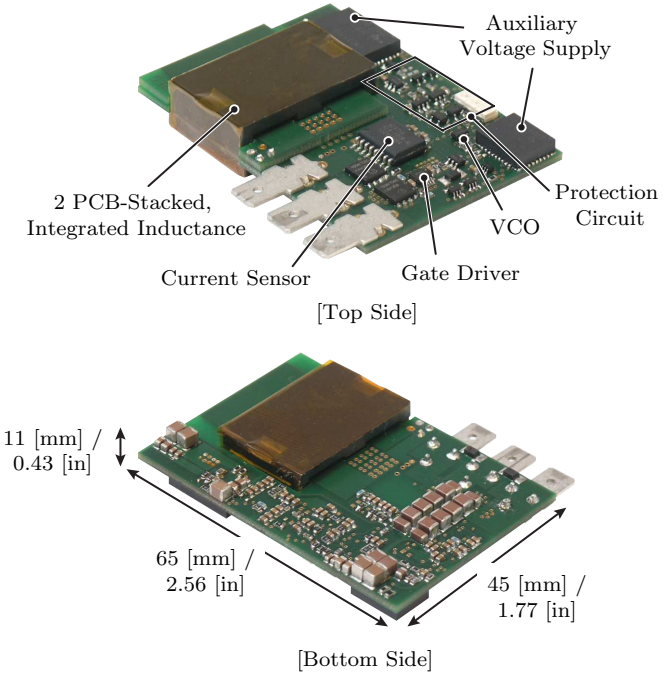

Fig. 3.34: Dimensions and components of the voltage balancing converter prototype for PV panel voltages of $V_{\mathrm{PV}} = 15\,\mathrm{V}...45\,\mathrm{V}$.

Tab. 3.4: List of main components per balancing converter.

Component	**Specifications**
2x MOSFETs	BSC190N15NS3 / Infineon [$R_{\mathrm{DS,on}} = 19\,\mathrm{m\Omega}$ @ $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$, $V_{\mathrm{DS}} = 150\,\mathrm{V}$, $I_{\mathrm{D}} = 50\,\mathrm{A}$]
1x Gate driver	Half-bridge gate driver LM5106 / TI
1x PCB integrated inductor	ELP32/6/20, N87 ferrite / EPCOS [$L \approx 9.5\,\mu\mathrm{H}$, 6 turns, 2 stacked 4-layer PCBs, track width $t_{\mathrm{w}} \approx 7\,\mathrm{mm}$, copper thickness $t_{\mathrm{h}} = 35\,\mu\mathrm{m}$, $l_{\mathrm{airgap}} = 0.37\,\mathrm{mm}$]
1x VCO	LTC6992-2 / Linear Technology
2x Auxiliary supply	LMZ35003 & LMZ31503 / TI
2x Capacitors	X7R ceramic capacitors [$C = 10.8\,\mu\mathrm{F}$ (4x2.2 µF and 2x1.0 µF), $V_{\mathrm{rated}} = 100\,\mathrm{V}$]

the inductance of the main inductor can be calculated as $L = \lambda_{\mathrm{L}}/\Delta I_{\mathrm{L}}$.

The PV panel voltage is strongly influenced by the PV panel temperature, thus the converter has to be designed for a wide input voltage range, i.e. $V_{\mathrm{PV}} = 15\,\mathrm{V}...45\,\mathrm{V}$ (cf. **Fig. 3.7**) covering a factor of $k = V_{\mathrm{PV,max}}/V_{\mathrm{PV,min}} = 3$. The switching frequency has to be varied with the same factor between maximum and minimum switching frequency. Since half-bridge gate drivers usually have a fixed dead-time (often in the range of $T_{\mathrm{dead}} \approx 100 - 200\,\mathrm{ns}$), the maximum switching frequency is chosen to be $f_{\mathrm{max}} = 250\,\mathrm{kHz}$, so that the total dead-time is less than 10% of the total switching period. As a result, the prototype operates with a switching frequency in the range of $f_{\mathrm{sw}} = 80\,\mathrm{kHz}...250\,\mathrm{kHz}$ which translates into $\lambda_{\mathrm{L}} = 100\,\mu\mathrm{Vs}$ and a required inductance of $L = 10\,\mu\mathrm{H}$.

In order to achieve a compact converter layout with minimal height to facilitate the integration into the junction box of a PV panel, a PCB integrated inductor design has been chosen. Thus, for the optimization of the inductor, all available EPCOS N87 cores with ELP and I-core shape for PCB-integration have been considered. The losses in the inductor can be divided into core losses and winding losses. For the calculation of the core losses the improved generalized Steinmetz equation (iGSE) (cf. (3.16)) has been applied. The eddy current losses in the PCB tracks of the integrated inductor have been calculated based on the results of [103]. The combined core and winding losses of the chosen inductor design (cf. **Table 3.4**) amount to 1.93 W at PV panel

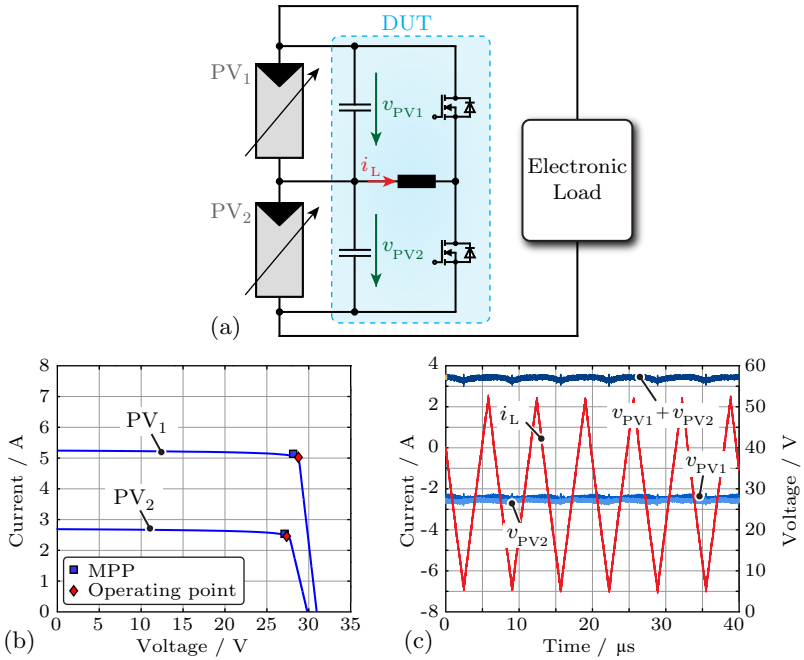

Fig. 3.35: Voltage balancing converter measurement setup and results: (a) measurement setup where a SAS is used to emulate two PV panels and an electronic load to emulate the central inverter; (b) parameters of the emulated PV panels (PV_1 and PV_2) and measured operating points; (c) measured waveforms of the inductor current i_L and PV panel voltages v_{PV1} and v_{PV2}.

voltages of 25 V. The conduction losses in the MOSFETs at a junction temperature of $T_j = 25\,°C$ are calculated as $P_{MOSFET,cond} = 180\,mW$ based on (3.45).

3.4.5 Measurement Results

The measurement setup and results of one balancing converter connected around two PV panels are shown in **Fig. 3.35**. The electrical characteristics of PV panels were emulated with a Solar Array Simulator (SAS) from Agilent (E4360) and the central DC/AC converter was resembled by an electronic load (Chroma / 63200), which was operated in constant voltage mode. The applied test scenario reflects

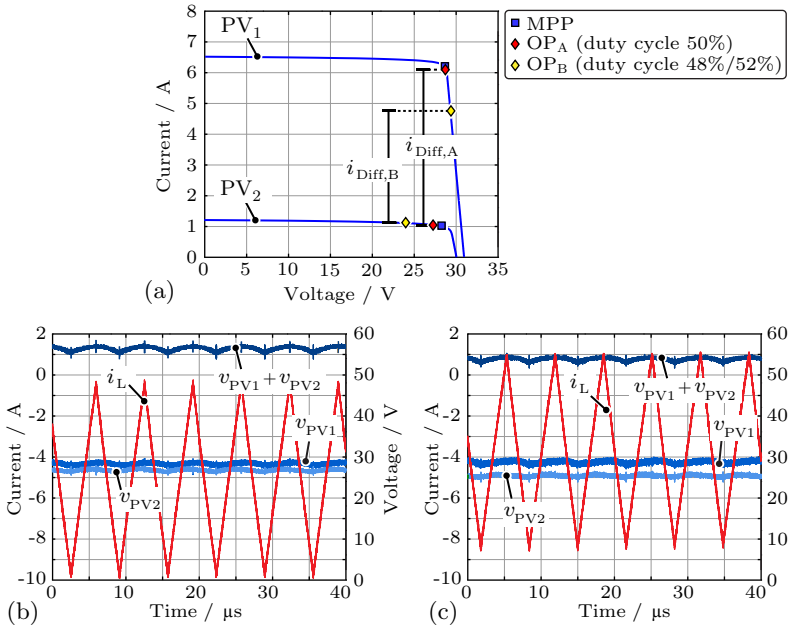

Fig. 3.36: Measurement results of the overcurrent protection concept: (a) operating points OP_A and OP_B of a system consisting of one heavily shaded and one unshaded PV panel with a balancing converter shown for the cases without any protection concept (i.e OP_A) and with the proposed protection concept (i.e OP_A); (b) measured voltage and current waveforms for the operation without any protective measures with the MOSFETs operating at hard switching; (c) activated protection concept where the PV panels are operated at different voltages with a smaller current difference and thus the triangular current is utilized for ZVS.

the case of one unshaded PV panel with a maximum output power of $P_{PV1,MPP} = 145\,W$ (i.e. $V_{PV1,MPP} = 29\,V$ and $I_{PV1,MPP} = 5\,A$) and a shaded panel with a maximum output power of only $P_{PV2,MPP} = 70\,W$ (i.e. $V_{PV2,MPP} = 28\,V$ and $I_{PV2,MPP} = 2.5\,A$). With the application of the balancing module, both PV panels can be operated in or close to their MPP as visible in **Fig. 3.35(b)**. The measured inductor current waveform with triangular shape and the balanced PV panel voltages are depicted in **Fig. 3.35(c)**.

The protection circuitry was tested with a scenario where one panel

is unshaded (i.e. $P_{\mathrm{PV1,MPP}} = 145\,\mathrm{W}$, $V_{\mathrm{PV1,MPP}} = 29\,\mathrm{V}$ and $I_{\mathrm{PV1,MPP}} = 6.5\,\mathrm{A}$) and the second panel is heavily shaded (i.e. $P_{\mathrm{PV2,MPP}} = 28\,\mathrm{W}$, $V_{\mathrm{PV2,MPP}} = 28\,\mathrm{V}$ and $I_{\mathrm{PV2,MPP}} = 1.0\,\mathrm{A}$) accordingly delivering only a fraction of the power of the unshaded panel. Without any protective measures, the average inductor current in the balancing module is driven above the predefined upper limit of 5 A and the MOSFETs are operated in hard switching mode since there is no change in the direction of the current anymore, as shown in **Fig. 3.36(b)**. When the protection circuit is active, however, the duty cycles of the balancing converter are slightly adapted until they reach 48 % / 52 %. This allows to drive the operating points of the PV panels to values with a lower current difference, i.e. the unshaded PV panel is operated at a voltage above the MPP whereas the shaded PV panel is operated at a voltage below its MPP. Then the absolute value of the average current in the inductor decreases and, since the current changes its direction again at each switching state, the MOSFETs are operated again with ZVS, as depicted in **Fig. 3.36**.

The total losses in one balancing module at no load operation (i.e. no mismatch between the PV panels) for PV panel voltages of 25 V were measured to be $P_{\mathrm{Loss,tot}} = 2.65\,\mathrm{W}$, where the losses that can be attributed to the auxiliary electronics account for around $P_{\mathrm{Loss,aux}} \approx 550\,\mathrm{mW}$. As a result, in a PV system with a string of 10 equally irradiated PV panels with an output power of $P_{\mathrm{MPP}} = 220\,\mathrm{W}$ each, the system efficiency reaches $\eta_{\mathrm{Sys}} = 99.0\%$ based on (3.46).

3.4.6 Summary

For the class of parallel-connected partial-power PV panel integrated converters a voltage balancing converter based on the buck-boost topology is presented. The converter is designed to operate with ZVS at all operating points by adjusting the switching frequency depending on the PV panel voltage and by an additional two-level overcurrent protection concept. The two-level protection concept provides safe operation with ZVS also at undesired shading scenarios by adjusting the duty cycle or by shutting down the balancing module if severe mismatch conditions occur. Furthermore, an analytical framework is introduced to describe the current distribution within a PV system with an arbitrary number of PV panels and corresponding balancing converters. Based on this analytic framework, a converter optimization is performed and a com-

pact prototype with low part count and easy controllability is designed. The measurement results show that the output power of a string with PV panels receiving different irradiance can be maximized with a very high efficiency with this concept. The protection concept is verified with measurements at two very unequally irradiated PV panels.

3.5 Series-Connected Partial-Power MIC

The S-PPC can add the output voltage of the converter to the panel output voltage (boost operation) and/or subtract it from the panel voltage (buck operation). The S-PPC with only boost functionality is also often referred to as Series Connected Boost (SCB) converter [104], [105]. This converter type can be realized with a transformer with either a full-bridge, half-bridge or push-pull stage on the primary side and a full-bridge diode rectifier, center-tapped rectifier or voltage doubler rectifier on the secondary side [106]. Topologies which allow for both buck and boost operation are presented in [107], [108] and [109]. For the same reasons as explained for the series connected full-power converter concept (cf. **Sec. 3.2**), a S-PPC with buck-boost voltage conversion capability is favorable.

3.5.1 Component Load Factors

In order to assess the potential of the S-PPC concept in comparison to series-connected full-power converters, the concept of component load factors (CLF) [110] is selected among different evaluation methodologies such as e.g. calculating component utilization quantities [74, 89, 111, 112], and other criteria [113]. According to [110], the CLF is calculated by relating the apparent power of a component to the active output power of a system:

$$\sigma = \frac{V^* I^*}{P_{\mathrm{tot}}} \ . \tag{3.47}$$

A total CLF can be derived for each component type, i.e. for transistors, diodes, inductive components and capacitors by adding the CLF values of the individual components of the same type. A low CLF indicates a low component and/or low realization effort due to a good utilization of the components and thus low values are better than large values. Depending on the type of component, the values of V^* and I^* can be peak, RMS or peak-to-peak values. The quantity P_{tot} is the total output power which is for PPCs the sum of the power directly transferred to the load and the power processed by the converter (cf. **Fig. 3.4**).

Since the buck-boost S-PPCs [107–109] exhibit a high component count and complexity, which renders the application as MICs with long

lifetime requirement as rather unlikely, only S-PPC with boost functionality are regarded in the assessment to identify their potential as MICs. In the following, three different topologies of S-PPC boost converters (cf. **Fig. 3.37(b)-(d)**) are evaluated and compared to the standard full-power boost converter (**Fig. 3.37(a)**). All values related to the full-power boost converter are labeled by the subscript FP as an acronym for

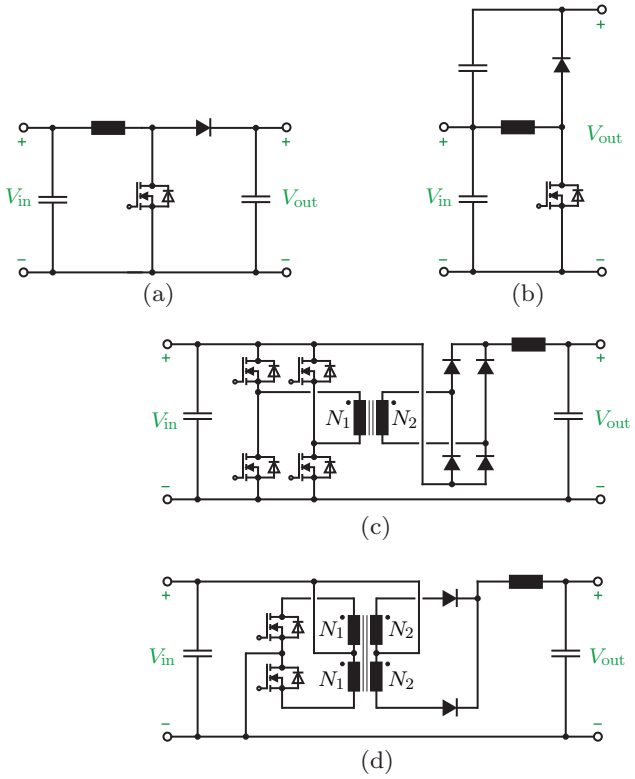

Fig. 3.37: Full-power and S-PPC boost converter topologies: (a) Standard full-power boost converter used as reference (label: FP), (b) cascaded S-PPC consisting of a buck-boost converter with cascaded input and output voltages (label: CAS), (c) S-PPC with a MOSFET full-bridge on primary side and full-bridge diode rectifier on the secondary side (label: PP1), (d) S-PPC with push-pull stage on the primary side and center-tapped rectifier on the secondary side (label: PP2).

full-power. The S-PPC converter topology shown in **Fig. 3.37(b)** [114] is labeled with the subscript CAS since it can be seen as a boost converter with input/output voltage cascading. (The topology is similar to the P-PPC voltage balancer converter shown in **Fig. 3.29(a)** even if both converters perform a different function.) The other two topologies are a subset of possible S-PPC realizations of the series connected boost converter (SCB) [104], [105] that can comprise either a full-bridge, half-bridge or push-pull topology on the primary side or a full-bridge rectifier, voltage-doubler, current-doubler or center-tapped rectifier on the secondary side [109], [108], [106]. The realization of **Fig. 3.37(c))** is labeled with PP1 and the one from **Fig. 3.37(d))** with PP2. For a meaningful comparison, the duty cycles of all topologies have to be given as a function of the voltage transfer ratio $T_\mathrm{R} = V_\mathrm{out}/V_\mathrm{in}$,

$$D_\mathrm{FP} = D_\mathrm{CAS} = \frac{T_\mathrm{R} - 1}{T_\mathrm{R}} \tag{3.48}$$

$$D_\mathrm{PP1} = D_\mathrm{PP2} = (T_\mathrm{R} - 1)\frac{N_1}{N_2} \ . \tag{3.49}$$

For the deduction of the CLF values, following assumptions were made [110]:

- Ripple currents in filter chokes are neglibly small.
- Converter losses are negligble, thus $P_\mathrm{in} = P_\mathrm{out}$.

Transistor CLFs

As MOSFETs have a resistive on-state behavior, the RMS current is chosen as I^*. For V^* the peak blocking voltage is selected based on the simplification that no over-voltage occurs during the switching transient. This yields as total transistor CLF values

$$\sigma_\mathrm{S,FP} = \frac{\sqrt{D_\mathrm{FP}}}{1 - D_\mathrm{FP}} \tag{3.50}$$

$$\sigma_\mathrm{S,CAS} = \frac{\sqrt{D_\mathrm{CAS}}}{1 - D_\mathrm{CAS}} \tag{3.51}$$

$$\sigma_\mathrm{S,PP1} = 4\sqrt{\frac{D_\mathrm{PP1}}{2}}\frac{1}{1 + \frac{N_2}{N_1}D_\mathrm{PP1}}\frac{N_2}{N_1} \tag{3.52}$$

$$\sigma_\mathrm{S,PP2} = 2\sqrt{\frac{D_\mathrm{PP2}}{2}}\frac{1}{1 + \frac{N_2}{N_1}D_\mathrm{PP2}}\frac{N_2}{N_1} \ . \tag{3.53}$$

Diode CLFs

The conduction losses of diodes are mainly determined by the average diode current chosen as I^*. Similar to the transistor CLF, the peak diode blocking voltage is chosen as V^*. The total diode CLF values can be determined as

$$\sigma_{\mathrm{D,FP}} = 1 \tag{3.54}$$

$$\sigma_{\mathrm{D,CAS}} = 1 \tag{3.55}$$

$$\sigma_{\mathrm{D,PP1}} = 2\frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1} \tag{3.56}$$

$$\sigma_{\mathrm{D,PP2}} = 2\frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}\ . \tag{3.57}$$

Inductor CLFs

For the inductors, the average current is approximately equal to the RMS current if a low current ripple is assumed and is accordingly selected as I^*. For V^* the average AC-voltage is chosen, which is the product of applied voltage and duty cycle if a square wave excitation voltage is assumed [110][1]. This results in

$$\sigma_{\mathrm{L,FP}} = D_{\mathrm{FP}} \tag{3.58}$$

$$\sigma_{\mathrm{L,CAS}} = D_{\mathrm{CAS}} \tag{3.59}$$

$$\sigma_{\mathrm{L,PP1}} = D_{\mathrm{PP1}}(1-D_{\mathrm{PP1}})\frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1} \tag{3.60}$$

$$\sigma_{\mathrm{L,PP2}} = D_{\mathrm{PP2}}(1-D_{\mathrm{PP2}})\frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}\ . \tag{3.61}$$

Transformer CLFs

Only the topologies **Fig. 3.37(c)** and **(d)** comprise a transformer for which again a CLF can be computed for each transformer winding.

[1] The energy stored in an inductor is equal to $W = L \cdot I_{\mathrm{DC}}^2/2$ where the inductance value L is determined by the current ripple ΔI and the applied voltage; $L = V \cdot D/(f_{\mathrm{sw}} \cdot \Delta I)$. With an allowed current ripple of $\varepsilon_{\mathrm{iL}} = \Delta I/I_{\mathrm{DC}}$ the energy can be expressed as $W = I_{\mathrm{DC}} \cdot V \cdot D/(2 \cdot \varepsilon_{\mathrm{iL}} \cdot f_{\mathrm{sw}})$ which yields $W = I^* \cdot V^*/(2 \cdot \varepsilon_{\mathrm{iL}} \cdot f_{\mathrm{sw}})$ and therefore justifies the selection of the above mentioned values for the calculation of the CLF.

The average AC voltage and the RMS current are selected as V^* and I^* respectively and the transformer load factor is calculated as the sum of the load factors of all windings

$$\sigma_{\mathrm{T,PP1}} = D_{\mathrm{PP1}}\sqrt{D_{\mathrm{PP1}}}\frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1} \tag{3.62}$$

$$\sigma_{\mathrm{T,PP2}} = 2D_{\mathrm{PP2}}\sqrt{\frac{D_{\mathrm{PP2}}}{2}}\frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}\ . \tag{3.63}$$

Please note that this concept is different to the definition of the rated power of a transformer, which is calculated by dividing the sum of all apparent power values of all windings by a factor of two.

Capacitor CLFs

The capacitor design is determined by the current stress and the voltage rating (besides a voltage ripple condition defining a minimum capacitance value). Thus the RMS current is chosen as I^* and the DC voltage as V^*. The CLF values can be derived as

$$\sigma_{\mathrm{C,FP}} = \frac{1}{1-D_{\mathrm{FP}}}\sqrt{(1-D_{\mathrm{FP}})D_{\mathrm{FP}}} \tag{3.64}$$

$$\sigma_{\mathrm{C,CAS}} = \frac{1}{1-D_{\mathrm{CAS}}}\sqrt{(1-D_{\mathrm{CAS}})D_{\mathrm{CAS}}} \tag{3.65}$$

$$\sigma_{\mathrm{C,PP1}} = \frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP1}}}\frac{N_2}{N_1}\sqrt{(1-D_{\mathrm{PP1}})D_{\mathrm{PP1}}} \tag{3.66}$$

$$\sigma_{\mathrm{C,PP2}} = \frac{1}{1+\frac{N_2}{N_1}D_{\mathrm{PP2}}}\frac{N_2}{N_1}\sqrt{(1-D_{\mathrm{PP2}})D_{\mathrm{PP2}}}\ . \tag{3.67}$$

3.5.2 Comparison of the Results

The CLFs are evaluated for the requirement of a small maximum transfer ratio of $T_{\mathrm{R,max}} = 1.2$, which yields a transformer winding ratio of $N_2/N_1 = 0.2$ for the PPCs. The results for each component type are shown in **Fig. 3.38(a)-(e)** versus T_{R} for the topologies of **Fig. 3.37**. As already visible from the derived CLF equations above, the full-power boost converter and the cascaded S-PPC exhibit the same CLF values for all components. Thus, in this case the cascaded S-PPC (CAS) potentially does not exhibit any advantages in terms of converter losses

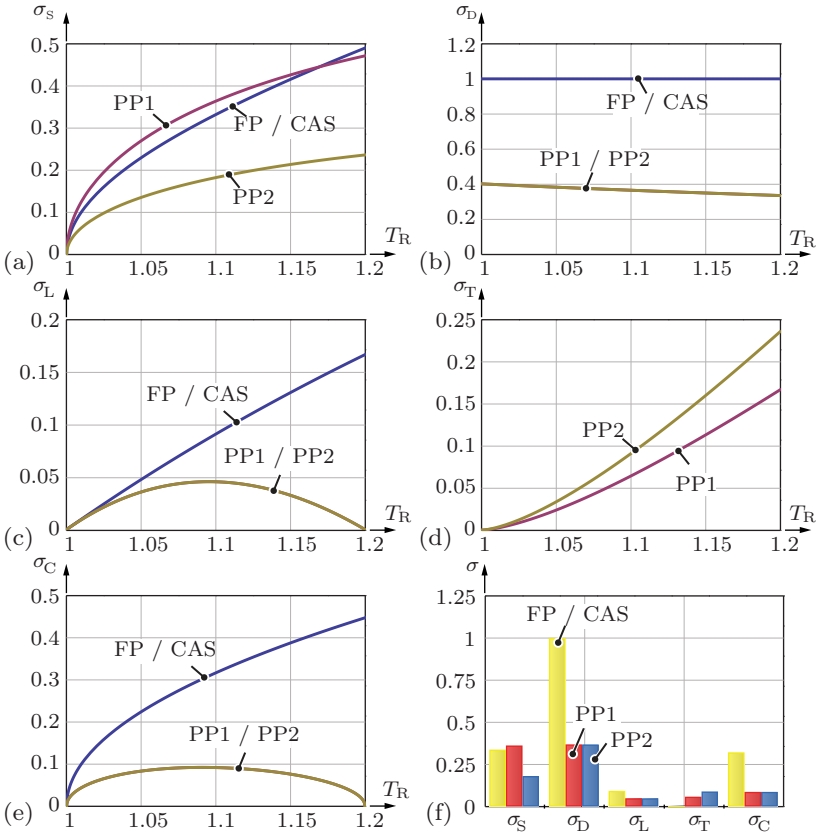

Fig. 3.38: CLF values of the different component types for the converters of **Fig. 3.37** for a maximum transfer ratio of $T_{\mathrm{R,max}} = 1.2$: (a) transistor CLF (σ_{S}), (b) diode CLF (σ_{D}), (c) inductor CLF (σ_{L}), (d) transformer CLF (σ_{T}) and (e) capacitor CLF. In (f) the different CLF values are plotted for a transfer ratio of $T_{\mathrm{R}} = 1.1$.

and/or realization effort. Conversely, the other two concepts (PP1 and PP2) exhibit lower values of the diode CLF (σ_{D}), the inductor CLF (σ_{L}), and the capacitors CLF (σ_{C}) than the full-power boost converter and the PP2 topology also features a lower CLF value of the transistors (σ_{S}). Yet, the S-PPCs require the use of a transformer which yields an additional CLF value. In order to facilitate an easier assess-

ment and comparison of the CLF values of the different topologies, the CLF results for a transfer ratio of $T_{\mathrm{R}} = 1.1$ are shown for the different topologies in the bar chart of **Fig. 3.38 (f)**.

However, even though only a very small maximum transfer ratio was chosen, which requires only a small fraction of the power to be processed by the converter stage of the S-PPC concepts (cf. (3.2)), they do not exhibit a lot smaller CLF values than the full power concept and some CLFs are even larger. However, the partial shading can lead to severe mismatch conditions, which, in combination with the requirement of some flexibility regarding the number of PV panels per string, requires series-connected converters to have a large output voltage range (cf. **Fig. 3.7**). Thus, the concept of S-PPCs will not have any advantages anymore compared to the series-connected full-power converter concept. Quite the contrary, a S-PPC with buck-boost functionality is substantially more complex than the 4-switch buck-boost concept of **Sec. 3.2** and thus will not be investigated further.

3.5.3 Summary

The class of series-connected partial-power converters for PV panel integration is analyzed by means of component load factor comparison. As a result, the possibility to exploit the advantages of S-PPCs as PV panel-integrated DC/DC converters mainly depends on the required voltage conversion ratio. The S-PPC concept only offers an advantage if a slight adaption of the PV panel current is required, and thus the rated power of the converter can be relatively low, which yields low CLF values as shown for small maximum transfer ratios of $T_{\mathrm{R,max}} = 1.2$. However, as already mentioned in **Sec. 3.2**, the output voltages of the converters have to cover a wide range (up to a factor of four between the minimum and maximum voltage) in order to cope with the most challenging shading scenarios. In combination with the relatively high complexity of the S-PPC buck-boost concept, this renders the S-PPC as unsuitable for PV panel integration.

3.6 Summary and Conclusion

In this chapter, all four possible combinations of series and parallel connection of full- and partial-power converters for PV panel integration are analyzed in detail. The partial-power concepts feature the advantage, that the overall system efficiency is only to some extent influenced by the conversion efficiency of the converter, depending on the mismatch condition between the PV panels. However, the analysis of the partial-power converter concepts has revealed some drawbacks of these concepts:

- *P-PPC*: The power flows in the balancing modules are interdependent, such that a shading of one PV module affects all balancing modules. Depending on the length of the PV string and the specific shading scenario, very high currents can occur in the balancing modules. This requires the implementation of over-current protection schemes, which however reduce the power output of the string. Since the string length and the specific shading scenarios also influence the design of the converter, it is difficult to define general converter specifications and design guidelines. Furthermore, paralleling strings, which are equipped with P-PPCs is only possible for the exact same number of PV panels in each string.
- *S-PPC*: In order to obtain some flexibility in the number of PV panels per string and in order to cope with different levels of mismatch conditions, the S-PPCs have to be designed with almost the same component load factors as a full-power converter. In addition, the S-PPC topologies are substantially more complex than full-power converters.

Therefore, the partial-power concepts are well suited for applications with small voltage conversion ratios and/or cells with similar power levels. In PV systems, however, the purpose of the module-integrated converters is to mitigate the negative effects of mismatch between the PV panels where these conditions are not given.

Consequently, the full-power concepts are better suited for the application as PV module integrated converters where the parallel and series connected concepts have different advantages:

- *P-FPC*: The concept of parallel-connected full-power converters offers the greatest flexibility in the design of a PV system. Since

each converter steps up the PV voltage to the DC-link voltage, the system can already be operated with only one PV panel. This might be an advantage for islanded operation in remote areas, where only a small number of PV panels might be available. The maximum number of PV panels is only determined by the power rating of the central DC/AC converter. Furthermore, the operation of a P-FPC is independent from the shading conditions of the other converters, which simplifies the design process.

- *S-FPC*: The concept of series-connected full-power converters provides a higher efficiency than the P-FPC concept. This is due to the fact that always only one conversion stage is employed with a smaller conversion ratio than in the P-FPC concept (which in this thesis has been implemented with two series connected converter stages, cf. **Fig. 3.22(a)**). In addition, a bypass mode can be activated when the input and output voltage of a S-FPC are in close vicinity. Furthermore, due to the omission of a second conversion stage, the part count is lower, which also reduces the costs of this concept.

4

Multi-Cell Telecom Rectifier

DRIVEN by the increasing popularity of cloud-based internet services, the Internet-of-Things, and the trend around "big data", the electricity consumption of data centers has grown tremendously in the past decade and is projected to grow even further in the future, e.g. around 70% from 2013 to 2020 in the US alone [115]. As a consequence, data centers are now one of the largest consumers of electricity and therefore also under a growing financial and political pressure to increase their energy efficiency.

State-of-the-art single-phase telecom power supply modules usually comprise a PFC rectifier stage and an isolated DC/DC converter output stage, usually generating a nominal output voltage of 48 V. The rectifier stage is typically a boost-type PFC rectifier which in the simplest case consists of a full-bridge diode rectifier in connection with a boost converter. Since the forward voltage drops of the diodes in the rectifier account for high conduction losses, alternative bridgeless topologies have gained significant interest over the past years [116, 117]. One example of a highly efficient single-phase bridgeless telecom rectifier is described in [55]. This is a triple-parallel-interleaved Triangular Current Mode (TCM) PFC rectifier system with a double-parallel-interleaved phase-shift full-bridge isolated DC/DC converter (rated power $P_{\text{out}} = 3.3\,\text{kW}$, rated output voltage $V_{\text{out}} = 48\,\text{V}$) which features a power density of $\rho = 3.3\,\text{kW/dm}^3$ and an efficiency of $\eta = 97\,\%$ at half of the rated power. A new approach towards a hyper-efficient and super-compact telecom rectifier design beyond the barriers of traditional converter concepts is presented in this chapter. The approach is based on the employment of multiple low power converter cells which are connected in series at the input terminals and in parallel at the output terminals

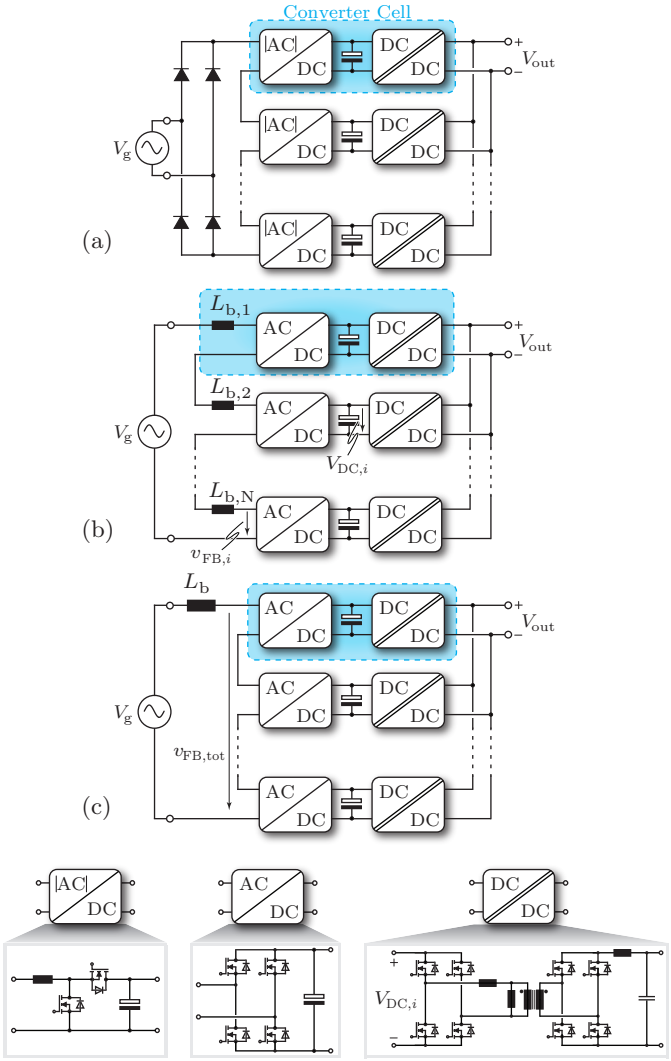

Fig. 4.1: Multi-cell telecom power supply module topologies in input-series output-parallel (ISOP) arrangement: (a) input side diode rectifier with converter cells containing an |AC|/DC boost converter (processing a time-varying input voltage) and an isolated DC/DC converter connected in series; topologies where each cell contains an AC/DC converter input stage with (b) either a distributed line inductance or (c) a single line inductor, and an isolated DC/DC converter stage.

(Input Series Output Parallel - ISOP). A multi-cell telecom power supply with this configuration can essentially be realized in three different ways, as shown in **Fig. 4.1**. Common to all three concepts is the application of multiple converter cells that equally share the input voltage and the output current, which requires a means of isolation between the individual series-stacked DC-link potentials from the common output potential. Therefore, in all three concepts an isolated DC/DC converter stage is employed in each converter cell. The three concepts mainly differ concerning the rectification of the sinusoidal mains voltage. In **Fig. 4.1(a)** a full-bridge diode rectifier is utilized, similar to the structure of a conventional boost PFC rectifier, but with the difference that the boost stage is split-up into multiple |AC|/DC converter boost stages, which are located at the input of each converter cell. Since the diode full-bridge leads to significant conduction losses and synchronous rectification devices would have to be rated for the full peak input voltage, this concept will be discarded. In **Fig. 4.1(b)** and **(c)** the diode bridge is omitted and, instead, a full-bridge synchronous rectifier is integrated in each converter cell, which only requires semiconductors which are rated for the DC-link voltage of a single cell. The boost inductor (L_b) can either be realized by distributed inductors where each inductor is associated to one converter cell (cf. **Fig. 4.1(b)**) similar to the distributed boost stages of **Fig. 4.1(a)**, or can be realized by a single inductor for the whole converter system (cf. **Fig. 4.1(c)**). The inductance value of the single inductor in the latter concept equals the sum of the distributed inductances of the former concept, for the assumption of same input current ripple. Since the realization effort and the total volume is smaller for a single inductor than for distributed inductors[1], the concept of **Fig. 4.1(c)** is selected in this paper.

In the following sections the benefits of the multi-cell converter approach, the optimization, the design, and the control of the multi-cell telecom rectifier system of **Fig. 4.1(c)** are analyzed. At first,

[1]The area product of an inductor (defined as product of the winding area and the core area) scales with the required inductance and can be calculated in a first step as $A_\mathrm{w}A_\mathrm{c} = L \cdot I^2/(S \cdot k_\mathrm{fill} \cdot B_\mathrm{max})$ where S is the current density, k_fill is the filling factor of the winding area and B_max the maximum flux density. The area product is proportional to the fourth power of the linear dimension l whereas the volume is proportional to l^3. Thus, the volume of N inductors with each having an inductance of L/N is $\mathrm{Vol}_\mathrm{tot} = N \cdot (A_\mathrm{w}A_\mathrm{c}/N)^{(3/4)} = N^{1/4}\mathrm{Vol}_\mathrm{single}$ which is by a factor of $N^{1/4}$ larger than the volume $\mathrm{Vol}_\mathrm{single}$ of a single inductor with inductance L.

in **Sec. 4.1** fundamental scaling laws of power electronic systems are summarized, which highlight the advantages of multi-cell converters for AC/DC conversion. The implemented control scheme for the ISOP multi-cell system with a master-slave regime is presented in **Sec. 4.2**. In **Sec. 4.3** the available degrees of freedom in the design of a multi-cell converter system are analyzed, the modeling of the losses and volumes of the employed components is outlined and the optimization results are discussed. Subsequently, in **Sec. 4.4** the design of the hardware demonstrator is shown and critical design aspects are analyzed. In order to verify the optimization results, different measurement results of the hardware demonstrator are presented in **Sec. 4.5**. Since the standard control concepts do not leverage all available degrees of freedom in the control the ISOP system, a more advanced 4D-interleaving control scheme is introduced in **Sec. 4.7**. Finally, conclusions are drawn in **Sec. 4.8**.

4.1 AC/DC Converter Scaling Laws

In this section, the benefits offered by a multi-cell AC/DC converter system compared to its single-cell converter counterpart are presented. The discussion is based on the fundamental scaling laws of both parallel- and series-interleaved DC/DC converter systems introduced in **Chapter 2** which are now applied to the AC/DC multi-cell converter system at hand.

4.1.1 Input Voltage Harmonic Spectrum and Input Current Ripple

The AC/DC conversion of the multi-cell telecom PFC rectifier (cf. **Fig. 4.1(c)**) comprises multiple series connected full-bridge switching stages that are advantageously operated with a phase-shifted (interleaved) modulation scheme considering a phase shift of $\delta_{\mathrm{ph}} = 2\pi/N_{\mathrm{cells}}$, with N_{cells} being the number of converter cells. In the simplest case, only one bridge leg of each cell is operated at switching frequency $f_{\mathrm{sw,cell}}$, while the other bridge leg is operated at mains frequency f_{g}. This modulation method is commonly referred to as totem-pole modulation [118]. For a system with N_{cells} series-connected and interleaved full-bridge cells, this results in an effective switching frequency $f_{\mathrm{sw,eff}}$ of the entire rectifier stage, which is N_{cells} times higher than the switching

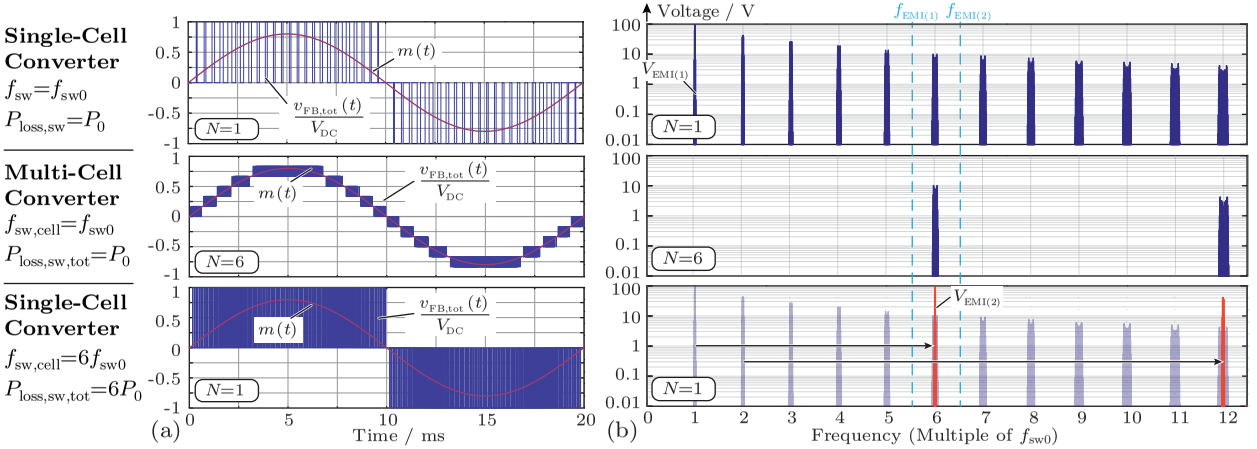

Fig. 4.2: Effect of multiple rectifier stages with phase-shifted modulation on the system behavior: (a) comparison of the switched voltage waveform between (top) a single-cell converter system and (middle) a multi-cell converter system with six converter cells. Both systems feature the same switching losses (cf. Tab. 2.1); (bottom) single-cell converter waveform with six times the switching frequency and also six times higher switching losses than the other two options; (b) Corresponding harmonic spectra of the waveforms shown in (a). As a result, operating a single rectifier stage with six times the switching frequency does not yield the same harmonics (in amplitude) as the multi-cell converter system but creates six times higher switching losses. The cancellation of harmonics can lead to a reduction of the EMI filter volume if the EMI limited frequency range starts after the harmonic which is not canceled, i.e. $f_{\mathrm{EMI}(2)}$. On the contrary, if the uncanceled harmonic is the first harmonic in the limited frequency range, i.e. $f_{\mathrm{EMI}(1)}$, the EMI filter has to be designed with the same attenuation as for the single-cell system operated at $f_{\mathrm{sw},0}$.

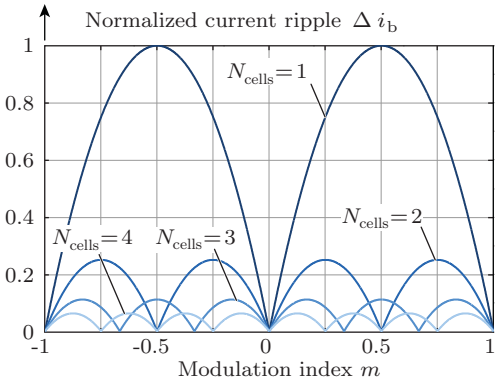

Fig. 4.3: Peak-to-peak current ripple reduction of the boost inductor current i_b (normalized to $V_{DC}/(4f_{sw}L_b)$) for different numbers of rectifier stages N_{cells} in dependency of the modulation index $m = v_{FB,tot}/V_{DC}$ for a given value of boost inductance L_b.

frequency $f_{sw,cell}$ of a single cell, i.e. $f_{sw,eff} = N_{cells} \cdot f_{sw,cell}$. Compared to the conventional single-cell topology where a capacitor voltage V_{DC} is required for the operation of the PFC rectifier (i.e. sufficiently above the peak value of the mains voltage $\hat{V}_g$), in the multi-cell system this voltage is distributed among N_{cells} capacitors, i.e. each DC-link capacitor is charged to $V_{DC,i} = V_{DC}/N_{cells}$. As a result, the voltage $v_{FB,tot}$ (i.e sum of all rectifier stage voltages $v_{FB,i}$) comprises $2 \cdot N_{cells} + 1$ voltage levels, as shown in **Fig. 4.2(b)**.

Consequently, with a higher effective switching frequency and more voltage levels of the rectifier voltage $v_{FB,tot}$, the peak-to-peak current ripple Δi_b of the boost inductor current i_b decreases with increasing number of converter cells. The current ripple can be calculated in dependency of the modulation index m by introducing an effective modulation index $m_{eff} = (m \text{ modulo } 1/N_{cells})$, i.e. a modulation index that has only values between 0 and $1/N_{cells}$, with the relation of $v = L\mathrm{d}i/\mathrm{d}t$ as

$$\Delta i_b(m_{eff}) = \frac{V_{DC}}{f_{sw}L_b} \cdot m_{eff} \cdot \left(\frac{1}{N_{cells}} - m_{eff} \right) . \tag{4.1}$$

(cf. [119]). This relation is shown in **Fig. 4.3** normalized to the value of $V_{DC}/(4f_{sw}L_b)$. The maximum peak-to-peak value of the boost inductor

current ripple can be found at $m_{\mathrm{eff}} = 0.5/N_{\mathrm{cells}}$ as

$$\Delta i_{\mathrm{b,max}} = \frac{V_{\mathrm{DC}}}{4N_{\mathrm{cells}}^2 f_{\mathrm{sw}} L_{\mathrm{b}}} \ . \tag{4.2}$$

As a result, by increasing the number of cells, N_{cells}, with the same switching frequency, the current ripple of the boost inductor current decreases quadratically for a given boost inductance L_{b}.

The additional voltage steps of the converter voltage in combination with a higher effective switching frequency also lead to an improved EMI spectrum, as can be derived based on [120]. For a single full-bridge stage with a total DC-link voltage V_{DC}, the amplitude $\hat{V}_{\mathrm{FB,single(q)}}$ of a harmonic with order q of the mains frequency $f_{\mathrm{g}} = 1/T_{\mathrm{g}}$ can be calculated for a modulation index $m(t) = v_{\mathrm{FB,tot}}(t)/V_{\mathrm{DC}}$ as

$$\hat{V}_{\mathrm{FB,single}(q)} = \frac{-4 \cdot V_{\mathrm{DC}} \cdot (1-(-1)^k)}{n\pi T_{\mathrm{g}}} \cdot \int_0^{T_{\mathrm{g}}/4} \cos(k \cdot \omega_{\mathrm{g}} \cdot t) \cdot \sin(n \cdot \pi \cdot m(t))\, dt \tag{4.3}$$

with $q = n \cdot z + k$, where $z = f_{\mathrm{sw}}/f_{\mathrm{g}}$ and $|k| \leq z/2$. Typically n is referred to as number of the harmonic of the switching frequency and k specifies the sideband ($n, k \in \mathbb{N}$), as visualized in **Fig. 4.4** for the example of $f_{\mathrm{g}} = 50\,\mathrm{Hz}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$. In a system with N_{cells} rectifier stages, each cell emits harmonics where the amplitude of a harmonic with order q can be calculated according to (4.3) just with a lower DC-link voltage, i.e.

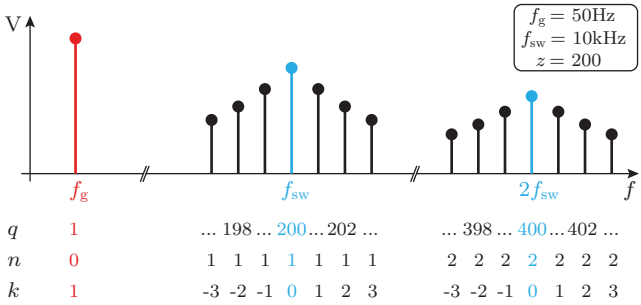

Fig. 4.4: Explanation of the nomenclature used to specify the order $q = n \cdot z + k$ of the harmonics with the example of $f_{\mathrm{g}} = 50\,\mathrm{Hz}$ and $f_{\mathrm{sw}} = 10\,\mathrm{kHz}$.

$$\hat{V}_{\mathrm{FB,cell}(q)} = \frac{\hat{V}_{\mathrm{FB,single}(q)}}{N_{\mathrm{cells}}} \ . \tag{4.4}$$

Since the cells are operated interleaved to each other, the time dependent waveform of a harmonic with order q of the total multi-cell converter input voltage $v_{\mathrm{FB,tot}}$ has to be expressed as a sum of voltages of all cells, taking into account the phase-shift between the individual cells,

$$\hat{V}_{\mathrm{FB,tot}(q)}(t) = \sum_{i=1}^{N_{\mathrm{cells}}} \frac{\hat{V}_{\mathrm{FB,single}(q)}}{N_{\mathrm{cells}}} \cos\left(q\left(2\pi f_{\mathrm{g}} t + \frac{2\pi}{zN_{\mathrm{cells}}}(i-1)\right)\right). \tag{4.5}$$

By assuming $z \to \infty$, (4.5) converges to the simplified expression of

$$\hat{V}_{\mathrm{FB,tot},(q)}(t) = \begin{cases} \hat{V}_{\mathrm{FB,single(q)}} \cos(q 2\pi f_{\mathrm{g}} t), & \text{if } n = l \cdot N_{\mathrm{cells}},\ l \in \mathbb{N} \\ 0, & \text{else.} \end{cases} \tag{4.6}$$

The amplitude of this time-dependent waveform is the amplitude of the considered harmonic. Consequently, the harmonic spectrum of the multi-cell system can be derived from the spectrum of a single-cell converter system by considering only the harmonics $q = n \cdot z + k$ where n is a multiple of the number of converter cells N_{cells}, i.e. $\hat{V}_{\mathrm{FB,tot},(q)} = \hat{V}_{\mathrm{FB,single(q)}}$ for $n = l \cdot N_{\mathrm{cells}}$, $l \in \mathbb{N}$, as visualized in **Fig. 4.2(b)**. Thus, the interleaving of multiple low-voltage converter cells has the advantage of harmonic cancellation compared to a single-cell converter under the assumption of equal switching losses.

In order to quantify the effect of the harmonic cancellation on the EMI filter design and/or requirement, however, the relevant EMI standards have to be taken into account. In typical PFC applications the conducted high-frequency harmonic noise emissions are restricted by EMI standards (e.g. CISPR Class A and B) which define absolute allowable emissions limits on harmonics in the frequency range of $150\,\mathrm{kHz} \leq f \leq 30\,\mathrm{MHz}$. Since the noise transfer function of an EMI filter stage has a roll-off slope of $-40\,\mathrm{dB/dec}$ and an EMI filter has typically two or more filter stages, the overall filter frequency characteristic has a much steeper roll-off characteristic than the EMI standard which shows a roll-off slope of the admissible noise level of only $-20\,\mathrm{dB/dec}$ (Class B) up to a frequency of 500 kHz. Therefore, typically only the

first harmonic of the converter, which falls into the restricted EMI spectrum, has to be considered for the design of the EMI filter. As a result, the cancellation of harmonics in multi-cell converter systems is only offering benefits in terms of reduced EMI filtering efforts compared to single-cell systems if the first harmonic is among the canceled harmonics of the single-cell system and would fall into the limited EMI spectrum, which was previously determining the filter design in the single-cell converter. That means, that e.g. in **Fig. 4.2(b)** the multi-cell converter with six converter cells has the greatest reduction of the EMI filter volume if the restricted frequency band starts between the sixth and seventh harmonic (i.e. after a harmonic that is not canceled) of the single-cell system (cf. $f_{\mathrm{EMI}(2)}$ in **Fig. 4.2(b)**), e.g. if the sixth harmonic is at 140 kHz . On the contrary, however, if the sixth harmonic would be the first harmonic in the EMI limited frequency band (cf. $f_{\mathrm{EMI}(1)}$ in **Fig. 4.2(b)**), e.g. at 150 kHz or above, then the interleaving of the converter with six cells would not result in EMI filter benefits since the sixth harmonic is not canceled, i.e. the harmonic which determines the filter design in the single-cell system is the same harmonic as in the multi-cell system.
Please note, that the cancellation of harmonics in multi-cell systems is not equal to operating the single-cell system with N_{cells} times the switching frequency. This would (apart from a sixfold increase of switching losses) only shift the harmonics to higher frequencies but not additionally reduce the amplitude of the harmonics, as it is the case for the interleaved cell operation of a multi-cell system. The reason for this is, that the single-cell converter would still switch the full DC-link voltage and not the low voltage levels as in the staircase voltage waveform of the multi-cell system. This is visualized in **Fig. 4.2(b)** where the harmonic spectrum of $V_{\mathrm{EMI}(2)}$ is the spectrum of the single-cell converter with six times the switching frequency of the original system with spectrum $V_{\mathrm{EMI}(1)}$.

The boost inductor can also be considered as a part of the EMI filter since it provides attenuation to emitted harmonics of the converter, which offers a degree of freedom in the choice of the boost inductance and the attenuation of the remaining EMI filter. Instead of designing the multi-cell converter for the same maximum peak-to-peak current ripple $\Delta i_{\mathrm{b,max}}$ as the single-cell system, which would yield a boost inductance which is $1/N_{\mathrm{cells}}^2$ times smaller, a reduction of the boost inductance of e.g. only $1/N_{\mathrm{cells}}$ might also be acceptable which in addition

to a smaller boost inductance also leads to a lower current ripple. This would result for the multi-cell system in a lower attenuation requirement of the remaining EMI filter and thus in a smaller volume of this part of the EMI filter in addition to the smaller volume of the boost inductor than in the single-cell system.

4.2 ISOP Converter Control Concept

One of the main challenges regarding the control of multi-cell converters in general is the equal distribution of the current and/or voltage among the converter cells. In ISOP systems, the total DC-link voltage should be equally shared between the individual cells in order to avoid critical voltages above the component ratings of each cell. Furthermore, the output current and/or power should be equally split among the DC/DC converter stages such that no cell exceeds its power rating and the losses are evenly distributed between the cells.

4.2.1 Common-Duty Cycle Control

The most convenient way to operate an ISOP multi-cell system is to apply a common modulation index to all AC/DC converter stages and a common duty cycle (i.e. phase-shift for the phase-shifted full-bridge (PSFB) converters) to all converter cells. This operation scheme relies on the natural balancing behavior inherent to ISOP multi-cell converter systems [25, 37, 121].

Voltage and Current Balancing

For the case that all converter cell hardware realizations are exactly identical, the DC-link voltage and output currents are perfectly balanced since any deviation of the DC-link voltages from the balanced steady state leads to different output power levels which are counteracting the unbalance. Since this balancing method is not actively controlling the DC-link voltages and output currents, however, any mismatch between the converters, such as e.g. slightly different transformer terminal behaviors, leads to unbalanced DC-voltage levels and output currents but not to a runaway situation [25]. The DC-link cell voltages $V_{\mathrm{DC},i}$ can be calculated for the case of different transformer turns ratios as [25]

$$V_{\mathrm{DC},i} = V_{\mathrm{DC}} \frac{1}{\left(\sum_{k=1}^{N_{\mathrm{cells}}} \frac{1}{n_{\mathrm{k}}}\right) \cdot n_{\mathrm{i}}} \tag{4.7}$$

with n_{k} being the transformer turns ratio $N_{\mathrm{sec},k}/N_{\mathrm{prim},k}$ of cell k with $k \in [1, N_{\mathrm{cells}}]$. In the same way, the average steady state output current $I_{\mathrm{out},i}$ of each converter cell can be calculated in dependence of the total output current $I_{\mathrm{out,tot}}$ as

$$I_{\mathrm{out},i} = I_{\mathrm{out,tot}} \frac{1}{\left(\sum_{k=1}^{N_{\mathrm{cells}}} \frac{1}{n_{\mathrm{k}}}\right) \cdot n_{\mathrm{i}}} \ . \tag{4.8}$$

As a consequence, the total power of the system is unequally shared among the converter cells, i.e.

$$P_{\mathrm{cell},i} = P_{\mathrm{tot}} \frac{1}{\left(\sum_{k=1}^{N_{\mathrm{cells}}} \frac{1}{n_{\mathrm{k}}}\right) \cdot n_{\mathrm{i}}} \ . \tag{4.9}$$

Typically, the mismatch between the transformers of the different cells can be kept reasonably small with standard industrial manufacturing methods and/or before assembling a multi-cell converter only transformers with similar terminal characteristics can be selected.

Circulating Currents

Another issue of mismatch between the converter cells can arise from different DC-link capacitances. The employed capacitors in the DC-links are usually electrolytic capacitors featuring a high energy density which is required to filter the power pulsation with twice the grid frequency, if not more advanced compensation techniques such as power pulsation buffers [52] are used. The electrolytic capacitors in the individual cells, however, might have different capacitance values either from the beginning due to manufacturing variance or after some time because of unequal aging processes which might lead to an uneven reduction of the capacitance values [122]. This difference in the DC-link capacitances can cause additional circulating currents between the ISOP connected converter cells with the common-duty cycle control, which is analyzed in the following.

For the simplified case of only two converter cells with equal transformer turns ratios of $n = 1$ (cf. **Fig. 4.5(a)**), an equivalent circuit

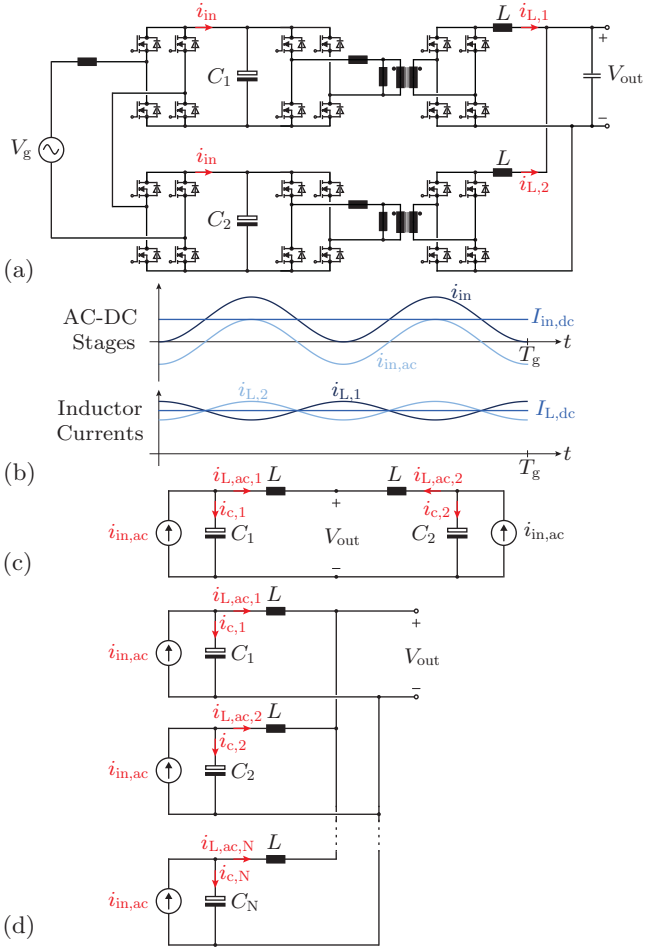

Fig. 4.5: Analysis of circulating currents in ISOP multi-cell systems with common-duty cycle control: (a) simplified ISOP AC/DC converter system with only two converter cells; (b) characteristic waveforms of the input currents and the circulating currents in the output inductors for the case where $C_1 > C_2$; (c) low-frequency AC-equivalent circuit of the two cell ISOP system. The AC/DC converter full-bridges can be modeled as current sources where only the AC-component is considered for the analysis of the circulating current. Since the impedance of the output capacitor at low frequencies is dominating compared to the impedance of the output inductors, the output capacitor can be regarded as an open circuit for the AC-analysis; (d) generalized equivalent circuit with N_{cells} cells.

model can be derived (cf. **Fig. 4.5(c)**) for the analysis of the circulating currents that can occur with the common-duty cycle control. The analysis can be further simplified by considering the low frequency of the circulating current (i.e. twice the fundamental frequency), which allows to regard the output capacitor C_{out} as an open-circuit due to its large impedance ($Z_{\mathrm{c,out}} = 1/\omega C_{\mathrm{out}}$) at low frequencies compared to the impedance of the output inductors ($Z_{\mathrm{L}} = \omega L$). The AC/DC converter stages can be modeled as equal current sources, where only the AC-component is of interest for the following analysis, which is

$$i_{\mathrm{in,ac}} = \frac{P_{\mathrm{sys}}}{V_{\mathrm{DC}}} \cdot e^{j2\omega_{\mathrm{g}}t} \tag{4.10}$$

under the assumption of negligible voltage ripples on the DC-links. By applying the concept of superposition for the two current sources, the currents into the capacitors ($i_{\mathrm{c,1}}$, $i_{\mathrm{c,2}}$) and the ac-components of the inductor currents ($i_{\mathrm{L,ac,1}} = -i_{\mathrm{L,ac,2}}$) can be found in dependence of the component impedance values, i.e.

$$i_{\mathrm{c,1}} = i_{\mathrm{in,ac}} \cdot \frac{2 \cdot (Z_{\mathrm{L}} + Z_{\mathrm{c,2}})}{Z_{\mathrm{tot}}} \tag{4.11}$$

$$i_{\mathrm{c,2}} = i_{\mathrm{in,ac}} \cdot \frac{2 \cdot (Z_{\mathrm{L}} + Z_{\mathrm{c,1}})}{Z_{\mathrm{tot}}} \tag{4.12}$$

$$i_{\mathrm{L,ac,1}} = i_{\mathrm{in,ac}} \cdot \frac{Z_{\mathrm{c,1}} - Z_{\mathrm{c,2}}}{Z_{\mathrm{tot}}} \tag{4.13}$$

with $Z_{\mathrm{c,1}} = 1/(j2\omega_{\mathrm{g}}C_1)$, $Z_{\mathrm{c,2}} = 1/(j2\omega_{\mathrm{g}}C_2)$, $Z_{\mathrm{L}} = j2\omega_{\mathrm{g}}L$ and $Z_{\mathrm{tot}} = Z_{\mathrm{c,1}} + Z_{\mathrm{c,2}} + 2 \cdot Z_{\mathrm{L}}$. The resulting voltage ripple on each capacitor can thus be calculated by

$$v_{\mathrm{c},i} = i_{\mathrm{c},i} \cdot Z_{\mathrm{c},i} \ . \tag{4.14}$$

As a result, the amplitude of the circulating current equals

$$\hat{i}_{\mathrm{L,ac,1}} = \frac{P_{\mathrm{sys}}}{V_{\mathrm{DC}}} \cdot \left| \frac{Z_{\mathrm{c,1}} - Z_{\mathrm{c,2}}}{Z_{\mathrm{tot}}} \right| \ . \tag{4.15}$$

This analysis can be extended to ISOP systems with N_{cells} cells with the same methodology of superposition. For the case that only the first cell has a different DC-link capacitance value than the other cells ($Z_{\mathrm{c,1}} \neq Z_{\mathrm{c,2}} = ... = Z_{\mathrm{c,N}} = Z_{\mathrm{c}}$) the amplitude of the circulating current in the first cell can be derived as

$$\hat{i}_{\mathrm{L,ac,1}} = \frac{P_{\mathrm{sys}}}{V_{\mathrm{DC}}} \cdot \left| \frac{(N_{\mathrm{cells}} - 1) \cdot (Z_{\mathrm{c,1}} - Z_{\mathrm{c}})}{N_{\mathrm{cells}} \cdot Z_{\mathrm{L}} + (N_{\mathrm{cells}} - 1) \cdot Z_{\mathrm{c,1}} + Z_{\mathrm{c}}} \right| \tag{4.16}$$

and in the remaining cells as

$$\hat{i}_{\mathrm{L,ac,2}} = ... = \hat{i}_{\mathrm{L,ac,N}} = \frac{\hat{i}_{\mathrm{L,ac,1}}}{(N_{\mathrm{cells}} - 1)} \ . \tag{4.17}$$

Even though the circulating currents are not destabilizing the system operation, they are a source of additional conduction losses due to higher rms-values of the currents conducted by the switches, transformers and output inductors.

4.2.2 Active Balancing Control Schemes

In order to remedy the adverse effects associated with the mismatch in common-duty cycle control and to guarantee balanced operation, different active control strategies have been proposed for ISOP AC/DC converter systems [123–125]. The balancing of the DC-link voltages can be controlled either by the AC/DC converter stages (also termed cascaded H-bridges in [126–128]) and/or the isolated ISOP DC/DC converter stages whereas the output current sharing is only controllable by the DC/DC stages where control concepts known from ISOP DC/DC conversion systems can be applied [41, 129–131].
In [123] a voltage balancing control is presented which is based on modifying the common-duty cycle control (in *dq*-coordinates) for the AC/DC converter stages [125] in order to balance the DC-link voltages by allowing different duty cycles. Since this can only counteract limited power unbalances of the DC/DC converter stages, an additional power balancing control is also required for the DC/DC converters that are connected in parallel at their outputs.

In [124], the voltage of the DC-links is balanced by operating the AC/DC converter stages with a mixture of low and high frequency PWM and the power transferred through the DC/DC converter stages is balanced by additional controllers. In the aforementioned methods, the voltage balancing is performed by a different stage than the power balancing.
In the selected control scheme, both the DC-link voltage balancing and the output current sharing are handled by the DC/DC converter stages whereas the grid current is controlled by the AC/DC converter stages

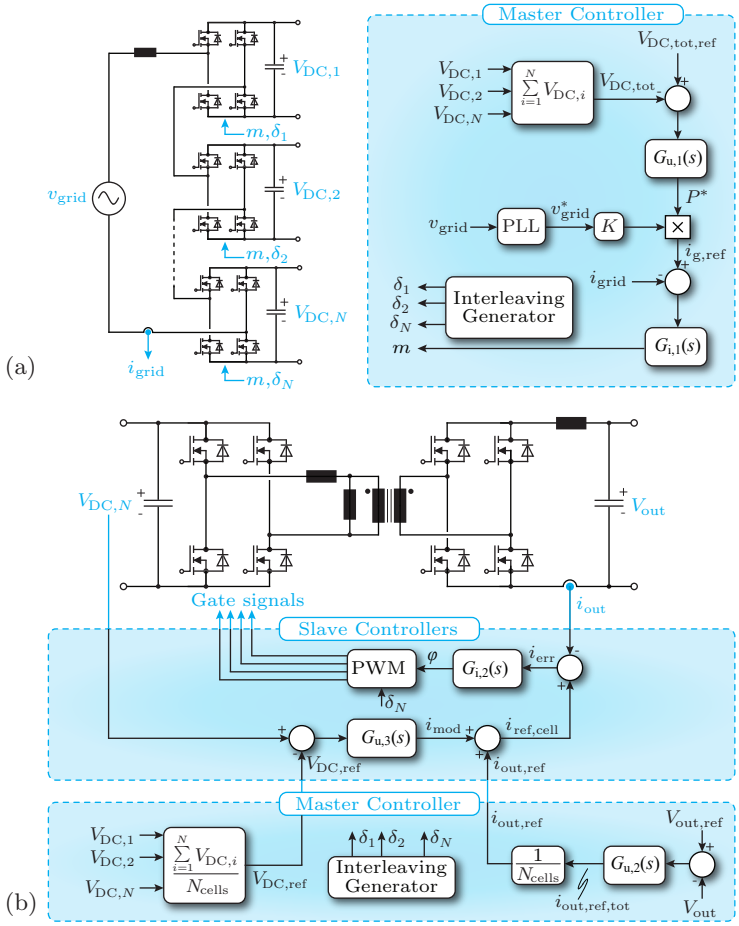

Fig. 4.6: Control implementation of the multi-cell telecom rectifier: (a) total DC-bus voltage controller and input current controller; (b) output current controller and DC-link voltage controller.

with a common-duty cycle control, as shown in **Fig. 4.6**. This control scheme contains a total DC-link voltage regulator on the rectifier side (cf. **Fig. 4.6(a)**) in order to obtain a constant total DC-link voltage (i.e. the sum of all DC-link voltages) with a superimposed 100 Hz ripple. The DC-link voltage regulator of the AC/DC converter stage

consists of cascaded control loops where the outer control loop comprises a proportional-resonant (PR) voltage controller $G_{\mathrm{u},1}(s)$. This controller creates a current reference value $i_{\mathrm{g,ref}}$ of the input current by multiplying the controller output value (power reference value P^*) with the time varying grid voltage value v_{grid} and a factor $k = 2/\hat{V}^2_{\mathrm{grid}}$. This current reference value is tracked by the inner proportional-integral (PI) current controller $G_{\mathrm{i},1}(s)$ which outputs the modulation index m that is given to all AC/DC stages.

Furthermore, the control scheme of the DC/DC converters contains a cascaded output voltage regulator (cf. **Fig. 4.6(b)**) consisting of the outer PI voltage controller $G_{\mathrm{u},2}(s)$, implemented on the master cell, and inner PI current controllers $G_{\mathrm{i},2}(s)$ which are implemented locally on each cell. By controlling the output current of each cell, circulating currents can be prevented. Since output current control alone is not leading to a stable operation of an ISOP system with balanced DC-link voltages [41], an additional DC-link voltage balancing control mechanism has to be implemented. For this reason, each cell also receives the value of the average DC-link voltage of all cells $V_{\mathrm{DC,ref}}$. Each cell can compare this value with its own DC-link voltage and based on that difference the voltage controller $G_{\mathrm{u},2}(s)$ creates a current value i_{mod} which is added to $i_{\mathrm{out,ref}}$, the output of the voltage controller $G_{\mathrm{u},2}(s)$ of the master cell [41]. Thus, the system is driven back to the state where the output power and the total DC-link voltage are equally shared among the converter cells.

This control concept can be implemented as a master-slave control regime. The master cell measures the input current i_{grid}, the grid voltage v_{grid}, the output voltage V_{out} and its own output current $i_{\mathrm{out},i}$. The slave cells, on the other hand, only need to measure their own DC-link voltage $V_{\mathrm{DC},i}$ and output current $i_{\mathrm{out},i}$. The slave cells transmit the value of the DC-link voltage $V_{\mathrm{DC},i}$ to the master cell and receive the modulation m index for the AC/DC stages, the output current reference value $i_{\mathrm{out,ref}}$ which they have to track, the average value of the DC-link voltage of all cells $V_{\mathrm{DC,ref}}$ and the information about their individual phase-shift δ_N required for the interleaved operation of the cells.

4.3 Converter Optimization

In order to identify the efficiency (η) vs. power density (ρ) Pareto performance limit of the proposed multi-cell telecom power supply module

Tab. 4.1: Specifications of the ISOP multi-cell telecom rectifier module.

Parameter	Variable	Value
Nominal grid voltage	$V_{\text{grid,RMS,nom}}$	230 V / 50 Hz
Grid voltage range	$V_{\text{grid,RMS}}$	180 V - 270 V
Rated output power	$P_{\text{sys,rat}}$	3.3 kW
Nominal output voltage	$V_{\text{out,nom}}$	48 V
Output voltage range	V_{out}	40 V - 60 V
Hold-up time	T_{hold}	10 ms at rated power
Switching freq. per cell	f_{sw}	$\geq$ 18 kHz
EMI standards		CISPR Class B
Max. ambient temperature	T_{amb}	40 °C

(the full set of specifications can be found in **Tab. 4.1**), a comprehensive converter optimization has to be performed. This routine takes all available degrees of freedom of the design of the converter into account, which constitutes the design space, and maps the design space into the performance space by means of a performance function, as visualized in **Fig. 4.7**. This allows to compare all possible converter designs with respect to their efficiency and power density [62,132]. The performance function contains the converter behavioral models and analytical models of the losses and volumes of each type of component. The behavioral models allow to determine the characteristic waveforms for each component at a given operating point, and thus to identify the electrical quantities of each component required for the loss and volume calculation, e.g. the RMS values and peak values of voltages and currents and voltage-time areas seen by the components.

4.3.1 Design Space

The design space (cf. **Fig. 4.7(i)**) is comprised of different levels of available degrees of freedoms in the multi-cell converter design where the most basic level is the multi-cell topology itself, i.e. the interconnection of the converter cells such as input-series output-parallel (ISOP), input-series output-series (ISOS), input-parallel output-parallel (IPOP) and input-parallel output-series (IPOS) (cf. [133]). In the case at hand, the ISOP structure is selected since it inherently provides a step-down

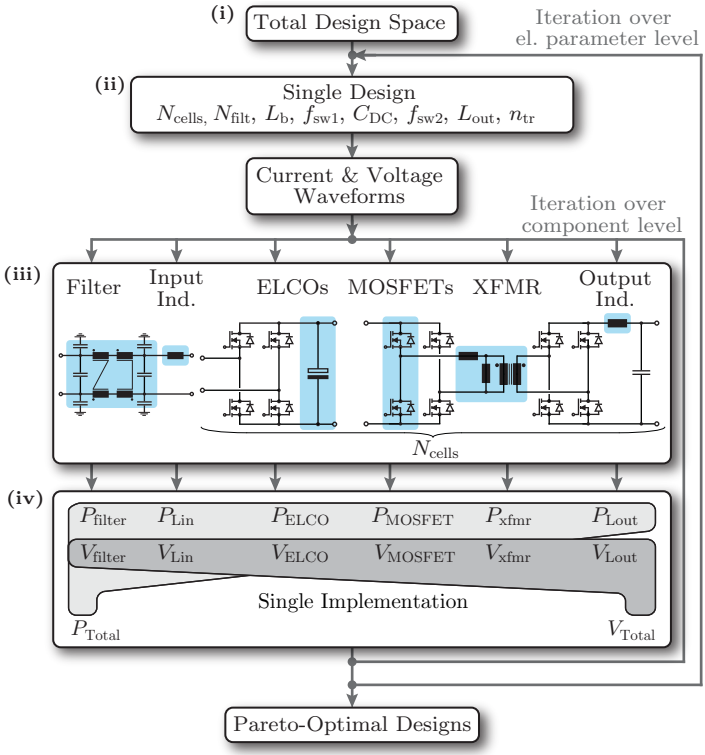

Fig. 4.7: Flowchart visualization of the η-ρ multi-objective optimization of the multi-cell telecom rectifier module.

voltage conversion ratio of $1/N_{\text{cells}}$, depending on the number of employed converter cells N_{cells}, as also utilized in [134] for a DC/DC power supply. As already mentioned, another benefit of the ISOP structure is that the input voltage and output current are already naturally balanced among the converter cells when operated with the same control parameters (cf. **Sec. 4.2**) for the case of no mismatch between the cells.

The choice of the converter topologies for the AC/DC and the isolated DC/DC stages is an additional very basic level of degree of freedom. The selected topology of the AC/DC converter stages is a full-bridge rectifier operated with totem-pole modulation, which means that one bridge-leg of the full-bridge is operated with high frequency

whereas the other bridge-leg is switched with line frequency. The totem-pole modulation has the potential to reduce the common-mode voltage spectrum compared to bipolar or unipolar modulation schemes [118, 135]. For the isolated DC/DC converters a Phase-Shifted Full-Bridge converter (PSFB) with a secondary-side synchronous rectification for higher efficiency is selected [136]. This topology has the advantage of an easy controllability with a single control parameter (i.e phase-shift value) and of a high efficiency due to ZVS where only a small circulating energy is required [137, 138]. The drawback of the PSFB converter is the over-voltage occurring at the secondary rectifier devices due to resonances between parasitic elements such that a snubber is required, as will be addressed later on. The LLC resonant converter [139] and the dual-active bridge converter (DAB) [140] have also been considered since they also allow to achieve high efficiencies over a wide power range. However, either they require unreasonable transformer designs (e.g. a leakage inductance in the same order of magnitude as the magnetizing inductance) for the specifications at hand in the case of the LLC converter or the control implementation for minimum conduction losses [141] mandates the employment of an FPGA on each cell with a high power consumption in the case of the DAB, which renders them unfeasible for the implementation in a multi-cell system. Furthermore, the system specification also requires a current and a voltage source characteristic of the power supply, which means it has to be able to control the output voltage and to limit the output current in case of a short circuit. This requirement is fulfilled by the PSFB converter.

The above mentioned basic level of degrees of freedom are determined beforehand and are not part of the iteration in the optimization routine since this would lead to unreasonable computational and modeling efforts beyond the scope of this thesis.

The next level of degrees of freedom is the abstract level of electrical parameters (cf. **Fig. 4.7(ii)**) which define a single converter design. The most universal parameter is the

- *Number of converter cells* N_{cells}: With increasing number N_{cells} the benefits of the scaling laws of [133] and **Sec. 4.1** are leveraged to a larger extent. However, the communication overhead and the constant losses associated with each converter cell also increase. Thus, for the optimization algorithm the range for the number of cells is limited to $N_{\text{cells}} \in [3...10]$.

Additional electrical parameters which define a single converter design are associated with the AC/DC stages (including the EMI filter) and the isolated DC/DC converter stages as discussed in the following.

AC/DC Converter Stages

- *DC-link capacitance* C_{DC}: The converter system and especially the energy stored by the DC-link capacitors have to be designed for the worst case operating condition, which is given for the case of a grid outage during half a mains period (i.e. $T_{\mathrm{hold}} = 10\,\mathrm{ms}$ hold up time) when the system still has to supply the full amount of power to the load. This case inevitably leads to a voltage drop in the DC-link, depending on the overall energy stored in the DC-link. Thus, by specifying a maximum permissible drop of the DC-link voltage (i.e. $k_{\mathrm{DC,drop}} \in [10\,\%...40\,\%]$), the required capacitance value $C_{\mathrm{DC,cell}}$ of the DC-link in a cell can be determined as

$$C_{\mathrm{DC,cell}} = \frac{2 \cdot N_{\mathrm{cells}} \cdot P_{\mathrm{sys,rat}} \cdot T_{\mathrm{hold}}}{(2 - k_{\mathrm{DC,drop}}) \cdot k_{\mathrm{DC,drop}} \cdot V_{\mathrm{DC}}^2} \ . \tag{4.18}$$

- *Switching frequency* $f_{\mathrm{sw},1}$: The lower limit of the switching frequency of each cell is deduced from the audible frequency range and thus should not be lower than $f_{\mathrm{sw},1} \geq 18\,\mathrm{kHz}$. An upper boundary of the switching frequency is not inherently given; however, the CISPR EMI standards impose limits on the harmonics in the frequency range above $f_{\mathrm{EMI}} = 150\,\mathrm{kHz}$ [142]. Thus, an upper boundary of the switching frequency per cell can be derived as $f_{\mathrm{sw},1} < f_{\mathrm{EMI}}/N_{\mathrm{cells}}$ which allows to have the first harmonic below the EMI restricted frequency range.
- *Boost inductance* L_{b}: The inductance of the boost inductor depends on the specified maximum allowable current ripple $\Delta i_{\mathrm{b,max}}$ derived in (4.2) for a given number of cells and switching frequency. The maximum peak-to-peak current ripple is varied between $\Delta i_{\mathrm{b,max}} \in [5\,\%...30\,\%]$.
- *Input filter stages* N_{filt}: The input filter, which is needed to suppress harmonics such that the EMI standards are fulfilled, can be designed with different numbers of stages $N_{\mathrm{filt}} \in [1...3]$ and different filter component values

Isolated PSFB DC/DC Converters

- *Switching frequency* $f_{\mathrm{sw},2}$: The switching frequency is an important parameter for the design of the DC/DC converter as it influences the transformer design, the output inductor design and also the losses in the MOSFETs (i.e. gate driver losses). The effective frequency at the output inductor is twice the switching frequency of the full-bridge rectification. The range of the switching frequency for the optimization is set to $f_{\mathrm{sw},2} \in [50...300\,\mathrm{kHz}]$.
- *Output inductance* L_{out}: The required output inductance can be calculated for a defined switching frequency in dependency of the maximum peak-to-peak output current ripple, which is varied in the range of $\Delta I_{\mathrm{out}} \in [5\,\%...20\,\%]$.
- *Transformer turns ratio* n_{tr}: The PSFB converter is a buck-type topology which is not able to boost the output voltage beyond $V_{\mathrm{out}} = V_{\mathrm{DC,cell}} \cdot n_{\mathrm{tr}}$. Therefore, the minimum turns ratio is defined by the lowest DC-link voltage (during the hold-up time) and the maximum specified output voltage.

For a single converter design, there are still many available degrees of freedom on the component level, which are based on the various possibilities of how the physical components can be realized. Therefore, a Pareto front can be calculated for each component by sweeping through all possible combinations of a component implementation, as shown in (**Fig. 4.7(ii)**). Thus, the total Pareto front of a single converter design is obtained by combining the Pareto results of the individual components. The degrees of freedom in the component implementations are as follows:

- *MOSFETs*: For MOSFETs the technology (Si, GaN or SiC) as well as the chip size can vary for a given voltage rating. For the optimization in this paper, Si is selected due to the broad availability of devices with different chip sizes. The chip size optimization allows to trade-off conduction and switching losses and is performed in the range of $A_{\mathrm{chip}} \in [5\,\mathrm{mm}^2...30\,\mathrm{mm}^2]$. Additionally, the junction temperature can also be varied ($T_{\mathrm{j}} \in [70\,^{\circ}\mathrm{C}...110\,^{\circ}\mathrm{C}]$) which enables the trade-off between heat sink volume and conduction losses (since the switching losses show a negligible temperature dependency).

- *Magnetic components*: The magnetic components can be realized with a variety of different options. For the cores, all available E-cores and RM-cores of N87 and N97 ferrite material (TDK-EPCOS) and AMCC cores of amorphous material 2605SA1 (Metglas) are considered. For the windings, litz wires with different wire diameters and strand numbers, solid round wire and foil windings are considered. Additionally, the winding number and the length of the air-gap (in inductors) are further degrees of freedom.
- *DC-link capacitors*: The required capacitance can be realized with different numbers of paralleled electrolytic capacitors. This allows to trade-off the ESR-related losses with the leakage current losses.
- *EMI filter*: For the EMI filter ring cores with T35 and T38 ferrite material (TDK-EPCOS) with solid round wires are considered.

4.3.2 Mapping of Design Space into Performance Space

In order to map the obtained design space with all possible implementations into the performance space, detailed component loss and volume models have to be applied to the aforementioned components:

- *MOSFETs*: For performing a chip size optimization, the conduction and switching losses of the MOSFETs have to be described in dependence of the chip size A_{chip}. For the AC/DC converter, the losses have to be calculated as an average value over a mains period. The conduction losses can be calculated with the RMS current I_{RMS} of a MOSFET as

$$P_{\mathrm{MOSFET,cond}}(T_{\mathrm{jct}}, A_{\mathrm{chip}}) = I_{\mathrm{RMS}}^2 \cdot R_{\mathrm{DS,on}}(T_{\mathrm{jct}}, A_{\mathrm{chip}}) \; . \quad (4.19)$$

  In the considered current range, the on-state resistance of the low-voltage MOSFETs is basically not dependent on the conducted current.
  The switching losses of the MOSFETs of the AC/DC stage (the DC/DC converters are operated with ZVS) depend on the specific layout of the commutation loop (e.g. the parasitic loop inductance) and thus are difficult to precisely calculate. However,

a fairly good approximation can be obtained by taking into account different loss mechanisms of the switching process, such as the stored charge in the parasitic drain-source capacitances (Q_{oss}), the reverse recovery charge of the intrinsic body diodes (Q_{rr}), and the gate drive losses in dependence of the chip size [143]. The energy lost in a hard switching transition of the AC/DC stages is at least

$$E_{\mathrm{MOSFET,loss}} = V_{\mathrm{DC}} \cdot (Q_{\mathrm{oss}} + Q_{\mathrm{rr}}) + V_{\mathrm{gate}} \cdot Q_{\mathrm{gate}} \tag{4.20}$$

For the losses associated with the soft-switching transitions of the DC/DC stages it is assumed that only gate driver losses occur and C_{oss}-related losses during ZVS [144] are not considered, as they are small for low-voltage Si MOSFETs. Since the hard and soft switching losses increase and the conduction losses decrease with larger chip size, an optimal value of the chip size leading to the lowest total losses can be found. The thermal resistance of the junction to the case is also influenced by the chip size. Thus, in the last step, the required heatsink can be calculated based on the total MOSFET losses and the specified junction temperature. By considering the CSPI (cooling system performance index [145]) of different types of heatsinks or by employing a more sophisticated cooling system design approach [146], the volume of a heatsink for a MOSFET can be calculated based on the required value of thermal resistance $R_{\mathrm{Th,HS}}$. Since the PCB itself also functions as heat-spreader and helps to dissipate heat, there is no need for a heatsink if the required $R_{\mathrm{Th,HS}}$ is below a certain threshold (e.g. 50 K/W for a board with a copper area of 6 cm^2 and copper thickness of 70 µm around the switch).

- *Inductive components*: The losses of inductors and transformers can be divided into winding and core losses. The core losses (per unit volume) can be calculated for arbitrary waveforms of the flux with the improved Generalized Steinmetz Equation (iGSE) by

$$P_{\mathrm{c,iGSE}} = k_{\mathrm{i}} \cdot f_{\mathrm{sw}} \cdot (\Delta B)^{\beta-\alpha} \cdot \int_0^{1/f_{\mathrm{sw}}} \left| \frac{\mathrm{d}B}{\mathrm{d}t} \right|^{\alpha} \mathrm{d}t \tag{4.21}$$

where ΔB is the local peak-to-peak flux density and

$$k_{\mathrm{i}} = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} \, 2^{\beta-\alpha} \mathrm{d}\theta} \tag{4.22}$$

with α, β and k being the material parameters. These can be deduced from data sheets of the manufacturer or by means of loss maps based on measurement values which also allow to incorporate DC-offsets in the flux [66]. The winding losses consist of DC losses and AC current losses (skin and proximity effect) which can be calculated based on [34, 68] for different winding types. For the calculation of the proximity losses, the external magnetic field strength on each conductor has to be known. This can be determined via 1-D [147] or 2-D [67] modeling approaches or FEM simulations. A thermal impedance network [34] is applied to adequately model the heat-transfer within an inductive component and to the ambience which also impacts the losses in both the core and the windings.

- *DC-link capacitors*: The electrolytic DC-link capacitors have to carry an RMS current, which creates losses in connection with the equivalent series resistance (ESR) of the capacitors. Since the ESR is frequency dependent, the total losses are the sum of the losses at twice the fundamental frequency and at the switching frequency of the AC/DC stage. Furthermore, each capacitor exhibits a leakage current which has to be taken into account, too. The total capacitor losses can be modeled in dependency of the number of paralleled capacitors n_{par} as

$$\begin{aligned} P_{\mathrm{ELCO}} &= \frac{(I_{\mathrm{rms,100Hz}} \cdot R_{\mathrm{ESR,100Hz}} + I_{\mathrm{rms,fsw}} \cdot R_{\mathrm{ESR,fsw}})}{n_{\mathrm{par}}} \\ &+ n_{\mathrm{par}} \cdot V_{\mathrm{DC,cell}} \cdot I_{\mathrm{leak}} \ . \end{aligned} \tag{4.23}$$

  The volume of the capacitors in a single cell can be approximated with the fitting function of (2.45).

- *Input filter*: The volume of the input filter is considered in the optimization by models which translate the required filter attenuation for different numbers of filter stages into component volumes [148].

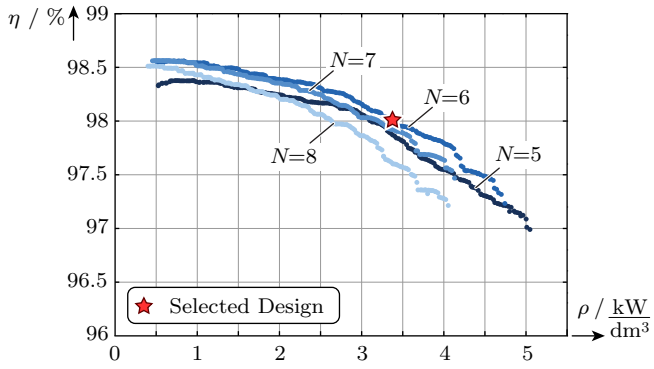

Fig. 4.8: Pareto-optimal (efficiency / power density) designs of the multi-cell telecom power supply module for different numbers of converter cells and a drop of the DC-link voltage during the hold-up time of $k_{\mathrm{DC,drop}} = 20\%$ for the operation at nominal voltages and $P_{\mathrm{out}} = 80\% \cdot P_{\mathrm{out,rat}}$.

- *Auxiliary electronics*: For the losses attributed to auxiliary electronics (e.g. a digital signal processor, voltage and current sensing) on each slave converter cell constant losses of $P_{\mathrm{slave,const}} = 800\,\mathrm{mW}$ are estimated and for the master cell constant losses of $P_{\mathrm{master,const}} = 2\,\mathrm{W}$ are considered since this cell also has to operate the precharge relay and additional sensors. It should be noted, that the constant losses change with the number of cells and therefore have an influence on the optimal number of converter cells, but for a given number of cells they do not influence the choice of Pareto-optimal designs but only reduce the achievable efficiency of all designs.

4.3.3 Optimization Results

The η-ρ Pareto-limits resulting from the optimization for the entire multi-cell converter system of **Fig. 4.1(c)** are depicted in **Fig. 4.8** for operation at $P_{\mathrm{out}} = 80\% \cdot P_{\mathrm{out,rat}}$ and nominal voltages for different numbers of converter cells and a maximum permissible drop of the DC-link voltage during the hold-up time of $k_{\mathrm{DC,drop}} = 20\%$. It can be seen that the optimum number of converter cells is $N_{\mathrm{opt}} = 6$ where a performance of $\eta = 98\%$ and $\rho = 3.3\,\mathrm{kW/dm^3}$ (calculated by summing

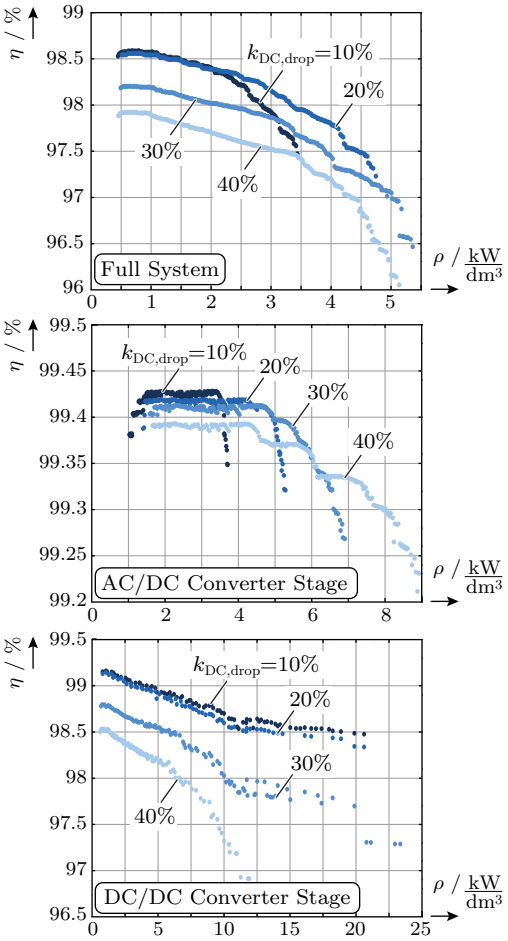

Fig. 4.9: Impact of different values of the maximum permissible drop of the DC-link voltage during the hold-up time on the achievable Pareto-optimal results of the entire system, the AC/DC converter stages and the DC/DC converter stages for $N = 6$ converter cells.

up the boxed volumes of all components, i.e. not yet considering intermediate spaces between components of different shapes and sizes) can be achieved. In a real setup, the power density typically decreases by factor of around 2/3 compared to the calculation due to spaces between the components and other mechanical constraints.

An optimum value can also be found for the maximum permissible drop of the DC-link voltage during the hold-up time. In **Fig. 4.9(a)** the Pareto-optimal results are shown for the entire system for different values of $k_{\mathrm{DC,drop}}$ for $N_{\mathrm{cells}} = N_{\mathrm{opt}} = 6$. The results are examined in greater detail in **Fig. 4.9(b)** and **Fig. 4.9(c)** which depict the individual results for the AC/DC converter stage and the DC/DC conversion stage, respectively. Based on these results an optimum value of $k_{\mathrm{DC,drop,opt}} = 20\%$ can be deduced. The trade-offs, leading to this optimal value, are described in the following:

- *AC/DC converters*: In the AC/DC converters, the value of $k_{\mathrm{DC,drop}}$ mainly influences the trade-off between the losses and the size of the electrolytic DC-link capacitors. With a larger permissible voltage drop, lower capacitance values can be used within the cells. However, since the ESR of electrolytic capacitors increases with decreasing capacitance, the losses also increase.
- *DC/DC converters*: The performance of the DC/DC converters deteriorates with larger values of $k_{\mathrm{DC,drop}}$. This is due to the fact, that the transformer turns ratio has to be adjusted according to the lowest DC-link voltage value. Thus, at the nominal operating point a lower duty cycle of the DC/DC converter is required which results in larger RMS current values in the transformer and the input full-bridge switches and therefore in higher losses if large values of $k_{\mathrm{DC,drop}}$ are chosen.

In **Fig. 4.10(a)** and **(b)** a loss and volume breakdown is provided for the selected design operating at $P_{\mathrm{out}} = 80\% \cdot P_{\mathrm{out,rat}}$ at nominal voltages. The main share of the losses is attributed to the DC/DC stages where the transformers and the output inductors account for half of the total converter losses. Regarding the volume distribution it can be deduced that half of the total converter volume consists of DC-link capacitors. The second and third largest volume contributors are the transformers and output inductors, respectively, of the DC/DC converter stages. In summary, the converter losses and volumes are dominated by the passive components, whereas the active components

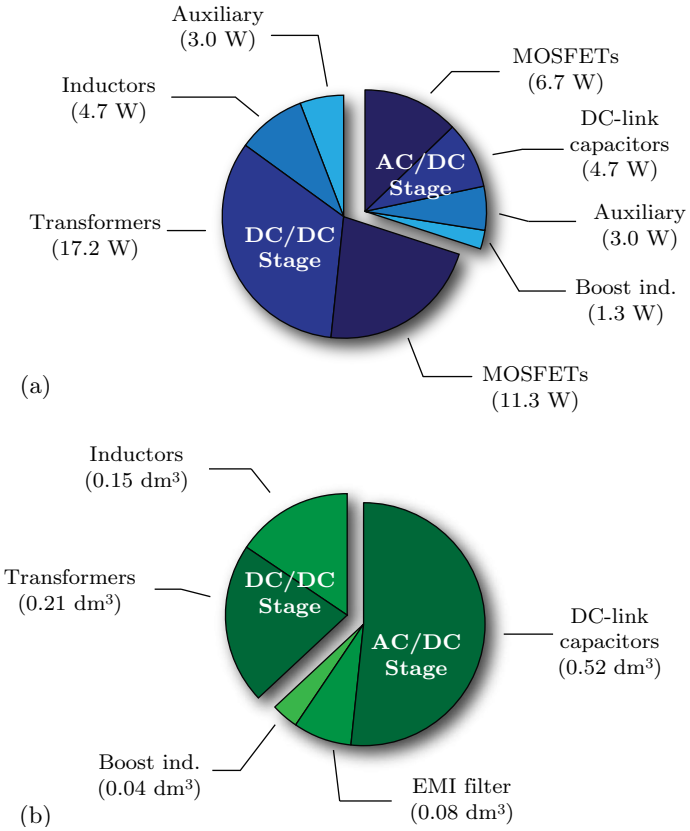

Fig. 4.10: Break-down of the losses (a) and the volume (b) for the optimized converter design of the multi-cell telecom power supply module at $P_{\text{out}} = 80\% \cdot P_{\text{out,rat}}$ at nominal voltages for $N = 6$ converter cells.

(i.e. semiconductors) contribute only around 30% of the losses and a negligible share of the overall volume due to an absence of heatsinks.

4.4 Hardware Demonstrator Design

The design, which is selected for the hardware demonstrator with a calculated maximum efficiency of $\eta = 98\%$ at 75% of the rated output power and a power density above $\rho_{\text{calc}} = 3\,\text{kW/dm}^3$, is marked in

Tab. 4.2: Main system parameters of the selected design for the hardware demonstrator with $N = 6$ converter cells. (All values given per component, e.g. parallel MOSFETs, if not otherwise noted.)

AC/DC Converter	
Switching frequency	$f_{\mathrm{sw,cell}} = 20\,\mathrm{kHz}$
Boost inductance	AMCC-4, 2605SA1, 25 µH, 7 turns
MOSFETs	2x BSC040N10NS5G, 100 V, 4.0 mΩ
DC-link cap.	4x Panasonic ECO-S1KA222CA, alum. elect., 80 V, 2.2 mF
EMI filter	3 stages, 2x common mode chokes (EPCOS R40 cores T38, 10 turns), 3x680 nF
DC/DC Converter	
Switching frequency	$f_{\mathrm{sw}} = 80\,\mathrm{kHz}$
Transformer	turns ratio 9:9, RM14, N97, EPCOS litz wire (420x71 µm)
Inductance	RM14LP, N97, EPCOS, 25 µH
Prim. MOSFETs	BSC040N10NS5G, 100 V, 4.0 mΩ
Sec. MOSFETs	BSC040N10NS5G, 100 V, 4.0 mΩ

Fig. 4.8. The main system parameters of the selected design are listed in **Tab. 4.2**. A picture of the assembled prototype is shown in **Fig. 3.34** which features a volume of $Vol = 30.4\,\mathrm{cm} \cdot 4.5\,\mathrm{cm} \cdot 11\,\mathrm{cm} = 1.504\,\mathrm{dm}^3$ and thus an overall power density of $\rho_{\mathrm{sys}} = 2.2\,\mathrm{kW/dm}^3$. The power density of the prototype is lower than the calculated value since the space between the components adversely affects the achievable power density and the volume of the PCB and the control boards have not been included in the calculations.

4.4.1 Phase-Shifted Full-Bridge Converter Design

The phase-shifted full-bridge converter (PSFB) with full-bridge synchronous rectification (SR) is chosen for the isolated DC/DC converter stage since it allows to achieve a comparably high efficiency by operating the semiconductors under zero-voltage switching (ZVS) and still provides an easy way to control the power flow by means of the phase shift between the bridge legs on the primary side at a constant switching

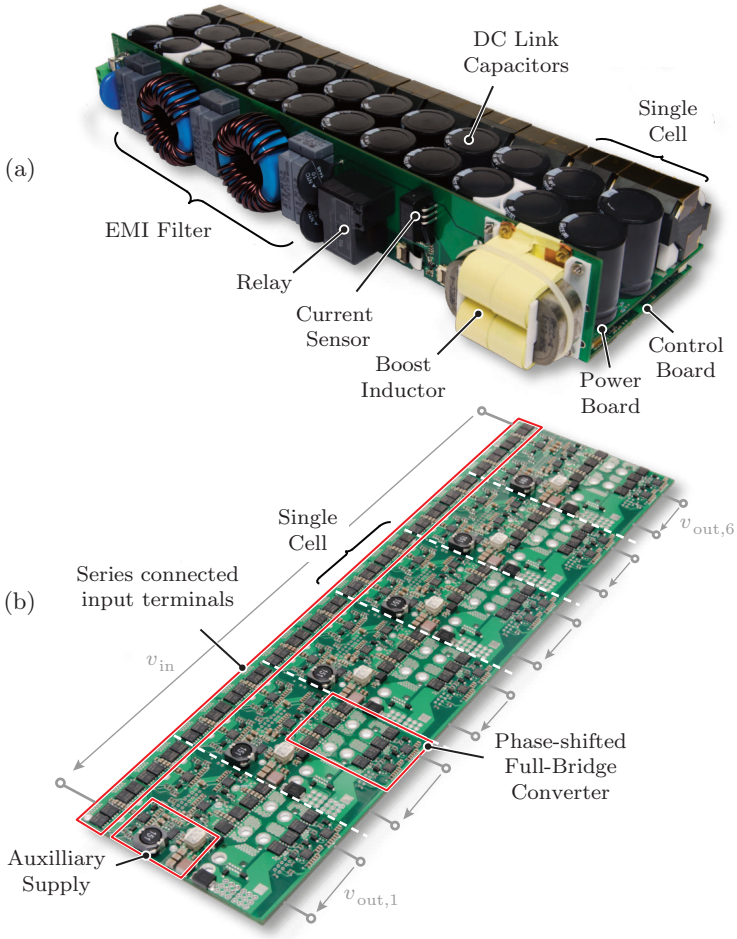

Fig. 4.11: Prototype of the multi-cell telecom rectifier with $N = 6$ converter cells according to the specification of **Tab. 4.2**: (a) full system consisting of the power board, the control board (mounted on top of the power board), and the EMI filter board with the boost inductor. The power board is shown individually in (b) for a better visualization of the ISOP interconnection of the converter cells.

frequency. For a proper operation of the converter, however, certain design guidelines have to be considered [149]. While ZVS can be achieved

for the leading leg (i.e. transition from active into freewheeling phase) of the primary side full-bridge easily by utilizing both, the energy stored in the output inductor and in the leakage inductance of the transformer, the operation of the lagging leg (i.e. transition from the freewheeling into the active phase) with ZVS relies solely on the energy stored in the leakage inductance during the freewheeling phase

$$E_{\mathrm{L}\sigma} = \frac{1}{2} L_\sigma \left(I_{\mathrm{Load}} \cdot n_{\mathrm{tr}} + I_{\mathrm{mag}} \right)^2 \ . \tag{4.24}$$

This energy has to be sufficient to charge/discharge the parasitic output capacitances of the MOSFETs in the lagging bridge leg. The energy analysis of **Appendix C** reveals, that soft-switching can only be achieved if the energy $E_{\mathrm{L}\sigma}$ is larger than the energy which is fed back into the DC input voltage during discharging of the charge-equivalent capacitance of a MOSFET, i.e.

$$E_{\mathrm{C,sw}} = C_{\mathrm{oss,Q,eq}} \cdot V_{\mathrm{DC}}^2 \ . \tag{4.25}$$

In the prototype at hand, the leakage inductance of the transformer was selected to be $L_\sigma = 1\,\mu\mathrm{H}$ by adjusting the spacing between the primary and secondary winding. This allows to achieve soft-switching in the lagging leg at levels of the output current above $I_{\mathrm{Load}} \geq 3.4\,\mathrm{A}$ (i.e. 30%) according to (4.24) and (4.25).

Increasing the leakage inductance even further for a broader range of load currents for soft-switching would introduce the drawback of a larger duty cycle loss caused by the time required to reverse the current in the leakage inductance from $(-I_{\mathrm{Load}} \cdot n_{\mathrm{trafo}})$ to $(+I_{\mathrm{Load}} \cdot n_{\mathrm{trafo}})$ or vice versa, and also to a larger ringing of the voltage at the synchronous rectification MOSFETs (as described in the following paragraph) thus rendering it an unpractical solution.

Another issue in the operation of the PSFB is the voltage ringing at the secondary rectifier MOSFETs after the freewheeling phase. The ringing is caused by the resonant circuit comprising the leakage inductance L_σ of the transformer and the parasitic capacitances of the rectifier MOSFETs ($2 \cdot C_{\mathrm{oss}}$) since the voltage across the output rectifier is decoupled by the output inductor from the output voltage and therefore not clamped to a fixed voltage (cf. **Fig. 4.12(b)**). The resonant frequency of this resonant circuit equals

$$\omega_{\mathrm{res}} = 1/\sqrt{2 C_{\mathrm{oss}} L_\sigma n_{\mathrm{tr}}^2} \tag{4.26}$$

and the characteristic impedance amounts to

$$Z_{\mathrm{res}} = \sqrt{L_\sigma n_{\mathrm{tr}}^2/(2C_{\mathrm{oss}})}\ . \tag{4.27}$$

The worst case voltage overshoot can reach a value of twice the transformed primary voltage $V_{\mathrm{SR,peak}} = 2V_{\mathrm{sec}} = 2n_{\mathrm{tr}}V_{\mathrm{DC}}$, as shown in **Fig. 4.12(d)**. In the case at hand, the DC-bus voltage in each cell equals $V_{\mathrm{DC}} = V_{\mathrm{DC,tot}}/N_{\mathrm{cells}} = 400\,\mathrm{V}/6 = 66\,\mathrm{V}$ and with a transfomer turns ratio of $n_{\mathrm{tr}} = 1$ the worst case voltage spike could reach around $V_{\mathrm{SR,peak}} = 133\,\mathrm{V}$ which would lead to the destruction of the synchronous rectification MOSFETs with a voltage rating of $V_{\mathrm{DS,max}} = 100\,\mathrm{V}$. Since the diodes in the rectifier MOSFETs are prone to reverse recovery effects, the voltage spike increases further depending on the peak reverse recovery current I_{RR} and can be calculated as

$$V_{\mathrm{SR,pk}} = V_{\mathrm{DC}}n_{\mathrm{tr}} + \sqrt{(V_{\mathrm{DC}}n_{\mathrm{tr}})^2 + (Z_{\mathrm{res}}I_{\mathrm{RR}})^2}\ . \tag{4.28}$$

In order to limit the voltage spike a loss-less snubber circuit consisting of a snubber capacitor C_{Snub} and two diodes is added to the converter [150]. An alternative snubber that works with an additional transformer winding can be found in [151]. By introducing the snubber, the equivalent circuit of the resonant network changes as shown in **Fig. 4.12(c)** and the resonant frequency becomes

$$f_{\mathrm{res,snub}} = 1/\sqrt{L_\sigma n_{\mathrm{tr}}^2(2C_{\mathrm{oss}} + C_{\mathrm{snub}})} \tag{4.29}$$

while the resonant impedance becomes

$$Z_{\mathrm{res,snub}} = \sqrt{L_\sigma n_{\mathrm{tr}}^2/(2C_{\mathrm{oss}} + C_{\mathrm{snub}})} \tag{4.30}$$

after the voltage v_{SR} has reached the level of the output voltage V_{out}. This is also depicted in **Fig. 4.12(d)** where the sudden change of the resonant impedance leads to a drop in the $v_{\mathrm{SR}} - Z \cdot i$ plane. The maximum voltage spike can then be derived as a function of the output voltage to be

$$V_{\mathrm{SR,pk,sb}} = V_{\mathrm{DC}}n_{\mathrm{tr}} + \sqrt{(V_{\mathrm{DC}}n_{\mathrm{tr}} - V_{\mathrm{out}})^2 + (Z_{\mathrm{res,snub}}I_{\mathrm{SR}})^2} \tag{4.31}$$

where the value of I_{SR} can be found through geometrical considerations in the v-Zi plane as

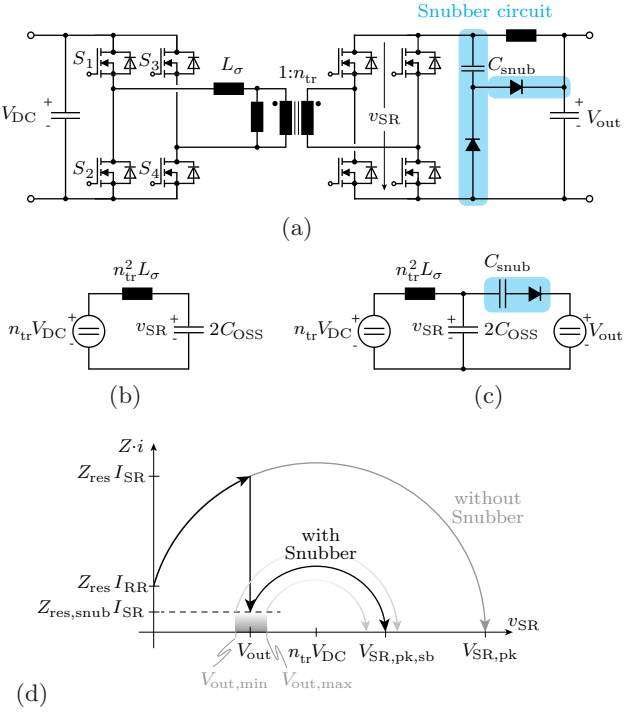

Fig. 4.12: Phase-shifted full-bridge converter with over-voltage limiting lossless snubber circuit [150] for the secondary side synchronous rectifier MOSFETs: (a) application of the snubber circuit to the converter; (b) equivalent circuit of the resonant network for the case without snubber; (c) modified resonant network for the case with snubber elements; (d) comparison of the resonant trajectories for the cases with and without snubber elements and their resulting voltage peaks $V_{SR,pk,sb}$ and $V_{SR,pk}$, respectively.

$$I_{SR} = \sqrt{R^2 - (V_{DC} n_{tr} - V_{out})^2} \tag{4.32}$$

with $R = \sqrt{I_{RR}^2 + (V_{DC} n_{tr})}$. The value of the over-voltage depends on the output voltage V_{out} in which the worst case situation is obtained for low output voltages, as indicated in **Fig. 4.12(d)**. The snubber capacitor is chosen to have a value of $C_{Snub} = 14\,\text{nF}$ which limits the worst case voltage spike at the lowest output voltage of $V_{out,min} = 40\,\text{V}$ to $V_{SR,peak,snub} = 92\,\text{V}$ without considering the influence of the reverse

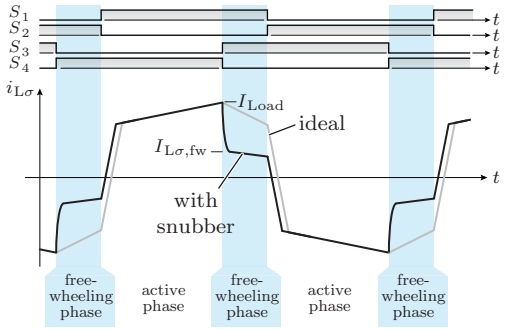

Fig. 4.13: Effect of a large snubber capacitor on the freewheeling current of the transformer leakage inductance.

recovery current. For the material of the ceramic snubber capacitors the C0G (NP0) dielectric is chosen since it provides a stable capacitance value under varying temperature and voltage. In order to minimize the reverse recovery currents of the diodes, the conduction time of the diodes in the SR MOSFETs is kept to a minimum (around 10 ns) by adjustments of the timings of the gate signals [152].

Please note, that the snubber capacitor also adversely affects (i.e. reduces) the current in the transformer leakage inductance during the freewheeling phase of the primary full-bridge (cf. **Fig. 4.13**), which is required for soft-switching of the lagging leg. In order to change from the active phase into the freewheeling phase, the snubber capacitor C_{snub} has to be completely discharged. During the discharging process, which is dependent on the output current of the converter, the voltage of the snubber capacitor is opposing the leakage inductance and reducing its current level. In case the snubber capacitor is significantly larger than the parasitic capacitances of the employed primary and secondary side MOSFETs (e.g. a factor of 10), the current value of the leakage inductance after the transition from the active phase into the freewheeling phase can be approximated as

$$I_{\text{L}\sigma,\text{FW}} = n_{\text{tr}} \cdot \left(I_{\text{Load}} - V_{\text{C,snub}} \cdot \sqrt{\frac{C_{\text{snub}}}{L_\sigma}} \right) + I_{\text{mag}} \tag{4.33}$$

by considerations of the differential equations of the resonant network of L_σ and C_{snub} with an impressed output current I_{Load} of the output

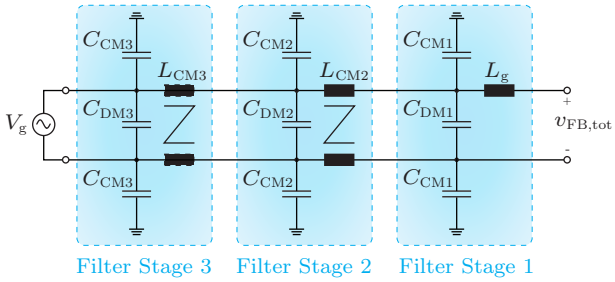

Fig. 4.14: Schematic of the employed 3-stage common-mode and differential-mode mains EMI filter.

inductor. The voltage $V_{C,snub}$ of the snubber capacitor C_{snub} can be obtained as $V_{C,snub} = V_{SR,pk,sb} - V_{out}$, based on (4.31).

The energy in the leakage inductance, which is available for soft-switching of the lagging leg, is then reduced to

$$E_{L\sigma} = \frac{1}{2} L_\sigma I^2_{L\sigma,FW} \tag{4.34}$$

which is lower than the value given for the ideal case of (4.24). This requires either to increase the leakage inductance value to obtain soft-switching at the desired output power level or to take the additional losses resulting from incomplete soft-switching into account based on **Appendix C**.

4.4.2 EMI Filter Design

For the design of the EMI filter, the influence of the differential-mode and the common-mode noise have to be considered. The filter design can be performed individually for the common-mode and the differential-mode noise if the required attentuation for each case is calculated with a margin of around 16 dB to the limits, i.e. 6 dB for the worst case addition of the two noise signals and 10 dB to account for component tolerances.

In order to calculate the required attenuation for the differential-mode noise, the first harmonic that falls into the EMI constrained spectrum ($f_{EMI} \geq 150\,kHz$) is considered, since the amplitude of the harmonic spectrum of square wave voltage decreases with 20 dB per

frequency decade, whereas the filter attenuation increases with $40 \cdot N_\mathrm{s}\,\mathrm{dB/dec}$ with N_s being the number of filter stages. For the case at hand, the first harmonic in the constrained frequency range is at twice the effective switching frequency of $f_\mathrm{sw,eff} = 120\,\mathrm{kHz}$ of the interleaved AC/DC stages, i.e. at $f_\mathrm{filt} = 240\,\mathrm{kHz}$. The compliance with EMI standards is evaluated by determining the quasi-peak emission levels of the converter. The quasi-peak voltage of the harmonic at $f_\mathrm{filt} = 240\,\mathrm{kHz}$ is calculated by considering a 9 kHz band around that harmonic and by synthesizing a time domain signal which is fed into the non-linear quasi-peak detection network [120] and results in a quasi-peak noise voltage of the converter at $f_\mathrm{filt} = 240\,\mathrm{kHz}$ of $V_\mathrm{filt,qp} = 17.2\,\mathrm{V}$ and/or a required attenuation of 92.8 dB including the margin previously mentioned. Following the filter volume optimization guidelines presented in [148] the number of filter stages for a minimum volume and its associated volume can be found at $n_\mathrm{filt} = 3$ as shown in **Fig. 4.14**. The maximum value of the total differential-mode capacitance is limited by the maximum allowable reactive power consumption of the filter. The limit was set, such that a power factor of $\cos\phi = 0.9$ can be reached above 10% of the nominal power. This leads to a total differential-mode capacitance of $C_\mathrm{DM,tot} = 2\,\mu\mathrm{F}$, which means each differential-mode capacitance amounts to $C_\mathrm{DM} = 660\,\mathrm{nF}$. This leads to differential-mode inductances of $L_\mathrm{DM} = 18\,\mu\mathrm{H}$ in order to achieve the required attenuation in combination with the boost inductor L_b.

The precise modeling of the common-mode noise is challenging since it requires the exact knowledge of the stray capacitances of all electric nodes in the converter cells to the ground. Since this is practically impossible to determine for multi-cell converter systems, an approach as presented in [153] was followed which deduces an equivalent circuit for the common-mode noise. By applying a worst-case approximation and neglecting small capacitances compared to larger ones, it can be found that due to the nature of the series connection of the converter inputs the measured common-mode voltage at the line impedance stabilization network (LISN) depends on which cell of the series stack is switching. So, for example each time the lowest cell of the series stack switches, all upper cells are also moved in respect to their potential to ground. Since the cells are operated interleaved, the common-mode voltage resembles a staircase like voltage waveform with the levels being

$$v_\mathrm{CM}(i) = \frac{N_\mathrm{cells} - i}{N_\mathrm{cells}} \cdot V_\mathrm{DC} \tag{4.35}$$

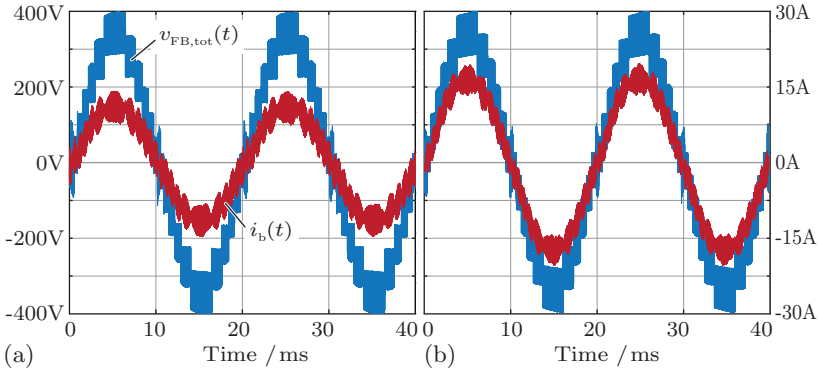

Fig. 4.15: Measured waveforms of the operation of the AC/DC stages of the multi-cell telecom rectifier with a grid voltage of $V_{\mathrm{g,RMS}} = 230\,\mathrm{V}$: (a) measurement of the converter input voltage $v_{\mathrm{FB,tot}}$ and the boost inductor current i_{b} for a load power of $P_{\mathrm{L}} = 1.5\,\mathrm{kW}$ and (b) for a load power of $P_{\mathrm{L}} = 2.5\,\mathrm{kW}$.

for $i \in [1, N_{\mathrm{cells}}]$ where $i = 1$ means that the lowest cell of the stack is switched and $i = N_{\mathrm{cells}}$ means the uppermost cell is switched. Based on that voltage waveform the quasi-peak voltage spectrum can be derived by means of simulations and the required common-mode filter attenuation can be determined to be 78 dB. The maximum allowable total common-mode filter capacitance is limited by the maximum total leakage current to earth (e.g. 3.5 mA RMS) which leads to $C_{\mathrm{CM,tot}} = 36\,\mathrm{nF}$ and thus the value for each common-mode capacitor is selected as $C_{\mathrm{CM}} = 4.7\,\mathrm{nF}$. Usually, the smallest common-mode filter volume is obtained by utilizing the maximum allowable amount of common-mode filter capacitance [154]. As a result, the common-mode inductances can be determined to be $L_{\mathrm{CM}} = 1.6\,\mathrm{mH}$. In the prototype, the leakage inductances of the common-mode chokes are utilized as differential-mode filter inductances.

4.5 Measurement Results

In order to validate the operation of the multi-cell system and the result of the optimization routine, different measurements of the hardware demonstrator are shown in this section.

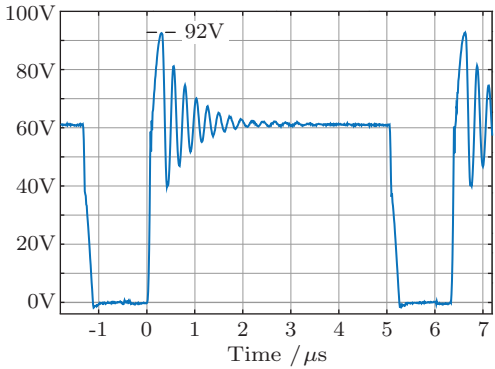

Fig. 4.16: Measurement of the voltage v_{SR} across the synchronous rectification MOSFETs of the DC/DC converter stage for an output voltage of $V_{out} = 48\,V$ and a load power of $P_L = 2.5\,kW$. The employed snubber is capable of limiting the voltage ringing to values below the maximum blocking voltage of $V_{DS,max} = 100\,V$

.

In **Fig. 4.15** the measured waveforms of the converter input voltage $v_{FB,tot}$ and the boost inductor current i_b are shown for different power levels (i.e. $P_L = 1.5\,kW$ and $P_L = 2.5\,kW$). The converter input voltage exhibits multiple voltage levels, as described in **Sec. 4.1**. The boost inductor current shows a sinusoidal shape in phase with the input voltage.

The proper operation of the over-voltage snubber (cf. **Fig. 4.12**) for the synchronous rectification MOSFETs of the phase-shifted full-bridge DC/DC converters is demonstrated in **Fig. 4.16** for an output voltage of $V_{out} = 48\,V$. The selected snubber design allows to suppress the voltage overshoot to values below the rated drain-source voltage of $V_{DS,max} = 100\,V$. Since the MOSFETs are avalanche-rated, a short spike of voltage over-shoot above the rated drain-source voltage will not lead to a destruction of the device but introduce additional losses.

The conversion efficiency of the entire system has been measured with a single-phase grid emulator (SW 5250A / ELGAR), a high-precision power analyzer (WT3000 / Yokogawa) and resistive loads. The measurement results for the full multi-cell system are depicted in **Fig. 4.17** for different output power levels P_{out}. The measurement results include all losses associated with the system, i.e. also control

losses, and the peak efficiency of $\eta_{\max} = 97.7\,\%$ is reached at an output power level of around $P_{\text{out}} = 2.25\,\text{kW}$. The measured power factor at nominal output power and nominal input voltage is $\lambda = 99.8\,\%$ and the THD of the input current is $\text{THD}_\text{I} = 4.6\,\%$.

For a more detailed analysis, the efficiency of the DC/DC stage has also been measured independently. Based on this result and the efficiency characteristic of the entire system, the efficiency of the AC/DC stage (including the EMI filter) is calculated. The measurement results of the DC/DC stage and the calculated efficiency curve of the AC/DC stage are also shown in **Fig. 4.17**.

The main deviations between the measured and the calculated efficiency (cf. **Sec. 4.3.3**) arise from non-idealities in the hardware setup, that have not been considered in the optimization:

- *PCB losses*: Even though the PCB containing the power electronic components and the EMI filter board are manufactured with a copper thickness of $d_{\text{Cu}} = 70\,\mu\text{m}$, additional conduction losses are generated. At the operating point of $P_{\text{out}} = 2.25\,\text{kW}$ these losses are estimated based on the converter layout to amount to almost $P_{\text{PCB}} = 5\,\text{W}$ for the entire converter. This results in a drop of the efficiency of around $\Delta\eta = -0.2\,\%$.
- *Thermal coupling*: Due to the dense layout of the power stage, the components are no longer thermally decoupled. This means, that e.g. the inductive components transfer heat to the MOSFETs which leads to a larger than expected junction temperature. Since the $R_{\text{DS,on}}$ of the silicon MOSFETs is strongly dependent on the junction temperature, larger MOSFET conduction losses are created. An increase of the junction temperature from $T_\text{j} = 50\,^\circ\text{C}$ to $70\,^\circ\text{C}$ results in an increase of the $R_{\text{DS,on}}$ of around 15%.
- *Magnetic coupling*: The close vicinity of the inductive components and the electrolytic capacitors and also the PCB creates eddy currents in the capacitors and the PCB, which are induced by the stray fields of the inductive components. The precise extent of this effect is difficult to quantify, though.
- *MOSFET switching losses*: For the calculation of the switching losses, the parasitic capacitances of the PCB traces connected to the switch nodes have not been considered, which also contribute to a small amount of losses. Furthermore, the dead-time of the synchronous rectifier switches has been assumed to be zero, such

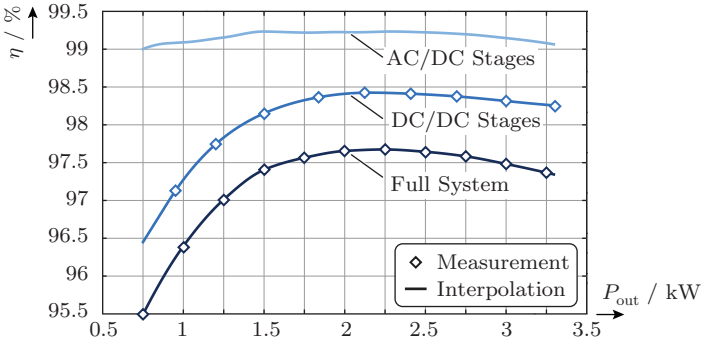

Fig. 4.17: Measurement of the conversion efficiency of the multi-cell telecom rectifier. The efficiency of the full system and the efficiency of the DC/DC stages have been measured with a power analyzer. Based on these measurements, the efficiency of the AC/DC stages was derived.

that the conduction interval of the internal body-diode of the MOSFETs is negligible.

- *Control, communication, and auxiliary electronics*: The amount of losses attributed to control and auxiliary electronics (e.g. damping resistors of the EMI filter, power relay) have only been estimated by a fixed value of losses and thus lead to an additional deviation between the calculation and the measurements.

Since the exact layout of the components and the precise design of the converter are not known at the stage of the optimization, it is very difficult to include the above mentioned loss components in a meaningful way in the optimization.

4.5.1 Challenges in the Operation of the Hardware Demonstrator

Apart from the challenges in the design of the PSFB converter, such as the load current dependent ZVS range and the voltage ringing at the synchronous rectification MOSFETs, additional issues have occured during the commissioning of the hardware demonstrator:

- *Common-mode currents*: As already mentioned in **Sec. 2.3.2** the series connection of cells leads to increased common-mode cur-

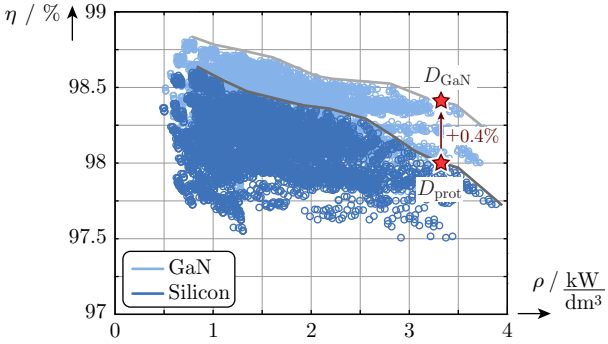

Fig. 4.18: Possible performance improvements by shifting from Si to GaN semiconductors as a result of an η-ρ Pareto optimization. The efficiency of the prototype design D_{prot} can be increased by $\Delta\eta = +0.4\%$.

rents since the potentials of the cells with reference to ground exhibits a step-change every time any other cell in the stack below changes its switching state. The change of the potential drives a current through all parasitic common-mode capacitances, which also includes the capacitances of the signal isolators. It was found that these currents disturb the SPI communication between the master and the slave cells if not properly attenuated by common-mode chokes on the signal lines. Since the communication between the master and slaves is vital for the operation of the entire system, a CRC check is implemented in order to verify that the data transmission is not corrupted. Further methods of suppressing the common-mode currents suggest the application of common-mode chokes at the input terminals of each cell [155].

- *System startup*: Due to the boost characteristic of the AC/DC stages the DC-links are charged via a precharging circuit as soon as the converter is connected to the grid. Directly after the connection to the grid, the DC/DC stages are not immediately operated which means that the system can be regarded as a stack of series-connected capacitors and does not posses the natural balancing capability at this point, which is inherent to ISOP systems. This requires some method of balancing the voltages of the DC-link capacitors until the system is in normal operation.

4.6 GaN Implementation

The multi-cell telecom power supply offers different paths for future performance improvements. One possibility is on the hardware level to shift the semiconductor technology from Si towards wide-bandgap materials such as GaN. The superior Figure-of-Merit (FOM = $1/\sqrt{R_{\mathrm{DS,on}}C_{\mathrm{oss}}}$ [55]) of GaN high electron mobility transitors (HEMTs) compared to Si MOSFETs allows to push the performance of the multi-cell system to higher levels. A multi-objective optimization (cf. **Sec. 4.3**) with GaN HEMTs (based on the $V_{\mathrm{DS}} = 100\,\mathrm{V}$ devices of EPC) reveals the achievable performance gain in case wide-bandgap semiconductors are employed. The optimization results are shown in **Fig. 4.18** and indicate that the performance of the design of the prototype system D_{prot} can be increased by $\Delta\eta = +0.4\%$ (D_{GaN}) without altering the power density.

4.7 Advanced 4D-Interleaving Control of ISOP Converters

Another possibility to improve the performance of the multi-cell system is on the software level the operation of the system with a sophisticated 4D-interleaving modulation scheme, as will be described in the following.

The multi-cell converter system with ISOP configuration itself can be considered as a spatial, i.e. 3-dimensional interleaving of multiple converter cells, where the cells are operated with a fixed operation mode and/or constant time-invariant interleaving with a common duty cycle, as described in **Sec. 4.2**. This ensures an equal voltage sharing at the series connected inputs and an equal current sharing at the parallel connected outputs of the converter cells.

However, this modulation scheme, does not take into account that the time-varying input voltage and load power in addition to the presence of large DC-link capacitors provide additional degrees of freedom for the operation of the system. These degrees of freedom allow to introduce a 4^{th} dimension (4D) of interleaving the converter cells, where the operation mode (e.g. PWM vs. fundamental frequency modulation) and/or the number of active cells is varied over time - hence the denomination of 4D. Depending on the input voltage and output power,

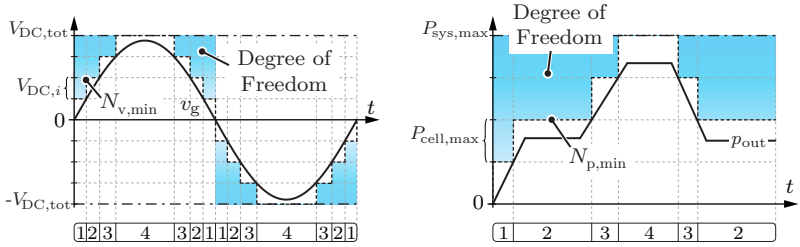

Fig. 4.19: 4D interleaving concept for the ISOP multi-cell telecom power supply module. The available degrees of freedom in the operation of the system arise from the fact, that for each operating point of input voltage and output power only a certain minimum number of active AC/DC and DC/DC converter stages - $N_{v,min}$ and $N_{p,min}$ - is required. Any number of stages between the minimum and the maximum available number of cells can be operated as shown in **(a)** for the AC/DC and in **(b)** for the DC/DC stages. Furthermore, the number of active cells can be different for both stages, as the DC-link capacitors employed in the cells decouple the instantaneous power flow between the input and the output stages.

the number of active rectifier stages and output stages can vary over time as long as the following three conditions are fulfilled:

- *Input voltage*: At any given time the AC/DC converter stages have to provide a voltage $v_{FB,tot}(t)$ which is defined by the grid voltage, i.e. $v_g(t) \approx \overline{v}_{FB,tot}(t)$ over a switching period, where $\overline{v}_{FB,tot}(t) = \sum_{i=1}^{N_{cells}} \overline{v}_{FB,i}(t) = \sum_{i=1}^{N_{cells}} V_{DC,i} \cdot m_i(t)$ with m_i denoting the modulation index of a cell. This allows to derive a minimum number of active rectifier stages $N_{v,min}$ that are required for the operation of the system: $N_{v,min} = \left\lceil \frac{v_g(t)}{V_{DC,i}} \right\rceil$ (cf. **Fig. 4.19(a)**).
- *Output current*: The total output current $i_{out,tot}(t)$ which is provided by the parallel connected DC/DC converters has to be equal to the load current, i.e. $i_{load}(t) = i_{out,tot}(t) = \sum_{i=1}^{N_{cells}} i_{out,i}(t)$. Since each converter cell has a maximum power and current rating $I_{DC/DC,max}$, a minimum number $N_{p,min}$ of converter cells required for the power transfer can be derived as $N_{p,min} = \lceil \frac{i_{load}(t)}{I_{DC/DC,max}} \rceil$ (cf. **Fig. 4.19(c)**).
- *DC link capacitors*: The DC-link capacitance is typically sized

for a hold-up time requirement. Therefore, especially at low-power levels, this capacitance allows to have a power flow of the AC/DC converter stages that is different from the power flow of the DC/DC converters. The difference in the power flow is then stored in or supplied by the DC-link capacitors. This means, that the number of active AC/DC converter stages $N_{\mathrm{v,op}}$ at a given time can be different from the number of active DC/DC converter stages $N_{\mathrm{p,op}}$, as long as the net power flow of the DC-link capacitors of each cell is zero over a certain time interval, e.g. some milliseconds.

Based on the above mentioned degrees of freedom, a selection of modulation schemes making use of the 4^{th} dimension of interleaving is presented in the following paragraphs.

4D-Modulation of the AC/DC Converter Input Stages

The total sinusoidal cell input voltage $v_{\mathrm{FB,tot}}$ can be distributed among the AC/DC converter stages in different ways. Apart from the number of active modules ($N_{\mathrm{v,op}} \in [N_{\mathrm{v,min}}, N_{\mathrm{cells}}]$) the mode of operation of each active module can also be chosen. Namely, an active module can be either operated with PWM modulation or with fundamental frequency modulation (ON-OFF). Based on these degrees of freedom, two essentially different modulations schemes can be identified:

- *Variable number of PWM cells*: In this modulation scheme only the minimum number $N_{\mathrm{v,op}} = N_{\mathrm{v,min}}$ of required cells is operated with PWM while the remaining cells are turned off, as shown in **Fig. 4.20(a)**. This means, that the number of active cells $N_{\mathrm{v,op}}$ changes with the time-varying value of the grid voltage. All active cells are operated with a fixed frequency PWM, i.e. $N_{\mathrm{PWM}} = N_{\mathrm{v,op}}$, with the same modulation index and a phase shift between the cells which depends on the number of active cells, $\phi = 360°/N_{\mathrm{PWM}}$. This leads to a varying effective switching frequency due to the varying number of active cells. In order to limit the difference between the maximum and minimum effective switching frequency, a lower limit for the number of active PWM cells $N_{\mathrm{PWM,min}}$ can be defined.
- *Fixed number of PWM cells*: Instead of changing the number of PWM cells during a grid cycle, this modulation scheme operates

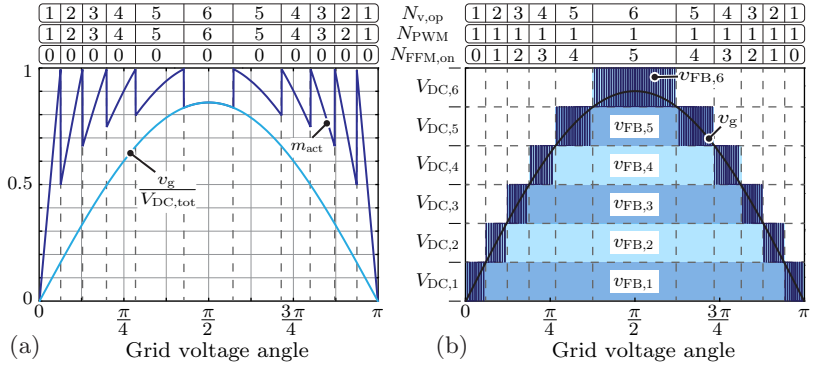

Fig. 4.20: Examples of the 4D-interleaving concepts for the series connected AC/DC converter stages: (a) operation with a variable number of PWM modules where all active rectifier stages ($N_{v,op}$) are operated with PWM with the same modulation index m_{act}. The minimum number of active PWM stages is set to $N_{PWM,min} = 1$; (b) operation with a fixed number of PWM stages (i.e. $N_{PWM} = 1$) where the remaining cells are operated with fundamental frequency and are either turned on or off ($N_{FFM,on} = N_{v,op} - N_{PWM}$).

with a defined number of PWM cells at all times ($N_{PWM} = \text{const}$), as depicted in **Fig. 4.20(b)** for the case of a single PWM cell ($N_{PWM} = 1$). The remaining cells are operated with fundamental frequency which means that they are either turned on or off ($N_{FFM,on} = N_{v,op} - N_{PWM}$). As a result, in this operation mode only a fixed number of cells (N_{PWM}) exhibits switching losses, whereas the other cells only have conduction losses. A disadvantage, however, is the reduced effective switching frequency which requires an increase of the boost inductance value in order to limit the peak-to-peak ripple of the input current.

For all of the above cases, the instantaneous cell power values are unequal and the individual DC-link capacitor voltages inherently fluctuate. Thus, it is required to properly permute the operation of the cells, e.g. by cyclically changing the selection of PWM cells. Especially, in order to achieve an accurate cancellation of harmonics by interleaving multiple PWM cells, the DC-link voltages of these PWM cells should be kept as close as possible to the same value.

4D-Modulation of the DC/DC Converter Output Stages

Similarly to the voltage distribution among the input side series connected AC/DC converter stages the output current can be distributed in different ways among the parallel connected DC/DC converter output stages:

- *Equal current sharing*: The number of active DC/DC stages varies depending on the output current. All cells are operated with the same current reference value and therefore equally share the output current. The current reference of a single cell can be calculated by dividing the total output current by the number of active cells. As a drawback, however, the current reference of each cell will exhibit a step change every time the number of active cells changes, which requires a highly dynamic current controller in each cell.
- *Unequal current sharing*: In this modulation scheme the output current is unequally divided among the active cells. This might be achieved e.g. if an additional cell is only activated when the previously actived cell has reached its maximum current value. This has the advantage that the current reference values of all cells are continuously changed over time without any step changes (under the assumption that there are no load steps). As a drawback, the stress on the DC-link capacitors is heavily unbalanced as some cells operate at their maximum power levels while others are in stand-by mode.

A minimum number of DC/DC converter stages can be defined to reduce the total current ripple at the output by interleaving the active DC/DC converter stages. This can be applied to both concepts, since the current ripple at the output of an individual cell is independent from the current level of the cell (i.e. the average value of the output current). Thus, even the interleaving of two cells with unequal current sharing reduces the output current ripple.

4.7.1 Simulation and Optimization Results

In this section the aforementioned different 4D-interleaving modulation schemes are comparatively evaluated in order to identify the best possible modulation scheme for the AC/DC and the DC/DC converter

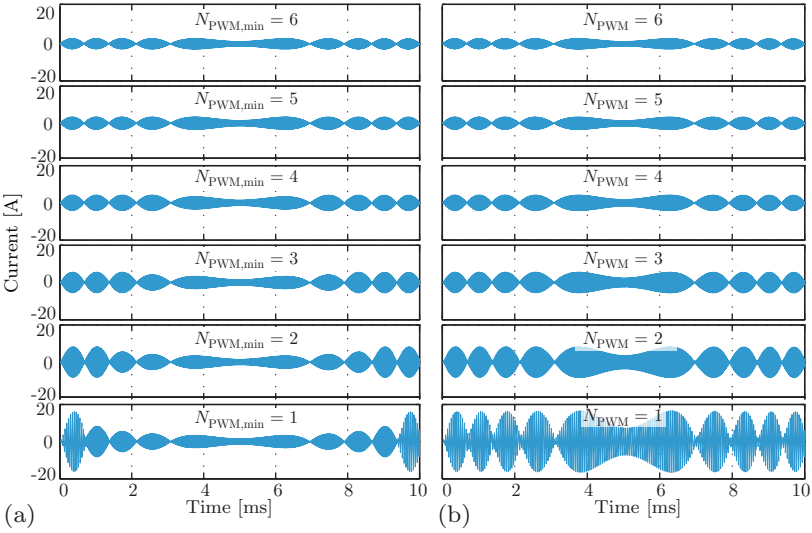

Fig. 4.21: Comparison of simulated boost inductor current ripple waveforms (i.e. current i_{b} without the 50 Hz low frequency component) for different 4D-interleaving schemes: (a) variable number of PWM modules ($N_{\mathrm{PWM,min}}$ denotes the minimum number of active PWM modules); (b) fixed numbers N_{PWM} of PWM modules where the remaining cells are operated as fundamental frequency modules. (System with 6 cells and a switching frequency of the PWM cells of $f_{\mathrm{sw,PWM}} = 20\,\mathrm{kHz}$, a boost inductance of $L_{\mathrm{b}} = 25\,\mu\mathrm{H}$, and a DC-link voltage of each cell of $V_{\mathrm{DC,cell}} = 66\,\mathrm{V}$.)

stages. In the following, the 4D-interleaving modulation schemes are analyzed for the ISOP multi-cell telecom power supply module with $N_{\mathrm{cells}} = 6$ converter cells where each cell has a rated power level of $P_{\mathrm{rat}} = 550\,\mathrm{W}$ and a DC-link capacitance of $C_{\mathrm{DC}} = 8.8\,\mathrm{mF}$ with a nominal DC-link voltage of $V_{\mathrm{DC,cell}} = 66\,\mathrm{V}$.

AC/DC Converter Stages

The modulation scheme of the AC/DC stages takes direct influence on the harmonic spectrum of the input current waveform, the RMS value of the input current, and also on the total switching losses. The effect of the selected modulation scheme on the input current waveform is shown for both modulation schemes (variable and fixed numbers of

PWM cells) in **Fig. 4.21** for two selected scenarios. The modulation with a variable number of PWM modules and a value of $N_{\mathrm{PWM,min}} = 6$ is equal to the operation with a fixed number of $N_{\mathrm{PWM}} = 6$ cells which is the standard 3D interleaving operation as measured in **Fig. 3.35(b)**.

The harmonic spectrum of the generated converter input voltage is shown for both of the aforementioned modulation schemes in **Fig. 4.22**. It can be seen that the modulation with the variable number of PWM modules (**Fig. 4.22(a)**) leads to a more even distribution of the switching frequency harmonics over the frequency range, due to its varying effective switching frequency.

As a remark, for the generation of the plots in **Fig. 4.21** and **Fig. 4.22** the DC/DC stages were operated with conventional (3D) modulation where all stages are activated and equally share the total output power.

Since the choice of the modulation scheme affects several system parameters, a comprehensive optimization of the entire input stage comprising the EMI filter, the boost inductor and the MOSFET chip area of the AC/DC full bridges has to be performed to take into account the dependencies between the different elements and the modulation schemes. This optimization allows to identify the Pareto-limit of the trade-off between efficiency and power density of the entire rectification stage by considering all available degrees of freedom given for the design:

- *EMI Filter*: Regardless of the selected modulation scheme, the system has to comply with the CISPR Class B directive which specifies limits for the conducted noise emissions in the frequency range of $f_{\mathrm{CISPR}} = 150\,\mathrm{kHz} - 30\,\mathrm{MHz}$. This requires the calculation of the harmonic spectrum for each modulation scheme and the identification of the Pareto-optimal filter designs which can be found by considering different degrees of freedom like the number of filter stages and the choice of different values for the filter elements.
- *Boost Inductor*: The value of the boost inductance is another optimization parameter since a small value leads to a large input current ripple which increases the RMS value and also the losses of the inductor and conduction losses of the MOSFETs. However, a large current ripple also results in lower switching losses of the MOSFETs as the hard-switching instants occur at lower current levels. In addition, the design of the boost inductor represents a

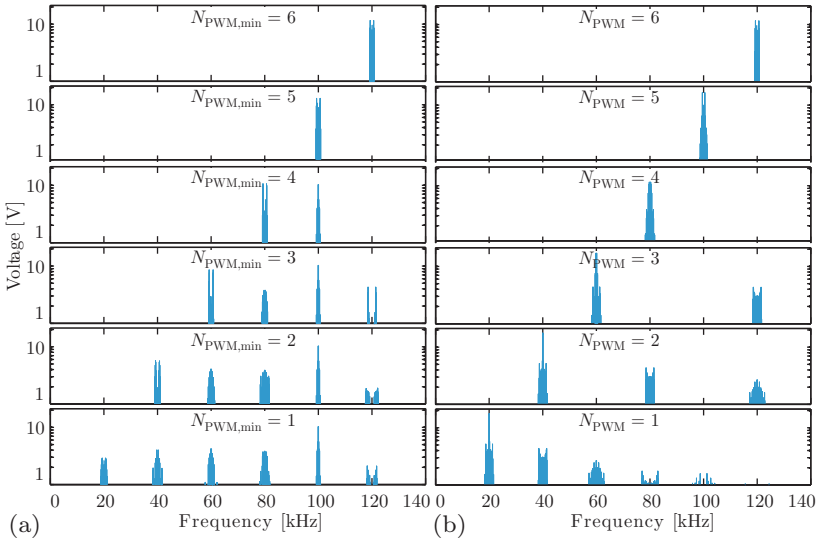

Fig. 4.22: Comparison of the harmonic spectrum of the input voltage $v_{\mathrm{FB,tot}}$ of the series connection of AC/DC converter cells (without the 50 Hz low-frequency component) for different 4D-interleaving schemes: (a) variable number of PWM modules ($N_{\mathrm{PWM,min}}$ denotes the minimum number of active PWM modules); (b) fixed numbers of PWM modules N_{PWM} where the remaining cells are operated as fundamental frequency modules. (System with 6 cells and a switching frequency of the PWM cells of $f_{\mathrm{sw,PWM}} = 20\,\mathrm{kHz}$ and a DC-link voltage of each cell of $V_{\mathrm{DC,cell}} = 66\,\mathrm{V}$.)

Pareto-optimization problem by itself as for a given set of electrical parameters different inductor designs can be found due to the possibility of employing e.g. different types of core material, core shapes, winding types (e.g. litz or foil windings), number of turns and air gap lengths.

- *Switching Frequency*: The switching frequency directly impacts the switching losses but also the shape of the input current for a given boost inductance. This also has an effect on the inductor design and the EMI filter design. Regarding the MOSFETs, a high switching frequency leads to larger switching losses but to a lower current ripple and thus to a lower current RMS value which decreases the conduction losses.

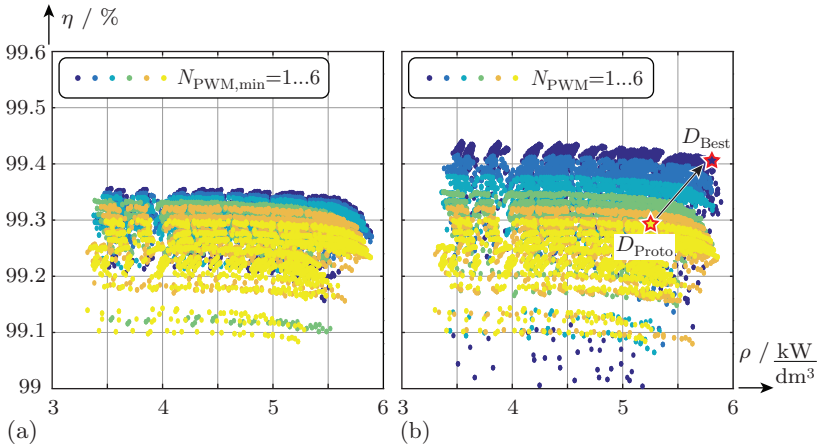

Fig. 4.23: η-ρ efficiency vs. power density Pareto-optimization results of the entire rectification stage (including EMI filter, boost inductor, AC/DC full bridges, and DC-link capacitors): (a) Performance trade-off with a variable number of PWM cells for different minimum numbers $N_{\mathrm{PWM,min}}$ of PWM cells, and (b) performance space for a fixed number N_{PWM} of PWM cells where the remaining cells are operated with fundamental frequency modulation. Compared to a conventional approach employed in the prototype system (D_{Proto}, $N_{\mathrm{PWM}} = 6$) a selected design on the Pareto-front (D_{Best}, $N_{\mathrm{PWM}} = 1$) shows 10% lower total volume and 17% lower losses.

- *MOSFET Chip Areas*: The chip area selection of the MOSFETs allows to trade-off conduction losses which decrease with a larger chip area and hard-switching (turn-on) losses, which increase with a larger chip area.

The results of the Pareto-optimization of the entire rectification stage, including the EMI filter, boost inductor, full-bridge MOSFETs of the AC/DC stages, DC-link capacitors (selected for a hold-up time of $t_{\mathrm{holdup}} = 10\,\mathrm{ms}$), resistive PCB losses, and constant control losses, for operation at rated power ($P_{\mathrm{rat}} = 3.3\,\mathrm{kW}$) are plotted in **Fig. 4.23(a)** and **4.23(b)** for the modulation scheme with a variable number of PWM modules and the modulation scheme with a fixed number N_{PWM} of PWM modules, respectively. It can be concluded that the highest performance can be achieved by operating only one cell with PWM and the remaining cells with fundamental frequency modulation. Com-

pared to the design of the hardware demonstrator (D_{Proto}) [156] with a continuous operation of $N_{\mathrm{PWM}} = 6$ cells, the 4D-interleaving concept allows to simultaneously improve the efficiency and the power density of the rectification stage; the losses are reduced by 17% and the volume by 10%, as shown for design D_{Best} in **Fig. 4.23(b)**. More details about both designs can be found in **Tab. 4.3**.

DC/DC Converter Stages

For the parallel connected DC/DC converter stages the most efficient 4D-interleaving modulation scheme can be analytically derived by assuming a generic loss function of each DC/DC converter depending on the output power as

$$p_{\mathrm{loss},i} = k_0 + k_1 \cdot p_{\mathrm{out},i} + k_2 \cdot p_{\mathrm{out},i}^2 \tag{4.36}$$

where k_0 models the constant losses (e.g. auxiliary power), $k_1 \cdot p_{\mathrm{out},i}$ the linearly output power dependent losses (e.g. a diode voltage drop) and $k_2 \cdot p_{\mathrm{out},i}^2$ the quadratically dependent losses (e.g. resistive losses). The total losses of the DC/DC converter stage comprising N DC/DC converters can thus be written as

$$p_{\mathrm{losses,tot}} = N \cdot k_0 + k_1 \cdot \sum_{i=1}^{N} p_{\mathrm{out},i} + k_2 \cdot \sum_{i=1}^{N} p_{\mathrm{out},i}^2 \ . \tag{4.37}$$

By applying the Lagrangian method to the minimization problem of (4.37) under the constraint of $p_{\mathrm{out,tot}}(t) = \sum_{i=1}^{N_{\mathrm{cells}}} p_{\mathrm{out},i}(t)$ the solution for the general case is

Tab. 4.3: Comparison of the parameters of the AC/DC converter stages of the prototype design D_{Proto} and the Pareto-optimal 4D-interleaving design D_{Best} (cf. Fig. 4.23).

Variable	D_{Proto}	D_{Best}
N_{PWM}	6	1
$f_{\mathrm{sw,PWM}}$	20 kHz	24 kHz
L_{b}	25 µH	90 µH
EMI Filter Stages	3	3
Parallel MOSFETs	2	5

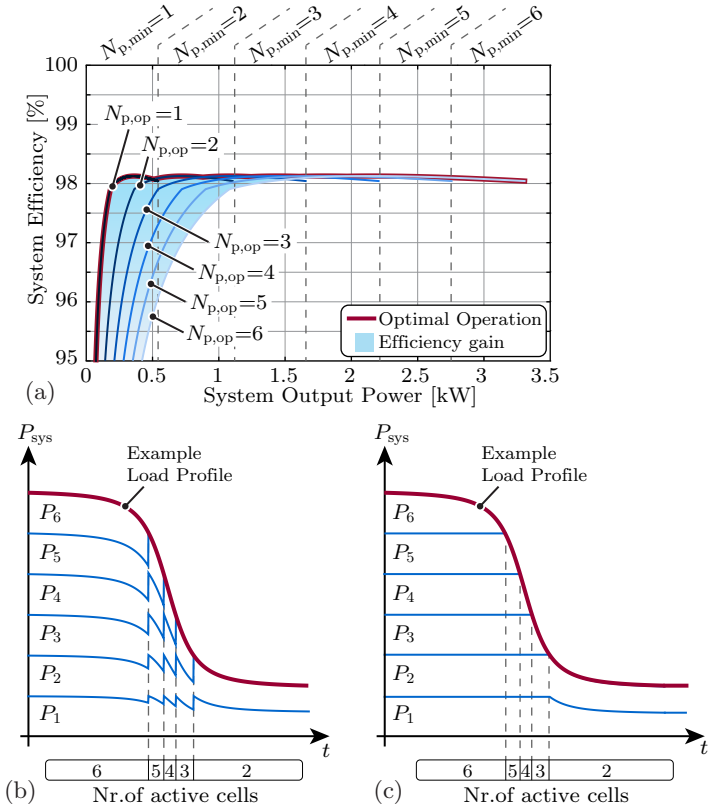

Fig. 4.24: 4D-interleaving of the parallel connected DC/DC converter stages of an ISOP system with $N_{cells} = 6$ converter cells which leads to a higher part-load efficiency (cf. (a)) by always operating only a subset of converter cells. (b) Operation mode with equal power reference values for all active cells, which results in discontinuous changes of the power levels of the individual active cells. (c) Alternative operation with unequal power levels of the converter cells but smooth changes of the power levels of the individual cells.

$$p_{out,1,opt} = p_{out,2,opt} = ... = p_{out,N,opt} = \frac{p_{out,tot}}{N} \ , \tag{4.38}$$

under which the total losses are minimized. By inserting the solution of (4.38) in (4.37) the total losses can be calculated as

$$p_{\text{losses,tot}} = N \cdot k_0 + k_1 \cdot p_{\text{out,tot}} + k_2 \cdot \frac{p_{\text{out,tot}}^2}{N} \ . \tag{4.39}$$

The remaining optimization parameter is the optimum number of active DC/DC converters $N = N_{\text{opt}} \in [N_{\text{p,min}}, N_{\text{cells}}]$ used for the power transfer for maximum efficiency. By differentiating (4.39) with respect to N and setting the derivative equal to zero, the optimal number of active cells can be found as

$$N_{\text{opt}} = \sqrt{\frac{k_2}{k_0}} \cdot p_{\text{out,tot}} \ . \tag{4.40}$$

Since the number N_{opt} is typically a rational number, the two nearest integer values have to be considered and the integer value which still satisfies $N_{\text{opt,int}} \in [N_{\text{p,min}}, N_{\text{cells}}]$ and leads to lower losses according to (4.39) has to be considered. If none of the nearest integer values satisfies the condition of $N_{\text{opt,int}} \in [N_{\text{p,min}}, N_{\text{cells}}]$ (typically for systems with larger constant losses than quadratic losses, i.e. $k_0 \gg k_2$), the value of $N_{\text{opt,int}} = N_{\text{p,min}}$ has to be chosen.

As a conclusion, this means, that the most efficient 4D-interleaving modulation scheme for the parallel connected DC/DC stages is obtained by equally sharing the total power and/or the total output current among the active DC/DC cells. This allows to extend the level of highest efficiency also to very low power levels as shown in **Fig. 4.24(a)** for the multi-cell telecom rectifier of **Fig. 3.35(a)**. Compared to the standard modulation where all six DC/DC stages are operated at all power levels, significant efficiency gains can be achieved at power levels below 30% of the rated power $P_{\text{rat,tot}}$.

In order to avoid step changes of the power reference values of the cells every time the number of cells changes (cf. **Fig. 4.24(b)**) it is preferable to allow unequal reference values in load changing intervals (cf. **Fig. 4.24(c)**).

4.7.2 DC-Link Voltage Balancing

The 4D-interleaving modulation schemes lead to an unequal stress of the DC-link capacitors since, on the one hand, at low input voltage and/or output power only a fraction of the AC/DC stages and DC/DC stages is active at a given time and, on the other hand, the number $N_{\text{v,op}}$ of active AC/DC input stages can be different from the number

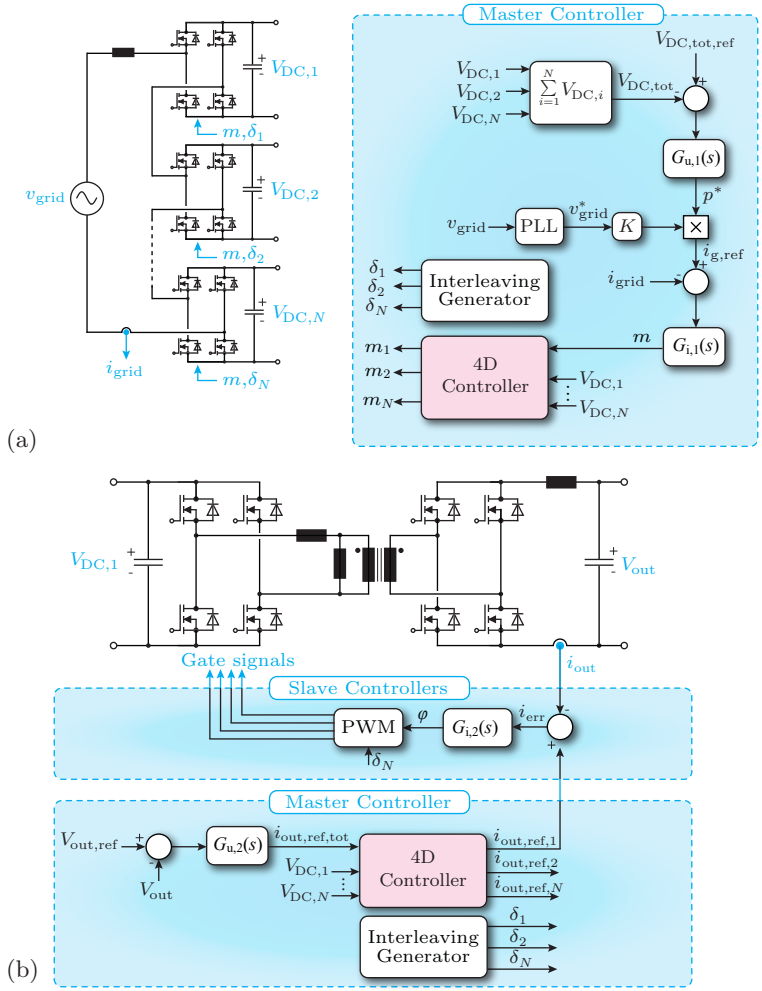

Fig. 4.25: Implementation of the 4D-controller in the existing control loops of the multi-cell system as shown in **Fig. 4.6**.

$N_{p,op}$ of active DC/DC output stages. Thus, in order to balance the DC-link voltages during the operation with 4D-interleaving, a proper permutation algorithm has to be employed which activates/deactivates the AC/DC and DC/DC stages of the cells in such way that a minimal

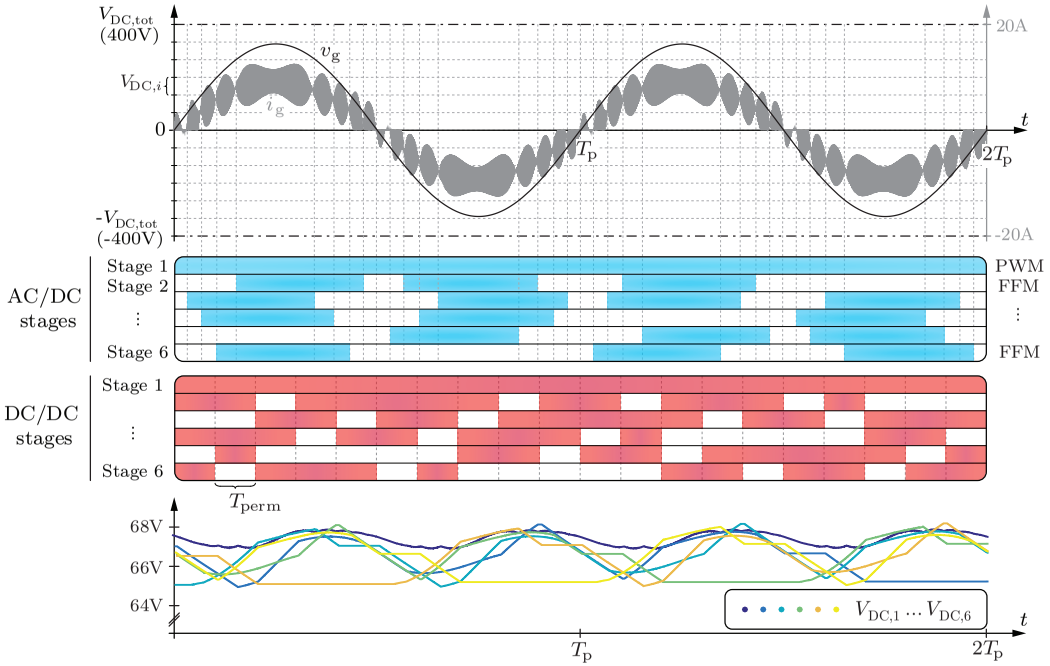

Fig. 4.26: Simulation results of the 4D-interleaving modulation of the ISOP multi-cell telecom rectifier system with $N_{cells} = 6$ at the operating point of $P_{out} = 1.5\,kW$. At the input side only one AC/DC stage (Stage 1) is modulated with PWM while the remaining five stages are operated with fundamental frequency modulation (FFM). At the selected power level of $P_{out} = 1.5\,kW$ the most efficient operation of the DC/DC stages is achieved with $N_{p,op} = 4$ active DC/DC stages. The balancing algorithm selects the active AC/DC and DC/DC stages based on the DC-link voltages of the cells. The permutation time interval for the DC/DC stages is chosen as $T_{perm} = 2\,ms$.

voltage ripple on the DC-link capacitors is obtained. This necessitates that the 4D-controller is implemented in the master cell, as shown in **Fig. 4.25**. For the AC/DC stages the 4D-controller is added to the existing control structure (cf. **Fig. 4.6**) and receives the calculated modulation index m. Based on that and the actual DC-link voltages, the individual modulations indices $m_1 ... m_N$ are determined. Regarding the DC/DC stages, the control loop of the slave controllers is slightly adjusted, since the individual DC-link voltage balancing loops are no longer required. Again, the master cell determines the individual reference output currents $i_{\mathrm{out,ref,1}} ... i_{\mathrm{out,ref,2}}$ based on the required total output current $i_{\mathrm{out,ref,tot}}$ and the DC-link values of all cells.

One possible permutation algorithm for the AC/DC stages is described below for a system with $N_{\mathrm{cells}} = 6$ converter cells and a fixed number of $N_{\mathrm{PWM}} = 1$ PWM AC/DC stages and $N_{\mathrm{FFM}} = 5$ AC/DC stages with fundamental frequency modulation (FFM). In contrast to the balancing scheme proposed in [128], the AC/DC stage which is selected for PWM operation is always the uppermost cell in the stack of converter cells, i.e the cell which is connected to the input side boost inductor L_{b}, since this minimizes the common-mode currents in the system caused by the switching operation of the PWM cell. The proposed permutation algorithm works in such way, that an additional FFM AC/DC stage is activated every time the modulation index of the PWM cell reaches its upper limit and is deactivated when the lower limit of the modulation index of the PWM stage is reached, similar to the concept shown in **Fig. 4.20(b)**. The decision about which FFM AC/DC stage to activate/deactivate is based on the deviation of the DC-link voltages of the cells from the set-point voltage ($V_{\mathrm{DC,set}} = 400\,\mathrm{V}/N_{\mathrm{cells}}$) in such a way that the AC/DC stage of the cell with the lowest DC-link voltage is always the next one to be activated and the AC/DC stage of the cell with the highest voltage is the next one to be deactivated.

Apart from the AC/DC stages of the cells the DC/DC stages can also be utilized for DC-link voltage balancing by means of permutation. For a system which operates at a constant power level, however, there is no natural event when DC/DC stages have to be activated/deactivated like there is for the AC/DC stages, due to the time-varying input voltage. Thus, a constant time interval of e.g. $T_{\mathrm{perm}} = 2\,\mathrm{ms}$ is chosen after which the selection of active stages is re-evaluated based on the DC-link voltage values of the cells. This means, that the DC/DC stages of the $N_{\mathrm{p,op}}$ cells with the highest DC-link voltages are activated.

Consequently, the balancing of the DC-link voltage is achieved by permutation of the active AC/DC and DC/DC stages, which is shown in **Fig. 4.26** for the operation at a constant output power level of $P_{\mathrm{out,tot}} = 1.5\,\mathrm{kW}$ where the most efficient operation is achieved with $N_{\mathrm{p,op}} = 4$ active DC/DC stages. As can be seen, the ISOP system can be operated in a stable condition with 4D-interleaving at the AC/DC and DC/DC stages while the DC-link voltages are effectively balanced with only small deviations of around a maximum of $\Delta V_{\mathrm{DC}} \approx 3\,\mathrm{V}$.

4.8 Summary and Conclusion

In this chapter, a new approach towards a highly efficient and very compact single-phase telecom recitifier module is presented. The system is based on the multi-cell converter approach with a series connection of the cells at the input and a parallel connection of the cells at the output (ISOP). Each converter cell employs an AC/DC converter stage, which consists of a full-bridge and an isolated DC/DC converter, which is made up of a phase-shifted full-bridge DC/DC converter.

Based on fundamental scaling laws, the benefits of a multi-cell converter system are derived in comparison to a single-cell AC/DC converter system. As a result from the increased effective switching frequency and the multi-level voltage waveform, due to the interleaving of the series-connected AC/DC stages, the ripple of the boost inductor current is greatly reduced and a cancellation of harmonics occurs.

The degrees of freedom in the design procedure of the multi-cell telecom power supply module in ISOP configuration are outlined. Based on the degrees of freedom in the converter design, a multi-objective optimization is performed, which allows to map each converter design into the performance space by use of analytical component loss and volume models. The optimization results show, that a converter design with an efficiency of $\eta = 98\%$ and a power density of $\rho = 3.3\,\mathrm{kW/dm^3}$ can be achieved. The results also reveal an optimum value of $N_{\mathrm{cells}} = 6$ for the number of converter cells and an optimum maximum permissible drop of 20% of the DC-link voltage during the hold-up time.

In order to validate the theoretical aspects of the multi-cell converter operation and the optimization results, a prototype system is designed and built up. Different critical design aspects like the ZVS conditions and the snubber design of the DC/DC converter stage are analyzed in detail. The measurement results confirm the optimization results and

show that this converter concept can achieve a very high conversion efficiency. Additionally, several pitfalls and challenges in the operation and commissioning of the converter are highlighted.

The overall control of the ISOP multi-cell system is described with a master-slave control concept. In addition to this state-of-the-art control concept, a novel 4D-interleaving control concept is introduced. The proposed concept is based on a time-varying activation/deactivation of individual AC/DC input and DC/DC output stages of different cells and utilizes the decoupling of the input and output sides of the cells provided by the energy storage capability of the DC-link capacitors. Different 4D-interleaving operation schemes are discussed for the series connected AC/DC stages and the parallel connected DC/DC stages and evaluated by means of a comprehensive η-ρ Pareto optimization and analytical calculations. Compared to the standard 3D-interleaving, the losses of the entire rectifier stage can be reduced by 17% and the volume can be decreased by 10% and a very flat efficiency vs. output power characteristic of the parallel connected DC/DC converter stages can be achieved.

Considering the increasing importance of high efficiency telecom power supplies, also in the part-load operation range, the multi-cell converter approach in combination with the proposed 4D-interleaving concept therefore provides an interesting solution for future implementations.

Furthermore, the degrees of freedom in the operation of multi-cell systems in general and the ISOP converter in particular are discussed. Based on these degrees of freedom, different new control concepts are presented which allow for an optimal operation of the converter system as will be theoretically and experimentally verified in the course of future research.

5

Multi-Cell Auxiliary Power Supply with High Step-Down Ratio

STATE-OF-THE-ART electronic systems do not only comprise power electronic components but also auxiliary electronics such as digital signal processors, measurement electronics required for the control of the entire system and gate drivers. These parts of the system usually require a low DC supply voltage (e.g. 3.3 V for a DSP) and their combined power consumption often lies in the low double-digit Watts range. Generally, it is preferable to generate this auxiliary supply voltage from the input voltage of the power electronic system to avoid further connections to an external supply. However, in high power systems e.g. traction converters, the input voltage is in the medium voltage range and/or up to some tens of kVs and thus a voltage conversion with a high step-down ratio at a low power level is needed.

A high step-down ratio can be achieved in several different ways. The most straight forward option is to use buck converters which are cascaded in order to avoid too small duty cycles. Another option is to use a flyback or forward converter. The aforementioned possibilities, however, share a common drawback: the employed switches have to be rated for the full input voltage of the system. Due to that, those switches will mainly be IGBT switches, if available for the voltage rating, or a series connection of such. This will lead to an increased size of the passive components, since they operate at a lower switching frequency than MOSFETs. Furthermore, as the auxiliary supply draws only a small current, the conduction losses will be increased if IGBTs have to be used instead of MOSFETs.

The Input-Series Output-Parallel (ISOP) converter (**Fig. 5.1(a)**) is

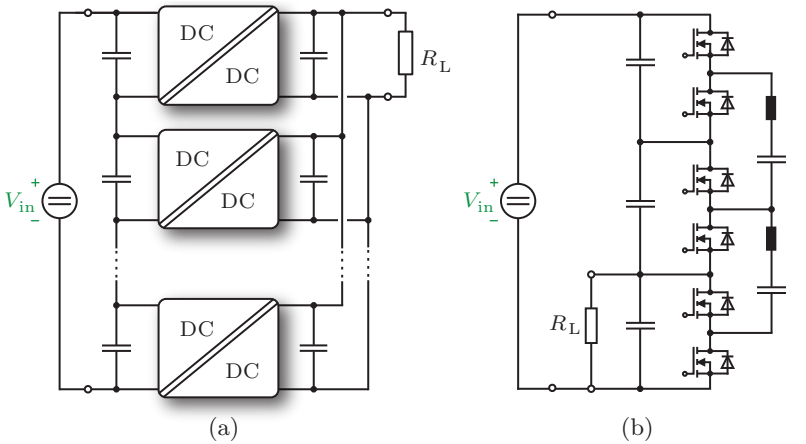

Fig. 5.1: Converter concepts for high step-down ratios as presented in literature: (a) ISOP (Input-Series Output-Parallel) converter and (b) switched capacitor converter (resonant version).

another type of converter that has been presented in literature [25, 130, 157] to facilitate the voltage conversion with a high step-down ratio. Here, the input terminals of several isolated DC/DC converters are connected in series in order to divide the input voltage by the number of converters and to limit the voltage stress of the employed switches of each converter, and the converter output terminals are connected in parallel to each other. One disadvantage is, that the employement of transformers is necessary and the isolation between the primary and secondary side needs to withstand voltages as high as the total input voltage.

Another concept to obtain a high step-down conversion ratio is by using switched capacitor converters (**Fig. 5.1(b)**) [85, 86]. These circuits basically consist of a capacitive voltage divider where the load is attached to one or more capacitors and an additional voltage balancing circuit in order to still ensure an equal voltage distribution among the capacitors despite the asymmetric load connection. Such balancing circuits are also known from battery management systems [93, 94]. In the operation of the circuit, the capacitors of the balancing circuit are alternately connected in parallel to adjacent capacitors of the voltage divider. As a further modification of this concept, the topology can

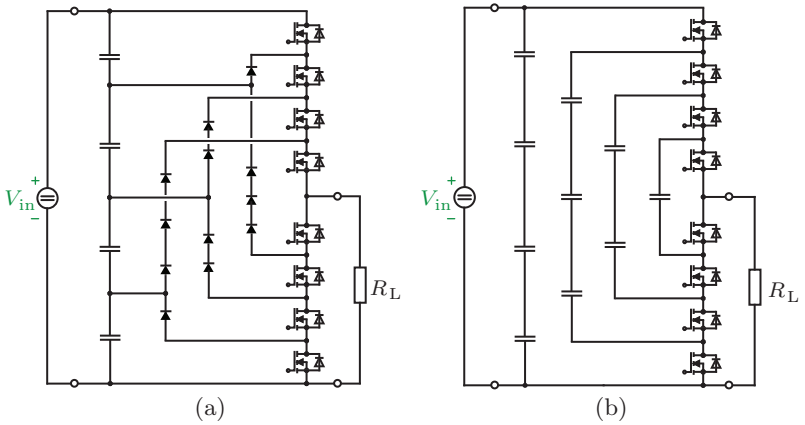

Fig. 5.2: Multilevel converter concepts for high step-down conversion ratios: (a) diode-clamped topology and (b) flying capacitor topology.

also be implemented as a resonant circuit where additional inductors are connected in series to each capacitor of the balancing circuit [158]. A main drawback of this concept is that the switches of the balancing circuit have to be controlled synchronously for proper operation of the system. Accordingly, a central control stage and a distribution of the gate drive signals with high isolation voltage has to be provided.

The multilevel converter concept has also been proposed for high step-down voltage conversion [159, 160]. The most basic structure does not comprise inductive components and thus features a high power density. Common types of multilevel converters are the diode-clamped topology (**Fig. 5.2(a)**) and the flying capacitor topology (**Fig. 5.2(b)**). The former category exhibits high voltage stresses on the diodes and hence requires a large number of series connected diodes which leads to increased conduction losses. The latter category exhibits high voltage stresses on the capacitors, thus requiring many capacitors to be arranged in a series connection. Since the total capacitance of series connected capacitors is smaller than that of a single capacitor, multiple capacitor cascades need to be paralleled. Furthermore, only the flying capacitor topology can actively balance the input voltages of the DC/DC converters equally by means of redundant switching states [161]. The diode-clamped topology, however, requires an additional balancing circuit [162].

The problem of high conversion ratios, although with reversed power flow direction, can also be found in photovoltaic (PV) architectures as described in **Chapter 3**. There, a DC-bus voltage which is much larger than the individual PV panel voltages has to be supplied to feed power into the grid. Among the suitable converter concepts for that application, the parallel connected partial-power converter (P-PPC) (cf. **Sec. 3.4**) equalizes the PV panel voltages of series connected PV panels, which ensures the operation of all panels in or close to their Maximum Power Point. These P-PPC topologies can also be applied to vertically stacked voltage domains such as proposed for multi-core microprocessor power supplies [163], [164]. They allow for regulating the operating voltage of series connected loads supplied from a fixed DC-bus. Thus, as the loads are no longer connected in parallel, the load current is decreased, which leads to a higher system efficiency.

This chapter introduces a new type of multi-cell high step-down converter, based on the P-PPC concept. Due to its operating principle, this new converter is denominated as Rainstick converter (RSTC). The converter features low voltage stresses of the employed components and a simple control scheme. First, the fundamental principle of operation is explained in **Sec. 5.1**. Subsequently, an analysis of the average current values in the inductors and RMS current values in the switches along with the conversion efficiency is presented in **Sec. 5.2**. In addition, the topology and the working principle of an auxiliary power supply on cell level are detailed in **Sec. 5.3**. Furthermore, different alternative realizations of the RSTC principle are described in **Sec. 5.4**. The optimization and realization of a RSTC prototype are shown in **Sec. 5.5** and measurement results are depicted in **Sec. 5.6**.

5.1 Operating Principle

In this section the structure of the RSTC and the fundamental operating principle are described.

The converter, as depicted in **Fig. 5.3(a)**, has a modular structure which is based on a capacitive voltage divider ($C_1 ... C_\mathrm{N}$) with buck-boost DC/DC converters as balancing modules and/or cells (e.g. B_1), similar to the P-PPC converter structure for PV panel voltage equalization in **Fig. 3.29**. The balancing modules are connected around two adjacent capacitors. This means, that an RSTC consisting of N capacitors contains $(N-1)$ balancing modules i.e. $(2(N-1))$ switches and $(N-1)$

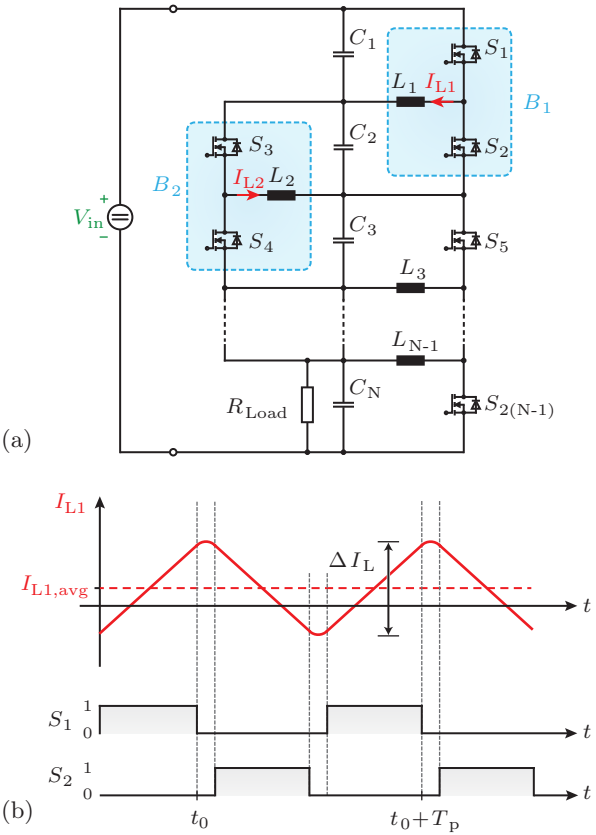

Fig. 5.3: New Rainstick converter (RSTC) topology: (a) circuit diagram showing a capacitive voltage divider ($C_1 ... C_N$) and balancing modules (B_1,B_2, highlighted) and (b) inductor current waveform and gate signals of one balancing module.

inductive components in total. A load can be attached in parallel to one or more capacitors of the voltage divider. The converter output voltage at the load R_{Load} is a fixed fraction of the input voltage V_{in}, determined by the number N of capacitors. For the sake of simplicity, the load is depicted as a single resistor, whereas in reality it would usually consist of an additional DC/DC converter in order to provide a variable voltage conversion of the RSTC output voltage to the voltage

level of the load.

The switches of each buck-boost converter can be controlled by a simple PWM signal with a fixed duty cycle of (slightly less than) 50% and a 180 ° phase shift at a fixed switching frequency. There is no communication or synchronization needed between the different balancing modules, which allows them to operate independent from each other.

The waveform of the gate signals and the resulting inductor current and its average value are shown for one balancing module in **Fig. 5.3(b)**. The system can operate with zero voltage switching (ZVS) as the direction of the inductor current reverses during each half period. Thus, in combination with the parasitic drain-source capacitances of the MOSFETs, ZVS can be provided. The converter can operate in ZVS over the whole range of input voltages by linearly increasing the switching frequency with increasing input voltage, which yields a constant peak-to-peak current ripple ΔI_{L} of the inductor current I_{L} for different input voltages V_{in}.

In this thesis, the main focus is on the step-down operation, but the converter structure is bidirectional and thus equally well suited for step-up operation, too. For that kind of operation, the source would be connected to one or more capacitors and the load would be attached across the whole stack of capacitors.

5.2 Analytical Description

In case of no load operation, the inductor currents shows no DC value. However, if a load is connected to the system, the currents in the inductors exhibit a DC value with a superimposed switching frequency ripple as shown in **Fig. 5.3(b)**. The average current value in the inductors ($I_{\mathrm{L,avg}}$) can be calculated for a given load current I_{Load}. The highest average current is obtained when the load is connected across only one capacitor and at the same time one terminal of the load is either connected to the highest or lowest potential of the system, i.e. the load is connected around the first or last capacitor in the stack of capacitors. Then, for a system with N capacitors, the average current values in the inductors 1 to $N-1$ are given by

$$|I_{\mathrm{L,avg}}|_{\mathrm{i}} = \frac{2 \cdot i}{N} I_{\mathrm{Load}},\ i \in \{1, 2, ..., N-1\} \tag{5.1}$$

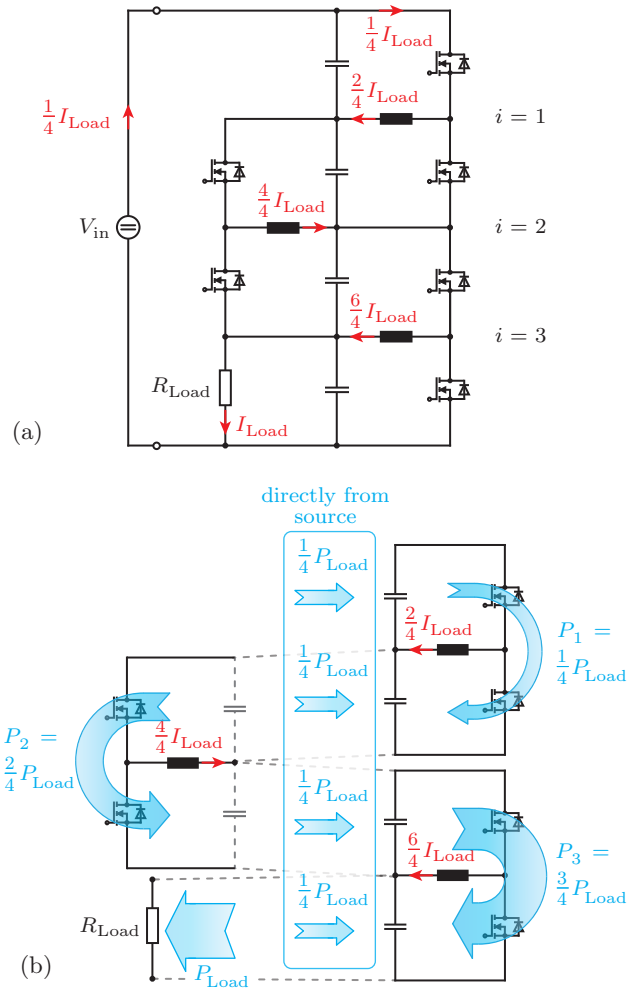

Fig. 5.4: Steady state analysis of the RSTC: (a) current distribution in the converter and (b) different representation of the converter with multiple buck-boost converters for an easier understanding of the power flows. The power is not at once directly transferred from the source to the load but through a cascade of different converter stages, comparable to the pebbles falling down in a rainstick.

where each of those values appears only in one inductor. So, in a converter with e.g. $N = 5$ capacitors, the average current values in the inductors are $\frac{2}{5}$, $\frac{4}{5}$, $\frac{6}{5}$ and $\frac{8}{5}$ of the load current. The largest value occurs in the inductor closest to the load. For $N \to \infty$ the maximum average current value approaches $2 \cdot I_{\mathrm{Load}}$.

The main sources of losses in the RSTC are winding and core losses in the inductors and conduction losses of the switches. The RMS values of the currents in the switches of a balancing module depend on the average value $I_{\mathrm{L,avg}}$ and on the peak-to-peak value ΔI_{L} of the inductor current ripple in that module,

$$I_{\mathrm{sw,rms}} = \frac{1}{2}\sqrt{2 \cdot I_{\mathrm{L,avg}}^2 + \frac{1}{6}\Delta I_{\mathrm{L}}^2} \,. \tag{5.2}$$

For calculations of the system efficiency, the power flow in the converter has to be analyzed. In general, the converter structure can be visualized as a stack of multiple buck-boost converters, as shown in **Fig. 5.4(b)**, which facilitates the power flow analysis. Similar to the pebbles in a rainstick, the power is not at once transferred from the source to the load but through a cascade of buck-boost stages. As seen in **Fig. 5.4(b)**, the largest amount of power is processed by the lowest converter of the chain, i.e. the converter closest to the load. It is interesting to note, that none of the balancing converters has to transfer the full amount of load power. Thus, this converter concept can be classified as partial-power converter [55]. A detailed power flow analysis can be found in **Appendix B**.

For the calculation of the RSTC efficiency, it is assumed that each of the balancing modules has a certain conversion efficiency, which is a function of the output power P_{i} of the module, i.e. $\eta_{\mathrm{i}}(P_{\mathrm{i}})$. Then the total converter efficiency can be calculated as

$$\eta_{\mathrm{sys,N}} = \frac{1 + \sum_{i=1}^{N-1} \left(\prod_{j=i}^{N-1} \eta_{\mathrm{j}} \left(P_{\mathrm{j}} \right) \right)}{N} \,. \tag{5.3}$$

For the above mentioned example of a RSTC converter with 4 capacitors and 3 balancing modules, this equation yields $\eta_{\mathrm{sys,4}} = 1/4 \cdot (1 + \eta_3(P_3) + \eta_3(P_3) \cdot \eta_2(P_2) + \eta_3(P_3) \cdot \eta_2(P_2) \cdot \eta_1(P_1))$. However, the conversion efficiency is usually of minor interest, since the main idea of the RSTC concept is a high voltage conversion ratio for low power (e.g. auxiliary) electronics. Since the power consumption of the

auxiliary electronics in a power electronic system is usually very small compared to the rated power of the system, the impact of the efficiency of the auxiliary power supply on the overall system efficiency is very small. Nevertheless, the RSTC efficiency can still be optimized, if the hardware of each buck-boost balancing module is optimized for the respective power level. The output power of the individual balancing modules can be found as

$$P_{\mathrm{i}} = \begin{cases} P_{\mathrm{Load}} \left(1 - \frac{1}{N \cdot \eta_{\mathrm{sys,N}}}\right), & \mathrm{i} = N-1 \\ \frac{P_{\mathrm{i+1}}}{\eta_{\mathrm{i+1}}(P_{\mathrm{i+1}})} - \frac{P_{\mathrm{Load}}}{N \cdot \eta_{\mathrm{sys,N}}}, & \mathrm{i} \in \{1, 2, ..., N-2\} \end{cases} . \tag{5.4}$$

The values of η_{sys} and P_{i} can be calculated in an iterative process as they are dependent on each other. This is due to the fact, that the losses of a balancing module are influencing the power, that has to be delivered by the balancing modules located above that module, i.e. located closer to the upper power source terminal.

5.3 Balancing Cell Auxiliary Supply

In order to supply the gate drives and the control electronics of each balancing module with power, an on-board auxiliary supply with a low component count and simple controllability is preferable. This allows to operate each module without an external power supply or external gate signals. The proposed auxiliary supply consists of capacitor C_{aux}, diode D_{aux} and switch S_{aux} which are integrated into each balancing module, as depicted in **Fig. 5.5(a)**.

With the switch S_{aux} being turned on, the balancing module operates as usual. If the voltage V_{CC} drops below the lower threshold $V_{\mathrm{CC,th1}}$, however, the switch S_{aux} is turned off, as shown at time t_1 in **Fig. 5.5(b)**. At time t_2, when the switch S_2 starts conducting the inductor current I_{L1}, capacitor C_{aux} is charged via the diode D_{aux}. This charging interval ends when current I_{L1} changes its direction, i.e. at t_3, which is necessary for ZVS operation of the switches S_1 and S_2. Then, the internal body diode of S_{aux} (or an external diode placed in anti-parallel to that switch) conducts the current I_{L1}. The charging continues at time t_4 when switch S_2 is turned on again. The switch S_{aux} is turned on when the voltage V_{CC} of capacitor C_{aux} reaches the upper threshold $V_{\mathrm{CC,th2}}$.

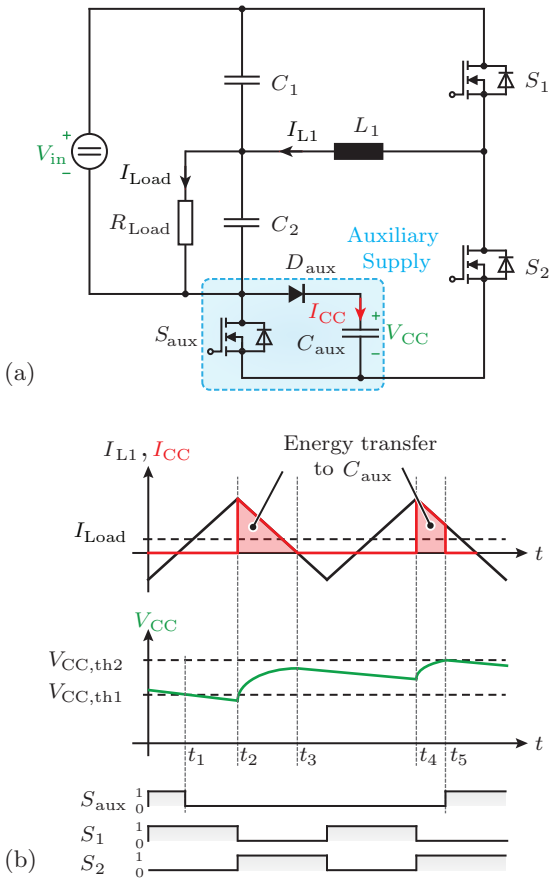

Fig. 5.5: Structure and analysis of the proposed module integrated auxiliary power supply unit: (a) balancing module with auxiliary power supply unit comprising switch S_{aux}, diode D_{aux} and capacitor C_{aux}; (b) characteristic waveforms of inductor current I_{L1}, charging current I_{CC} of auxiliary capacitor C_{aux}, auxiliary voltage V_{CC} and gate signal of auxiliary switch S_{aux}.

The minimum energy transfer to C_{aux} during a switching period of S_1 and S_2 can be calculated for the case of an inductor current without an average value (i.e. $I_{L,avg} = 0$), as with an increasing load current I_{Load} the energy transfer is increased (cf. **Fig. 5.5(b)**). Under the simplification of a small width of the voltage band defined by the

voltage thresholds (i.e. $V_{\mathrm{CC}} \approx V_{\mathrm{CC,th2}} \approx V_{\mathrm{CC,th1}}$), the transferred energy equals

$$\begin{aligned} W_{\mathrm{aux}} &= \int_0^{T_{\mathrm{P}}} V_{\mathrm{CC}}(t) \cdot I_{\mathrm{CC}}(t) dt \\ &\approx V_{\mathrm{CC}} \int_0^{T_{\mathrm{P}}} I_{\mathrm{CC}}(t) dt \\ &= V_{\mathrm{CC}} \cdot \frac{1}{16} \cdot \frac{1}{f_{\mathrm{sw}}} \cdot \Delta I_{\mathrm{L}} \ . \end{aligned} \tag{5.5}$$

Hence, the minimum average power that can be delivered by the auxiliary supply is independent of the switching frequency, as it is given by

$$P_{\mathrm{aux}} = W_{\mathrm{aux}} \cdot f_{\mathrm{sw}} = \frac{V_{\mathrm{CC}} \cdot \Delta I}{16} \ . \tag{5.6}$$

The proposed power supply unit can also be used in other converter topologies. A (minor) drawback of this auxiliary supply unit is, that the voltage, which is applied across inductor L_1, is altered by the value of V_{CC} each time the auxiliary switch S_{aux} is turned on or off. This can have an effect on the voltage balancing of the capacitors if the voltage V_{CC} is not negligibly small compared to the voltage of the capacitors $C_1 ... C_{\mathrm{N}}$.

5.4 Alternative Designs

The concept of the multi-cell Rainstick converter can be realized in different ways. In this section a number of possible modifications of the basic circuit from **Fig. 5.3** are described and examples of their potential applications are given.

5.4.1 Load Connection

The load can also be connected to capacitors in the middle of the voltage divider, as shown for example in **Fig. 5.6(a)**. This offers the advantage to limit the maximum average current value that appears in any inductor to

$$|I_{\mathrm{ind,avg}}|_{\max} = \begin{cases} I_{\mathrm{Load}}, & \text{if } N \text{ is even} \\ \frac{N-1}{N} I_{\mathrm{Load}}, & \text{if } N \text{ is odd} \end{cases} \tag{5.7}$$

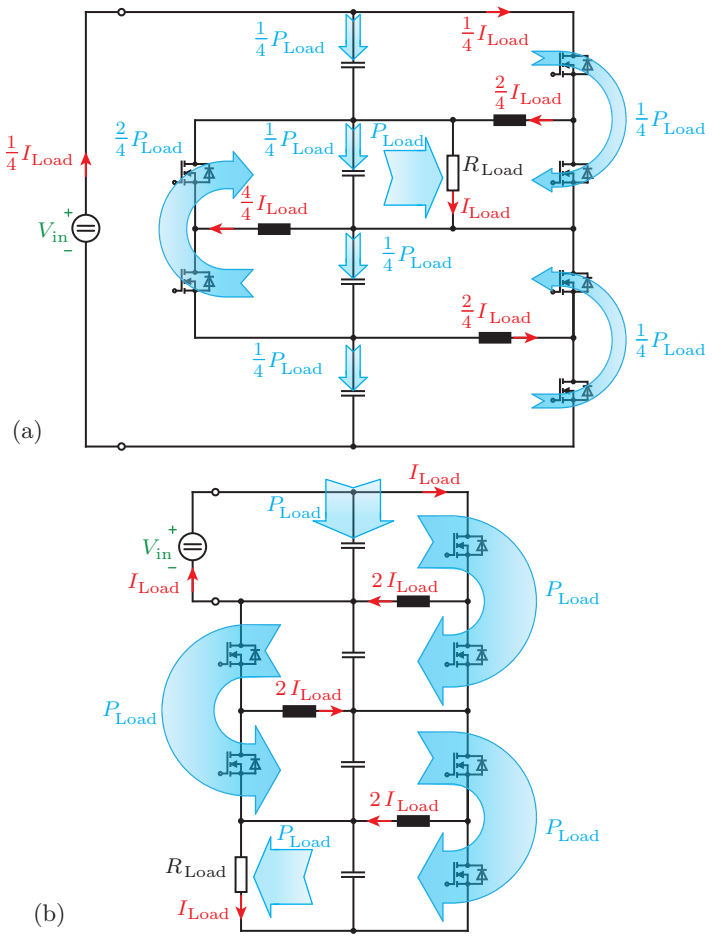

Fig. 5.6: Possible modifications of the Rainstick converter concept: (a) load connection to a capacitor in the middle of the capacitor stack, yielding lower average current values in the inductors and (b) connection of the source to only a fraction of the stacked capacitors.

Hence, inductor losses and conduction losses decrease and the overall system efficiency increases when the load is connected to capacitors closer to the middle of the voltage divider.

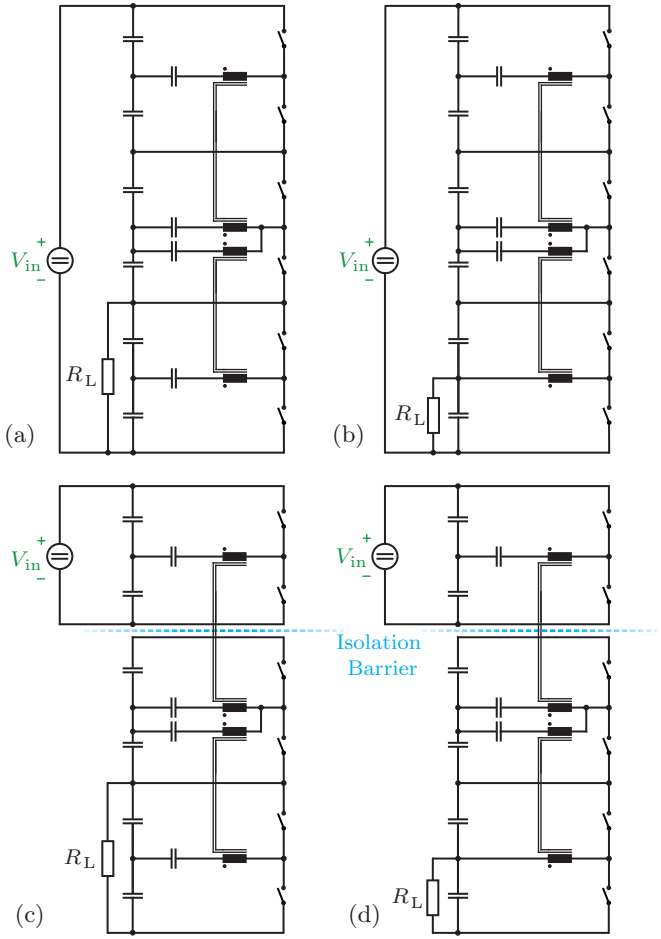

Fig. 5.7: Possible modifications of the RSTC converter concept with reduced component count by use of coupled inductors: (a, b) resonant versions with different load connections and (c, d) isolated output stages.

5.4.2 Source Connection

The RSTC operation principle does also apply when the source is only connected to some of the N capacitors. An example with corresponding power flows is given in **Fig. 5.6(b)**. In contrast to the original idea of

the RSTC, those balancing modules that are not connected to the source need to carry the full load power and the losses.

5.4.3 Coupled Inductors and Isolation

The component count can be reduced by the use of coupled inductors i.e. transformers with a voltage transfer ratio of 1:1, instead of inductors as depicted in **Fig. 5.7**. The basic circuit of the RSTC can be modified in such way, that for an even number (N) of capacitors only $(N/2-1)$ transformers and (N) switches are needed. With resonant capacitors in series with the transformers, the system can still be operated in ZVS. This can be done by adjusting the switching frequency to the resonance frequency of the resonance capacitors and the leakage inductance of the transformer. It is also possible to couple all cells together by means of only one transformer. The different coupling concepts are analyzed in more detail in **Appendix B**.

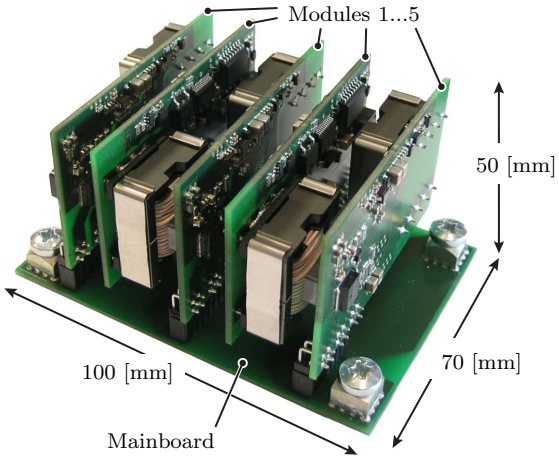

Fig. 5.8: Rainstick converter prototype with five balancing modules for an input voltage of up to $V_{\mathrm{in,max}} = 2.4\,\mathrm{kV}$ and $P_{\mathrm{out}} = 30\,\mathrm{W}$.

5.5 Prototype Optimization and Realization

A prototype of the RSTC comprising five balancing modules, each with its own on-board power supply unit (cf. **Sec. 5.3**), has been assembled and is shown in **Fig. 5.8**. As five balancing modules are used, the converter output voltage is equal to one sixth of the input voltage. The prototype is designed for a maximum input voltage of $V_{\mathrm{in,max}} = 2.4\,\mathrm{kV}$ and a rated output power of $P_{\mathrm{out}} = 30\,\mathrm{W}$ (at input voltages between $V_{\mathrm{in}} = 1.6\,\mathrm{kV}...2.4\,\mathrm{kV}$). Thus, each balancing capacitor has to be rated for a voltage of at least 400 V and the employed switches have to withstand voltages of up to $V_{\mathrm{DS,max}} = 800\,\mathrm{V}$. The switching frequency of each balancing module is adjusted by a voltage controlled oscillator (VCO) that senses the voltage accross both balancing capacitors. Hence, the switching frequency is linearly increased with increasing converter input voltage, yielding constant volt-seconds $\lambda_{\mathrm{L}} = V_{\mathrm{C}}/(2f_{\mathrm{sw}})$ which are applied across the main inductor during all switching periods. As a certain peak-to-peak inductor current ripple ΔI_{L} is required by the auxiliary supply of a module, the inductance of the main inductor L_1 equals

$$L_1 = \frac{\lambda_{\mathrm{L}}}{\Delta I_{\mathrm{L}}}\ . \tag{5.8}$$

The power consumption of the control electronics was estimated

Tab. 5.1: List of main components of the RSTC prototype. (Note: All quantities are given per balancing module.)

Component	**Specifications**
2x MOSFETs	STD3NK100Z / ST [$R_{\mathrm{DS,on}} = 5.4\,\Omega$, $V_{\mathrm{DS}} = 1000\,\mathrm{V}$, $I_{\mathrm{D}} = 2.5\,\mathrm{A}$]
1x Gate driver	Half-bridge gate driver IR2214 / Int. Rectifier
1x Inductor	EFD25/13/7, N87 ferrite / EPCOS [$L \approx 1\,\mathrm{mH}$, 60 turns, litz wire (60x71µm), $l_{\mathrm{airgap}} = 0.25\,\mathrm{mm}$]
1x VCO	MCB14046B / ON Semiconductor
2x Capacitors	X7R ceramic capacitors [$C = 1.05\,\mu\mathrm{F}$ (7x150 nF), $V_{\mathrm{rated}} = 500\,\mathrm{V}$]

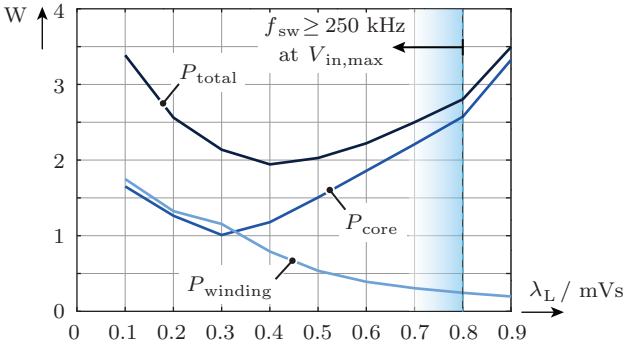

Fig. 5.9: Calculated inductor losses depending on the applied volt-seconds (λ_L) for an EFD25 N87 core, $\Delta I_L = 0.8\,A$, and capacitor voltages of $V_c = 300\,V$. The total inductor losses P_{total} consist of core losses P_{core} and winding losses $P_{winding}$.

to be less than 400 mW per balancing module. With a lower voltage threshold level of the auxiliary supply of the module of $V_{CC,th1} = 8\,V$, a minimum required peak-to-peak current ripple in the inductor of $\Delta I_L = 0.8\,A$ can be calculated. In order to select a suitable value of λ_L, an inductor optimization has been performed. Here, the inductor design with the lowest losses for a given value of λ_L is computed. For this optimization, all available EPCOS N87 cores with either ETD or EFD core shape and a selection of Rupalit litz wires are considered. The results for an EFD25 core are demonstrated in **Fig. 5.9** for a capacitor voltage of $V_C = 300\,V$ and $\Delta I_L = 0.8\,A$. Even though the lowest inductor losses can be achieved at $\lambda_L = 0.4\,mVs$, values below 0.8 mVs already yield switching frequencies above $f_{sw} = 250\,kHz$, which proved to be unpractical in combination with the selected gate drive due to high gate drive losses. Thus, a value of $\lambda_L = 0.8\,mVs$ was selected for the prototype. Furthermore, the employed components of the RSTC prototype are listed in **Tab. 5.1**.

5.6 Measurement Results

The converter efficiency measurements of a single RSTC balancing module are performed with a high precision setup shown in **Fig. 5.10**, which is in accordance to setup proposed in **Fig. 3.14**. The measurement

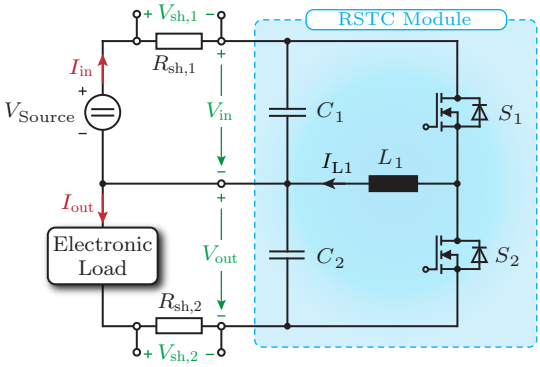

Fig. 5.10: Measurement setup for the efficiency measurements of a single RSTC balancing module. The setup utilizes shunt resistors ($R_{sh,1}, R_{sh,2}$) with high-precision voltmeters for precise measurements of the input and output currents. More details about the measurement setup can be found in **Sec. 3.2.4**.

results of a single balancing module at different levels of capacitor voltages are presented in **Fig. 5.11(a)** in dependence of the output power. The results show, that for higher capacitor voltages and thus higher switching frequencies the efficiency decreases. This is due to the fact, that any increase of the switching frequency results in higher inductor losses since the core losses as well as the winding losses are frequency dependent. Furthermore, the power consumption of the gate-drive also increases linearly with the switching frequency. One way to increase the efficiency of the system would be to design the system with a larger value for λ_L and with a larger core size. Thereby, the switching frequency of the balancing modules could be decreased without increasing the magnetic flux density, both being contributors to core losses. This, however, would decrease the power density of the system and thus has to be considered as a trade-off.

Based on the efficiency measurements of an individual module, the efficiency of the system with 5 balancing modules has been calculated based on (5.3) and (5.4) for different levels of input voltages. The calculated efficiency values are compared to the measured system efficiency in **Fig. 5.11(b)**. It can be seen, that the calculation results correspond well with the measurement results with a maximum error of around 7%

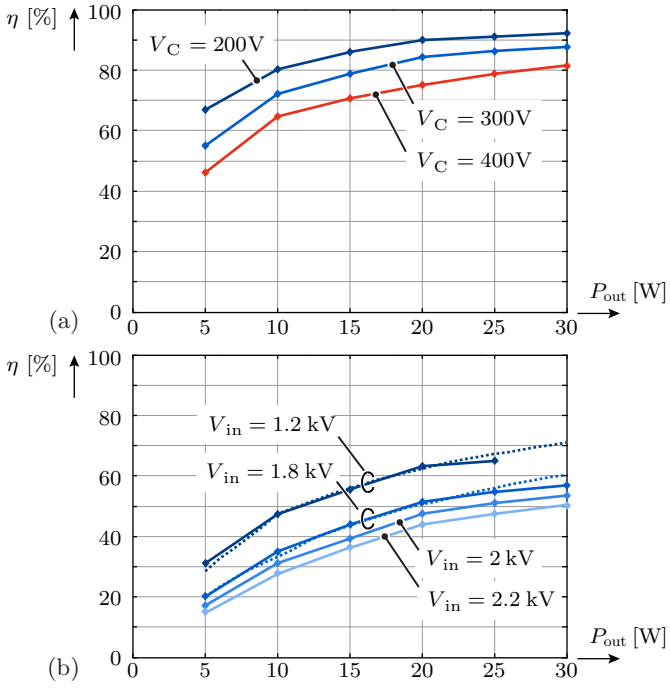

Fig. 5.11: Efficiency measurement results of the RSTC plotted over the output power: (a) single balancing module at three different levels of capacitor voltages V_C and (b) full system comprising five balancing modules at different levels of input voltage V_{in}. The dotted lines denote calculated system efficiency values. *Remark:* The measurement for $V_{in} = 1.2\,kV$ and $P_{out} = 30\,W$ could not be performed as the prototype can only supply the rated output power at input voltages between $V_{in} = 1.6\,kV...2.4\,kV$.

at rated power.

The measured waveforms of the inductor current I_L and the inductor voltage U_L of the balancing module closest to the load are shown in **Fig. 5.12** for the operation at an input voltage of $V_{in} = 1.8\,kV$ and an output power of $P_{load} = 20\,W$. The small current dips of the inductor current during the reversal of the inductor voltage are caused by intra-winding capacitances of the inductor.

The voltage distribution of the input voltage V_{in} among the six capacitors of the RSTC prototype is shown for no-load operation in

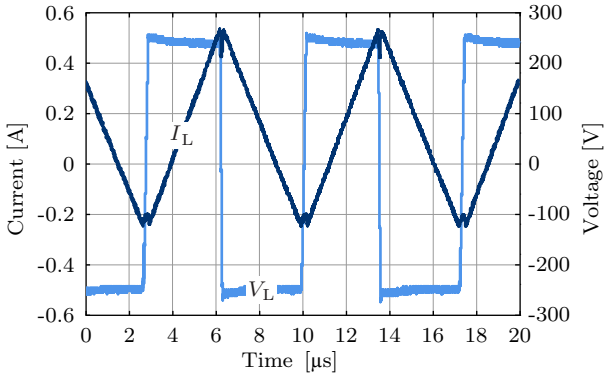

Fig. 5.12: Measured waveforms of the inductor current I_L and inductor voltage U_L of the balancing module closest to the load. The measurements were performed during the operation with an input voltage of $V_{in} = 1.8\,kV$ and an output power of $P_{load} = 20\,W$.

Fig. 5.13. It is visible, that the input voltage is not equally divided among the capacitors. Instead, the voltage of the uppermost capacitor is up to around 17% higher than the expected value whereas the voltage of the lowest capacitor is around 16% lower than what is expected if

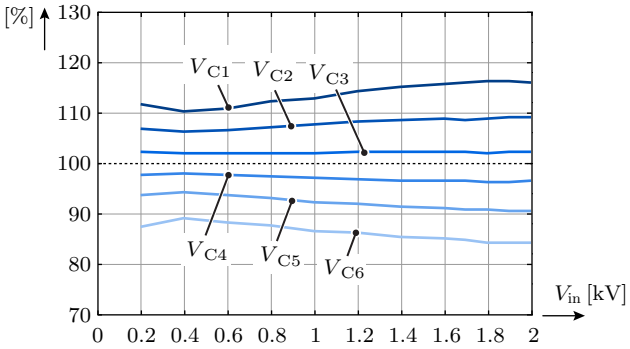

Fig. 5.13: Distribution of the input voltage V_{in} among the six capacitors of the RSTC converter prototype in percent of nominal value (i.e. $V_{in}/6$). The capacitors are numbered with C_1 being the uppermost and C_6 the lowest capacitor of the stack. The load is connected in parallel to capacitor C_6.

perfect equalization was assumed. This can partly be explained by the fact, that the auxiliary power supply unit is connected in series to the lower capacitor of a balancing module. Thus, each time the auxiliary switch S_{aux} (cf. **Fig. 5.5**) is turned off, the voltage of the upper capacitor (C_1) is equalized with the voltage of the series connection of the lower capacitor (C_2) and the auxiliary capacitor (C_{aux}). If a load is connected to the RSTC, this unequal voltage distribution tends to become slightly worse, as the superimposed load current causes voltage drops across the MOSFETs and the inductor in each balancing module, which influences the voltage equalization. A solution would be to include a controller in each individual balancing module that adapts the duty-cycles of the switches to values that are slightly different from 50%. This could be implemented e.g. as a feedback loop with the voltage difference of the capacitors as input variable for a PI controller.

5.7 Summary and Conclusion

In this chapter, a novel modular multi-cell converter structure, named the Rainstick converter, has been presented for a voltage conversion with high conversion ratios.

The converter structure consists of multiple converter cells which balance the voltages of a capacitive voltage divider employing a stack of series connected capacitors. The converter allows for bidirectional power flow with a fixed voltage conversion ratio, which, due to its modular structure, can be easily adapted to high conversion ratios. Based on the presented current and power flow analysis, this converter structure can be classified as a partial-power converter since none of the employed modules needs to transfer the full amount of load power.

In order to operate all converter cells independently without any exchange of information between the cells, a self-controlled on-board power supply unit with a low part count has been presented. This power supply unit serves to provide the power required by each cell to run the control electronics and the gate drives.

Different variations of the basic multi-cell Rainstick converter are shown. They allow to reduce the component count by coupling different balancing converter cells by means of transformers. Furthermore, different possibilities to connect the load are presented.

In order to verify the theoretical analysis and the operation of the proposed concept, a converter prototype has been optimized and built

up. The measurement results of the operation of the prototype for input voltages up to $V_{\mathrm{in}} = 2.4\,\mathrm{kV}$ and an output power up to $P_{\mathrm{Load}} = 30\,\mathrm{W}$ have been shown. The measurements verify the operation principle and demonstrate that the converter can be operated over a wide range of input voltages beginning from $V_{\mathrm{in}} = 200\,\mathrm{V}$.

6 Conclusion & Outlook

Power electronics is a key enabling technology for several megatrends that are shaping the way we will be living in the future. Thus, innovations and further improvements of power electronic systems with respect to different performances like efficiency, power density, and cost are mandatory prerequisites to further continue the advancement of these megatrends. Many performance improvements in power electronics are based on the gradual improvement of employed materials, e.g. core materials, or on disruptive technology changes like the shift towards wide-bandgap semiconductors.

In this thesis, the multi-cell converter approach in combination with a multi-objective optimization is identified as another path to the performance improvement of power electronic systems. The multi-cell converter approach employs well-known topologies within the cells, which can benefit from fundamental scaling laws attributed to sharing the power flow among the cells of a multi-cell system. Inherent to all power electronic systems is the trade-off between different performance measures which necessitates a multi-objective optimization. This approach, in contrast to a single-objective optimization, allows to directly identify the feasible performance space and the Pareto front, which quantifies the trade-off between different performance aspects that is given by Pareto-optimal designs. This requires the mapping of the design space, which contains the set of possible realizations, into the performance space by means of accurate multi-physic component models. In multi-cell systems, this approach is even more called for, as the design space is augmented by more degrees of freedoms like e.g. the number of employed cells.

As a result of the systematic optimization of the multi-cell converter

systems for different applications, a broad variety of improvements and advantages of multi-cell systems compared to single-cell counterparts are revealed in this thesis:

- *Higher performance*: The hardware demonstrators for the different applications verify the introduced scaling laws by achieving higher efficiency and power density values than state-of-the-art systems with only one converter cell. This is especially true for the multi-cell PFC telecom rectifier, which not only features a high peak efficiency but, by means of 4D-interleaving control, also a very flat efficiency vs. output power characteristic.
- *Increased control flexibility and functionality*: The multi-cell approach for PV systems allows to operate each PV panel individually in its MPP. This maximizes the power output of the total PV system by mitigating the effects of partial shading of the PV string. Furthermore, with the possibility of supervising the operation of each PV panel, additional functionality is introduced that is not available with conventional string inverters. The control of individual cells is also the basis for the advanced 4D-interleaving modulation of the ISOP telecom PFC rectifier, which not only increases the system performance but also offers additional failure-handling possibilities by bypassing the cell where a failure has occurred and potentially allowing to hot-swap a broken cell.
- *Modularity*: The inherent modularity of multi-cell systems offers an easy scalability of the operating range by changing the number of employed cells. Once the design of the basic building block (i.e. of one conversion cell) of the system is determined, the system can be easily scaled for other power and/or voltage levels. This was shown for the "Rainstick" multi-cell auxiliary power supply, which can be extended with additional cells to higher input voltage levels. In a similar way, PV systems can be extended to higher power levels with additional PV panels with PV module-integrated converter cells.
- *Economies of scale*: Each conversion cell is designed for just a fraction of the power and/or the voltage of the entire system. Therefore, the cells contain only high-volume low-cost components (e.g. low-voltage MOSFETs and standard core shapes) instead of specialized and expensive components (e.g. semiconductors with high blocking voltage and custom made core shapes).

This potentially allows to benefit from economies of scale effects which can lead to lower costs of the system.

- *Well-proven topologies*: The cells are based on well-proven and established converter topologies, which potentially increases the industry acceptance of the multi-cell approach.

Apart from the multitude of benefits arising from the multi-cell approach, some weaknesses have to be mentioned that are inherent to designing and commissioning a multi-cell system:

- *Increased control and communication complexity*: The balancing of the voltages and/or currents among the cells has to be guaranteed for all operating conditions. Even if the system exhibits self-balancing features (e.g. typically given for ISOP and IPOS systems) during normal operation, this might not be the case during start-up and/or shut-down phases. There, special care has to be taken and additional control algorithms might have to be implemented. Furthermore, the control of the system requires a reliable communication between the cells, which leads to an increased communication overhead.

- *Inter-cell influence*: The operation of the cells within a multi-cell system is strongly coupled and implicates that the cells influence each other. This can result, e.g., in common-mode currents within cells, which are caused by the switching action of others cells due to the series connection of cell terminals in ISOP systems. This can require additional hardware components, e.g. common-mode chokes for each cell, to limit the effect of the coupled operation of cells.

- *Debugging*: The commissioning of a multi-cell system and the inevitable trouble-shooting requires to simultaneously monitor many system variables of the power as well as the control part, which necessitates a more extensive measurement setup.

Consequently, the multi-cell converter approach is a feasible way of improving the performance of power electronic systems, however at the cost of a higher control and operational complexity.

6.1 Future Trends & Outlook

A main weakness of multi-cell systems at present time is the additional control complexity and inter-cell communication effort. This drawback will however diminish, since Moore's law predicts an exponential growth of computation power over time [165]. This fundamental trend will drive down the cost overhead for the communication between the cells in a multi-cell system and provide enough computation power for more advanced 4D-interleaving control schemes in multi-cell systems.

In order to gain a broader adoption of multi-cell systems in industry and to bridge the gap between academic research and commercial applications, the integration level has to be advanced [3]. This can be the integration of multiple semiconductors into a package, preferably with their gate drives, or the integration of passives and other components into the PCB. This allows to design a switching and in the next step the conversion cell as a highly integrated building block, which is the smallest element of a multi-cell system. Thus, the high number of individual components in multi-cell systems, built up of discrete components, is decreased to a smaller number of building blocks. The conversion cells can then be arranged in different ways, e.g. with series or parallel connections of the input and output terminals, according to the intended operation. By also integrating the fiber-optic communication into the PCB, the additional communication effort for multi-cell systems can be reduced with the additional benefit of immunity of the communication channel against common-mode noise.

The presented multi-objective optimization results of the different multi-cell systems were limited to the performance measures of efficiency and power density. This can be extended in future research to additional performance measures such as costs and reliability in order to obtain a more complete comparison of multi-cell systems to state-of-the-art converter concepts.

Appendices

A

Derivation of Converter Scaling Laws

The efficiency of a power electronic system with input power P_1, output power P and losses P_L is defined as

$$\eta = \frac{P}{P_1} = \frac{P}{P + P_\mathrm{L}} \Rightarrow P_\mathrm{L} = \frac{1-\eta}{\eta} P \ . \tag{A.1}$$

In the most simplified approach, the power electronic system is considered to be a cube with a total surface area A which scales with the volume V of the cube by $A = 6V^{2/3}$. The heat dissipation capability p_L of a system can be defined by relating the losses of the system to its surface area,

$$p_\mathrm{L} = \frac{P_\mathrm{L}}{A} = \frac{1-\eta}{\eta} \cdot \frac{P}{6V^{2/3}} \ . \tag{A.2}$$

This allows to derive fundamental scaling laws since any scaled system needs to have the same value of p_L as the reference system (denoted by subscript "$_0$"),

$$\frac{1-\eta}{\eta} \cdot \frac{P}{6V^{2/3}} = \frac{1-\eta_0}{\eta_0} \cdot \frac{P_0}{6V_0^{2/3}} \ . \tag{A.3}$$

Rearranging this equation yields

$$\frac{P}{P_0} = \frac{(1-\eta_0)}{(1-\eta)} \cdot \frac{\eta}{\eta_0} \cdot \left(\frac{V}{V_0}\right)^{2/3} \ . \tag{A.4}$$

By assuming a constant efficiency, i.e. $\eta = \eta_0$, the relation

$$\frac{V}{V_0} = \left(\frac{P}{P_0}\right)^{3/2} \tag{A.5}$$

can be found. This means, that doubling the power ($P = 2P_0$) leads to an increase of the volume of $V = 2^{3/2} \cdot V_0 \approx 2.83 \cdot V_0$. This is also reflected in a decrease of the power density ($\rho = P/V$) which can be derived for the case of a constant efficiency as

$$\rho = \frac{P}{V} = \frac{P}{V_0 \left(\frac{P}{P_0}\right)^{3/2}} = \frac{P_0}{V_0} \cdot \left(\frac{P_0}{P}\right)^{1/2} = \rho_0 \left(\frac{P}{P_0}\right)^{-1/2} \tag{A.6}$$

and yields $\rho = 2^{-1/2} \cdot \rho_0 = 0.707 \cdot \rho_0$ when the power is doubled. This can be explained by the fact, that a system with a larger volume has a smaller surface-to-volume ratio than smaller systems. Since the surface area is required for heat dissipation, the power per volume can only be scaled with the surface area of the system and not with the volume. This leads to smaller power densities of (thermally limited) larger systems.

The scaling law of (A.4) can also be evaluated for the condition of a constant power density, i.e. $\rho = P/V = \rho_0 = P_0/V_0$, which leads to

$$\eta = \frac{\eta_0 \left(\frac{P}{P_0}\right)^{1/3}}{1 + \eta_0 \left(\left(\frac{P}{P_0}\right)^{1/3} - 1\right)} \,. \tag{A.7}$$

For an assumed efficiency of $\eta_0 = 98\%$ of the reference system, the efficiency of the scaled system has to be increased to $\eta = 98.4\%$ if the power of the system is doubled ($P = 2P_0$).

B

Unified Power Flow Analysis of String Current Diverters

Partial power processing converter architectures for series connected sources and/or loads, also termed power shufflers, differential power processing converters, or current diverters, have gained significant interest in the past, due to their capability of balancing local asymmetries in voltages by processing only a fraction of the full system power. This promises high efficiencies and small converter volumes compared to full-power converters since the converter modules can have a low power rating and their efficiency has a reduced impact on the total conversion efficiency. Popular applications are battery state-of-charge (SOC) equalization [93, 166], data center power distribution [167], multistage stacked boost converters [168–170], stacked voltage domains for CPU power delivery [163], photovoltaic (PV) energy systems (cf. **Sec. 3.4** and **Fig. B.1(a)**) [98,171,172] and auxiliary supplies for high conversion ratios (cf. **Chapter 5** and **Fig. B.1(b)**). The current diverter modules typically consist of synchronous buck-boost converters (**Fig. B.1(c)**) for bi-directional power flow which can be operated with zero voltage switching (ZVS) if the (peak-to-peak) current ripple in the inductor is sufficiently high, i.e. $\Delta I_{\mathrm{L}} \geq 2 \cdot I_{\mathrm{L,avg}}$, as shown in **Fig. B.1(d)**. Another advantage of this converter type is, that for voltage balancing every module can be operated with a fixed duty cycle of 50% without any communication between the modules and without any control. Furthermore, due to the modular nature of this type of system, it can easily be extended to longer strings and/or higher voltages.

Even though the current diverters have been in the focus of research for many years, there are still no general design guidelines for the con-

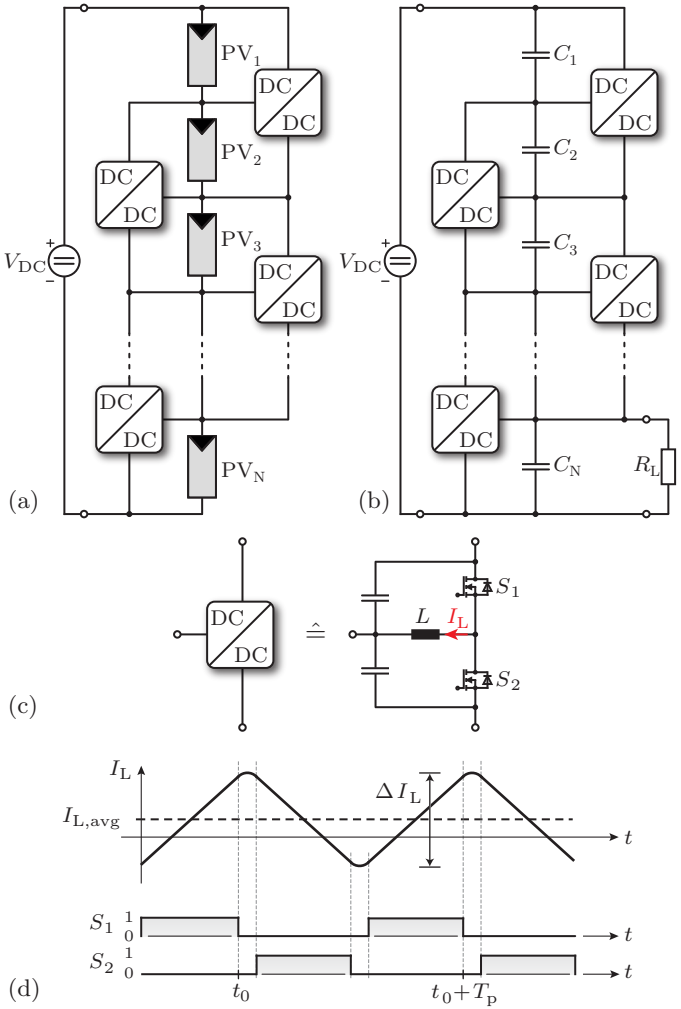

Fig. B.1: Possible applications of string current diverter modules: (a) PV energy systems where local asymmetries can be caused by mismatched operating conditions, e.g. due to shading of some PV panels; (b) power supplies with high conversion ratios where asymmetries are created since the load is attached e.g. to only one capacitor or to a fraction of all capacitors. (c) buck-boost topology of the current diverters. (d) characteristic inductor current waveform and gate signals of one balancing module for ZVS operation.

struction of the diverter modules. Especially in the area of photovoltaic energy systems, the design of the diverters is strongly dependent on the number of PV panels in a string and the expected worst case shading scenario, as described in **Sec. 3.4**, which partly explains the lack of general design guidelines. Therefore, in this chapter a universal power flow analysis is introduced, which can be applied to the different applications of the current diverter concept. This analysis allows to identify the power level which is processed by any diverter module in order to derive the required specifications for the design of the diverter modules. The chapter is structured such that the universal power flow analysis is introduced in **Sec. B.1** and the specific application to solar energy systems is presented in **Sec. B.2** and the application to converters with high conversion ratios in **Sec. B.3**. The concept of coupling the inductors of the diverter modules and the associated advantages and disadvantages is analyzed in **Sec. B.4**.

B.1 Power Flow Analysis

In this appendix a universal analytical solution for the power flow in the current diverters is derived, which is applicable to all operation scenarios of the diverter modules.

From a very general point of view, the structure of the system consists of N_s power sources/sinks and $N_\mathrm{b} = N_\mathrm{s} - 1$ current diverter modules, as shown in **Fig. B.2**. Depending on the type of operation and/or application, the power sources/sinks can have any of the following three states:

- *Positive:* Operation as a power sink, i.e. load;
- *Negative:* Operation as a power source, e.g. PV panel;
- *Zero:* No net power flow, i.e. capacitor.

The sources/sinks in the system can be written in a vector form $\overrightarrow{p_\mathrm{s}} = (P_{\mathrm{s},1}, P_{\mathrm{s},2}, ..., P_{\mathrm{s},Ns})$, which defines the power flow in the system.

Based on $\overrightarrow{p_\mathrm{s}}$ the power flow P_tot to/from the DC-link source V_DC can be derived as the sum of all sources in $\overrightarrow{p_\mathrm{s}}$. Due to the stacked nature of the power sources in $\overrightarrow{p_\mathrm{s}}$ and/or cells (which implies that the current from/to the DC-link through the individual cells is equal) and the fact, that the voltages of the cells are equalized by the current diverter modules (i.e. every power source has the voltage of $V_\mathrm{DC}/N_\mathrm{s}$), the power P_tot

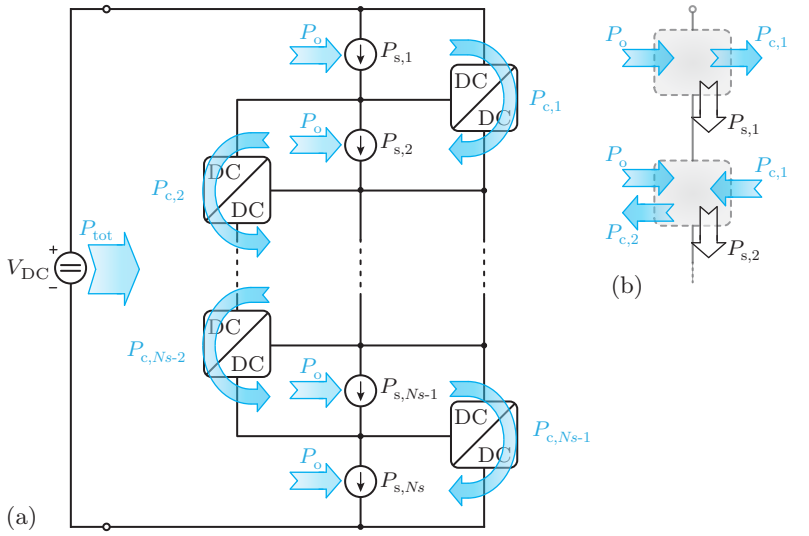

Fig. B.2: Generalized equivalent circuit of N_s series stacked power sources and/or converter cells with $N_b = N_s - 1$ current diverter modules. (a) The power sources $P_{s,i}$ can either have a positive value (i.e. loads), a negative value (i.e. generators) or be zero (i.e. capacitors). (b) Detailed explanation of the power balance of the converter cells in (a), where $P_{s,i} > 0$ indicates that power is transferred from a cell to an attached load.

to/from the voltage source V_{DC} is equally divided among the individual power sources. This means, that each cell provides/receives a power of P_o which is directly transferred to/from the DC-link source V_{DC}, which can be calculated as

$$P_o = \frac{\sum_{i=1}^{N_s} P_{s,i}}{N_s} = \frac{P_{tot}}{N_s} \,. \tag{B.1}$$

Accordingly, that the average power of all sources is directly transferred to the DC-link (or taken from the DC-link). The current diverters thus only balance the power asymmetries among the stacked power sources such that the difference between the average power P_o and actual power level $P_{s,i}$ of the power sources is compensated.
Furthermore, since for each of the stacked power sources a power balance has to prevail, the following set of equations has to be fulfilled

$$\begin{aligned} -P_{\mathrm{s},1} + P_{\mathrm{o}} - P_{\mathrm{c},1} &= 0 \\ -P_{\mathrm{s},2} + P_{\mathrm{o}} + P_{\mathrm{c},1} - P_{\mathrm{c},2} &= 0 \\ &\vdots \\ -P_{\mathrm{s},Ns\text{-}1} + P_{\mathrm{o}} + P_{\mathrm{c},Ns\text{-}2} - P_{\mathrm{c},Ns\text{-}1} &= 0 \\ -P_{\mathrm{s},Ns} + P_{\mathrm{o}} + P_{\mathrm{c},Ns\text{-}1} &= 0 \end{aligned} \tag{B.2}$$

where $P_{\mathrm{c},i}$ is the power transferred in each current diverter module, as shown in **Fig. B.2**. This set of equations can be solved to find the levels of power which are transferred by the current diverter modules, i.e. $\overrightarrow{p_{\mathrm{c}}} = (P_{\mathrm{c},1}, P_{\mathrm{c},2}, ..., P_{\mathrm{c},Ns\text{-}1})$, as

$$P_{\mathrm{c},i} = \frac{1}{N_{\mathrm{s}}} \left(i \cdot \underbrace{\sum_{j=i+1}^{N_{\mathrm{s}}} P_{\mathrm{s},j}}_{①} - (N_{\mathrm{s}} - i) \cdot \underbrace{\sum_{j=1}^{i} P_{\mathrm{s},j}}_{②} \right) . \tag{B.3}$$

It can be seen, that the power transferred through any current diverter module is influenced by all power sources, since the power level is calculated by weighting the sum ① of all power sources "below" the diverter module with the index number i of the diverter, i.e. the number of sources "above" this diverter, and subtracting the sum ② of the power sources "above" the diverter module weighted with the number of sources $N_{\mathrm{s}} - i$ "below". For the case of equal power sources, the power in the diverter modules becomes zero, which is in accordance with the expectation that there is no power transfer through the diverter modules if there is no mismatch.

B.2 PV Energy Systems

As a solution to the problem caused by mismatched operation conditions in a PV system, current diverter modules (also termed parallel-connected partial-power module integrated converters) can be installed, as described in **Sec. 3.4**. Based on the nomenclature introduced in **Sec. B.1**, where power sources have a negative sign, the vector of power

sources $\overrightarrow{p_s}$ can be written as $\overrightarrow{p_s} = (-P_{\mathrm{MPP},1}, -P_{\mathrm{MPP},2}, ..., -P_{\mathrm{MPP,NPV}})$, $P_{\mathrm{MPP},i} > 0$, for a system with N_{PV} PV panels.

In the following, a worst case scenario is considered, where the string of PV panels is divided into a shaded part and an unshaded part. It is assumed that the first n panels are shaded and have a maximum power generation of $k_{\mathrm{sh}} \cdot P_{\mathrm{MPP}}$ per panel and the remaining $N_{\mathrm{PV}} - n$ panels are unshaded with a maximum output power of P_{MPP}. According to (B.1), the power which is directly transferred from each PV panel to the DC-link source is

$$P_{\mathrm{o}} = -\frac{n \cdot k_{\mathrm{sh}} \cdot P_{\mathrm{MPP}} + (N_{\mathrm{PV}} - n) \cdot P_{\mathrm{MPP}}}{N_{\mathrm{PV}}} \ . \tag{B.4}$$

Regarding the diverter modules in this scenario, the biggest amount of power has to be processed in the diverter module n which is at the boarder of the shaded and unshaded section of the PV string. Based on (B.3), this diverter module processes a power level of

$$P_{\mathrm{c},n} = -\frac{P_{\mathrm{MPP}}}{N_{\mathrm{PV}}} \cdot (n \cdot (N_{\mathrm{PV}} - n) - n \cdot (N_{\mathrm{PV}} - n) \cdot k_{\mathrm{sh}}) \ . \tag{B.5}$$

The maximum of (B.5) can be found at $n = \frac{N_{\mathrm{PV}}}{2}$, i.e. in case half of the PV string is shaded and the other half is unshaded, which leads to a power flow through the balancing converter connecting the two sections of

$$|P_{\mathrm{c,max}}| = \frac{N_{\mathrm{PV}}}{4} \cdot P_{\mathrm{MPP}} \cdot (1 - k_{\mathrm{sh}}) \ . \tag{B.6}$$

As can be seen clearly in (B.6), $P_{\mathrm{c,max}}$ is not only proportional to the panel power P_{MPP} and k_{sh} but also to the total number of PV panels in the string N_{PV}. Thus, by relating the maximum converter power to the MPP power of the unshaded panels, i.e. $r_{\mathrm{p}} = |P_{\mathrm{c,max}}|/P_{\mathrm{MPP}}$, the number of PV panels in the string can be found, where a certain power ratio r_{p} is reached in dependence of the light transmissibility factor of the shade, k_{sh}, as

$$N_{\mathrm{PV}} = \frac{4 \cdot r_{\mathrm{p}}}{1 - k_{\mathrm{sh}}} \ . \tag{B.7}$$

As an example of this worst case scenario, for a string with $N_{\mathrm{PV}} = 20$ PV panels out of which the first (or last) 10 PV panels are shaded, and a shading scenario of $k_{\mathrm{sh}} = 0.8$ (i.e. the shaded panels deliver 80% of the

power of the unshaded panels P_{MPP}) the diverter module in between the shaded and the unshaded section of the string has to process already 100% of the power generated by an unshaded PV module (P_{MPP}), i.e. $r_{\mathrm{p}} = 1$. Hence, this diverter module has to be designed for the same power rating as the full power converter concepts of **Chapter 3** and would thus nullify the advantages of the partial power conversion. For even more severe shading scenarios (i.e. lower k_{sh}) the situation becomes even worse and the most affected current diverter module has to process multiple times the power of a single PV panel.

B.2.1 Power Limited Current Diverters

The dependency of the required power rating of the current diverter on the shading scenario and the string length complicates the converter design. Therefore, in **Sec. 3.4** a current diverter module (cf. **Fig. 3.34**) is presented with an over-current protection mechanism, which modifies the duty cycle of the switches once the current rating is exceeded. This allows to operate the diverter modules at a predefined power limit. By limiting the power of the diverters, however, it is no longer possible to operate all PV panels in their respective MPPs at all times.

Considering again the worst case, where the string with N_{PV} panels is split into halves, i.e. an unshaded section (each panel delivers the power of P_{MPP}) and a shaded section (each panel delivers a power of $k_{\mathrm{sh}} \cdot P_{\mathrm{MPP}}$), the total theoretically available power of the entire string is

$$P_{\mathrm{th,max}} = \frac{N_{\mathrm{PV}}}{2} \cdot P_{\mathrm{MPP}} \cdot (1 + k_{\mathrm{sh}}) \; . \tag{B.8}$$

This is shown in **Fig. B.3** (normalized to $P_{\mathrm{max}} = N_{\mathrm{PV}} \cdot P_{\mathrm{MPP}}$) as the topmost line with the highest power.
In state-of-the-art systems with only bypass diodes, the string can either be operated at the MPP current level of the unshaded panels, i.e. bypassing the shaded panels, which yields an output power of

$$P_{\mathrm{D2}} = \frac{N_{\mathrm{PV}}}{2} \cdot P_{\mathrm{MPP}} \tag{B.9}$$

which is independent of light transmissibility factor k_{sh} and thus a horizontal line in **Fig. B.3**.
Alternatively, all PV panels can also be operated at the MPP current

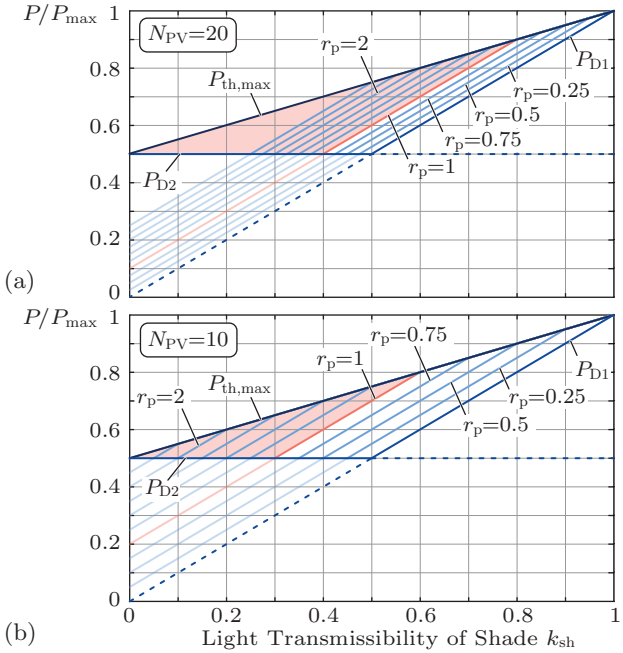

Fig. B.3: Influence of the current diverter power rating r_p on the harvested power of a string with N_PV PV panels for different shading intensities. In the considered worst case scenario, the string of PV panels is divided into two sections, where one half is unshaded and the other half is shaded. The maximum output power of the shaded section is by a factor of k_sh lower than the maximum power of the unshaded section. For the case that only bypass diodes are used without current diverter modules, the achievable output power of the string is given by P_D1 and P_D2 whereas the theoretically available power is given by $P_\mathrm{th,max}$. The red colored area defines the power which can not be harvested even when the diverter modules are sized for the full power of an unshaded PV panel, i.e. for $r_\mathrm{p} = 1$.

level of the shaded panels, i.e. operating the unshaded panels at suboptimal operating points below their MPPs, which results in an output power of

$$P_\mathrm{D1} = \frac{N_\mathrm{PV}}{2} \cdot k_\mathrm{sh} \cdot P_\mathrm{MPP} \ . \tag{B.10}$$

which is directly proportional to k_sh and thus in a diagonal line in

Fig. B.3.
In the case were current diverters with a limited power rating of $r_\mathrm{p} = |P_\mathrm{c,max}|/P_\mathrm{MPP}$ are used, the theoretically available string power can only be harvested above a light transmissibility factor k_sh of the shade of

$$k_\mathrm{sh} \geq 1 - \frac{4 \cdot r_\mathrm{p}}{N_\mathrm{PV}} \tag{B.11}$$

which can be derived from (B.7). If the light transmissiblity falls below this limit, the only way to keep the power of the current diverters at or below their maximum power rating is to operate the unshaded panels at an operating point $P_\mathrm{PV,sub} = k_\mathrm{PV,lim} \cdot P_\mathrm{MPP}$ below their MPP. The factor of power reduction $k_\mathrm{PV,lim}$ can be derived by modifying (B.6) to

$$|P_\mathrm{c,max}| = \frac{N_\mathrm{PV}}{4} \cdot P_\mathrm{MPP} \cdot (k_\mathrm{PV,lim} - k_\mathrm{sh}) \ . \tag{B.12}$$

Inserting the relationship of $|P_\mathrm{c,max}| = r_\mathrm{p} \cdot P_\mathrm{MPP}$ and solving the equation for $k_\mathrm{PV,lim}$ yields

$$k_\mathrm{PV,lim} = k_\mathrm{sh} + \frac{4 \cdot r_\mathrm{p}}{N_\mathrm{PV}} \ . \tag{B.13}$$

Based on this, the total power that can be harvested from a string of PV panels under the worst case shading scenario (i.e. splitting the string into two equal sections), can be derived for power limited current diverters as

$$P_\mathrm{out,lim} = \frac{N_\mathrm{PV}}{2} \cdot P_\mathrm{MPP} \cdot \left(2 \cdot k_\mathrm{sh} + \frac{4 \cdot r_\mathrm{p}}{N_\mathrm{PV}} \right) \tag{B.14}$$

(parallel lines in **Fig. B.3**) which are valid for $k_\mathrm{sh} \leq 1 - \frac{4 \cdot r_\mathrm{p}}{N_\mathrm{PV}}$. For $k_\mathrm{sh} \geq 1 - \frac{4 \cdot r_\mathrm{p}}{N_\mathrm{PV}}$, the total available power can be harvested.

The results of the calculations above are visualized in **Fig. B.3(a)** (normalized to $P_\mathrm{max} = N_\mathrm{PV} \cdot P_\mathrm{MPP}$) for a string length of $N_\mathrm{PV} = 20$. It can be seen, that even if the current diverters are designed for the full power rating of an unshaded PV panel (i.e. $r_\mathrm{p} = 1$, which is the same as full-power converter concepts are requiring), it is not possible to harvest all of the string power $P_\mathrm{th,max}$ for shading factors below $k_\mathrm{sh} \leq 0.8$. The red colored area represents the lost power for $r_\mathrm{p} = 1$. In **Fig. B.3(b)** the results are shown for a shorter string length with $N_\mathrm{PV} = 10$ PV panels. It can be seen, that in this case the maximum available power

can be harvested for lower values of k_{sh}, i.e. $k_{\mathrm{sh}} \geq 0.6$, for the same converter power ratings r_{p}.

As a conclusion, even when the current diverters are designed for the full PV panel power rating, it is not possible to harvest all of the available power of a PV string if the power levels of the shaded panels differ too much from the power of the unshaded PV panels. Especially for longer PV strings, the tolerable power difference can only be e.g. up to 20% for $N_{\mathrm{PV}} = 20$ before the power limit of the most affected diverter module is exceeded. Furthermore, the gain in harvested power compared to using only bypass diodes is limited and even reduces with longer string lengths.

As a protection mechanism, the unshaded PV panels have to be operated below their maximum power levels to avoid overloading the diverters. Thus, full-power converters (cf. **Sec. 3.1**, which are by definition designed for the full power rating of the PV panels, i.e. $r_{\mathrm{p}} = 1$, are a better choice for more severe shading scenarios (i.e. lower values of k_{sh}) since the power level they have to process is decoupled from the power levels of the other PV panels.

B.3 High Step-Down Conversion Ratio "Rainstick" Converters

Another application for current diverter modules are "Rainstick" power supplies with high conversion ratios as presented in **Chapter 5**. In this application, current diverter modules are connected around a stack of series connected capacitors, where e.g. a voltage source is connected in parallel to the stack of capacitors and the load is attached to the bottom capacitor, as depicted in **Fig. B.1(b)**. The achievable conversion ratio thus depends on the number N_{s} of employed capacitors. According to the definitions of **Sec. B.1**, the vector of power sources becomes $\overrightarrow{p_{\mathrm{s}}} = (0, 0, ..., 0, P_{\mathrm{L}})$ in this case. Consequently, the power P_{o} which is directly delivered from the source to the load (i.e. flowing through the series connected capacitors) is

$$P_{\mathrm{o}} = \frac{P_{\mathrm{L}}}{N_{\mathrm{s}}} \, . \tag{B.15}$$

The remaining part of the load power has to be delivered by the diverters. The power level which is processed by each current diverter

module depends on the position of the diverter in the stack and can be determined with (B.3) as

$$\begin{aligned} P_{\mathrm{c},i} &= \frac{1}{N_\mathrm{s}} \left(\underbrace{i \cdot \sum_{j=i+1}^{N_\mathrm{s}} P_{\mathrm{s},j}}_{=P_\mathrm{L} \cdot i} - \underbrace{(N_\mathrm{s} - i) \cdot \sum_{j=1}^{i} P_{\mathrm{s},j}(j)}_{=0} \right) \\ &= \frac{P_\mathrm{L} \cdot i}{N_\mathrm{s}} \,. \end{aligned} \tag{B.16}$$

This means, that the largest amount of power is processed by the converter closest to the load, i.e. at $i = N_\mathrm{s} - 1$ which yields

$$P_{\mathrm{c,max}} = P_\mathrm{L} \cdot \frac{(N_\mathrm{s} - 1)}{N_\mathrm{s}} \tag{B.17}$$

and approaches the load power $P_{\mathrm{c,max}} \approx P_\mathrm{L}$ for high values of N_s. As a result, for large conversion ratios the current diverters have to be designed for almost the same power rating as the load power. Furthermore, the total system efficiency contains a multiplication of the efficiencies of the individual diverter modules according to (5.3). As an advantage of this type of voltage conversion, however, due to the modular structure of the system, the diverter modules have to be designed for only a fraction of the entire DC-link voltage which enables the use of semiconductors with reduced blocking voltage compared to full-power concepts. In addition, the modular structure allows for an easy realization of the system by employing multiple diverters modules with identical hardware. Another advantage is the simple and robust control of each diverter module with fixed duty cycles of 50% without any communication between the divertes. Thus, this conversion concept is especially well suited in high-voltage and high-power environments (e.g. traction applications) where low-voltage equipment with a low rated power has to be supplied and a high conversion ratio is required (e.g. as an auxiliary supply). For this type of application the limited conversion efficiency of this supply is of minor concern since it will not affect the efficiency of the entire system which has a power rating that is magnitudes larger than the auxiliary power.

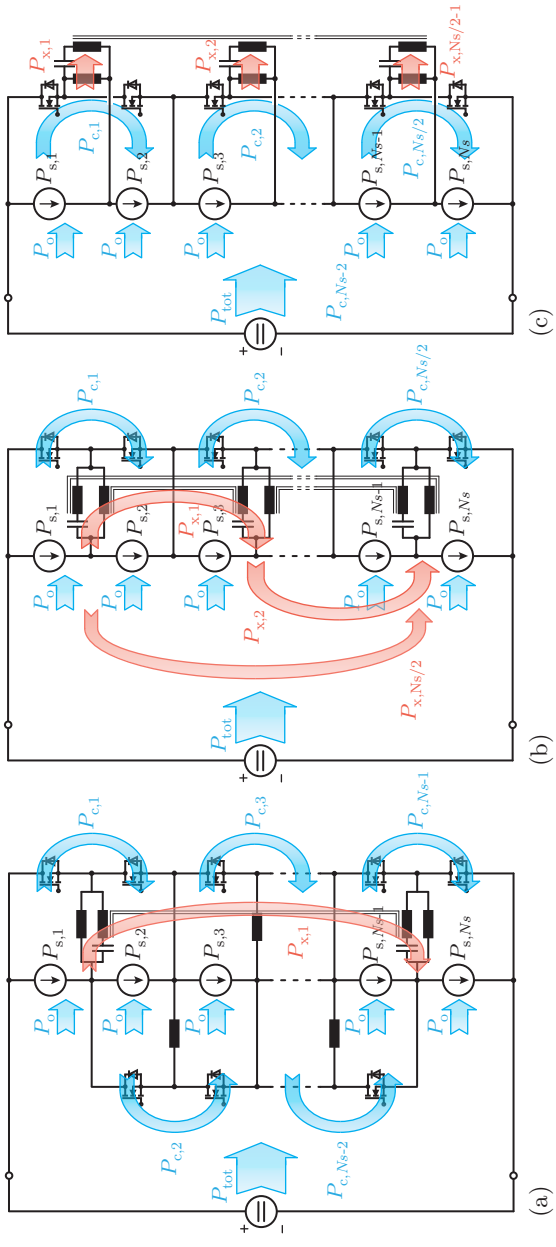

Fig. B.4: Current diverter concepts employing coupled inductors: (a) daisy chain configuration where coupled inductors allow to transfer power from the first diverter module to the last one, and vice versa; (b) use of coupled inductors to reduce the overall component count by reducing the number of required diverter modules; (c) coupling all diverter modules on a common core which enables the direct power transfer between all diverter modules.

B.4 Coupled Inductor Concepts

As mentioned in the previous sections, a disadvantage of the current diverter concept is the influence of the number of sources N_s on the power transfer through the diverter modules. This is especially unfavorable for the application of this concept in PV energy systems, but is also a disadvantage for the Rainstick converters, where each diverter module has to be designed for a power rating (almost) equal to the load power. One possibility to mitigate or even remedy this problem is to couple the inductors of diverter modules, as will be described in the below.

The first option is the addition of coupled inductors in the first and last diverter module. Together with series connected capacitors, this creates a series resonant converter (SRC) structure as shown in **Fig. B.4(a)**, and/or allows to transfer power between these two diverter modules. The resonant frequency of the SRC (defined by the leakage inductance of the coupled inductors and the resonant capacitor) can be tuned to the switching frequency of the diverter modules in order to operate the SRC in HC-DCM [91]. The SRC allows to transfer power directly between the first and the last module which creates a daisy chain (i.e. ring) structure. As a result, the maximum power which is transferred in any diverter module or the module employing the coupled inductor is half of the maximum power of the uncoupled structure. This can be intuitively explained, by considering that the power flow can be divided into two paths in the ring structure. The disadvantage of this option, however, is the required voltage isolation of the coupled inductors which has to be rated for the full input voltage.

The second option is to couple each diverter module with the neighboring diverter modules. With this arrangement, the SRC topology can be used to minimize the component count of the system, as shown in **Fig. B.4(b)**. Instead of employing $N_s - 1$ inductors and $2 \cdot (N_s - 1)$ switches as in the uncoupled structure, the proposed concept with SRCs employs only N_s switches and $N_s/2$ sets of coupled inductors with $N_s/2$ capacitors for the resonant operation. The SRCs are used to transfer power from two sources to another two sources, e.g. the power $P_{x,1}$ is transferred from $P_{s,1}$ to $P_{s,3}$ and $P_{s,2}$ to $P_{s,4}$, and vice versa. In order to balance the power between $P_{s,1}$ and $P_{s,2}$ or $P_{s,3}$ and $P_{s,4}$ etc., the magnetizing currents of the SRC converters are used. It should be noted, that the magnetizing current will have a DC-offset if the power levels of the two sources on one side of the SRC are unequal. Thus, the magne-

tizing current can only balance the sources on the side of an SRC where no resonant capacitor is present. This is also visualized in **Fig. B.5**, where the current i_p can have a DC-offset if the voltages V_1 and V_2 are unequal (i.e. a DC-offset in the magnetizing current is created in order to balance the voltages V_1 and V_2), while the resonant capacitor C_res between V_3 and V_4 also functions as a DC-blocking capacitor, which prevents current i_s from having a DC-offset. In case the resonant capacitors are placed on both sides of the coupled inductors, additional inductors have to be employed in at least one diverter module, which then allows to balance two neighboring sources.

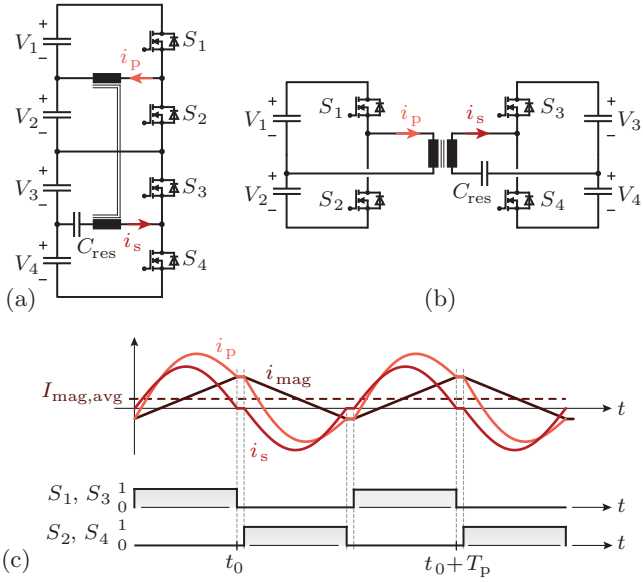

Fig. B.5: Detailed explanation of the operation of diverter modules with coupled inductors: (a) coupled inductors as proposed for the current diverters. Splitting the stack of capacitors in (a) between C_2 and C_3 yields the equivalent series resonant converter (SRC) in (b); (c) characteristic current waveforms and switching patterns of the SRC where the current i_p is an addition of the current i_s and the magnetizing current i_mag. Due to the presence of the resonant capacitor C_res, the current of i_s cannot show any DC-offset in , while a DC-offset can result in the current i_mag (and thus also in i_p) if the voltages V_1 and V_2 are unequal.

The third option for further minimizing the power rating of the diverter modules is to assemble all coupled inductors on a common core, as visualized in **Fig. B.4(c)**. This does not only reduce the number of coupled inductors to just one multi-terminal coupling device, but also enables the direct power flow between all diverter modules. Each SRC transfers the power level of

$$P_{\mathrm{x},i} = \underbrace{\frac{2}{N_\mathrm{s}} \cdot \sum_{j=1}^{N_\mathrm{s}} P_{\mathrm{s},j}}_{\text{Twice the average of all sources}} - \underbrace{\sum_{j=2i-1}^{2i} P_{\mathrm{s},j}}_{\text{Sources at diverter module } i} . \tag{B.18}$$

The power transferred via the uncoupled inductors can be calculated as

$$P_{\mathrm{c},i} = \frac{1}{2}\left(P_{\mathrm{s},2i} - P_{\mathrm{s},(2i-1)}\right) \tag{B.19}$$

which is just required to balance the two sources on one side of the SRC modules. The option shown in **Fig. B.4(c)** has uncoupled inductors in every diverter module such that all modules are identical. Alternatively, the balancing of the power sources will also work if only one diverter module is equipped with an uncoupled inductor. In that case, since the SRCs are balancing only the sources with even numbers and also the sources with odd numbers, this single uncoupled inductor is used as the balancing module between the group of sources with even numbers and the group of sources with odd numbers. It should be noted, however, that besides the advantage of a reduced number of components, this option has the drawback that in the worst case where the even numbered sources have very different power levels than the odd numbered sources, the diverter with the uncoupled inductor has to process very high power levels (i.e. similar to the situation in PV systems where the diverter module in between the shaded and unshaded section requires the highest power rating).

When applying the option of **Fig. B.4(c)** to the worst case scenario in PV energy systems (i.e. the PV string is divided into a shaded and an unshaded half) the maximum power level that has to be processed by any SRC equals

$$P_{\mathrm{x,max}} = P_{\mathrm{MPP}} \cdot (1 - k_{\mathrm{sh}}) \tag{B.20}$$

which is independent of the number of PV panels in the string and is just the power difference between the shaded and the unshaded panels which is always lower than the power processed by full-power converters.

Despite the various advantages there are also some disadvantages resulting from the employment of coupled inductors. Foremost, the operation of the diverter modules can no longer function without synchronizing the switching patterns between the diverters. This mandates the implementation of some sort of communication or synchronization signal among the diverters which leads to additional hardware and wiring effort. Another drawback especially of the concept with only one common core for coupling the diverters lies in the loss of modularity. The system and particularly the multi-terminal coupled inductor has to be designed for a specific number of sources and can no longer be easily extended for larger numbers of sources as given for the uncoupled system.

B.5 Conclusion

The concept of voltage balancing with current diverter modules can be utilized in various different applications ranging from SOC equalization of batteries to mitigating mismatch effects in PV systems. Therefore, a universal power flow analysis is introduced in this chapter, which can be applied to any application of current diverter modules. This analysis allows to derive the power transferred by each diverter module, which is a mandatory requirement for properly designing the diverter modules. The application of the power flow analysis is shown with the example of PV energy systems and a power supply with a high conversion ratio. As a result of the analysis it is revealed, that in PV systems the shading scenario as well as the string length take a great influence on the power rating of the current diverter modules. This can necessitate a dimensioning of the diverter modules for a higher power level than the rated power of the PV panels.

For the “Rainstick” power supplies with high conversion ratios it is shown, that the power rating of the diverter modules approaches the load power level for large numbers of diverters. The advantages of this concept, however, are the modularity of the system, which allows an easy adjustment for different conversion ratios, and the absence of any communication between the diverter modules due to the operation with fixed duty cycles of 50%. Additionally, none of the employed compo-

nents has to be rated for the full input voltage. Thus, this concept is especially well suited for high-voltage environments where a step-down conversion is required for low-power equipment, e.g. as an auxiliary supply.

Moreover, the concept of coupling the inductors of the diverter modules is presented, which allows to reduce the required power rating of the diverter modules and/or to minimize the number of required diverter modules.

C

ZVS of Power MOSFETs Revisited

For the design and optimization of a converter system with ZVS it is crucial to identify the conditions under which soft-switching can be achieved. A basic structure enabling ZVS is a semiconductor half-bridge with an inductive element connected to the midpoint of the half-bridge as given for a phase-shift full-bridge converter (cf. **Chapter 4**) and other topologies depicted in **Fig. C.1**. In order to calculate the required energy stored in the inductive component at the beginning of a switching transition to achieve soft-switching a practical approach such as presented in [173] can be used.
This chapter however, introduces an analytical approach to specify the conditions for ZVS which only relies on data sheet values of the semiconductors. At first, the non-linear behavior of the parasitic MOSFET capacitances is described in **Sec. C.1**. **Sec. C.2** analyzes the conditions to achieve ideal soft-switching. In **Sec. C.3** analytical formulas are presented that allow to calculate the losses associated with incomplete soft-switching, i.e. the turn-on of switches at non-zero voltage. The derived equations are validated with measurements on different hardware setups with different types of semiconductors in **Sec. C.4**. Finally, **Sec. C.5** summarizes the key results.

C.1 Non-linear Parasitic MOSFET Capacitances

It is widely known, that the parasitic output capacitance C_{oss} of MOSFETs exhibits a non-linear dependency on the applied drain-source voltage V_{DS}, which is shown in **Fig. C.2(a)** for a low-voltage Si MOS-

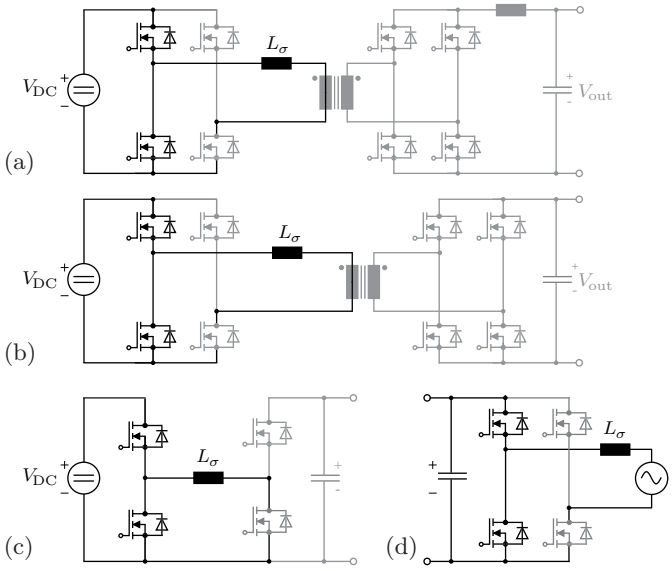

Fig. C.1: Popular ZVS converter topologies: (a) phase-shift full-bridge converter, (b) Dual Active Bridge converter, (c) cascaded buck-boost converter with constant switching frequency ZVS modulation [6] and (d) Triangular Current Mode (TCM) PFC rectifier. The basic structure of all soft-switching topologies consisting of a MOSFET bridge-leg and an inductor/inductance L_σ is highlighted.

FET (BS046N100NS3 / Infineon). Due to this non-linearity, the charge stored in parasitic capacitances is also a non-linear function of the applied voltage, as shown **Fig. C.2(b)** for the charge Q_{oss} stored in C_{oss}. In order to facilitate the modeling of MOSFETs, a linear charge-equivalent capacitance $C_{\mathrm{Q,eq}}$ can be introduced which exhibits the same amount of stored charge as the non-linear capacitance at a given drain-source voltage V_{DS} [32], i.e.

$$C_{\mathrm{Q,eq}}(V_{\mathrm{DS}}) = \frac{Q_{\mathrm{oss}}(V_{\mathrm{DS}})}{V_{\mathrm{DS}}} = \frac{\int_0^{V_{\mathrm{DS}}} C_{\mathrm{oss}}(v)\,\mathrm{d}v}{V_{\mathrm{DS}}}. \tag{C.1}$$

In a similar way, the energy E_{oss} stored in the non-linear capacitance C_{oss} can be considered. In **Fig. C.2(b)** the blue shaded area enclosed between the graph of the charge Q_{oss} and the y-axis equals the energy

which is stored in C_{oss} at a given voltage V_{DS}. Thus, a linear energy-equivalent capacitance $C_{\mathrm{E,eq}}$ that stores the same amount of energy as C_{oss} at a selected voltage V_{DS} needs to have the same enclosed area, i.e.

$$C_{\mathrm{E,eq}}(V_{\mathrm{DS}}) = \frac{2 \cdot E_{\mathrm{oss}}(V_{\mathrm{DS}})}{V_{\mathrm{DS}}^2} \stackrel{!}{=} \frac{2 \cdot \int_0^{V_{\mathrm{DS}}} v \cdot C_{\mathrm{oss}}(v)\,\mathrm{d}v}{V_{\mathrm{DS}}^2}. \tag{C.2}$$

As a result, the energy-equivalent capacitance $C_{\mathrm{E,eq}}$ and the charge-equivalent capacitance $C_{\mathrm{Q,eq}}$ can be calculated for every drain-source voltage V_{DS} (cf. **Fig. C.2(c)**). It can be seen that the values of these capacitances differ for the considered case by a factor of up to $C_{\mathrm{Q,eq}}(V_{\mathrm{DS,max}})/C_{\mathrm{E,eq}}(V_{\mathrm{DS,max}}) = 1.5$. For other MOSFET devices, such as super-junction MOSFETs, the equivalent capacitances may even differ up to a factor of 4 to 5. This difference implies the necessity to clarify which equivalent capacitance has to be used in the case of modeling the soft-switching behavior of MOSFETs.

C.2 Conditions for Ideal Soft-Switching

In order to avoid the losses caused by hard-switching transitions of MOSFETs, zero-voltage switching (ZVS) is commonly applied. This requires the presence of an impressed inductive current which charges/discharges the output capacitances of the MOSFETs within a bridge-leg during the interlocking time of the associated gate signals, as visualized in **Fig. C.3** for a transition where switch S_2 turns off and S_1 turns on. The required energy of the inductor for a complete soft-switching transition can be found by considering the energy balance of

$$E_{\mathrm{initial}} + E_{\mathrm{delivered}} = E_{\mathrm{final}} + E_{\mathrm{dissipated}} \tag{C.3}$$

where E_{initial} denotes the energy within the system at $t = t_1$ and E_{final} denotes the energy after the ZVS transition. $E_{\mathrm{delivered}}$ is the energy which is delivered by the DC source and $E_{\mathrm{dissipated}}$ is the energy which is dissipated during the ZVS transition which is assumed to be $E_{\mathrm{dissipated}} = 0$. Furthermore, it is assumed that the switches S_1 and S_2 in the half-bridge are equal, which means that they exhibit the same non-linear characteristic of C_{oss} in dependency of V_{DS}. This is also typically the case in half-bridge configurations with bidirectional power flow capability.
At the beginning of the transition ($t < t_1$) the current i_{L} of the inductor

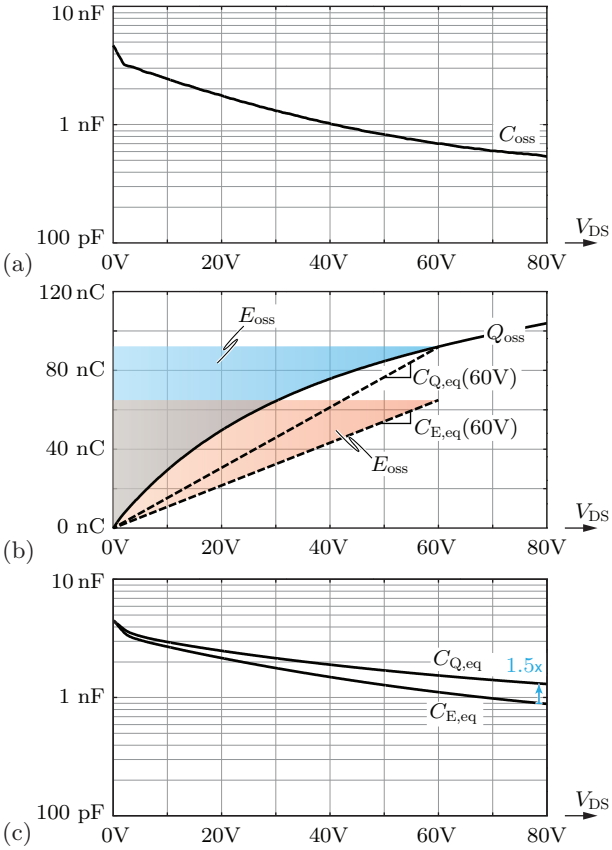

Fig. C.2: Non-linear behavior of parasitic MOSFET capacitances: (a) parasitic capacitance C_{oss} in dependency of the applied drain-source voltage V_{DS} as provided by the datasheet (BS046N100NS3 / Infineon); (b) charge Q_{oss} stored in C_{oss} as a function of V_{DS}, charge-equivalent capacitance $C_{Q,eq}$ and energy-equivalent capacitance $C_{E,eq}$ for a drain-source voltage of $V_{DS} = 60\,V$; (c) calculated values of $C_{Q,eq}$ and $C_{E,eq}$ in dependence of the drain-source voltage.

is free-wheeling through S_2 and the output capacitance $C_{oss,1}$ of switch S_1 is charged to the source voltage V_{DC}. Assuming a linear inductance, the energy within the system for $t < t_1$ is therefore equal to

$$E_{\text{initial}} = E_{\text{oss}}(V_{\text{DC}}) + \frac{1}{2} L I_1^2. \tag{C.4}$$

During the switching transition ($t_1 < t < t_2$), the inductor and the capacitances of the switches are forming a resonant circuit. The current i_{L} is split up between both capacitances and charges $C_{\text{oss},2}$ and discharges $C_{\text{oss},1}$. In the case of a complete ZVS transition at the boundary to loosing ZVS, the charging/discharging process is finished at the same time (t_2) when the inductor current reaches $i_{\text{L}} = 0\,\text{A}$ which is also when switch S_1 is turned on. Thus, the energy in the system after the ZVS transition equals

$$E_{\text{final}} = E_{\text{oss}}(V_{\text{DC}}), \tag{C.5}$$

and the energy received by the source during the transition equals

$$E_{\text{delivered}} = -Q_{\text{oss}}(V_{\text{DC}}) \cdot V_{\text{DC}} \tag{C.6}$$

since the charge of switch S_1 was moved by i_{S} to the source with voltage V_{DC}. As a result, the energy balance of (C.3) reveals that the requirement for a complete zero-voltage transition is given by

$$\frac{1}{2} L I_1^2 \geq Q_{\text{oss}}(V_{\text{DC}}) \cdot V_{\text{DC}}. \tag{C.7}$$

This requires the evaluation of the charge-equivalent (and *not* the energy-equivalent [138, 174–176]) capacitance at the voltage V_{DC}

$$\frac{1}{2} L I_1^2 \geq C_{\text{Q,eq}}(V_{\text{DC}}) \cdot V_{\text{DC}}^2. \tag{C.8}$$

Please note, that additional parasitic capacitances of the switch node (e.g. PCB capacitances and the parasitic capacitance of the inductor) also influence the required energy of the inductor for soft-switching. The parasitic capacitances are assumed to be linear with respect to their capacitance value in dependency of the applied voltage, which allows to lump them into a total parasitic capacitance C_{par}. Accordingly, considering **Fig. C.3** the energy term $\frac{1}{2} C_{\text{par}} V_{\text{DC}}^2$ has to be added to the right-hand sides of (C.7) and (C.8).

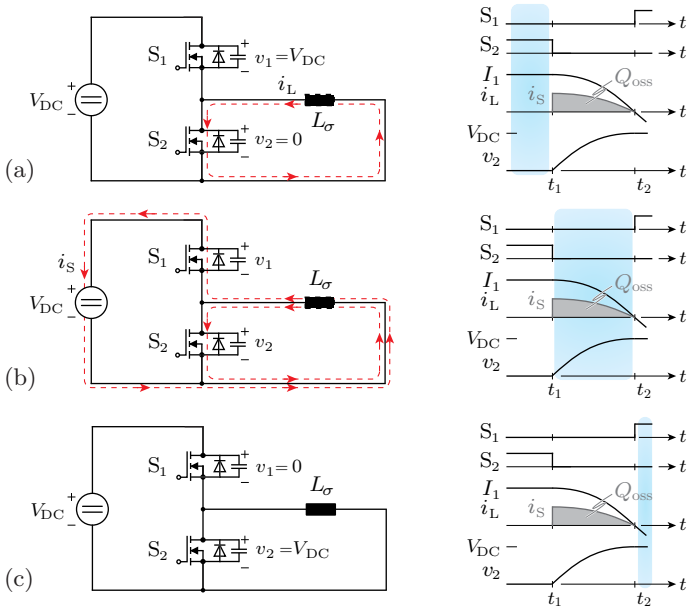

Fig. C.3: Soft-switching transition of a MOSFET bridge-leg and an inductor L: (a) free-wheeling interval with inductor current $i_\mathrm{L} = I_1$; (b) switch S_2 turns off and resonant transition starts with an additional current path through the DC source. (For simplicity reasons the parasitic output capacitances are assumed to be linear); (c) end of transition when the drain-source voltage of S_2 has reached the source voltage, i.e. $v_2 = V_\mathrm{DC}$, and switch S_1 turns on at zero voltage. As a result of the transition, the charge Q_oss was moved from switch S_1 to the DC-source and the energy of the inductor L_σ is zero whereas the total energy stored in the MOSFET bridge-leg remains unchanged. Thus, the condition for complete soft-switching equals $\frac{1}{2} L I_1^2 \geq Q_\mathrm{oss}(V_\mathrm{DC}) \cdot V_\mathrm{DC}$.

ZVS losses due to non-idealities

Even if the above mentioned condition for ZVS is fulfilled, switching losses might still be measured due to following two effects:

- At large inductor currents, turn-off losses can occur if the gate drive circuitry is too slow to turn-off of the semiconductor before the drain-source voltage rises. The resulting overlapping of drain-source current and drain-source voltage leads to losses in

the semiconductor.

- The charging/discharging process of the output capacitances creates additional losses [144]. For SiC MOSFETs, GaN HEMTs, and low-voltage Si MOSFETs, this effect is mainly of resistive nature and might lead to a dissipation of up to 10% of the stored energy in the output capacitance. For super-junction Si MOSFETs, however, the loss mechanism is a combination of a resistive and a diode-like component and might dissipate more than 50% of the stored energy. More details about the C_{oss} related losses of super-junction MOSFETs can be found in [144, 177]. As a result, a significantly larger energy has to be stored in L to achieve ZVS and even with ZVS significant switching losses can occur.

C.3 Incomplete Soft-Switching

Even if all non-idealities of real MOSFET circuits (cf. **Sec. C.2**) are disregarded, the soft-switching transition can result in losses if the condition for ZVS, (C.7), is not fulfilled and/or incomplete soft-switching (iZVS) occurs. This means, that there is still a voltage ΔV present across the switch S_1 that turns on after the resonant transition. In order to calculate the remaining voltage ΔV, the energy expression E_{final} has to be revised to

$$E_{\text{final}} = E_{\text{oss}}(V_{\text{DC}} - \Delta V) + E_{\text{oss}}(\Delta V) \tag{C.9}$$

and the energy delivered by the source has to be changed to

$$E_{\text{delivered}} = -\left(Q_{\text{oss}}(V_{\text{DC}}) - Q_{\text{oss}}(\Delta V)\right) \cdot V_{\text{DC}} \ . \tag{C.10}$$

The value of ΔV can then be found by solving the energy balance of (C.3) (again for $E_{\text{dissipated}} = 0$). Please note, that additional parasitic capacitances and resistive losses are not included in this equation.
In the incomplete ZVS transition, switch S_1 turns on while $C_{\text{oss},1}$ is still charged to ΔV, which dissipates a certain amount of energy that can be derived by solving the energy balance of

$$E_{\text{diss,iZVS}} = E_{\text{initial,iZVS}} - E_{\text{final,iZVS}} + E_{\text{delivered,iZVS}} \ . \tag{C.11}$$

Before S_1 turns on, the energy within the system is equal to

$$E_{\text{initial,iZVS}} = E_{\text{oss}}(V_{\text{DC}} - \Delta V) + E_{\text{oss}}(\Delta V) \ . \tag{C.12}$$

After S_1 has turned on, $C_{\text{oss},2}$ of switch S_2 is charged to V_{DC}, therefore

$$E_{\text{final,iZVS}} = E_{\text{oss}}(V_{\text{DC}}) \ . \tag{C.13}$$

In order to charge the output capacitance of S_2 to V_{DC}, the source has to deliver the remaining charge ΔQ_{S2} which is

$$\Delta Q_{\text{S2}} = Q_{\text{oss}}(V_{\text{DC}}) - Q_{\text{oss}}(V_{\text{DC}} - \Delta V) \tag{C.14}$$

and thus has to deliver the energy

$$E_{\text{delivered,iZVS}} = \Delta Q_{\text{S2}} \cdot V_{\text{DC}} \ . \tag{C.15}$$

As a result, the dissipated energy of the incomplete ZVS transition can be derived and interpreted as

$$\begin{aligned} E_{\text{diss,iZVS}} \quad = \quad & \underbrace{E_{\text{oss}}(\Delta V)}_{\text{① Energy dissipated in } S_1 \text{ when } S_1 \text{ turns on}} \\ & + \quad \underbrace{\Delta Q_{\text{S2}} \cdot V_{\text{DC}}}_{\text{② Energy provided by source during turn-on of } S_1} \\ & - \quad \underbrace{\left(E_{\text{oss}}(V_{\text{DC}}) - E_{\text{oss}}(V_{\text{DC}} - \Delta V)\right)}_{\text{Share of energy of ② which is stored in } C_{\text{oss}} \text{ of } S_2} \end{aligned} \tag{C.16}$$

For the case of a complete soft-switching transition (i.e. $\Delta V \to 0$) the above equation yields $E_{\text{diss,iZVS}} \to 0$. For the second limit case of $\Delta V \to V_{\text{DC}}$, which denotes hard-switching, the energy

$$E_{\text{diss,iZVS}} \to Q_{\text{oss}}(V_{\text{DC}}) \cdot V_{\text{DC}} = C_{\text{Q,eq}} \cdot V_{\text{DC}}^2 \tag{C.17}$$

can be used to estimate the losses which occur due to the parasitic output capacitance in the event of hard-switching [32]. Please note again, that in the case of incomplete soft-switching and also in the case of (full) hard-switching, the charge-equivalent and *not* the energy-equivalent capacitance (as frequently used in literature) is relevant and therefore the actual switching losses are greater than switching losses estimated using the energy equivalent capacitance. Furthermore, non-idealities resulting in additional losses are not included in the equations.

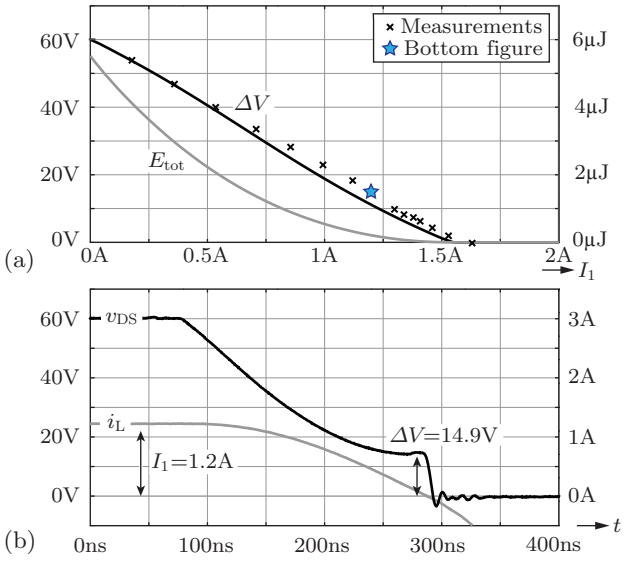

Fig. C.4: Measurements of an incomplete ZVS transition with a MOSFET bridge-leg (BS046N100NS3 / Infineon) and an inductor with $L = 4.6\,\mu\text{H}$: (a) calculated and measured remaining voltage ΔV (cf. (*C*.9)) across switch S_2 for different initial values of inductor current $i_L = I_1$ and the associated dissipated energy $E_{\text{diss,iZVS}}$ of an incomplete ZVS transition with remaining voltage ΔV; (b) measured waveform of the drain-source voltage v_{DS} of switch S_2 and inductor current i_L for an initial inductor current value of $i_L = 1.2\,\text{A}$.

C.4 Experimental Validation

The theoretical derivations of the previous sections have been experimentally validated and the results are shown in the following.

C.4.1 Incomplete Soft-Switching Transition

The incomplete soft-switching process was tested with a bridge-leg containing two low voltage MOSFETs (BS046N100NS3 / Infineon) connected to a voltage source with $V_{DC} = 60\,\text{V}$ and an inductor with $L = 4.6\,\mu\text{H}$. The voltage ΔV, remaining at the switch node after an incomplete soft-switching process, was calculated according to (C.4) and (C.9) and is shown in **Fig. C.4(a)** for different values of the initial in-

Tab. C.1: Detailed comparison of selected incomplete ZVS (iZVS) loss measurement results with calculated values.

V_{DC}	ΔV	$E_{\mathrm{diss,iZVS,meas}}$	$E_{\mathrm{diss,iZVS,calc}}$	Error
200 V	200 V	8.26 µJ	8.39 µJ	1.5%
200 V	100 V	1.26 µJ	1.35 µJ	7.0%
200 V	50 V	0.273 µJ	0.318 µJ	13.9%
400 V	300 V	11.6 µJ	11.4 µJ	-1.8%
400 V	100 V	1.11 µJ	1.11 µJ	0.5%
600 V	400 V	18.1 µJ	18.1 µJ	0.4%
600 V	200 V	4.13 µJ	4.3 µJ	3.9%

ductor current I_1 and compared to measurement results. The difference between the measurements and calculations can be attributed to ohmic losses in the conduction path (i.e. coil winding, MOSFETs, PCB) and to additional layout dependent capacitances which require additional energy to be charged/discharged. In addition, the calculated value of the energy $E_{\mathrm{diss,iZVS}}$ which is dissipated at this incomplete ZVS transition is also shown as a function of the initial inductor current. The transient waveforms of the inductor current and the bridge leg voltage are depicted for an initial inductor current of $I_1 = 1.2\,\mathrm{A}$ in **Fig. C.4(b)**.

C.4.2 Loss Measurements

In order to verify the derived formulas of **Sec. C.3** of the switching losses occuring in case of incomplete soft-switching, a measurement setup for precise switching loss measurements (cf. **Fig. C.5(a)**) was used with SiC MOSFETs (C2M0080120D / Cree). In this setup, the current and voltage waveforms across the top switch S_1 are measured by means of a high bandwith oscilloscope and a current shunt which allows to determine the energy released or stored by this switch during the incomplete soft-switching process and thus to verify equation (C.16). The experimental setup contains specific layout dependent parasitic capacitances (e.g. probes, PCB) that are included into the calculation by means of a lumped capacitance, which was measured to amount to $C_{\mathrm{par}} = 123\,\mathrm{pF}$. The energy stored in the parasitic capacitances is also dissipated in switch S_1 and has to be included into the calculations,

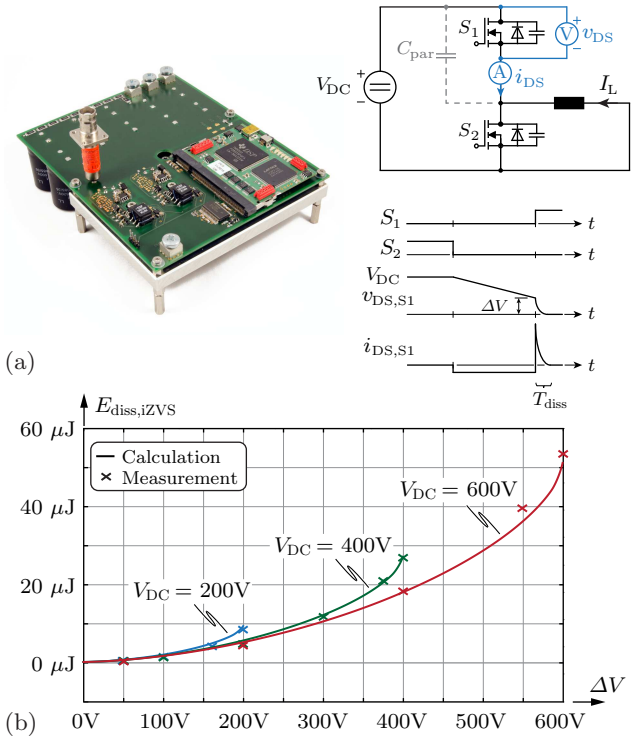

Fig. C.5: Experimental verification of switching energies for incomplete ZVS: (a)measurement setup to determine the dissipated energy of S_1 which turns on with a non-zero drain-source voltage of $v_{DS,S1} = \Delta V$. The test bench employs a digital controller to generate the gate signals of the double pulse tests. High-bandwith 1 GHz current shunts (SDN-414-10 / T&M Research) are used to measure the currents by means of a coaxial cable whereas the voltages are measured with high-voltage passive probes. The schematic waveforms are split into the resonant transition phase (T_{res}) where energy is recovered from S_1 and a dissipative phase (T_{diss}) which occurs when switch S_1 is turned on. The total dissipated energy $E_{diss,iZVS}$ for different DC-link voltage V_{DC} and different remaining voltages ΔV is shown in (b) as a comparison between measured and calculated values according to (C.16).

which yields

$$E_{diss,iZVS,calc} = E_{diss,iZVS} + \frac{1}{2} C_{par} \Delta V^2. \tag{C.18}$$

The measurements were conducted for different levels of DC-link voltage V_{DC} and different levels of remaining midpoint voltage ΔV. The results are visualized in **Fig. C.5(b)** and a detailed overview of the measurement results is provided in **Tab. C.1**. The theory is confirmed by the measurements with a high accuracy.

C.5 Conclusion

In order to determine whether soft-switching can be achieved in a circuit with a MOSFET bridge-leg and an inductor carrying the initial current $i_{\mathrm{L}} = I_1$ the stored charge Q_{oss} of the MOSFETs has to be considered and the condition

$$\frac{1}{2} L I_1^2 \geq Q_{\mathrm{oss}}(V_{\mathrm{DC}}) \cdot V_{\mathrm{DC}} \tag{C.19}$$

has to be fulfilled. For the case that the condition for complete soft-switching is not fulfilled the additional losses of the incomplete soft-switching process can be calculated based on formula (C.16). The formulas also allow to calculate the losses which occur due to the parasitic output capacitances in the event of (full) hard-switching. The derived equations have been validated with high accuracy on dedicated measurement setups with low voltage Si MOSFETs and high voltage SiC MOSFETs.

Nomenclature

Abbreviations

4D	Four Dimensional
AC	Alternating Current
CCM	Continuous Conduction Mode
CLF	Component Load Factor
CM	Common-Mode
CRC	Cyclic Redundancy Check
DAB	Dual-Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
DM	Differential Mode
DOI	Digital Object Identifier
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FPC	Full-Power Converter
FPGA	Field Programmable Gate Array
GaN	Gallium Nitride
iGSE	Improved Generalized Steinmetz Equation
GSE	Generalized Steinmetz Equation
HB	Half-Bridge
HC-DCM	Half-Cycle Discontinuous Conduction Mode
HCS	Half-Cycle Skipping
HEMT	High-Electron-Mobility Transistor
IGBT	Insulated-Gate Bipolar Transistor
IPOP	Input-Parallel Output-Parallel
IPOS	Input-Parallel Output-Series
ISOP	Input-Series Output-Parallel
ISOS	Input-Series Output-Series
LCS	Line Cycle Skipping
MC	Multi-Cell
MIC	(PV) Module Integrated Converter
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
PCB	Printed Circuit Board

PFC	Power Factor Correction
P-FPC	Parallel-connected Full-Power Converter
P-PPC	Parallel-connected Partial-Power Converter
PPC	Partial-Power Converter
PSFB	Phase-Shift Full-Bridge
PWM	Pulse-Width Modulation
RMS	Root-Mean-Square
RSTC	Rainstick Converter
Si	Silicon
S-PPC	Series-connected Partial-Power Converter
S-FPC	Series-connected Full-Power Converter
SiC	Silicon Carbide
SR	Synchronous Rectification
SRC	Series Resonant Converter
TCM	Triangular Current Mode
iZVS	Incomplete Zero Current Switching
ZVS	Zero Voltage Switching

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