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Author(s):
Peftitsis, Dimosthenis; Jehle, Andreas; Biela, Jürgen

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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Laboratory for High
Power Electronic Systems

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Peftitsis D., Jehle A., Biela J.
Power Electronic Systems Laboratory, ETH Zürich
Physikstrasse 3, 8092 Zürich, Switzerland

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Dimosthenis Peftitsis, Andreas Jehle and Jürgen Biela
Lab for High Power Electronics Systems, ETH Zürich
Email: dimosthenis.peftitsis@ntnu.no, URL: http://www.hpe.ee.ethz.ch/

Keywords

<<dc circuit breaker>>, <<HVDC>>, <<Multi-terminal HVDC>>, <<Short-circuit faults>>

Abstract

This paper presents a performance evaluation in terms of applicability, response times, energy dissipation, passive components and power semiconductors requirements of the four most promising hybrid DC circuit breaker concepts for HVDC grids. Specific design guidelines for all of the hybrid DC circuit breakers are also shown. The evaluation of the hybrid DC circuit breakers has been performed using PLECS.

1 Introduction

In terms of power losses and bidirectional active power control flexibility, high-voltage direct current (HVDC) transmission systems exhibit an advantageous performance compared to state-of-the-art alternative current (AC) solutions. There are basically two converter technologies for HVDC systems, namely the *Line-Commutated Converter, (LCC)*, and the *Voltage-Source-Converter, (VSC)* [1, 2]. LCC-based HVDC systems are well-established for large-scale energy transmission systems (>1 GW). On the other hand, VSC HVDC systems are found more attractive for smaller scale electricity transmission systems. In future point-to-point HVDC transmission lines both LCC and VSC-based systems are interesting solutions. However, for multi-terminal HVDC systems VSCs are the most attractive solutions which offers active and reactive power control flexibility, power reversal and a stiff voltage on the DC side [2]. A drawback of VSC-based HVDC systems is that they are more vulnerable to direct current faults than the LCC technology. Thus, DC circuit breakers (DC-CBs) are required in VSC-based HVDC systems.

In point-to-point VSC HVDC systems DC-CBs must have shorter response times than breakers in AC grids which require a few cycles to clear faults, because of the semiconductors which are generally not able to conduct the large fault current peaks. In multi-terminal HVDC systems, DC CBs are vital components for a stable operation because they are able to disconnect a faulty line from the nodes, enabling the rest of the interconnected lines to operate without interruption. These two examples reflect the need for fast DC CBs in the future HVDC grids.

From the DC CB point-of-view, there are three requirements listed in [2], which must be fulfilled for a reliable operation. 1) A zero-crossing of the breaker current must be created, since a direct fault current always increases. 2) Moreover, the DC CB must be able to withstand the transient interruption voltage (TIV) after the clearing of the fault and to dissipate the residual energy of the DC-line. 3) Low losses at normal operation of the breaker. For addressing these challenges, various DC CBs concepts have been presented. Among the first DC CBs concepts a mechanical circuit breaker (MCB) employing a resonant circuit is found [3, 4]. Under a fault condition, the resonant circuit is triggered in order to create an artificial zero-crossing of the CB current. Nevertheless, this concept is associated with relatively long response times (50-60 ms), while the dimensioning of the resonant tank as such, is not trivial either. The response time can be reduced if a pure semiconductor-based CB without employing a MCB is used. This is, however, done at the cost of higher conduction losses [4, 5], also requiring a bulky cooling system. Consequently, a very tempting solution is the so-called "hybrid DC CB" (hDC-CB), which is a combination of MCBs with power electronics circuits, so that very low conduction losses at steady-state and fast fault clearing are possible at the same time.

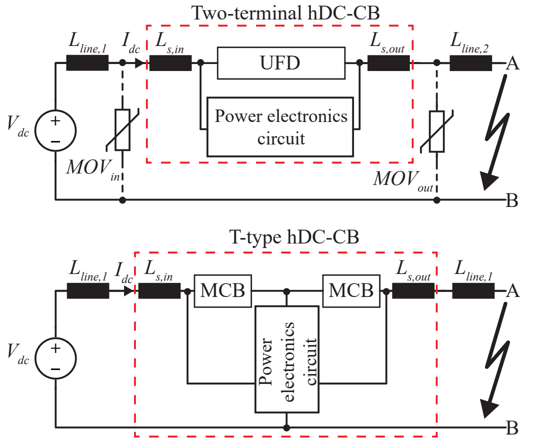

Figure 1: Block diagrams of the two-terminal/T-type hybrid DC CBs.

In terms of current commutation from the mechanical switch (MS), there are two major hDC-CB concepts proposed in literature. Fig. 1 shows block diagrams of these two hDC-CB concepts where the connection of the MS and the power electronics circuits are visible. The first concept is a two-terminal

CB connected in series with the DC-line. The main idea of this hDC-CBs is to bypass the ultra-fast disconnector (UFD) by an active switch and create a zero-current condition in the UFD. Two alternative realizations of this concept are presented in [6] and [7]. Fault current commutation branches connected in parallel to the UFD and employing solid-state switches are required in order to bypass the fault current. The protection against over-voltages in the DC-line is achieved by employing external circuity (e.g. MOV_{in} and MOV_{out} in Fig. 1). On the other hand, the T-type hDC-CB employs a MCB and is connected between the poles of a DC-line, incorporating an inherent over-voltage protection. In T-type CBs, a current having an opposite direction to the fault current is injected to the MCB in order to commutate the fault current from the MCB to antiparallel diodes. An example of a T-type hDC-CB is presented in [8]. Semiconductors (i.e. high-voltage, high-current thyristors and diodes) are also required in this concept. Last but not least, a hDC-CB concept which combines the characteristics of two-terminal and T-type hDC-CBs is shown in [9]. In this hDC-CB, the fault current is bypassed in a similar way as in the two-terminal concept, while over-voltage protection is ensured using a circuit connected between the two poles of the DC-line. For the presented analysis, this last hDC-CB is listed as a two-terminal concept due to the way that the fault current is commutated from the UFD to the power electronics circuit.

Individual design challenges and operating limitations, which must be carefully addressed, can be itemized for each hDC-CB concept mentioned above. Moreover, selection criteria for choosing the most appropriate hDC-CB for different types of DC-grid configurations (i.e. monopole or bipolar grid) must also be set. This paper presents a comparison study of the four most promising hDC-CB concepts in terms of performance (e.g. response time, over-voltage protection of the DC-line etc.), system design complexity, control complexity and different line configuration. Section 2 presents the characteristics and operating principles of the four hDC-CB concepts under a fault condition. The design inputs for the comparison, as well as, a short-overview of the expected fault types in a DC-line are given in Section 3. The detailed comparison of the concepts with respect to the various characteristics is shown in Section 4.

2 DC Circuit Breaker Concepts under Investigation

This section presents the design parameters and the operating principle of the two-terminal and T-type hDC-CBs when a fault appears in the DC-line. Additionally, conceptual differences among the hDC-CBs are also described.

2.1 Two-terminal DC circuit breakers

In two-terminal hDC-CB a UFD and a power electronics circuit using power semiconductors are usually connected in parallel. By properly designing the power electronics circuit, the two-terminal hDC-CB concepts are able to clear fault currents in both directions. The operating principle of these CBs is based on a fault current commutation from the UFD to the power electronics circuit and, thus, the UFD opens at zero current and withstands both the TIV and the blocking voltage at steady-state.

In literature, there are two promising two-terminal hDC-CB concepts. The hDC-CB which employs a pure semiconductor-based power electronics circuit (2TSEM) [6] (Figs. 2 (A)-(D)) and the hDC-CB having delay branches for the fault current (2TDB) [7] (Fig. 3). The delay branches consist of power semiconductors in series with capacitive energy-storage elements. Figs. 2 (A)-(D) and Fig. 3 summarize the operating states under a fault current clearing procedure. As can be seen from these figures, the operating principles of the two hDC-CB concepts are identical. At a first step, the fault current commutates to the power electronics branches and the UFD opens under zero current condition. The residual energy of the DC-line is then dissipated in metal-oxide-varistors (MOV). The detailed circuitry of a single cell

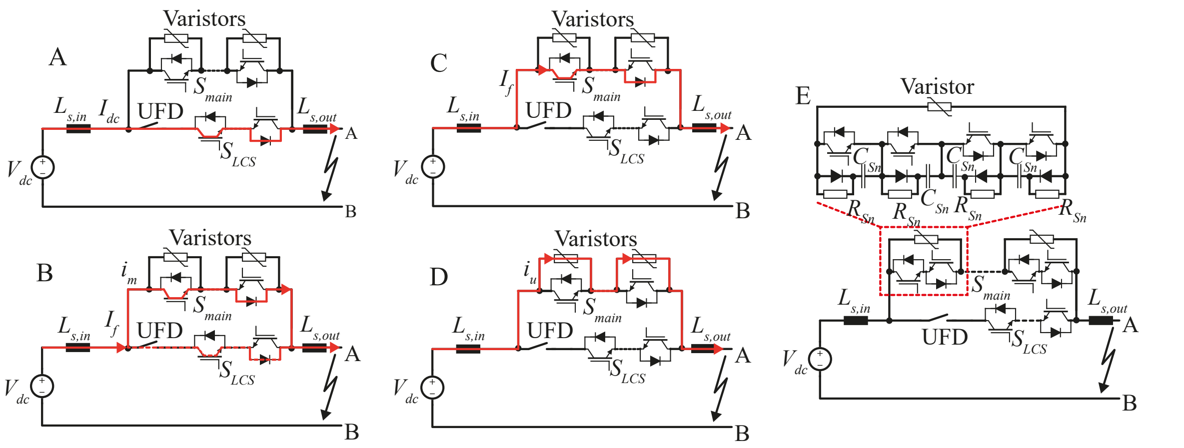

Figure 2: Operating states of the two-terminal hDC-CB employing a pure semiconductor-based power electronics circuit [6] (For simplicity, the line inductances are not shown). (A): Normal operation of the hDC-CB, (B): Fault current commutation to the main breaking path, (C): Fault current interruption by turning-off the semiconductor switches, (D): Energy dissipation in the varistors. (E): Detailed circuit diagram of the hDC-CB showing the snubber circuitry.

employed in the commutation switch of 2TSEM hDC-CB including the snubber circuits is depicted in Fig. 2 (E).

Along with these two hDC-CB two-terminal concepts, a third very promising two-terminal hDC-CB concept having a line-to-ground over-voltage protection is presented in [9]. Fig. 4 shows the operating states of this hDC-CB (2TBYP). A power electronics circuit enables commutation of the fault current in a similar way as in the case of the aforementioned two-terminal hDC-CBs. However, as shown in Fig. 4 the circuit of the 2TBYP also enables over-voltage protection of the DC-line. In case of the 2TBYP hDC-CB, the dissipation of the residual energy is done separately for the energy stored in the input and output line inductances, ($L_{s,in}$ and $L_{s,out}$). In particular, assuming a load current direction as shown in Fig. 4(A), the energy of $L_{s,in}$ is dissipated in MOV_4, while the energy stored in $L_{s,out}$ and in the line inductance is dissipated in MOV_3.

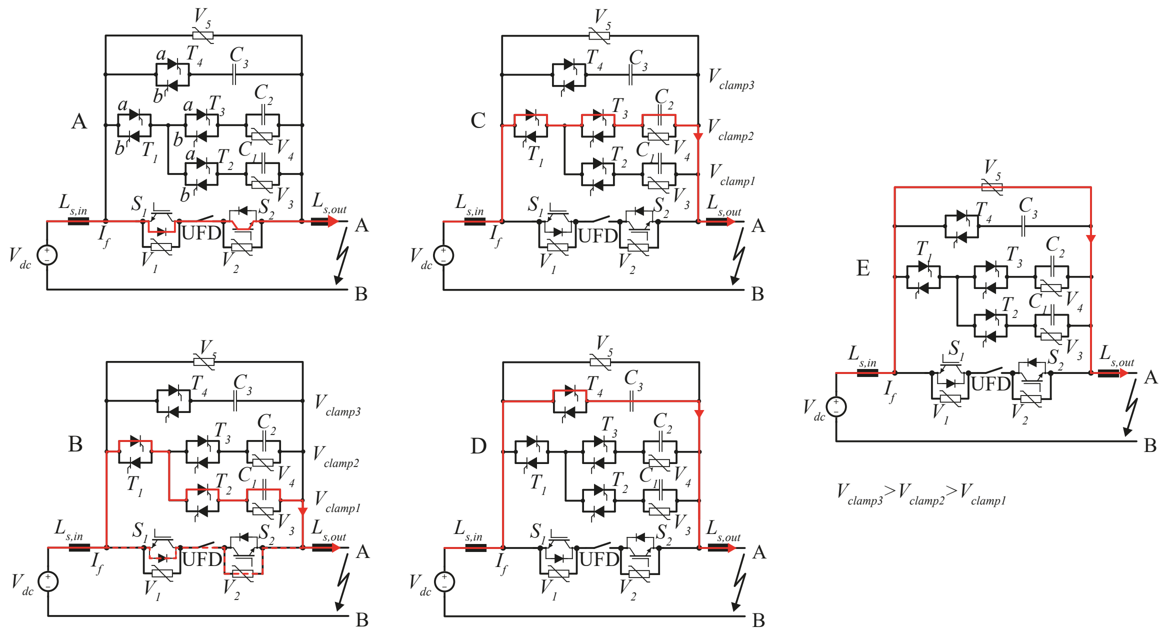

Figure 3: Operating states of the two-terminal hDC-CB containing delay branches [7] (For simplicity, the line inductances are not shown). (A): Normal operation of the hDC-CB, (B): Fault current commutation to the first delay branch, (C): Fault current commutation to the second delay branch, (D): Fault current commutation to the full-blocking-voltage delay branch, (E): Energy dissipation.

2.2 T-type DC circuit breaker

A T-type hDC-CB is connected between the two poles of a DC-line, so that apart from fault current clearing, an inherent protection against line-to-ground over-voltages is given. The operating states of the T-type hDC-CB concept (TPG) are shown in Fig. 5. This figure shows that the T-type hDC-CB employs a power-electronics-based pulse generator (PG) and two reverse-current branches. In case of a fault, the PG is triggered and a reverse current flows through either MCB_{in} or MCB_{out}, depending on the direction of the load current. If the reverse current exceeds the value of the fault current, the current commutates from the MCB to one of the bypass diodes, D_{in} or D_{out}. Thus, the current in one of the MCB drops to zero and the arc in the MCB is extinguished. Energy dissipation and over-voltage protection of the DC-line and equipment are realized by means of the varistor, VDR_{PG}.

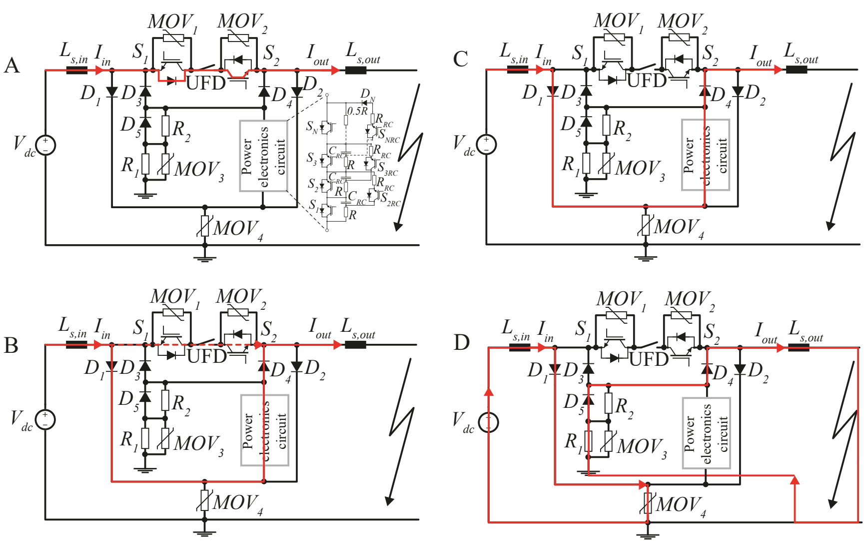

Figure 4: Operating states of the hDC-CB employing a power-electronics-based circuit for bypassing the fault-current and an over-voltage protection circuit [9] (For simplicity, the line inductances are not shown). (A): Normal operation of the hDC-CB, (B): Fault current commutation from the MCB to the power electronics circuit, (C): Fault current interruption, (D): Separate energy dissipation from the input and output current-limiting and line inductances.

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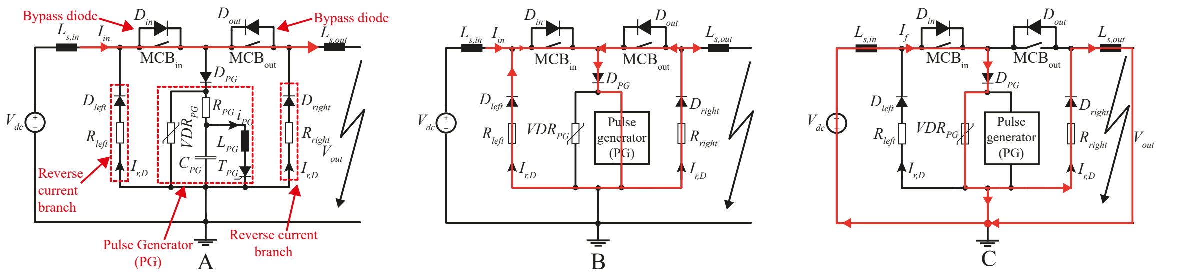

Figure 5: Operating states of the T-type hDC-CB employing a power-electronics-based pulse generator (PG) [8] (For simplicity, the line inductances are not shown).

2.3 Conceptual differences

Even though the target of all four hDC-CB concepts is to turn-off the fault current, conceptual differences for each hDC-CB can be identified. A main difference between the two-terminal and T-type hDC-CBs is associated with the specific type of the MS that is employed. In particular, the two-terminal hDC-CBs use UFDs, which only open when the current is zero [10]. On the other hand, the T-type hDC-CB employs MCBs, which are also able to interrupt the fault current after a zero crossing of the MCB current [11].

A crucial constraint of the hDC-CBs is associated with the rate of rise of the blocking voltage across the UFD of the two-terminal concepts, dV_{UFD}/dt. In particular, dV_{UFD}/dt must not exceed 120 kV/ms if a linear opening of the contacts and a linear increase of the blocking voltage are assumed (Table II) [12]. The design of the power electronics circuits in the hDC-CBs mainly governs the dV_{UFD}/dt. In the case of 2TSEM, for instance, the turn-off sequence of the semiconductor switches in the main breaker path and the design of the snubber circuits (Fig. 2 (E)) determine dV_{UFD}/dt. A proper design of the delay branches (i.e. capacitive energy storage elements) in 2TDB hDC-CB concept will also result in a dV_{UFD}/dt not exceeding 120 kV/ms. Similar considerations can also be done for the 2TBYP breaker concept.

On the contrary, in the T-type TPG the dV_{MCB}/dt depends on the capacitor value C_{PG}, along with the power circuit design. Since the contacts of the MCB are already fully open when the arc is extinguished, a significantly higher rate of change of the blocking voltage can be withstood. More specifically, dV_{MCB}/dt can be as high as 1 kV/μs provided that the contacts of the MCB in TPG are fully open before the arc is extinguished. This will also be analyzed in Section 4.2.

In order to ensure a fair comparison among the examined hDC-CB concepts, specific parameters have been chosen so that dV_{UFD}/dt and dV_{MCB}/dt do not exceed the maximum allowed values. These crucial design parameters are summarized in Table I.

Table I: Specific design parameters for each hDC-CB concept.

hDC-CB	Parameters
2TSEM	43 cells with C_{Sn}=46 μF, R_{Sn}=130 Ω (per cell)
2TDB	C_1=1 mF, C_2=200 μF, C_3=130 μF
2TBYP	43 cells with C_{RC}=6 mF, R_{RC}=0.05 Ω, R=500 Ω (per cell)
TPG	C_{PG}=28 μF, L_{PG}=25 μH, R_{PG}=0.5 Ω, $R_{right,left}$=0.5 Ω

The re-closing process of the MS and the mechanism of this operation is also of high importance. It is only the 2TSEM hDC-CB concept which offers controllability of the voltage across the MS during the re-closing process. In fact, this is achieved by properly turning-on the switches in the main breaker in order to obtain a desired performance of MS.

A crucial constraint for the hDC-CBs is also related to the peak current that is allowed through the MCB before the slope of the current is getting either zero or negative. Assuming that the peak current through the MS is the same for all four CBs, a special attention must be paid in choosing the appropriate values for the current-limiting inductors, L_s. In the TPG hDC-CB, even if the opening signal to the MCB is sent, the slope of the MCB current is still positive for at least the time required to fully open the contacts of the MCB and trigger the PG. On the other hand, in the case of two-terminal hDC-CB concepts, the fault current commutates from the UFD to the power electronics circuit as soon as the detection process is completed. Therefore, the current-limiting inductors, L_s, employed in the TPG and two-terminal hDC-CB concepts will differ. This constraints will be analyzed in the next section.

Table II: Design parameters of the monopolar DC grid and hDC-CBs.

Nominal direct voltage V_{dc}	80 kV
Rated power P	50 MW
Nominal current I_N	625 A
Length of line	100 km
Maximum overvoltage	1.5 pu (120 kV)
Peak current in the UFD and MCB	10 kA
Maximum dV_{UFD}/dt for the UFDs	120 kV/ms
Maximum dV_{MCB}/dt for the MCB	1 kV/μs
L_s for 2TSEM, 2TDB and 2TBYP	17.1 mH
L_s for TPG	37.1 mH
$L_{line,1}$, $L_{line,4}$	0 mH
$L_{line,2}$+$L_{line,3}$	42 mH

3 Design Inputs for the Comparison

3.1 Design parameters for the grid

For a fair comparison of the four hDC-CBs, the parameters listed in Table II are chosen. Moreover, an XLPE high-voltage (HV) cable with a nominal operating voltage equal to 110 kV and the parameters shown in Table III has been taken into account for this investigation.

3.2 Type of faults

Table III: Parameters of the XLPE HV cable.

Line inductance L_{line}	0.42 mH/km
Line resistance R_{line} at 20^oC	0.06 Ω/km
Line capacitance C_{line}	0.17 μF/km

For the performance evaluation, a single DC-line being part of a multi-terminal HVDC grid is assumed as test case. Fig. 6 shows a simplified circuit diagram of the considered DC-line. In particular, the direct voltages on each node, N_1 and N_2 are represented as voltage sources, V_{dc1} and V_{dc2}. The line inductances of the cable are denoted as $L_{line,1}$, $L_{line,2}$+$L_{line,3}$, and $L_{line,4}$. Assuming that the distance between each CB and the corresponding node is very short, $L_{line,1}$ and $L_{line,4}$ are considered to be negligible. On the other hand, the value of $L_{line,2}$+$L_{line,3}$ is given in Table II. For the simulations, however, the inductance of the return path must also be considered. It should be noted that current-limiting inductors, L_s, might be required for specific hDC-CB designs in order to limit the rate of rise of the fault currents. In the presented test case, the required L_s is equally divided in $L_{s,in}$ and $L_{s,out}$ connected on the left and right hand-sides of the CBs.

In Fig. 6 L_s are placed between the hDC-CB (CB_1 or CB_2) and the node of the multi-terminal HVDC grid (N_1 or N_2, respectively). However, a placement of L_s on the right-hand side of CB_1 or left-hand side of CB_2 or equally-divided L_s connected on both sides of the CB, might also result in a proper fault clearing in the case of specific hDC-CB concepts. More specifically, in case of 2TSEM and 2TDB concepts the fault current is properly interrupted even if L_s is connected on one side of the CB_1 or CB_2. Nevertheless, for ensuring an overvoltage limitation in the DC-line, L_s is equally divided in $L_{s,in}$ and $L_{s,out}$ (Fig. 6). In the TPG hDC-CB, on the other hand, for a proper fault clearing L_s must be equally divided and connected to both sides of the CB. In particular, the connection of L_s on both sides of the CB will force the reverse current to flow through the parallel combination of the MCBs and D_{in} or D_{out}. Similarly to TPG, in case of 2TBYP, L_s must also be equally divided in $L_{s,in}$ and $L_{s,out}$ connected on the left and right hand-sides of the CB.

The hDC-CBs under investigation are evaluated assuming three potential types of faults, f_1, f_2 and f_3 as depicted in Fig. 6. The first fault appears between node N_1 and CB_1, f_2 happens at the CB side where the DC cable is connected and f_3 is a pole to ground fault at an arbitrary position in the line. It is noted that the worst-case fault is f_2 (or f_1).

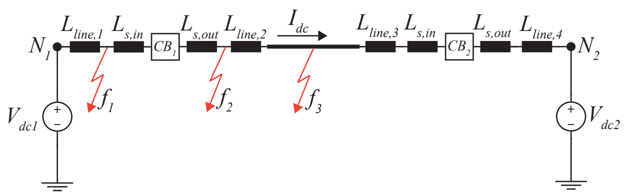

Figure 6: Simplified circuit diagram of the monopolar DC-line under investigation.

Before presenting the results of the evaluation, it is worth to mention the operating procedure from the time a fault occurs until an opening signal is sent to the MS. A fault condition in the DC-line is detected when the line current exceeds twice the nominal current. In addition, for all four examined hDC-CBs, a detection time of t_{det}=2 ms, was also taken into account. During t_{det} no action is taken by the hDC-CB. An opening signal to the MS is sent at the end of t_{det}. On top of this, an additional delay associated with ensuring that an opening signal has received by all MCBs in the case of series-connected MCBs must also be considered. In case of the TPG hDC-CB, even though the contacts of the MCB have opened, the plasma is not extinguished at least for a time equal to one quarter of the resonance time period of the PG. This additional time must also be taken into account when, for instance, the current-limiting inductors are designed. Thus, considering the total time until the time derivative of the fault current is either zero or becomes negative, and that the peak current allowed through the MS must not exceed 10 kA, the values for the current-limiting inductors were calculated for all four hDC-CBs. As given in Table II, for the hDC-CB concepts where the fault current commutates from the UFD to the clearing branch, the value of L_s is equal. On the contrary, in case of TPG hDC-CB, the required value of L_s, which keeps the fault current below 10 kA, is significantly higher. The main reason is the additional delay time ($t_{delayMCB}$=2.3 ms) [11] for the MCB, in order to ensure that the contacts of the MCB are fully open.

4 Performance evaluation of the hDC-CBs

The performance of the examined hDC-CB concepts has been evaluated in terms of applicability, response time, energy dissipation in the various components (e.g. MOVs etc.) and dissipated energy from the direct high-voltage sources considering the three fault cases shown in Fig. 6. Moreover, the CB concepts were also evaluated with respect to the semiconductors and passive components requirements. Last but not least, crucial design guidelines for all hDC-CBs, which must be followed for a reliable operation, are also presented.

The normalized current-voltage characteristic of the MOV considered for the presented evaluation is shown in Fig. 7. The performance of this specific MOV can be properly adjusted by choosing the base voltage which corresponds to 1 p.u. In reality, this can be done by stacking the appropriate number of series-connected MOV disks.

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4.1 Applicability

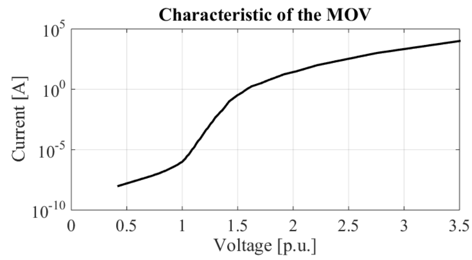

Figure 7: Current-voltage characteristic of the MOV considered for the presented investigation [13].

The term “applicability” is associated with the connection of the hDC-CB in various DC-line configurations (i.e. monopolar or bipolar grid) and the inherent characteristics that are incorporated. In particular, the T-type TPG and the two-terminal 2TBYP hDC-CB concepts, offer an over-voltage protection of the DC-line without the need for additional components. However, this is not the case if the 2TSEM and 2TDB hDC-CBs are employed in a DC-line. It is clear that, in such a case, additional circuitry for over-voltage protection (e.g. pole-ground MOVs) is required as shown in the block diagram in Fig. 1. For bipolar DC-lines with either a metallic return conductor or not, the circuit of the TPG and 2TBYP hDC-CBs also requires modifications for a proper clearing of the faults.

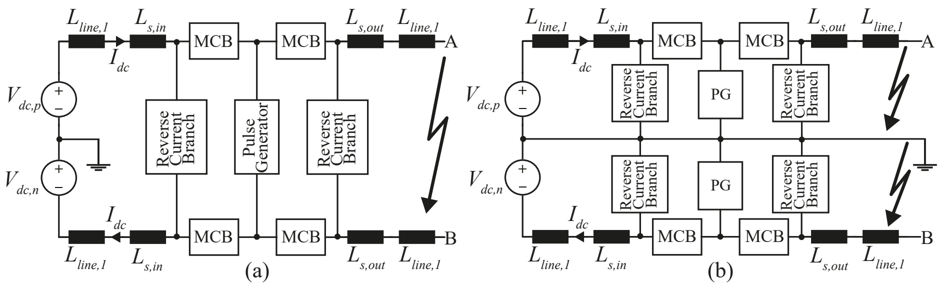

Figure 8: Block diagrams showing the connection of the TPG hDC-CB concept in two configurations of a bipolar HVBC grid: (a) Bipolar HVDC grid without metallic return path and (b) Bipolar HVDC grid with metallic return path.

Taking into account the TPG concept, the connection of this hDC-CB in a bipolar HVDC grid is shown in Fig. 8. In case of a bipolar HVDC grid without a metallic return path, a common PG and common reverse-current branches are sufficient for a proper operation of the hDC-CB. On the other hand, when a metallic return path is present, Fig. 8 (b) shows the connection of the PG and reverse-current branches. In this case, separate systems, connected with respect to the metallic return path, are required for the positive and negative poles of the grid. Thus, independent fault management and over-voltage protection for each pole is feasible if a pole-ground fault appears. In case of pole-pole fault, both PGs must be triggered in order to clear the fault. Similar considerations can also be done for the 2TBYP hDC-CB concept, which also offers an inherent over-voltage protection of the DC-line.

4.2 Response time

In the case of the two-terminal hDC-CBs, the response time, t_{resp}, of the hDC-CBs is the sum of the time required to detect a fault condition, t_{det}, and the clearing time of the fault current, t_{clear} which is required for the UFD to be able to block the maximum voltage. Fig. 9 (a) shows the time sequence for the aforementioned actions taken by the 2TSEM, 2TDB and 2TBYP hDC-CBs. On the other hand, an additional delay time, $t_{delayMCB}$, must be added for the TPG hDC-CB (Fig. 9 (b)). This is the time required for the contacts of the MCB to completely open, to be able to extinguish the arc and to withstand the maximum voltage. This means that the PG must be triggered at the end of $t_{delayMCB}$. However, the reverse current from the PG does not flow until a time interval equal to a quarter of the resonance time of the PG, $t_{PG}/4$, has passed. Therefore, the PG might also be triggered slightly before $t_{delayMCB}$ is over. Last but not least, a significant amount of time is also required in order to dissipate the fault energy of the DC-line. This is denoted as t_{energy} in Figs. 9 (a) and (b).

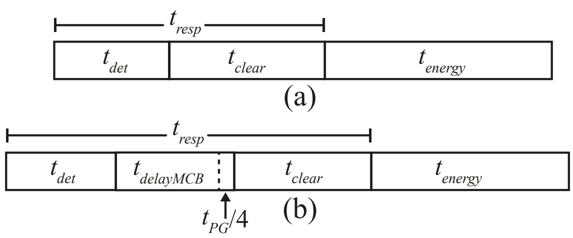

Figure 9: Time sequence of the required actions performed by the (a) 2TSEM, 2TDB and 2TBYP hDC-CBs, and (b) TPG hDC-CB. Note that the time intervals of the itemized actions are not in scale, but they only show a qualitative representation of the operating sequence of the hDC-CBs.

For the presented investigation t_{det} has been set to 2 ms for all four examined CB concepts. This is the time period between the point of time when an over-current is detected and the point of time when the first action is taken on the hDC-CB side. A constraint for the maximum blocking voltage capability of the UFD has also been set. In this study, a linear increase of the blocking voltage, $V_{UFD,max}$, capability of the UFD is considered, where during the opening process of the UFD, $V_{UFD,max}$ increases from 0 to 240 kV within 2 ms (dV_{UFD}/dt <120 kV/ms, Table II). Thus, the voltage increase across the MCB of the examined hDC-CB concepts must not exceed the $V_{UFD,max}$ envelop. Similar considerations are taken into account for the MCB employed in TPG hDC-CB (dV_{MCB}/dt <1 kV/μs, Table II).

In case of the two-terminal hDC-CBs (i.e. 2TSEM, 2TDB and 2TBYP) the fault current is commutated from the UFD by turning-off the series-connected semiconductor switches. On the other hand, a commutation of the fault current from the MCB to the bypass diodes, by injecting a reverse current generated in the PG, happens in the TPG. Thus, using the current through the MS as a measure to compare the response times of the hDC-CBs is not fair. On the contrary, the time required until the MS establishes a blocking voltage equal to DC-line voltage is used to evaluate the response of the four CB concepts. Considering that the parameters of the DC-line and the fault type are the same for all four CBs, Fig. 10

shows the performance of the blocking voltage across the MSs employed in the hDC-CBs when the fault f_2 appears, which is basically the worst-case fault for CB_1 (Fig. 6). It is clear that the energy of the DC-line is dissipated during the time period when the MS is subjected to an over-voltage. Therefore, a second measure to evaluate the response of the hDC-CBs is the energy dissipation from the DC-line during the fault-clearing process. A steep voltage drop is observed in V_{MS} of TPG, 2TDB and 2TSEM concepts. In case of 2TDB and 2TBYP this happens at the point of time where the fault current is fully interrupted, while in the case of TPG it is the point of time where C_{PG} is fully recharged after a fault-clearance process.

The rate of rise and the overshoot of V_{MS} (Fig. 10) must also be examined carefully. In particular, the rate of rise is governed by the choice of the parameters summarized in Table I, while the peak value of V_{MS} depends on the choice of the MOV characteristic. As shown in Fig. 10, the rate of rise of V_{MS} and the peak value comply with the requirements of $V_{UFD,max}$ and $V_{MCB,max}$, whereas a safety margin between the peak values of V_{UFD} and $V_{UFD,max}$ also exists. It must be noted that a larger peak value of V_{UFD} would result in lower dissipated energy from the VSC, E_{VSC}, (faster response of the hDC-CB) at a cost of power semiconductors having higher blocking voltages. Consequently, the choice of the peak value of V_{UFD} and V_{MCB} is a trade-off between the maximum allowed E_{VSC} and the number of series-connected semiconductors. Therefore, using these configurations of the hDC-CBs, potential re-ignition of the arc in the MCB is avoided.

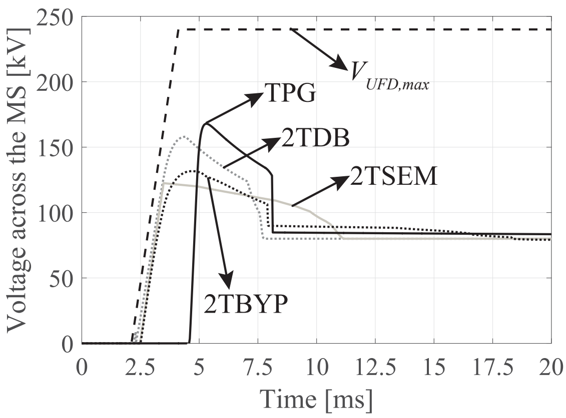

Figure 10: Results of the voltage across the MSs for the four hDC-CB concepts for the fault case f_2.

4.3 Energy dissipation

Along with the response time of the MS, the maximum expected value of the dissipated energy from the DC-line during the fault-clearing process is also of interest in order to properly design the components of the hDC-CB. Table IV summarizes these energies for the four hDC-CB concepts under investigation when f_2 fault appears. As expected, the maximum expected energy from the DC-line is dissipated under the worst-case fault f_2 due to the highest expected fault current when a fault appears exactly at the terminals of the DC-CB (minimum inductance of the DC-line). On the other hand, the corresponding minimum energy is dissipated under the best-case fault f_3 due to the lower peak fault current compared to f_2 fault. It must be highlighted that the total amount of this energy must be properly dissipated in the various components employed in the hDC-CBs (i.e. MOVs and other resistive components).

As shown in Fig. 10, the 2TBYP hDC-CB requires the longest time to reach the steady-state direct voltage of the DC-line. This is also reflected in Table IV, where the highest energy among all four hDC-CBs is dissipated in the case of the 2TBYP hDC-CB. A slightly lower energy dissipation is expected from the DC-line when the 2TSEM hDC-CB is employed, while the lowest energy in the case of fault f_2 is dissipated using the TPG breaker. From Table IV, it is observed that the energy dissipation from the VSC under f_2 using the 2TBYP is the highest among all examined hDC-CBs. This is due to the lower overvoltage across the UFD observed in Fig. 10, which also results in a longer required time of the CB to establish the steady-state voltage of 80 kV.

4.4 Components requirements

A fair comparison among the investigated hDC-CB concepts also requires an evaluation in terms of the required number of semiconductor devices and the requirements of energy-storage and energy-dissipation components (i.e. capacitors, inductors and MOVs). For the presentation of the components requirements, the worst case conditions are assumed. In terms of fault type, the worst case is fault f_2. However, for specific components, the worst case corresponds to fault f_3 (e.g. higher required blocking voltage of semiconductors etc.).

4.4.1 Inductors

The two-terminal hDC-CBs only require current-limiting inductors ($L_{s,in}$ and $L_{s,out}$) in the input and output terminals. The role of these inductors is to control the rate of rise of the fault current in order to let the hDC-CB operate properly. On the contrary, the TPG concept, in addition requires the inductor L_{PG} in the pulse generator. As mentioned above, the criterion of choosing an appropriate value for the current-limiting inductors depends on the peak value of the fault current and the required time until the first action in the hDC-CB is performed. Thus, the values of $L_{s,in}$ and $L_{s,out}$ employed in the two-terminal concepts are lower than the corresponding current-limiting inductors of the TPG hDC-CB. Consequently, the reflected energy dissipation in $L_{s,in}$ and $L_{s,out}$ employed in the TPG will also be higher compared to the two-terminal hDC-CBs (Table IV). An additional design criterion of the current-limiting inductors is the peak current, $\hat{I}_{Ls}$, which flows through the current-limiting inductors. The corresponding values of $\hat{I}_{Ls}$ are also summarized in Table IV. As can be seen, the maximum value for $\hat{I}_{Ls}$ is observed for the 2TBYP concept.

In Table IV, the maximum energy dissipation in L_{PG}, $E_{L_{PG}}$, along with the peak value of the current in the PG, $\hat{I}_{L_{PG}}$, are also shown. Even though $E_{L_{PG}}$ is significantly lower than the sum of $E_{Ls,in}$ and $E_{Ls,out}$,

Table IV: Worst-case energy dissipation/storage and power semiconductor devices requirements for the hDC-CBs.

hDC-CB	2TSEM	2TDB	2TBYP	TPG
Energy dissipation/storage requirements				
Dissipated energy from VSC E_{VSC} [MJ]	**5.64**	**4.74**	**5.87**	**3.66**
Peak current drawn from the VSC $\hat{I}_{VSC}$ [kA]	**13.76**	**14.42**	**17.46**	**11.26**
Time required to interrupt the VSC current t_{off} [ms]	**11.37**	**7.97**	**8.34**	**8.16**
Thermal stress of VSC $\int I_{VSC}dt$ [As]	**70.55**	**58.67**	**71.8**	**45.68**
Inductive energy-storage requirements for L_s, E_{L_s} [MJ]	**1.62**	**1.79**	**2.61**	**2.34**
Inductive energy-storage requirements for L_{PG}, $E_{L_{PG}}$ [MJ]	–	–	–	**0.09** $\hat{I}_{L_{PG}}$=84 kA; 0.17 ms
Capacitive energy-storage requirements E_C [MJ]	$\sum_{n=1}^{43} E_{Cs,n} =$ $43 \cdot 188 \cdot 10^{-6} =$ $=$ **0.00806**	E_{C_1}=0.00355 E_{C_2}=0.0041 E_{C_3}=1.62 $E_{C_{total}}$=**1.63**	$\sum_{n=1}^{43} E_{C_{RC,n}} =$ $43 \cdot 0.0192 =$ $=$ **0.826**	**0.28**
Energy-dissipation requirements of the MOVs E_{MOV} [MJ]	$\sum_{n=1}^{43} E_{mov,n}$ =**5.64**	E_{V_1}=0.00186 E_{V_2}=0.00186 E_{V_3}=0.00353 E_{V_4}=0.0253 E_{V_5}=3.06 $E_{V_{total}}$=**3.13**	E_{MOV1}=0.002 E_{MOV2}=0.002 E_{MOV3}=0.66 E_{MOV4}=3.28 $E_{V_{total}}$=**3.94**	**2.57**
Conduction power losses P_{cond} [kW]	**4.98 (0.006%)**	**4.98 (0.006%)**	**4.98 (0.006%)**	**0**

Component type	Specific component	di_{cr}/dt [kA/μs]	2TSEM	2TDB	2TBYP	TPG
Power semiconductors requirements						
Thyristors	TR_1[a]	5	–	109	–	30
	TR_2[b]	1	–	109	–	58
	TR_3[c]	22	–	388	–	162
IGBTs with diodes	S_1[d]	–	262	4	634	–
Diodes	D_1[e]	–	86	–	598	145
	D_2[f]	–	86	–	1376	244

[a]Infineon T2563NH, [b]ABB 5STP 37Y8500, [c]Dynex PT85QWx45, [d]ABB 5SNA 3000K452300, [e]ABB 5SDD 50N5500, [f]ABB 5SDF 28L4521,

$\hat{I}_{L_{PG}}$ is higher compared to the $\hat{I}_{L_s}$. Therefore, this constraint must also be taken into account not only during the design process of L_{PG}, but also for the proper selection of the thyristors in the PG.

4.4.2 Capacitors

The worst-case energy-storage requirements of the capacitors employed in the four hDC-CB concepts are listed in Table IV. The maximum energy-storage requirements among all four hDC-CBs are observed for the 2TDB concept. The reason to this is that the capacitor C_3 and C_{PG} in the 2TDB is directly subjected to the full blocking voltage of the UFD. On the other hand, 2TSEM and 2TBYP consist of several individual cells which are able to block significantly lower voltages compared to the other two hDC-CBs. In particular, these voltages equal the full blocking voltage of the UFD divided by the number of cells. For the evaluation study presented here, the number of cells has been set to 43. For a clear presentation of the capacitive energy storage requirements, the individual stored energies in the various capacitors are also summarized in Table IV. However, it must be noted that even though the capacitive energy storage requirements for the TPG breaker is lower than for 2TDB and 2TBYP, C_{PG} must withstand the peak circulating current created as soon as the PG is triggered.

4.4.3 MOVs

The maximum energy dissipation is given in Table IV. The highest value is observed for the 2TSEM hDC-CB, which is actually the sum of the energy dissipation in the individual cells. In particular, this amount of energy is approximately equal to the energy delivered from the VSC during the fault clearing procedure. The reason is the absence of energy-storage components in the 2TSEM breaker concept, as for instance in the 2TBYP hDC-CB. In this breaker, a significant amount of energy is dissipated in the various resistors (Table I) employed in the cells of the hDC-CB. On the contrary, in case of the 2TDB hDC-CB concept, apart from energy dissipation in the MOVs, a part of the delivered energy from the VSC is stored in the capacitors of the delay branches. Last but not least, the minimum E_{MOV} is observed for the TPG hDC-CB. In this case, the delivered energy form the VSC is mainly dissipated in the MOV, while a lower contribution of this energy is recharging C_{PG}.

It must be noted that it is only the TPG hDC-CB where a single MOV is sufficient for a proper operation of the breaker. However, in the two-terminal hDC-CBs, multiple MOVs are required. The 2TSEM concept, for instance, requires one MOV connected across each of the individual cells of the main breaking-path. Similarly to this, a single MOV which is properly dimensioned is also connected in each of the delay branches of the fault current in the 2TDB breaker. Therefore, Table IV shows not only the sum of the individual dissipated-energy amounts in the MOVs, but also the itemized energy dissipation in each separate MOV. Taking into account a specific I-V characteristic of a MOV (e.g. Fig. 7) and the associated maximum energy dissipation, the number of series and parallel MOV disks can be easily specified for each hDC-CB case.

4.4.4 Semiconductors

The most commonly-used semiconductors in the hDC-CBs are HV thyristors, insulated-gate bipolar transistors (IGBTs) and diodes. A crucial design constraint regarding the power semiconductors deals with the number of series and parallel-connected devices in order to fulfill the blocking voltage and current requirements. Based on simulations of the examined hDC-CB concepts, the worst-case blocking voltage and current conditions for each power semiconductor device have been identified. The results are summarized in Table IV. All power semiconductors have been chosen such, that they meet both the highest possible voltage and current ratings among all commercially-available devices. In the case of HV thyristors, however, the critical rate of rise of on-state current, di_{cr}/dt, has also been considered during the selection process. In particular, di_{cr}/dt must be sufficiently high than the rate of rise of the actual load current flowing through them.

For the investigations, three different HV thyristors, having different voltage and current ratings and various di_{cr}/dt values, have been considered. In case of the TPG hDC-CB the thyristors must withstand the excessively high circulating current in the PG tank. Depending on the specific design of the PG, this current might exceed a few tens of kA.

As shown in Table IV, the minimum number of required HV thyristors for both 2TDB and TPG is obtained if either Infineon T2563NH or ABB 5STP 37Y8500 devices are employed. However, the first HV thyristor has a significantly higher di_{cr}/dt than the second device, which is found to be desired, especially, for the TPG hDC-CB. This is particularly due to the fast-rising reverse current which is generated by the PG. Apart from the total number of required HV thyristors, the itemized requirements of series and parallel-connected devices is also of high importance as presented in Table V.

The total numbers of HV IGBT switches required for the 2TSEM, 2TDB and 2TBYP hDC-CBs are summarized in the third row of Table IV. The specific HV IGBT ABB 5SNA 3000K452300 has been chosen considering the maximum possible voltage and current ratings among all commercially-available HV IGBTs. It must also be noted that the package of this HV IGBT switch contains HV antiparallel diodes having the same voltage and current ratings. Thus, the numbers of required HV IGBTs are also refereed to the corresponding antiparallel diodes. However, in the case of 2TSEM and 2TBYP discrete HV diodes are also needed (e.g. snubber diodes in 2TSEM, diodes $D_1 ... D_4$ in 2TBYP etc.). The estimation of the total numbers of these diodes has been done separately and it is shown in the last row of Table IV. It must be noted that the number of discrete HV diodes in the case of 2TSEM hDC-CB depend on the number of individual cells of the breaker, which is defined by $V_{UFD,max}$ and dV_{UFD}/dt. This is the reason that, regardless of the specific HV diode type shown in the last row in Table IV, the required number of the devices is the same. However, the voltage and current ratings of these diodes must be sufficient for a proper operation of the hDC-CB.

In terms of power semiconductors requirements, a direct comparison is only possible between the 2TSEM and 2TBYP hDC-CBs. This is due to the nature of these concepts, where series-connected individual cells are employed. In these two hDC-CB concepts, the smallest discretization of the cells was considered as the design criterion for the required number of cells. Thus, the highest flexibility for shaping the voltage across the UFD, V_{UFD} is also reached. Practically, the smallest discretization corresponds to cells designed such that the voltage across each cell can be blocked by a single HV IGBT. Therefore, 43 individual cells were considered for the design case of the 2TSEM. In order to obtain a fair comparison between the 2TSEM and 2TBYP concepts, the latter one was also designed assuming 43 individual cells. This means that the HV IGBTs denoted as $S_1 ... S_N$ must be able to withstand the same voltage as the capacitors C_{RC}. However, the HV IGBTs $S_{2RC} ... S_{(N-1)RC}$ are connected across two series-connected capacitors C_{RC} (Fig. 4A). Hence, the blocking voltage capability of $S_{2RC} ... S_{(N-1)RC}$ must be twice the voltage of C_{RC} under operation without faults. This is the main reason that the number of required HV IGBTs in the 2TBYP hDC-CB are approximately 50% higher compared to the corresponding number of IGBTs employed in the 2TSEM breaker.

An additional challenge of hDC-CBs is associated with employing the least possible number of power semiconductor components in the main current conduction path so that the conduction power losses in the DC-line are minimized. In the two-terminal hDC-CB concepts where the current commutates from the UFD, series-connected HV IGBTs are required in the main conduction path. Nevertheless, the number of these HV IGBTs must be kept as low as possible in order to reduce the conduction losses. This can be actually seen from the number of required HV IGBTs in the 2TDB hDC-CB. In particular, by properly choosing the breakdown voltage of the varistors V_1 and V_2 (Fig. 3) a single IGBT is sufficient to withstand the blocking voltage. However, parallel-connection of several HV IGBTs might be necessary to properly turn-off the peak fault current. Therefore, in the case of the 2TDB hDC-CB, each of the two commutation switches consists of 2 parallel-connected HV IGBT of the type ABB 5SNA 3000K452300 (4 HV IGBTs in total).

4.5 Specific design guidelines for the hDC-CBs

Specific design challenges can be listed for each specific hDC-CB concept. Such challenges might be associated not only with a proper tuning of the control schemes, but also with a proper design of the various crucial components of the CB. Hence, the CB will operate successfully under a fault condition.

Table V: Worst-case series and parallel-connected HV thyristors using the Infineon T2563NH.

hDC-CB	2TDB				TPG
Component	T_1	T_2	T_3	T_4	T_{PG}
Series	19	10	10	14	30
Parallel	2	2	2	2	1
Total	109				30

A very crucial design constraint of the hDC-CBs is associated not only with the maximum blocking voltage of the MS, $V_{MS,max}$, but also with the rate of rise of V_{UFD} and V_{MCB}. In particular, the actual voltage across the MS during the fault-clearing process must comply with the pre-defined constraints analyzed in Section 4.2. The control of dV_{UFD}/dt and dV_{MCB}/dt is achieved by properly designing specific components of the hDC-CBs and tuning the operation of them according to the desired performance. In the TPG hDC-CB the dV_{MCB}/dt is mainly governed by the design of the PG. The value of the capacitor, C_{PG}, employed in the PG along with the value of the charging resistor, R_{PG}, determine the rate of rise of the voltage across the PG. In case of the 2TSEM hDC-CB an appropriate turn-off timing of the series-connected semiconductors is very crucial to obtain the desired blocking voltage shape. The choice of C_3 in the 2TDB hDC-CB concept governs the main part of dV_{UFD}/dt, while $V_{UFD,max}$ depends on the choice of the breaking voltage of MOV V_5. Last but not least, the rate of rise of V_{UFD} in the 2TBYP hDC-CB depends on the design of the individual $R_{RC} - C_{RC}$ networks and $V_{UFD,max}$ is equal to the difference of the breaking voltages of MOV_4 and MOV_1.

An additional device parameter of the HV thyristors that must be taken into account is the sum of the reverse recovery time, t_{rr}, and the gate recovery time, t_{gr}. This sum is usually referred as the turn-off time, t_q, of the thyristor. Especially, this is of high importance in the 2TDB hDC-CB concept, where the fault current commutates from a thyristor-based delay branch to the next one. This time can be influenced via control of the current slope at turn-off and the voltage slope of the re-applied voltage, but even with employing several parallel and series-connected thyristors, to meet the recovery time might be a demanding task, since HV thyristors with blocking voltages above 2 kV have recovery times exceeding 100 μs.

5 Discussion/Conclusions

This paper presents a performance evaluation of the four most-promising hDC-CBs under the worst-case fault scenario. Along with a brief presentation of the operating principle of each hDC-CB concept, it is shown that two types of hDC-CBs are found with respect to the fault-current commutation method. These are the two-terminal hDC-CBs where the fault current is bypassed from the UFD by an active switch, and the T-type hDC-CB where a reverse current having a higher peak value than the fault current is injected causing free-wheeling commutation of the fault current from a MCB to a bypass diode. Thus, in any case, a zero-current condition is created in the MS.

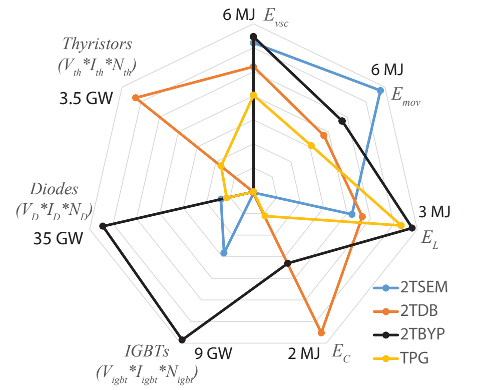

Figure 11: Design requirements of the four examined hDC-CB concepts.

In order to achieve a fair comparison of the hDC-CB concepts, the same DC-line parameters and four design constraints were assumed. These constraints are the maximum breaking current through the MS, and the maximum overvoltage in the DC-line. However, due to the different operating principles of the hDC-CBs as such, the response of each breaker is evaluated in terms of energy dissipation, E_{VSC}, from the VSC under the worst-case fault condition and not based on the response time. It has been shown that the 2TBYP concept dissipates the maximum energy from the VSC under the worst-case fault among all the examined breakers. This is also reflected in Fig. 10, where the time required for V_{UFD} to be stabilized at V_{dc} is the longest. With respect to the inductive energy storage, 2TBYP requires the highest energy-handling capability due to the highest peak current drawn from the VSC among all hDC-CBs. Considering the capacitive energy requirements, 2TDB needs the highest one among all examined concepts. In particular, this energy is twice the corresponding E_C in case of 2TBYP. Last but not least, 2TSEM exhibits the highest energy dissipation in the MOVs. In particular this energy is approximately 80% higher than E_{MOV} of 2TDB, 72% higher than E_{MOV} in TPG and 43% higher than E_{MOV} dissipated in the case of 2TBYP.

The power semiconductors are vital components for a proper fault-clearing process of the hDC-CBs. It was shown that a direct comparison in terms of semiconductors requirements is only possible between the 2TSEM and 2TBYP hDC-CBs. In particular, it was found that in case of 2TBYP a 50% higher number of HV IGBTs is required compared to 2TSEM, while the corresponding number of HV diodes are expected to be approximately 4 times higher than the HV diodes employed in 2TSEM. A qualitative representation of the stored/dissipated energy and the installed power semiconductors requirements of the four hDC-CB concepts is shown in Fig. 11. The power semiconductors requirements are represented as the multiplication of their rated voltage, current and number of installed units of each specific component ($V_{rated} * I_{rated} * n$). For the presented energies, on the other hand, the actual values are shown in Fig. 11. A closer examination of Fig. 11 reveals that the TPG hDC-CB exhibits the best performance among all four concepts.

Last but not least, specific design guidelines for all four hDC-CB concepts are given. For achieving a reliable operation of the hDC-CBs under a fault condition, these guidelines must be carefully considered.

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