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Metal Oxide Semiconductor Thin-Film Transistors for Flexible Electronics

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Zürich, April 2016 Luisa Petti

Contents

Abstract

The rapid progress in semiconductor technology is fueled by the growing demand for electronic devices with improved performance, higher integration density, and new functionality. On one side, aspects like electrical performance, feature size, and manufacturing cost are still pushing the development of silicon-based devices, as predicted by Gordon Moore in 1965. On the other side, the quest for increased functionality of electronic devices is calling for alternative technological platforms, providing novel features like flexibility, light-weight, transparency, conformability, stretchability, biocompatibility, and even biodegradability. A new generation of flexible electronics allowing higher functionality of wearable devices and smart textiles, e.g. for sports or healthcare applications, is rapidly expanding. Even disruptive applications like artificial robotic skins or imperceptible implants seem to be possible by embedding thin, soft and flexible electronic systems everywhere.

Among flexible electronic technologies, metal oxide semiconductor thin-film transistors (TFTs) are particularly appealing, owing to their ability to combine optical transparency, carrier mobility larger than $10\,cm^2\,V^{-1}\,s^{-1}$, low temperature processability, and low sensitivity to mechanical strain. These features, together with the possibility to develop large-area and scalable manufacturing processes, render metal oxide semiconductor TFT technology the most prominent candidate to drive tomorrow's ubiquitous electronics.

In this thesis, metal oxide semiconductor TFTs were fabricated on free-standing 50 μm-thick polyimide foils utilizing a wide range of materials, device structures, and manufacturing processes. Advanced vertical and quasi-vertical geometries were used to realize indium gallium zinc oxide (IGZO) TFTs with 500 nm and 300 nm channel lengths, respectively. Two-photon direct laser writing (DLW) was utilized to fabricate flexible IGZO TFTs with channel lengths down to 280 nm.

For future electronic systems, also memory functionality needs to be integrated on flexible substrates. In particular, memory devices that combine low-power operation and mechanical flexibility are especially attractive. Low-voltage non-volatile memory TFTs with ferroelectric P(VDF-TrFE) gate dielectrics and IGZO active layers were fabricated. The behavior of IGZO memory devices under applied mechanical bending (tensile and compressive strain up to ±0.6 %) was investigated

and correlated to the piezoelectric properties of P(VDF-TrFE).

An approach for the deposition of metal oxide semiconductors is represented by solution processing techniques, which are much less studied until today. These techniques would further increase the possibilities of large-area and low-cost fabrication methods. In this work, indium oxide (In_2O_3) active layers were grown by ultrasonic spray pyrolysis at 250 °C and integrated into flexible n-type TFTs and unipolar logic inverters.

Most common metal oxide semiconductors yield a good electron conduction. To allow the development of a compact and low-power flexible complementary TFT technology, inorganic and organic p-type solution-processable semiconductors were investigated. Especially spin-casted single walled carbon nanotube (SWCNT) devices proved to be a particularly attractive option, owing to their hole effective mobility above 8 $cm^2\ V^{-1}\ s^{-1}$ and their mechanical flexibility down to 4 mm.

To take advantage of both n-type and p-type TFTs, flexible complementary logic inverters were demonstrated. Complementing n-type IGZO with p-type SWCNTs allowed realizing flexible inverters yielding gains up to 85 V/V, even while bent to a tensile radius of 10 mm. The demonstration of flexible complementary inverters based on fully solution-deposited active layers (spray-coated In_2O_3 and spin-coated SWCNTs) is considered a step towards large-area and solution-processed flexible electronics.

Riassunto

Il rapido progresso delle tecnologie a semiconduttore è alimentato da una crescente richiesta di dispositivi elettronici con migliori prestazioni, maggiore densità d'integrazione e nuove funzionalità. Da un lato, talune caratteristiche come le prestazioni elettroniche, le dimensioni del transistore e i costi di produzione continuano a sollecitare lo sviluppo di dispositivi al silicio, come previsto da Gordon Moore nel 1965. Allo stesso tempo, la domanda di una maggiore funzionalità dei dispositivi elettronici induce a utilizzare piattaforme tecnologiche alternative, che forniscano nuove caratteristiche quali la flessibilità, la leggerezza, la conformabilità, l'elasticità, la biocompatibilità e la biodegradabilità. A tale scopo, è in crescita una nuova generazione di circuiti elettronici flessibili che consentano una maggiore funzionalità dei dispositivi portabili e dei tessuti intelligenti, ad esempio per lo sport o per il settore medico. Sistemi elettronici leggeri e sottili sembrano consentire persino innovazioni futuristiche quali pelle artificiale per robot o addirittura protesi impercettibili.

Una tecnologia elettronica flessibile particolarmente interessante è quella dei transistori a film sottile a semiconduttori di ossido di metallo, che consente di combinare transparenza ottica, mobilità elettronica maggiore di $10\,cm^2\,V^{-1}\,s^{-1}$, processabilità a basse temperature e bassa sensitività alle tensioni meccaniche. Queste caratteristiche, unite alla possibilità di sviluppare processi di produzione su larga scala, rendono la tecnologia a semiconduttori di ossido di metallo il candidato più promettente per i dispositivi elettronici del futuro.

In questa tesi, transistori a film sottile a ossidi di metallo sono stati fabbricati su un substrato polimmidico flessibile e autoportante (50 μm di spessore) utilizzando una vasta gamma di materiali, di strutture e di processi di fabbricazione. Geometrie verticali e quasi-verticali sono state usate per realizzare transistori a ossido di indio-gallio-zinco (IGZO) aventi lunghezza di canale, rispettivamente, di 500 nm e 300 nm. Inoltre, la scrittura diretta laser è stata utilizzata per fabbricare transistori a IGZO con lunghezza di canale di 280 nm.

Per i sistemi elettronici del futuro, anche le memorie devono essere integrate su substrati flessibili. In particolare, sono particolarmente importanti le memorie che combinano operazione a basso consumo di potenza e flessibilità meccanica. Utilizzando transistori a IGZO con un dielettrico ferroelettrico [P(VDF-TrFE)], sono state realizzate memorie

non volatili a basso voltaggio. Inoltre, è stata studiata la risposta delle memorie a seguito di sollecitazioni meccaniche di trazione e di compressione (±0.6 %). I risultati ottenuti sono stati messi in correlazione con le proprietà piezoelettriche del P(VDF-TrFE).

Un metodo interessante (anche se ancora poco studiato) per la crescita dei semiconduttori a ossidi di metallo è rappresentato dall'uso di processi da soluzione. Questa tecnica potrebbe favorire ulteriormente lo sviluppo di metodi di fabbricazione su larga scala e a basso costo. In questa tesi, ossido di indio (In_2O_3) è stato cresciuto mediante pirolisi a spruzzo ultrasonico a 250 °C ed integrato in transistori e invertitori unipolari di tipo n.

Comunemente i semiconduttori a ossido di metallo esibiscono una buona conduzione di elettroni. Per poter sviluppare una tecnologia flessibile complementare che sia compatta e a basso consumo di potenza, sono stati investigati anche semiconduttori inorganici e organici di tipo p processabili da soluzione. In particolare, dispositivi a nanotubi di carbonio a parete singola (SWCNT) si sono dimostrati un'opzione interessante per la mobilità di lacuna al di sopra degli $8\,cm^2\,V^{-1}\,s^{-1}$ e per la flessibilità meccanica fino a 4 mm di raggio di curvatura.

Per sfruttare i vantaggi dei transistori di tipo n e p, sono stati fabbricati invertitori complementari flessibili. Grazie a transistori a IGZO (di tipo n) e SWCNT (di tipo p), è stato possibile realizzare invertitori flessibili aventi un guadagno di 85 V/V e flessibilità meccanica fino ad un raggio di curvatura di 10 mm. La realizzazione di invertitori complementari flessibili con semiconduttori processati da soluzione (In_2O_3 e SWCNTs) rappresenta un passo avanti nello sviluppo dell'elettronica flessibile e processabile da soluzione su larga scala.

1

Introduction

1.1 Motivation

Today electronics is facing a disruptive evolution, advancing from being heavy, bulky and rigid and becoming light-weight, soft and flexible. A key driver of this change is the need to unobtrusively embedd electronics into everyday objects and allow higher functionality of wearable devices [1] and smart textiles [2], e.g. for sport or healthcare applications. At the same time, seamless integration of electronics is paving the way to new applications like smart tags [3], intelligent packaging [1], artificial robotic skins [4], imperceptible [5] biomimetic [6] and transient [7] prostheses, as well as advanced surgical tools [8]. To enable these scenarios and revolutionize the future daily life of billions of people in the world, electronic devices that are flexible, light-weight, transparent, conformable, stretchable, biocompatible, and even biodegradable are required. Flexible thin-film transistors (TFTs) are able to fulfill these requirements, and are thus becoming increasingly important. Even if high-performance applications will still rely on devices based on semiconductors like Si, GaAs or SiC, flexible TFTs will push the development of next-generation electronics in novel directions and allow new products.

Among state-of-the-art flexible TFT technologies, metal oxide semiconductors are especially suitable, owing to their high optical transparency (above 80 % [9]), good electrical performance (carrier mobility $\geq 10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [10]), and good insensitivity to mechanical strain. In particular, metal oxide semiconductors, like amorphous silicon (a-Si) and organic materials, are characterized by low-cost and large-area scalability, but at the same time yield carrier mobility values closer to those achievable with more expensive (and less scalable) platforms, such as low-temperature poly-crystalline silicon (LTPS). This is why metal oxide semiconductors are considered the most prominent candidate for next-generation flexible active matrix organic light emitting display (AMOLED) backplanes [11], as well as the most suitable technology to fuel tomorrow's ubiquitous electronics [12].

Nowadays flexible metal oxide semiconductor TFTs have made their entry in the AMOLED market [13], whereas their commercialization in application areas beyond optical displays is still prevented by various technological bottlenecks. In particular, while optical display backplanes can be realized with flexible TFTs operating at frequencies below 100 Hz, other applications like transceivers, radio-frequency identification (RFID) tags, or AM radios require devices with smaller

feature sizes and higher transit frequencies. Nevertheless, the fabrication of flexible TFTs with sub-500 nm channel lengths and Megahertz frequencies is challenged by the limited thermal and mechanical stability of flexible substrates. At the same time, novel large-area and cost-effective applications like foldable and printable displays, disposable smart labels, and intelligent packaging call for low-cost and high-throughput solution processing techniques. However, to date, low-temperature solution deposition methods on flexible substrates need still to be optimized and established in order to allow fully printed or roll-to-roll processes. Another open issue is represented by the scarce availability and performance of flexible p-type metal oxide semiconductor TFTs. Realizing p-type devices is intrinsically hindered by the electronic structure of metal oxide semiconductors, which guarantees a good electron conduction and at the same time a bad hole transporting path. This limits the development of a compact and low-power complementary technology based on n- and p-type metal oxide semiconductors.

In this thesis, novel device structures and fabrication processes allowing sub-500 nm feature sizes on flexible substrates are investigated and applied to realize short-channel flexible metal oxide semiconductor TFTs. Furthermore, low-temperature and scalable solution processes are employed to fabricate flexible n-type metal oxide semiconductor TFTs and circuits. At the same time, promising solution-processable inorganic and organic p-type semiconductors are explored and incorporated in flexible TFTs and circuits. Finally, the application of metal oxide semiconductor TFTs for flexible non-volatile memories and complementary logic circuits is demonstrated.

1.2 State of the Art[1]

This section summarizes the state of the art of flexible metal oxide semiconductor devices. First of all, an overview of the existing flexible TFT technologies is given. In the second part, the focus is on flexible metal oxide semiconductor TFTs. In particular, the materials and the fabrication techniques employed for the manufacturing of flexible metal oxide semiconductor devices are first reviewed, followed by a

[1]This section is based on: L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T.D. Anthopoulos, and G. Tröster, Metal Oxide Semiconductor Thin-Film Transistors for Flexible Electronics. In *Applied Physics Review*, 3 (2), 021303.

description of the electrical performance as well as of the mechanical properties of the resulting n- and p-type TFTs. Finally, in the last part unipolar and complementary circuits based on metal oxide semiconductors are presented.

1.2.1 Flexible TFTs

If compared to standard Si MOSFETs, flexible TFTs yield a significantly lower carrier mobility. On one hand, in MOSFETs the substrate is a single crystal Si wafer (representing also the active layer) and device functionality is added through a large variety of complex, high temperature (>1000 °C) and expensive processes (e.g. diffusion/implantation of dopants, lithography, etching) [14]. On the other hand, TFTs are typically fabricated on insulating substrates, on which the device layers are grown at lower temperature (<650 °C) by vacuum- or solution-processing deposition techniques. This different manufacturing process (especially if on flexible substrates) enables on one side a wide range of novel applications that are not possible with standard rigid and crystalline Si MOSFETs, but on the other side limits the charge carrier transport of the typically poly-crystalline or amorphous semiconductors [9]. Nevertheless, if compared to other established flexible TFT technologies (Table 1.1), metal oxide semiconductors represent an excellent trade-off between good electrical properties, large-area scalability, and low process cost and complexity. As evident from Table 1.1, metal oxide semiconductors present several advantages over a-Si and organic materials, such as low-cost, low process complexity and temperature, large-area scalability, combined with a large carrier mobility [9]. Compared to LTPS, metal oxide semiconductors present slightly lower carrier mobility, but also larger scalability, smaller manufacturing cost, as well as reduced process complexity and temperature [9]. Furthermore, metal oxide semiconductor TFTs show better insensitivity to mechanical strain if compared to LTPS devices [13].

In the following we will review the state of the art of flexible metal oxide semiconductor TFTs and circuits.

1.2.2 Flexible metal oxide semiconductor TFTs

Since 2004 when Nomura et al. reported the first flexible metal oxide semiconductor TFT [10], a large variety of different manufacturing approaches have been demonstrated. Some of these approaches require

	Structure	Mobility ($cm^2\ V^{-1}\ s^{-1}$)	Process cost	Process complexity	Process temperature (°C)	Large-area scalability	Device type
Metal oxide semiconductors	Mainly amorphous	10-100	Low	Low	RT to 350	High	Mainly n-type
Amorphous silicon	Amorphous	1	Low	Low	150-300	High	N-type
Low-temperature poly-crystalline silicon	Poly-crystalline	50-100	High	High	350-500	Low	N- and p-type
Organic semiconductors	Mainly poly-crystalline	0.1-10	Low	Low	RT to 250	High	Mainly p-type

Table 1.1: Comparison between metal oxide semiconductors and other established flexible TFT technologies [15, 9, 16, 17].

materials and fabrication techniques that are not utilized in standard Si MOSFET technology. Additionally, the electrical and mechanical properties of the resulting flexible TFTs are significantly different to those that can be achieved with standard rigid Si MOSFETs.

1.2.2.1 Materials

The realization of flexible metal oxide semiconductor TFTs incorporates the use of different classes of materials: flexible substrates, dielectrics, conductive layers, and most importantly semiconductors.

Flexible substrates: In contrast to standard Si MOSFET technology, the substrate used for the realization of TFTs is in general not a part of the active device itself, since it only provides a surface for the fabrication process. Nevertheless, the substrate, especially if flexible, has a significant influence on the final TFT properties, as well as on the manufacturing process. The key requirements concerning the substrate are:

- The surface has to be compatible with standard thin-film fabrication technology, which calls for nanometer roughness values.
- The melting or glass transition temperature (T_m or T_G) has to be sufficiently high to be compatible with the chosen fabrication.
- The substrate has to be flexible enough, and at the same time has to provide sufficient stability for the manufacturing process.
- The deformation of the substrate caused by temperature gradients, mechanical load, and absorption (desorption) of gasses and liquids during the fabrication process has to be smaller than the minimum device feature size.
- Vacuum-processing techniques call for small outgassing rates, compatible with the available deposition tools.
- Concerning a future mass production and commercialization, the substrates should be at least potentially available in large quantities and sizes, as well as cost-effective.
- Furthermore, the substrate needs to be resistant to the chemicals used during the process (i.e. photoresists and developers).

- Finally, specific applications require substrates that are transparent, light-weight, conformable, stretchable, biocompatible, and even biodegradable.

Due to their properties and their availability, polymers are the natural choice and the most commonly used substrate material. Among the different polymers, polyimide (PI) foils with thicknesses between 5 μm [18] and 125 μm [19] are the most frequently utilized substrates. This is because of the numerous advantages of PI (commercially known as Kapton®): a small coefficient of thermal expansion (CTE) of 12×10^{-6} K, a small humidity expansion coefficient (9×10^{-6} %RH), a high T_G of ≈360 °C, and a surface roughness in the nanometer range [20]. Since standard PI exhibits a yellowish to brownish color, other polymeric substrates have been introduced to benefit from their transparency in the visual wavelength range. These materials, which are in general also cheaper and more easily available, include polyethylene terephthalate (PET) [10] polyethylene naphthalate (PEN) [21], polyetheretherketone (PEEK) [22], polyarylate (PAR) [23], polycarbonate (PC) [24], polypropylene (PP) based synthetic paper [25], parylene [26], polyethersulfone (PES) [27], water-soluble polyvinyl alcohol (PVA) [28], as well as stretchable and biocompatible polydimethylsiloxane (PDMS) [29].

An alternative to polymers is constituted by metal foils, such as Al foils [30], and stainless steel substrates [31]. The main benefit of metal foils is the high $T_m \geq 1000$ °C [32]. Nevertheless, metallic substrates are conductive and thus require additional insulating buffer layers, which increase weight and decrease flexibility.

Other typologies of supports include flexible and transparent glass substrates (with high T_G) [33], as well as paper [34].

Gate dielectrics: Besides the active layer, the gate dielectric plays also a key role in the device performance, due to the following reasons:

- The TFT drain current is directly proportional to the dielectric constant (ϵ_R) and inversely proportional to the thickness of the gate dielectric. For low-voltage device operation, thin gate dielectrics with high ϵ_R are desirable.
- The insulation properties, correlated with the specific resistance and pinhole density (and therefore the layer deposition quality) of the dielectric material define the gate leakage of the device.

- The quality of the interface between the gate dielectric and the semiconductor determines the interface trap density and influences thus the device performance and stability.

The most widely used gate dielectric is aluminum oxide (Al_2O_3), due to its comparably high ϵ_R around 9.5, its low pinhole density if deposited by atomic layer deposition (ALD), and, especially in combination with metal oxide semiconductors, its good interface quality. Employed materials with a higher ϵ_R include hafnium oxide (HfO_2) [35], hafnium lanthanum oxide (HfLaO) [36], titanium oxide (TiO_2) [37], yttrium oxide (Y_2O_3) [10], zirconium oxide (ZrO_2) [38], and tantalum oxide (Ta_2O_5) [39]. Nevertheless, these dielectrics present a scarcer availability, a worst interface quality, as well as a reduced compatibility with the TFT fabrication process. At the same time silicon oxide is a more established material, but results in a reduced ϵ_R of $\approx$3.9 [30].

Besides metal oxide dielectrics, also organic dielectrics can be used, especially solution-processed polymers like polyvinylpyrrolidon (PVP [40]), poly(methyl methacrylate) (PMMA) [41], and PVA [42]. Nevertheless, compared to metal oxide dielectrics, polymers yield lower ϵ_R.

A third class of gate dielectrics are ferroelectric materials, in particular poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] [21]. P(VDF-TrFE) can be reversibly polarized and used to generate a gate hysteresis of up to several volts in the TFT transfer characteristics. Such hysteresis allows realizing non-volatile memory elements. Interestingly, recently also chicken albumen ferroelectric gate dielectrics have been demonstrated [25].

A fourth class of gate dielectric materials is constituted by solid electrolytes, which allow achieving low-voltage device operation [43]. This improvement is generally ascribed by a redistribution of mobile ions with the applied voltage.

To combine the advantageous properties of different dielectric materials, hybrid and multi-layer dielectrics can also be utilized, e.g. TiO_2 with HfO_2 [24] PVP-Al_2O_3 [19], as well as tri-layer stacks like TiO_2 sandwiched between SiO_2 or TiO_2 sandwiched between HfO_2 [37].

Finally, an interesting approach is constituted by the use of cellulose fiber-based paper acting both as substrate and gate dielectric [34].

Conductive layers: This class of materials includes metals and other conductors employed to fabricate gate and source/drain electrodes.

Since the gate contact of a TFT does not need to conduct a significant amount of current, the material is in general selected to achieve a high compatibility with the TFT fabrication process. Consequently a variety of different metals like silver (Ag) [44], aluminum (Al) [33], gold (Au) [21] chromium (Cr) [6], copper (Cu) [45], molybdenum (Mo) [46], nickel (Ni) [19], platinum (Pt) [45], titanium (Ti) [29] as well other metal alloys have been used as gate contacts [36]. As regards adhesion to the flexible substrate, Cr and Ti show good results, whereas Cr often suffers from a high built-in strain [47].

Multi-layer metals offer in general a compromise between good adhesion and high conductivity, especially in the case of Ti/Au [6], Ti/Cu [48], Cr/Au [33], or Ti/Au/Ti gate stacks [49].

Besides metals, transparent indium tin oxide (ITO) [26], indium zinc oxide (IZO) [34], indium oxide (In_2O_3) [50], zinc indium tin oxide (ZITO) [51], and aluminum zinc oxide (AZO) [52] can be utilized.

As regards source/drain electrodes, the material has to provide a high conductivity and at the same time a small contact resistance with the active layer. Moreover, also adhesion and/or transparency need to be considered. These requirements resulted in the use of different metals: Al [36], Au [53], Cu [29], Mo [46], and Ti [52], whereas Mo and Ti seem to exhibit the lowest specific contact resistance.

At the same time, a big variety of multi-layer contacts have been developed to combine the advantageous properties of different materials; recent examples are: Ti/Au [45], Ni/Au [34], Mo/Al [54], Cr/Au [20], Mo/Al/Mo [55], or Ti/Au/Ti [49].

Transparent source/drain can be realized with ITO [26] or IZO [43].

Finally, solution-deposited source/drain (as well as gate) contacts have been realized with organic poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) [56] or ITO [57].

Semiconductors: The choice of the semiconducting active layer strongly influences the carrier mobility, and thus both the DC and the AC performance of flexible TFTs. In general, metal oxide semiconductors are characterized by a wide band gap ($E_g > 3\,eV$), a large transmission in the visible range (>80 %), a high carrier concentration in the order of $10^{16}\,cm^{-3}$-$10^{21}\,cm^{-3}$, and a carrier mobility above $10\,cm^2\,V^{-1}\,s^{-1}$ [58]. The predominantly n-type characteristics is explained by the electronic structure of metal oxide semiconductors. The

conduction band minimum (CBM) of metal oxide semiconductors is indeed formed by highly dispersive unoccupied metal orbitals, whereas the valence band maximum (VBM) is constituted by fully occupied and localized oxygen orbitals. Due to the spherical (i.e. non directional) properties of the metal orbitals, electron transport can easily occur through the direct overlap of the metal orbitals in neighboring metal cations, whereas hole transport is prevented by a larger effective mass [9]. Nevertheless, together with a large range of n-type vacuum- and solution-processed metal oxide semiconductors, also p-type active layers have also been demonstrated.

In the case of flexible n-type vacuum-processed metal oxide semiconductor TFTs, amorphous indium gallium zinc oxide (IGZO) is the most used material [21]. State of the art flexible amorphous IGZO TFTs exhibit average field-effect mobility μ_{FE} of $\approx$15 $cm^2\,V^{-1}\,s^{-1}$ (with maximum values up to 76 $cm^2\,V^{-1}\,s^{-1}$ [37]). Also c-axis aligned crystalline (CAAC) IGZO TFTs on plastic foils have been demonstrated [59]. Crystalline ZnO is the second most used vacuum-processed metal oxide semiconductor in flexible TFTs [35]. Other metal oxide semiconductors used are: IZO [60], gallium zinc oxide (GZO) [61] and zinc tin oxide (ZTO) [62]. Despite being considered a conductor in general, thin layers of ITO can also be used [44].

Contrary to most organic semiconducting materials, metal oxide semiconductors are not at all or only poorly soluble in common solvents. This is why, solution-processing of metal oxide semiconductors typically requires a chemical reaction (synthesis) between suitable reagents (the so-called precursors) at high process temperatures, which limits their deposition on flexible substrates. Most suitable metal oxide semiconducting materials that can be solution-processed at low temperatures are crystalline and binary In_2O_3 and ZnO. Flexible TFTs based on neat solution-processed In_2O_3 or ZnO films exhibit μ_{FE} values up to 4 $cm^2V^{-1}s^{-1}$ [63] and 7 $cm^2\,V^{-1}\,s^{-1}$ [64], respectively. Recently also IZO [65], ZTO [38], indium gallium oxide (IGO) [66], and IGZO [57] have been solution-deposited at low temperatures.

Realizing p-type TFTs with metal oxide semiconductors is complicated, especially if low temperatures are targeted to fabricate on flexible substrates. To date, only tin oxide (SnO_x) [34] and cuprous oxide (Cu_xO) [67] have been incorporated into flexible p-type TFTs. In particular, flexible SnO_x and Cu_xO devices yield a maximum μ_{FE} of 5.87 $cm^2\,V^{-1}\,s^{-1}$ [68] and 0.0022 $cm^2\,V^{-1}\,s^{-1}$ [67], respectively.

To date and to the best of my knowledge, there is no report on flexible p-type solution-processed metal oxide semiconductor devices. This is why alternative p-type active layers that allow room temperature processing are under investigation. An interesting material is copper (I) thiocyanate (CuSCN) – an inorganic molecular compound– that can be easily spin-casted at low process temperatures [69]. Nevertheless, up to now, only rigid TFTs based on solution-processed CuSCN layers have been demonstrated (with μ_{FE} up to $0.5\,cm^2\,V^{-1}\,s^{-1}$) [69].

1.2.2.2 Fabrication techniques

The fabrication of flexible metal oxide semiconductor TFTs utilizes several approaches to prepare (and/or handle) the flexible substrates, as well as to deposit and structure the various device layers. Some of these approaches (especially for vacuum-processed devices) employ standard semiconductor fabrication tools, while other approaches require techniques especially developed for flexible TFTs.

Substrate preparation: Free-standing flexible substrates are widely employed [61], due to their compatibility with large-scale substrates and future roll-to-roll processes, as well as due to their mechanical robustness (resulting in insensitivity against mechanical shocks). At the same time free-standing substrates also present drawbacks:

- They have to be sufficiently thick and stable to be mechanically handled with tweezers.
- They can suffer from expansion caused by temperature gradients or by the absorption of solvents.
- They have to be temporarily attached to a rigid carrier (at least during the use of standard photolithographic tools).

One way to simplify the use of photolithographic tools like mask aligners or spinners is to bond the flexible foil to a glass or Si wafer for the complete fabrication process [21].

In alternative to flexible foils manufactured independently from the TFTs, it is also possible to create the flexible substrate by covering a host substrate with a polymer [26]. The advantages of these fabrication techniques based on a rigid support are a high compatibility with the standard fabrication processes on Si or glass wafers, a reduction of the expansion of the substrate during the manufacturing process, as well

as the possibility to realize devices on very thin (≈1 μm) substrates. After the TFT fabrication is completed, the flexible foils or thin deposited polymer layers carrying the devices can be separated from the rigid support using: 1) mechanical peeling [32], 2) a low adhesion releasing layer [70], 3) a supporting laser [71], or 4) a sacrificial layer between the host carrier and the polymer [29].

In addition to the different handling possibilities, the substrate preparation typically includes a heat treatment step prior to the device fabrication itself. In the case of fabrication on free-standing plastic foil or foil bonded to a host substrate, the substrate is backed at high temperatures (around 200 °C) for several hours, to remove trapped residual liquids [36]. This step allows also pre-shrinking flexible substrates that are not permanently attached to a rigid support.

Deposition methods: Besides the standard criteria used for thin-film deposition techniques on Si or glass wafer (e.g homogenous and dense layers), there are extra requirements that are especially important for the realization of flexible devices. These include:

- Low process temperatures, compatible with the thermal resistance of the employed flexible substrates.
- A sufficient adhesion of the deposited materials to the substrate, in order to prevent a possible delimitation of the layers, especially when the substrate is bent.
- Finally, the strain built in the deposited materials has to be small enough to allow good mechanical properties (e.g. bendability) of the final devices.

The predominant technique to deposit n-type and p-type vacuum-processed metal oxide semiconductors is sputtering (RF, RF-magnetron, or DC [68, 6]). The advantages of sputtering are the large availability of sputter tools, the low (typically room) deposition temperature, as well as the good adhesion and dense structure of the final layers. Additionally, sputter tools offer several opportunities to optimize the layer properties, by adjusting the power and/or the sputtering pressure. Furthermore, ZnO can also be deposited by ALD [52], plasma

enhanced atomic layer deposition (PEALD) [18], and pulsed laser deposition (PLD) [10]. Even if ALD has the advantage that the layers are conformal, the process is slow and less prone to variations.

The deposition of dielectrics aims at a high ϵ_R, a low pinhole density and a good sidewall coverage. This is why, conformal deposition techniques are well-suited, especially ALD [26], PEALD [18], and plasma-enhanced chemical vapor deposition (PECVD) [61]. These depositions are in general done at temperatures between 150 °C and 200 °C.

As regards the deposition of conductive materials, we have to distinguish between metals and transparent metal oxide conductors. Metals are typically deposited using e-beam [6] or thermal evaporation [19], which ensure a non-conformal shape of the layers that is beneficial for subsequent lift-off processes. Non metallic but transparent metal oxide conductors have been fabricated mainly by sputtering [32].

At the same time, semiconductors, dielectrics and conductive films can also be solution-deposited using the following techniques:

- Spin-coating is the most common coating method, due to the simplicity, the low investment costs, as well as the resulting homogeneous and reproducible film properties. As a drawback, spin-coating can only be carried out in batch processes and becomes more difficult when the substrate size is increased. Spin-coating is commonly utilized to grow metal oxide semiconductors (e.g. In_2O_3 [65], ZnO [42], or IGZO [57]), organic and metal oxide gate dielectrics (e.g. PVP [40], P(VDF-TrFE) [21] or Al_2O_3 [57]), and sometimes also source/drain and gate electrodes (ITO [57]).

- Drop casting is probably the simplest deposition technique, especially suited for nanowire (NW) or nanorod (NR) metal oxide semiconductors [72].

- Hydrothermal growth is a solution-based method that can be easily configured to achieve compact films (e.g. ZnO [64]).

- A more sophisticated method is ink-jet printing, which is a digitally controlled drop-on-demand deposition technique. During ink-jet printing, the metal oxide semiconductor is deposited only where needed, preventing waste of material and need for subsequent patterning steps. However, due to the patterned deposition, the ink drying conditions need to be specially controlled, in order to avoid irregularities and effects like the coffee ring

formation. Ink-jet printing has been utilized mainly to deposit metal oxide semiconductors (ZnO, In_2O_3, or ZTO) [38].

- In the process of spray pyrolysis, a fine spray of the precursor solution is created (using an air-blast or an ultrasonic nozzle) and directed onto a heated substrate [73]. Given a sufficiently high substrate temperature, the precursor immediately undergoes the conversion reaction and forms the final film material. In addition to the specific precursor material and concentration, parameters such as substrate temperature, droplet size and distribution, as well as solvent type and feed rate present the toolbox to fine tune the material parameters. Good film properties of metal oxide semiconductors processed via spray pyrolysis are normally achieved for temperatures ≥300 °C-400 °C [74], thereby ruling out plastic substrates. However, recent advances have enabled the realization of spray-coated In_2O_3 TFTs at 250 °C on rigid substrates [73]. Main advantage of spray pyrolysis is the possibility to automate the process, ensuring repeatability of the film characteristics. In addition, the spray pyrolysis deposition can be further up-scaled, and potentially run in a continuous process.

- Aerosol-jet printing combines attributes from spray pyrolysis and ink-jet printing. In aerosol-jet printing, a fine mist is created and shaped (by an inert carrier gas and a special nozzle design), allowing localized and digitally controlled deposition. Aerosol-jet printing has been utilized to realize semiconductors (ZnO), dielectrics (ionic gel), and gate electrodes (PEDOT:PSS) [56].

Layer structuring: As for the structuring of layers on rigid wafers, patterning of thin-films on flexible substrates is mainly done by etching and lift-off processes. However, the definition of flexible structures needs to be adapted to the mechanical and chemical properties of the substrates. Since the most common substrates, in particular PI foils, are resistant to standard photolithographic chemicals, UV lithography is widely used [32]. Employing etching and lift-off processes allows realizing flexible structures with lateral feature size down to 1 μm [75]. If the chosen substrate is not resistant to chemicals (e.g. photoresists, developers and/or strippers) and if feature sizes ≫1 μm are sufficient, shadow masking can be used [36]. Shadow mask structuring does not require any photoresist baking step and allows therefore preventing unintended annealing of the devices, as well as undesired thermal load

of the substrate leading to subsequent expansion. The problem of substrate expansion is illustrated by the fact that a 7.6 cm × 7.6 cm large PI substrate undergoes an expansion of ≈25 μm (in each direction) during a 150 °C TFT fabrication process [20]. Due to this expansion, tolerances of ≈10 μm on the photolithographic masks are necessary, limiting the minimum feature sizes that can be achieved. In particular, special care needs to be taken during the alignment of the source/drain contacts to the gate electrode, which can result in large total overlap lengths (L_{OV}) and low transit frequencies (f_T). A solution to misalignment caused by thermally-induced substrate expansion is constituted by self-aligned (SA) lithography. Due to the transparency of the majority of flexible substrates, the photoresist can be structured using back-side exposure and predefined opaque patterns (e.g. metallic gate contacts) [75]. In this way, there is no need for tolerances on the photolithographic masks and feature sizes down to 0.5 μm are possible [20].

Additionally, some solution deposition techniques allow alternative structuring possibilities. For example, ink-jet and aerosol-jet printing are direct writing methods (i.e. the liquid deposition is carried out only where desired) that enable feature sizes down to few tens of microns [56]. Finally, even if not inherently a direct writing method, spray pyrolysis can be combined with shadow masking.

Device configurations: Most peculiar planar TFT structures are: bottom-gate (BG) and top-gate (TG) architectures, depending whether the gate electrode is deposited before or after the active layer. BG and TG devices can be either staggered or coplanar, depending if the source/drain contacts are on the opposite or on the same side of the semiconductor/dielectric interface. BG [19], especially staggered, are the most common geometry due to easier processing and enhanced performance [9]. Nevertheless, BG structures call for an additional layer (back-channel passivation) that protects the back channel from air exposure and therefore hinders undesired instability effects [9]. TG structures are also well employed, especially in combination with fragile gate dielectrics that do not survive extensive processing and/or chemicals [e.g. P(VDF-TrFE)] [53]. Additionally, in TG TFTs the gate dielectric can also act as a passivation, reducing thus the number of patterning steps [10]. To improve the DC performance, double-gate (DG) TFT structures can be employed [47]. In DG TFTs, an additional gate is utilized to effectively control the semiconductor channel.

1.2.2.3 Electrical performance

One of the main reasons why flexible metal oxide semiconductor TFTs have received an increasingly amount of attention in the last years is their electrical performance, which is superior to other flexible TFT platforms, especially organic and a-Si technologies (see Table 1.1).

N-type vacuum-processed TFTs: Table 1.2 presents an overview of the electrical performance of state of the art flexible n-type vacuum-processed metal oxide semiconductor TFTs. The best performance parameters ever reported for flexible n-type vacuum-processed metal oxide semiconductor TFTs are highlighted in **bold**.

The best DC performance parameters include: a μ_{FE} of 76 $cm^2\,V^{-1}\,s^{-1}$ [37], a sub-threshold swing SS as low as 69 mV/dec [47], and current on/off ratio I_{ON}/I_{OFF} up to 2×10^{10} [45]. Furthermore, a wide range of positive and negative threshold voltage (V_{TH}) values have been presented, illustrating that it is possible to realize both enhancement and depletion mode TFTs.

The AC performance of flexible field-effect transistors (FETs) is typically quantified by the transit frequency f_T [77], which is given by [78]:

$$f_T = \frac{1}{2 \cdot \pi} \cdot \frac{g_m}{C_G} \propto \frac{\mu_{FE}}{L \cdot (L + L_{OV})}, \tag{1.1}$$

where g_m is the transconductance ($g_m = \frac{dI_D}{dV_{GS}}$), C_G the gate capacitance, μ_{FE} the effective mobility, L the channel length, and L_{OV} the total overlap length between gate and source/drain electrodes. A first approximation of f_T can be calculated from g_m and C_G values extracted from the current-voltage and capacitance-voltage TFT characteristics, respectively. A more precise value of the f_T can be calculated by measuring the TFT's S-parameters and calculating the corresponding small signal current gain h_{21} as a function of the frequency. f_T is then given by the value where $|h_{21}|$ equals 1. Even if f_T is an important parameter (e.g. for analog circuits), it is only rarely measured and reported. A few direct measurements of f_T of flexible n-type vacuum-processed metal oxide semiconductor TFTs resulted in values in the Megahertz regime [75, 20], with the highest f_T value of 135 MHz reported for a flexible self-aligned IGZO TFT with 500 nm channel length [20].

	μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	V_{TH} (V)	SS (mV/dec)	I_{ON}/I_{OFF}	f_T (MHz)	Channel Length (μm)	Substrate Thickness (μm)	Bending Radius (mm)	Strain (%)	Bending Cycles
IGZO TFT with stacked TiO_2 dielectric [37],	**76**	0.5	129	1×10^3	-	32	-	15	0.43	-
DG IGZO TFT [47],	8.5	0.95	**69**	2×10^9	-	10	50	5	0.55	-
BG IGZO TFT [45],	15.3	1	126	$\mathbf{2 \times 10^{10}}$	-	60	50	1.9	1.4	1
SA IGZO TFT [20],	7.5	0	130	2×10^9	**135**	**0.5**	50	3.5	0.72	1
IGZO TFT on thin PI [6],	17	0.6	165	-	-	15	**0.7**	**0.025**	-	1
IGZO TFT with hybrid buffer [76],	15.5	4.1	200	5×10^9	-	-	125	3.3	**1.89**	10.000
IGZO TFT on islands [71].	14	-	-	1×10^7	-	4	17	1	-	**100.000**

Table 1.2: Set of performance parameters extracted from state of the art flexible n-type vacuum-processed metal oxide semiconductor TFTs. The best performance parameters ever reported are highlighted in **bold**.

N-type solution-processed TFTs: Table 1.3 presents an overview of the electrical performance of state of the art flexible n-type solution-processed metal oxide semiconductor TFTs. As shown in Table 1.3, the DC performance strongly depends on the semiconductor solution deposition approach (based on nano-scaled shapes or precursors) and technique, as well as on the maximum process temperature. As regards devices based on nano-scaled shapes, a wide range of performance parameters can be obtained in dependence of the employed shape, e.g. nanoparticles (NPs), nanorods (NRs) or nanowires (NWs). On one hand, flexible NP TFTs typically yield a low $\mu_{FE} \ll 1\,cm^2V^{-1}s^{-1}$ [72]. The limited performance of flexible NP-based devices can be attributed to the large surface roughness of flexible foils (if compared to rigid Si or glass substrates), which limits the realization of high-quality nanoparticles. On the other hand, NWs allow realizing longer TFT channels (extending over several microns) based on long range and undisturbed crystalline metal oxide semiconductors. Therefore flexible NW metal oxide semiconductor devices exhibit μ_{FE} up to $120\,cm^2V^{-1}s^{-1}$ (for In_2O_3 NW TFTs) [79]. Nevertheless, the random orientation and placement of NWs currently hinders their integration in large-area substrates. Especially for integration purposes, TFTs based on n-type metal oxide semiconductors solution-processed from precursors are preferable. Flexible TFTs based on metal oxide semiconductor solution-processed from precursors yield a widespread range of μ_{FE} values between $\approx 0.1\,cm^2V^{-1}s^{-1}$ [83] up to $84\,cm^2V^{-1}s^{-1}$ [57].

To date, no AC performance of flexible n-type solution-processed metal oxide semiconductor TFTs has been reported.

P-type TFTs: Table 1.4 compares the electrical performance obtained for recently reported flexible p-type vacuum-processed metal oxide semiconductor TFTs. As shown in Table 1.4, flexible p-type vacuum-processed metal oxide semiconductor devices yield μ_{FE} up to $5.87\,cm^2\,V^{-1}\,s^{-1}$ (for SnO_x TFTs) [68] and I_{ON}/I_{OFF} up to 4×10^4 [84].

To date, no AC performance of flexible p-type vacuum-processed metal oxide semiconductor TFTs has been reported.

1.2.2.4 Mechanical properties

A complete set of performance parameters of flexible TFTs cannot be limited to the electrical characteristics, but needs to deal also with the mechanical properties. Bending is the most common technique

	Semicond. Deposition	Max. Temp. (°C)	μ_{FE} ($cm^2\,V^{-1}\,s^{-1}$)	V_{TH} (V)	I_{ON}/I_{OFF}	Substrate Thickness (μm)	Bending Radius (mm)	Strain (%)	Bending Cycles
ZnO NR TFT with electrolyte dielectric [72],	Drop-casting	150	0.03	0.8	1×10^2	-	1.1	-	100
In_2O_3 NP TFT with electrolyte dielectric [80],	Ink-jet printing	**RT**	0.8	0.55	2×10^3	125	-	-	-
ZnO TFT with PVP dielectric [42],	Spin-casting	200	0.09	5.4	1×10^5	12	4.3	-	**10000**
ZnO TFT with electrolyte dielectric [56],	Aerosol-jet printing	250	1.6	0.97	1×10^5	50	25	**1**	**10000**
Quasi-superlattice TFT with ZrO_2/Al_2O_3 dielectrics [81],	Spin-casting	175	11	0.5	1×10^5	-	-	-	
IGZO TFT with Al_2O_3:Zr dielectric [82],	Spin-casting	150	7.7	1.26	$\mathbf{1 \times 10^9}$	**3**	**1**	-	-
IGZO TFTs with Al_2O_3 dielectric [57].	Spin-casting	350	**84**	0.6	1×10^5	18	10	-	320

Table 1.3: Set of performance parameters extracted from state of the art flexible n-type solution-processed metal oxide semiconductor TFTs. The best performance parameters ever reported are highlighted in **bold**.

	Depos./Anneal. Temp. (°C)	μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	V_{TH} (V)	I_{ON}/I_{OFF}	Substrate Thickness (μm)	Bending Radius (mm)	Bending Cycles
Cu_xO TFT [67],	Room/150	0.0022	-4.75	-	-	-	-
SnO_x TFT with and on paper [34],	Room/150	1.3	-1.4	1×10^2	75	-	-
Nano-crystalline Cu_xO TFT [84],	**Room/-**	0.8	-	$\mathbf{4 \times 10^4}$	-	-	-
SnO_x TFT with HfO_2 dielectric [68],	Room/150	**5.87**	-1	6×10^3	-	**10**	**200**
SnO_x TFT with P(VDF-TrFE) dielectric [85].	Room/200	2.51	-11.73	1×10^2	-	-	-

Table 1.4: Set of performance parameters extracted from state of the art flexible p-type vacuum-processed metal oxide semiconductor TFTs. The best performance parameters ever reported are highlighted in **bold**.

employed to induce strain in flexible TFTs. This is mainly because bent thin-film devices enable many applications like rollable displays, smart labels, seamless and embedded patch-like systems, electronic textiles, and implantable electronic devices for medical equipment. While rollable displays, smart labels, as well as embedded patch-like systems can be realized using flexible TFTs with minimum bending radii in the centimeter range, smart electronic textiles call for much smaller radii in the sub-millimeter regime. On the other side, medical applications need thin-film devices that can adapt to the human body, e.g. to a human hair that exhibits a radius of ≈50 μm.

Bendability: Flexible metal oxide semiconductor TFTs, especially based on vacuum-processed IGZO active layers, bent to different radii (mainly in the centimeter range) have been characterized by many research groups [26, 18, 19, 37, 32, 30]. Mechanical bending tests are in general performed by winding the flexible TFT substrate around cylindrical rods. At the same time, some research groups have also developed automated bending testers, which can be used to perform multiple bending and re-flattening cycles [19, 18], as well as to characterize the TFTs at arbitrary bending radii while the devices are connected to a parameter analyzer [86]. The approach based on the bending tester allows carefully controlling the applied strain during the entire measurement, and in some cases also ensures a permanent and reliable contact between the TFTs and the characterization equipment. Independently of the measurement setup, flexible metal oxide semiconductor TFTs can be bent down to 50 μm in the case of tensile (outward) bending [26] and down to 25 μm for compressive (inward) bending [6]. As visible from Table 1.2, the maximum strain values do not only depend on the minimum bending radius, but also on the device materials and thicknesses. Since the calculation of the mechanical strain in a multi-layer system can be complex, different equations have been used to estimate numerical values of the strain induced by bending. One of the most common approximations is the following [87]:

$$\epsilon = \left(\frac{1}{r} \pm \frac{1}{r_0}\right) \times \frac{t_S + t_D}{2} \times \frac{\frac{Y_D}{Y_S}\left(\frac{t_D}{t_S}\right)^2 + 2\frac{Y_D}{Y_S}\frac{t_D}{t_S} + 1}{\frac{Y_D}{Y_S}\left(\frac{t_D}{t_S}\right)^2 + \frac{Y_D}{Y_S}\frac{t_D}{t_S} + \frac{t_D}{t_S} + 1}, \tag{1.2}$$

where r is the bending radius, r_0 is the initial bending radius caused

by the built-in strain (has to be added if the built-in strain is in the opposite direction as the induced strain, elsewhere subtracted), t_S and t_D are respectively the thicknesses of the substrate and of the device, and Y_S and Y_D are the Young's moduli of the substrate and the device, respectively. The highest strain values at which flexible n-type vacuum-processed metal oxide semiconductor TFTs have been able to operate is 1.89 % (tensile direction) [76].

In addition to one-time bending tests, also the TFT resistance to mechanical fatigue caused by repeated bending and re-flattening cycles has been investigated. In particular, tensile bending cycles up to 100.000 have been reported [71, 19].

Influence of strain: While the majority of the published bending measurements have only confirmed the functionality of the devices at a given bending radius or after repeated bending cycles, other more sophisticated experiments have focused on the influence of strain on the electrical TFT performance. In the majority of the cases (for vacuum-processed IGZO TFTs), bending results in a increase of the drain current under tensile bending, and in a decrease of the drain current under compressive strain. At a typical tensile strain of ≈0.5 %, the drain current changes are caused by an increase of the μ_{FE} by ≈2.5 % and by a decrease of the V_{TH} by ≈20-200 mV. At the same time, compressive strain of ≈0.5 % causes μ_{FE} and V_{TH} changes around ≈-2 % and ≈10-150 mV, respectively [47, 31, 30, 45]. The observed V_{TH} and μ_{FE} shifts induced under tensile/compressive bending have been explained by an increase/decrease of the carrier density caused either by the creation of oxygen vacancies [88] or by a change of the electronic structure [86].

1.2.3 Flexible metal oxide semiconductor-based circuits

For future applications, not only single metal oxide semiconductor TFTs, but also circuits constituted by a larger number of devices are required. The majority of the reported circuits are digital gates or analog amplifiers based on unipolar n-type vacuum-processed metal oxide semiconductors (mainly IGZO) [86]. N-type solution-processed metal oxide semiconducting materials are only rarely used for circuits, and in any case only for unipolar inverters (NOT gates) or test structures like ring oscillators (ROs) [56, 72]. At the same time, complementary circuits can be realized by either employing n- and p-type metal oxide

semiconductors, or by complementing n-type metal oxide active layers with p-type organic materials.

1.2.3.1 Unipolar circuits

Due to the scarce performance and availability of p-type metal oxide semiconductors, n-type unipolar circuits (both digital and analog) have been widely employed.

Digital circuits: Flexible unipolar vacuum-processed IGZO NOT gates can typically achieve gains up to 2.5 V/V at 20 V supply [89], whereas aerosol-jet printed ZnO NOT gates yield gains up to 8 V/V (at a supply voltage of 2 V) [56]. Besides NOT gates, ROs (i.e. digital test circuits comprising an odd number of NOT gates –the so-called delay stages– connected in a closed loop chain) are commonly utilized. Key parameter for ROs is the stage delay, which is a measure of the maximum switching speed that can be achieved in larger digital gates. The lowest stage delay ever reported is of 16 ns at 18 V supply voltage (for vacuum-processed ZnO 16-stage ROs) [90]. At the same time, also IGZO-based NAND gates [6], display driving circuits (e.g. line drivers [91] or shift registers [92]), as well as near-field communication (NFC) transceivers [46] (with up to 438 TFTs and an occupied area of 10.884 mm^2) have been reported.

Analog circuits: To date, the majority of the reported flexible metal oxide semiconductor-based analog circuits are single- or multiple-stage amplifiers. The highest DC gain of 44.67 V/V and gain bandwidth product (GBWP) of 18.5 MHz has been achieved for a self-aligned IGZO TFT-based Cherry-Hooper amplifier [93]. Apart from this example, other metal oxide semiconductor-based amplifiers show DC gains ≤20 V/V and GBWP ≤ 2.2 MHz. The flexible metal oxide semiconductor-based analog circuit with the largest TFT count is an operational amplifier with 16 IGZO TFTs [94].

1.2.3.2 Complementary circuits

Low-power and compact circuit design calls for complementary circuitry based on n- and p-type TFTs with similar performance (especially μ_{FE}). This is particularly difficult in the case of metal oxide semiconductors, due to the typically low μ_{FE} of flexible p-type devices.

For this reason, only few groups have reported flexible complementary circuits (mainly NOT gates and ROs) based on n- and p-type metal oxide semiconductor TFTs [34, 67, 35]. To overcome this bottleneck, other technologies have been considered to realize the p-type channel. For instance, p-type organic semiconductors like pentacene [95], poly-(9,9-dioctylfluorene-co-bithiophene) (F8T2) [96], and single-walled carbon nanotubes (SWCNTs) [97] have been combined with n-type metal oxide active layers to realize flexible hybrid complementary circuits.

Digital circuits: Flexible complementary metal oxide semiconductor-based NOT gates achieve gains up to 165 V/V nearly perfectly centered at midpoint voltages V_M = 14 V (for supply voltages of 30 V) [98]. Besides NOT gates, also complementary NAND or NOR logic gates (e.g with IGZO and SnO_x [99] or with IGZO and SWCNTs [97]) and ROs (with up to 1004 IGZO and SWCNT TFTs [97]) have been shown.

Analog circuits: At the same time, by complementing IGZO TFTs with SnO_x TFTs, flexible common-source and differential amplifiers with gains respectively of 16.3 V/V and 4.1 V/V have been realized [99]. Finally, also common-source amplifiers based on IGZO and SWCNT devices with gains >1.77 V/V have been shown [100].

1.3 Objectives

This thesis aims at exploring and advancing the field of metal oxide semiconductor TFTs for flexible electronics. The first objective of the work focuses on short-channel flexible metal oxide semiconductor devices and how the device structure and fabrication process can be modified to realize TFTs with sub-500 nm feature sizes. Here, vertically integrated device architectures (both vertical and quasi-vertical TFT geometries) are investigated and applied to flexible IGZO TFTs. Additionally, the use of two-photon direct laser writing (DLW) photolithography is also explored as a viable route to manufacture flexible planar IGZO TFTs with short channel lengths. In the second objective, the focus is on low-temperature and scalable manufacturing techniques and how the materials and processes can be adapted to obtain flexible devices based on solution-deposited semiconductors. In particular, flexible TFTs and unipolar circuits based on spray-coated In_2O_3 n-type

active layers are shown. Furthermore, also flexible TFTs and unipolar circuits based on spin-coated p-type inorganic CuSCN and organic SWCNTs are demonstrated. In the last objective, the integration of metal oxide semiconductor TFTs for flexible electronic applications is tackled. In particular, flexible non-volatile memory devices employing ferroelectric P(VDF-TrFE) gate dielectrics and IGZO active layers are first investigated. Then, flexible complementary circuits based on the integration of n-type metal oxide semiconductors (either IGZO or spray-coated In_2O_3) and p-type solution-processed SWCNTs are presented. Especially, the realization of flexible complementary circuits employing fully solution-deposited semiconductors is evaluated as a step towards flexible low-power and solution-processed electronics.

1.3.1 Flexible short-channel device structures

The realization of flexible metal oxide semiconductor devices is in general difficult due to the limited thermal and mechanical stability of flexible substrates. On one hand, when frequencies below 100 Hz are sufficient for applications like optical displays these limitations can be overcome with large feature sizes and tolerances. On the other hand, when frequencies in the Megahertz regime are targeted for flexible and compact transceivers, RFID tags, or AM radios novel device structures and fabrication processes are required to achieve short channel lengths.

In this thesis, the following research questions concerning short-channel flexible metal oxide semiconductor devices are tackled:

- Which specific properties of flexible substrates limit the minimum feature sizes of flexible metal oxide semiconductor TFTs?
- Which device structures and fabrication processes allow overcoming these limitations?
- How can such device structures reliably be applied to realize flexible IGZO TFTs with sub-500 nm channel lengths?
- Can the resulting short-channel IGZO TFTs be bent to radii in the centimeter range?

1.3.2 Solution-based materials and processes

To fully exploit the potential of flexible metal oxide semiconductor TFTs for next-generation electronic applications (e.g. rollable and foldable displays, disposable smart labels), the development of large-area and simple solution processes is required. Among the various solution techniques demonstrated, spray pyrolysis is especially appealing since it offers a scalable and cost-effective route for high throughput and large-area deposition of various metal oxide semiconductors. Recent development in low-temperature spray pyrolysis have allowed the fabrication of n-type In_2O_3 TFTs at 250 °C on rigid substrates [73].

Within this work the following research questions are addressed, aiming at the evaluation of solution-processed materials and processes for flexible devices:

- Is it possible to realize flexible TFTs employing In_2O_3 spray-deposited at temperatures ≤250 °C?
- Can the resulting In_2O_3 TFTs be bent to radii in the centimeter range?
- Can logic circuits based on spray-coated In_2O_3 be fabricated?
- What is a suitable inorganic or organic low-temperature solution-processable p-type semiconductors?

1.3.3 Material and device integration and application

To realize novel flexible electronic applications (e.g. smart labels and intelligent packaging, seamless and embedded electronic devices, wearable sensory systems), also memory and logic functionality need to be integrated on flexible substrates. At this regard, memories as well as logic circuits that combine mechanical flexibility, small footprint, and low-power dissipation are required. As regards memory functionality, an attractive possibility is offered by ferroelectric gate dielectrics [especially P(VDF-TrFE)], which can be integrated in flexible TFTs to realize non-volatile memories. However, to use these non-volatile memories in flexible applications, it is crucial to understand their behavior under applied mechanical strain (both tensile and compressive), especially in view of the piezoelectric properties of P(VDF-TrFE). For logic functionality, low-power and compact complementary

circuits are desirable. Nevertheless, the realization of a flexible metal oxide semiconductor-based complementary technology is limited by the scarce performance and availability of p-type TFTs. At this regard, p-type organic semiconductors (especially SWCNTs) are drawing considerable attention, owing to their good electrical and mechanical properties, as well as solution-processability.

In this thesis, answers to the following research questions concerning the integration and application of flexible metal oxide semiconductors will be given:

- What is the influence of mechanical strain (both tensile and compressive) on the performance of non-volatile flexible memory TFTs employing ferroelectric P(VDF-TrFE) gate dielectrics?
- Is it possible to integrate solution-processed SWCNTs with n-type metal oxide semiconductors (either IGZO or spray-deposited In_2O_3) to realize flexible complementary logic circuits?
- Can the resulting flexible complementary logic circuits be bent to radii in the centimeter range?

1.4 Thesis Outline

The thesis is structured into seven chapters. In chapter 2, a summary of the achievements is given, the conclusions are drawn and the limitations of the work are highlighted. Finally, an outlook over the field with a prediction of possible future research directions is provided. In chapters 3 to 7, five scientific publications are presented, according to the order shown in Table 1.5. Fig. 1.1 explains the structure of the thesis together with the relation of each scientific article to the formulated objectives of this work.

In chapter 3, short-channel flexible metal oxide semiconductor TFTs are first reviewed. Then, vertical TFT (VTFT) structures are introduced and applied to fabricate flexible IGZO devices with channel lengths down to 500 nm. The realization of even shorter channel lengths of 300 nm by means of quasi-vertical TFT (QVTFT) architectures is presented in chapter 4. In chapter 5, the focus is on solution-processed metal oxide semiconductors for flexible devices. In particular, flexible TFTs and unipolar logic circuits based on spray-coated

Table 1.5: Publications and corresponding chapters in this thesis.

Chapter	Publication
3	Mechanically flexible vertically integrated a-IGZO thin-film transistors with 500 nm channel length fabricated on free standing plastic foil L. Petti, P. Aguirre, N. Münzenrieder, G.A. Salvatore, C. Zysset, A. Frutiger, L. Büthe, C. Vogt, and G. Tröster IEEE International Electron Devices Meeting, IEDM, San Francisco, USA, pp. 11.4.1-11.4.4, 2013
4	Flexible quasi-vertical In-Ga-Zn-O thin-film transistor with 300 nm channel length L. Petti, A. Frutiger, N. Münzenrieder, G.A. Salvatore, L. Büthe, C. Vogt, G. Cantarella, and G. Tröster IEEE Electron Device Letters, 36 (5), pp. 475-477, 2015
5	Low-temperature spray-deposited indium oxide for flexible thin-film transistors and integrated circuits L. Petti, H. Faber, N. Münzenrieder, G. Cantarella, P.A. Patsalas, G. Tröster, and T.D. Anthopoulos Applied Physics Letters, 106 (9), p. 092105, 2015
6	Influence of mechanical bending on flexible InGaZnO-based ferroelectric memory TFTs L. Petti, N. Münzenrieder, G.A. Salvatore, C. Zysset, T. Kinkeldei, L. Büthe, and G. Tröster IEEE Transactions on Electron Devices, 61 (4), pp. 1085-1092, 2014
7	Integration of solution-processed (7,5) SWCNTs with sputtered and spray-coated metal oxides for flexible complementary inverters L. Petti, F. Bottacchi, N. Münzenrieder, H. Faber, G. Cantarella, C. Vogt, L. Büthe, I. Namal, F. Späth, T. Hertel, T.D. Anthopoulos, and G. Tröster IEEE International Electron Devices Meeting, IEDM, San Francisco, USA, pp. 26.4.1-26.4.4, 2014

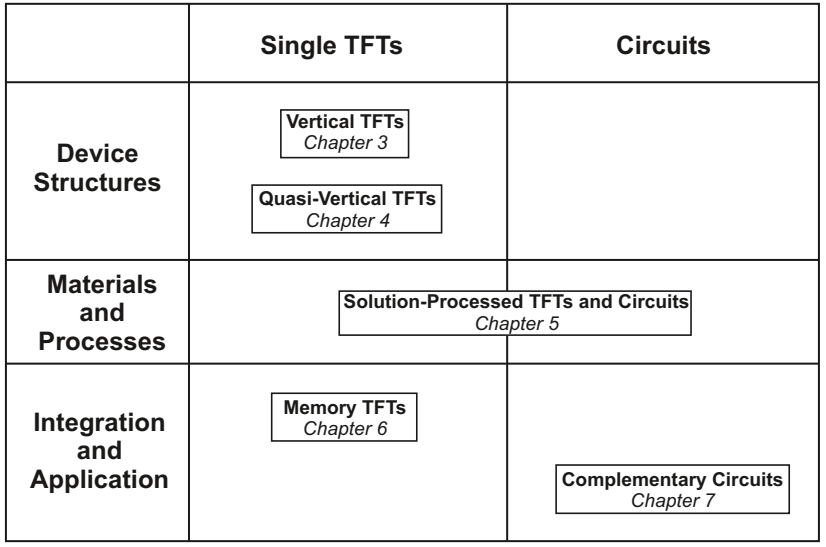

Figure 1.1: Outline of the thesis, structured into seven chapters.

In_2O_3 are demonstrated. The last two chapters 6 and 7 deal with the application of metal oxide semiconductor TFTs for flexible electronics. In chapter 6, non-volatile memory TFTs based on IGZO active layers and ferroelectric P(VDF-TrFE) gate dielectrics are described. To evaluate the use of the memory TFTs in flexible applications, the influence of mechanical strain on the device performance is also explained in detail. Finally, chapter 7 shows the realization of flexible complementary logic circuits based on the integration of SWCNTs and metal oxide semiconductors (either IGZO or spray-coated In_2O_3).

1.5 Additional Publications

The following publications have been written in addition to those presented in this thesis:

- L. Petti, N. Münzenrieder, C. Vogt, H. Faber, L. Büthe, G. Cantarella, F. Bottacchi, T. D. Anthopoulos, and G. Tröster, Metal Oxide Semiconductor Thin-Film Transistors for Flexible Electronics. Accepted in *Applied Physics Review*, 2016.

- G. Cantarella, C. Vogt, N. Münzenrieder, G. A. Salvatore, L. Petti, A. Daus, L. Büthe, S. Knobelspies and G. Tröster. Tunable wrinkle formation of PDMS for stretchable IGZO TFTs. In *12th International Thin-Film Transistor Conference (ITC)*, [best poster award], 2016.

- A. Daus, N. Münzenrieder, L. Petti, S. Knobelspies, G. Cantarella, C. Vogt, L. Büthe, G. A. Salvatore and G. Tröster. Low-voltage flexible memory thin-film transistor based on charge generation from Fowler-Nordheim tunnel stress. In *12th International Thin-Film Transistor Conference (ITC)*, 2016.

- R. Shabanpour, C. Carta, K. Ishida, T. Meister, B. K. Boroujeni, N. Münzenrieder, L. Petti, G. A. Salvatore, G.Tröster and F. Ellinger. Baseband amplifiers in a-IGZO TFT technology for flexible audio systems. In *International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS)*, pages 357–361, 2015.

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- T. Meister, K. Ishida, R. Shabanpour, B. K. Boroujeni, C. Carta, F. Ellinger, N. Münzenrieder, L. Petti, G. A. Salvatore, G. Tröster, M. Wagner, P. Ghesquiere, S. Kiefl and M. Krebs. Bendable energy-harvesting module with organic photovoltaic, rechargeable battery and a-IGZO TFT charging electronics. In *European Conference on Circuit Theory and Design (ECCTD)*, pages 1–4, 2015.

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2

Thesis Summary

2.1 Contributions

In this section, the contributions of this work are summarized. In the first part, novel device structures and fabrication processes for flexible short-channel IGZO TFTs based on VTFT and QVTFT geometries, as well as on DLW-defined channels are described. In the second part, low-temperature and scalable spray pyrolysis is employed to realize flexible n-type In_2O_3 TFTs and unipolar circuits. Additionally, also inorganic CuSCN and organic SWCNT p-type solution-processable semiconductors are integrated into flexible TFTs and unipolar circuits. Finally, the application of flexible metal oxide semiconductor TFTs for non-volatile memories and complementary circuits is tackled. The majority of the data shown (VTFTs, QVTFTs, spray-coated In_2O_3 TFTs, memory TFTs, complementary circuits) is further presented in detail in the chapters 3 to 7. Other results (TFTs with DLW-defined channels, solution-deposited CuSCN TFTs) are based on unpublished data, while solution-processed SWCNT TFTs are further described in [101].

2.1.1 Flexible short-channel device structures

Realizing flexible metal oxide semiconductor TFTs with sub-500 nm feature sizes is difficult, due to the following reasons:

- Photolithography with glass masks and mask aligners combined with lift-off processes limit the minimum channel lengths achievable on flexible foils to ≈1 μm [75];
- The minimum feature sizes that can be obtained are also limited by the deformation that the flexible foils undergo during the manufacturing process: typically a 7.6 x 7.6 cm^2 large PI substrate expands of ≈25 μm during a standard 150 °C fabrication process [20]. Due to this deformation, tolerances of approximately 10 μm are necessary on the photolithographic masks, especially when aligning the gate contact to the source/drain electrodes [20];
- Self-aligned lithography (using back-side illumination through the flexible foil) allows overcoming the problem of thermal-induced substrate expansion and enables smaller total gate to source/drain overlaps of ≈3 μm [20]. Nevertheless, channel lengths ≤500 nm are not possible and long illumination times in the order of 30 min have to be utilized [20];

- For channel lengths $\lesssim$2 µm (defined by either conventional or self-aligned lithographic lift-off), the corresponding channel widths are also limited to $\lesssim$50 µm, due to the mechanical stability of the thin lift-off resist stripes utilized to define the channels.

In this work, flexible IGZO TFTs with sub-500 nm channel lengths have been fabricated by exploring alternative device structures. In particular, three different device geometries based on VTFT (chapter 3, page 85) and QVTFT (chapter 4, page 97) architectures, as well as on TG structures with DLW-defined channels are proposed. In particular for each of the three approaches, the device structure and fabrication process employed, together with the electrical performance and mechanical properties of the resulting devices are described.

2.1.1.1 Vertical IGZO TFTs

As described in chapter 3 (page 85), VTFT geometries represent an attractive alternative to planar devices especially when short channels are required. Main advantages of VTFTs include:

- a channel defined by the thickness of a device layer and not limited anymore by photolithographic constrains, allowing sub-500 nm channel lengths;
- large channel widths $\geq$50 µm even for short channel lengths $\leq$500 nm, leading to large W/L ratio and thus high TFT drain current;
- a $\approx$3x smaller device area compared to planar transistors, allowing higher device-packing densities [102].

In this thesis, vertical device structures have been explored, and flexible IGZO VTFTs with 500 nm channel lengths have been fabricated and characterized.

Device structure and fabrication: The VTFT geometry used to fabricated flexible IGZO TFTs with 500 nm channel length is shown in Fig. 2.1. The channel was formed on a multi-layer stack constituted by the source contacts, a dielectric spacing layer, and the drain electrodes. The manufacturing process of flexible IGZO VTFTs is described in

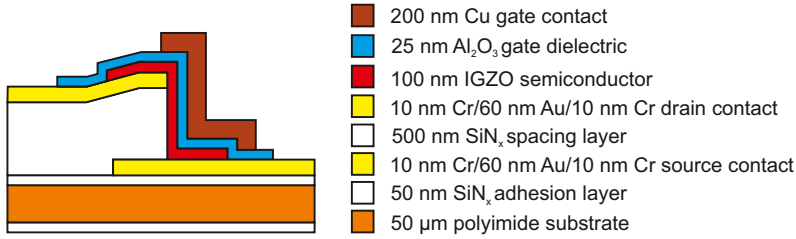

Figure 2.1: Schematic cross section of flexible IGZO vertical TFTs (VTFTs) with 500 nm channel length fabricated directly on a free-standing polyimide (PI) foil. More details are available in section 3.2 (page 87).

section 3.2 (page 87) and was optimized aiming at devices with high electrical performance, long-term reliability and stability, as well as good mechanical bendability. In particular, the following materials and fabrication steps were employed:

As a substrate a 50 µm-thick free-standing Kapton® E PI foil (surface area 3 x 3 cm^2) was utilized.

50 nm SiN_x layers were grown by PECVD (at 150 °C) on both sides of the PI foil to increase the adhesion between the substrate and the successive device layers, and at the same time to reduce the outgassing of the foil during the fabrication process.

As source contacts, a metallic multi-layer constituted by 10 nm Cr, 60 nm Au and 10 nm Cr deposited by e-beam evaporation was employed. Here, the multi-layer electrodes offer a compromise between good adhesion and high electrical conductivity, with Cr acting as an adhesion layer and Au providing a high conductivity. The Cr/Au/Cr multi-layer was structured using standard UV photolithography (photolithographic mask 1) and lift-off.

Since SiN_x offers a high breakdown voltage ≥500 V/µm and can be easily structured by reactive ion etching (RIE), SiN_x deposited by PECVD (at 150 °C) was used to realize the 500 nm-thick spacing layer.

The drain contacts were realized by 10 nm Cr/60 nm Au/10 nm Cr deposited by e-beam evaporation and structured by lift-off (mask 2). The drain electrodes were successively utilized as a hard mask to etch the 500 nm-thick SiN_x spacer by RIE, using a $CF4/O_2$ plasma.

100 nm amorphous IGZO (a-IGZO) were deposited using room-temperature RF magnetron sputtering from a ceramic $InGaZnO_4$ tar-

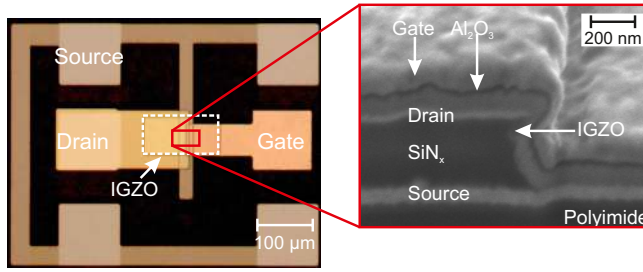

Figure 2.2: Optical micrograph of flexible IGZO VTFT with 500 nm channel length fabricated directly on a free-standing PI foil. The enlargement on the channel area displays the SEM image of a focused ion beam (FIB) cross section through the VTFT channel. More details are available in section 3.2 (page 87).

get. The thickness was optimized to ensure coverage across the vertical sidewall. The IGZO layer was patterned into islands by photolithography (mask 3) and wet etching in diluted hydrochloric acid.

As gate dielectric, 25 nm ALD-grown Al_2O_3 layers were utilized. Main advantages of Al_2O_3 are the conformability, the relatively high dielectric constant ($\epsilon_R \approx 9.5$), and the low pinhole density. The Al_2O_3 is grown at 150 °C, which is the highest temperature employed during the entire TFT fabrication process. Drain and source vias were opened by photolithography (mask 4) and wet etching [103]. In this case, the Al_2O_3 acts also as a passivation for the IGZO layer.

Since Cu provides a good ductility (thin film rupture strain $\epsilon_r \approx$ 4.5 %) [45], and can also be easily patterned by wet etching, the TG electrodes were formed by a 200 nm-thick Cu layer deposited by e-beam evaporation. The Cu thickness and the 30° substrate tilt used during the deposition ensured a wide coverage of the gate contact on top of the 500 nm-long vertical sidewall.

Fig. 2.2 displays an optical micrograph of the device, which uses a ground-signal-ground (GSG) layout to allow AC characterization. The flexible IGZO VTFT presented has a channel length L = 500 nm and a width W = 60 µm. The enlargement on the channel area in Fig. 2.2 shows the scanning electron microscopy (SEM) cross sectional image of the VTFT channel taken after focused ion beam (FIB) milling.

TFT electrical performance: Flexible IGZO VTFTs have been characterized according to their DC and AC performance (section 3.3, page 87), as well as their electrical stability (chapter 3.4, page 91).

DC performance: Fig. 2.3 shows the I_D-V_{GS} transfer and I_D-V_{DS} output characteristic of a flexible IGZO VTFT with 500 nm channel length, measured under ambient conditions. Based on these measurements, the following DC performance parameters were extracted using the Shichman-Hodges model [104]: an effective saturation field-effect mobility μ_{SAT} of 0.02 $cm^2V^{-1}s^{-1}$, a V_{TH} of 2.2 V, an I_{ON}/I_{OFF} of 2 x 10^7, a SS of 0.6 V/dec, and a g_m of 4.9 µS (at V_{GS} = V_{DS} = 5 V). The μ_{SAT} values obtained for flexible IGZO VTFTs are lower than the Hall mobility $\mu_H \approx 11.8\,cm^2V^{-1}s^{-1}$ of the deposited IGZO layers and the $\mu_{SAT} = 7.5\,cm^2V^{-1}s^{-1}$ of flexible planar IGZO TFTs with similarly short channel lengths [20]. This drop can be explained considering the effective mobility model of short-channel IGZO TFTs presented in [75]:

$$\mu_{FE} = \frac{\mu_H}{1 + \mu_H \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_{TH}) \cdot R_{C\{Lov\}}}, \tag{2.1}$$

where C_{ox} is the specific gate dielectric capacitance and R_C the contact resistance, which is a function of the total overlap length between gate and source/drain electrodes (L_{OV}) [75]. Based on this model, the degraded μ_{FE} can be attributed to the high R_C at the interface between source/drain and IGZO [75] (width-normalized contact resistance $r_C \approx 3\,k\Omega\,cm$), caused by oxidation and contamination of the Cr surface during the RIE etching. Optimization of the source/drain contacts (60x smaller r_C) leading to a larger μ_{SAT} (10x larger μ_{SAT}) in quasi-vertical TFT geometries is briefly presented in the next paragraph 2.1.1.2 (page 44), and more in detail in subsection 4.3.1 (page 101).

AC performance: C_G-V_{GS} measurements (Fig. 3.5, page 90) of flexible IGZO VTFTs (W/L = 60 µm/0.5 µm) highlight a large value of the gate capacitance (C_G/W = 163 $fF\mu m^{-1}$), which is attributed to the presence of a significant overlap between the gate and the source/drain ($L_{OV} \approx 13.7\,\mu m$), as well as between the gate and the IGZO island (≈57 µm), as shown in the top-view micrograph of Fig. 2.2. From

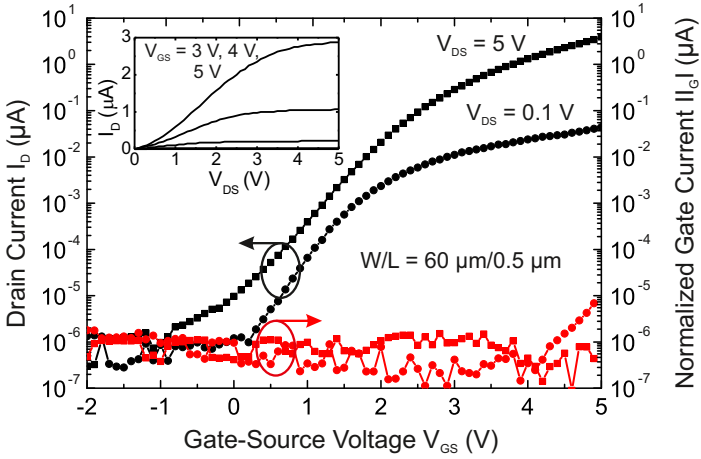

Figure 2.3: Transfer characteristic of flexible IGZO VTFT with 500 nm channel length and 60 μm channel width measured at a source-drain voltages V_{DS} of 0.1 V (linear regime) and 5 V (saturation regime). The inset displays the corresponding output characteristic. More details are available in section 3.3 (page 87).

the extracted capacitance (C_G/W = 163 fFμm^{-1}) and transconductance (g_m/W = 0.08 μSμm^{-1} at $V_{GS} = V_{DS}$ = 5 V) values, the transit frequency was estimated to be $f_T \approx$ 80 kHz. This frequency is lower than previously published values of 49 MHz for flexible IGZO BG TFTs (μ_{FE} = 14 $cm^2V^{-1}s^{-1}$, L = 1 μm, L_{OV} = 10 μm) [75] and 135 MHz for flexible self-aligned IGZO BG TFTs (μ_{FE} = 7.5 $cm^2V^{-1}s^{-1}$, L = 500 nm, L_{OV} = 3.1 μm) [20]. Such large difference in the achieved frequency, is attributed to the degraded μ_{FE} of vertical flexible IGZO VTFTs, as well as to the large overlap lengths. The next paragraph 2.1.1.2 (page 44) and more specifically chapter 4 (page 97) describe process and material optimizations that enabled a 60 fold reduction of R_C in flexible IGZO QVTFTs with even shorter channel, leading to an ≈19x higher f_T.

TFT mechanical properties: The mechanical properties of flexible IGZO VTFTs were investigated in section 3.5 (page 91), where issues like maximum strain resistance, influence of strain on the electrical performance, as well as resistance to mechanical fatigue are addressed.

Strain resistance and influence of strain: To characterize the maximum strain resistance and the influence of strain on the electrical performance of IGZO VTFTs, the device substrate was wound around cylindrical rods of 10, 6 and 5 mm bending radius (see Fig. 3.7a, page 92). In this way, tensile strain ϵ of 0.25 %, 0.4 %, and 0.5 % (calculated using equation 1.2 [87]) was induced parallel to the channel width. The VTFTs were functional while bent to radii of 5 mm and after re-flattening, whereas bending to smaller radii induced cracks perpendicular to the applied strain that permanently damaged the devices. The slightly reduced bendability of flexible IGZO VTFTs compared to planar IGZO TG TFTs made of similar device materials (but without spacer) [105] is attributed primarily to the brittle and thick SiN_x spacing layer. Bending the flexible IGZO VTFTs up to a tensile strain of 0.5 % results in a decreased μ_{SAT} (down to -2 % at ϵ = 0.5 %) and in a positive V_{TH} shift (up to +97 mV at ϵ = 0.5 %). Compared to previously published measurements on flexible planar IGZO TFTs (both BG and TG) [105, 106], the observed shifts correspond to compressive strain in the device channel. This is due to the Poisson effect, which induces compressive strain perpendicular to the externally applied strain, and thus parallel to the VTFT channel. Comparable results were also observed for IGZO QVTFTs (see subsection 4.3.2, page 103).

Resistance to mechanical fatigue: To evaluate long-term bendability of flexible IGZO VTFTs, a custom-built bending tester (see Fig. 3.10, page 94) was utilized. The VTFTs were characterized before and after 1000 cycles of repeated bending (ϵ = 0.25 %) and re-flattening, corresponding to ≈15 h of continuous bending. The VTFTs were functional after 1000 bending cycles, yielding a V_{TH} shift of ≈-460 mV and an almost constant μ_{SAT} (±0.3 %).

2.1.1.2 Quasi-vertical IGZO TFTs

In chapter 4 (page 97), the standard VTFT geometry based on a multilayer stack of source-spacer-drain (see paragraph 2.1.1.1 and chapter 3) is analyzed in detail and compared to alternative vertical device structures with the channel defined by the gate [107, 108] or the semiconductor [109] thickness. In particular, VTFTs with channels defined by the gate thickness are not considered a valid alternative to standard vertical geometries, due to their large gate to source/drain capacitance, which limits the TFT AC performance [107, 108]. At the same time, also

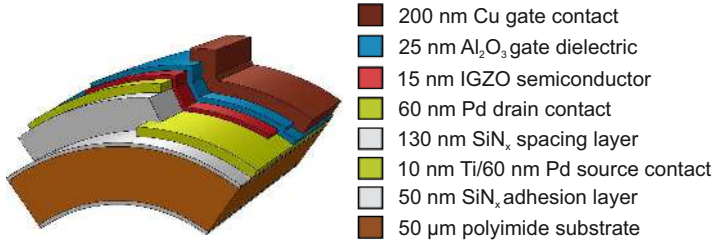

Figure 2.4: Schematic cross section of flexible IGZO quasi-vertical TFT (QVTFT) with 300 nm channel length fabricated directly on a free-standing PI foil. More details are available in section 4.2 (page 99).

VTFTs with the channel length defined by the semiconductor thickness are not a viable option, owing to their poor electrostatic control over the channel [109]. Nevertheless, the dry etching process typically utilized to fabricate the vertical sidewalls of standard VTFTs results in under-cut profiles and contaminated source/drain contacts, leading to degraded TFT performance [110, 111, 52]. Even if contact contamination in VTFTs can be overcome by defining the vertical profile by means of wet etching [52], the under-cut profile is still present. To overcome these limitations, chapter 4 (page 97) explores a novel fabrication process of the source/spacer/drain stack of standard VTFTs based on a bi-layer lift-off of the spacing layer and the drain contacts on top of the source electrode. This results in the reliable formation of a tilted vertical sidewall, which ensures also a conformable deposition of the successive device layers. Compared to the previously described IGZO VTFTs (chapter 3, page 85), the resulting flexible IGZO QVTFTs present an even shorter channel length of 300 nm, as well as a reduced contact resistance (≈60x lower), which results in an enhanced DC and AC performance (approximately a 10x larger μ_{FE} and a 19x higher f_T).

Device structure and fabrication: Section 4.2 (page 99) describes in detail the fabrication process of flexible IGZO QVTFTs with 300 nm channel length (Fig. 2.4). Compared to the previously described fabrication process of flexible IGZO VTFTs (see paragraph 2.1.1.1 and section 3.2), there are four main differences:

- The source and drain contacts are constituted by 10 nm Ti/60 nm Pd and 60 nm Pd, respectively. Pd was chosen as opposed to Au,

mainly due to its good adhesion to other materials. By employing Pd, it is indeed possible to avoid additional Cr [111] or Ti [105] layers, which are typically more prone to oxidation in ambient air [111]. Furthermore, Pd is expected to form an ohmic contact with IGZO sputtered in a pure Ar plasma [112] (as in our case).

- In this case, the SiN_x spacer is not anymore structured by dry etching, but rather by a bi-layer lift-off process. After the e-beam evaporation and lift-off of the Ti/Pd source contacts, a bi-layer resist made of 4.1 μm LOR-5B and 2 μm SU-8 was spin-coated and structured into drain electrodes by standard UV photolithography. Deposition and structuring of the bi-layer were optimized to achieve an under-cut between the SU-8 and the LOR-5B (≈4.1 μm). During the subsequent deposition of the 130 nm-thick SiN_x spacer (PECVD) and Pd drain electrodes (e-beam evaporation), the suspended SU-8 layer collapsed on the substrate in the under-cut area and SiN_x/Pd were uniformly deposited around the SU-8. The successive controlled rupture of the thin SiN_x layer during lift-off yielded a tilted sidewall with a length of 300 nm and a perfectly aligned Pd drain contact.

- As already anticipated, compared to flexible IGZO VTFTs (Fig. 2.1), a ≈3.85x thinner SiN_x spacing layer was employed. Thicker spacing layers ≥130 nm cannot be utilized in this process, due to resulting non-uniform rupture of the SiN_x layer during lift-off. Thinner SiN_x films down to 95 nm can be utilized, at a cost of higher off currents (flowing between source and drain electrodes). Furthermore, the PECVD process temperature was reduced from 150 °C to 120 °C, to avoid any damage to the underlying LOR-5B and SU-8 resist layers.

- Thanks to the quasi-vertical sidewall, a standard IGZO thickness of 15 nm (typically used in flexible TFTs [20]) could be employed, while still ensuring a conformal coverage over the vertical stack.

Fig. 2.5 shows an optical micrograph of the QVTFT, which employes a GSG layout to allow AC measurements. The flexible IGZO QVTFT presented has a channel length L = 300 nm and a width W = 55 μm. The enlargement on the channel area displays the SEM image of the QVTFT channel taken after forming a hole with FIB milling. The

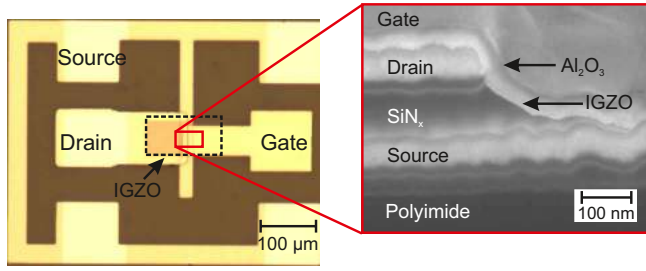

Figure 2.5: Optical micrograph of flexible IGZO QVTFT with 300 nm channel length fabricated directly on a free-standing PI foil. The enlargement on the channel area displays the SEM image of a FIB cross section through the QVTFT channel. More details are available in section 4.2 (page 99).

image shows how the quasi-vertical profile ensures a good coverage of the IGZO, Al_2O_3 and Cu device layers.

TFT electrical performance: The DC and AC performance of flexible IGZO QVTFTs has been characterized in subsection 4.3.1 (page 101).

DC performance: Flexible IGZO QVTFTs with 300 nm channel length yield the following DC performance parameters: a μ_{SAT} of $0.2\,cm^2V^{-1}s^{-1}$, a V_{TH} of 1.5 V, an I_{ON}/I_{OFF} of 10^4, a SS of 0.4 V/dec, and a g_m of 40 µS ($V_{GS} = 5$ V, $V_{DS} = 5$ V). Even if flexible IGZO QVTFTs exhibit a 10x larger μ_{SAT} if compared to IGZO VTFTs, the μ_{SAT} values obtained are still lower than the Hall mobility $\mu_H \approx 11.8\,cm^2V^{-1}s^{-1}$ of the deposited IGZO layers. Such degraded μ_{FE} was attributed to the still high contact resistance ($r_C \approx 45\,\Omega$ cm), expected to be originated from process-induced surface contamination of the Pd contacts. Anyway, due to the ≈60x reduced contact resistance, compared to VTFTs flexible IGZO QVTFTs present a 9x larger $g_m/W = 0.73\,\mu S\mu m^{-1}$. Furthermore, compared to planar devices, QVTFTs enable higher drain currents densities. In particular, if fabricated with tolerances resulting in a total yield significantly above 90 %, the channel area of a planar IGZO TFT is able to switch a current of ≈1 mA over an area of ≈40 000 μm^2. If an IGZO QVTFT is used, the effective area can be reduced to ≈4000 μm^2. The obtained on/off current ratio of 10^4 is sig-

nificantly lower compared to flexible vertical [111] and planar IGZO TFTs [20]. This is due to the large I_{OFF} (2 nA) caused by leakage between source and drain contacts through the low-temperature deposited SiN_x spacer. Smaller I_{OFF} and larger I_{ON}/I_{OFF} can be achieved by reducing the source/drain overlap.

AC performance: The flexible IGZO QVTFT exhibits a width-normalized gate capacitance of 76 $fF\mu m^{-1}$, which is dominated by the capacitance of the still large overlap between gate and source/drain (17.8 µm), and between gate and IGZO (74 µm). From the extracted C_G and g_m values, an f_T of 1.52 MHz was calculated. A more precise value of the f_T = 1.5 MHz was derived measuring the S-parameters and extracting the frequency-dependent current gain h_{21} (see Fig. 2.6). Due to the improved transconductance and gate capacitance, flexible QVTFTs exhibit a 19x enhanced f_T if compared to flexible IGZO VTFTs.

TFT mechanical properties: The mechanical properties of flexible IGZO QVTFTs were investigated in subsection 4.3.2 (page 103). Flexible IGZO QVTFTs were shown to be operational while bent down to a tensile radius of 5 mm (tensile strain ϵ = 0.48 % parallel to the channel width calculated using equation 1.2 [87]), and after re-flattening. Tensile bending results only in small variations of the device performance (μ_{SAT} changes by -5 % and V_{TH} by +126 mV). These values are in line with the previously presented strain-induced shifts of IGZO VTFTs (section 3.5, page 91). Bending to smaller radii below 5 mm was not possible, due to delamination of the Cu TG contacts.

2.1.1.3 Top-gate IGZO TFTs

As explained in the previous paragraphs 2.1.1.1 and 2.1.1.2, vertically integrated device structures allow achieving short channel lengths down to 300 nm. Nevertheless, process-induced source/drain contact contamination results in large R_C values, which degrade both the DC and the AC TFT performance. In general, also in planar IGZO TFTs, when the channel length is reduced below ≈1 µm, the channel resistance becomes smaller than the contact resistance, which results in a drop of the μ_{FE} (see equation 2.1 [75]). Nevertheless, the degradation of the μ_{FE} encountered in flexible planar IGZO TFTs is not as pronounced as in vertically integrated devices: the minimum μ_{FE} reported for flexible planar IGZO TFTs is of 5 $cm^2V^{-1}s^{-1}$ for a device

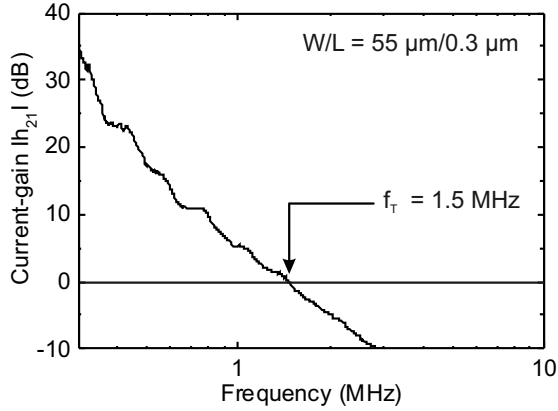

Figure 2.6: Absolute value of the small-signal current gain h_{21} extracted from S-parameters measurements of a flexible IGZO QVTFT with 300 nm channel length ($V_{GS} = V_{DS} = 5$ V). More details are available in subsection 4.3.1 (page 101).

with a channel length of 500 nm [75]. Furthermore, as visible in equation 1.1. and 2.1, the overlap length between the gate contact and the source/drain electrodes (L_{OV}) is another key parameter in determining the f_T, as it influences both R_C and C_G [75]. Compared to planar TFTs, in vertical devices the optimization of the L_{OV} is further complicated by the VTFT structure with source and drain deposited, structured and aligned in separated process steps. For these reasons, it is important to explore alternative fabrication processes enabling short channel lengths also in flexible planar TFTs. To this regard, two-photon DLW [113] has been proposed as an attractive tool for the fabrication of three-dimensional (3D) microstructures for various application fields, ranging from optical interconnects [114], photonics [115], micro-fluidics [116], to cell scaffolds and biomimetics [117]. Recently, also conductive 3D Au-based microstructures have been realized by two-photon DLW [118]. Strangely, two-photon DLW has not yet been employed to fabricate short-channel TFTs. In this work, we explore the use of DLW for the realization of flexible IGZO TG TFTs with 280 nm channel lengths.

Device structure and fabrication: Fig. 2.7 shows the manufacturing process of IGZO TFTs fabricated on a free-standing 50 µm-thick PI foil

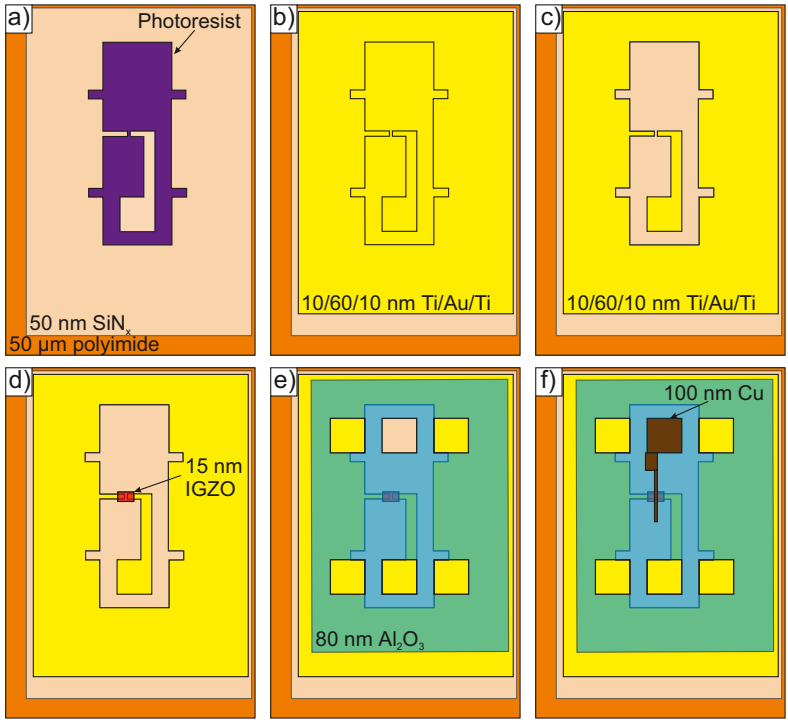

Figure 2.7: Manufacturing process flow of flexible IGZO top-gate bottom-contact (TG-BC) TFT with channel length defined via two-photon direct laser writing (DLW): a) DLW illumination and development of photoresist, b) e-beam evaporation of Ti/Au/Ti source and drain contacts, c) channel structuring by lift-off, d) RF magnetron sputtering and wet etching of IGZO semiconductor, e) ALD deposition and wet etching of Al_2O_3 gate dielectric, f) e-beam evaporation and wet etching of Cu TG electrode. The fabrication process is based on unpublished results obtained during this thesis.

(area 2.5 x 2.5 cm^2). The devices are based on a top-gate bottom-contact (TG-BC) TFT structure:

First, a 50 nm SiN_x was deposited by PECVD on both sides of the substrate, to increase the adhesion to the following device layers.

Next, to allow the structuring of the TFT channels by DLW photolithography, the PI substrate was attached to a glass carrier and

subsequently coated with a drop-casted IP-Dip photoresist. IP-Dip is a negative photoresist, which behaves similarly to SU-8 and other acrylate-based negative photoresists [119]. In particular, IP-Dip is specifically suited for two-photon DLW photolithography [120], allowing minimum line widths of 150 nm [119]. For the DLW process, the photonic professional system from NanoScribe GmbH was utilized[1]. NanoScribe is the first commercial DLW system based on two-photon polymerization with ultra-short laser pulses [121]. Differently to other conventional additive manufacturing technologies, in the NanoScribe process the microstructures are written following 3D paths connected from the beginning to the end of the writing process [119]. Therefore, an optimized computer-aided design (CAD) of the desired channel structures was generated and converted to a suitable writing scheme, including 3D writing paths that do not overlap with each other (to avoid writing through already exposed photoresist areas [119]). The channel structures displayed in Fig. 2.7a were patterned into the IP-Dip photoresist by directly exposing the photoresist –using the so-called dip-in-lithography (DILL) configuration [120]– with an optimized laser power of 4.6 μW. Afterward, the PI foil was detached from the glass carrier and the photoresist was developed, leading to channel structures with lengths down to 280 nm patterned in the IP-Dip photoresist (Fig. 2.7a).

Following the two-photon DLW photolithography, 10 nm/60 nm/ 10 nm Ti/Au/Ti were e-beam evaporated on the substrate (Fig. 2.7b). A lift-off process was performed to remove the IP-Dip photoresist and define the channel areas and the source and drain contacts (Fig. 2.7c).

Subsequently, a 15 nm-thick IGZO film was RF magnetron sputtered (at room temperature) and structured into 19 x 20 μm^2 semiconductor islands by wet etching (Fig. 2.7d). Then, an 80 nm-thick Al_2O_3 film was grown by ALD and wet etched to open source/drain contact holes (Fig. 2.7e). In this case, the 80 nm-thick Al_2O_3 dielectrics represents a trade-off between high μ_{FE} (see μ_{FE} dependance with C_{ox} in equation 2.1) and low-voltage operation.

Finally, 100 nm of Cu were e-beam evaporated and patterned in gate contacts using wet etching (Fig. 2.7f).

Fig. 2.8 displays an optical micrograph of the device, which uses a GSG layout to allow AC characterization. The inset in Fig. 2.8 shows enlargements of the TFT channel taken by optical microscopy and SEM.

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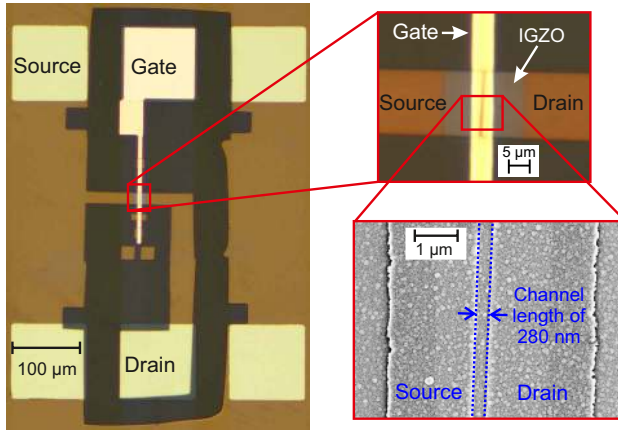

Figure 2.8: Optical micrograph of a flexible IGZO TG-BC TFT with 280 nm channel length defined via DLW fabricated directly on a free-standing PI foil. The enlargements display both an optical micrograph and an SEM image of the channel area. The images are based on unpublished results obtained during this thesis.

The flexible IGZO TFT presented has a channel length L = 280 nm and a width W = 17 µm. On each 2.5 x 2.5 cm^2 PI foil, up to 9 different GSG devices with diverse channel lengths and widths can be realized with the presented manufacturing process (Fig. 2.7). A larger number of TFTs can hardly be accomplished within this process, due to long DLW processes up to 5 hours, as well as complicated alignment of the NanoScribe laser over larger areas (above 2 x 2 mm^2). Nevertheless, standard IGZO TG TFTs with channels lengths ≥1 µm could be realized on the same substrate by utilizing Cr/Au/Cr source/drain contacts and integrating an additional UV photolithographic and wet etching step after the lift-off process of the channel structures (Fig. 2.7c).

TFT electrical performance: The DC and AC performance of flexible IGZO TFTs with channels defined via DLW has been characterized.

DC performance: Fig. 2.9 shows the I_D-V_{GS} transfer and I_D-V_{DS} output characteristic of a flexible IGZO TFT with 280 nm channel length, measured under ambient conditions. Based on these measure-

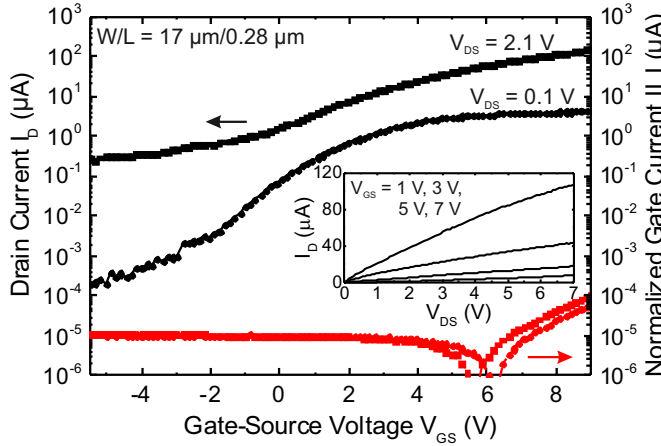

Figure 2.9: Transfer characteristic of flexible IGZO TG-BC TFT with 280 nm channel length defined via DLW (channel width W = 17 µm) measured at a V_{DS} of 0.1 V and 2.1 V. The inset displays the corresponding output characteristic. The data is based on unpublished results obtained during this thesis.

ments, the following DC performance parameters were extracted: a μ_{SAT} of 1.1 $cm^2V^{-1}s^{-1}$, a V_{TH} of 3 V, an I_{ON}/I_{OFF} of 10^3, a SS of 2 V/dec, and a g_m = 250 µS (V_{GS} = 9 V, V_{DS} = 5.1 V). As expected, flexible planar short-channel IGZO TFTs exhibit significantly larger μ_{SAT} if compared to flexible IGZO QVTFTs with similarly short channel lengths. This is mainly due to approximately halved contact resistance (r_C = 22 Ω cm) that planar IGZO TFTs (L = 280 nm) yield compared to IGZO QVTFTs (L = 300 nm). The extracted r_C is indeed only slightly higher than state-of-the-art values of 12.5 Ω cm obtained for flexible self-aligned IGZO BG TFTs (L = 500 nm) [20, 75]. The larger r_C can be attributed to the ≈2x lower average μ_{FE} of IGZO TG TFTs if compared to BG devices made of the same material stack [105]. This, combined with a channel length of 280 nm explains the achieved μ_{SAT} value of 1.1 $cm^2V^{-1}s^{-1}$. As shown in Fig. 2.9, I_{OFF} always exceeds 100 pA, and further increases for increasing V_{DS} (up to I_{OFF} = 1 µA at V_{DS} = 5.1 V). Such large off current (leading to small I_{ON}/I_{OFF}) is due to the still large IGZO semiconductor islands (19 x 20 $µm^2$), which provide an additional current path between source and drain contacts.

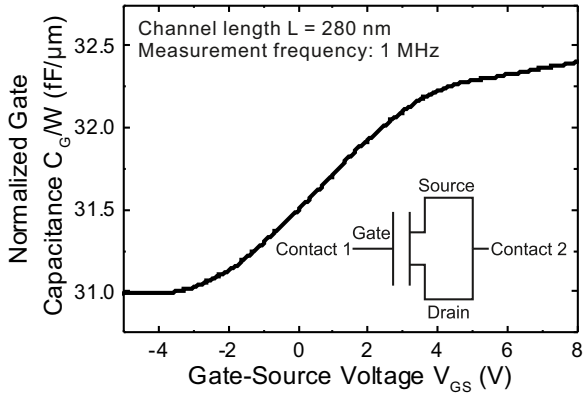

Figure 2.10: Gate capacitance of flexible IGZO TG-BC TFT with 280 nm channel length defined via DLW, measured with source/drain contacts grounded. The measurement was performed at a frequency of 1 MHz. The inset displays the corresponding measurement setup. The data is based on unpublished results obtained during this thesis.

AC performance: From C-V measurements (Fig. 2.10), a gate capacitance of 32.47 fFμm^{-1} was extracted. Such low C_G value has been obtained despite the 80 nm-thick Al_2O_3 dielectric, mainly due to the short channel length of 280 nm, combined with a small total overlap between gate and source/drain (L_{OV} = 5.2 µm). From the h_{21} plot (Fig. 2.11), an f_T of 80 MHz was derived. The measured f_T nicely agrees with the value of 81 MHz estimated from g_m and C_G data. Compared to IGZO QVTFTs (L = 300 nm), flexible IGZO TFTs with DLW-defined channels yield an ≈53x higher f_T. Even if the obtained frequency is lower than the f_T = 135 MHz reported for flexible self-aligned IGZO TFTs (L = 500 nm) [20], future optimization of the source/drain contacts, combined with shorter channel lengths promises to enable transit frequencies above 135 MHz. Already based on these preliminary results, DLW photolithography offers a viable and promising route for the realization of flexible short-channel and high-frequency devices.

TFT mechanical properties: Flexible IGZO TFTs with 280 nm channel lengths were demonstrated to be operational while bent to a tensile radius of 10 mm (ϵ = 0.2 % calculated using equation 1.2 [87]), showing

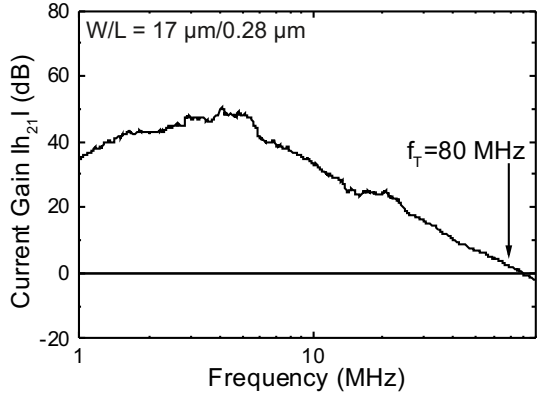

Figure 2.11: Absolute value of h_{21} extracted from S-parameters measurements of a flexible IGZO TG-BC TFT with 280 nm channel length defined via DLW (V_{GS} = 8.5 V and V_{DS} = 9 V). The data is based on unpublished results obtained during this thesis.

small variations in the performance parameters (μ_{SAT} changes by -4 % and V_{TH} by +130 mV). These changes can be explained by the under tensile increased resistance of the metallic contacts, which becomes dominant for small channel resistances [122]. Bending to smaller radii leads to the formation of cracks in the extended Ti/Au/Ti metallic surface, which cause permanent parameter shifts at 6 mm radii and device failure at radii ≤5 mm.

2.1.2 Solution-processed materials and processes

The possibility to replace standard vacuum-processing techniques with higher throughput continuous processes is especially attractive in view of novel large-area and cost-effective applications, such as foldable and printable displays, disposable smart labels and intelligent packaging [74]. To this aim, solution processing methods of both n- and p-type semiconductors are attracting an increasing interest [74].

In this work, In_2O_3 films were deposited by spray pyrolysis at process temperature ≤250 °C and incorporated into rigid and flexible n-type TFTs and circuits (chapter 5, page 105). Additionally, p-type

inorganic CuSCN and organic SWCNTs were grown by spin-coating at low temperatures and integrated into flexible TFTs and circuits.

2.1.2.1 In_2O_3 TFTs and circuits

Among solution-processable metal oxide semiconductors, In_2O_3 is especially attractive since it can be grown employing a diverse range of processes like ink-jet printing [123], spray pyrolysis [124], and spin-casting [125, 51, 126, 127, 128]. Employing neat In_2O_3 layers spin-casted and annealed at temperatures $\leq$250 °C, flexible devices with μ_{FE} ranging from 1.5 $cm^2V^{-1}s^{-1}$ to 4 $cm^2V^{-1}s^{-1}$ have been shown [63, 51]. Recently, the Centre for Plastic Electronics and Department of Physics at Imperial College has demonstrated optimized precursor material formulations and processing protocols, allowing the spray deposition of In_2O_3 at 250 °C [73]. The so-formed electron conducting In_2O_3 active layers have also been incorporated in rigid TFTs [73].

In this thesis, In_2O_3 films have been spray-deposited at 250 °C and incorporated into TFTs and logic circuits (section 5.2, page 108). The resulting TFTs and circuits have then been characterized (section 5.3, page 108). The results shown have been obtained in a collaboration between Imperial College London (Centre for Plastic Electronics and Department of Physics), ETH Zurich, and Aristotle University of Thessaloniki (Laboratory of Applied Physics).

Device structure and fabrication: Fig. 2.12a displays the device structure and fabrication process employed to realize bottom-gate bottom-contact (BG-BC) In_2O_3 TFTs on a free-standing 50 μm-thick PI foil (surface area 7.6 x 7.6 cm^2):

First, a 50 nm-thick SiN_x layer was deposited by PECVD on both sides of the flexible foil.

Next, 30 nm of Cr were e-beam evaporated and structured into gate contacts using standard UV photolithography and wet etching.

Following, a 50 nm-thick Al_2O_3 gate dielectric was deposited by ALD at 150 °C. Gate contact holes through the Al_2O_3 were patterned by standard UV photolithography and wet etching.

Subsequently, 10 nm/50 nm of Ti/Au were e-beam evaporated and patterned into source/drain contacts using a lift-off process.

Prior to the active layer deposition, the substrate was diced into 1.5 x 1.5 cm^2-large chips to allow multiple depositions with different pro-

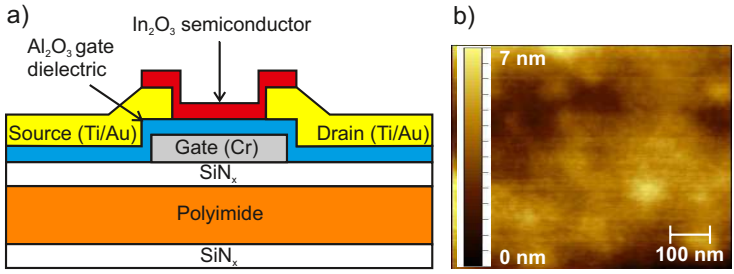

Figure 2.12: a) Schematic device cross section of flexible BG bottom-contact (BG-BC) TFT based on spray-deposited In_2O_3 fabricated on a free-standing PI foil. b) Atomic force microscopy (AFM) surface topography image of In_2O_3 film processed on $Si/SiO_2/SiN_x/Cr/Al_2O_3$ surface. More details are available in section 5.2 (page 108).

cess protocols. The diced chips were then cleaned by ultra-sonication in acetone and isopropanol for 5 min, and subjected to 30 min UV/ozone treatment. The deposition was carried out using ultrasonic spray pyrolysis and an In_2O_3 solution constituted by 30 mg/mL indium nitrate hydrate ($In(NO_3)_3{\cdot}H_2O$) dissolved in deionized water. The deposition was performed in ambient air at 250 °C. During spray pyrolysis, the flexible chip was mechanically clamped on the border with a heavy stencil mask (mass of ~30g). The resulting ~15 nm-thick In_2O_3 active layer was left unstructured and unpassivated.

Employing the same BG-BC device structure and fabrication process, rigid In_2O_3 TFTs were also realized on a 4-in. Si substrate with 1 μm thermally grown SiO_2 acting as isolation layer (Fig. 5.1a, page 109). Additionally, also bottom-gate top-contact (BG-TC) In_2O_3 TFTs were fabricated onto a p-type doped Si wafer acting as common gate electrode with 400 nm-thick SiO_2 films as gate dielectric (Fig. 5.1b, page 109). In this case, the In_2O_3 active layer was processed using the previously described protocols followed by the thermal evaporation (with shadow mask) of top Al source/drain electrodes in high vacuum (10^{-6} mbar). The channel dimensions of the resulting In_2O_3 devices are: W/L of 1400 μm/20 μm, 500 μm/10 μm and 1000 μm/50 μm for flexible BG-BC, rigid BG-BC and rigid BG-TC TFTs, respectively.

Fig. 2.12b shows the atomic force microscopy (AFM) image of the

surface topography of a ~15 nm-thick In_2O_3 film deposited by spray pyrolysis. The film appears continuous and smooth with a surface roughness of ~1.1 nm. X-ray diffraction (XRD) measurements in Bragg-Brentano geometry of the spray-deposited In_2O_3 layers (Fig. 5.1d, page 109) reveal a polycrystalline structure.

TFT electrical performance: The DC performance of flexible BG-BC, rigid BG-BC and rigid BG-TC TFTs has been characterized in section 5.3 (page 108). Fig. 2.13 shows the I_D-V_{GS} transfer and I_D-V_{DS} output characteristic of a flexible BG-BC In_2O_3 TFT, measured in nitrogen. Based on these measurements, the following DC performance parameters were extracted: a μ_{SAT} of 0.2 $cm^2V^{-1}s^{-1}$, a V_{TH} of 5.29 V, an I_{ON}/I_{OFF} of 6 x 10^3, and a SS of 0.9 V/dec. The gate leakage current I_G is always below 20 nA. The large I_{OFF} ≤10 nA is attributed to the unpatterned semiconductor. Compared to flexible In_2O_3 TFTs, rigid BG-BC and BG-TC devices yield a higher μ_{SAT} of 1.25 $cm^2V^{-1}s^{-1}$ and 16 $cm^2V^{-1}s^{-1}$, respectively, as well as larger I_{ON}/I_{OFF} >10^4. The better performance of BG-BC devices on rigid substrates, compared to TFTs on flexible foils, is most likely attributed to the comparatively lower thermal conductivity of PI that hinders the precursor conversion during the spraying process, as well as to the increased dielectric/semiconductor interface roughness. The even higher μ_{FE} of rigid BG-TC devices, compared to BG-BC TFTs, can be explained by the different TFT structure combined with low work function Al S/D electrodes.

TFT mechanical properties: The mechanical properties of flexible In_2O_3 devices were investigated in subsection 5.3.4 (page 112). Flexible In_2O_3 TFTs were shown to be operational while bent down to a tensile radius of 4 mm (ϵ = 0.65 % parallel to the TFT channel calculated using equation 1.2 [87]), and after re-flattening. Tensile bending results in an increase of μ_{SAT} by 13 % and a shift of V_{TH} by -230 mV. These values are in good agreement with previously reported strain-induced shifts of IGZO and IZO devices [106, 129], and can be explained by the enhanced conductivity of In_2O_3 films induced under tensile strain. Bending to smaller radii leads to the formation of cracks in the brittle Cr gate that permanently harm the device operation.

Circuits: To exploit the potential of spray-deposited In_2O_3 TFTs, logic circuits were explored (see subsection 5.3.3, page 110). Unipo-

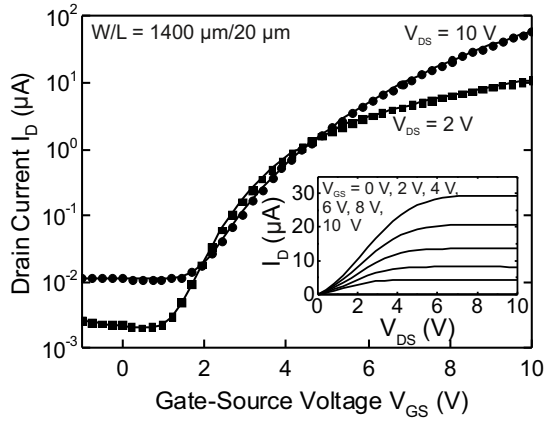

Figure 2.13: Transfer characteristic of flexible BG-BC TFT based on spray-deposited In_2O_3 (W/L = 1400 µm/20 µm) measured at a V_{DS} of 2 V (linear regime) and 10 V (saturation regime) in nitrogen atmosphere. The inset displays the corresponding output characteristic. More details are available in section 5.3 (page 108).

lar In_2O_3 inverters comprising one driving In_2O_3 BG-BC TFT (W/L = 1400 µm/20 µm) and one passive load (metal thin-film resistor with R = 160 kΩ) were fabricated on both rigid and flexible substrates. The circuit schematic is displayed in the inset of Fig. 2.20 (page 68). Compared to the TFT manufacturing process, the circuit fabrication does not require additional steps, since the interconnections were integrated into the Ti/Au source/drain metallization layer and the resistor was implemented using the Cr gate metal. Rigid unipolar inverters (Fig. 5.3, page 113) exhibit a gain G = 5.3 V/V and an almost centered midpoint voltage V_M = 5.8 V (when the input voltage V_{IN} is swept from 0 V to 10 V at a supply voltage V_{DD} = 10 V). Flexible inverters yield a comparatively lower gain of 1.2 V/V, which is attributed to the worse performance of flexible In_2O_3 TFTs (compared to rigid devices). Higher gains ≥22 V/V can be realized by complementing n-type In_2O_3 with p-type SWCNT TFTs, as presented later and in chapter 7 (page 135).

2.1.2.2 CuSCN TFTs and circuits

To date, it is difficult to realize p-type metal oxide semiconductors, especially at low process temperatures. This is why, only few reports on flexible p-type metal oxide semiconductor TFTs are available [34, 67, 84, 130, 68, 99, 85]. Among these, there is no report on solution-processed p-type metal oxide semiconductors. CuSCN –an inorganic metal pseudohalide compound– is an attractive p-type semiconductor, owing to its hole transporting characteristics and solution-processability at 80 °C [69]. Recently, the Centre for Plastic Electronics and Department of Physics at Imperial College London has demonstrated rigid TFTs based on CuSCN spin-casted at 80 °C (μ_{FE} close to 0.5 $cm^2V^{-1}s^{-1}$) [69].

In this thesis, CuSCN films spin-casted at 80 °C have been incorporated into flexible TFTs and circuits. The electrical and mechanical performance of the resulting devices has been characterized. The results shown have been obtained in a collaboration between Imperial College London (Centre for Plastic Electronics and Department of Physics), ETH Zurich, and the Hong Kong Polytechnic University (Department of Applied Physics and Materials Research Center).

Device structure and fabrication: Fig. 2.14a displays the device structure and fabrication process employed to realize CuSCN TG-BC TFTs on a free-standing 50 μm-thick PI foil (surface area 1.5 x 1.5 cm^2):

First, a 50 nm-thick SiN_x layer was deposited by PECVD on both sides of the flexible foil.

Next, 50 nm of Au were deposited by thermal evaporation in high vacuum (10^{-6} mbar) and structured into source and drain contacts using shadow masking.

The active layer solution was prepared by dissolving the CuSCN precursor (Aldrich) in dipropyl sulfide (Merck, 99 %) at a concentration of 20 mg/mL. Undissolved material was removed by stirring, centrifugating, and filtering the CuSCN solution at room temperature. The resulting solution was then spin-casted (800 rpm for 60 s at room temperature) and annealed at 80 °C in nitrogen. The resulting 15 nm-thick CuSCN film was left unstructured.

As gate dielectric, poly(vinylidene fluoride-trifluoroethylene-chlorofluoroethylene) [P(VDF-TrFE-CFE)] layers were utilized. P(VDF-TrFE-CFE) is a high-k relaxor ferroelectric polymeric dielectric (ϵ_R up

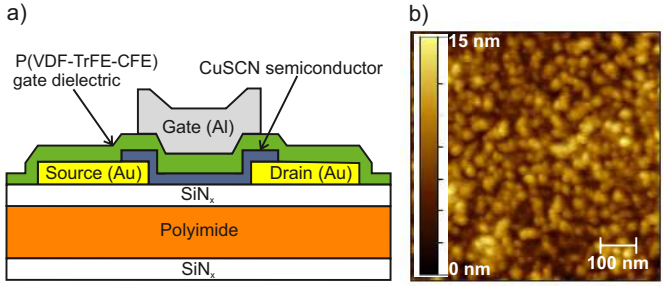

Figure 2.14: a) Schematic device cross section of flexible TG-BC TFT based on spin-casted CuSCN fabricated on a free-standing PI foil. b) AFM surface topography image of CuSCN film processed on a $Si/SiO_2/SiN_x/Cr/Al_2O_3$ surface. The fabrication process and AFM image are based on unpublished results obtained during this thesis.

to ≈60), which can be solution-processed at low temperatures [69, 131]. The gate dielectric solution (6/36.5/7.5 mol%) was first synthesized and then dissolved in methyl-ethyl-ketone (MEK). As spin-coated P(VDF-TrFE-CFE) films were annealed at 60 °C for 3 h. The resulting 160 nm-thick P(VDF-TrFE-CFE) gate dielectric was left unpatterned.

Finally, 60 nm of Al were deposited by thermal evaporation in high vacuum and patterned into gate electrodes using shadow masking.

Additionally, also flexible BG-BC CuSCN TFTs were realized, employing the device architecture shown in Fig. 2.12a (page 57) with CuSCN active layers and 25 nm Al_2O_3 gate dielectrics. The channel dimensions of the resulting CuSCN devices are: W/L of 1400 µm/20 µm and 1500 µm/40 µm for flexible BG-BC and TG-BC TFTs, respectively.

Fig. 2.14b shows the AFM image of the surface topography of a ~15 nm-thick CuSCN film deposited by spin-casting. The film appears homogeneous and smooth with a surface roughness of ~1.5 nm.

TFT electrical performance: The I_D-V_{GS} transfer and I_D-V_{DS} output characteristics of flexible CuSCN BG-BC devices measured in nitrogen atmosphere are shown in Fig. 2.15. Based on these measurements, the following DC performance parameters were extracted: a μ_{SAT} of $0.0013\,cm^2V^{-1}s^{-1}$, a V_{TH} of -1 V, an I_{ON}/I_{OFF} of 5 x 10^2, and a SS of

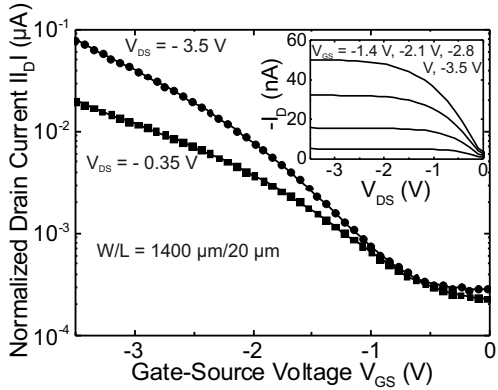

Figure 2.15: Transfer characteristic of flexible BG-BC TFT based on spin-casted CuSCN (W/L = 1400 μm/20 μm) measured at a V_{DS} of -0.35 V (linear regime) and -3.5 V (saturation regime) in nitrogen atmosphere. The inset displays the corresponding output characteristic. The data is based on unpublished results obtained during this thesis.

1.7 V/dec. I_G is always below 10 nA. When measured with a double sweep of V_{GS}, the CuSCN TFTs present a counter-clockwise hysteresis <250 mV, which is attributed to the presence of traps at the interface CuSCN/Al_2O_3. If measured in ambient atmosphere, flexible CuSCN BG-BC TFTs yield a lower μ_{SAT} of 0.0007 $cm^2V^{-1}s^{-1}$ and a negatively shifted V_{TH} of -1.2 V. TG-BC TFTs (Fig. 2.16) yield a μ_{SAT} of 0.0012 $cm^2V^{-1}s^{-1}$, a V_{TH} of -3.13 V, and I_{ON}/I_{OFF} of 2 x 10^3. Compared to BG-BC devices with Al_2O_3 gate dielectrics, TG-BC TFTs present a significantly reduced hysteresis <25 mV, which is explained by the improved interface between CuSCN and P(VDF-TrFE-CFE) in the TG-BC structure [69]. Compared to the average μ_{SAT} of 0.01-0.1 $cm^2V^{-1}s^{-1}$ of rigid CuSCN TFTs [69], the obtained μ_{FE} is lower. Such degraded value is most likely attributed to the worse thermal conductivity of PI foils that prevents the precursor conversion, as well as to the increased dielectric/semiconductor interface roughness.

TFT mechanical properties: Flexible CuSCN TFTs (both BG-BC and TG-BC) were demonstrated to be operational while bent down to tensile radii of 4 mm (ϵ = 0.58 % calculated using equation 1.2 [87]).

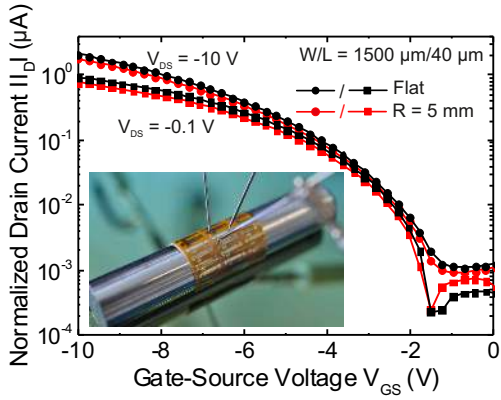

Figure 2.16: Transfer characteristic of flexible TG-BC TFT based on spin-casted CuSCN (W/L = 1500 µm/40 µm) measured at a V_{DS} of -0.1 V (linear regime) and -10 V (saturation regime), while flat and bent to a tensile radius of 4 mm. The inset displays a photograph of the actual flexible CuSCN TFT bent to a tensile radius of 4 mm. The data is based on unpublished results obtained during this thesis.

Fig. 2.16 shows the transfer characteristic of a flexible CuSCN TG-BC TFT measured while flat and bent to a tensile radius of 4 mm. Bending to a radius of 4 mm results in a decrease of μ_{SAT} by -16 % and in a positive shift of V_{TH} by +30 mV. Also BG-BC devices are operational at bending radii of 4 mm (ϵ = 0.58 %), showing similar strain-induced variations: a μ_{SAT} decrease by -23 % and a V_{TH} shift of -100 mV. Bending to smaller radii leads to crack formation in the brittle Cr gate contacts.

Circuits: Fig. 2.17 displays the voltage transfer characteristic (VTC) and the static gain of a flexible CuSCN-based unipolar voltage inverter based on one driving CuSCN BG-BC TFT (W/L = 3200 µm/20 µm) and a TFT (W/L = 450 µm/20 µm) in diode-load configuration, as shown in the inset of Fig. 2.17. Flexible unipolar inverters exhibit a G = 3.4 V/V and an almost centered V_M = -1.5 V (when V_{IN} is swept from 0 V to -3.5 V at a V_{DD} = -3.5 V). Bending the flexible CuSCN inverters to 4 mm results in a shift of V_M of -100 mV and an increase of the gain of 0.1 V/V, as shown in Fig. 2.17. These changes are explained by the variations in the μ_{SAT} and V_{TH} of the flexible CuSCN TFTs.

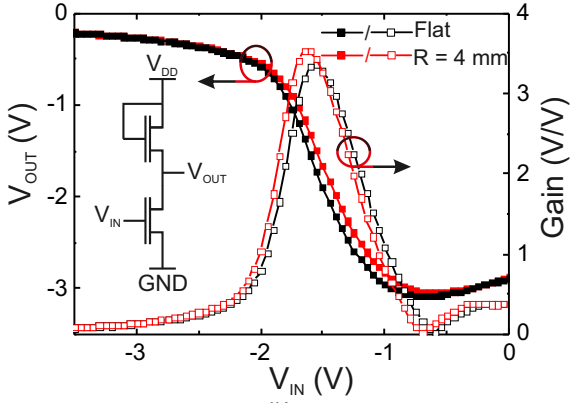

Figure 2.17: Voltage transfer characteristic (VTC) and corresponding static gain of a flexible CuSCN-based unipolar voltage inverter (measured at a supply voltage V_{DD} = -3.5 V), while flat and bent to a tensile radius of 4 mm. The inset shows a schematic of the circuitry used: it comprises a driving CuSCN BG-BC TFT (W/L = 3200 µm/20 µm) and a TFT (W/L = 450 µm/20 µm) in diode-load configuration. The data is based on unpublished results obtained during this thesis.

2.1.2.3 SWCNT TFTs and circuits[2]

Besides CuSCN, also SWCNTs are an attractive solution-processable p-type semiconductor. Flexible devices based on SWCNTs drop-casted [97], dip-coated [132, 100, 133], or ink-jet printed [134] yield average μ_{FE} from 2 $cm^2V^{-1}s^{-1}$ to 50 $cm^2V^{-1}s^{-1}$. Among these methods, one of the main difficulty is represented by the purification and separation of the semiconducting nanotubes from the metallic ones (before deposition). To this end, it has been recently shown that conjugated polymers like polyfluorene-based derivates allow successfully sorting SWCNTs with specific diameters [135, 136], which at the same time have a specific semiconducting or metallic characteristic [137].

In this thesis, polymer-sorted semiconducting SWCNT films spin-

[2]This paragraph is based on: F. Bottacchi, L. Petti, F. Späth, I. Namal, G. Tröster, and T.D. Anthopoulos, Polymer-sorted (6,5) single-walled carbon nanotubes for solution-processed low-voltage flexible microelectronics. In *Applied Physics Letter*, 106. © 2015 AIP.

casted at 90 °C have been incorporated into flexible TFTs and unipolar inverters. The electrical and mechanical performance of the resulting TFTs and circuits has been characterized. The results shown have been obtained in a collaboration between Imperial College London (Centre for Plastic Electronics and Department of Physics), ETH Zurich, and Julius-Maximilian University of Würzburg (Institute of Physical and Theoretical Chemistry).

Device structure and fabrication: SWCNT TFTs were manufactured on a free-standing 50 μm-thick PI foil employing the same device structure (BG-BC) and fabrication process previously described for In_2O_3 TFTs (see Fig. 2.12a, page 57). The only difference is represented by the semiconducting material and deposition process:

The active layer solution was prepared by mixing 100 mg CoMoCat SWCNTs (Sigma-Aldrich) and 200 mg poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-co-(6,6′-2,2′-bipyridine)] PFO-BPy (American Dye Source) in 200 mL of toluene. The so-formed mixture was subjected to ultrasonication for 14 h, centrifugation, and vacuum filtering to remove the excess polymer. The resulting single chirality (6,5) SWCNTs were then re-dispersed in chlorobenzene, spin-casted (1000 rpm for 30 s at room temperature), and annealed at 90 °C in nitrogen. The resulting 10 nm-thick (6,5) SWCNT film was left unstructured. Additionally, by employing PFO instead of PFO-BPy, also SWCNTs with a different chirality (7,5) can be achieved (see chapter 7, page 135).

The channel width over length ratio (W/L) of the resulting flexible BG-BC SWCNT devices is of 280 μm/35 μm.

Fig. 2.18a displays the absorption spectrum of the polymer/SWCNT solution in chlorobenzene, measured using an UV-Vis-NIR spectrophotometer in absorbance mode and 1 mm light path cuvette. Single chirality (6,5) is proven by the presence of the two sharp absorption peaks at 1000 nm and 575 nm, which correspond respectively to the first and second excitonic transitions of the (6,5) diameter SWCNT [138]. Fig. 2.18b shows the AFM image of the surface topography of a ~10 nm-thick polymer-wrapped spin-casted SWCNT film. From Fig. 2.18b, the randomly oriented SWCNT network is visible.

TFT electrical performance: The I_D-V_{GS} transfer and I_D-V_{DS} output characteristics of flexible SWCNT BG-BC devices measured in

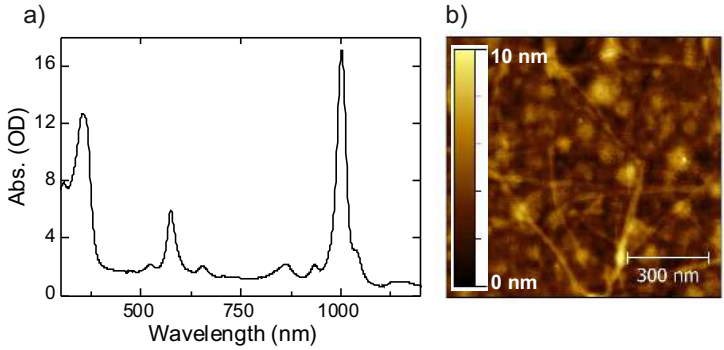

Figure 2.18: a) Absorption spectrum of the SWCNT solution in clorobenzene. b) AFM surface topography image of SWCNT film spin-casted on $Si/SiO_2/SiN_x/Cr/Al_2O_3$. More details are available in [101].

nitrogen atmosphere are shown in Fig. 2.19. Based on these measurements, the following DC performance parameters were extracted: a μ_{SAT} of 8.1 $cm^2V^{-1}s^{-1}$, a V_{TH} of -3.1 V, an I_{ON}/I_{OFF} >10^4, and a SS of 1.1 V/dec. When measured with a double sweep of V_{GS}, the SWCNT TFTs present a large counter-clockwise hysteresis in the drain current <1.7 V, which is caused by the polymeric presence in the SWCNT solution, whereas the slightly ambipolar behavior is due to the intrinsic properties of the SWCNTs. The obtained performance, especially the hole μ_{FE} of 8.1 $cm^2V^{-1}s^{-1}$, demonstrate that polymer-sorted semiconducting SWCNTs are a particularly appealing option to realize flexible complementary circuits.

TFT mechanical properties: Flexible SWCNT TFTs were demonstrated to be operational while bent down to tensile radii of 4 mm (ϵ = 0.63 % calculated using equation 1.2 [87]). Bending to 4 mm results in a decrease of μ_{SAT} by -6 % and in a shift of V_{TH} by -50 mV. Smaller bending radii are not possible due to the formation of cracks in the brittle Cr gate.

Circuits: Fig. 2.20 displays the VTC and the corresponding static gain of a flexible SWCNT-based unipolar voltage inverter constituted by one driving SWCNT BG-BC TFT (W/L = 1400 μm/20 μm) and a passive load (metal thin-film resistor with R = 160 kΩ), as shown in the inset

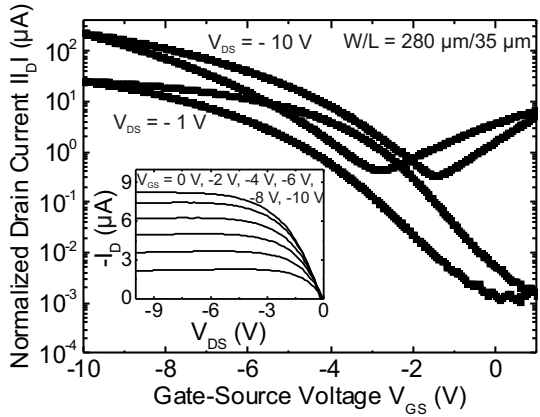

Figure 2.19: Transfer characteristic of flexible BG-BC TFT based on spin-casted (6,5) SWCNTs (W/L = 280 μm/35 μm) measured at a V_{DS} of -1 V (linear regime) and -10 V (saturation regime) in nitrogen atmosphere. The inset displays the corresponding output characteristic. More details are available in [101].

of Fig. 2.20. Flexible unipolar inverters exhibit a G = 5.3 V/V and a perfectly centered V_M = -1 V (when V_{IN} is swept from 0 V to -2 V at a V_{DD} = -2 V). Higher gains ≥87 V/V (22 V/V) can be realized in flexible inverters by complementing p-type solution-processed SWCNT TFTs with n-type IGZO (In_2O_3), as presented in the next section 2.1.3 and in chapter 7 (page 135).

2.1.3 Material and device integration and application

In this subsection, the integration of metal oxide semiconductor TFTs for flexible electronic applications is tackled. In particular, flexible non-volatile IGZO memory TFTs are first investigated. Then, the integration of n-type metal oxide semiconductors (either IGZO or spray-coated In_2O_3) and p-type solution-processed SWCNTs for the realization of flexible complementary (CMOS) circuits is presented.

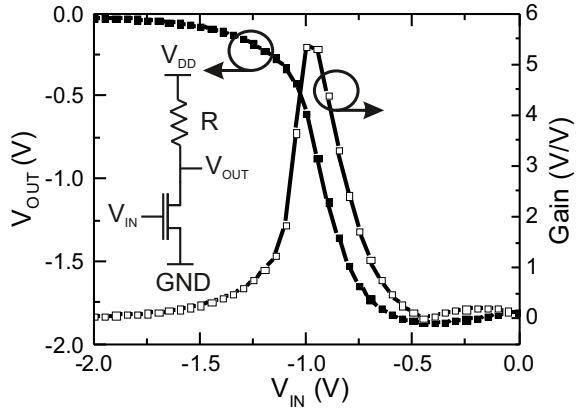

Figure 2.20: VTC and corresponding static gain of a flexible (6,5) SWCNT-based unipolar voltage inverter (measured at a V_{DD} = -2 V). The inset shows a schematic of the circuitry used: it comprises a driving SWCNT BG-BC TFT (W/L = 1400 μm/20 μm) and one metal thin-film resistor (R = 160 kΩ). More details are available in [101].

2.1.3.1 IGZO memory TFTs

To enable novel flexible electronic applications, non-volatile memory devices that combine mechanical flexibility and low-power dissipation are required. To this aim, ferroelectric gate dielectrics, in particular P(VDF-TrFE), are especially attractive, owing to their high spontaneous polarization of 50-100 mC/m^2 and their solution-processability at process temperature <140 °C [139]. The reversible polarization of P(VDF-TrFE) can be used in metal oxide semiconductor ferroelectric TFTs (Fe-TFTs) to realize single transistor non-volatile memory devices [140, 21, 141, 142, 85]. To employ these memory devices in flexible applications, it is crucial to understand their behavior under mechanical strain. Such study is particularly important considering that P(VDF-TrFE) is not only a ferroelectric, but also a piezoelectric polymer [143].

In this thesis, flexible IGZO Fe-TFTs have been characterized at tensile and compressive bending radii down to 5.5 mm.

Fabrication: Section 6.2 (page 119) describes the device structure and fabrication process of flexible IGZO Fe-TFTs with P(VDF-TrFE)

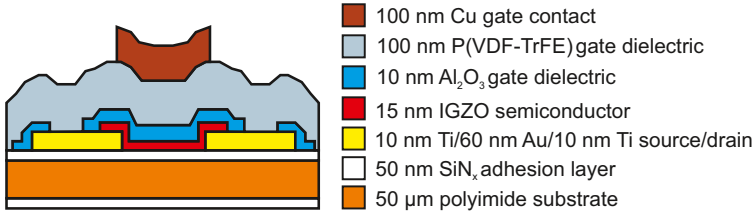

Figure 2.21: Schematic cross section of flexible IGZO memory TFT with ferroelectric P(VDF-TrFE) gate dielectric fabricated directly on a PI foil. More details are available in section 6.2 (page 119).

dielectrics (Fig. 2.21). The IGZO Fe-TFTs are based on the same device structure (TG-BC) previously described for IGZO TFTs with DLW-defined channel, with the following difference:

As a gate dielectric, a hybrid multi-layer constituted by 10 nm Al_2O_3 and 100 nm P(VDF-TrFE) was employed. The Al_2O_3/P(VDF-TrFE) multi-layer dielectric ensures a low gate leakage current and at the same time a good interface with the active IGZO layer [144]. The Al_2O_3 was first grown by ALD and patterned by standard UV photolithography and wet etching. Subsequently, 1 wt% VDF (70 mol%) and TrFE (30 mol%) were dissolved in MEK, spin-coated and crystallized at 140 °C in ambient air.

In addition to IGZO Fe-TFTs, also reference IGZO TG-BC with 25 nm Al_2O_3 gate dielectrics were fabricated on the same substrate. The reference TFTs have a W/L = 280 µm/115 µm, whereas the Fe-TFTs have a W/L = 1400 µm/20 µm to partially compensate for the different gate capacitance per area. For the bending measurements, the TFT masks were designed to allow cutting the process substrate (area 7.6 x 7.6 cm^2) into stripes with one TFT per stripe.

Electrical performance: The electrical performance of flexible IGZO ferroelectric memory TFTs, as well as reference devices, has been characterized in section 6.3 (page 121).

DC performance: Flexible IGZO TG-BC reference TFTs yield the following DC performance parameters: an effective linear field-effect mobility μ_{LIN} of 7.5 $cm^2V^{-1}s^{-1}$, a V_{TH} of 0.3 V, an I_{ON}/I_{OFF} of 2.2×10^7,

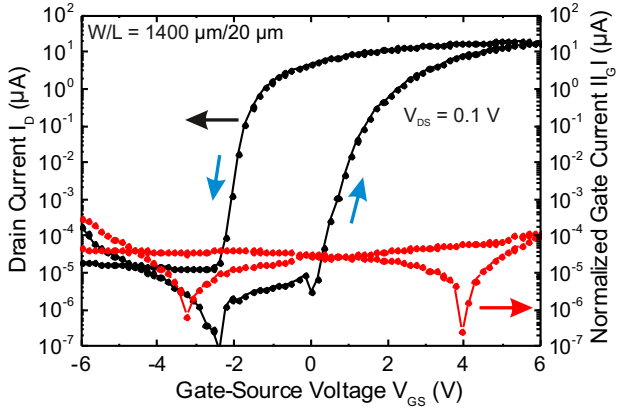

Figure 2.22: Flexible IGZO memory TFT with ferroelectric P(VDF-TrFE) gate dielectric (W/L = 1400 µm/20 µm): a) hysteretic transfer characteristic (at V_{DS} = 0.1 V). Indicated blue arrows describe the direction of the transfer curve measured with a double sweep of V_{GS} between −6 V and 6 V. More details are available in section 6.3 (page 121).

and a SS of 106 mV/dec. Compared to flexible IGZO BG TFTs with the same gate stack materials [45], the ≈2x lower μ_{LIN} is attributed to a less clean IGZO/Al_2O_3 interface in the TG-BC geometry. When measured with a double sweep of V_{GS}, reference TFTs present a clockwise hysteresis <25 mV. Fig. 2.22 shows the I_D-V_{GS} hysteretic transfer characteristic of a flexible IGZO Fe-TFT, measured with a double sweep of V_{GS} between −6 V and 6 V, at V_{DS} = 0.1 V. The ferroelectric-driven memory operation is demonstrated by the counter-clockwise hysteresis of the drain current (see blue arrows in Fig. 2.22). Due to the hysteresis, the transfer curve presents a forward (V_{GS} from -6 to 6 V) and a reverse (V_{GS} from 6 to -6 V) branch. This leads to two different values of the threshold voltage V_{TH} of 1.3 V (forward) and −1.9 V (reverse). The memory window MW, which is defined as the difference of V_{TH} under the forward and the reverse operation, is therefore 3.2 V. The memory on/off ratio, which is the ratio between the memory on-value $I_{D,REV}$ (V_{GS} = 0 V) and off-value $I_{D,FOR}$ (V_{GS} = 0 V) is 1.5 x 10^6. Furthermore, the IGZO Fe-TFT exhibits a μ_{LIN} of 8 $cm^2V^{-1}s^{-1}$, an I_{ON}/I_{OFF} of 1.7 x 10^7, and a SS of 152 mV/dec. These parameters are comparable to those of previously reported flexible IGZO Fe-TFTs [140, 21, 141, 142].

The programming and retention characteristics of flexible IGZO Fe-TFTs were evaluated in subsection 6.3.2 (page 122). Applying V_{GS} pulses of 6 V (set memory state <1>) and -6 V (set memory state <0>) for 1 s, an initial memory on/off ratio of more than 10^3 (at V_{GS} = 0 V) was obtained, and still remained to be more than 50 after 100 s. This is comparable to previous reports on metal oxide semiconductor Fe-TFTs with Al_2O_3/P(VDF-TrFE) gate dielectric [145, 146]. Larger values can be obtained by utilizing single-layer high-quality P(VDF-TrFE) gate dielectrics (without Al_2O_3) [142].

Mechanical performance: The mechanical properties of flexible IGZO Fe-TFTs (and reference devices) were investigated in section 6.4 (page 124) using a custom-built bending setup to measure the devices at arbitrary bending radii while connected to the parameter analyzer.

Setup: To measure the influence of bending, a mask layout with contact pads 1 cm away from the channel was utilized. Each single TFT/Fe-TFT was cut from the process substrate and attached to a flexible carrier substrate. Contact pads on the TFTs/Fe-TFTs were electrically connected to the carrier interconnections using glued Cu wires [106]. Interconnections on the carrier were subsequently connected to the parameter analyzer to be able to constantly monitor the device characteristics at arbitrary bending radii, without the need of probe tips. The carrier substrate was then placed between two movable plates in a custom build bending tester (see inset of Fig. 2.23). The substrate was positioned with the Fe-TFT/TFT facing upward (downward) to apply tensile (compressive) strain parallel to the channel length. The actual bending radius was defined by moving the plates, and was measured by fitting circles to images taken by an optical camera.

Influence of strain: Flexible IGZO TG-BC reference TFTs were bent down to tensile (compressive) radii of 5.5 mm, resulting in tensile (compressive) strain ϵ = 0.64 % (-0.59 %) calculated using equation 1.2 [87]. As expected, tensile and compressive bending results in opposite variations: for tensile (compressive) strain ϵ = 0.64 % (-0.59 %), the maximum drain current $I_{D,MAX}$ changes by +10 % (-11 %) and V_{TH} shifts by -90 mV (+90 mV). These values are in good agreement with previous reports on flexible IGZO BG and TG devices [106, 147, 45, 148],

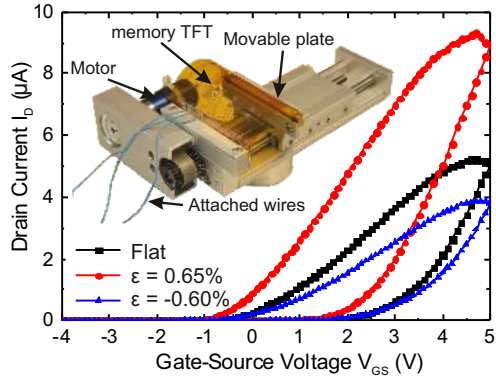

Figure 2.23: Transfer characteristic of flexible IGZO memory TFT with ferroelectric P(VDF-TrFE) gate dielectric (W/L = 1400 μm/20 μm), measured while flat, bent to a tensile radius of 5.5 mm (ϵ = 0.65 %) and bent to a compressive radius of 5.5 mm (ϵ = −0.6 %) at V_{DS} = 0.1 V. The inset shows a photograph of the custom-built bending tester utilized for the measurement. More details are available in section 6.4 (page 124).

and are attributed to the under tensile (compressive) strain-induced increase (decrease) of the IGZO mobility and carrier density [106]. Fig. 2.23 shows the linear transfer characteristic of a flexible IGZO Fe-TFT, measured while flat, bent to a tensile radius of 5.5 mm (ϵ = 0.65 %) and then bent to a compressive radius of 5.5 mm (ϵ = -0.6 %). Like for reference TFTs, the transfer curve presents shifts in opposite directions for tensile and compressive bending. Nevertheless, for Fe-TFTs, the measured changes are larger than those observed for reference TFTs. Bending IGZO Fe-TFTs at tensile (compressive) strain ϵ = 0.65 % (-0.6 %) results indeed in the following changes: the $I_{D,MAX}$ varies by 177 % (-24 %), the forward V_{TH} shifts by -810 mV (-40 mV), whereas the reverse V_{TH} changes by -580 mV (-10 mV). Since V_{TH} shifts in the same direction for the forward and the reverse branch, the memory window is not significantly affected by bending. On the other hand, the memory on/off ratio changes up to +318% (-28%) for tensile (compressive) strain ϵ = 0.65 % (-0.6 %). The observed behavior can be explained considering that P(VDF-TrFE) is not only ferroelectric, but also piezoelectric [143], therefore its polarization depends on the applied mechanical strain.

In subsection 6.4.3 (page 127), the mechanism behind the observed bending-induced variations of flexible IGZO Fe-TFTs are investigated thoroughly, and explained by a superposition of the strain-induced dependence of the polarization in the piezoelectric P(VDF-TrFE) layer, and the strain-dependent IGZO properties. These shifts need to be considered when designing future flexible memories. Memory operation down to bending radii of 5.5 mm demonstrates that these devices are feasible for next-generation large-area highly functional flexible electronic systems.

2.1.3.2 Complementary circuits

To realize low-power and compact circuitry with metal oxide semiconductor devices, complementary circuits based on both n- with p-type TFTs are required. Nevertheless, the scarce availability and performance of p-type metal oxide semiconductor TFTs limits the realization of a complementary technology. For this reason, to date, there are only a few reports on flexible circuits based on n- and p-type metal oxide semiconductors [34, 67, 99, 35]. Recently, solution-based SWCNTs are drawing a considerable attention for flexible electronics [97, 100, 133].

In this work, spin-coated highly-selected semiconducting (7,5) SWCNTs have been integrated with sputtered IGZO and spray-coated In_2O_3 to fabricate complementary logic inverters. The results shown have been obtained in a collaboration between Imperial College London (Centre for Plastic Electronics and Department of Physics), ETH Zurich, and Julius-Maximilian University of Würzburg (Institute of Physical and Theoretical Chemistry).

Fabrication: Section 7.2 (page 137) describes the fabrication process of flexible complementary inverters based on SWCNTs and sputtered IGZO or spray-coated In_2O_3. Fig. 2.24 shows the schematic cross section and the circuit diagram of the flexible inverters fabricated on a free-standing 50 µm-thick PI foil (area 7.6 x 7.6 cm^2). The inverters are based on the BG-BC device structure previously described for flexible In_2O_3 and SWCNT single TFTs. In this case, after the Ti/Au top metallization e-beam evaporation and lift-off:

The foil was diced into chips of 1.5 x 1.5 cm^2 to allow multiple depositions at different process conditions. Then, either RF sputtered IGZO or spray-coated In_2O_3 were deposited using the already de-

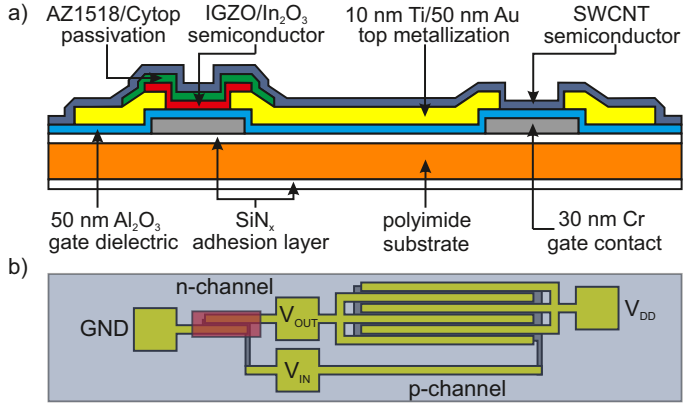

Figure 2.24: Flexible complementary inverter based on solution-processed SWCNT TFTs and metal oxide semiconductor TFTs on a free-standing PI foil: schematic cross section and b) circuit layout. More details are available in section 7.2 (page 137).

scribed process conditions. In the case of IGZO n-type active layers, semiconductor islands were formed by wet etching and passivated with photoresist (AZ1518®). For In_2O_3, the n-type semiconductor was patterned during the automated spray process using shadow masking, and subsequently passivated with a Cytop® layer.

To complement the n-type IGZO and In_2O_3, a semiconducting (7,5) SWCNT solution, behaving as p-type active layer, was used. The unstructured and unpassivated (7,5) SWCNT film was obtained with the same process protocol previously presented for single SWCNT devices. In this case, (7,5) chirality was achieved by means of PFO-wrapping.

All TFTs have a channel length of 25 μm, with an interdigitated channel, as visible in Fig. 2.24b. The complementary inverters were realized using the circuit schematic shown in the inset of Fig. 2.26.

Electrical performance: The electrical performance of flexible IGZO, In_2O_3 and SWCNT single TFTs, as well as flexible IGZO/SWCNT and In_2O_3/SWCNT complementary inverters has been characterized in sections 7.3 (page 138) and 7.4 (page 142). Fig. 2.25 displays the VTC and the static gain of flexible IGZO/SWCNT complementary inverters mea-

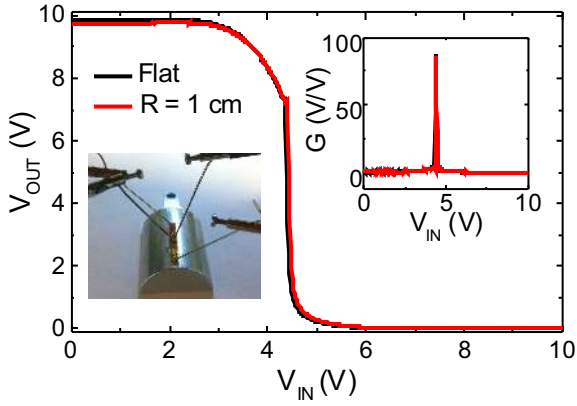

Figure 2.25: VTC of a flexible IGZO/SWCNT complementary inverter (measured at a V_{DD} = 10 V in nitrogen atmosphere), while flat and bent to a tensile radius of 1 cm. The inset shows both the corresponding static gain and a photograph of the flexible inverter measured while bent to 1 cm. The circuit comprises an n-type IGZO TFT (W/L = 1000 µm/25 µm) and a p-type SWCNT TFT (W/L = 10 000 µm/25 µm). More details are available in section 7.3 (page 138).

sured at a V_{DD} = 10 V in nitrogen (when V_{IN} is swept from 0 V to 10 V). At V_{DD} = 10 V, the flexible inverter exhibits a V_M = 4.39 V, a G = 87 V/V, and a rail-to-rail output swing from 0.29 V to 9.93 V. To exploit the potential of solution-processed semiconductors, spin-coated SWCNTs were also integrated with spray-coated In_2O_3. Fig. 2.26 displays the VTC and the static gain of flexible In_2O_3/SWCNT complementary inverters measured at a V_{DD} = 10 V in nitrogen (when V_{IN} is swept from 0 V to 10 V). At a V_{DD} = 10 V, the flexible inverter yields a V_M = 3.97 V, a G = 22 V/V, and an output swing from 0.3 V to 9.2 V.

Mechanical performance: The mechanical performance of flexible IGZO and SWCNT single TFTs, as well as flexible IGZO/SWCNT complementary inverters has been characterized in section 7.3 (page 138). Fig. 2.25 shows the VTC and the static gain of flexible IGZO/SWCNT complementary inverters, measured while flat and bent to 1 cm tensile radius ($\epsilon \approx 0.29\,\%$ parallel to the channels calculated using equation 1.2 [87]) at a V_{DD} = 10 V. Flexible IGZO/SWCNT inverters are func-

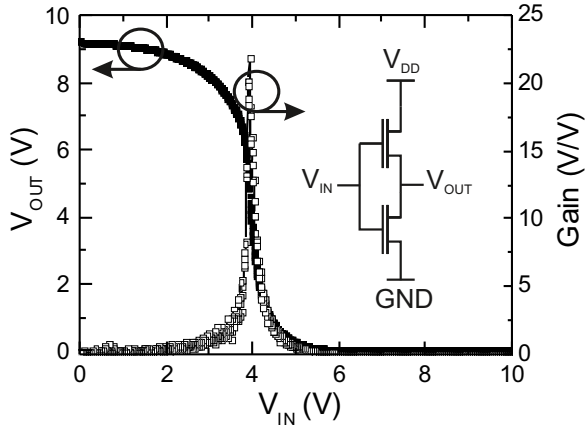

Figure 2.26: VTC and corresponding static gain of of a flexible In_2O_3/SWCNT complementary inverter (measured at a V_{DD} = 10 V in nitrogen atmosphere). The inset shows a schematic of the circuitry used: it comprises an n-type In_2O_3 TFT (W/L = 2500 µm/25 µm) and a p-type SWCNT TFT (W/L = 10 000 µm/25 µm). More details are available in section 7.4 (page 142).

tional while bent and exhibit only small changes in V_M (+40 mV) and G (-1.6 %), which are due to the variations in the μ_{FE} and V_{TH} of the n- and p-type TFTs.

2.2 Conclusion

This thesis focuses on the development of metal oxide semiconductor TFTs for flexible electronics. A wide range of materials, device structures, and fabrication processes have been utilized to manufacture flexible TFTs, as summarized in Table 2.1. In particular, advanced device structures and fabrication processes have been employed to realize flexible IGZO TFTs with channel lengths down to 280 nm; low-temperature and scalable spray pyrolysis has been employed to fabricate flexible n-type In_2O_3 TFTs and unipolar logic inverters; inorganic (CuSCN) and organic (SWCNT) p-type semiconductors have been solution-deposited at low temperatures and incorporated in flexible TFTs and unipolar logic inverters; the influence of mechanical strain on the performance of non-volatile ferroelectric IGZO memory

	Semicond. Deposition	Max. Temp. (°C)	Device Type	μ_{FE} ($cm^2\ V^{-1}\ s^{-1}$)	V_{TH} (V)	I_{ON}/I_{OFF}	f_T (MHz)	Channel Length (μm)	Bending Radius (mm)	Strain (%)	Bending Cycles
IGZO VTFT,	RF sputtering	150	N-type	0.02	2.2	2×10^7	0.08	0.5	5	0.5	1000
IGZO QVTFT,	RF sputtering	150	N-type	0.2	1.5	1×10^4	1.5	0.3	5	0.48	-
IGZO TG TFT with DLW,	RF sputtering	150	N-type	1.1	3	1×10^3	80	0.28	10	0.2	-
In_2O_3 BG TFT,	Spray pyrolysis	250	N-type	0.2	5.29	6×10^3	-	20	4	0.65	-
CuSCN BG TFT,	Spin casting	150	P-type	0.0013	-1	5×10^2	-	20	4	0.58	-
(6,5) SWCNT BG TFT,	Spin casting	150	P-type	8.1	-3.1	1×10^4	-	35	4	0.63	-
IGZO Fe-TFT.	RF sputtering	150	N-type	8	1.3/-1.9	2×10^7	-	20	5.5	0.65	-

Table 2.1: Set of performance parameters extracted from the flexible TFTs reported in this thesis.

TFTs has been investigated; flexible complementary inverters based on n-type metal oxide semiconductors (both sputtered IGZO and spray-coated In_2O_3) and p-type SWCNTs have been demonstrated. Based on the summary of the contributions presented in section 2.1, the following conclusions can be drawn:

- Short channel lengths below 500 nm are necessary to fabricate flexible metal oxide semiconductor TFTs with small footprint and high transit frequency for e.g. transceivers, RFID tags, or AM radios. The realization of sub-micrometer feature sizes on flexible substrates is challenging. State of the art conventional and self-aligned photolithography on flexible foils are limited to TFT channel lengths of 1 µm and 500 nm, respectively [20, 75]. To obtain smaller feature sizes on flexible substrates, vertically integrated device structures were explored. Vertical devices not only enable shorter channel lengths, but also higher drain current densities (if compared to planar TFTs). Among the possible vertical-type TFTs, the VTFT geometry based on a multi-layer source-spacer-drain stack was identified as the most performing in terms of DC and AC performance. To realize IGZO VTFTs with this structure, two different fabrication processes based on dry etching and bi-layer lift-off of the vertical sidewall were proposed and compared. While dry etching resulted in an under-cut vertical profile and in strong source/drain contact contamination, the bi-layer lift-off process led to the reliable formation of a quasi-vertical sidewall and to the conformal coverage of the successive device layers. Even if channel lengths down to 300 nm were demonstrated for flexible IGZO QVTFTs, the still existing (even if reduced) process-induced source/drain contamination resulted in large contact resistance, which degraded μ_{FE} and f_T to values of $0.2\,cm^2V^{-1}s^{-1}$ and 1.5 MHz, respectively. Despite also planar IGZO TFTs with 500 nm channel lengths exhibit a degraded contact resistance, the less pronounced effect allows higher μ_{FE} and transit frequency [20, 75]. This is why, alternative structuring techniques based on DLW photolithography were explored and successfully employed to fabricate flexible planar IGZO TFTs. The resulting TG devices exhibit a channel length as small as 280 nm. Nevertheless, compared to self-aligned IGZO BG TFTs (L = 500 nm), flexible IGZO TG devices (L = 280 nm) still yield slightly lower μ_{FE} and f_T of $1.1\,cm^2V^{-1}s^{-1}$ and 80 MHz, respectively. This worse performance is not only attributed to

the further degraded contact resistance of flexible IGZO devices with even shorter channels, but also to the ≈2x lower average μ_{FE} of IGZO TG devices, compared to BG TFTs made of the same materials [105]. Nonetheless, already based on these first results, DLW photolithography seems to be a promising technique for flexible short-channel and high-frequency metal oxide semiconductor-based electronics.

- Cost-effective, large-area and high-throughput manufacturing techniques of flexible metal oxide semiconductor TFTs are required for applications like foldable and printable displays, disposable smart labels, and intelligent packaging. To this aim, simple and scalable solution processes like spray pyrolysis on large-area flexible substrates are especially desirable. Nevertheless, solution processing of metal oxide semiconductors typically requires high process temperatures ($\gg$250 –350 °C for spray pyrolysis) incompatible with temperature-sensitive flexible plastic substrates. The use of new precursor material formulations and optimized processing protocols allowed spray-coating In_2O_3 films on flexible foils at 250 °C. The resulting spray-deposited In_2O_3 active layers were successfully incorporated in flexible TFTs with μ_{FE} of 0.2 $cm^2V^{-1}s^{-1}$, as well as in unipolar inverters. Device operation at tensile bending radii of 4 mm demonstrated the potential of spray pyrolysis as a simple and scalable deposition tool for the manufacturing of flexible metal oxide semiconductor-based electronics.

- P-type semiconductor TFTs are necessary for the development of a flexible complementary thin-film technology. Applications like smart labels and intelligent packaging, as well as wearable sensory systems would certainly profit from the availability of high-performance, low-power, compact and flexible metal oxide semiconductor-based CMOS circuits. Nevertheless, to date, it is still difficult to achieve p-type metal oxide semiconductors, especially at low process temperatures. To this aim, promising solution-processable inorganic (CuSCN) and organic (SWCNT) p-type semiconductors were explored. Flexible p-type TFTs based on spin-casted CuSCN exhibited an μ_{FE} of 0.0013 $cm^2V^{-1}s^{-1}$, whereas flexible devices with spin-casted SWCNT yielded a significantly higher value of 8.1 $cm^2V^{-1}s^{-1}$. Employing solution-processed CuSCN and SWCNT TFTs, also

flexible unipolar inverters with gains of at least 3.4 V/V were realized. Notably larger gains of 87 V/V were achieved by complementing n-type IGZO with p-type SWCNTs on flexible substrates. Circuit operation at tensile bending radii of 10 mm proved the potential of flexible hybrid CMOS circuits. Additionally, to exploit the advantages of solution-processed semiconductors, flexible CMOS inverters based on spin-coated SWCNTs and spray-coated In_2O_3 with gains of 22 V/V were demonstrated. These results pave the way towards large-area and high-performance solution-processable flexible electronics.

- Besides logic, also memory functionality is important in applications like smart labels, intelligent packaging, and wearable sensoric systems. At this regard, non-volatile memories combining low-power dissipation and mechanical flexibility are desirable. IGZO TFTs with ferroelectric P(VDF-TrFE) gate dielectrics offer an attractive technological platform to realize non-volatile flexible memories. Nevertheless, to use these devices in flexible applications, it is crucial to understand their behavior under applied mechanical strain, especially considering that P(VDF-TrFE) is not only a ferroelectric, but also a piezoelectric polymer. The influence of tensile and compressive strain (up to $\epsilon \approx \pm 0.6\,\%$) on the performance of flexible IGZO memory TFTs with ferroelectric P(VDF-TrFE) dielectrics was investigated thoroughly. The observed variations were explained by the superposition of the strain-induced dependence of the polarization in the piezoelectric P(VDF-TrFE) layer and the strain-dependent IGZO properties. These shifts need to be considered when designing future flexible memories. Memory operation down to bending radii of 5.5 mm demonstrated that non-volatile ferroelectric memory devices are feasible for next-generation large-area flexible metal oxide semiconductor-based electronics.

2.3 Limitations

This thesis demonstrates the successful development of metal oxide semiconductor devices for flexible electronic applications. Nonetheless, the following limitations were identified:

- The realization of short-channel flexible metal oxide semiconductor TFTs presents the following limitations: 1) First of all,

the device structures (and fabrication processes) are limited to less favorable vertical or top-gate architectures. Compared to BG TFTs, flexible IGZO VTFTs require additional device layers (e.g. SiN_x spacer) and process steps (e.g. spacer structuring), which result in process-induced source/drain contamination. Compared to BG devices, also flexible IGZO TG TFTs require complicated and time-consuming fabrication (especially for DLW), which at the same time results in a more contaminated IGZO/Al_2O_3 interface. Unfortunately, BG devices cannot be realized with DLW photolithography. Indeed, the DLW photoresist encounters polymerization issues (e.g. absorbance and/or reflection of laser wavelengths by different layers) if opaque BG contacts are used, whereas transparent gate electrodes do not allow a correct alignment of the laser. All these issues, combined with the already high contact resistance of short-channel IGZO BG TFTs (L = 500 nm) in the order of 10 Ω cm [20, 75], leads to the limited μ_{FE} values ≤1.1 $cm^2V^{-1}s^{-1}$ shown for flexible IGZO TFTs with sub-500 nm channel lengths. 2) At the same time, the process-induced thermal expansion of the flexible plastic foils limits the minimum overlap length (L_{OV}) between gate contacts and source/drain electrodes, and thus of the minimum gate capacitance (C_G) that can be achieved. This effect is especially dominant in VTFTs, where the source and drain contacts are deposited and structured in two different steps, leading to large L_{OV} ≥ 13 μm (over an active TFT area of 3 x 3 cm^2). This overlap, combined with an even larger overlap between the gate electrodes and the IGZO islands, results in $C_G/W \geq 70$ $fF\mu m^{-1}$ in flexible IGZO VTFTs. On the other side, in IGZO TG TFTs, the overlap between gate contacts and source/drain electrodes (deposited and structured in the same step) is only limited to 5.2 μm (over a lower active TFT area of ≈2 x 2 mm^2), while C_G/W is 32.47 $fF\mu m^{-1}$. All these issues lead to the reported transit frequencies ≤80 MHz, as well as to time-consuming processes up to 5 hours (for devices with DLW-defined channels). 3) The integration of flexible short-channel IGZO devices over circuits with a large count of TFTs (even with long channels ≥1 μm) is limited with the currently presented fabrication processes. As regards flexible IGZO VTFTs, the channel lengths are limited to values between 220 nm (with QVTFTs and 95 nm spacer) and 500 nm, whereas in the case of TG TFTs the limit is given by the low TFT

count and by the reduced laser alignment area.

- There are limitations also on the performance of the demonstrated TFTs. Due to the different semiconductors, gate dielectrics and passivation layers employed (combined with diverse device structures and channel lengths), a large range of effective mobilities was obtained. On one hand, TG long-channel IGZO TFTs with Al_2O_3 gate dielectrics yielded standard μ_{SAT} of $7.5\,cm^2V^{-1}s^{-1}$, $I_{ON}/I_{OFF} \geq 10^7$ and small hysteresis <25 mV at low voltages of 5 V. On the other hand, depending on the device material, structure and fabrication process employed, significantly lower μ_{SAT} and I_{ON}/I_{OFF}, as well as larger hysteresis were obtained (sometimes even at higher voltages). Furthermore, the reduced stability in ambient air of solution-processed semiconductors poses a limit to their applications.

- Unobtrusive integration of flexible devices calls for cheap, large-area, transparent, ultra-thin, flexible, stretchable, and even biocompatible substrates. Here, PI foils were chosen due to their excellent thermal, chemical and mechanical stability, as well as low surface roughness. Other flexible substrates with higher optical transparency and which are at the same time cheaper and more easily available (e.g. PET and PEN), ultra-thin and biocompatible (e.g. parylene), or stretchable and biocompatible (e.g. PDMS) require significant device material and process modifications.

- Both IGZO and In_2O_3 metal oxide semiconductors are based on In, which might be expensive in the future due to its scarcity.

2.4 Outlook

Flexible electronics in general, and metal oxide semiconductor-based devices in particular, promise to enable an unobtrusive integration into everyday objects, and thereby change the future daily life of billion of people in the world. Listed here are some additional research questions that could assist in achieving this goal:

- Flexible short-channel metal oxide semiconductor devices with small footprint and high transit frequency in the GHz regime would have a large effect on the commercialization of flexible electronic circuits and systems. To achieve this, first of all the

source and drain contacts need to be optimized by selecting optimized materials (e.g. sputtered Mo electrodes) and processing conditions (e.g. thermal annealing). Moreover, also the overlap length requires further reductions, for example by self-aligning the gate electrodes to the source and drain contacts in flexible TG TFTs with DLW-defined channels. Additionally, alternative structuring techniques allowing short-channel BG TFTs (which yield an ≈2x μ_{FE} compared to TG devices) have also to be explored. One attractive possibility to realize sub-300 nm in BG devices is offered by FIB-induced milling of the channel area in appropriately selected source/drain contacts. Alternatively, also the use of e-beam photolithography could be investigated, especially on substrates with flat surface and small area. Such properties could be achieved either by attaching a flexible foil to a rigid carrier, or more promisingly by spin-coating a thin polymeric film on top of a rigid Si or glass substrate. This second approach would also allow increasing the bendability of the resulting short-channel devices.

- The future success of flexible metal oxide semiconductor-based electronics strongly depends on the reliable and robust integration of single devices into large-area circuits and systems. For what concerns applications like transceivers, RFID tags, or AM radios, it is necessary to integrate on the same substrate (and within the same process) flexible TFTs with short and long channels. To this regard, modifications to the existing fabrication processes need to be explored, e.g. in DLW-based devices by employing wet etchable source/drain contacts (with optimized work function). This would allow realizing on the same substrate also TG TFTs (with long channels defined by standard UV photolithography and wet etching), improving at the same time also the mechanical bendability of the devices. Similar integration approaches could also be utilized for devices with FIB-defined channels. At the same time, large-area analog and digital CMOS circuits are necessary to boost the performance of metal oxide semiconductor-based flexible electronics. Here, a hybrid approach based on metal oxide semiconductors and SWCNTs was proposed and demonstrated for CMOS inverters. Future work should be devoted to decrease the device hysteresis (e.g. by reducing or suppressing the polymeric content in SWCNTs) and

increase air-stability (e.g. using suitable encapsulation layers). Such improvements could pave the way to high-performance and large-area flexible complementary systems based on sensors, circuits, memories, display elements, and power supplies.

- Future commercialization of flexible metal oxide semiconductor electronics calls for a reduction of the manufacturing cost. To this aim, scalable and high-throughput solution processing techniques on large-area flexible substrates need to be optimized, aiming at printed or roll-to-roll manufacturing processes. To achieve this, further material and processing protocols improvements are required for the semiconducting layers. At the same time, also solution-deposited gate dielectrics (e.g. spin-casted Al_2O_3) and contacts (e.g. spin-casted ITO) need to be developed and integrated into flexible, high-performance and fully solution-processed TFTs and circuits.

- To allow a completely unobtrusive integration of electronic devices everywhere, flexible metal oxide semiconductor TFTs and circuits have to become transparent, thin, flexible, conformable, stretchable, biocompatible and/or even biodegradable. To this aim, further efforts need to be devoted to combine advanced flexible substrates (e.g. biocompatible parylene or PDMS) with suitable device layers (e.g. biocompatible IGZO, SiO_2, and Mg), in order to realize for example electronics that can be implanted into the body. At the same time, also implantable metal oxide semiconductor-based wireless data- and power-transmission systems need to be developed and integrated.

3

Vertical TFTs

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Mechanically flexible vertically integrated a-IGZO thin-film transistors with 500 nm **channel length fabricated on free standing plastic foil**

Electron Device Meeting (IEDM), 2013 IEEE International, pp. 11.4.1-11.4.4, 2013
10.1109/IEDM.2013.6724609

Abstract

We report the first mechanically flexible amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) vertical thin-film transistors (VTFTs) with 500 nm *channel length, fabricated on a free-standing plastic foil, using a low temperature process* <150 °C. *The VTFTs exhibit a well-shaped transfer characteristic, with an on/off current ratio* $>10^7$ *and a threshold voltage of* 2.2 V. *We demonstrate full device functionality down to* 5 mm *bending radius, even after* 1000 *bending cycles. These results proof that VTFTs are feasible for realizing compact and bendable electronic systems.*

3.1 Introduction

Future large-area electronic applications, such as bendable AM radios and radio frequency identification (RFID) tags require flexible devices operating in the MHz regime. Amorphous semiconductors, especially a-IGZO [10], are promising materials due to the high carrier mobility $>10\,cm^2V^{-1}s^{-1}$ and the low deposition temperatures. To achieve high-frequency TFTs, channel length scaling in the sub-micron regime is required. However, due to the dimensional instability of plastic substrates, the channel lengths of flexible amorphous semiconductor-based TFTs are limited to several micrometers [31, 122]. One possibility to reduce the channel length is constituted by the self-alignment technique [149], which allows realizing flexible TFTs with sub-micron length [20]. Nevertheless, this method still suffers from photolithographic constrains, which limit further scaling of the channel length. An attractive alternative is to adopt vertical-type TFTs, where the channel length is defined by the thickness of a dielectric layer, and hence, not limited by lithography resolution and alignment [150]. This enables lengths in the nanoscale regime [102], and at the same time, much higher device-packing densities. To date, amorphous semiconductor VTFTs based on a-Si [150, 102, 151], ZnO [107], and a-IGZO [110] have been reported. However, to our best knowledge, all existing VTFTs have been realized on rigid substrates.

In this work, we advance current state-of-the-art, by reporting the first mechanically flexible amorphous semiconductor-based VTFTs with a channel length of 500 nm fabricated on a free-standing polyimide foil. These results demonstrate that VTFTs are amenable to realize compact, portable and bendable electronic systems. Future im-

provements promise to further gain advantage of the short channels and enable the realization of fast, small-area bendable devices.

3.2 Fabrication

We fabricated flexible a-IGZO VTFTs with 500 nm channel length on a 50 μm-thick polyimide foil (surface area 3 x 3 cm^2). Maximum process temperature is 150 °C. Materials and thickness were optimized for high performance, long term reliability, and bendability. We first deposited 50 nm-thick SiN_x adhesion layers using PECVD. Next, 10 nm Cr/60 nm Au/10 nm Cr source contacts were deposited by e-beam evaporation and structured by lift-off (lithographic mask 1). Following, 500 nm SiN_x were deposited by PECVD. Subsequently, we deposited 10 nm Cr/60 nm Au/10 nm Cr drain contacts (mask 2). Lift-off structured drain contacts were then used as a hard mask to etch the 500 nm thick SiN_x layer by reactive ion etching (RIE), using a $CF4/O_2$ plasma. Next, we deposited 100 nm a-IGZO using RF magnetron sputtering from a ceramic $InGaZnO_4$ target. The IGZO was patterned into islands by lithography (mask 3) and diluted hydrochloric acid. Afterward, 25 nm Al_2O_3 gate dielectric were deposited by ALD at 150 °C. Drain and source vias were opened using lithography (mask 4) and wet etching. Finally, we deposited 200 nm Cu by e-beam evaporation, tilting the substrate 30° to obtain uniform coverage across the VTFT stack. We patterned gates using lithography (mask 5) and wet etching. Fig. 3.1 shows: a) the process flow and b) the device cross section. Fig. 3.2 displays: a) a micrograph and b) an SEM image of a focused ion beam (FIB) cross section. A yield of 80 % was achieved over the entire 3 x 3 cm^2 substrate.

3.3 TFT Characteristic

The I_D-V_{GS} characteristic (Fig. 3.3b) of the fabricated VTFTs (W/L = 60 μm/0.5 μm) shows an on/off current ratio of 2 x 10^7, a threshold voltage V_{TH} of 2.2 V, a subthreshold swing SS of 0.6 V/dec, and a gate leakage current I_G <10 pA. The deposited a-IGZO layers, exhibit a Hall mobility μ_H of 11.8 $cm^2V^{-1}s^{-1}$. Together with a contact resistance $R_C \approx$ 500 kΩ (at the interface between source/drain and IGZO), we extract a transconductance g_m (Fig. 3.4) of 4.9 μS ($V_{GS} = V_{DS} = 5V$). This relatively high contact resistance value is attributed to the oxidation of the Cr contacts, as well as to the contamination of the metal surface during

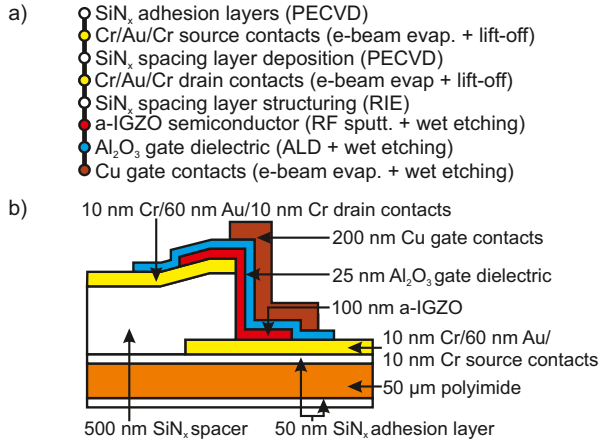

Figure 3.1: Flexible a-IGZO vertical TFTs (VTFTs) with 500 nm channel length fabricated directly on a free-standing plastic foil (3 x 3 cm^2): a) process flow and b) schematic cross section.

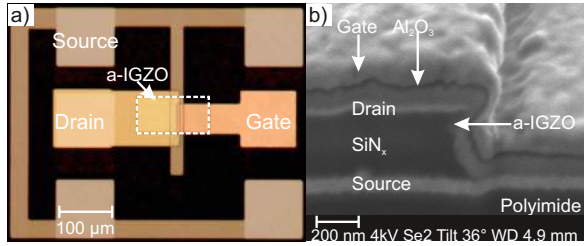

Figure 3.2: Fabricated flexible a-IGZO VTFTs (W/L = 60 µm/0.5 µm): a) micrograph and b) SEM image of the focused ion beam (FIB) cross section through the VTFT channel.

the RIE etching. From I_D-V_{DS} data (Fig. 3.3a), we derive an output conductance g_{ds} (Fig. 3.4) of 0.13 µS (V_{GS} = V_{DS} = 5V), resulting in excellent intrinsic gain $g_m/g_{ds} \geq 38$. The C-V measurements (Fig. 3.5) highlight a relatively high value of the gate capacitance $C_G \approx 9.8$ pF, which is explained by the presence of a parasitic capacitance between gate contact and IGZO, as visible in Fig. 3.2a. This value can be reduced by an optimized layout design with smaller IGZO islands. From the extracted C_G and g_m values, we estimate a transit frequency of ≈80 kHz.

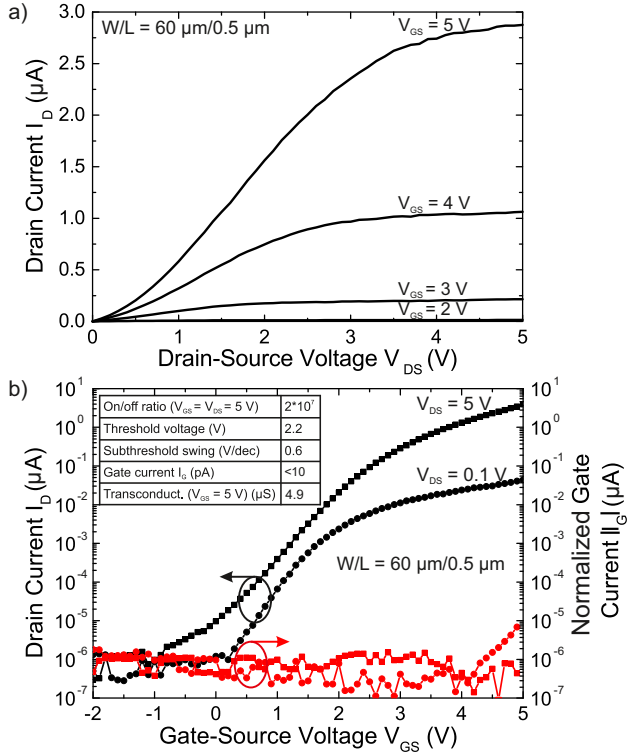

Figure 3.3: DC characteristic of flexible a-IGZO VTFTs (W/L = 60 µm/0.5 µm): a) output and b) transfer characteristic. The inset in b) shows the performance parameters extracted using standard MOSFET equations to model the transistor current. VTFTs do not exhibit hysteresis when the gate-source voltage V_{GS} is swept from -2 V to 5 V (forward) and from 5 V to -2 V (reverse).

This frequency is lower than previously published values of 10 MHz for flexible bottom-gate a-IGZO TFTs [122] and 135 MHz for flexible bottom-gate self-aligned a-IGZO TFTs [20]. However, we believe our VTFTs have a great potential of improvement. Especially, process and layout optimization will enable a reduction of both R_C and C_G, and thus higher frequencies.

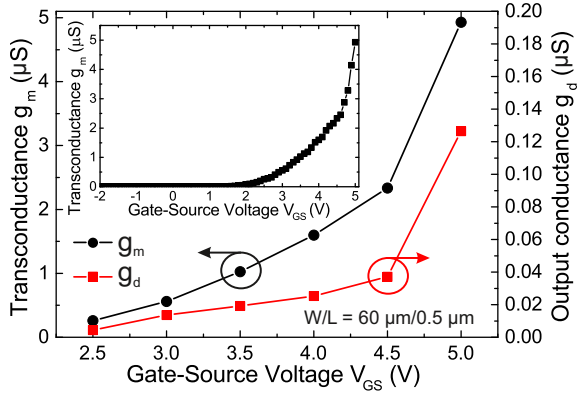

Figure 3.4: Transconductance g_m and output conductance g_{ds} (extracted from data shown in Figure 3.3) of flexible a-IGZO VTFTs (W/L = 60 μm/0.5 μm). The inset displays the derivation of the drain current I_D (transconductance g_m) measured at V_{DS} = 5V. The intrinsic gain (g_m/g_{ds}) exhibits excellent values of 63, always exceeding a value of 38.

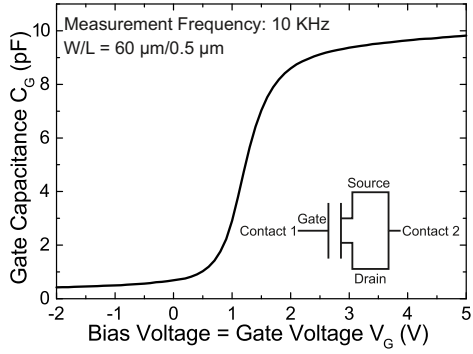

Figure 3.5: Flexible a-IGZO VTFTs (W/L = 60 μm/0.5 μm): gate capacitance C_G measured with source/drain contacts grounded. The measurement was performed at a frequency of 10 kHz. A relatively high capacitance value of $C_G \approx 9.8$ pF is explained by the presence of a parasitic capacitance between gate contact and IGZO (Fig. 3.2a). This value can be reduced by adopting an optimized layout design with smaller IGZO islands.

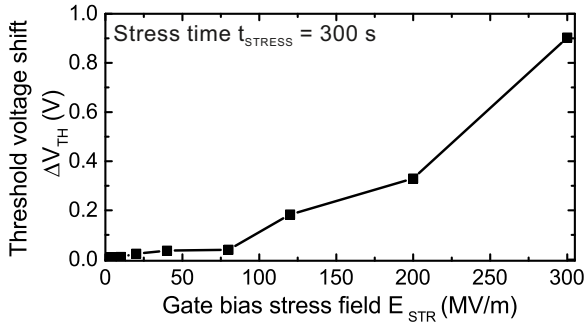

Figure 3.6: Electrical stability of flexible a-IGZO VTFTs (W/L = 60 µm/0.5 µm): threshold voltage shift ΔV_{TH} induced by different bias stress fields applied to the gate contact for a time period of 300 s. For the measurement, source and drain contacts were grounded.

3.4 Stability

To study the electrical stability of flexible a-IGZO VTFTs, I_D-V_{GS} characteristics are measured before and after applying a gate bias stress field between 4 MV/m (V_{GS} = 0.1 V) and 300 MV/m (V_{GS} = 7.5 V) for a time period of 300 s. The VTFTs exhibit a positive threshold voltage shift ΔV_{TH} (Fig. 3.6), caused by carrier injection into the gate dielectric. The maximum observed shift of 0.9 V is comparable with typical shifts in bottom-gate a-IGZO devices [152]. Additionally, our flexible VTFTs have a shelf lifetime of more than 100 days.

3.5 Bendability

Mechanical stability is investigated by winding the substrate around cylindrical rods of 10, 6 and 5 mm bending radius (Fig. 3.7a). This corresponds to tensile strain ϵ of 0.25 %, 0.4 %, and 0.5 % [87] in the direction given in Fig. 3.7b. Fig. 3.8 shows I_D-V_{DS} and I_D-V_{GS} characteristics measured while the substrate is flat and bent to 5 mm. Bending to 5 mm changes V_{TH} by +97 mV and the saturation field effect mobility μ_{SAT} by -2 %. Fig. 3.9 displays the evolution of the threshold voltage shift ΔV_{TH} and of the normalized saturation mobility $\mu_{SAT}/\mu_{SAT,0}$ as a function of the bending radius. Compared to previously published measurements on flexible bottom-gate a-IGZO devices [106], the observed shifts cor-

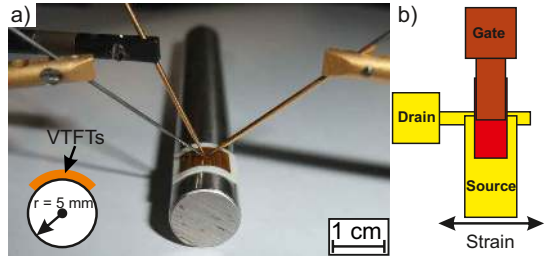

Figure 3.7: a) Photograph of flexible a-IGZO VTFTs contacted and bent around a cylindrical rod of 5 mm bending radius. Tensile strain is applied in the direction shown in b).

respond to compressive strain in the TFT channel. This is due to the Poisson effect, which causes compressive strain perpendicular to the externally applied strain, and thus parallel to the VTFT channel. After re-flattening, the VTFTs stay fully functional; while bending to smaller radii induces cracks perpendicular to the applied strain that permanently harm the devices. Long-term bendability is evaluated by characterizing the VTFTs before and after 1000 cycles of repeated bending (ϵ = 0.25 %) and re-flattening. This corresponds to 15 h of continuous bending using the custom-build bending machine displayed in Fig. 3.10. Fig. 3.11 shows the I_D-V_{DS} and I_D-V_{GS} characteristics of the VTFTs before and after 1000 bending cycles. After 1000 bending cycles, the VTFTs are fully operational, with a threshold voltage shift $\Delta V_{TH} \approx$ -460 mV and an almost constant saturation mobility μ_{SAT} (±0.3 %).

3.6 Conclusion

We present mechanically flexible a-IGZO VTFTs with 500 nm vertical channels fabricated on a free-standing plastic foil, using a low temperature process <150 °C. Our a-IGZO VTFTs are electrically and mechanically stable down to a 5 mm bending radius, withstanding also 1000 cycles of repeated bending and re-flattening. To our knowledge, these are the first mechanically flexible amorphous semiconductor-based VTFTs. These results proof that VTFTs are amenable to realize compact, portable and bendable electronic systems. Furthermore, we foresee potential for future improvements in the fabrication process and in the device layout. In particular, reducing source/drain contact

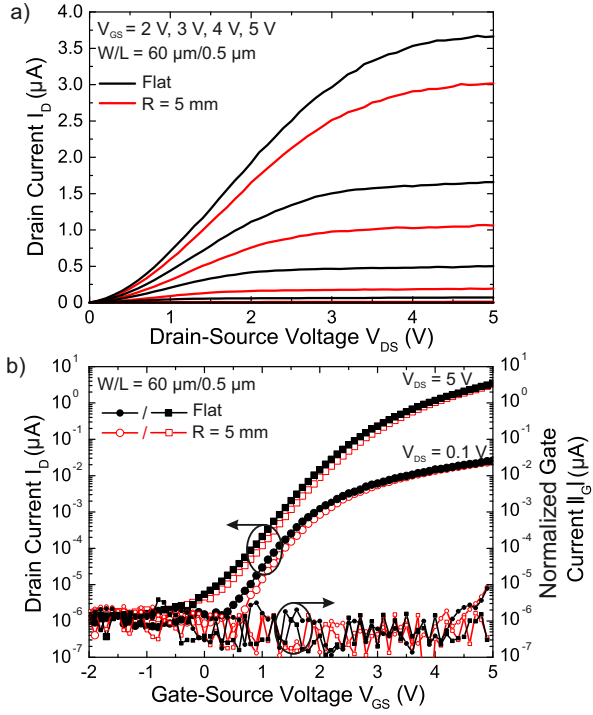

Figure 3.8: DC characteristic of flexible a-IGZO VTFTs (W/L = 60 µm/0.5 µm) while flat and bent to 5 mm (tensile strain ϵ of 0.5 % applied in the direction given in Fig. 3.7b): a) output and b) transfer characteristic. Bending to 5 mm changes V_{TH} by +97 mV and μ_{SAT} by -2 %.

resistance and parasitic capacitances promises enhanced DC and AC performance. This opens the way to high-speed densely-packed flexible devices for bendable AM radios, ultra-sound devices and LF-RFID tags.

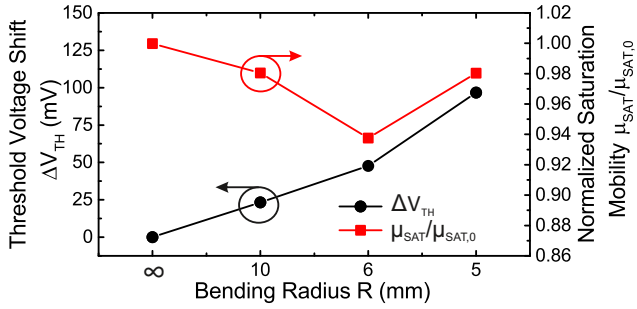

Figure 3.9: Bendability of flexible a-IGZO VTFTs (W/L = 60 µm/0.5 µm): threshold voltage shift ΔV_{TH} and normalized saturation mobility $\mu_{SAT}/\mu_{SAT,0}$ while flat and bent to 10, 6, and 5 mm (strain ϵ of 0.25 %, 0.4 %, and 0.5 %).

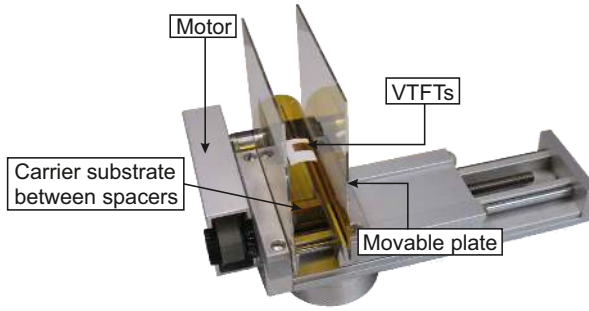

Figure 3.10: Photograph of the custom-built bending tester used for the multiple bending experiments. The actual bending radius was measured by fitting circles to images taken by an optical camera.

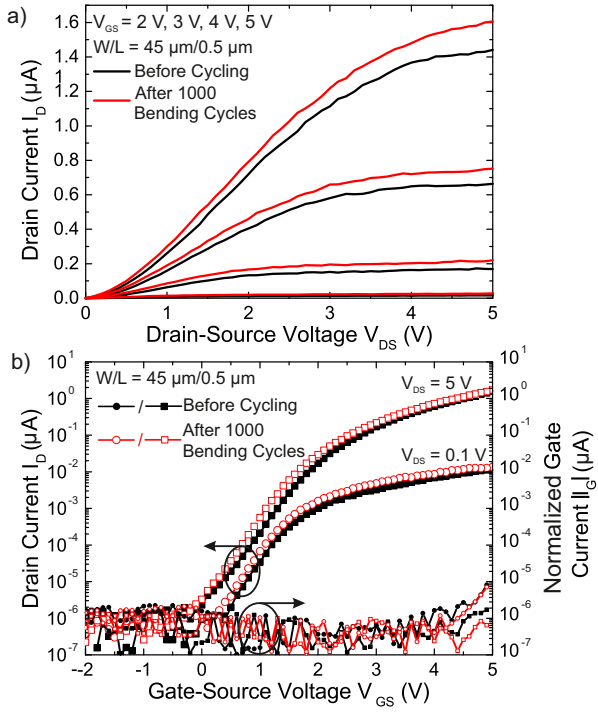

Figure 3.11: DC characteristic of flexible a-IGZO VTFTs (W/L = 45 µm/0.5 µm) before and after 1000 cycles of repeated bending (r = 10 mm, ϵ = 0.25 %) and re-flattening: a) output and b) transfer characteristic. After 1000 bending cycles, the threshold voltage V_{TH} changes by -460 mV, while the saturation mobility μ_{SAT} stays almost constant (±0.3 %).

4

Quasi-Vertical TFTs

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Flexible Quasi-Vertical In-Ga-Zn-O Thin-Film Transistor with 300-nm Channel Length

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Abstract

In this letter, we report a flexible Indium-Gallium-Zinc-Oxide quasi-vertical thin-film transistor (QVTFT) with 300 nm *channel length, fabricated on a free-standing polyimide foil, using a low temperature process* <150 °C. *A bi-layer lift-off process is used to structure a spacing layer with a tilted sidewall and the drain contact on top of the source electrode. The resulting quasi-vertical profile ensures a good coverage of the successive device layers. The fabricated flexible QVTFT exhibits an on/off current ratio of* 10^4 *, a threshold voltage of* 1.5 V, *a maximum transconductance of* 0.73 $\mu S \mu m^{-1}$, *and a total gate capacitance of* 76 $fF \mu m^{-1}$. *From S-parameters measurements, we extracted a transit frequency of* 1.5 MHz. *Furthermore, the flexible QVTFT is fully operational when bent to a tensile radius of* 5 mm.

4.1 Introduction

Bendable thin-film transistors (TFTs) are the fundamental building block for new electronic applications, such as rollable displays, sensory skin, or e-textiles [2]. To enable these, there is strong demand for flexible TFTs with high frequency operation, large current densities and small areas, which can be fabricated using low-temperature processes. In the last decades, vertical TFTs (VTFTs) [150] have emerged as an attractive alternative to planar devices, owing to:

- a channel defined by non-photolithographic methods, allowing nanoscaled lengths and high frequencies [102];
- large W/L ratios, leading to high current densities;
- ≈3x smaller device area, compared to planar TFTs [102].

First examples of VTFTs with mobilities <0.02 $cm^2V^{-1}s^{-1}$ have been realized employing amorphous Silicon (a-Si) [150, 102] and organic semiconductors [153]. Compared to a-Si and organic materials, oxide semiconductors, especially Indium-Gallium-Zinc-Oxide (IGZO), offer carrier mobilities >10 $cm^2V^{-1}s^{-1}$ even if deposited at room temperature [10]. Several types of oxide-based VTFTs have been demonstrated, by using either standard structures with the channel formed on a multilayer stack of source-spacer-drain [110, 111, 52], or alternative architectures with the channel defined by the gate [107, 108] or the semiconductor [109] thickness. To date, IGZO VTFTs with standard structures have

been realized using dry etched sidewalls [110, 111]. However, such dry etching approaches are difficult to optimize in order to avoid under-cut profiles and contaminated source/drain contacts, which degrade TFT performance. Contact contamination can be overcome by wet etching or photolithographic techniques, yet the under-cut in the profile is still present allowing only the use of uniformly layered semiconductors like ALD-deposited ZnO [52]. Alternative structures with channels defined by the gate thickness lead to better DC performance, but cause large gate/source-drain capacitances, limiting AC performance [107, 108]. Additionally, VTFTs with lengths defined by the IGZO thickness yield poor electrostatic control [109].

To overcome these issues, we propose a VTFT structure with a quasi-vertical sidewall, realized by a bi-layer lift-off of spacing layer and drain contact. This approach circumvents the problems related to wet and dry etched profiles, leading to a reliable sidewall formation and a conformal deposition of all device layers. The resulting IGZO VTFT exhibits 300 nm channel length, well-shaped characteristics and megahertz operation. In addition, the flexible substrate enables device operation at 5 mm radius.

4.2 Device Structure and Fabrication

An IGZO quasi-vertical TFT (QVTFT) (Fig. 4.1a) was fabricated on a free-standing 50 μm-thick polyimide foil (area 3 x 3 cm^2). Both sides of the substrate were covered with 50 nm PECVD-deposited SiN_x as adhesion layer. Next, 10 nm Ti/ 60 nm Pd were deposited by e-beam evaporation and structured into source contacts using a lift-off process. Subsequently, we spin-coated 4 μm LOR-5B (MicroChem Corp.) at 400 rpm for 4 sec, followed by 4000 rpm for 45 sec, and baking at 115 °C for 2 min. Then, 2 μm SU-8 2002 (MicroChem Corp.) was spin-coated at 500 rpm for 10 sec, followed by 2000 rpm for 50 sec, and baking at 95 °C for 90 sec. Successively, the bi-layer was structured into drain contacts by photolithography. Post-lithographic procedures included development in Ethylactate for 60 sec, post-baking at 170 °C for 10 min and development of LOR-5B in MA-D533s (90 sec). Deposition and structuring of the bi-layer were optimized to achieve an under-cut between SU-8 and LOR-5B (≈4.1 μm). During the subsequent deposition of a 130 nm-thick SiN_x (PECVD, 120 °C) and 60 nm-thick Pd (e-beam evaporation), the suspended SU-8 layer collapsed on the substrate (in

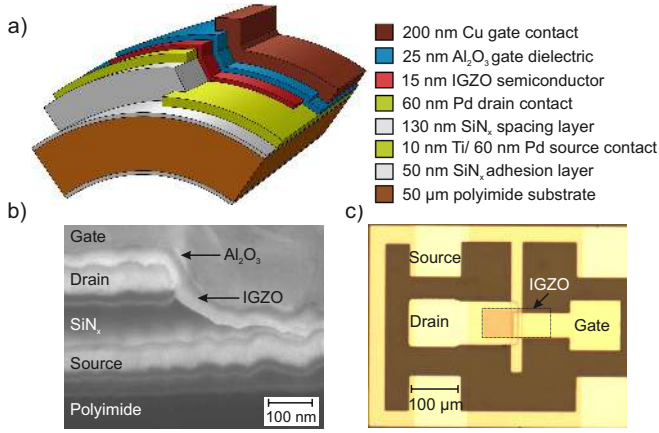

Figure 4.1: Flexible IGZO QVTFT with 300 nm channel length: a) schematic device cross section, b) SEM image of the focused ion beam (FIB) cross section through the channel, and c) optical micrograph.

the under-cut area) and SiN_x/Pd were uniformly deposited around the SU-8. The successive controlled rupture of the SiN_x layer during lift-off yielded a tilted sidewall with a length of 300 nm and a perfectly aligned Pd drain contact. Here, we chose Pd (as opposed to Au [111, 105]) as contact material, because it provides directly good adhesion to the other materials without the need of additional Cr [111] or Ti [105] layers, which are more prone to oxidation in ambient air. Subsequently, an IGZO layer (≈12 nm at the sidewall) was deposited by RF magnetron sputtering ($InGaZnO_4$ target) in a pure Ar atmosphere and patterned into islands by wet etching. The semiconductor was then electrically insulated by 25 nm Al_2O_3 (dielectric constant: 9.5) deposited by atomic layer deposition (ALD, 150 °C). Contact holes for source/drain electrodes were opened by wet etching. Finally, 200 nm Cu were e-beam evaporated (30° tilt), and patterned into gate contacts by wet etching. Fig. 4.1b displays the SEM picture of a focused ion beam (FIB) cross section through the QVTFT channel. The image shows how the quasi-vertical profile ensures a good coverage of the IGZO, Al_2O_3 and Cu layers. Fig. 4.1c displays a micrograph of the device, which uses a ground-signal-ground layout to allow AC measurements. The QVTFT presented has a length of 300 nm and a width of 55 µm. QVTFTs with

different lengths (220 nm-300 nm) can be realized by controlling the spacer thickness (95 nm-130 nm). Thinner or thicker SiN_x either results in large off-currents or non uniform rupturing of the SiN_x layer during lift-off. However, top-gate devices with longer channels can be integrated on the same substrate without additional lithography and deposition steps [105].

4.3 Results and Discussion

TFT characterization was performed under ambient conditions using an HP 8753E network analyzer and an Agilent technologies B1500A parameter analyzer. TFT performance parameters were extracted using standard MOSFET equations.

4.3.1 Electrical Performance

The transfer and output characteristics of the flexible IGZO QVTFT are shown in Fig. 4.2. The QVTFT exhibited well-shaped transfer characteristic and clear current saturation, with threshold voltage $V_{TH} = 1.5\,V$ and sub-threshold swing $SS = 0.4\,V/dec$. Gate current I_G is $<300\,pA$, which is 10^3 larger than standard values ($<0.1\,pA$) reported for planar IGZO devices [20]. The QVTFT yielded an on/off current ratio I_{ON}/I_{OFF} of 10^4, which is large enough for analog circuit applications. Nevertheless, this value is significantly lower compared to standard I_{ON}/I_{OFF} of $\approx 10^9$ of flexible small-channel planar IGZO TFTs [20]. This is due to the large I_{OFF} (2 nA) caused by leakage through the thin SiN_x spacing layer between source and drain contacts. Smaller I_{OFF} and therefore larger I_{ON}/I_{OFF} can be achieved by reducing the source/drain overlap. The saturation field-effect mobility μ_{SAT} was $0.2\,cm^2V^{-1}s^{-1}$, which is lower than the Hall mobility $\mu_H \approx 11.8\,cm^2V^{-1}s^{-1}$ of the IGZO layer and the mobility $\mu_{SAT} = 7.5\,cm^2V^{-1}s^{-1}$ of flexible small-channel planar IGZO TFTs [20]. This degradation was attributed to the high contact resistance at the IGZO/Pd interface. Even though Pd is known to form a Schottky barrier with IGZO sputtered at high O_2 partial pressures, if a pure Ar plasma is used (as in our case) an ohmic contact is expected [112]. The high normalized contact resistance $r_C = 45\,\Omega\,cm$, estimated based on the TFT DC and AC performance using the method described in [75], is expected to be originated from process-induced surface contamination of the Pd contacts. Similar contact resistance issues with even more pronounced effects were reported for IGZO VTFTs with n-

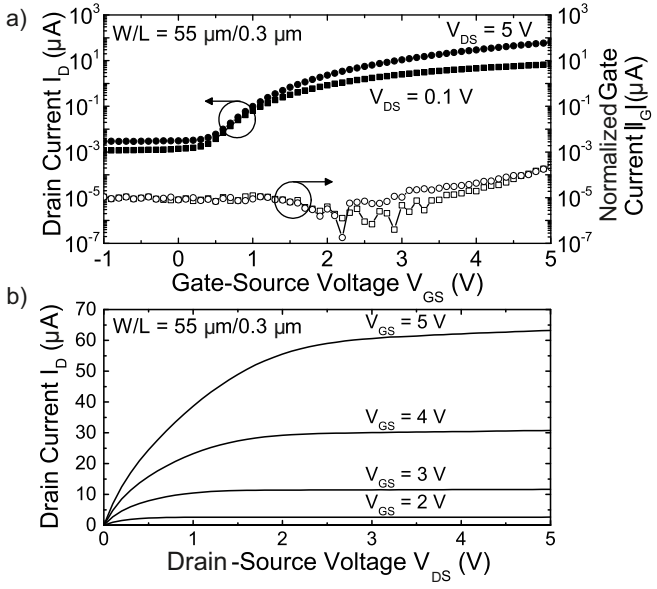

Figure 4.2: Transfer (a) and output (b) characteristics of a flexible IGZO QVTFT measured in the linear and saturation regime.

type Si [110] and Cr/Au/Cr [111] contacts. Nevertheless, the presented QVTFT yielded improved characteristics if compared to other flexible IGZO VTFTs [111, 109]. Future optimization of the source/drain contacts will allow larger μ_{SAT}. A way to achieve this is the use of sputtered Mo source/drain contacts, which were reported to form the lowest contact resistance with amorphous oxides [154]. From I_D-V_{GS} data (Fig. 4.2a), we derived a transconductance $g_m/W = 0.73\,\mu S\mu m^{-1}$ ($V_{GS} = 5\,V$, $V_{DS} = 5\,V$) (Fig. 4.3a). The improved g_m/W, compared to our previously reported value of $\approx 0.08\,\mu S\mu m^{-1}$ for IGZO VTFT with dry etched sidewall and Cr/Au/Cr contacts [111] is a result of the by a factor of ≈60 reduced r_C. The gate capacitance C_G (at 1 MHz) is displayed in Fig. 4.3b. The QVTFT presented a gate/source-drain overlap capacitance of $29\,fF\mu m^{-1}$ ($V_{GS} = -1\,V$s) and a total gate capacitance of $76\,fF\mu m^{-1}$ ($V_{GS} = 5\,V$). C_G is dominated by the capacitance of the overlap between gate and source/drain (17.8 µm), and between gate and IGZO (74 µm) (Fig. 4.1c). An optimized layout with reduced IGZO islands and channel length is expected to decrease C_G. Furthermore, the

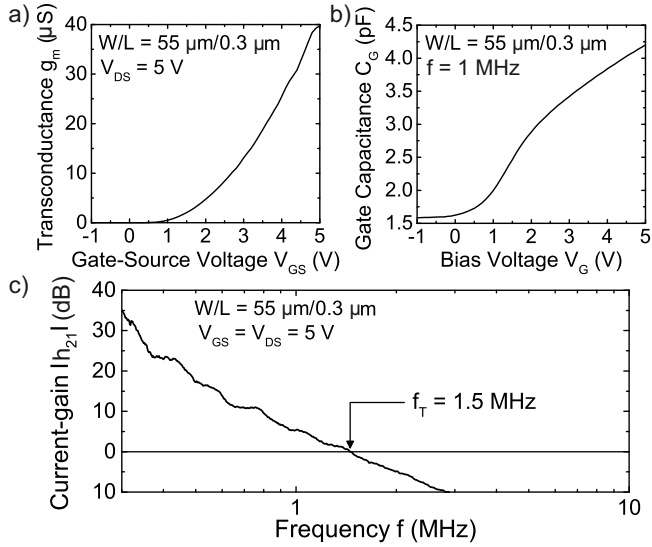

Figure 4.3: Transconductance (up to 5 V) (a), total gate capacitance (b), and measured current gain (c) of a flexible IGZO QVTFT.

use of a transparent ITO source contact [155] can potentially allow the self-alignment of the gate to the drain contact, and thus lead to smaller overlap capacitances. The frequency-dependent current gain h_{21} calculated from the S-parameters is plotted in Fig. 4.3c. From this plot, we derived a transit frequency f_T of 1.5 MHz, which nicely agreed with the f_T = 1.52 MHz calculated from g_m and C_G values. Due to improved g_m and C_G, our QVTFT exhibits a 19x enhanced f_T compared to our previously reported value of ≈80 kHz for IGZO VTFTs.

4.3.2 Bending

To demonstrate the QVTFT bendability, we wound the device around a cylindrical rod with 5 mm radius (tensile strain of 0.48 % parallel to the channel width). The QVTFT stayed fully functional when bent, and after re-flattening. The I_D-V_{GS} curve measured while flat and bent, as well as a photograph of the bent substrate is shown in Fig. 4.4. Bending to 5 mm radius changed μ_{SAT} by -5 % and V_{TH} by +126 mV. These values are comparable to previously published strain-induced

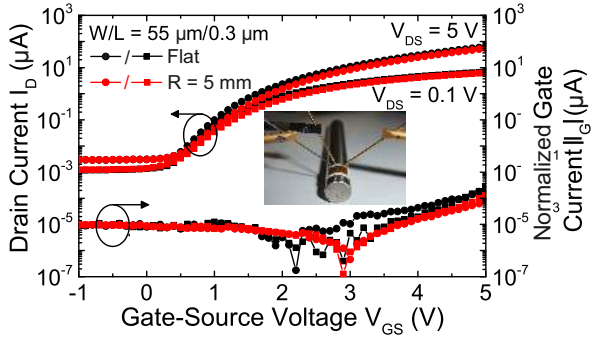

Figure 4.4: Transfer characteristic of a flexible IGZO QVTFT measured while flat and subsequently bent to a tensile radius of 5 mm (strain: 0.48 %).

shifts of IGZO VTFTs [111]. Bending to radii <5 mm was not possible, due to delamination of the Cu gate contact. The use of better adhering gate metals promises smaller radii.

4.4 Conclusion

A flexible IGZO QVTFT with 300 nm channel length was fabricated by a low temperature process <150 °C. A lift-off process to structure the SiN_x spacing layer and the Pd drain contact enabled the realization of a tilted sidewall on top of a Ti/Pd source electrode. Conformal coverage of the IGZO active layer, Al_2O_3 gate dielectric, and Cu gate electrode was possible thanks to the quasi-vertical profile of the underlying layers. Our QVTFT yielded an on/off current ratio of 10^4, a threshold voltage of 1.5 V, a maximum transconductance of 40 µS, and a transit frequency of 1.5 MHz. Furthermore, the flexible device remained functional even when bent to 5 mm radius. These results confirm QVTFTs as a promising technology for small-area bendable integrated circuits.

5

Solution-Processed TFTs and Circuits

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Low-temperature spray-deposited indium oxide for flexible thin-film transistors and integrated circuits

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Abstract

Indium oxide (In_2O_3) films were deposited by ultrasonic spray pyrolysis in ambient air and incorporated into bottom-gate coplanar and staggered thin-film transistors. As-fabricated devices exhibited electron-transporting characteristics with mobility values of $1\,cm^2V^{-1}s^{-1}$ *and* $16\,cm^2V^{-1}s^{-1}$ *for coplanar and staggered architectures, respectively. Integration of In_2O_3 transistors enabled realization of unipolar inverters with high gain (*5.3 V/V*) and low-voltage operation. The low temperature deposition (*≤250 °C*) of In_2O_3 also allowed transistor fabrication on free-standing* 50 μm*-thick polyimide foils. The resulting flexible In_2O_3 transistors exhibit good characteristics and remain fully functional even when bent to tensile radii of* 4 mm*.*

5.1 Introduction

Thin-film transistors (TFTs) based on transparent metal oxide semiconductors [156, 157] hold great promise for a host of future large-area, large-volume electronic applications including flexible radio-frequency identification (RFID) tags [3], flexible and paper-like displays [158], and electronic skin [159]. To this end, recent year have witnessed the development of a range of high-mobility metal oxide semiconductors and devices that can be manufactured over large areas employing simple and low-temperature fabrication methods [160]. Among the various deposition techniques demonstrated, solution processing offers a scalable and cost effective route for high throughput and large-area deposition of various oxide materials including ZnO, In_2O_3, and SnO_x to name a few [161, 74]. Among those, In_2O_3 –a simple binary metal oxide– has attracted an increasing interest in the last years owing to its large electron mobility (up to $160\,cm^2V^{-1}s^{-1}$ in single crystal device grown from vapor-phase at 1000 °C [162]) and the high optical transparency (>90 %) given by its wide band gap (~3.1 eV [162]). A significant advantage associated with the application of In_2O_3 in thin-film devices is that it can be grown at relatively low temperatures employing a diverse range of vapor-phase techniques [163, 164, 165], as well as solution-based methods [123, 166, 167, 125]. To date, solution-processed In_2O_3-based devices have been demonstrated by ink-jet printing [123] and spin-casting [167, 125, 168, 169]. Tremendous advances have been made to realize solution-processed TFTs at low temperatures (170-400 °C) with field effect electron mobility values ranging

from 0.01 $cm^2V^{-1}s^{-1}$ up to 44 $cm^2V^{-1}s^{-1}$ [123, 167, 125, 168, 169]. Despite the huge promise, however, accurate control over the morphology and the chemical composition of solution-grown In_2O_3 still remains very challenging, leading to significant device-to-device variations. Recently spray pyrolysis (SP) has demonstrated to be a particularly appealing technology, enabling a simple and scalable deposition of a large variety of oxide semiconductors, from n-type ZnO [170, 171], IZO [172], ZTO [173], and Ga_2O_3 [174] to p-type Cu_xO [175]. Furthermore, addition of suitable dopants in the precursor solution has also allowed the demonstration of Be-doped ZnO transistors and integrated circuits with optimized operating characteristics [176]. Despite the tremendous potential, however, deposition of semiconducting metal oxides by spray pyrolysis has so far been limited to high processing temperatures typically in the excess of >350 °C, hence rendering the technology incompatible with inexpensive, temperature-sensitive substrate materials such as plastic. In order to overcome this rather serious bottleneck, development of new material formulations and optimized processing protocols would be needed.

Here, we report the development of low-voltage In_2O_3-based TFTs and inverters using ambient ultrasonic spray pyrolysis (SP) and indium nitrate hydrate as the precursor. Optimal process conditions enable the growth of high-quality electron-transporting In_2O_3 layers and the realization of low-voltage bottom-gate, bottom-contact (BG-BC) as well as bottom-gate, top-contact (BG-TC) TFTs with electron mobility of ~1 $cm^2V^{-1}s^{-1}$ and ~16 $cm^2V^{-1}s^{-1}$, depending on the particular device configuration employed. Use of the application relevant BG-BC transistor architecture allows the fabrication of fully functional unipolar inverters with excellent operating characteristics. Finally, by taking advantage of the moderate process temperature (~250 °C), fabrication of fully functional and bendable In_2O_3-based TFTs on plastic substrate is also demonstrated. Although the use on In-based oxide semiconductors may ultimately prove expensive for application in future large-volume electronics due to the scarcity of In, our work highlights the potential of spray pyrolysis as a viable large-area deposition tool even for plastic microelectronics.

5.2 Device Structure and Fabrication

Bottom-gate coplanar transistors were fabricated on a 4-in. silicon substrate with 1 μm thermally grown SiO_2 acting as isolation layer. Fig. 5.1a shows the schematic device cross section. The substrate was covered by 500 nm of SiN_x grown via Plasma-enhanced chemical vapor deposition (PECVD). Next, 30 nm-thick e-beam evaporated Cr was structured into bottom-gate contacts using standard photolithographic etching. Following, a 50 nm thick Al_2O_3 gate dielectric layer (dielectric constant: 9.5) was deposited by atomic layer deposition (ALD) at 150 °C. Gate contact holes through the Al_2O_3 were patterned by photolithography and wet chemistry [103]. Subsequently, 10 nm/60 nm of Ti/Au were e-beam evaporated and structured into source/drain (S/D) contacts using a lift-off process. Prior to the semiconductor deposition, the substrate was diced into chips of 1.5 x 1.5 cm^2. The diced chips were then cleaned by ultra-sonication in acetone and IPA for 5 min, and submitted to 30 min UV/ozone treatment. The In_2O_3 deposition was carried out by ultrasonic spray pyrolysis using a 30mg/mL indium nitrate hydrate ($In(NO_3)_3{\cdot}H_2O$) in deionized water solution. The deposition was performed in ambient air at 250 °C. The resulting transistors have channel length (L) and width (W) of 10 μm and 500 μm, respectively. Bottom-gate, staggered transistors (Fig. 5.1b) were fabricated onto doped Si^{++} wafers acting as the common gate electrode with a 400 nm-thick SiO_2 layer as the gate dielectric. In_2O_3 was processed using the identical protocols followed by the thermal evaporation of top Al source/drain electrodes in high vacuum (10^{-6} mbar).

5.3 Results and Discussion

X-ray diffraction (XRD) in Bragg-Brentano geometry were performed using a Bruker D8-Advance X-ray diffractometer. The surface morphology of the films was investigated by intermittent contact mode atomic force microscopy (AFM). Electrical measurements were performed in nitrogen atmosphere using a semiconductor parameter analyzer. Finally, the charge carrier field-effect mobility values were extracted using the standard gradual channel approximation model [177].

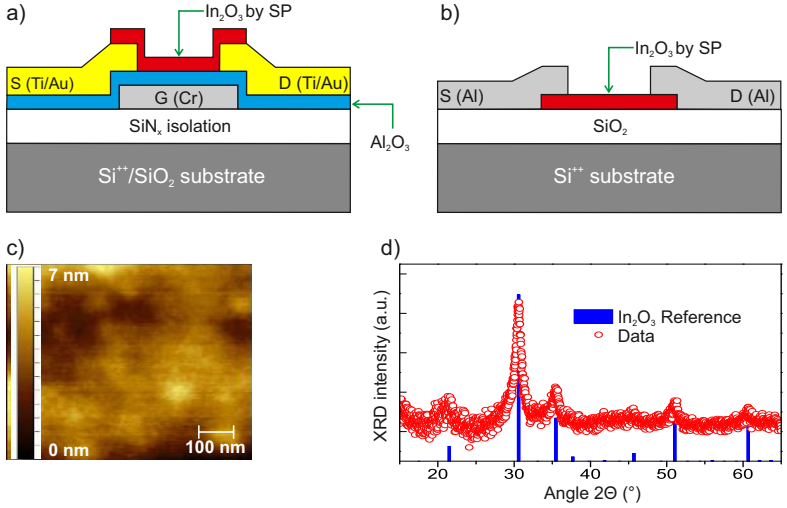

Figure 5.1: Schematic cross sections of a) the coplanar, bottom-gate, bottom contact and b) staggered bottom-gate, top-contact indium oxide (In_2O_3) TFTs fabricated on Si/SiO_2 substrates. c) AFM surface topography image of an In_2O_3 film processed on $Si/SiO_2/SiN_x/Cr/Al_2O_3$ substrate. d) XRD diffraction patterns of spray-deposited In_2O_3 layers in comparison with peak positions of reference powder diffraction file (JCPDS-PDF 06-0416).

5.3.1 In_2O_3 Characterization

Fig. 5.1c shows a representative AFM image of the surface topography of a ~15 nm-thick In_2O_3 film processed on a Si^{++}/SiO_2 substrate by ultrasonic SP in air. The film appears continuous and extremely smooth with a root mean square (rms) surface roughness of ~1.1 nm. To investigate whether the as-process In_2O_3 films are amorphous, we performed XRD measurements on the same films. Fig. 5.1d displays the measured XRD spectrum of a ~15 nm-thick spray-deposited In_2O_3 layer together with the reference powder diffraction file (JCPDS-PDF 06-0416) for comparison. It can be seen that In_2O_3 films are clearly polycrystalline as the diffraction peaks are in good agreement with the reference powder diffraction data. The mean crystallite size was also calculated from the (222) peak at around 30.5° using the Scherrer method yielding a value of ~9.3 nm.

5.3.2 Rigid In_2O_3 TFTs

In order to investigate the charge transport properties of as-deposited In_2O_3 films, we fabricated coplanar BG-BC transistors (Fig. 5.1a) and electrically characterize them in nitrogen at room temperature. Fig. 5.2a and 5.2b display representative sets of the output and transfer characteristics measured for an In_2O_3 TFT, respectively. All devices operate at low voltages ($\leq$8 V) and exhibit electron transporting (n-channel) behaviour with clear channel current saturation. The devices show current on/off ratio (I_{ON}/I_{OFF}) of $>10^4$, threshold voltage (V_{TH}) around ~2.5 V, sub-threshold swing (SS) of ~0.9 V/dec, and linear (μ_{LIN}) and saturation (μ_{SAT}) field-effect mobilities of 0.6 $cm^2V^{-1}s^{-1}$ and 1.25 $cm^2V^{-1}s^{-1}$, respectively. The mobility values obtained here are generally lower than values reported previously for solution-processed In_2O_3 transistors with comparable high-k dielectrics [167, 125]. This is primarily attributed to the unfavorable coplanar BG-BC transistor architecture and the high work function gold S/D electrodes (-5 eV) used [178]. When similar spray-deposited In_2O_3 channel layers were employed in staggered bottom-gate, top-contact (BG-TC) device structures (Fig. 5.1b) in combination with low work function Al S/D electrodes, the electron mobility reached values up to 16 $cm^2V^{-1}s^{-1}$ (Fig. 5.2c). Although the latter value is approximately one order of magnitude lower than the Hall electron mobilities reported for single crystals of In_2O_3 prepared at 1000 °C [162], it is amongst the highest field-effect mobilities reported to date for In_2O_3 TFTs prepared from solution at comparable temperatures. Despite the improved performance, however, the staggered BG-TC device architecture is not practical for use in integrated circuits due to the significant complexity associated with the manufacturing and the chemically unstable nature of the low work function Al electrodes.

5.3.3 Rigid In_2O_3 Circuits

Because of these practical issues, we explored the use of coplanar BG-BC In_2O_3 TFTs for fabricating integrated circuits such as unipolar logic NOT gates (Fig. 5.3). Preliminary discrete transistor characterization was used to design NOT gates with centered midpoint voltage $V_M \approx V_{DD}/2$. The inset in Fig. 5.3 displays the schematic diagram of the inverter. The circuit comprises one driving In_2O_3 TFT with W/L of 1400/20 μm and one passive load resistor R = 160 kΩ. The inverter was fabricated with the same process used for single TFTs, with the

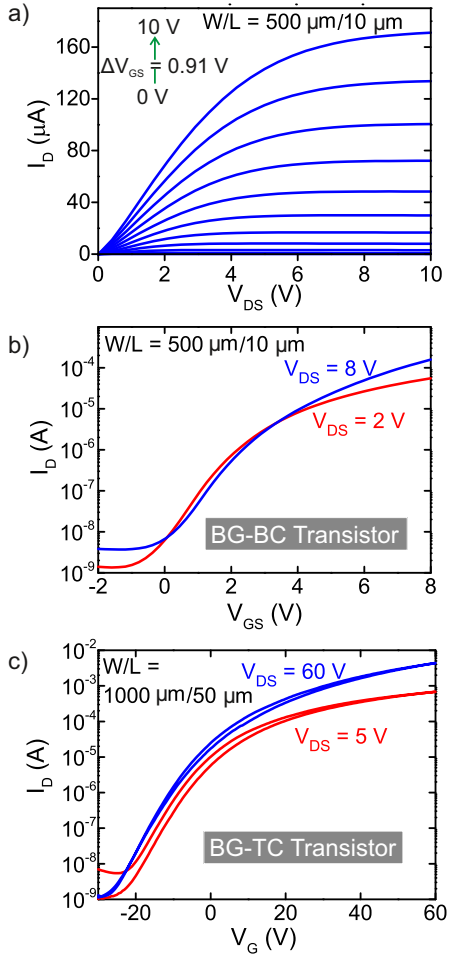

Figure 5.2: a) Output and b) transfer characteristic of a coplanar bottom-gate, bottom-contact In_2O_3 TFT fabricated on Si/SiO_2 substrate by spray pyrolysis in air. The channel dimensions for this device were W/L = 500 µm/10 µm. c) Representative transfer characteristics measured for a staggered bottom-gate, top-contact In_2O_3 TFT fabricated on Si/SiO_2 employing Al S/D electrodes. The channel dimensions for this device were W/L = 1000 µm/50 µm.

exception that the circuit interconnect lines were integrated directly into the source/drain metallization layer. The required resistor was implemented using the gate metal (Cr, 1.16 x $10^{-6}\,\Omega\,m$), thereby no additional process steps were needed. Fig. 5.3a and Fig. 5.3b show the voltage transfer characteristic (VTC) and the corresponding gain of the unipolar inverter measured at different supply voltages (V_{DD}) of 4, 6, 8, and 10 V. The inverter exhibits a gain >2, even at a low V_{DD} = 4 V. At V_{DD} = 10 V, the inverter yields an almost centered V_M = 5.8 V, and a gain as high as 5.3 V/V. Furthermore, the circuits show good output swing (output high voltage V_{OH} = 9.8 V and output low voltage V_{OL} = 1.1 V) and wide noise margins (noise margin high NM_H = 3.1 V and noise margin low NM_L = 3.68 V).

5.3.4 Flexible In_2O_3 TFTs

To demonstrate the compatibility of spray-deposited In_2O_3 TFTs with temperature-sensitive substrate materials such as plastic, we fabricated BG-BC In_2O_3-transistors directly onto polyimide (PI) foils. We have chosen 50 μm-thick Kapton PI because of its stability against the chemicals used during device fabrication, its relatively low surface roughness (rms ~ 4 nm), the low thermal (12 x 10^{-5} K) and humidity (9 x 10^{-6} % RH) expansion coefficients, and its high glass transition temperature (T_G ~ 360 °C) [20, 179]. The TFT fabrication on foil followed the same process steps employed on Si/SiO_2 substrates. The inset in Fig. 5.4 shows the schematic device cross section of the flexible In_2O_3 TFTs. To provide a sufficient adhesion of the Cr gate metal and the Al_2O_3 gate dielectric to the polyimide, a 50 nm-thick SiN_x was deposited on both sides of the foil by PECVD. Additionally, during the spray pyrolysis process, the flexible chip was mechanically clamped on the border by employing a heavy stencil mask (mass of ~ 30g). A typical set of transfer characteristics for a flexible In_2O_3 TFT (W = 1400 μm and L = 20 μm) is shown in Fig. 5.4a. Flexible In_2O_3 TFTs exhibit good operating characteristics with an I_{ON}/I_{OFF} = 6 x 10^3 (I_{OFF} < 20 nA), V_{TH} = 5.29 V, and μ_{SAT} = 0.2 $cm^2V^{-1}s^{-1}$. The lower on/off current ratio and electron mobility of flexible TFTs, compared to devices made on Si/SiO_2 substrates, are most likely attributed to the comparatively lower thermal conductivity of the polyimide, which limits the precursor conversion during the spray process as well as the increased dielectric/semiconductor interface roughness.

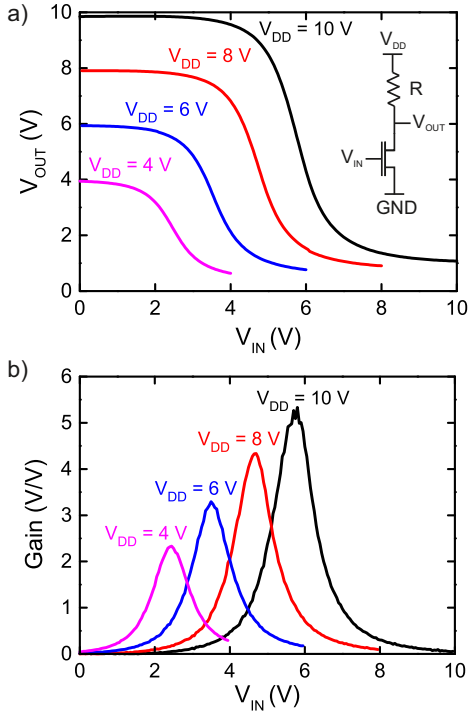

Figure 5.3: a) Voltage transfer characteristic of an In_2O_3-based unipolar voltage inverter (NOT gate) on Si/SiO_2 substrate, measured at different supply voltages (V_{DD}). The inset shows a schematic of the inverter circuitry used. The inverter comprises a driving In_2O_3 TFT with W = 1400 µm and L = 20 µm and a passive load with resistance R = 160 kΩ. b) Corresponding gains calculated from the voltage transfer characteristics.

Bendability: Beside electrical performance, the mechanical flexibility of future TFT technologies is also expected to be a determinant factor for widespread application of the technology in flexible microelectronics. In an effort to test the effect of mechanical stress on the operating characteristics of our spray deposited In_2O_3 TFTs, discrete devices were attached to double-sided tape and wound around a metallic rod of 4 mm radius, in a configuration that tensile strain was applied parallel to the TFT channel. Fig. 5.4a shows the transfer

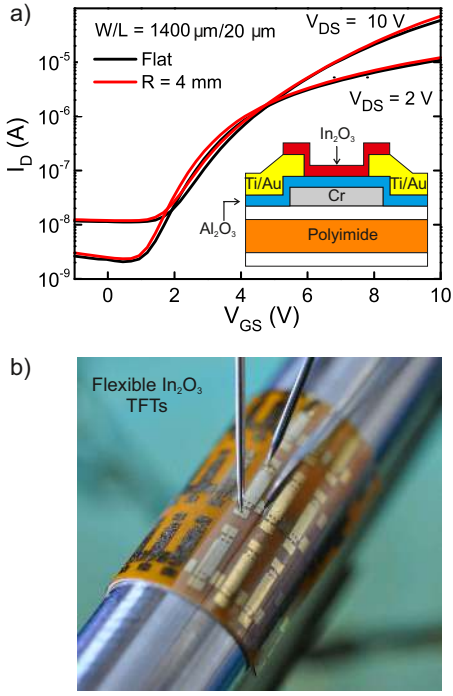

Figure 5.4: a) Transfer characteristics of spray-deposited In_2O_3 TFT fabricated on free-standing flexible polyimide foil, measured while flat and bent to a tensile radius of 4 mm. The inset shows the schematic device cross section. The TFT dimensions are W = 1400 µm and L = 20 µm. b) Photograph of the actual flexible In_2O_3 TFT bent to a tensile radius of 4 mm.

characteristic for a typical device measured (in nitrogen) while flat and subsequently bent to a tensile radius 4 mm, which corresponds to a mechanical strain (ϵ) of ~ 0.65 % [87]. Fig. 5.4b displays a photograph of the actual TFT bent to 4 mm radius and contacted with the probe needles. From these measurements, it can be seen that flexible In_2O_3 TFTs are fully operational even when strained to 0.65 % with only minor changes in the operating characteristics that are manifested as a negative shift in V_{TH} of -230 mV and an increased μ_{SAT} by 13 %. These reversible variations are most likely related to an increase in the elec-

tron mobility and hence conductivity of In_2O_3 induced under tensile strain. This finding is in good agreement with previous reports on flexible transistors based on IGZO and IZO [106, 129]. Bending to smaller radii induces cracks in the brittle Cr gate that permanently harm the device operation [45]. These results demonstrate the potential of ultrasonic spray pyrolysis as a simple and scalable deposition tool for the manufacturing of flexible oxide microelectronics and certainly pave the way to future development. Combination of new precursor materials and formulations combined with improved device architectures is anticipated to lead to devices and circuits with improved performance.

5.4 Conclusion

In summary, we have demonstrated n-channel In_2O_3 transistors and unipolar circuits in which the semiconducting layer was deposited by ultrasonic spray pyrolysis at 250 °C. This simple and scalable method enables the fabrication of discrete transistors as well as unipolar inverters with appreciable gain (>5 V/V) and low voltage operation (<10 V). The moderate deposition temperature of 250 °C used for the growth of In_2O_3 renders the method compatible with low-cost plastic substrates. This is demonstrated with the fabrication of In_2O_3 transistors on free-standing 50 μm-thick flexible polyimide foils, which exhibit good operating characteristics even when bent to 4 mm tensile radii ($\epsilon \sim 0.65\,\%$).

6

Memory TFTs

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Influence of Mechanical Bending on Flexible InGaZnO-Based Ferroelectric Memory TFTs

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10.1109/TED.2014.2304307

Abstract

Future flexible electronic systems require memory devices combining low-power operation and mechanical bendability. Here, we present a mechanically flexible amorphous InGaZnO (a-IGZO) memory thin-film transistor (TFT) with a ferroelectric poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] gate dielectric. Memory operation is demonstrated with a memory window of 3.2 V *and a memory on/off ratio of* 1.5 *x* 10^6 *(gate-source voltage sweep of* ±6 V*). The measured mobility of* 8 $cm^2V^{-1}s^{-1}$ *and the on/off current ratio of* 10^7 *are comparable to the values for reference TFTs fabricated on the same substrate. To use memory TFTs in flexible applications, it is crucial to understand their behavior under mechanical strain. Flexible memory and reference TFTs are characterized under bending radii down to* 5.5 mm*, corresponding to tensile and compressive strain of* ≈±0.6%*. For both memory and reference TFTs, tensile strain causes negative threshold voltage shifts and increased drain currents, whereas compressive strain results in the opposite effects. However, memory TFTs, compared with reference TFTs, exhibit up to* 8× *larger threshold voltage shifts and* 17× *larger drain current variations. It is shown that the strain-dependent properties of a-IGZO can only explain the shifts observed in reference TFTs, whereas the variations in memory TFTs are mainly caused by the piezoelectric properties of P(VDF-TrFE).*

6.1 Introduction

Electronic devices fabricated on plastic substrates enable new applications, such as flexible radio-frequency identification (RFID) tags [3], sensor arrays [180], paper-like displays [181] or smart textiles [2]. Several of these electronic systems require non-volatile memory devices, combining mechanical flexibility and low-power dissipation [182]. Recently, thin-film transistors (TFTs) employing a ferroelectric material as gate dielectric have promised to enable such devices [183, 184]. Among the various ferroelectric materials, the co-polymer poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] is the most-suited, due to the high spontaneous polarization of 50-100 mC/m^2 and the process temperature <140 °C [139]. The ferroelectric properties of P(VDF-TrFE) originate from the intrinsic dipole moments of the molecules that orient themselves according to an externally applied electric field and maintain their orientation when the field is turned off [184]. In a ferroelectric TFT (Fe-TFT), the bistable polarization of the ferroelectric gate

dielectric is used for memory operation. Depending on the orientation of the polarization, positive or negative charges are stored at the semiconductor/gate dielectric interface, leading to a charge carrier density modulation in the semiconductor. The corresponding variation in the drain current can be used to define the binary <0> and <1> states of the memory [185]. Several groups have reported Fe-TFTs using organic semiconductors as channel material [183, 186, 187, 188, 182]. However, organic Fe-TFTs exhibit field effect mobilities $\leq 1\,\mathrm{cm^2V^{-1}s^{-1}}$ and poor ambient stability [189]. To overcome these limitations, various metal oxide-based Fe-TFTs using Zinc-Oxide [190, 188], Zinc-Indium-Oxide [146], Aluminum-Zinc-Tin-Oxide [145] and Indium-Gallium-Zinc-Oxide (IGZO) [191, 144, 141, 142] channel layers have been demonstrated. Amorphous IGZO (a-IGZO) is especially suitable for the fabrication of devices on temperature-sensitive plastic substrates, due its relative high carrier mobility around $10\,\mathrm{cm^2V^{-1}s^{-1}}$ and the high ambient stability, even if deposited at room temperature [10]. Very recently, flexible IGZO-based Fe-TFTs with retention time of 12 days [142] and mechanical flexibility down to a tensile bending radius of 7 mm [141] have been presented. However, to our best knowledge, the influence of tensile and compressive strain on a-IGZO Fe-TFTs has not yet been reported.

Here, we present the results of bending experiments to measure the electrical characteristics of a-IGZO Fe-TFTs under applied tensile and compressive strain down to radii of 5.5 mm. We also compare the effect of mechanical strain for Fe-TFTs and reference TFTs fabricated on the same substrate, and show that the increased influence of bending on Fe-TFTs, compared to reference TFTs is due to the piezoelectric properties of the P(VDF-TrFE) layer.

6.2 Fabrication Process

Reference TFTs and Fe-TFTs were fabricated on a free-standing flexible 50 µm-thick Kapton E polyimide foil (surface area = 7.6 cm × 7.6 cm). Fig. 6.1 shows the geometry of a: a) top-gate bottom-contact staggered a-IGZO reference TFT and b) a-IGZO memory TFT with a ferroelectric P(VDF-TrFE) layer. First, the polyimide substrate was cleaned by sonication in acetone and isopropanol for 5 min and then preshrunk in a vacuum oven at 200 °C for 24 h. Next, 50 nm-thick SiN_x acting

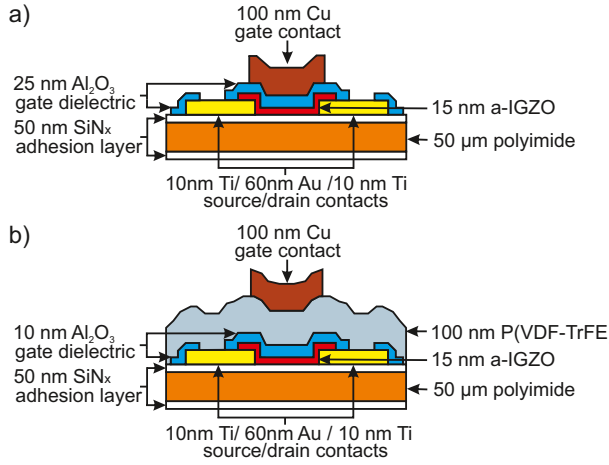

Figure 6.1: Schematic cross section of: a) top-gate bottom-contact staggered a-IGZO reference TFT, b) memory TFT with a ferroelectric P(VDF-TrFE) layer.

as adhesion layer was deposited on each side of the substrate using plasma-enhanced chemical vapor deposition (PECVD). Subsequently, 10 nm/60 nm/10 nm Ti/Au/Ti were e-beam evaporated and structured (photolithographic mask 1) into source/drain contacts using a lift-off process. Then, 15 nm a-IGZO was deposited at room temperature using RF magnetron sputtering. Sputter deposition was performed in a pure Ar atmosphere using a ceramic $InGaZnO_4$ target. Semiconductor islands were patterned by photolithography (mask 2) and wet etching [192]. To fabricate reference TFTs and Fe-TFTs on the same substrate, the polyimide foil was halved. On the first half, the IGZO islands of the reference TFTs were isolated from the successive top-gate using 25 nm Al_2O_3 (relative dielectric constant of ≈9.5) deposited by atomic layer deposition (ALD) at 150 °C. On the other half, the IGZO islands of the Fe-TFTs were isolated by a 10 nm-thick Al_2O_3 dielectric layer deposited by ALD. This Al_2O_3 buffer layer guarantees a similar interface in reference TFTs and Fe-TFTs and at the same time reduces the gate leakage currents in Fe-TFTs [144]. In both cases, source/drain contact holes were opened by standard lithography (mask 3) and wet chemistry [103]. For the fabrication of the Fe-TFTs, 100 nm-thick P(VDF-TrFE) was formed by spin-coating a solution of 1 wt% VDF (70 mol%) and TrFE (30 mol%)

in Methyl-Ethyl-Ketone (MEK) [193]. The deposited film was crystallized at 140 °C for 15 min in ambient air. The thickness and the recipe of the P(VDF-TrFE) layer were optimized to obtain Fe-TFTs with low-voltage operation <10 V [193, 191]. Finally, on both reference TFTs and Fe-TFTs, 200 nm of Cu were e-beam evaporated by tilting the substrate by 30°, and patterned in gate contacts using lithography (mask 4) and wet etching. After the etching, the unexposed photoresist was removed by a flood exposure and a successive development step, to avoid any damage of the P(VDF-TrFE) layer. Here, the use of the Al_2O_3 layer allowed utilizing an acid-based wet etchant to structure the Cu, without the risk of diffusing through the P(VDF-TrFE) layer down to the IGZO [144], and thus damaging the channel area. The maximum process temperature was 150 °C.

The reference TFTs have a W/L = 280 μm/115 μm, whereas the Fe-TFTs have a W/L = 1400 μm/20 μm to partially compensate for the different gate capacitance per area (C_G). TFT masks were designed to allow cutting the process substrate into stripes with one TFT per stripe.

6.3 Characterization

The devices were characterized under ambient conditions using an Agilent technologies B1500A parameter analyzer. The transfer curves were measured in the linear region, to minimize the influence of the drain-source voltage V_{DS} on the ferroelectric polarization of the Fe-TFT [193]. TFT performance parameters were extracted from the drain current using standard MOSFET equations [177]. The linear field-effect mobility μ_{LIN} was calculated from the slope of the drain current I_D (at V_{DS} = 0.1 V), using the value of C_G extracted from C-V measurements. With respect to later memory applications, the threshold voltage V_{TH} was defined as the gate-source voltage V_{GS} needed to reach an arbitrary drain current value. We selected a value $I_D = 5 \times 10^{-8}$ A, that could be easily measured by the parameter analyzer and marked the sub-threshold region in both reference TFTs and Fe-TFTs.

6.3.1 Reference TFTs

Fig. 6.2a shows the transfer characteristic of a flexible a-IGZO reference TFT, measured with a single sweep of V_{GS} from 4 V to −2 V, at V_{DS} = 0.1 V. When measured with a double sweep of V_{GS}, reference TFTs present a clockwise hysteresis <25 mV. The performance param-

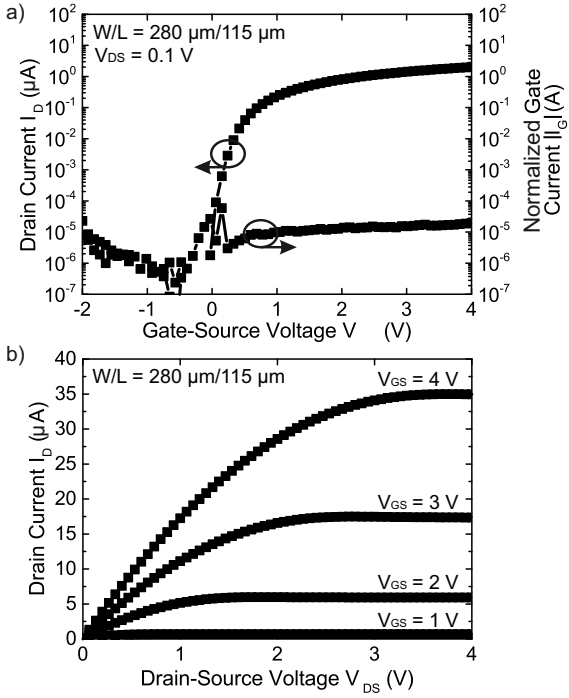

Figure 6.2: Flexible a-IGZO reference TFT: a) transfer characteristic (measured at V_{DS} = 0.1 V) and b) output characteristic.

eters are: linear field-effect mobility μ_{LIN} = 7.5 $cm^2V^{-1}s^{-1}$, V_{TH} = 0.3 V, on/off current ratio I_{ON}/I_{OFF} = 2.2×10^7, and sub-threshold swing SS = 106 mV/dec. The gate leakage current I_G is smaller than 10^{-10} A. These parameters are comparable to those achieved for flexible bottom-gate a-IGZO TFTs employing the same gate stack materials [45]. The output characteristic is given in Fig. 6.2b. It shows that I_D saturates for $V_{DS} > V_{GS}$-V_{TH}.

6.3.2 Ferroelectric TFTs

Fig. 6.3a shows the transfer characteristic of a flexible a-IGZO Fe-TFT, measured with a double sweep of V_{GS} between −6 V and 6 V, at V_{DS} = 0.1 V. The ferroelectric-driven memory operation is demonstrated by

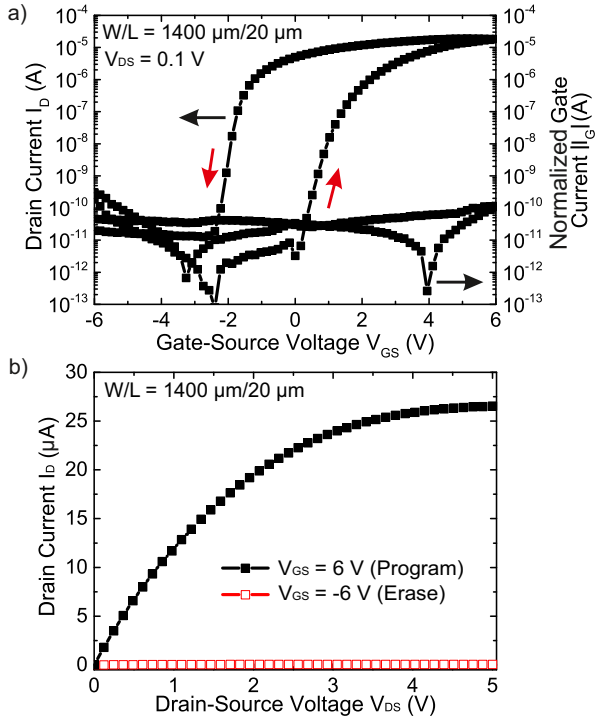

Figure 6.3: Flexible a-IGZO ferroelectric TFT: a) hysteretic transfer characteristic (measured at V_{DS} = 0.1 V). Indicated red arrows describe the direction of the transfer curves measured with a double sweep of V_{GS} between −6 V and 6 V. b) Output characteristic (measured at a V_{GS} = 0 V), after V_{GS} has been swept from 0 V to 6 V (black), and from 0 V to −6 V (red).

the counter-clockwise hysteresis of I_D, as shown by the red arrows in Fig. 6.3a. Due to the hysteresis, the transfer characteristic presents two branches, corresponding to the forward (V_{GS} from -6 to 6 V) and the reverse (V_{GS} from 6 to -6 V) sweep. This leads to two different values of V_{TH} of 1.3 V (forward) and −1.9 V (reverse). The memory window MW, which is defined as the difference of V_{TH} under the forward and the reverse operation, is therefore 3.2 V. The memory on/off ratio, which is the ratio between the memory on-value $I_{D,REV}$ (V_{GS} = 0 V) and off-value $I_{D,FOR}$ (V_{GS} = 0 V) is 1.5 x 10^6. It is worth mentioning that due to

the symmetry of the hysteretic transfer curve, the two memory states stored in the Fe-TFTs can be read-out at V_{GS} = 0 V. The Fe-TFTs exhibit: μ_{LIN} = 8 $cm^2V^{-1}s^{-1}$, on/off current ratio =1.7 x 10^7, and SS = 152 mV/dec. The I_G is confirmed to be smaller than 10^{-10} A. These parameters are comparable to those of previously reported flexible a-IGZO Fe-TFTs [141, 142]. Additionally, the values of linear mobility and on/off current ratio are comparable to those extracted from reference TFTs (Table 6.1). The 43% larger SS (Table 6.1) of Fe-TFTs, compared to reference TFTs, is due to the by 82% smaller C_G of Fe-TFTs (Table 6.1) [177]. Fig. 6.3b displays the output characteristic, measured at V_{GS} = 0 V, after V_{GS} has been swept from 0 V to 6 V (set memory state <1>) and from 0 V to −6 V (set memory state <0>). The I_D-V_{DS} curves clearly show the memory effect of our devices, with I_D changing from an off- to an on-state depending on the previously applied V_{GS}.

Programming and retention characteristics of our flexible Fe-TFTs were also evaluated. The memory states were programmed with V_{GS} pulses of 6 V (set memory state <1>) and -6 V (set memory state <0>) applied for 1 s. An initial memory on/off ratio of more than 10^3 (at V_{GS} = 0 V) was obtained, and it still remained to be more than 50 after 100 sec. This is comparable to previous reports on oxide semiconductor-based Fe-TFTs with Al_2O_3/P(VDF-TrFE) gate dielectric [145, 146]. Such low values can be explained considering that the Al_2O_3 buffer layer induces depolarization in the ferroelectric P(VDF-TrFE) layer [188]. Very recently, it has been shown that Fe-TFTs without buffer layer and with high-quality P(VDF-TrFE) exhibit retention times of 12 days, and at the same time gate leakage current <2 nA [142]. However, for the aim of this paper, the Al_2O_3 layer was still employed to ensure comparability between reference TFTs and Fe-TFTs.

6.4 Mechanical Bending

6.4.1 Setup

In order to measure the influence of bending in a reliable way, we designed our masks in a way that the process substrate could be cut into stripes (4.8 mm x 35 mm) with one TFT/Fe-TFT per stripe. On each stripe, the electrodes of the TFTs/Fe-TFTs were connected to 1 cm-long interconnect lines leading to 3 mm x 3 mm-large contact pads. To perform bending experiments, each TFT/Fe-TFT was attached to a

Table 6.1: Performance parameters of a flexible reference TFT (W/L = 280 μm/115 μm) and a ferroelectric TFT (W/L = 1400 μm/20 μm)

Parameter	Reference TFT	Ferroelectric TFT
Linear mobility ($cm^2V^{-1}s^{-1}$)	7.5	8
Threshold voltage (V)	0.3	1.3 (forward) −1.9 (reverse)
Sub-threshold swing (mV/dec)	106	152
On-off current ratio	2.2×10^7	1.7×10^7
Gate capacitance per area (Fm^{-2})	3.36×10^{-3}	5.9×10^{-4}

reusable flexible carrier substrate with Cu interconnections and pads, using double-sided tape. Next, the contact pads on the stripe were electrically connected to the interconnections on the carrier substrate using conductive adhesive and Cu wires [106] (Fig. 6.4a). Interconnections on the carrier substrates were subsequently connected to the parameter analyzer to to be able to constantly monitor the device characteristics at any arbitrary bending radius, without the need of placing probe tips. Afterward, the carrier substrate with the attached TFT/Fe-TFT was placed between two movable plates in our custom build bending tester (Fig. 6.4b). The substrate was positioned with the Fe-TFT/TFT facing upward (downward) to apply tensile (compressive) strain parallel to the channel length. The actual bending radius was defined by moving the plates, and was measured by fitting circles to images taken by an optical camera. The TFTs/Fe-TFTs were then characterized at different tensile and compressive radii down to 5.5 mm. This radius was selected to avoid breaking of the TFTs/Fe-TFTs at smaller radii. After each measurement at a specific radius and before moving to a new radius, a 5 min interval was waited in order to minimize the influence of electrical stress.

6.4.2 Reference TFTs

The applied bending radii range from infinity (flat substrate) to 5.5 mm, which correspond to tensile strain (ϵ) from 0.09 % to 0.64 % and compressive strain from -0.04 % to -0.59 %, due to the strain built-in the substrate. The strain values are calculated by adapting the strain theory developed in [87] to the layer structure of our TFTs. During the

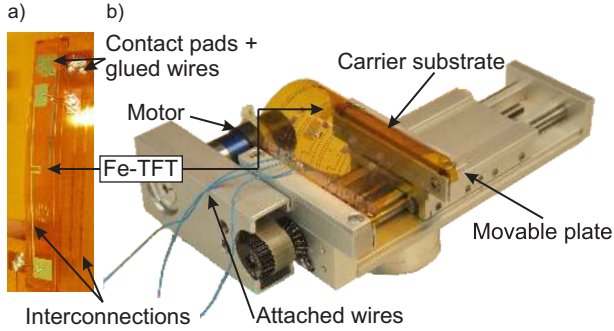

Figure 6.4: Photograph of: a) Fe-TFT attached to flexible carrier substrate and connected to interconnections, b) carrier substrate with attached Fe-TFT loaded in our custom-built bending tester and bent to a radius of ≈18 mm. The Fe-TFT is loaded to apply tensile strain parallel to the channel.

bending experiments, the reference TFTs were measured with a single sweep of V_{GS} from 4 V to −2 V, at V_{DS} = 0.1 V. Fig. 6.5 shows the transfer characteristics of a flexible reference TFT, measured when it is initially flat, and when it is bent to a tensile radius of 5.5 mm, and then to a compressive radius of 5.5 mm. As expected, the curve shifts in the opposite directions for tensile and compressive bending. After re-flattening, the reference TFTs are fully operational, whereas bending to radii <4 mm induces cracks in the TFT channel that permanently harm the devices. Fig. 6.6 displays: a) the normalized maximum drain current $I_{D,MAX}$ (measured at V_{GS} = 4 V and V_{DS} = 0.1 V) and b) the threshold voltage shift ΔV_{TH} versus applied strain (tensile and compressive). $I_{D,MAX}$ is normalized by its measurement at flat substrate, whereas ΔV_{TH} is given by the difference to the measurement at flat substrate. For tensile strain ϵ of 0.64 %, $I_{D,MAX}$ increases by 10 % and V_{TH} shifts by -90 mV. Compressive strain (ϵ = -0.59 %) on the other hand results in a decrease of $I_{D,MAX}$ by 11 % and a positive shift of V_{TH} by 90 mV. These values are in good agreement with previous reports on flexible a-IGZO bottom-gate [106, 147, 45] and top-gate [148] TFTs. Under tensile bending, the increased $I_{D,MAX}$ and the negative ΔV_{TH} are explained by the strain-induced increase of the IGZO mobility and carrier density. Compressive bending instead leads to a reduction of the mobility and channel conductivity, resulting thus in a decreased

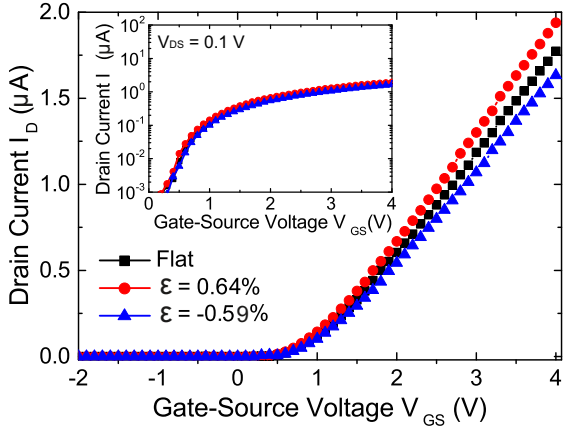

Figure 6.5: Transfer characteristics of a flexible a-IGZO reference TFT (W/L = 280 µm/115 µm), measured flat, bent to a tensile radius of 5.5 mm (ϵ = 0.64 %) and bent a compressive radius of 5.5 mm (ϵ = −0.59 %). All transfer characteristics are measured at V_{DS} = 0.1 V. (Inset) Enlargement of transfer characteristics in logarithmic scale.

$I_{D,MAX}$ and a positively shifted V_{TH} [106].

6.4.3 Ferroelectric TFTs

Fe-TFTs were measured down to bending radii of 5.5 mm, which correspond to tensile strain ϵ = 0.65 % and to compressive strain ϵ = -0.6 %. In the bending experiments, Fe-TFTs were measured with a double sweep of V_{GS} between 5 V and −2 V, at V_{DS} = 0.1 V. A smaller interval of V_{GS} was selected to minimize the effect of electrical stress in the measurement. The transfer characteristic of a flexible Fe-TFT, measured when flat, bent to a tensile radius of 5.5 mm and then bent to a compressive radius of 5.5 mm is displayed in Fig. 6.7. The small variations between the transfer curve (measured flat) and the curve shown in Fig. 6.3 are mainly due to the different V_{GS} intervals. Like for reference TFTs (Fig. 6.5), the transfer characteristic presents parallel shifts in opposite directions for tensile and compressive bending. Nevertheless, for Fe-TFTs the measured changes are larger than those observed for reference TFTs. After re-flattening, the Fe-TFTs are fully functional, whereas bending to radii <4.7 mm induces cracks in the

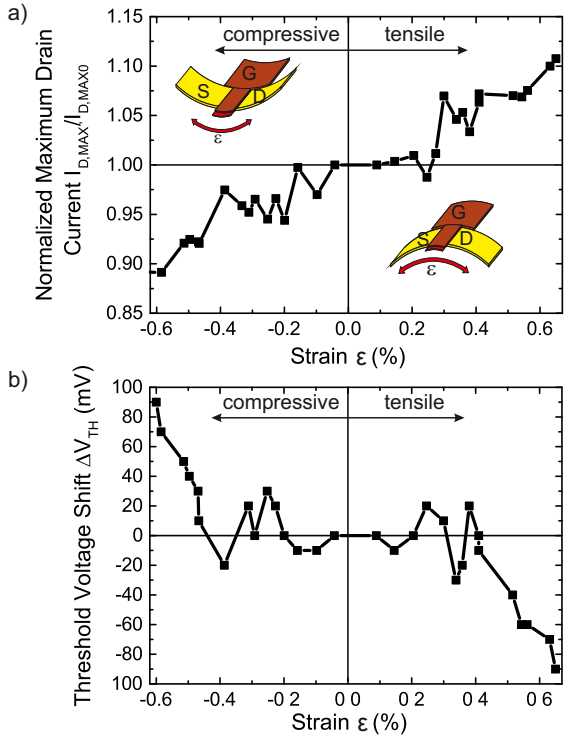

Figure 6.6: Flexible a-IGZO reference TFT: a) normalized maximum drain current (V_{GS} = 4 V and V_{DS} = 0.1 V) and b) threshold voltage shift for tensile and compressive strain. All values are extracted from the same TFT. The time interval between two consecutive measurement points is 5 min.

channel that permanently harm the devices. Fig. 6.8 displays: a) the normalized $I_{D,MAX}$ (measured at V_{GS} = 5 V and V_{DS} = 0.1 V), b) ΔV_{TH} for both the forward (black line) and the reverse (red line) branch, and c) the normalized memory on/off ratio (black line) and the normalized memory window MW (red line) versus the applied tensile and compressive strain. $I_{D,MAX}$, memory on/off ratio and MW are normalized by their measurement at flat substrate, whereas ΔV_{TH} is given by the difference to its value at flat substrate. Tensile strain ϵ of 0.65 % increases $I_{D,MAX}$ by 177 %, whereas V_{TH} shifts by -810 mV (forward) and -580 mV

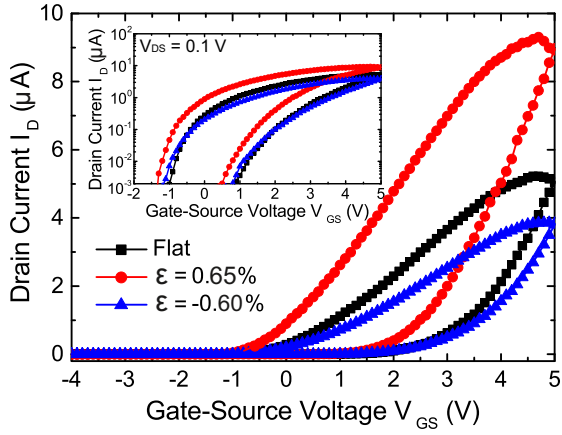

Figure 6.7: Transfer characteristics of flexible a-IGZO Fe-TFTs (W/L = 1400 μm/20 μm), measured flat, bent to a tensile radius of 5.5 mm (ϵ = 0.65 %) and bent to a compressive radius of 5.5 mm (ϵ = −0.6 %). All transfer characteristics are measured at V_{DS} = 0.1 V. (Inset) Enlargement of transfer characteristics in a logarithmic scale.

(reverse). Compressive strain of -0.6 % results in a decrease of $I_{D,MAX}$ by 24 % and a shift of V_{TH} of -40 mV (forward) and -10 mV (reverse). Even though the transfer curve shifts in the positive direction under applied compressive strain (Fig. 6.7), the extracted ΔV_{TH} does not show this trend (Fig. 6.8b). This behaviour can be explained considering that V_{TH} was defined as the V_{GS} value where I_D = 5 x 10^{-8} A. At this current value, the forward and the reverse branches present small shifts in the negative direction, as visible in Fig. 6.7 (logarithmic scale). These negative V_{TH} shifts are mainly caused by the strain-induced sub-threshold swing variations, as it will be explained afterward. Since V_{TH} shifts in the same direction for the forward and the reverse branch (Fig. 6.8b), the memory window MW = $V_{TH,FOR}$-$V_{TH,REV}$ (Fig. 6.8c) is not significantly affected by bending. On the other hand, due to the variations of I_D (Fig. 6.7), the memory on/off ratio $I_{D,REV}$ (V_{GS} = 0 V)/$I_{D,FOR}$ (V_{GS} = 0 V) (Fig. 6.8c) is increased by 318% for tensile strain (ϵ = 0.65 %), and decreased by 28% for compressive strain (ϵ = -0.6 %). These changes are caused by the variation of the memory on-value $I_{D,REV}$ (V_{GS} = 0 V), while the off-value $I_{D,FOR}$ (V_{GS} = 0 V) stays mainly unchanged. Larger changes in $I_{D,REV}$ (V_{GS} = 0 V) (Fig. 6.8c), compared to $I_{D,MAX}$ = I_D(V_{GS} =

5 V) (Fig. 6.8a) can be explained by a steeper slope of the curve at V_{GS} = 0 V, compared to V_{GS} = 5 V.

The observed behaviour can be explained considering that P(VDF-TrFE) is not only a ferroelectric, but also a piezoelectric polymer [143], therefore its polarization depends on the applied mechanical strain. In these experiments, tensile and compressive strain was applied parallel to the channel length, and therefore perpendicular to the direction of the dipole moments in the P(VDF-TrFE). In piezoelectric materials, the ratio between polarization and strain perpendicular to the direction of polarization is given by the transverse piezoelectric coefficient d_{31}, which is always positive for P(VDF-TrFE) [194]. This means that tensile strain increases the polarization in the P(VDF-TrFE) layer, whereas compressive strain decreases the polarization. Due to the bistable polarization of the P(VDF-TrFE), we have to distinguish the following two cases: 1) if a sufficiently large V_{GS} has been applied, the dipole moments in the P(VDF-TrFE) are aligned in such a way that the negatively charged fluorine atoms point in the direction of the gate and the positively charged hydrogen atoms in the direction of the substrate, as shown in Fig. 6.9a. With this orientation, negative carriers are accumulated in the semiconductor (Fig. 6.9a). 2) If a sufficiently negative V_{GS} has been applied, the dipole moments are aligned in the opposite direction (Fig. 6.9d). With this orientation, depletion is induced in the IGZO. In the following, we will discuss the main mechanisms behind the observed behaviour for $I_{D,MAX}$ and V_{TH}.

6.4.3.1 Maximum Drain Current Variations Induced By Bending:

$I_{D,MAX}$ is extracted at V_{GS} = 5 V, corresponding to the case shown in Fig. 6.9a. If tensile bending is applied, the polarization increases and thereby also the electron density in the channel (Fig. 6.9b). As a consequence, $I_{D,MAX}$ increases under applied tensile strain, as clearly visible from the measurement in Fig. 6.7 and 6.8a. If compressive bending is applied, the polarization reduces the conductivity in the IGZO (Fig. 6.9c), and therefore leads to a decreased $I_{D,MAX}$ (Fig. 6.7 and 6.8a). However, compressive strain results in a smaller effect. Since the influence of strain on the IGZO properties results in shifts in the same direction of the variations due to the strain-dependence of the P(VDF-TrFE) polarization, the two effects sum up.

6.4.3.2 Threshold Voltage Shifts Induced By Bending:

Concerning the V_{TH}, three different effects have to be taken into account: (i) the strain-dependent P(VDF-TrFE) polarization is responsible for charge carrier density modulation in the IGZO; (ii) the strain-dependent P(VDF-TrFE) polarization influences C_G and results in variations of SS; and (iii) the strain-dependent IGZO properties also lead to conductivity variations. In the following, we will investigate the three different effects individually.

(i) The strain-dependent P(VDF-TrFE) polarization leads to a variation in the IGZO carrier density, and therefore to shifts in V_{TH}. However, for this effect we need to consider two different cases depending on the polarization orientation: 1) when we extract the V_{TH} for the forward branch ($V_{TH,FOR}$), the case shown in Fig. 6.9d applies. With this orientation, the under tensile strain increased polarization leads to a decrease of the channel conductivity (Fig. 6.9e) and therefore to a positive $\Delta V_{TH,FOR}$ (↑). For compressive strain, the negative charge carrier concentration in the IGZO is increased (Fig. 6.9f) and this results in a negative $\Delta V_{TH,FOR}$ (↓). 2) For the reverse sweep, the case shown in Fig. 6.9a applies. Here, tensile bending increases the IGZO conductivity (Fig. 6.9b) and results in a negative $\Delta V_{TH,REV}$(↓) for the reverse branch. Compressive strain, on the other hand, causes a decreased IGZO carrier concentration (Fig. 6.9c), and thereby a positive $\Delta V_{TH,REV}$ (↑).

(ii) For tensile bending, the polarization is increased and thereby also the ferroelectric capacitance C_{FE}. This results in an increase of C_G, leading thus to a smaller SS [177]. For compressive bending, the decreased polarization leads to a larger SS. This effect is independent from the orientation of the polarization. As a result, under applied tensile strain, the smaller SS leads to a negative ΔV_{TH} (↓) for both forward and reverse branches, as shown in the measurement in Fig. 6.8b. Compressive strain instead results in a positive ΔV_{TH} (↑) for both forward and reverse branches, due to the increased SS. Compressive strain has a smaller effect due to the smaller SS variations (≤1%). It is worth mentioning that SS has such direct impact on V_{TH} due the method adopted for its extraction.

(iii) The strain-dependent IGZO carrier density leads to negative ΔV_{TH} (↓) for tensile strain, and a positive ΔV_{TH} (↑) for compressive bending, for both forward and reverse branches. Nevertheless, these shifts are <100 mV, as shown in the measurement of Fig. 6.6b.

For tensile strain, the large changes in the SS (ii) seem to dominate over the other effects, leading to a negative ΔV_{TH} ($\downarrow$) for both forward and reverse branch. For compressive strain, where the SS changes are smaller, all effects have a similar value, resulting in the shift shown in Fig. 6.8b.

The results of the bending experiments presented in this paper, in contrast to previous publications on flexible a-IGZO Fe-TFTs [141, 142], show that mechanical strain has a significant influence on the performance of Fe-TFTs. We were able to measure the influence of bending due to the use of a custom-built bending machine that allowed the continuous measurement of bent devices, with a defined interval between each measurement and without the need of placing probe tips each time. This setup allowed measuring the impact of mechanical strain independently from other effects, e.g. electrical stability and/or contact resistance.

6.5 Conclusions

In this paper, we presented mechanically flexible a-IGZO memory TFTs with a ferroelectric P(VDF-TrFE) gate dielectric. Memory operation was demonstrated with a memory window of 3.2 V and a memory on/off ratio of 1.5 x 10^6, for a gate-source voltage sweep of ±6 V. Fe-TFTs exhibit a field effect mobility of 8 $cm^2V^{-1}s^{-1}$ and an on/off current ratio of 10^7, which are comparable to values achieved in reference TFTs fabricated on the same substrate. Influence of tensile and compressive strain (minimum bending radius of 5.5 mm) on the device characteristics was estimated. For both reference TFTs and Fe-TFTs, tensile strain causes a negatively shifted threshold voltage and an increased drain current. On the other hand, compressive bending results in a positive threshold voltage shift and a decreased drain current. However, Fe-TFTs, compared with reference TFTs, exhibit strain-induced threshold voltage shifts that are up to 8× larger and drain current variations that are up to 17× larger. Shifts in the Fe-TFTs are caused by a superposition of the strain-induced dependence of the polarization in the piezoelectric P(VDF-TrFE) layer, and the strain-dependent IGZO properties. These shifts need to be considered when designing future flexible memories. Full memory operation down to bending radii of 5.5 mm demonstrates that these devices are feasible for next-generation large-area highly functional flexible electronic systems.

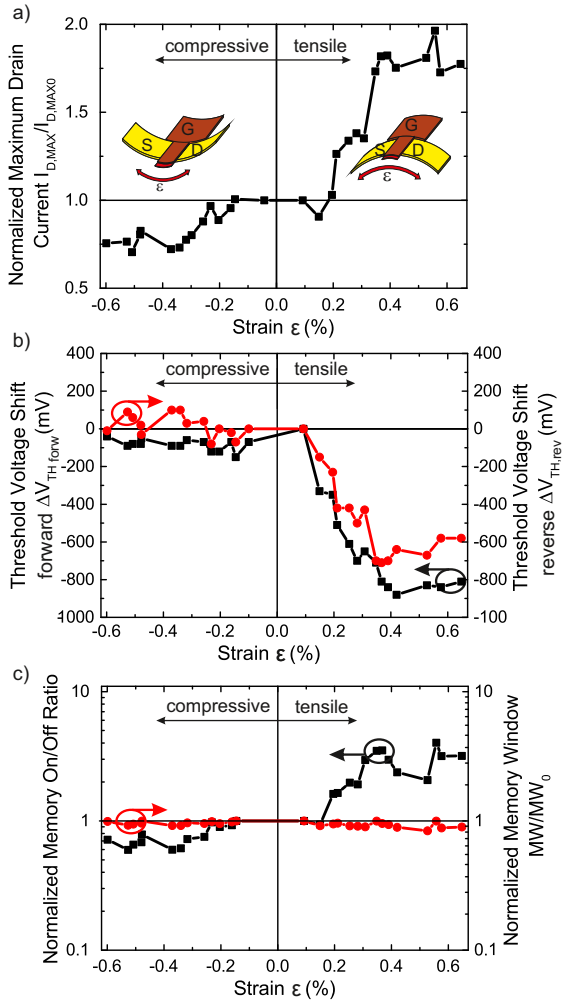

Figure 6.8: Flexible a-IGZO Fe-TFT: a) normalized maximum drain current (V_{GS} = 5 V and V_{DS} = 0.1 V), b) threshold voltage shift for the forward (black line) and the reverse (red line) branch, c) normalized memory on/off (black line) and normalized memory window MW (red line) for tensile and compressive strain. All values are extracted from the same Fe-TFT. The time interval between two consecutive measurement points is 5 min.

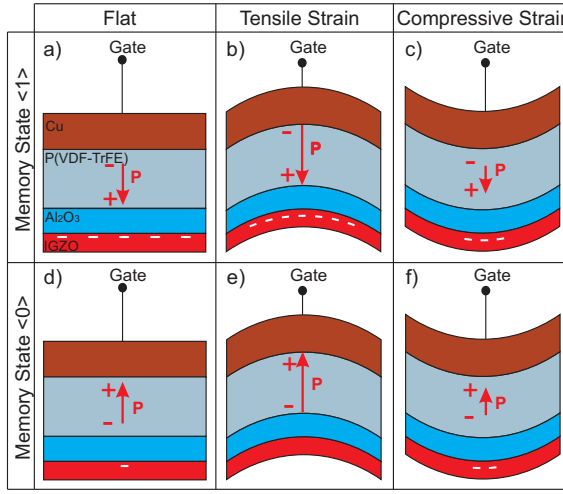

Figure 6.9: Schematic cross section of gate stack of flexible a-IGZO Fe-TFT: a) with memory state <1> stored when flat, b) bent to tensile strain, c) bent to compressive strain; d) and with memory state <0> stored when flat, e) bent to tensile strain, and f) bent to compressive strain. For each case the orientation and the amplitude of the dipole moments in the P(VDF-TrFE), as well as the charge carriers induced in the IGZO are displayed.

7

Complementary Circuits

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Integration of Solution-Processed (7,5) SWCNTs with Sputtered and Spray-Coated Metal Oxides for Flexible Complementary Inverters

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Abstract

We report the integration of solution-processed high-purity semiconducting (7,5) single walled carbon nanotubes (SWCNTs) with metal oxides for the fabrication of high-performance CMOS inverters on free-standing plastic foils. Flexible inverters based on spin-coated SWCNTs and sputtered amorphous InGaZnO (IGZO) exhibit gains up to 85 V/*V, even while bent to a tensile radius of* 1 cm. *To our knowledge, this is the highest gain ever reported for flexible and strained hybrid inverters, supplied at* V_{DD} $\leq$ 10 V. *We also realize flexible inverters based on fully solution-deposited SWCNTs and* In_2O_3 *semiconductors.*

7.1 Introduction

Complementary MOS technology, combining n- and p-type transistors, enables simplification of circuit design whilst lowering power consumption, and minimizing noise. The realization of a thin-film equivalent to silicon CMOS electronics suffers from the lack of complementary organic or inorganic semiconductors with similar performance. To date, several groups have reported logic circuits based on n-type metal oxides and organic [195] or inorganic [34] p-type semiconductors. While n-type metal oxides, especially amorphous IGZO [10], possess high mobility >10 $cm^2V^{-1}s^{-1}$ and ambient stability, organic and inorganic p-type materials with matching performance are difficult to achieve. Recently, solution-based SWCNTs have drawn a considerable attention, owing to their good electrical and mechanical properties. Using ink-jet printing methods, in combination with mixed semiconducting SWCNTs and ZTO, complementary circuits have now been demonstrated [196].

In this paper, we advance the current state-of-the-art, by integrating spin-coated highly-selected semiconducting (7,5) SWCNTs [135] with sputtered and spray-coated n-type metal oxides, offering a route towards flexible and strained complementary inverters with high gains and excellent noise margins.

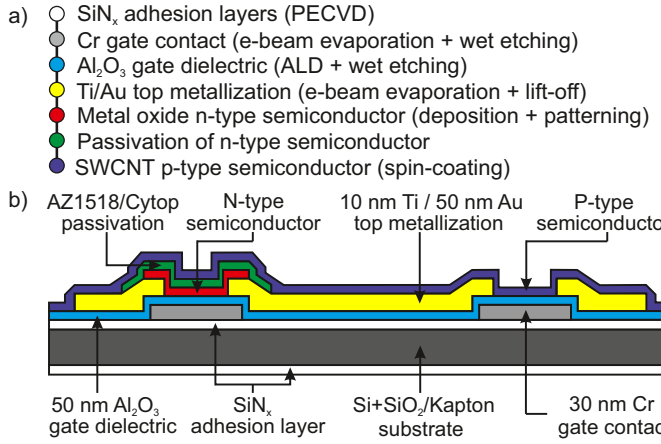

Figure 7.1: Hybrid complementary inverter based on solution-processed (7,5) SWCNT TFTs and metal oxide TFTs: a) process flow and b) schematic cross section. Fabrication process was optimized concerning low temperature fabrication, thickness of brittle materials, and adhesion between the different device layers aiming at good device performance and bendability.

7.2 Fabrication

Hybrid complementary inverters were fabricated on 4-in. Si/SiO_2 wafers and on 50 µm-thick polyimide foils (7.6 x 7.6 cm^2), using a bottom-gate coplanar TFT geometry. Fig. 5.1 shows: a) the fabrication process flow and b) the schematic cross section. Cr gate contacts, Al_2O_3 gate dielectric, and Ti/Au electrodes were realized using standard thin-film deposition methods and UV lithography [122]. Subsequently, the substrates were diced into chips of 1.5 x 1.5 cm^2. In the case of vacuum-processed metal oxide, a 15 nm-thick IGZO [10] film was deposited at room temperature, using RF magnetron sputtering and a ceramic $InGaZnO_4$ target. The IGZO was then patterned into islands by wet etching and passivated with photoresist (AZ1518®). For the solution-processed metal oxide, a 10 nm-thick In_2O_3 film was deposited in air via ultrasonic spray pyrolysis, using a solution of 30mg/ml indium nitrate hydrate in deionized water. During the automated spray process, the substrate was heated to 250 °C. The In_2O_3

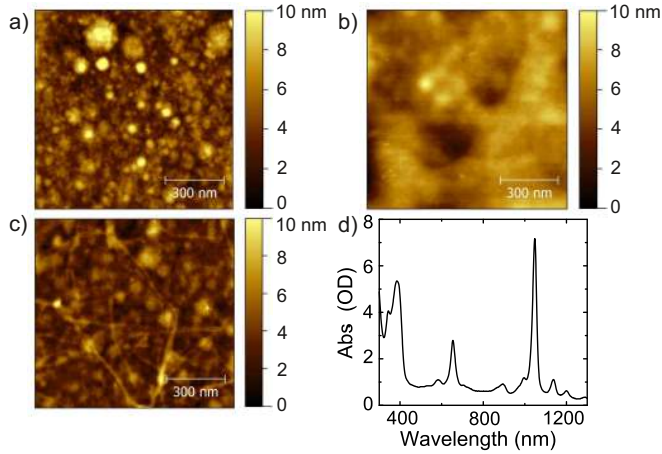

Figure 7.2: AFM images showing surface topography of: a) IGZO (15 nm), b) In_2O_3 (10 nm), and c) (7,5) SWCNT (10 nm) films on $Si/SiO_2/SiN_x/Al_2O_3$ surface. d) Absorption spectrum of the (7,5) SWCNT solution.

was patterned using a shadow mask, and then passivated with a Cytop® layer. To complement the n-type IGZO and In_2O_3, a semiconducting (7,5) SWCNT solution, behaving as p-type material, was used. Single-chirality was achieved by means of polymer-wrapping [135]. The SWCNT solution was spin-coated and annealed at 90 °C in nitrogen (N_2), resulting in a 10 nm-thick layer, which was left unstructured and unpassivated. Fig. 7.2 shows the surface topography of the three semiconductors obtained with atomic force microscopy (AFM). Both metal oxides present a homogeneous structure without any grain boundaries. Fig. 7.2c shows the randomly oriented SWCNT network, exhibiting continuous current percolation paths. Fig. 7.2d displays the absorption spectrum of the SWCNT solution. The peak at $\lambda = 1050$ nm corresponds to the first excitonic transition of the (7,5) diameter, proving that our SWCNTs are single-chirality.

7.3 IGZO/SWCNT TFTs and Inverters

Fig. 7.3 shows the I_D-V_{DS} and I_D-V_{GS} characteristics of the IGZO and SWCNT TFTs on Si/SiO_2 substrate, measured in nitrogen (N_2). TFT per-

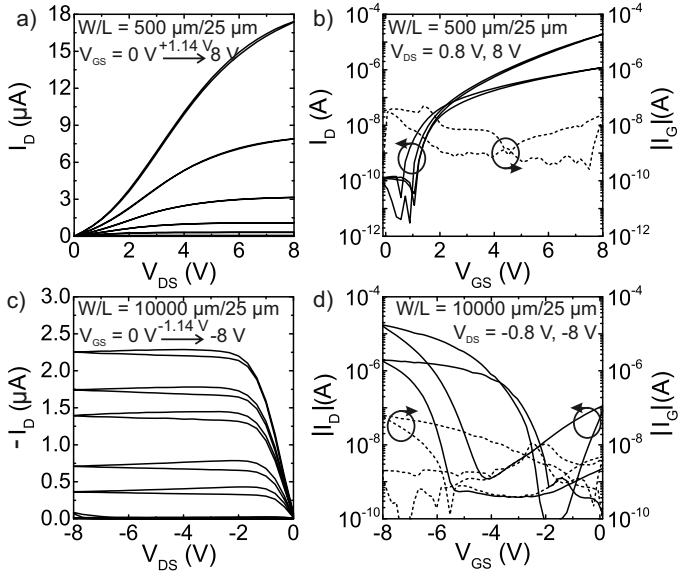

Figure 7.3: Output and transfer characteristics of sputtered IGZO [a) and b)] and spin-coated (7,5) SWCNT [c) and d)] TFTs on Si/SiO_2 substrate. TFT performance parameters are: $\mu_{FE,n}$ = 0.7 $cm^2V^{-1}s^{-1}$, $V_{TH,n}$ = 4 V, SS_n = 0.12 V/dec, $\mu_{FE,p}$ = 0.02 $cm^2V^{-1}s^{-1}$, $V_{TH,p}$ = -2.8 V, and SS_p = 0.42 V/dec. Electrical measurements were carried out in nitrogen (N_2).

formance parameters were extracted using standard MOSFET equations. The IGZO TFT exhibits a saturation field-effect mobility $\mu_{FE,n}$ = 0.7 $cm^2V^{-1}s^{-1}$, a threshold voltage $V_{TH,n}$ = 4 V, and a sub-threshold swing SS_n = 0.12 V/dec. The low effective mobility compared to [122] is attributed to the non-annealed IGZO film, as well as to the coplanar TFT structure with Au contacts. The SWCNT TFT yields $\mu_{FE,p}$ = 0.02 $cm^2V^{-1}s^{-1}$, $V_{TH,p}$ = -2.8 V, and SS_p = 0.42 V/dec. The hysteresis in the drain current is caused by the polymeric presence in the SWCNT solution, whereas the slightly ambipolar behavior is due to the intrinsic properties of the SWCNTs. The overall process yield of IGZO and SWCNT devices fabricated in multiple runs on 1.5 x 1.5 cm^2 chips, each containing 20 TFTs, is ≈70 %. Process variability results in the following parameter distribution: $V_{TH,n}$ = (3.2 ± 0.8) V, $\mu_{FE,n}$ = (0.7 ± 0.5) $cm^2V^{-1}s^{-1}$, $V_{TH,p}$ = (-2.5 ± 0.4) V, and $\mu_{FE,p}$ = (0.026 ± 0.01) $cm^2V^{-1}s^{-1}$.

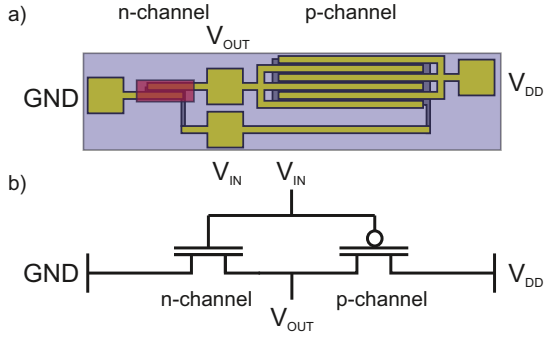

Figure 7.4: Circuit diagram (a) and schematic (b) of the fabricated hybrid complementary inverter based on metal oxide TFTs and solution-processed (7,5) SWCNT TFTs. All TFTs have a channel length L of 25 μm, with an interdigitated channel, as visible in a).

The complementary inverter was realized by connecting SWCNT and IGZO TFTs as shown in Fig. 7.4. An extensive TFT characterization was used to design inverters with centered midpoint voltages $V_M \approx V_{DD}/2$. Fig. 7.5 displays: a) the voltage transfer characteristics (VTC) and b) the static gain G, measured at different supply voltages. At V_{DD} = 10 V, the inverter exhibits a V_M = 4.75 V, a G = 60.6 V/V, a rail-to-rail swing (V_{OH} = 9.95 V, V_{OL} = 0.28 V), and excellent noise margins (NM_H = 4.33 V, NM_L = 4 V). When V_{IN} is swept from low to high voltage bias, V_M shifts by +20 mV for V_{DD} = 5 V, and by +1.9 V for V_{DD} = 10 V. This is attributed to the gate-induced current hysteresis of the SWCNT TFT, which can be reduced by decreasing the polymeric content in the solution. Furthermore, IGZO and SWCNT TFTs are electrically stable. A positive (negative) bias stress up to 100 MV/m for a period of 300 s induces a positive (negative) ΔV_{TH} up to 0.55 (-0.6) V in IGZO (SWCNT) TFTs, due to charge carrier injection in the gate dielectric. The static power dissipation (V_{DD} = 10 V) is less than 5 μW for V_{IN} HIGH or LOW, and reaches a maximum of 17 μW at $V_{IN} = V_M$. Measurements were carried out in N_2. Fig. 7.6 shows the VTC and the static gain of the inverter measured under ambient conditions. After being exposed to ambient air, the inverter is operational, with V_M = 5.1 V and G = 51.6 V/V. These variations are due to the changes in the performance of the unpassivated SWCNT TFT, and can be strongly reduced by encapsulating the SWCNT devices. Fig.7.7 shows the transfer characteristics

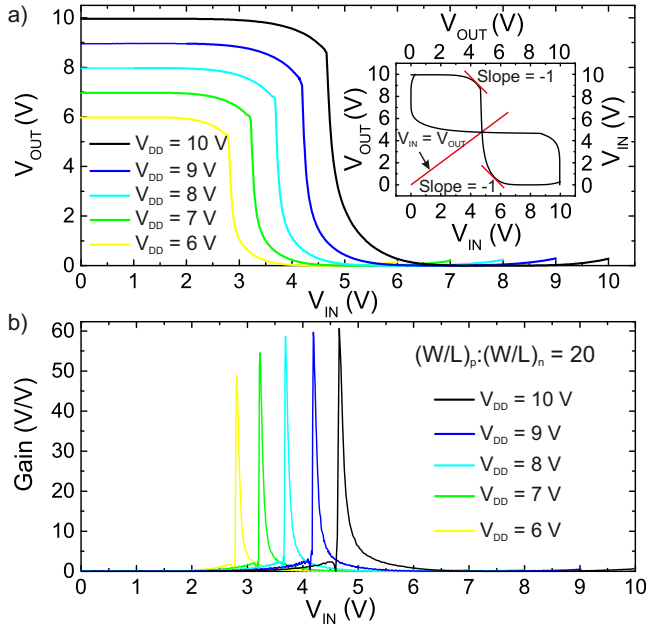

Figure 7.5: Voltage transfer characteristic (VTC) (a) and static gain (G) (b) of the complementary inverter based on sputtered IGZO and spin-coated (7,5) SWCNT TFTs on Si/SiO_2 substrate, measured at V_{DD} = 6, 7, 8, 9, 10 V. The inset shows the bi-stable hysteresis VTC at V_{DD} = 10 V. For V_{DD} = 10 V, V_M = 4.75 V, G = 60.6 V/V, NM_H = 4.33 V, and NM_L = 4 V.

of the IGZO and SWCNT TFTs on free-standing plastic foil, measured while flat and wound around a rod of 1 cm radius, which induces a tensile strain of ≈0.29 % parallel to the channels (Fig. 7.7). The TFTs stay fully functional while bent and show only minor variations in the device performance ($V_{TH,n}$ +30 mV, $V_{TH,p}$ +20 mV, $\mu_{FE,n}$ -0.8 %, $\mu_{FE,p}$ +2 %, SS_n +3 %, and SS_p -3.7 %). Compared to electrical stress, mechanical stress results in a smaller effect on the TFT performance. Fig. 7.8 shows the VTC and the static gain of the mechanically flexible complementary inverter, measured while the circuit is flat and bent. A gain of 87 V/V and a midpoint voltage of 4.39 V were obtained. The changes in V_M (+40 mV) and G (-1.6 %) are explained by the variations in the

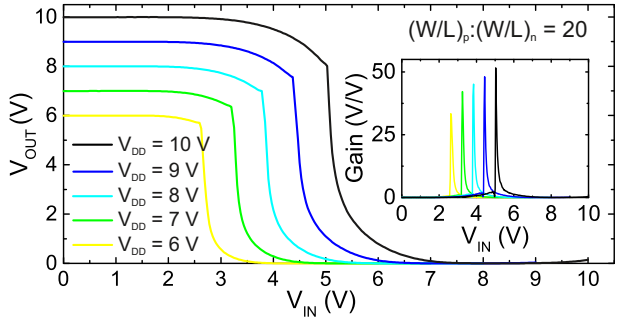

Figure 7.6: VTC and gain (inset) of IGZO/SWCNT complementary inverter on Si/SiO_2 substrate, measured at V_{DD} = 6, 7, 8, 9, 10 V. For V_{DD} = 10 V, V_M = 5.1 V and G = 51.6 V/V. Measurements were carried out in ambient conditions.

V_{TH}, μ_{FE}, and SS of the TFTs.

7.4 In_2O_3/SWCNT TFTs and Inverters

Fig. 7.9 shows the electrical characteristics of In_2O_3 and SWCNT TFTs on Si/SiO_2 substrate, measured in N_2. N-type In_2O_3 TFT parameters are: $\mu_{FE,n}$ = 0.02 $cm^2V^{-1}s^{-1}$, $V_{TH,n}$ = 1.2 V, and SS_n = 1.5 V/dec. High off current hint at large carrier conductivity in the In_2O_3 layer, caused by the generation of intrinsic defects during processing. The slightly different characteristics of the SWCNT TFT in Fig. 7.9, compared to Fig. 7.3, is due to process variability. Fig. 7.10 and 7.11 display the VTCs and static gains of In_2O_3/SWCNT inverters on Si/SiO_2 and polyimide substrates. For V_{DD} = 10 V, the rigid (flexible) inverter yields V_M = 5.1 (3.97) V, G = 48.4 (22) V/V, and V_{OH} = 9.6 (9.2) V. These differences are attributed to the comparatively poor performance of the flexible In_2O_3 TFT, caused by the increased roughness and the lower thermal conductivity of the polyimide when compared to Si/SiO_2.

7.5 Conclusion

Solution-based highly-selected semiconducting (7,5) SWCNTs and metal oxides enabled the fabrication of high-performance CMOS inverters on flexible plastic foils. Flexible complementary inverters based

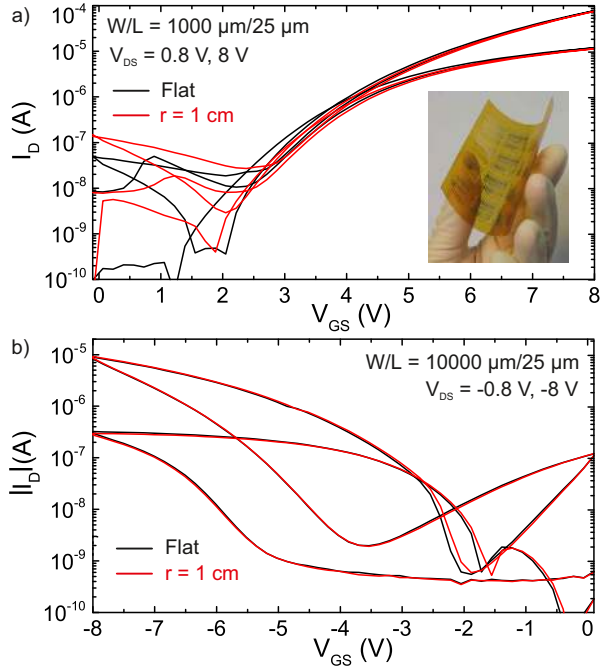

Figure 7.7: Transfer characteristics of flexible IGZO (a) and SWCNT (b) TFTs on plastic foil, measured while flat and bent to a radius of 1 cm, which corresponds to a tensile strain $\epsilon \approx 0.29\,\%$ parallel to the TFT channels. Bending changes $V_{TH,n}$ by +30 mV, $V_{TH,p}$ by +20 mV, $\mu_{FE,n}$ by -0.8 %, $\mu_{FE,p}$ by +2 %, SS_n by 3 %, and SS_p by -3.7 %. The inset shows a photograph of the processed flexible substrate. Electrical measurements were carried out in N_2.

on spin-coated SWCNT and sputtered IGZO TFTs exhibited gains up to 85 V/V (V_{DD} = 10 V), even while bent to a tensile radius of 1 cm. Furthermore, we also integrated SWCNTs with spray-coated In_2O_3 to realize mechanically flexible inverters with fully solution-deposited semiconductors. These results pave the way toward large-area solution-processed flexible electronics.

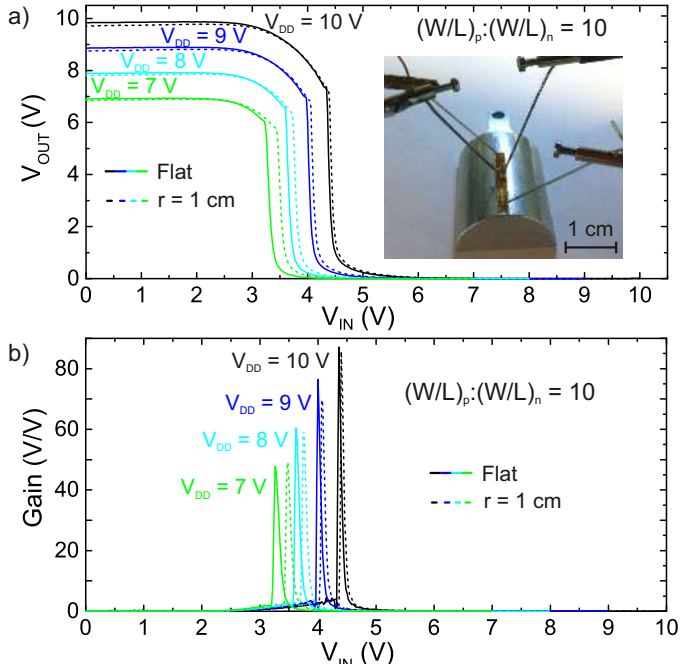

Figure 7.8: VTC (a) and static gain (b) of flexible complementary inverter based on IGZO and SWCNT TFTs on plastic foil, measured at V_{DD} = 7, 8, 9, 10 V while flat and bent to a tensile radius of 1 cm ($\epsilon \approx$ 0.29 % parallel to all TFT channels). For V_{DD} = 10 V, V_M = 4.39 (4.43) V and G = 87.1 (85.7) V/V for the flat (bent) circuit. The inset shows a photograph of the contacted flexible complementary inverter, bent to a tensile radius r = 1 cm. The changes in V_M (+40 mV) and G (-1.6 %) are explained by the variations in V_{TH}, μ_{FE}, and SS of the TFTs. Electrical measurements were carried out in N_2.

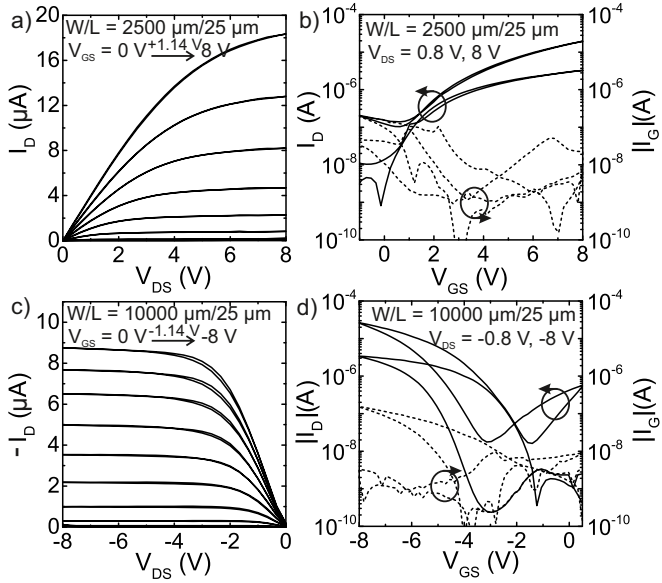

Figure 7.9: Output and transfer characteristics of spray-coated In_2O_3 [a) and b)] and spin-coated (7,5) SWCNT [c) and d)] TFTs on Si/SiO_2 substrate. TFT performance parameters are: $\mu_{FE,n} = 0.02\,cm^2V^{-1}s^{-1}$, $V_{TH,n} = 1.2\,V$, $SS_n = 1.5\,V/dec$, $\mu_{FE,p} = 0.01\,cm^2V^{-1}s^{-1}$, $V_{TH,p} = -2.4\,V$, and $SS_p = 1.15\,V/dec$. Electrical measurements were carried out in N_2.

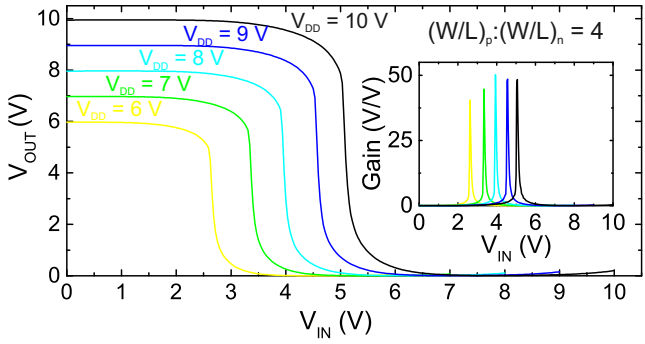

Figure 7.10: VTC and static gain (inset) of rigid complementary inverter with fully solution-processed semiconductors, based on spray-coated In_2O_3 and spin-coated SWCNT TFTs on Si/SiO_2 substrate, measured at V_{DD} = 6, 7, 8, 9, 10 V. For V_{DD} = 10 V, V_M = 5.1 V and G = 48.4 V/V. Electrical measurements were carried out in N_2.

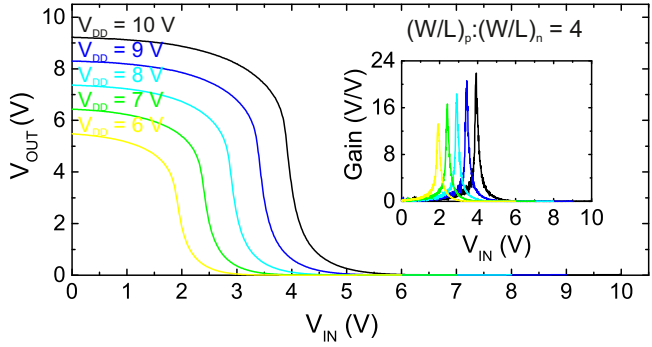

Figure 7.11: VTC and static gain (inset) of flexible inverter with fully solution-processed semiconductors, based on spray-coated In_2O_3 and spin-coated SWCNT TFTs on plastic foil, measured at V_{DD} = 6, 7, 8, 9, 10 V. For V_{DD} = 10 V, V_M = 3.97 V and G = 22 V/V. Measurements were carried out in N_2.

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Glossary

Si^{++}	Heavily Doped Silicon	108, 109
$\Delta V_{TH,FOR}$	Threshold Voltage Shift for Forward Sweep (Memory Transistor)	131
$\Delta V_{TH,REV}$	Threshold Voltage Shift for Reverse Sweep (Memory Transistor)	131
ΔV_{TH}	Threshold Voltage Shift (Transistor)	91, 92, 94, 126, 128, 129, 131, 132, 140
ϵ	Strain	44, 48, 54, 58, 62, 63, 66, 71, 72, 75, 80, 91–95, 114, 115, 125–129, 143, 144
ϵ_R	Dielectric Constant	7, 8, 13, 41, 60
ϵ_r	Rupture Strain	41
λ	Wavelength	138
$\mu_{FE,n}$	Electron Field-Effect Mobility (N-type Transistor)	139, 141–143, 145
$\mu_{FE,p}$	Hole Field-Effect Mobility (P-type Transistor)	139, 141, 143, 145
μ_{FE}	Effective Field-Effect Mobility (Transistor). The effective field-effect mobility is directly proportional to the drain current of a TFT. Therefore μ_{FE} also reflects changes in the contact resistance, in the oxide capacitance, and in the TFT channel geometry caused by strain or the formation of cracks	10, 16–20, 22, 23, 42, 43, 45, 47, 48, 51, 53, 56, 58, 60, 62, 64, 66, 76–79, 81, 83, 142, 144
μ_H	Hall Mobility	42, 47, 87, 101
μ_{LIN}	Linear Field-Effect Mobility (Transistor)	69, 70, 110, 121, 122, 124

μ_{SAT}	Saturation Field-Effect Mobility (Transistor)	42, 44, 47, 48, 53, 55, 58, 61–63, 66, 82, 91–93, 95, 101–103, 110, 112, 114
$\mu_{SAT}/\mu_{SAT,0}$	Normalized Saturation Field-Effect Mobility (Transistor)	91, 94
3D	Three-Dimensional	49, 51
a-IGZO	Amorphous Indium Gallium Zinc Oxide	40, 85–95, 118–124, 126–129, 132–134
a-Si	Amorphous Silicon	2, 4, 16, 86, 98
AC	Alternating Current	9, 16, 18, 41, 42, 44–48, 51, 52, 54, 78, 93, 99–101
AFM	Atomic Force Microscopy	57, 61, 65, 66, 108, 109, 138
Ag	Silver	9
Al	Aluminum	7, 9, 57, 58, 61, 108, 110, 111
Al_2O_3	Aluminum Oxide	8, 13, 19, 41, 47, 50, 51, 54, 56, 57, 61, 62, 66, 69–71, 81, 82, 84, 87, 100, 104, 108, 109, 112, 120, 121, 124, 137, 138
Al_2O_3:Zr	Zirconium-Doped Aluminum Oxide	19
ALD	Atomic Layer Deposition	8, 12, 13, 41, 50, 51, 56, 69, 87, 99, 100, 108, 120
AM	Amplitude Modulation	2, 25, 78, 83, 86, 93
AMOLED	Active Matrix Organic Light Emitting Diode	2
Ar	Argon	46, 100, 101, 120
Au	Gold	9, 40, 45, 49–52, 55, 56, 59, 60, 73, 87, 100, 102, 108, 120, 137, 139
AZO	Aluminum Zinc Oxide	9

BC	Bottom-Contact (Transistor)	50, 52–71, 73, 107, 110, 112
Be	Beryllium	107
BG	Bottom-Gate (Transistor)	15, 17, 43, 44, 53, 56–59, 61–68, 70, 71, 73, 77–79, 81, 83, 107, 110, 112
C_{FE}	Ferroelectric Capacitance (Memory Transistor)	131
C_G	Gate Capacitance (Transistor)	16, 42, 48, 49, 54, 81, 88–90, 102, 103, 121, 124, 131
C_G/W	Width-Normalized Gate Capacitance (Transistor)	42, 43, 81
C_{ox}	Specific Gate Dielectric Capacitance (Transistor)	42, 51
C-V	Capacitance-Voltage (Transistor)	54, 88
CAAC	C-Axis Aligned Crystalline	10
CAD	Computer-Aided Design	51
CBM	Conduction Band Minimum	10
CF4	Tetrafluoromethane	40, 87
CMOS	Complementary Metal Oxide Semiconductor	67, 79, 80, 83, 136, 142
Cr	Chromium	9, 40, 42, 46, 52, 56–59, 61, 63, 66, 87, 100, 102, 108, 109, 112, 115, 137
CTE	Coefficient of Thermal Expansion	7
Cu	Copper	9, 41, 47, 48, 50, 51, 71, 87, 100, 104, 121, 125
Cu_xO	Cuprous Oxide	10, 20, 107
CuSCN	Copper (I) Thiocyanate	11, 25, 38, 56, 60–64, 76, 77, 79
d_{31}	Transverse Piezoelectric Coefficient	130

DC	Direct Current	9, 15, 16, 18, 23, 42, 45, 47, 48, 52, 53, 58, 61, 66, 69, 78, 93, 95, 99, 101
DG	Double-Gate (Transistor)	15, 17
DILL	Dip-In-Lithography	51
DLW	Direct Laser Write	vii, 24, 38, 39, 49–55, 69, 77–79, 81, 83
E_g	Band Gap	9
e-beam	Electron-Beam	40, 46, 50, 51, 56, 73, 83, 87, 99, 100, 108, 120, 121
e-textile	Electronic-Textile	98
f_T	Transit Frequency (Transistor). The transit frequency is the unity gain frequency of the small-signal current gain h_{21}	15–17, 43, 45, 48, 49, 54, 77, 78, 103
F8T2	Poly-(9,9-Dioctylfluorene-Co-Bithiophene)	24
Fe-TFT	Ferroelectric Thin-Film Transistor	68–73, 77, 118–122, 124–127, 129, 132–134
FET	Field-Effect Transistor	16
FIB	Focused Ion Beam	41, 46, 47, 83, 87, 88, 100
G	Static Gain (Circuit)	59, 63, 67, 75, 76, 140–142, 144, 146
g_m	Transconductance (Transistor)	16, 42, 47, 48, 53, 54, 87, 88, 90, 103
g_m/W	Width-Normalized Transconductance (Transistor)	43, 47, 102
g_{ds}	Output Conductance (Transistor)	88, 90
g_m/g_{ds}	Intrinsic Gain (Transistor)	88, 90
Ga	Gallium	40, 87, 97, 100, 117, 118, 120, 136, 137
Ga_2O_3	Gallium Oxide	107

GaAs	Gallium Arsenide	2
GBWP	Gain Bandwidth Product	23
GSG	Ground-Signal-Ground	41, 46, 51, 52
GZO	Gallium Zinc Oxide	10
	Small Signal Current Gain	16, 48, 49, 54, 55, 103
h_{21}		
HfLaO	Hafnium Lanthanum Oxide	8
HfO_2	Hafnium Oxide	8, 20
high-k	Material with High Dielectric Constant (Compared to SiO_2)	60, 110
	Memory OFF-Value (Memory Transistor)	70, 123, 129
$I_{D,FOR}$		
$I_{D,MAX}$	Maximum Drain Current (Transistor)	71, 72, 126–130
$I_{D,REV}$	Memory ON-Value (Memory Transistor)	70, 123, 129
I_D	Drain Current (Transistor)	42, 52, 58, 61, 65, 70, 87, 88, 90–92, 102, 103, 121–124, 129, 138
I_G	Gate Current (Transistor)	58, 62, 87, 101, 122, 124
I_{OFF}	Off Current (Transistor)	48, 53, 58, 101, 112
I_{ON}/I_{OFF}	On/Off Current Ratio (Transistor)	16–20, 42, 47, 48, 53, 58, 61, 62, 66, 69, 70, 77, 82, 101, 110, 112, 122
IGO	Indium Gallium Oxide	10
IGZO	Indium Gallium Zinc Oxide	vii–x, 10, 13, 16, 17, 19, 21–25, 27, 29, 38–55, 58, 67–82, 84, 87, 88, 90, 98–104, 115, 119–121, 126, 130–132, 134, 136–144
In	Indium	40, 82, 87, 97, 100, 107, 117, 118, 120, 136, 137

In_2O_3	Indium Oxide	viii, x, 9, 10, 13, 14, 18, 19, 24–27, 29, 38, 55–59, 65, 67, 73–80, 82, 106–115, 136–138, 142, 143, 145, 146
$In(NO_3)_3 \cdot H_2O$	Indium Nitrate Hydrate	57, 108
in.	Inch	57, 108, 137
IPA	Isopropanol	108
ITO	Indium Tin Oxide	9, 10, 13, 84, 103
IZO	Indium Zinc Oxide	9, 10, 58, 107, 115
L	Length (Transistor)	16, 41, 43, 46, 52–54, 78, 81, 108, 112–114, 140
L_{OV}	Overlap Length between Gate and Source/Drain Electrodes (Transistor)	15, 16, 42, 43, 49, 54, 81
LF	Low-Frequency	93
LOR	Lift Off Resist	46, 99
LTPS	Low Temperature Poly-Crystalline Silicon	2, 4
MEK	Methyl-Ethyl-Ketone	61, 69, 121
Mg	Magnesium	84
Mo	Molybdenum	9, 83, 102
MOS	Metal Oxide Semiconductor	136
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor	4, 6, 89, 101, 121, 139
MW	Memory Window (Memory Transistor)	70, 123, 128, 129, 133
N_2	Nitrogen	138–140, 142–146
NFC	Near-Field Communication	23
Ni	Nickel	9
NIR	Near Infrared	65
NM_H	Noise Margin High (Circuit)	112, 140, 141
NM_L	Noise Margin Low (Circuit)	112, 140, 141
NOT	Inverter (Circuit)	22–24

NP	Nanoparticle	18, 19
NR	Nanorod	13, 18, 19
NW	Nanowire	13, 18
O	Oxygen	40, 87, 97, 100, 117, 118, 120, 136, 137
O_2	Molecular Oxygen	40, 87, 101
P(VDF-TrFE)	Poly(Vinylidene Fluoride-Trifluoroethylene)	vii–x, 8, 13, 15, 20, 25–27, 29, 68–73, 80, 118–121, 124, 130–132, 134
P(VDF-TrFE-CFE)	Poly(Vinylidene Fluoride-Trifluoroethylene-Chlorofluoroethylene)	60–62
PAR	Polyarylate	7
PC	Polycarbonate	7
Pd	Palladium	45–47, 99–101, 104
PDMS	Polydimethylsiloxane	7, 82, 84
PEALD	Plasma-Enhanced Atomic Layer Deposition	13
PECVD	Plasma-Enhanced Chemical Vapor Deposition	13, 40, 46, 50, 56, 60, 87, 99, 108, 112, 120
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) Polystyrene Sulfonate	9, 14
PEEK	Polyetheretherketone	7
PEN	Polyethylene Naphthalate	7, 82
PES	Polyethersulfone	7
PET	Polyethylene Terephthalate	7, 82
PFO	Poly[(9,9-Dioctylfluorenyl-2,7-diyl)]	65, 74
PFO-BPy	Poly[(9,9-Dioctylfluorenyl-2,7-diyl)-Alt-Co-(6,6′-{2,2′-Bipyridine})]	65
PI	Polyimide	7, 14, 15, 17, 38, 40, 41, 45, 47, 49–52, 56–58, 60–62, 65, 69, 73, 74, 82, 112
PLD	Pulsed Laser Deposition	13
PMMA	Polymethyl Methacrylate	8

PP	Polypropylene	7
Pt	Platinum	9
PVA	Polyvinyl Alcohol	7, 8
PVP	Polyvinylpyrrolidon	8, 13, 19
QVTFT	Quasi-Vertical Thin-Film Transistor	27, 38, 39, 43–49, 53, 54, 77, 78, 81, 98–104
R	Resistance	59, 66, 68, 110, 113
r	Bending Radius	21, 95, 144
r_0	Initial Bending Radius	21
R_C	Contact Resistance (Transistor)	42, 43, 48, 49, 87, 89
r_C	Width-Normalized Contact Resistance (Transistor)	42, 47, 53, 101, 102
RF	Radio-Frequency	12, 40, 50, 51, 73, 77, 87, 100, 120, 137
RFID	Radio-Frequency Identification	2, 25, 78, 83, 86, 93, 106, 118
RH	Relative Humidity	7, 112
RIE	Reactive Ion Etching	40, 42, 87, 88
rms	Root Mean Square	109, 112
RO	Ring Oscillator (Circuits)	22–24
RT	Room Temperature	5, 19
S-parameters	Scattering Parameters	16, 48, 49, 55, 98, 103
S/D	Source/Drain (Transistor)	58, 108, 110, 111
SA	Self-Aligned (Transistor)	15, 17
SEM	Scanning Electron Microscopy	41, 46, 47, 51, 52, 87, 88, 100
Si	Silicon	2, 4, 6, 11, 12, 18, 57, 61, 66, 83, 102, 109, 111–113, 137–139, 141, 142, 145, 146
SiC	Silicon Carbide	2

SiN_x	Silicon Nitride	40, 44, 46, 48, 50, 56, 57, 60, 61, 66, 81, 87, 99–101, 104, 108, 109, 112, 119, 138
SiO_2	Silicon Oxide	8, 57, 61, 66, 84, 108, 109, 111–113, 137–139, 141, 142, 145, 146
SnO_x	Tin Oxide	10, 18, 20, 24, 106
SP	Spray Pyrolysis	107, 109
SS	Sub-Threshold Swing (Transistor). The sub-threshold swing is the inverse of the sub-threshold slope	16, 17, 42, 47, 53, 58, 61, 66, 70, 87, 101, 110, 122, 124, 131, 132, 142, 144
SS_n	Sub-Threshold Swing (N-type Transistor)	139, 141–143, 145
SS_p	Sub-Threshold Swing (P-type Transistor)	139, 141, 143, 145
SWCNT	Single Walled Carbon Nanotube	viii, x, 24, 25, 27, 29, 38, 56, 59, 64–68, 73–80, 83, 136–146
T_G	Glass Transition Temperature	6, 7, 112
T_m	Melting Temperature	6, 7
t_D	Thickness of the Device	22
t_S	Thickness of the Substrate	22
Ta_2O_5	Tantalum Oxide	8
TC	Top-Contact (Transistor)	57, 58, 107, 110
TFT	Thin-Film Transistor	vii, viii, 2–12, 14–27, 29, 38–84, 86, 88, 89, 92, 98, 99, 101, 106, 107, 109–114, 118–128, 132, 137–146
TG	Top-Gate (Transistor)	15, 39, 41, 44, 48–50, 52–55, 60–63, 69–71, 77–79, 81–83
Ti	Titanium	9, 45, 46, 50, 51, 55, 56, 59, 73, 99, 100, 104, 108, 120, 137

TiO_2	Titanium Oxide	8, 17
TrFE	Trifluoroethylene	69, 120
UV	Ultraviolet	14, 40, 46, 52, 56, 57, 65, 69, 83, 108, 137
V_M	Midpoint Voltage (Circuit)	24, 59, 63, 67, 75, 76, 110, 112, 140–142, 144, 146
V_{DD}	Supply Voltage (Circuit)	59, 63, 64, 67, 68, 75, 76, 110, 112, 113, 136, 140–144, 146
V_{DS}	Drain-Source Voltage (Transistor)	42, 43, 47, 49, 52, 53, 55, 58, 59, 61–63, 65, 67, 70, 72, 87, 88, 90–92, 102, 121–124, 126–129, 133, 138
V_{GS}	Gate-Source Voltage (Transistor)	42, 43, 47, 49, 52, 53, 55, 58, 61, 62, 65, 66, 70, 71, 87–89, 91, 92, 102, 103, 121–124, 126–130, 133, 138
V_{IN}	Input Voltage (Circuit)	59, 63, 67, 75, 140
V_{OH}	Output High Voltage (Circuit)	112, 140, 142
V_{OL}	Output Low Voltage (Circuit)	112, 140
$V_{TH,FOR}$	Threshold Voltage for the Forward Sweep (Memory Transistor)	129, 131
$V_{TH,n}$	Threshold Voltage (N-type Transistor)	139, 141–143, 145
$V_{TH,p}$	Threshold Voltage (P-type Transistor)	139, 141, 143, 145
$V_{TH,REV}$	Threshold Voltage for the Reverse Sweep (Memory Transistor)	129

V_{TH}	Threshold Voltage (Transistor)	16, 17, 19, 20, 22, 42, 44, 47, 48, 53, 55, 58, 61–63, 66, 69–72, 76, 77, 87, 91, 93, 95, 101, 103, 110, 112, 114, 121–123, 126–131, 142, 144
VBM	Valence Band Maximum	10
VDF	Vinylidene Fluoride	69, 120
Vis	Visible	65
VTC	Voltage Transfer Characteristic (Circuit)	63, 64, 66, 68, 74, 75, 140–142, 144, 146
VTFT	Vertical Thin-Film Transistor	27, 38–49, 77, 78, 81, 86–95, 98, 99, 101–104
	Width (Transistor)	41, 46, 52, 53, 108, 112–114
W		
W/L	Width over Length Ratio (Transistor)	39, 42, 57, 59, 61–70, 72, 75, 76, 87–91, 93–95, 98, 110, 111, 121, 125, 127, 129
	X-Ray Diffraction	58, 108, 109
XRD		
	Yttrium Oxide	8
Y_2O_3		
Y_D	Young's Moduli of the Device	22
Y_S	Young's Moduli of the Substrate	22
	Zinc Indium Tin Oxide	9
ZITO		
Zn	Zinc	40, 87, 97, 100, 117, 118, 120, 136, 137
ZnO	Zinc Oxide	10, 12–14, 19, 23, 86, 99, 106, 107
ZrO_2	Zirconium Oxide	8, 19
ZTO	Zinc Tin Oxide	10, 14, 107, 136

Curriculum Vitae

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Work experience

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