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Development and Optimization of High-Speed InP/GaAsSb Double Heterojunction Bipolar Transistors

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Abstract

Thanks to their staggered band alignment, GaAsSb-based InP double heterojunction bipolar transistors (DHBTs) feature excellent electron transport characteristics. DHBTs with InP as collector material not only allow ballistic electron injection into the collector, but also provide a high breakdown voltage as well as a good thermal conductance. Therefore, GaAsSb-based DHBTs have a great potential for high-speed mixed signal integrated circuits applications.

The aim of the present work was to further improve the high-frequency figures-of-merit of InP/GaAsSb DHBTs. This goal was reached by two approaches: Firstly, an improvement was made by means of developing a novel fabrication process while maintaining the reproducibility and the high yield in the device fabrication. Secondly, the design of the DHBT epitaxial layer structure was optimized by changing the material composition as well as the thickness of the semiconductor layers.

The development efforts resulted in a record InP/GaAsSb DHBT with an $f_{\mathrm{MAX}} = 779\,\mathrm{GHz}$ and a simultaneous $f_{\mathrm{T}} = 503\,\mathrm{GHz}$. The improved RF performance is attributed to the reduced base access resistance and the decreased base-collector capacitance. The device features a 0.2×4.4 $\mu\mathrm{m}^2$ emitter area and a 0.4×5.5 $\mu\mathrm{m}^2$ collector area, a peak common-emitter current gain of $\beta = 17$, and a breakdown voltage of $BV_{\mathrm{CEO}} = 4.1\,\mathrm{V}$ at a collector current density of $J_{\mathrm{C}} = 1$ kA/cm^2. The devices were fabricated in a combination of Ar sputtering and wet etching in a self-aligned emitter formation process, which was developed in order to reduce the base access distance.

Optimizations of the epitaxial layer structure demonstrated that the f_{T} can be improved by introducing a GaInP emitter launcher with a high Ga content as well as by reducing the base layer thickness. Further refining the GaAsSb base design in combination with vertical device scaling should allow the InP/GaAsSb DHBTs to reach THz bandwidth.

Zusammenfassung

Dank ihrer gestaffelten Band-Anordnung besitzen GaAsSb-basierte InP Doppel-Heteroübergang-Bipolartransistoren (DHBT) ausgezeichnete Elektronentransport-Eigenschaften. DHBT mit InP als Kollektor-Material erlauben nicht nur eine ballistische Elektronen-Injektion, sie bieten auch eine hohe Durchbruchspannung sowie eine gute thermische Leitfähigkeit. Daher haben GaAsSb-basierte DHBT grosses Potenzial für Hochgeschwindigkeits-Mischsignal-Schaltungen.

Ziel dieser Arbeit war es, die Hochfrequenz-Leistungsmerkmale der InP/GaAsSb DHBT zu verbessern. Dies wurde durch zwei Herangehensweisen erreicht: Erstens durch die Entwicklung eines neuartigen Fabrikationsprozesses, bei dem die Reproduzierbarkeit und die Ausbeute der Transistor-Produktion verbessert wurde. Zweitens wurde die Epitaxie der DHBT optimiert, indem die Zusammensetzung der Materialien sowie die Dicke der Halbleiter-Schichten verändert wurden.

Die Bemühungen führten zu einem rekordbrechenden InP/GaAsSb DHBT mit einer $f_{\mathrm{MAX}} = 779\,\mathrm{GHz}$ und einer gleichzeitigen $f_{\mathrm{T}} = 503\,\mathrm{GHz}$. Die verbesserte RF-Leistung ist auf den verringerten Basis-Zugangs-Widerstand sowie die verringerte Basis-Kollektor Kapazität zurückzuführen. Der Transistor weist eine $0.2 \times 4.4\ \mu\mathrm{m}^2$ grosse Emitterfläche und eine $0.4 \times 5.5\ \mu\mathrm{m}^2$ grosse Kollektorfläche auf, sowie eine maximale Stromverstärkung in der Emitterschaltung von $\beta = 17$ und eine Durchbruchspannung von $BV_{\mathrm{CEO}} = 4.1\,\mathrm{V}$ bei einer Kollektor-Stromdichte von $J_{\mathrm{C}} = 1\ \mathrm{kA/cm}^2$. Die Transistoren wurden mittels einer Kombination von Ar-Ionen Beschuss und Nass-Ätzen in einem automatisch ausgerichteten Fabrikationsprozess hergestellt. Der Prozess wurde entwickelt, um die Basis-Zugangs-Distanz zu verringern.

Die Optimierung der epitaxischen Schicht-Struktur zeigte auf, dass die f_{T} verbessert werden kann, indem man eine GaInP Energie-Schanze mit hohem Ga-Gehalt einführt. Die f_{T} kann ausserdem verbessert werden, indem man die Dicke der Basis-Schicht verringert. Durch eine weitere Verfeinerung des GaAsSb Basis Designs in Verbindung mit einer vertikalen Transistor-Skalierung sollten InP/GaAsSb DHBT THz Bandweiten erreicht werden können.

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Chapter 1

Introduction

1.1 Background

The need for integrated millimeter-wave circuits for high data rate wireless and wired communications, signal processing, sensing, imaging and radar applications is the primary driving force for the development of high-speed transistors [1]. III-V Heterojunction Bipolar Transistors (HBTs) [2–4] and Si/SiGe HBTs [5–7] are among the device technologies that are promising candidates to reach terahertz speeds [8, 9].

The advantages of the silicon-based material system are mainly its low costs, its high yield of integration, and its manufacturability [10]. As for InP/GaInAs single heterojunction bipolar transistors (SHBTs), they have the potential to provide high speed for various circuit application areas due to the wide-bandgap InP emitter, the higher electron mobility and the electron velocities [11–13]. However, InP/GaInAs SHBTs suffer from low breakdown voltage due to a narrow-bandgap collector, which is a limitation for the power handling capability. To improve the transistor breakdown voltage – and therefore yield higher output power – InP is used as the collector material in double heterojunction bipolar transistors (DHBTs) [14]. Thus, InP based DHBTs have a number of advantages for RF as well as mixed-signal applications [15, 16].

InP/GaAsSb DHBTs were developed as an alternative to InP/GaInAs

DHBTs for applications in high-speed electronic systems. For InP/GaInAs/InP and AlInAs/GaInAs/InP DHBTs, the main concern is the conduction band potential barrier between the GaInAs base and the InP collector [17,18]. The staggered band alignment at InP/GaAsSb heterojunctions enables the use of a simplified device structure with a pure InP collector layer. Pure InP collectors increase the junction symmetry and provide good thermal conductivity as well as high breakdown voltages. GaAsSb has an additional advantage: It can be easily p-doped with carbon to levels of 1×10^{20} cm^{-3}.

GaAsSb-based DHBTs were reported by Dvorak et. al in 2001 with $f_\mathrm{T} = f_\mathrm{MAX} = 300\,\mathrm{GHz}$ and $BV_\mathrm{CEO} = 6\,\mathrm{V}$ [19]. Since then, aggressive scaling, advances in the process technology, and epitaxial layer optimization have resulted in a significant step forward in the device performance. In *this* thesis, InP/GaAsSb DHBTs were demonstrated with a $f_\mathrm{MAX} = 780\,\mathrm{GHz}$ and a simultaneous $f_\mathrm{T} = 503\,\mathrm{GHz}$ with a breakdown voltage $BV_\mathrm{CEO} = 5\,\mathrm{V}$ [20]. To date, this is the highest reported f_MAX for an InP/GaAsSb DHBT. However, GaInAs-based DHBTs have been reported with a comparable $f_\mathrm{T} = 404\,\mathrm{GHz}$ with a simultaneous $f_\mathrm{MAX} = 901\,\mathrm{GHz}$ and with a BV_CEO of 4.3 V [21]. Even though GaAsSb-based DHBTs eliminate electron blocking at the base-collector heterojunction, GaInAs-based DHBTs remain highly competitive [14].

Further improvement of the device performance (in particular high-frequency figures-of-merit such as f_T and f_MAX) requires lateral and vertical scaling, together with an optimization of the epitaxial layer design [22,23]. Lateral scaling is beneficial to the reduction of RC charging delays. Vertical profile scaling of the epitaxial base and the collector layers reduces transit time delays. Transistor scaling necessarily involves an optimization of the device parasitics because they become progressively more significant with decreasing size of the devices. The fabrication process and the epitaxial layer design must therefore be improved to extend the transistor RF bandwidth.

1.2 Scope of Dissertation

The objective of this PhD thesis is to improve the high-frequency performance of InP/GaAsSb DHBTs while maintaining the reproducibility and high yield of the device fabrication.

The thesis is structured as follows:

Chapter 1: Introduction
Chapter 1 presents a brief overview of the transistor technology.

Chapter 2: Theory and Characterization Methods
This chapter focuses on the aspects that are of practical relevance in the DHBT operation principles: The main figures-of-merit, the parasitics extraction methods, the measurement systems and the extrapolation techniques used throughout this thesis are presented.

Chapter 3: Optimization of DHBT Fabrication Process
Chapter 3 contains two parts: Firstly, an overview of the conventional process flow is presented. In the second part, the different approaches to decrease the parasitic resistances and capacitances needed to improve high-frequency device performance are shown. Various combinations of wet chemical and dry etching methods involving ICP (Inductively Coupled Plasma), Ar sputtering and Ion Milling processes were optimized and compared in order to demonstrate that etching methods have an important effect on the device performance and the level of manufacturability.

Chapter 4: Epitaxial Layer Design
This chapter firstly investigates the influence of an energy launcher for the hot electron injection at the emitter/base interface. Secondly, the results of the vertical scaling of the base layer are presented. Thirdly, the effects of the compositional gradient of the base material on the DC and high-frequency characteristics of the GaAsSb-based DHBTs are discussed.

Chapter 5: Conclusions and Outlook
The results achieved in this thesis are discussed and summarized. Also, possibilities and suggestions for future work are given. Finally, an outlook for future THz bandwidth transistors is presented.

Chapter 2

Theory and Characterization

In this chapter, firstly the basic configuration as well as geometrical device parameters of the DHBT are presented. Secondly, the most widely used figures-of-merit for the DC and RF device performance are introduced and discussed. Finally, methods for characterization and data extrapolation are addressed.

2.1 Basics of DHBTs

Operation Principles

Most heterojunction bipolar transistors (HBTs) are triple-mesa devices, with one layer built on top of the other like a pyramid (Fig. 2.1): The upper layer always acts as a mask for the one below, therefore it is a self-aligned process [24]. The emitter and the base-collector mesas form the transistor, while the third mesa is etched down to a semi-insulating substrate to provide an insulation between the devices. The transistor structure is designed emitter-up, since this layer sequence greatly simplifies the fabrication of the transistors for high-speed applications [25]. Transistors are usually operated in the active-forward mode (base-emitter junction forward-biased, base-collector junction reverse-biased). The active transistor area is located vertically below the emitter. In the active transistor area, the electrons injected into the base diffuse through it until

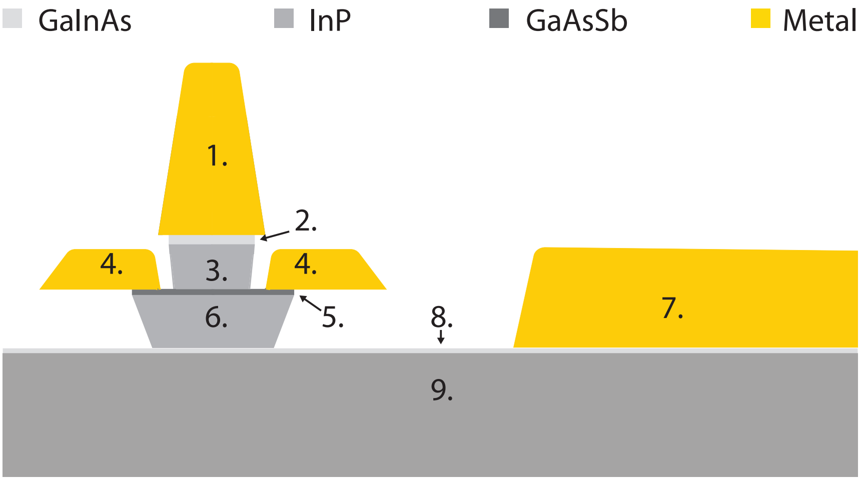


Figure 2.1 Schematic representation of the cross-section of the conventional DHBT structure. Legend: 1. Emitter Contact Metal 2. Emitter Contact Layer 3. Emitter (n) 4. Base Contact Metal 5. Base (p) 6. Collector (n) 7. Collector Contact Metal 8. Collector Contact Layer 9. Sub-Collector (n+)

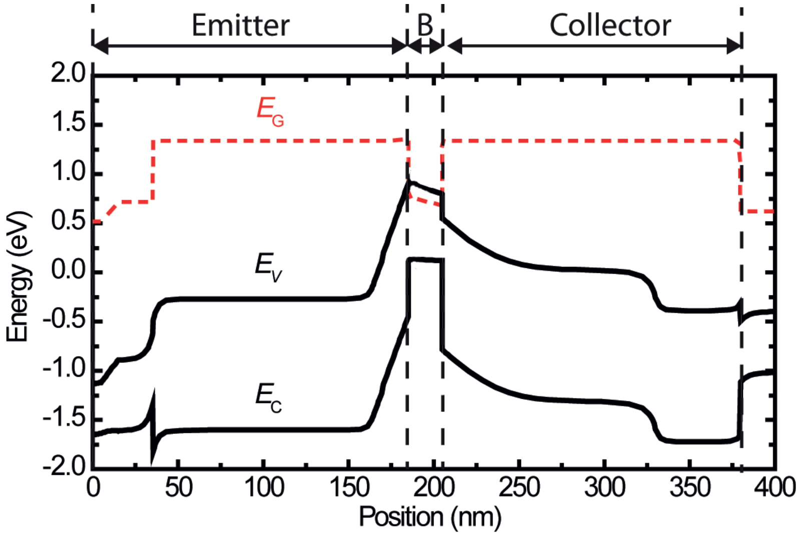


Figure 2.2 Equilibrium band diagram of an $\mathrm{InP/GaAs}_x\mathrm{Sb}_{1-x}\mathrm{/InP}$ DHBT

they reach the base-collector junction. From there, electrons are extracted towards the collector.

The InP/GaAsSb DHBT energy band diagram at equilibrium is shown in Fig. 2.2. It consists of an InP emitter, a $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base and an InP collector epitaxial layers [26, 27]. The base layer has a non-constant composition. The purpose of the compositional grading is to generate an electron drift field and thus to reduce the base transit time. Mostly, over the course of this work, a base with a linear composition and a doping grading from $x = 0.4$ ($N_\mathrm{B} \approx 4.5 \times 10^{19}$ cm^{-3}) to $x = 0.6$ ($N_\mathrm{B} \approx 9.2 \times 10^{19}$ cm^{-3}) was used. The doping is higher at the base-emitter interface, which enables low contact resistance and thus good base contacts. Other base compositions will be addressed in Chapter 4.

The As fraction x increases from the collector to the emitter side. Thus, the slope of the conduction band in the base creates an accelerating quasi-electric field that pushes electrons towards the collector. The type-II InP/GaAsSb heterojunction between the emitter and the base layer results in conduction and valence bands discontinuities of $\Delta E_\mathrm{C} \approx 0.10$ and $\Delta E_\mathrm{V} \approx 0.73\,\mathrm{eV}$, respectively. To minimize electron blocking at the step-up in the conduction band alignment, Ga is added to the InP emitter at the base interface. The edge of the conduction band of the $\mathrm{Ga}_{0.22}\mathrm{In}_{0.78}\mathrm{P}$ emitter region is aligned to the conduction band of the $\mathrm{GaAs}_{0.60}\mathrm{Sb}_{0.40}$ base layer. The valence band edge at the heterojunction $\mathrm{Ga}_{0.22}\mathrm{In}_{0.78}\mathrm{P}/\mathrm{GaAs}_{0.6}\mathrm{Sb}_{0.4}$ has a large offset which practically eliminates the back-injection of the holes from the base into the emitter. Additionally, the valence band discontinuity enables high base and low emitter doping levels. This allows a significantly reduced base-emitter capacitance and base resistance. The InP collector with a wide-bandgap of $E_\mathrm{G} \approx 1.35\,\mathrm{eV}$ provides a high breakdown voltage and therefore a high output power [28, 29]. The collector layer is followed by a heavily doped sub-collector to provide good collector contact with low sheet resistance.

DHBT structure

The schematic of the conventional DHBT structure is shown in Fig. 2.3. The dimensions of the final device are mainly determined by the emitter length L_E, the emitter width W_E and the width of the base metal contact $W_\mathrm{B,M}$. They are defined by electron beam lithography which provides an

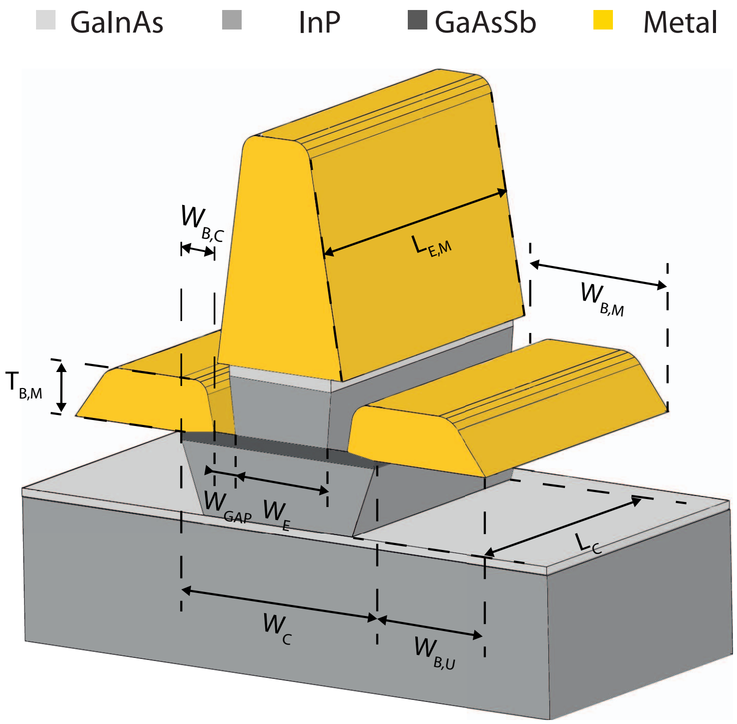


Figure 2.3 3D Schematic representation of the conventional DHBT structure

alignment accuracy within 40 nm. Device dimensions play a significant role in the device performance [30, 31]. With scaling down, the extrinsic base surface recombination starts to play a dominant role in the total base recombination, causing degradation of the current gain [32–34]. Also, the capacitances and resistances distributed along the perimeter of the active device become progressively more significant with scaling, and thus limit the high-frequency device performance.

For an optimal bipolar transistor operation, the ratio of the base-emitter and the base-collector junction areas need to be close to unity. Therefore, to eliminate the negative effect of the base-collector capacitance, the base and the collector epitaxial layers are underetched by $W_{\mathrm{B,U}}$ [35]. At the same time, in order to provide a good base contact, the intersection of the base metal and the semiconductor base layer $W_{\mathrm{B,C}}$ should be no less than the effective transfer length $L_{\mathrm{T,E}}$. The transfer length is given by

$$L_{\mathrm{T,E}} = \sqrt{R_{\mathrm{B,C}}/R_{\mathrm{SH,B}}}, \tag{2.1}$$

where $R_{\mathrm{B,C}}$ and $R_{\mathrm{SH,B}}$ are the contact and sheet resistance of the base, respectively. For a value of $R_{\mathrm{SH,B}} = 1024\,\Omega/\square$, the minimum value of $W_{\mathrm{B,C}}$ is $\approx 50\,\mathrm{nm}$. The device dimensions are connected through the following relations

$$W_{\mathrm{B,M}} = W_{\mathrm{B,C}} + W_{\mathrm{B,U}} \tag{2.2}$$

$$W_{\mathrm{C}} = W_{\mathrm{E}} + 2 \cdot (W_{\mathrm{B,C}} + W_{\mathrm{GAP}}) \tag{2.3}$$

The region between the base contact and the emitter mesa is called base access distance W_{GAP}. The width of the base access distance is determined by the undercut of the emitter stripe from the long side. The base access resistance is a function of W_{GAP}. Therefore, the reduction of the base access distance is necessary for the reduction of the base access resistance.

The cross-sectional area of the base metal stack $A_{\mathrm{B,M}}$ is inversely proportional to the base metal resistance. Thus, the thickness of the base metal stack $T_{\mathrm{B,M}}$ needs to be maximized in order to reduce the base metal resistance. At the same time, $T_{\mathrm{B,M}}$ is limited by the emitter mesa height: if the metal stack is too high, a base-emitter short-circuit might occur.

The base access resistance, base contact resistance and base metal resistance significantly contribute to the base-collector charging time $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ and therefore limit the maximum frequency of oscillation f_{MAX}.

The collector width W_{C}, in the conventional DHBT fabrication process, is determined according to Eqn. 2.3. There are other fabrication approaches that allow the choice of the W_{C} to be independent from the other device parameters. Those methods are: Introducing the GaInAs etch-stop layer after the collector layer [36, 37] and the transferred substrate approach [38–40]. To optimize cutoff frequencies, the collector width needs to be comparable to the emitter width. This will allow the f_{MAX} to benefit from the reduced base-collector capacitance. At the same time, additional modifications of the transistor structure need to be implemented to avoid a reduction of the f_{T} and the f_{MAX} from a suppressed collector current spreading and an increased base resistance. However, the aforementioned methods make the fabrication process more complicated and do not result in a significant improvement of the high-frequency device performance.

2.2 DHBT Figures-of-Merit

2.2.1 DC Characteristics

For the characterization of the DC properties of DHBTs, mainly three characterizations are used: measurements of the Gummel plot, of the I–V curves and of the Breakdown Voltage.

Gummel Plot

During Gummel characteristics measurements, a forward voltage V_{BE} is applied to the base-emitter diode, while the base-collector diode is kept at zero $V_{\mathrm{BC}} = 0\,\mathrm{V}$. The measured parameters are the base I_{B} and the collector I_{C} currents. The currents are plotted on a logarithmic scale versus the base-emitter voltage V_{BE}. The ratio of the two currents defines the common-emitter current gain β. In the ideal case of two perfect diodes, we would have a linear dependence with a constant gain. In actual devices, the emitter current gain β has a clear peak. Typical Gummel characteristics are plotted in Fig. 2.4 (a).

The currents I_{C} and I_{B} are defined by the diode equation

$$I_{\mathrm{C}} \approx I_{\mathrm{S,C}} \cdot (e^{V_{\mathrm{BE}}/n_{\mathrm{C}} \cdot V_{\mathrm{TH}}}) \tag{2.4}$$

and

$$I_{\mathrm{B}} \approx I_{\mathrm{S,B}} \cdot (e^{V_{\mathrm{BE}}/n_{\mathrm{B}} \cdot V_{\mathrm{TH}}}) \tag{2.5}$$

where $V_{\mathrm{TH}} = kT/q$. The base and collector saturation currents $I_{\mathrm{S,B}}$ and $I_{\mathrm{S,C}}$ are given by the intersection of I_{B} and I_{C} with the y-axis and can be directly read from the logarithmic scale. The emission coefficient or the ideality factor n is another common characteristic of the Gummel plot. In the ideal case, n is equal to 1 for I_{B} as well as for I_{C}. At low currents, the parasitic base recombination current affects I_{B} and the ideality factor becomes > 1. At high currents, effects such as series resistances, thermal effects as well as reverse injection of the holes tend to induce from the exponential behavior and lead to current saturation.

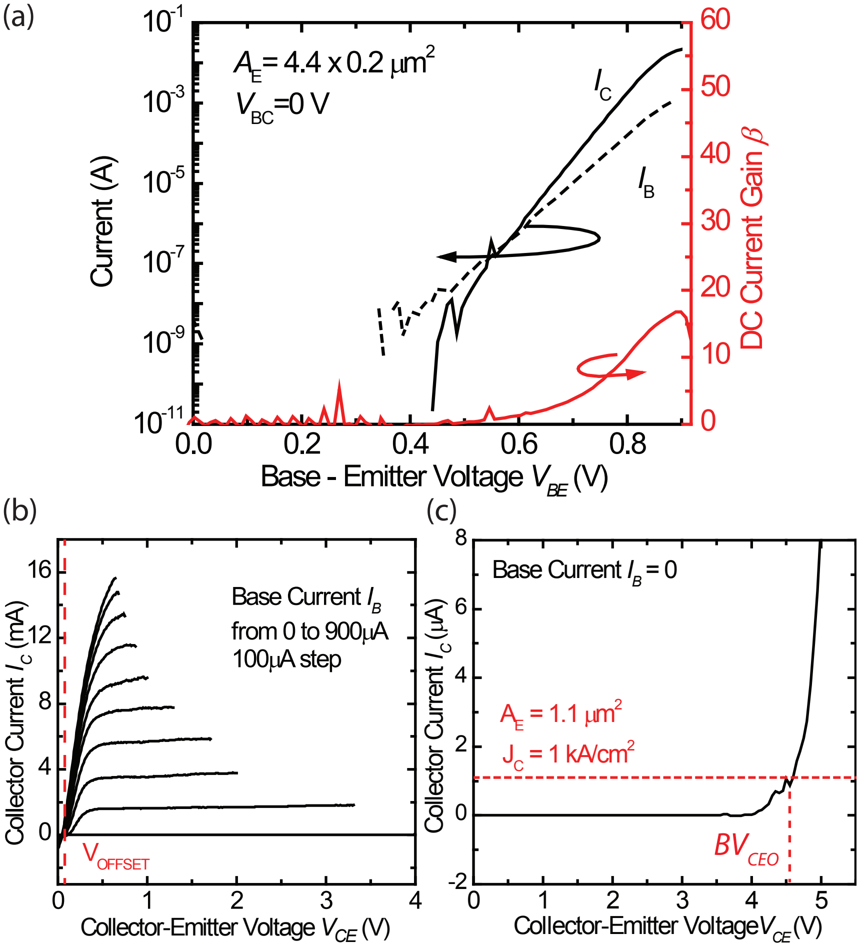


Figure 2.4 (a) Gummel characteristics of a DHBT. Left scale: Base I_B and collector I_C currents. Right scale: Emitter current gain β of the same device. (b) Common-emitter currentvoltage characteristic of a DHBT. (c) Breakdown Voltage BV_{CEO} definition

We want the DHBTs to have a high ratio of the emitter electron current to total current. Therefore, it is desirable that no carriers recombine at the base-emitter junction, since those will be lost. Recombination effects such as the base minority carrier bulk recombination, the recombination in the base-emitter space charge region and the base surface recombination have a strong negative influence on the common emitter current gain β. The minority carrier bulk recombination current is proportional to the base doping density. In InP/GaAsSb DHBTs, the current gain values are limited by the use of narrow bandgap heavily doped bases [41]. Also, geometrical device parameters play a significant role in the magnitude of the parasitic recombination currents. First of all, the bulk recombination current increases with the base thickness. Secondly, the lateral device sizes such as the emitter width and the length govern the surface recombination current which increases when the ratio of the emitter periphery to emitter area grows.

Apart from the parasitic currents, I_{B} and I_{C} and hence β suffer from extrinsic resistances and self-heating effects. For practical high-frequency DHBTs, maximizing the current gain β is not a primary goal, but it should be not less than 10 for normal device operation.

I–V Curves

For the I–V output curves, the collector current is measured as a function of the collector-emitter voltage V_{CE} with the base current as a fixed parameter $I_{\mathrm{C}} = f(I_{\mathrm{B}},V_{\mathrm{CE}})$, where I_{B} is increased from curve to curve in equal steps. Typical I–V characteristics are plotted in Fig.2.4 (b). The I–V output curves are very helpful in the analysis of the transistor behavior as well as in the quality control of the device fabrication process. The magnitude of the collector-emitter voltage when I_{C} becomes larger than zero is known as the offset voltage V_{OFFSET}. The offset voltage sets a lower bound for the collector-emitter knee voltage. A large V_{OFFSET} leads to a large knee voltage and a high power consumption in the circuits. In the DHBTs, the offset voltage is mainly influenced by the band alignment and the geometrical asymmetry of the base-emitter and the base-collector heterojunctions. But there are other factors that affect the V_{OFFSET}: For example, the magnitude of the offset voltage is known to be dependent on β [42,43]. Also, the base surface treatments during the fabrication process may cause an increased surface roughness and thus an increased extrinsic recombination which leads to a higher offset voltage.

I-V curves can be used to parametrize self-heating effects and help estimate their influence on the device performance.

Breakdown Voltage

During the breakdown voltage BV_{CEO} measurements, I_{B} is equal to zero and V_{CE} is increased until $I_{\mathrm{C}}/A_{\mathrm{E}} = 1\,\mathrm{kA/cm^2}$, where A_{E} is the emitter area. Fig. 2.4 (c) shows the BV_{CEO} of a DHBT fabricated in the course of this work. InP/GaAsSb DHBTs are known to have a high BV_{CEO} due to the wide-bandgap InP collector [42–44]. In the wide-bandgap collector, electrons need more kinetic energy in order to generate electron-hole pairs by impact ionization, thus enabling higher values of breakdown voltage. The breakdown voltage depends on the collector doping and thickness. BV_{CEO} increases as the doping is reduced: Stronger electric fields arise at the base-collector junction. The collector thickness determines the width of the depletion region, and thus limits the breakdown voltage.

The breakdown voltage is not an absolute limit to the RF voltage swing: It is possible to operate the device with a larger voltage swing if the base current is not constant, in other words, if holes generated by impact ionization are allowed to escape through the base contact. The main degradation mechanism is the thermal destruction, so if the RF signal is faster than the internal device heating, the voltage swing might be increased above the BV_{CEO} value [45].

2.2.2 RF Characteristics

The two most important figures-of-merit for high-speed DHBTs are the current gain cutoff frequency f_{T} and the maximum oscillation frequency f_{MAX}. In this section, we briefly introduce these concepts and discuss the influence of the physical device dimensions on RF device performance.

Current Gain Cutoff Frequency

The unity current gain frequency f_{T} in the common-emitter configuration, can be approximated by the following equations [46,47]

$$f_{\mathrm{T}} = \frac{1}{2\pi\tau_{\mathrm{EC}}}, \tag{2.6}$$

where τ_{EC} is the sum of the delay times associated with the diffusion through the base region, the drift through the collector depletion region, the emitter and the base-collector RC time delays

$$\tau_{\mathrm{EC}} = \tau_{\mathrm{B}} + \tau_{\mathrm{C}} + C_{\mathrm{BE}}r_{\mathrm{E}} + (C_{\mathrm{BC,E}} + C_{\mathrm{BC,I}})(r_{\mathrm{E}} + R_{\mathrm{EE}} + R_{\mathrm{C}}). \tag{2.7}$$

This commonly applied approximation of the transit frequency is derived from the T-topology small-signal equivalent circuit. The InP/GaAsSb DHBTs, fabricated with the current device technology, are mainly limited by base transit time τ_{B}, the collector delay time τ_{C} and the emitter time delay RC product C_{BE} r_{E}. Therefore, in order to maximize the f_{T}, we need to reduce the time that electrons spend in the base and the collector layers.

One approach would be to reduce the thickness of the layers. The reduction of the base layer thickness decreases the travel distance for the electrons. However, a thinner base layer causes a significant increase in the base resistance, which has a negative influence on the f_{MAX}. In Chapter 4, the influence of the base thickness on the device performance is presented in more detail.

Vertical scaling of collector layer provides shorter transit delays, though the base-collector capacitance increases. Another advantage of a thinner collector with a higher doping is the reduction of the current spreading in the collector. To be beneficial, vertical scaling needs to be implemented in conjunction with the lateral reduction of the collector dimensions. This will enable an improvement of the f_{T} due to a shorter collector delay time and, at the same time, the f_{MAX} will not suffer from the increased base-collector capacitance per unit area. Also, the collector delay time is significantly bias-dependent due to a non-linear dependence of the electron velocity on the electric field. Therefore, devices with thinner collectors need to be operated with lower collector-emitter voltages in order to provide τ_{C} reduction compared to devices with thicker collector. Thus, both of the cutoff frequencies are dependent on the collector thickness and therefore vertical scaling needs to be considered with respect to the application of the DHBTs.

As previously stated, another approach to decrease the base transit time is to introduce an electron accelerating field across the base layer. This can be done through grading of the base doping and/or the base composition [36, 48]. The quasi-electric field accelerates the electrons that are injected into the base toward the collector. Also, an accelerating field in the base can reduce the minority carrier bulk recombination by decreasing the time that electrons spend in the base layer.

The base transit time is influenced by the minority carrier mobility in the base material. The density-of-states effective mass for electrons in the L-valleys is much higher than in the Γ-valley, which means their mean free path and mobility are much lower. It was shown, that in GaAsSb at the p-doping density of 1.0×10^{20} cm^{-3} already one third of the minority carriers occupied the L-valleys [49]. Moreover, if in the Γ-valleys between GaAsSb base and InP collector there is a step down for the L-valleys, the conduction bands alignment forms a step up. Thus, it can lead to the electron blocking effect for the L-valleys and to the Γ-to-L-valleys scattering. Both result in a decreased performance of the devices.

An electron accelerating field in the base layer can enhance this effect. The reason is, that the energy separation between the Γ- and L-valleys in GaAsSb ($\approx 120\,\mathrm{meV}$) is small in comparison to the energy that electrons gain due to the sum of the electric and quasi-electric fields [49].

The question of the base grading and influence of it on the current gain cutoff frequency f_T is addressed in more detail in Chapter 4.

Maximum Oscillation Frequency

The maximum frequency of oscillation can be approximated as a function of the f_T and the equivalent circuit parameters [50]

$$f_\mathrm{MAX} = \sqrt{\frac{f_\mathrm{T}}{8\pi(R_\mathrm{B}C_\mathrm{BC})_\mathrm{EFF}}}, \tag{2.8}$$

where

$$(R_\mathrm{B}C_\mathrm{BC})_\mathrm{EFF} = R_\mathrm{B,I}C_\mathrm{BC,I} + R_\mathrm{B,E}(C_\mathrm{BC,E} + C_\mathrm{BC,I}) \tag{2.9}$$

$(R_\mathrm{B}C_\mathrm{BC})_\mathrm{EFF}$ is a time constant that includes not only the effects of the

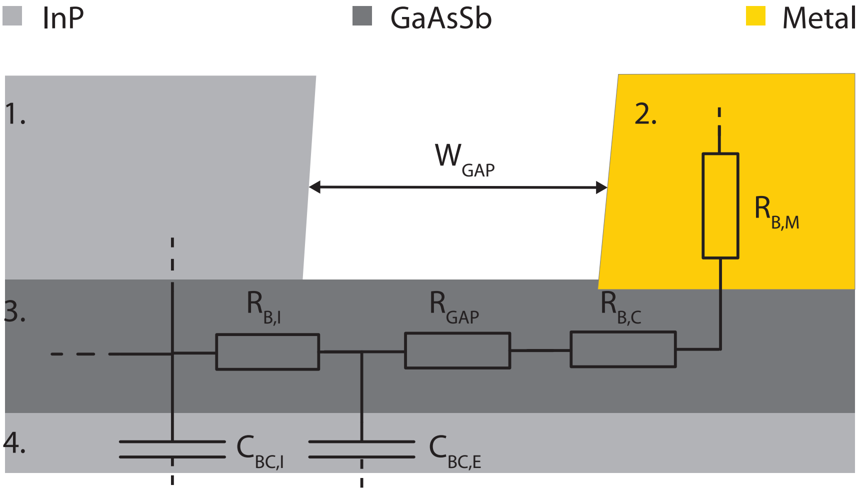


Figure 2.5 A simplified schematic cross-section of a conventional DHBT structure with labeled components of base resistance and base-collector junction capacitance. For simplicity, the details of the collector and sub-collector are not shown. Legend: 1. Emitter Layer 2. Base Contact Metal 3. Base Layer 4. Collector Layer

base resistance and base-collector capacitance, but also the effects of the parasitic emitter and collector resistances. While the f_{T} is limited by the intrinsic delay time of the electrons in the transistor, the f_{MAX} is limited by the time constant $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$. The maximum frequency of oscillation is very sensitive to the values of the extrinsic base-collector capacitance $C_{\mathrm{BC,E}}$ and to the extrinsic base resistance $R_{\mathrm{B,E}}$. The extrinsic collector does not play a significant role in the electron transport of the device, apart from introducing additional parasitic capacitance. However, the collector width needs to be greater than the emitter width in order to prevent a suppression of the collector current spreading. Therefore, the extrinsic collector cannot be completely removed. At the same time, we do not want to increase the base contact resistance so there is another limitation on the base-collector junction width. Experiments on the collector width optimization are discussed and presented in details in the thesis of our group [36, 37].

A partial schematic cross-section of a conventional DHBT structure shown in Fig. 2.5. The main components of the base resistance are the intrinsic base resistance $R_{\mathrm{B,I}}$, and the extrinsic base resistance $R_{\mathrm{B,E}}$. The intrinsic base resistance is defined by the following expression

$$R_{\mathrm{B,I}} = \frac{1}{12} \cdot R_{\mathrm{SH,B}} \cdot \frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}, \tag{2.10}$$

The intrinsic base resistance can be reduced by decreasing the base sheet resistance $R_{\mathrm{SH,B}}$. However, to lower base sheet resistance one usually has to increase the base doping which has a negative impact on the DC current gain.

In this thesis, we focused our efforts on minimizing the extrinsic base resistance, which can be described by the following expression

$$R_{\mathrm{B,E}} = R_{\mathrm{GAP}} + R_{\mathrm{B,C}} + R_{\mathrm{B,M}}, \tag{2.11}$$

where R_{GAP}, $R_{\mathrm{B,C}}$, $R_{\mathrm{B,M}}$ are the base access resistance, the base contact resistance and the base metal resistance, respectively. The base access resistance is proportional to the W_{GAP} and can be determined by

$$R_{\mathrm{GAP}} = \frac{1}{2} \cdot R_{\mathrm{SH,B}} \cdot \frac{W_{\mathrm{GAP}}}{L_{\mathrm{E}}}, \tag{2.12}$$

The current from the base contact has to cross the distance W_{GAP} to reach the active area of the device. Thus, the reduction of W_{GAP} is necessary to archive a low base access resistance. In the course of this work, we developed several approaches to reduce the base access distance and therefore significantly improved the f_{MAX} [20]. Through optimization of the emitter etching and the base contact evaporation parameters, the base access distance was reduced to $\approx 30\,\mathrm{nm}$. However, if the access distance is insufficient, the surface recombination increases, and thus the common-emitter current gain decreases. Chapter 3 addresses these experiments in detail.

The base contact resistance $R_{\mathrm{B,C}}$ can be expressed as

$$R_{\mathrm{B,C}} = \frac{1}{2} \cdot \frac{\sqrt{\rho_{\mathrm{B,C}} R_{\mathrm{SH,B}}}}{L_{\mathrm{E}}} \tag{2.13}$$

As seen from the equation above, the base contact resistance can be reduced by lowering the base contact resistivity $\rho_{\mathrm{B,C}}$. A reduced base contact resistivity was achieved by use of *in-situ* Ar sputtering immediately prior to the base contact deposition [51]. A detailed discussion of this approach is presented in Chapter 3.

The base metal resistance $R_{\mathrm{B,M}}$ increases rapidly with a decreasing cross-section metal area and can become the dominant contributor to the total base resistance. The conductance of the base electrode can be improved by increasing the thickness of the base metal stack $T_{\mathrm{B,M}}$. However, the base metal thickness is limited by the emitter mesa height.

2.3 Device RF Characterization

Measurement Methods

The high-frequency performance of the devices is evaluated by small-signal scattering parameter measurements –so called S-parameters. S-parameters are the elements of a matrix, describing the linear electrical behavior of a two-port network. f_{T} is the frequency at which the common-emitter current gain h_{21} drops to unity. Based on the measured S-parameters, h_{21} can be calculated as [37]

$$h_{21} = \frac{-S_{21}}{(1 - S_{11})(1 - S_{22}) + S_{12}S_{21}}, \tag{2.14}$$

The f_{T} is a function of a transistor operating point for a given collector-emitter voltage V_{CE}, the f_{T} increases with the collector current I_{C} to a certain critical collector current value. After passing the peak value, it decreases with increasing collector current.

Mason demonstrated that if a three-port device is embedded in a lossless reciprocal network and any two terminal-pairs are chosen as input (S_{11}, S_{12}) and output (S_{22}, S_{21}), then a certain quantity U remains invariant [50, 52]. The quantity U is defined as the maximally available power gain of a unilateralized structure and it is called the unilateral gain. The frequency at which U is equal to unity is called f_{MAX}. U can be expressed in terms of the S-parameters as

$$U = \frac{|(S_{21}/S_{12}) - 1|^2}{2(k|S_{21}/S_{12}| - \mathrm{Re}(S_{21}/S_{12}))}, \tag{2.15}$$

where k is the stability factor

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{21}S_{12}|}. \tag{2.16}$$

Measurement Setup

The S-parameters were measured from 0.2 to 67 GHz with either an Agilent N5245A PNA-X or from 0.2 to 40 GHz with a Hewlett Packard 8510C vector network analyzer. For the comparison, some devices were measured with HP8510 XF from 0.2 to 110 GHz. Both measurment methods yield comparable data in good agreement. Therefore, because it is less time consuming, most of the measurements were performed from 0.5 to 67 GHz. The vector network analyzer (VNA) was calibrated using the line-reflect-reflect-match technique and off-wafer impedance standards. The calibration of the VNA as well as the device measurement were performed with an absorption mat, in order to suppress parasitic modes.

De-embedding Method

After measuring the S-parameters in order to obtain the measurement of a single device, we need to subtract the contribution of the S-parameters of the pads. This process is called de-embedding. For this method, the S-parameters of two dummy structures (OPEN and SHORT) are measured in addition to the device. The OPEN and SHORT calibration structures are fabricated for each device size together with the devices on the same substrate. There are several methods to subtract the parasitics associated with the device probing pads. Two of them are known as the OPEN-SHORT and SHORT-OPEN deembedding. In this thesis, we used the *iterative de-embedding method*, which is described in detail in a thesis written in our group [37].

Extrapolation Method

The S-parameters, and hence U and $|h_{21}|^2$, can be measured only within a certain frequency range. This is due to the limited bandwidth of standard measurement equipment. The cutoff frequencies of modern DHBTs are approaching terahertz values. Therefore, the magnitudes of the cutoff frequencies are determined by single-pole transfer function fits to $|h_{21}|^2$

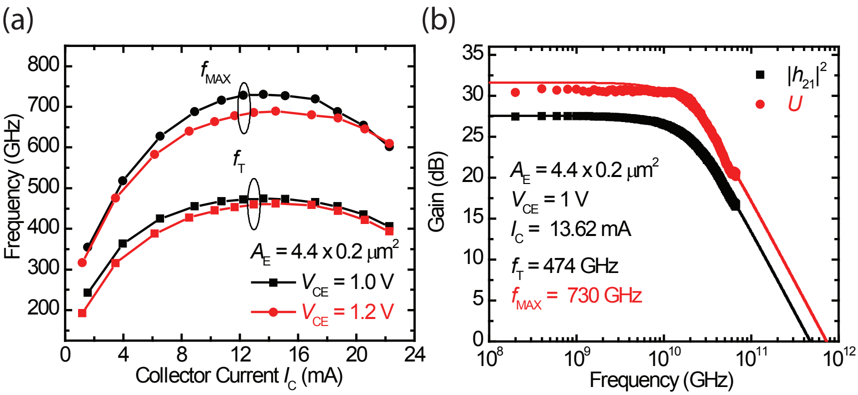


Figure 2.6 (a) Dependences of f_T and f_{MAX} on collector current at V_{CE} = 1 and 1.2 V (b) Extrapolation of f_{MAX} and f_T by single-pole transfer function fits

and U measured within a frequency range from 0.2 GHz to 67 GHz. In Fig. 2.6, the extrapolation of f_T and f_{MAX} from the measured U and $|h_{21}|^2$ is shown. The measured U and $|h_{21}|^2$ are plotted on a logarithmic scale versus the frequency. As depicted in the figure, first two single-pole transfer functions are fitted to the measured values, and then, their intercepts with the 0 dB line show the values of f_{MAX} and f_T, respectively.

2.4 Small-Signal Equivalent Circuit

The equivalent circuit based on the T-topology uses a distributed RC network which accounts for the transistor to intrinsic and extrinsic regions. It describes the small-signal linear behavior of a transistor around a given bias point. The values of the RC network components are determined from the measured S-parameters. The intrinsic part is associated with an active device and governs f_T, while the extrinsic part is a parasitic addition which limits the f_{MAX}. Inserting the complete S-parameters into the gain and RC network components formulas yields very complicated equations that are not easily used for analytical solutions. Hence, the simplified expressions Eqn. 2.6 and Eqn. 2.8 are introduced as approximations for f_T and f_{MAX}.

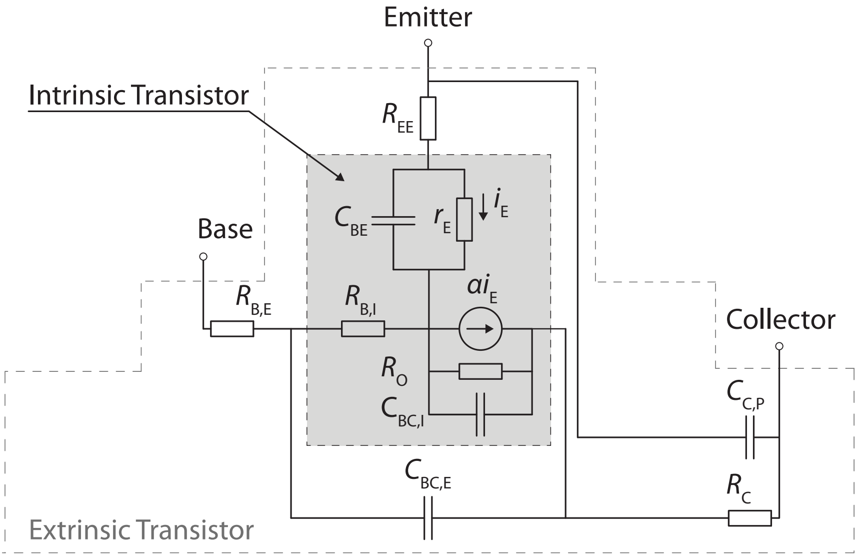

Emitter
Intrinsic Transistor
R_{EE}
C_{BE}
r_E
i_E
Base
$R_{B,E}$
$R_{B,I}$
ai_E
R_O
$C_{BC,I}$
Collector
$C_{C,P}$
$C_{BC,E}$
R_C
Extrinsic Transistor

Figure 2.7 Small-signal equivalent T-circuit of a common-emitter DHBT model. The grey-colored box represents the intrinsic, and dashed-line box the extrinsic transistor [53]

The small-signal T-equivalent circuit of a DHBT is shown in Fig. 2.7 [53]. This model is more closely related to the physical structure of the device and provides a good fit to the measured S-parameters at high frequencies [45]. To optimize and understand the device performance, we need to know the real physical values of the device components. However, the accurate extraction of the small-signal equivalent circuit elements of DHBTs is not a simple task.

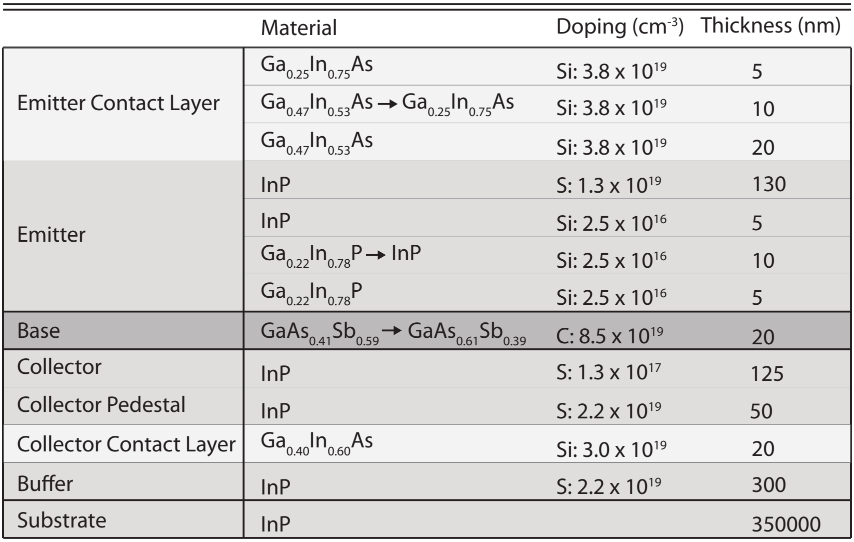
Chapter 3

Optimization of the DHBT Fabrication Process

The fabrication process is key to the electrical behavior of the transistor. Unfortunately, the conventional fabrication process limits the RF bandwidth of the DHBTs. Our main goal was to improve the high-frequency performance of the devices. In this pursuit, a special focus was put on the improvement of the f_{MAX} through optimization of the DHBTs fabrication process.

The fabrication of the DHBTs starts with epitaxial growth. Once the InP substrate is covered with the transistor semiconductor layers, it is processed in three cycles: Each cycle consist of lithographic patterning of the semiconductor layers, metallizing of the contact areas and then etching. The fabrication ends with a planarization process and by depositing the probe pads.

In this chapter, firstly, the conventional InP/GaAsSb DHBT epitaxial layer structure and characterization structures are presented. Secondly, the conventional fabrication method is introduced. Finally, the optimization of important process steps is discussed: a novel process for the base surface treatment, the reduction of the base access distance, the reduction of the excessive emitter end undercut and the passivation of the collector-base mesa.



	Material	Doping (cm^{-3})	Thickness (nm)
Emitter Contact Layer	$Ga_{0.25}In_{0.75}As$	Si: 3.8×10^{19}	5
	$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	Si: 3.8×10^{19}	10
	$Ga_{0.47}In_{0.53}As$	Si: 3.8×10^{19}	20
Emitter	InP	S: 1.3×10^{19}	130
	InP	Si: 2.5×10^{16}	5
	$Ga_{0.22}In_{0.78}P \rightarrow InP$	Si: 2.5×10^{16}	10
	$Ga_{0.22}In_{0.78}P$	Si: 2.5×10^{16}	5
Base	$GaAs_{0.41}Sb_{0.59} \rightarrow GaAs_{0.61}Sb_{0.39}$	C: 8.5×10^{19}	20
Collector	InP	S: 1.3×10^{17}	125
Collector Pedestal	InP	S: 2.2×10^{19}	50
Collector Contact Layer	$Ga_{0.40}In_{0.60}As$	Si: 3.0×10^{19}	20
Buffer	InP	S: 2.2×10^{19}	300
Substrate	InP		350000

Figure 3.1 The conventional InP/GaAsSb DHBT epitaxial layer structures that was used in this thesis

New fabrication steps were evaluated not only from a device performance point of view, but also from the perspective of homogeneity across the wafer, yield as well as reproducibility.

3.1 Epitaxial Layer Structure

The transistor material is grown by metalorganic chemical vapor deposition (MOCVD) in the ETH FIRST clean room. The conventional InP/GaAsSb DHBT epitaxial layer structure is shown in Fig. 3.1. The semiconductor layers are grown on 350 μm-thick semi-insulating (SI) InP:Fe (100) substrates with a diameter of 2 inches. A typical InP/GaAsSb DHBT is structured in three functional layers: the collector, the base and the emitter. The detailed description of each layer is presented below.

Sub-Collector and Collector

The buffer layer, the collector contact layer and the pedestal layer form the sub-collector of the transistor. The first layer on the semi-insulating InP substrate is a 300-nm-thick and highly n-doped InP buffer layer. It is doped at 2.2×10^{19} cm^{-3} and its purpose is to decrease the sheet resistance of the sub-collector. On the buffer layer, a collector contact layer is grown. It is a 20 nm thick $\mathrm{Ga_{0.40}In_{0.60}As}$ layer which is doped at 3×10^{19} cm^{-3} to enable a low contact resistance. The collector contact layer also serves as an etch-stop during base-collector mesa wet etching. A 50 nm thick InP:S pedestal layer doped at 2.2×10^{19} cm^{-3} is introduced in order to increase the mesa height. Thus, the parasitic base-collector capacitance is reduced.

The 125 nm thick InP collector layer is nominally doped with silicon at 1.3×10^{17} cm^{-3}. The collector doping should be low in order to provide a high BV_{CEO}. However, it should be high enough to achieve a high Kirk current density [36, 54].

Base

The 20-nm-thick $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base is compositionally graded from $x = 0.41$ on the collector side to $x = 0.59$ on the emitter side. The composition gradient leads to a bandgap variation which generates an accelerating quasi-electric field for electrons.

The average base doping density is 8.5×10^{19} cm^{-3}, resulting in $R_{\mathrm{SH}} = 1024\Omega/\square$. On the emitter side, the doping level is constant at $N_{\mathrm{B}} \approx 9.2 \times 10^{19}$ cm^{-3} to enable the low contact resistivity. The contact metal interdiffusion is not expected to significantly penetrate the GaAsSb base semiconductor material. Thus, the heavily doped part is only a few nanometers thick. The doping increases towards the emitter. On the collector side, the doping is $N_{\mathrm{B}} \approx 4.5 \times 10^{19}$ cm^{-3}. The doping gradient has two main benefits: Firstly, it generates an electron accelerating field across the base and secondly it reduces base recombination and hence increases the common emitter current gain β.

The influence of the base doping level, composition, and thickness on the DHBT performance is presented in Chapter 4.

Emitter

The composite GaInAs/InP/GaInP emitter consists of a 20-nm-thick GaInP/InP region, a 130-nm-thick n+ InP layer and 35-nm-thick n+ GaInAs contact layers. The purpose of the 15 nm thick $\mathrm{Ga}_y\mathrm{In}_{1-y}\mathrm{P}$ region is to align the conduction band of the emitter to the conduction band of the $GaAs_{0.60}Sb_{0.40}$ base layer. The first 5 nm of the ternary alloy have $y = 0.22$. The grading decreases to $y = 0$ over 10 nm towards the emitter surface side. A 5 nm thick InP layer is inserted as a doping transition layer. The 5 nm thick $Ga_{0.22}In_{0.78}P$:Si, the 10 nm thick graded $Ga_yIn_{1-y}P$ and the 5 nm thick InP are doped at 2.5×10^{16} cm^{-3}. The GaInP/InP region is followed by a 130 nm thick n+ InP:Si emitter layer which is doped at 1.3×10^{19} cm^{-3}. The n+ InP layer provides the mesa height needed to enable the self-aligned deposition of the base electrodes without a base-emitter short-circuit. The last layers of the composite emitter are the contact layers. The 35 nm thick emitter contact layer is doped at 3.8×10^{19} cm^{-3} and consists of 20 nm of $Ga_{0.47}In_{0.53}As$ lattice matched to InP, followed by 10 nm of $Ga_{0.47}In_{0.53}As$ graded to $Ga_{0.25}In_{0.75}As$, and 5 nm of $Ga_{0.25}In_{0.75}As$. The In rich contact layer is introduced to improve the contact resistivity.

3.2 Test Structures for Characterization

The epitaxial structure of the DHBT material is quite complex. Therefore, multiple calibration wafers are used to make sure that all layers possess the designed parameters. The thickness and the composition of the layers are determined by X-ray diffraction measurements. The doping densities are obtained from the Hall or C-V measurements. After the growth of the DHBTs, the following two test structures were fabricated: quick DHBTs and TLM test structures. Those structures enable to perform a relatively simple and fast characterization of the transistor material.

QDHBTs

Quick DHBTs (QDHBTs) are large-area DHBTs with emitter sizes of 20×30, 40×40, and 80×80 μm^2 used to characterize the properties of DHBT layers. Their name is derived from the fact that the fabrication time of the QDHBTs is much shorter in comparison to DHBTs. The fabrication is simple and reproducible: It consists of three optical lithography and two wet-etching steps with a common final metallization of the emitter, base and collector [55]. In this thesis, the fabrication process of the QDHBTs was kept unchanged, thus allowing a comparison of the transistor material of different MOCVD growth runs.

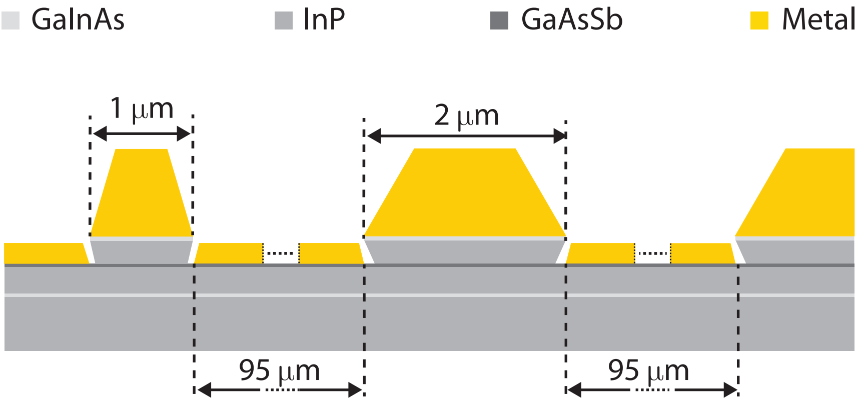


Figure 3.2 Simplified schematic cross-section of the pinched TLM test structure

Transmission Line Measurements

The TLM test structures are fabricated together with the QDHBTs on the same substrate. Four-point transmission line method (TLM) measurements are used to determine the contact resistivity and the sheet resistance of the emitter, base and collector layers [56]. However, the accuracy of the conventional TLM depends greatly on the fabrication process. It is especially important when the base contact resistivity and sheet resistance of the DHBT need to be determined precisely. The base surface treatment prior to the deposition of the base metal stack significantly contributes to the base contact quality.

To avoids these difficulties, TLM structures with emitters, so-called *pinched* TLM structures [57, 58] were used as an alternative for the base contact resistivity measurements. A simplified schematic cross-section of the pinched TLM structure is shown in Fig. 3.2. The fabrication process of the pinched TLM structures consists of the same self-aligned process used for the base-emitter mesa formation of the DHBTs (see Section 3.3). In this TLM structure configuration, the emitter layer acts as a mask for the base contact metal deposition and covers the base semiconductor surface of each TLM spacing. As an effect, no additional surface states are formed and thus the base sheet resistance can be determined more accurately. However, this method is more time consuming than the conventional TLM fabrication process. It is therefore not optimal for a rapid characterization of the layer quality.

3.3 Conventional Process Flow

In our fabrication process, the emitter and base electrodes are defined using electron beam lithography. The remaining lithography steps are made by optical printing. All metal stacks are formed by electron beam evaporation and a lift-off process.

Emitter Mesa and Contact Metal

The emitter electrode post consists of a Ti (5 nm)/Pt (30 nm)/Au (400 nm) metal stack. During the metal evaporation, the resist window gradually closes, which results in trapezoid metal shape as shown in Fig. 3.3 (a). After the emitter metal deposition, the emitter mesa is etched in a self-aligned manner using a combination of a dry and wet etching to expose the base surface. The first ≈ 80 nm of the GaInAs/InP emitter are etched anisotropically using the ICP-RIE system with a Cl_2/N_2 gas mixture. The remaining InP is isotropically wet etched using an HCl/H_3PO_4 solution. The GaInAs emitter contact layer acts as a mask in the InP wet etching step and thus determines the width of the emitter-base junction. The emitter mesa after the etching is shown in Fig. 3.3 (b).

Base-Collector Mesa and Contact Metal

Prior to the base metal deposition, the interface layer between the GaAsSb base and the emitter is removed using an HCl (32%) solution [55]. The base metal is evaporated in a self-aligned process, where the emitter metal acts as a mask, as shown in Fig. 3.3 (c.1) The base metal stack consists of Pd (2 nm)/ Ni (10 nm)/ Pt (10 nm) and Au (110 nm) [59, 60]. At the emitter end, the base electrode is connected with a micro-airbridge to a landing pad for the contact post, as shown in Fig. 3.3 (c.2).

After the base metal deposition, the emitter side-wall and the base access region are passivated with a ≈ 220 nm thick isolating SiN_x layer. The SiN_x is deposited by the low-temperature PECVD system. To remove the SiN_x from the metal contacts and the base semiconductor surface, it

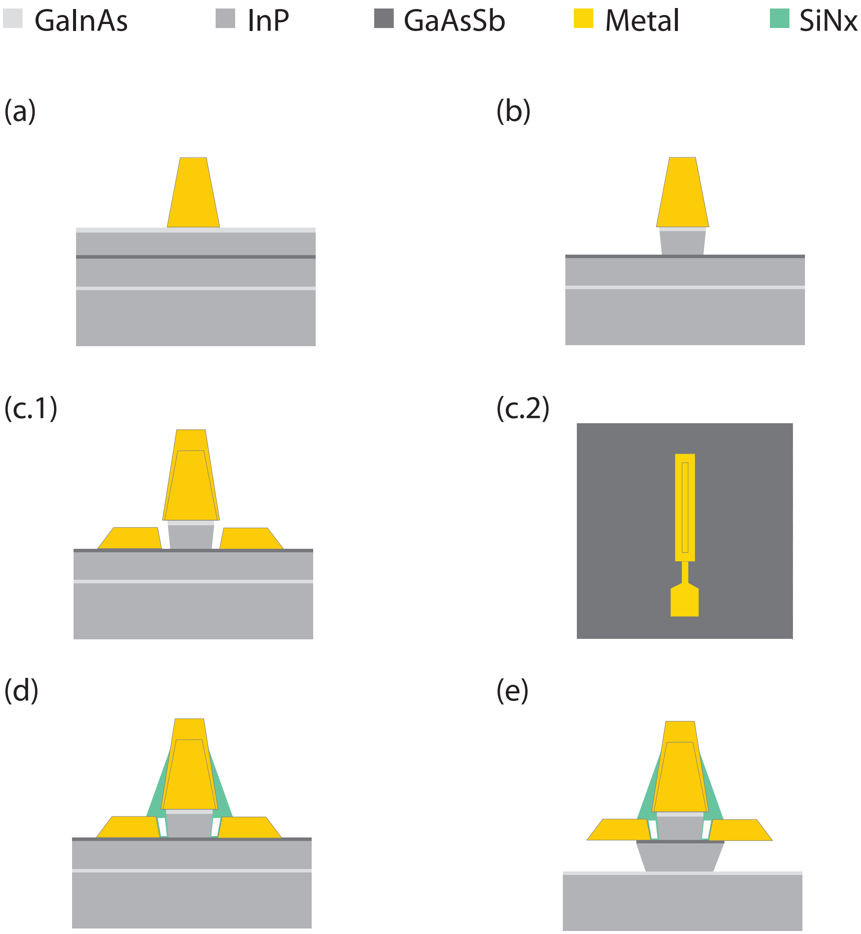

GaInAs
InP
GaAsSb
Metal
SiNx
(a)
(b)
(c.1)
(c.2)
(d)
(e)

Figure 3.3 Schematic representation of the conventional process flow (a) Emitter metal stack deposition (side view) (b) Emitter mesa etching (side view) (c) Base metal stack deposition ((c.1) side view, (c.2) top view) (d) SiNx passivation of the base-emitter mesa (side view) (e) Base-Collector mesa etching (side view)

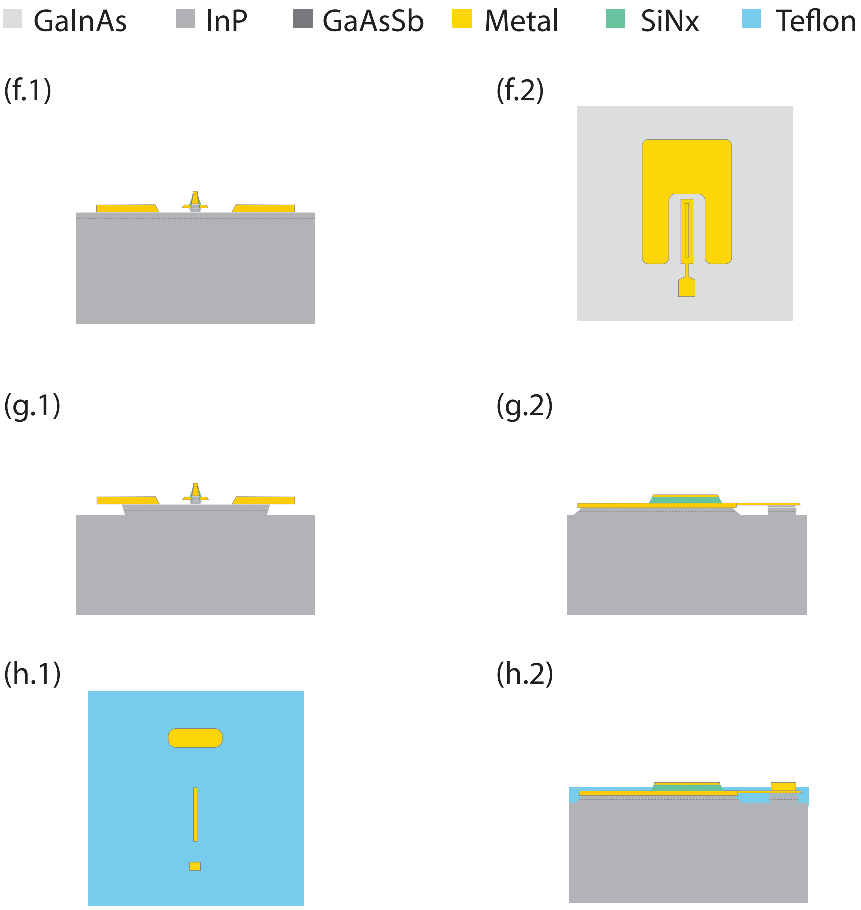

GaInAs
InP
GaAsSb
Metal
SiNx
Teflon
(f.1)
(f.2)
(g.1)
(g.2)
(h.1)
(h.2)

Figure 3.3 (cont.) (f) Collector metal stack deposition ((f.1) side view, (f.2) top view) (g) Isolation mesa etching ((g.1) side view, (g.2) side view) (h) Teflon planarization ((h.1) top view, (h.2) side view)

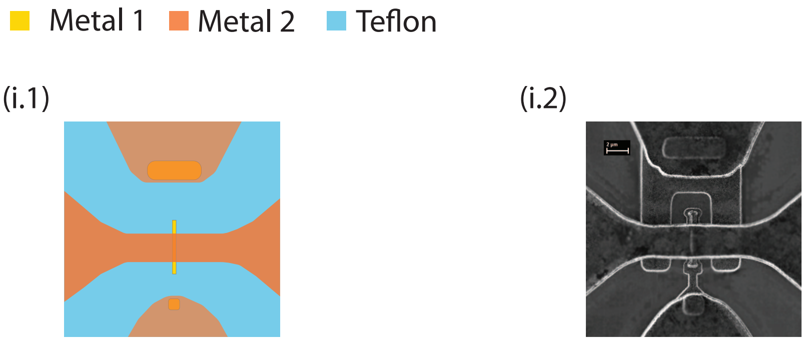


Figure 3.3 (cont.) (i.1) Schematic of the finished DHBT with the GSG probe pads (top view), (i.2) SEM image of the finished DHBT with the GSG probe pads (top view)

is over-etched using the RIE system in a CF_4 gas. The emitter side-wall and the base access region stay protected with a $\approx$ 30 nm thick SiN_x layer because the emitter metal acts as a shadow mask. Fig. 3.3 (d) shows the device structure after the SiN_x passivation. The SiN_x layer not only protects the emitter mesa during the following etching steps but also reduces the base surface recombination at the base access region [61].

The base metal acts as a mask during the etching of the base-collector mesa. The etching process includes dry and wet etching. Firstly, $\approx$ 40 nm of the GaAsSb/InP layer are anisotropically etched by using the ICP-RIE system with a $CH_4/Cl_2/H_2/Ar$ gas mixture. Secondly, the GaAsSb base layer is selectively under-etched to achieve the desired base-collector mesa width. The base resistance is unaffected by this process, even if the outer portion of the base under the base contact is etched away. The intersection of the base metal and the semiconductor base layer should be larger than the effective transfer length in order to provide a good ohmic contact [62]: The lateral base current component mainly flows inside the metal, due to its lower resistance, and enters the semiconductor base layer only near the inner edge of the metal. The transfer length for contacts on the base material described in Section 3.1 is approximately 50 nm. This sets the maximum limit for the base undercut $W_{\mathrm{B,U}}$. Finally, the InP is wet etched down to the GaInAs collector contact layer, as shown in Fig. 3.3 (e).

The collector contact is defined by optical printing and consists of Ti (10 nm)/ Pt (30 nm) / Au (300 nm). The thickness of the gold layer was chosen so that the collector electrode is the same height as the the base contact metal, as shown in Fig. 3.3 (f.1) and 3.3 (f.2).

The conductive GaInAs contact layer and InP buffer around the device area are etched away to provide an electrical isolation between devices. At the same time, it is important to remove all the conductive layers below the base micro-airbridge, because those layers contribute to the parasitic base-collector capacitance and thus reduce f_{MAX} [63, 64]. During the isolation etching, the active area of the device is protected by a photoresist mask. Fig. 3.3 (g.1-2) illustrates the device structure after the isolation mesa etch.

Planarization and Probe Pad Metal

After the isolation mesa etch, the transistor is finished, but in order to measure the S-parameters of a single device, probe pads are needed. The probe pads are relatively large in comparison to the device size. Hence, to provide sufficient mechanical support for the GSG probe pads and to avoid the short circuit between the device terminals, four additional steps are required: Firstly, the contact posts are deposited on the top of the base landing post and collector contact. The contact post provides access to the device terminals after the planarization. It consists of Ti (10 nm)/Pt (30 nm)/ Au (600 nm). Secondly, a layer of Teflon AF (amorphous fluropolymer) is spin-coated onto the substrate to planarize the devices [65, 66]. Thirdly, using an O_2 plasma, Teflon is etched down until the emitter contact, the base and the collector contact posts are exposed, as shown in Fig. 3.3 ((h.1) side view, (h.2) top view). Finally, the probe pad metal for the GSG probes is deposited. It consists of Ti (10 nm) and Au (900 nm). Fig. 3.3 illustrates the final device schematic (i.1) and shows the SEM image of the device (i.2).

3.4 Base Contact Optimization

For a given current gain cutoff frequency f_{T}, the maximum oscillation frequency f_{MAX} is determined by the base-collector capacitance and the base resistance as shown in Eqns. 2.8. - 2.13. Further improvement of the maximum oscillation frequency requires a reduction in the base-collector junction capacitance and/or base resistance. One of the components of the base resistance is the base contact resistance $R_{\mathrm{B,C}}$ which is proportional to the base contact resistivity, as shown in Eqn. 2.13. Thus, a reduction of the base contact resistivity is essential for the fabrication of high-speed DHBTs. In this section, the optimized and simplified base pre-metallization surface treatment is presented. The base surface at the intersection with the base metal must be pristine: Resist/developer chemistry as well as electron beam lithography cause surface contamination, increasing the resistivity of the base contacts. The contamination, due to a prior process steps, needs to be removed by base Ar sputtering. An additional advantage of the Ar pre-metalization base treatment is that it is performed *in-situ*, i.e. inside the chamber of the electron beam evaporation system. Therefore, the base surface is not exposed to the ambient environment before the contact evaporation and the contamination of the base contact area is minimized.

Ar sputtering is a physical process, which means that it is highly directional and not selective. Because the emitter contact acts as a mask during the Ar sputtering process, the gap region between the base contact and emitter mesa is not etched, as illustrated in Fig. 3.4 (a). However, it removes about 10 nm of the GaAsSb layer (including the natural oxide and the interface layer between the GaAsSb base and the emitter) in the base contact area. This enables one to omit the HCl solution base surface pre-treatment. In the conventional fabrication process, the emitter mesa is not protected, and hence is exposed to the concentrated HCl solution during the base surface pre-treatment. The etching solution attacks the InP emitter end and thus reduces the designed emitter length. The Ar pre-metalization base surface treatments are performed on the 20 nm thick, compositionally graded $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base as described in Section 3.1. For contact resistivity measurements, linear pinched TLM test structures are used. The pinched TLM test structures have 95×95 μm^2 contact pads and contact spacings ranging from 1 to 10 μm, as shown in Fig. 3.2. Fig. 3.4. (b) shows the SEM image of the cross-section of the pinched TLM test structure with the contact spacing 1 μm. The pinched TLM structures are defined by EBL in order to keep the same resist/developer chemistry as during DHBTs fabrication process. The TLM contact spacings are deter-

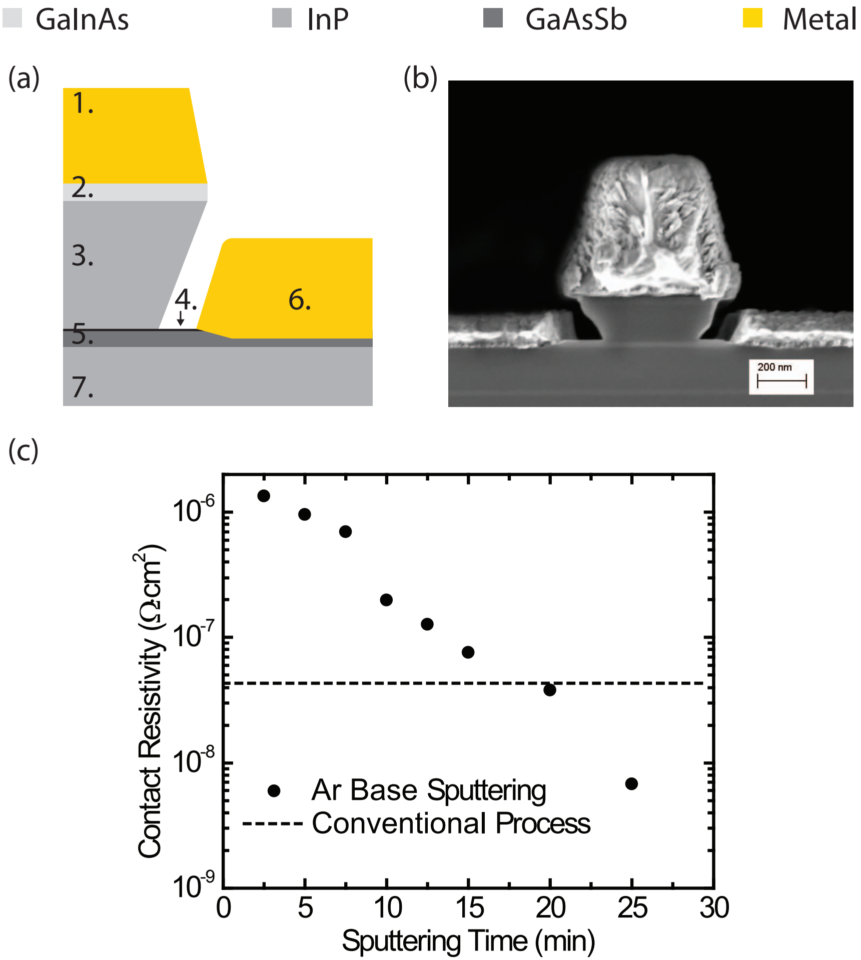


Figure 3.4 a) Simplified schematic of the base-emitter mesa cross-section. b) SEM image of the base-emitter mesa cross-section. c) Base contact resistivity *vs.* Ar sputtering time determined from the pinched TLM test structures measurements. The dashed line indicates the contact resistivity resulting from the conventional base contact formation process. Legend: 1. Emitter Contact Metal 2. Emitter Contact Layer 3. Emitter Layer 4. Interface Layer 5. Base Contact Metal 6. Base Layer 7. Collector Layer

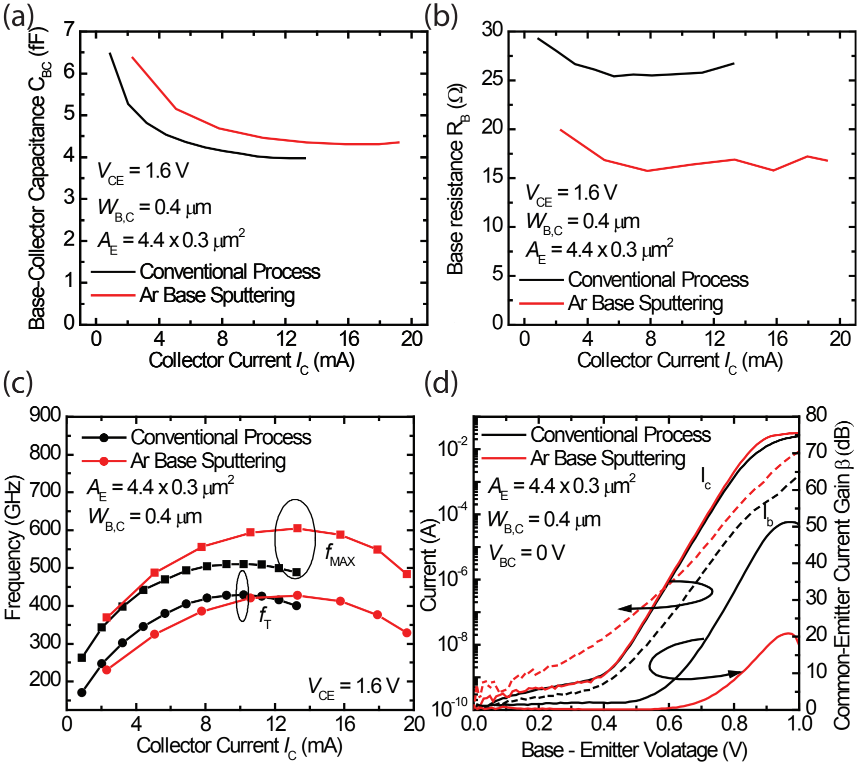


Figure 3.5 Comparison of the DC and RF performance of the devices fabricated using the conventional and Ar base sputtering method. The devices are the same size and fabricated using the same epitaxial layers described in Section 3.1. (a) Dependence of the C_{BC} on the collector current I_C (b) Dependence of the R_B on the collector current (c) Gummel characteristics (d) The dependance of f_T and f_{MAX} on the collector current I_C

mined by SEM to use their exact dimensions in the extrapolation. The pinched TLM measurements show an improved base contact resistivity with increased sputtering time, as shown in Fig. 3.4. (c). The contact resistivity reaches a value in the $10^{-9}\,\Omega \cdot cm^2$ range for a sufficiently long sputtering time, which is a clear improvement compared to the conventional fabrication process.

The transistors are fabricated in a process in which the GaAsSb base surface was *in-situ* sputtered with Ar ions prior to the deposition of the base metal stack. The values of C_{BC} in relation to the collector current are presented in Fig. 3.5. The magnitude of C_{BC} for the devices with $A_{\mathrm{E}} = 0.30 \times 4.4\ \mu\mathrm{m}^2$ and a base contact width of $W_{\mathrm{B,C}} = 0.4\ \mu\mathrm{m}$, the base-collector capacitance remains constant. Assuming that all other components of R_{B} remain unchanged, we calculate a fourfold reduction of the base contact resistance owing to the Ar sputtering, which is in general agreement with the TLM results shown in Fig. 3.4. (c). Compared to the device fabricated with the conventional process, we observe a reduction of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ time constant by a factor of two. The devices presented in this thesis devices show a 100 GHz higher f_{MAX} than devices fabricated with the conventional method on the same epitaxial layer structure, as shown in Fig. 3.5 (c). However, the comparison of the Gummel characteristics, shown in Fig. 3.6 (d), reveals a significant reduction of the emitter current gain β. It is due to the increased base surface recombination caused by the difference in the base contact geometry. Figure 3.6 shows Gummel characteristics for a record device fabricated with the base Ar sputtering method with a $0.3 \times 4.2\ \mu\mathrm{m}^2$ emitter area. The base and collector current ideality factors are $n_{\mathrm{B}} = 1.53$ and $n_{\mathrm{C}} = 1.04$, respectively. The peak common-emitter current gain is $\beta = 11$ with $V_{\mathrm{BC}} = 0\,\mathrm{V}$. The common-emitter current-voltage characteristics are shown in Fig. 3.6. (b). The common-emitter breakdown voltage BV_{CEO} is more than $5\,\mathrm{V}$ at a collector current density $J_{\mathrm{C}} = 1\,\mathrm{kA/cm^2}$. Figure 3.6 (a) shows an SEM image of the focused ion beam cross-section of a finalized DHBT. The Teflon film rapidly degrades under electron and ion beam irradiation and is therefore only partially visible and indicated by the arrow in Fig. 3.6 (a).

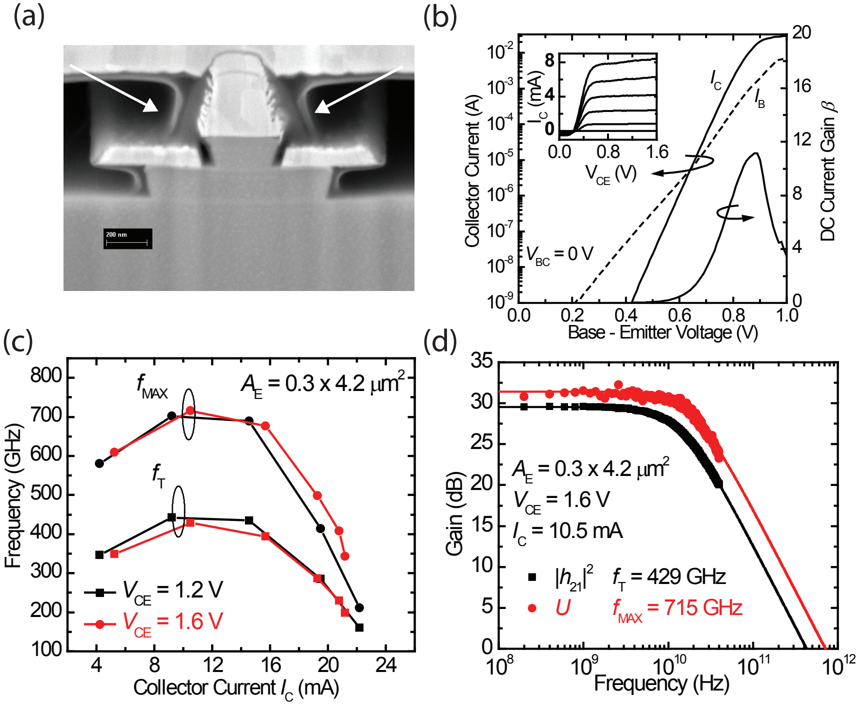


Figure 3.6 (a) SEM image of FIB cross section of a representative DHBT (b) Gummel characteristics Inset: I-V Characteristics (c) Dependence of f_{MAX} and f_T on the collector current I_C (d) Extrapolation of f_{MAX} and f_T by single-pole transfer function fits

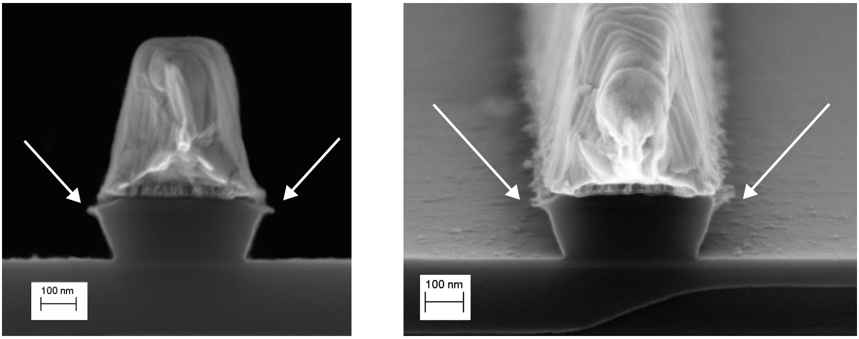


Figure 3.7 The SEM image of the cross-section of the emitter mesa etched in a two-step dry/wet technique. The arrows indicate the emitter *skirt*

3.5 Base Access Distance

The reduction of the base access distance is also essential for minimizing the negative effect of $(R_\mathrm{B}C_\mathrm{BC})_\mathrm{EFF}$ on the f_MAX. Firstly, the base access distance contributes to the extrinsic base resistance. Secondly, the reduction of the base access distance decreases the area of the extrinsic base-collector junction, and thus, also the capacitance [15]. Hence, the fabrication process of the emitter and the base need careful consideration in order to improve the maximum oscillation frequency.

3.5.1 Emitter Skirt

Once the emitter mesa is etched, the base metal is deposited in a self-aligned manner, as described in Section 3.3. Thus, the base access distance is determined by the emitter mesa undercut and the outer edge of the emitter. The SEM image of the cross-section of the resulting emitter mesa is shown in Fig. 3.7. The emitter mesa is etched in a two-step dry/wet process. Even though the emitter GaInAs contact layer is etched vertically using the ICP-RIE system, the edge of the GaInAs is not smooth as it is indicated by the arrows in Fig. 3.7. A possible reason is that the lift-off metal edge features of the emitter electrode are transferred into the GaInAs. The resulting edge or the emitter *skirt* acts as a mask during the base metal evaporation. Thus, the width of the skirt increases the base access distance. Moreover, the rough edge of the skirt leads to a variation

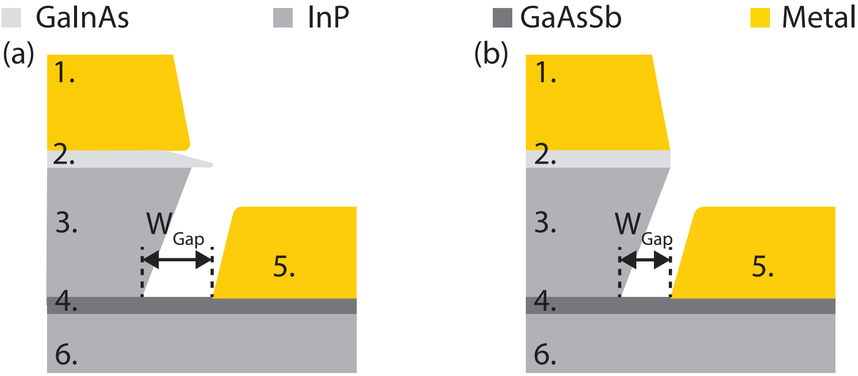


Figure 3.8 Schematic of the emitter mesa cross-section a) Conventional fabrication process b) Emitter sputtering method Legend: 1. Emitter Contact Metal 2. Emitter Contact Layer 3. Emitter Layer 4. Base Contact Metal 5. Base Layer 6. Collector Layer

in the access distance width which degrades the device reproducibility.

3.5.2 Emitter Sputtering

As previously discussed, the emitter-base junction width and the emitter undercut are determined by the width of the etch mask, which, in this case, is the width of the GaInAs emitter contact layer. Since the ICP-RIE etching process does not result in straight and smooth GaInAs side-walls, an alternative etching approach needs to be developed. One possible solution is to use physical etching, i.e. Ar sputtering. Sputtering offers two important advantages compared to dry chemical etching: The difference in the etch rates for the various materials is small and the method entails directional anisotropy. The process anisotropy is present because the volatility of the etch products for the inert Ar sputtering is not as critical as for the dry chemical etching; only the billiard-ball effect plays a role in physical etching. The nonselectivity of the process is attributed to the energy of the ions that are bombarding the surface: It is larger in comparison to the differences in the chemical bond energy and the chemical reactivity. Figure 3.8 illustrates the schematic comparison of the emitter-base mesa fabricated using the conventional (a) and the emitter sputtering (b) method. The highly directional Ar sputtering used during the GaInAs emitter contact layer etching step results in a minimized emitter mesa undercut and

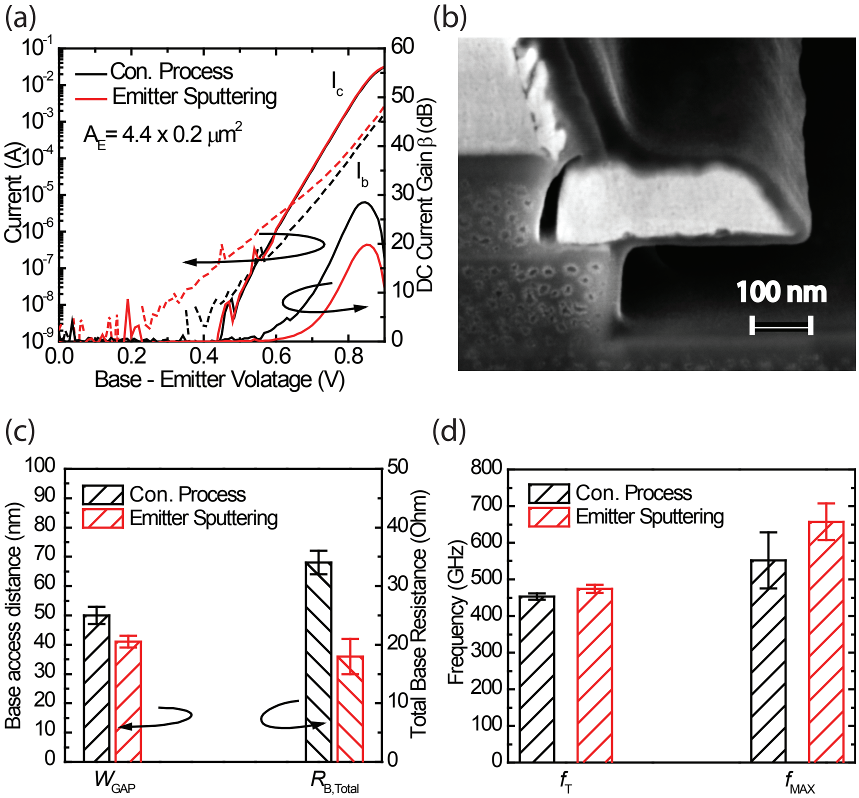


Figure 3.9 Comparison of the DC and RF performance of the devices fabricated using the conventional (black line) and the emitter sputtering (red line) method. (a) Gummel characteristics (b) SEM image of the cross-section of the device fabricated using the emitter sputtering method. (c) Comparison of the base access distances and the resulting base resistance R_B (d) Comparison of the f_T and f_{MAX} for the corresponding devices

reduces the base access distance W_{GAP}. Ar sputtering also eliminates the skirt (lift-off metal edge features), leaving an emitter contact electrode with steeper sidewalls and smoother edges.

A comparison of the devices with the conventional and the optimized emitter etching technique is presented in Fig. 3.9. The devices have an $A_{\mathrm{E}} = 0.20 \times 4.4\ \mu\mathrm{m}^2$ and are fabricated using the epitaxial layers described in Section 3.1. The Gummel characteristics of the devices are shown in Fig. 3.9. (a). While the collector I_{C} current is equal in both DHBTs, the base current I_{B} is higher and emitter current gain β is slightly reduced for the device fabricated using emitter sputtering. This indicates an increased base surface recombination, and thus, an increased parasitic recombination current, which results in a higher I_{B}. By using Ar sputtering during the GaInAs emitter contact layer etching step, the width of the emitter shadowing mask is reduced and a uniform base access distance along the emitter finger length is created, as confirmed by the SEM image (Fig. 3.9. (b)). The base access distance W_{GAP} was reduced from $50 \pm 3\,\mathrm{nm}$ to $41 \pm 2\,\mathrm{nm}$, which leads to a clear improvement of the base resistance, as demonstrated in Fig. 3.9. (c). The mean and standard deviation of the cutoff frequencies f_{T} and f_{MAX} of a conventional (black) and optimized (red) emitter etching technique are shown in Fig. 3.9. (d). The f_{T} values are comparable in both DHBTs. Small differences in the values are related to process variations (emitter end undercut, contact resistivity). The optimized emitter etching method results in a more than 100 GHz higher f_{MAX}, due to a lower base resistance.

Figure 3.10 shows the DC and RF characteristics of the record device fabricated with the emitter Ar sputtering method. Figure 3.10 (a) illustrates the Gummel characteristics of a device with a $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area and a $0.40 \times 5.5\ \mu\mathrm{m}^2$ collector area. The base and collector ideality factors are $n_{\mathrm{B}} = 1.44$ and $n_{\mathrm{C}} = 1.02$. The peak common-emitter current gain β is 24 with $V_{\mathrm{BC}} = 0\,\mathrm{V}$. The common-emitter current-voltage characteristics demonstrate a low offset voltage of $\approx 50\,\mathrm{mV}$ and are shown in Fig. 3.10 (b). The common-emitter breakdown voltage is $BV_{\mathrm{CEO}} \approx 5\,\mathrm{V}$ at a collector current density of $J_{\mathrm{C}} = 1\,\mathrm{kA/cm}^2$. The dependence of f_{T} and f_{MAX} on the collector current for $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$ and $V_{\mathrm{CE}} = 1.2\,\mathrm{V}$ is shown in Fig. 3.10. (c). The performance is slightly reduced due to self-heating effects at $V_{\mathrm{CE}} = 1.2\,\mathrm{V}$. The Current and Maison‘s unilateral gains

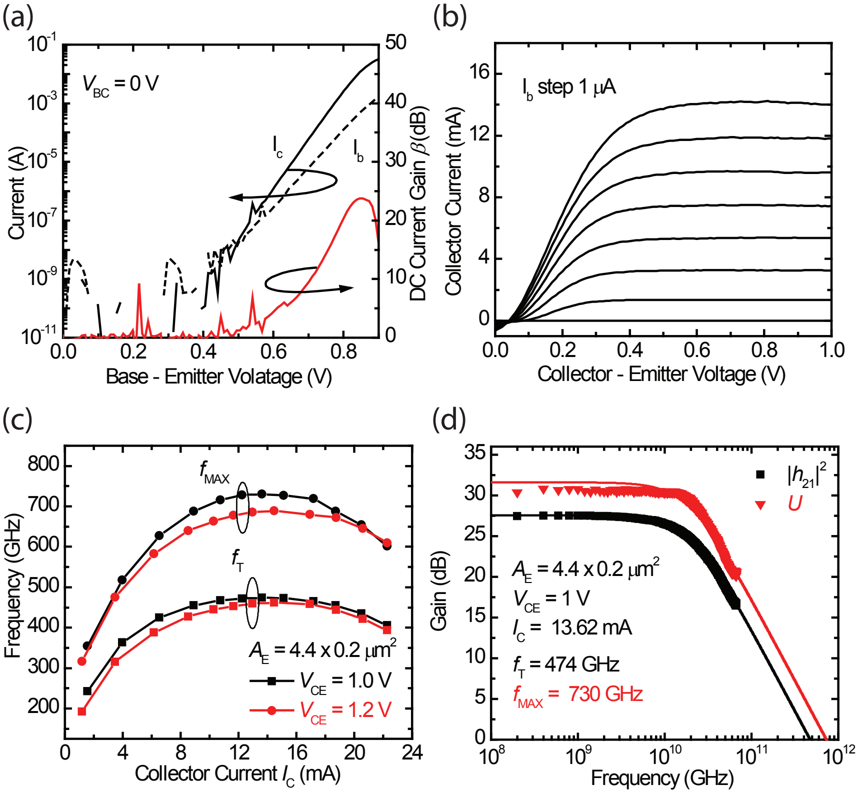


Figure 3.10 (a) Gummel characteristics (b) I-V Characteristics (c) Dependence of f_{MAX} and f_{T} on the collector current I_{C} (d) Extrapolation of f_{MAX} and f_{T} by single-pole transfer function fits

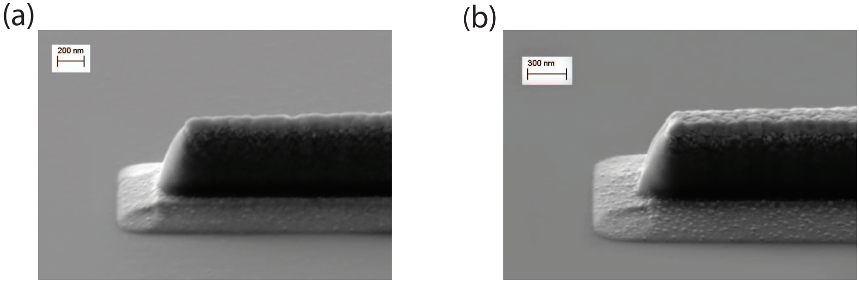


Figure 3.11 SEM image of the device base-emitter mesa after the tilted base metal evaporation (a) Tilt 10° (b) Tilt 15°

are plotted against the frequency in Fig. 3.10. (d). Extrapolations based on single-pole fits yield an $f_{\mathrm{MAX}} = 730\,\mathrm{GHz}$ with a simultaneous $f_{\mathrm{T}} = 474\,\mathrm{GHz}$ at $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$. The improved high frequency performance was achieved through a reduction of the base access distance using a combination of Ar sputtering and wet etching in the self-aligned emitter formation process.

3.5.3 Emitter Sputtering and Base Tilting

The reduction of the base access distance results in a decrease of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ time constant and thus an improved f_{MAX}. Further improvement of the maximum oscillation frequency requires an optimization of the self-aligned base contact formation process to achieve a shorter base access distance. For this purpose, the samples were tilted during the base electrode evaporation. Figure 3.11 shows the SEM images of the devices that are tilted by 10° (Fig. 3.11 (a)) and by 15° (Fig. 3.11 (b)) during the base electrode deposition. The tilting during the base evaporation reduces the geometrical limitation set by the self-aligned process: In this case, the outer edge of the emitter does not determine the position of the base electrode. The resulting base access distance is shorter than the distance between the emitter mesa undercut and the outer edge of the emitter.

Figure 3.12 shows the SEM image of the FIB cross-section of the base access distance for the test samples and of the finalized devices tilted by 10° and by 15°. The devices display an unusual shape of the base electrode:

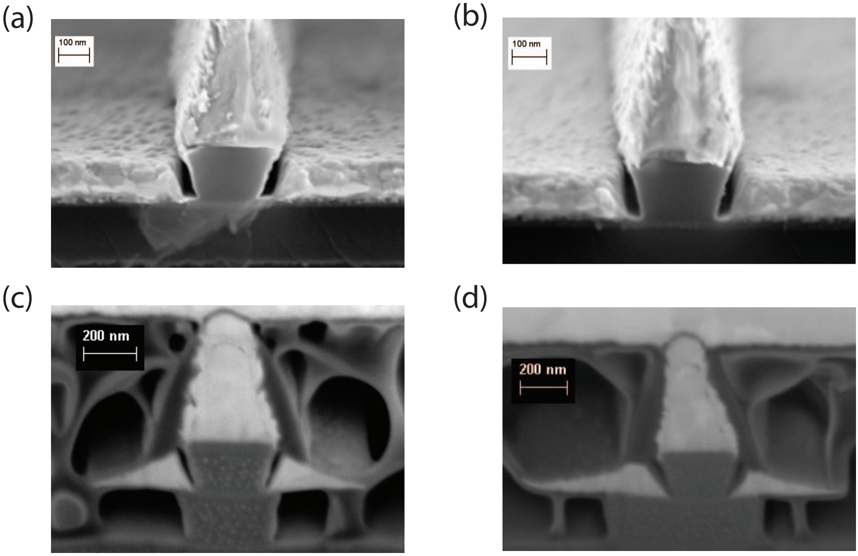

(a)
100 nm
(b)
100 nm
(c)
200 nm
(d)
200 nm

Figure 3.12 SEM image of the FIB cross-section: (a) of the base access distance for the test sample with 10° tilt (b) of the base access distance for the test sample with 15° tilt (c) of the base access distance for the finalized device with 10° tilt (d) of the base access distance for the finalized device with 15° tilt

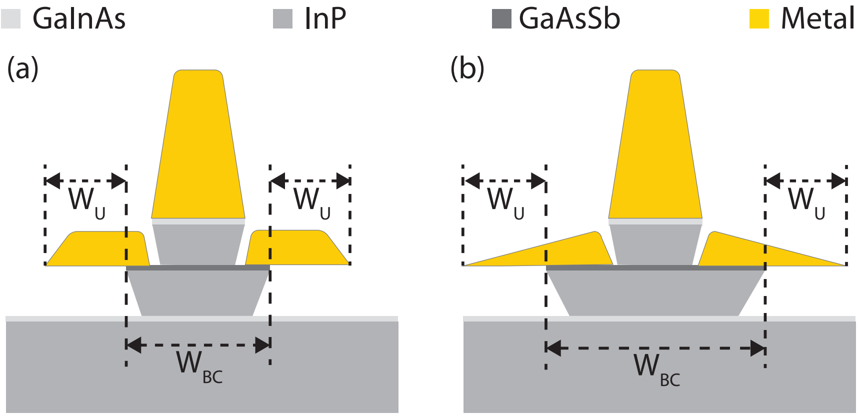

GaInAs
InP
GaAsSb
Metal
(a)
W_U
W_U
W_{BC}
(b)
W_U
W_U
W_{BC}

Figure 3.13 Schematic of the device cross-section (a) Conventional process (b) Devices fabricated by tilting during the base electrode deposition

It has a triangular cross-section and the width of the base electrodes is larger than the width of the base electrodes fabricated without tilting, as shown in Fig. 3.13. The reason for this is the edge of the PMMA resist window opening no longer determines the base electrode dimension. The resulting difference in the base contact width for the base electrodes fabricated without and with a 10° tilt during the evaporation is $\approx 100\,\mathrm{nm}$. Therefore, to avoid additional parasitic base-collector capacitance, the underetching time of the base-collector mesa was readjusted. Furthermore, the base-collector mesa width was reduced due to a shorter base-access distance, leading to a reduced base-collector capacitance.

The devices have an emitter area of $A_\mathrm{E} = 0.35 \times 4.4\ \mu\mathrm{m}^2$ and are fabricated using the epitaxial layers described in Section 3.1. In order to investigate the influence of the base-emitter mesa fabrication process on the device performance, the devices are made using five different methods: They are the conventional fabrication process (described in Section 3.2), the emitter Ar sputtering method (described in Section 3.5.2), the novel method of tilting during the base electrode evaporation by 10°, and finally, the emitter Ar sputtering method combined with tilting during the base electrode evaporation by 10° and 15°. The mean and the standard deviation of the base access distance W_GAP depending on the base-emitter mesa fabrication process are depicted in Fig. 3.14 (a). The base access distance is significantly reduced by using the emitter Ar sputtering method, as shown in Fig. 3.14 (a). Additionally, Ar sputtering results in the smoother edges of the emitter electrode. This leads to a smaller standard deviation and thus to a more reproducible base access distance along the emitter electrode. Tilting the samples by 10° during the base electrode evaporation reduces the base access distance even more. The resulting W_GAP is reduced from $41 \pm 2\,\mathrm{nm}$ to $18 \pm 4\,\mathrm{nm}$. However, the standard deviation of the base access distance increases with increasing the tilt. This is attributed to the asymmetry caused by the limited mechanical precision of the electron beam evaporation system: It leads to a base access distance that is in a range of 8 to $0\,\mathrm{nm}$ for the devices tilted by 15° during the base electrode evaporation. Devices fabricated using 15° tilting during the base electrode evaporation feature a base-emitter short-circuit and are thus not considered in the following performance analysis. The mean and standard deviations of the the common-emitter current gain β of the devices are

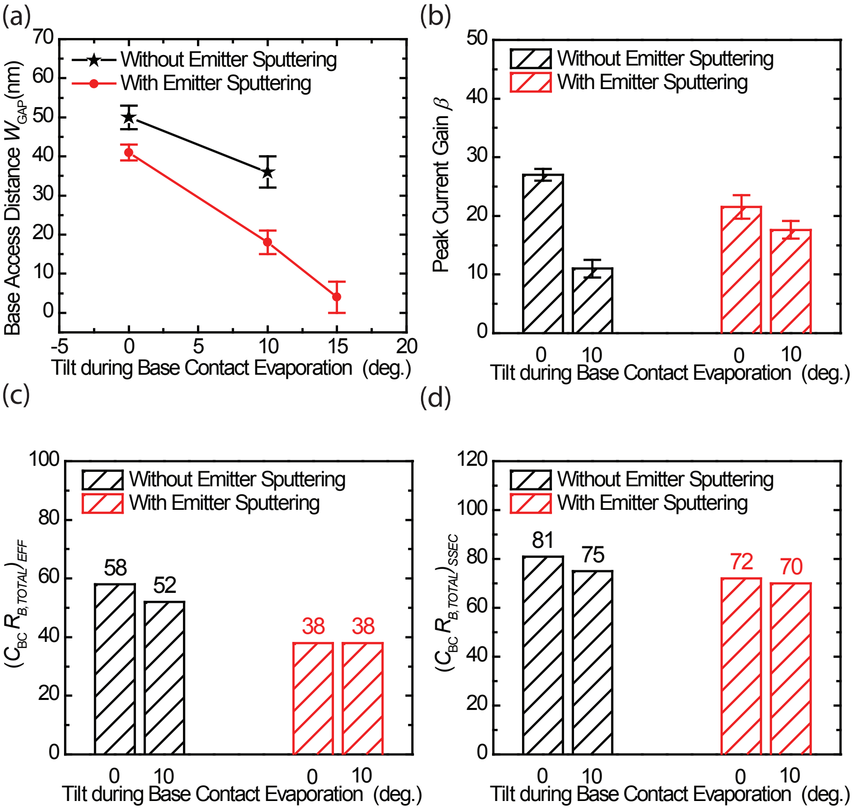


Figure 3.14 Comparison of the device parameters fabricated using five base-emitter mesa fabrication methods: The conventional fabrication process, the emitter sputtering method, tilting during the base electrode evaporation by 10° and the combination of the emitter Ar sputtering with the tilting during the base electrode evaporation by 10° and 15° (a) Comparison of the base access distances (b) Comparison of the emitter common gain of the devices (c) Comparison of the $(R_B C_{BC})_{EFF}$ time constant (d) Comparison of the $(R_B C_{BC})_{SSEC}$ time constant

shown in Fig. 3.14. (b). Tilting during the base electrode evaporation seems to have a negative effect on the emitter current gain, which is attributed to an increased base surface recombination. However, by using the emitter Ar sputtering technique, this negative effect is diminished due to the more uniform access distance along the emitter electrode. Figures 3.14 (c) and 3.14 (d) demonstrate the comparison of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ and $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{SSEC}}$ time constants of the fabricated devices. The values of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ are calculated from the extrapolated values of f_{T} and f_{MAX} by single-pole transfer function fits using the Eqns. 2.6 and 2.8. The values of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{SSEC}}$ are the fits of the small-signal equivalent circuit elements to the measured S-parameters of the corresponding devices. The values of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{SSEC}}$ are slightly higher than the values of the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$. This is attributed to difficulties in separating the intrinsic and the extrinsic SSEC elements during the extraction. Hence, only trends can be compared. Figure (c) and 3.14 (d) show two similar trends for the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ and $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{SSEC}}$ time constants: Firstly, the tilting during the base electrode evaporation slightly reduces the RC time constant. Secondly, the emitter Ar sputtering results in a drastic reduction of the parasitic delay time by more than 20%. The mean and standard deviations of the f_{T} and f_{MAX} of the fabricated devices are shown in Fig. 3.15 (a) and (b), respectively. The transistors fabricated with emitter Ar sputtering exhibit a slight improvement in the f_{T} from 415 to 428 GHz due to the improved emitter sidewall profile. As a result of the reduced $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ and of the higher f_{T}, f_{MAX} is also increased in the DHBTs fabricated with the emitter Ar sputtering method. For the devices with an emitter area of $A_{\mathrm{E}} = 0.35 \times 4.4\ \mu\mathrm{m}^2$, the average f_{MAX} was improved from 534 to 712 GHz due to a reduced base access distance. The combination of a lower base access resistance and a lower base-collector capacitance leads to a significant increases in both f_{T} and f_{MAX}.

Figure 3.16 shows the DC and RF characteristics of the record device fabricated with the combination of emitter Ar sputtering and tilting of the samples by 10° during the base evaporation. Figure 3.16 (a) illustrates the Gummel characteristics of a device with a $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area and a $0.40 \times 5.5\ \mu\mathrm{m}^2$ collector area. The base and collector ideality factors are $n_{\mathrm{B}} = 1.43$ and $n_{\mathrm{C}} = 1.02$. The peak common-emitter current gain β is 17 with $V_{\mathrm{BC}} = 0$ V. The common-emitter current-voltage characteristics

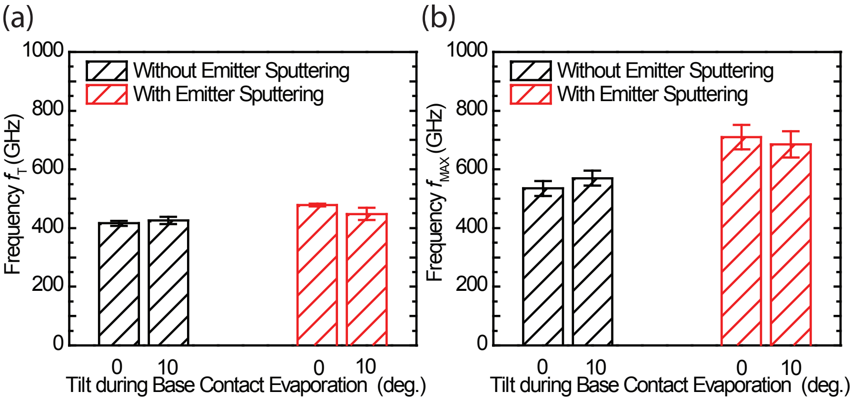


Figure 3.15 Comparison of the RF device parameters fabricated using four base-emitter mesa fabrication methods: The conventional fabrication process, the emitter sputtering method, tilting during the base electrode evaporation by 10° and the combination of the emitter Ar sputtering with tilting during the base electrode evaporation by 10° (a) Comparison of the f_T (b) Comparison of the f_{MAX}

demonstrate a low offset voltage of $\approx 50\,\mathrm{mV}$ and are shown in Fig. 3.16 (b). The common-emitter breakdown voltage is $BV_{\mathrm{CEO}} \approx 5\,\mathrm{V}$ at a collector current density of $J_{\mathrm{C}} = 1\,\mathrm{kA/cm^2}$. The dependence of f_{T} and f_{MAX} on the collector current for $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$ and $1.2\,\mathrm{V}$ is shown in Fig. 3.16. (c). The performance is slightly reduced due to self-heating effects at $V_{\mathrm{CE}} = 1.2\,\mathrm{V}$. The f_{T} and f_{MAX} are plotted against the frequency in Fig. 3.16. (d). Extrapolations based on single-pole fits yield $f_{\mathrm{MAX}} = 779\,\mathrm{GHz}$ with a simultaneous $f_{\mathrm{T}} = 503\,\mathrm{GHz}$ at $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$. The f_{MAX} compared with respect to our previous results [48] is improved by the reduced base access resistance $R_{\mathrm{B,GAP}}$ and the base-collector capacitance C_{BC}.

3.5.4 Emitter Ion Milling

The optimized fabrication process of the emitter mesa etching enables a significant improvement in the maximum oscillation frequency. However, the Ar sputtering of the emitter skirt in the Plassys II electron beam evaporation system has limitations: This Ar sputtering tool is intended for the surface pre-treatment prior to the metal evaporation. Thus, it is not suitable for long etching cycles. The emitter sputtering by the Plassys

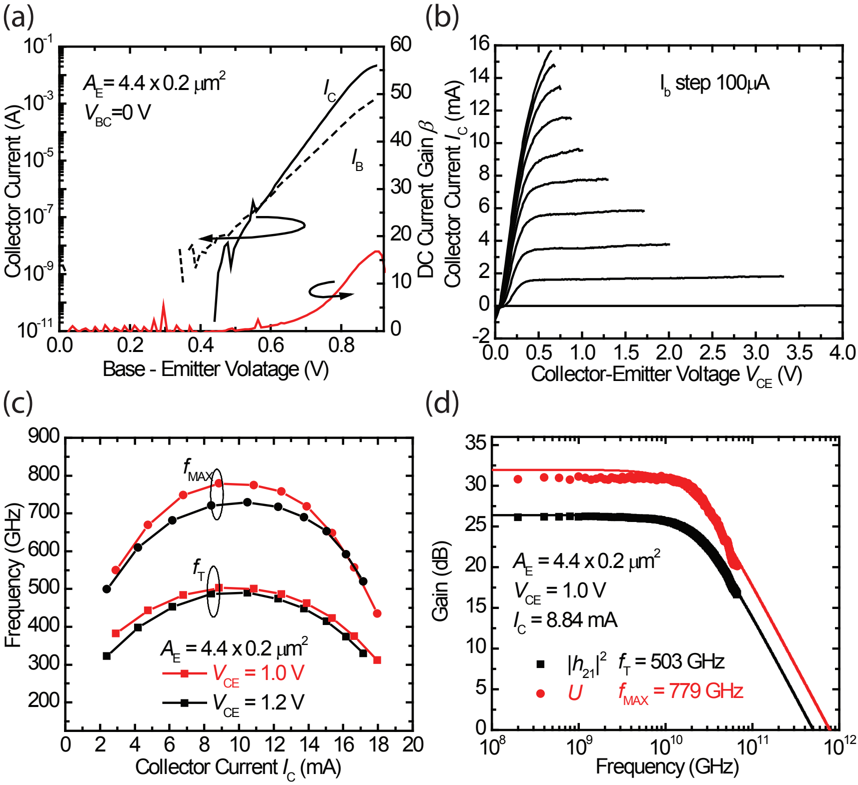


Figure 3.16 (a) Gummel characteristics (b) I-V Characteristics (c) Dependence of f_{MAX} and f_T on the collector current I_C (d) Extrapolation of f_{MAX} and f_T by single-pole transfer function fits

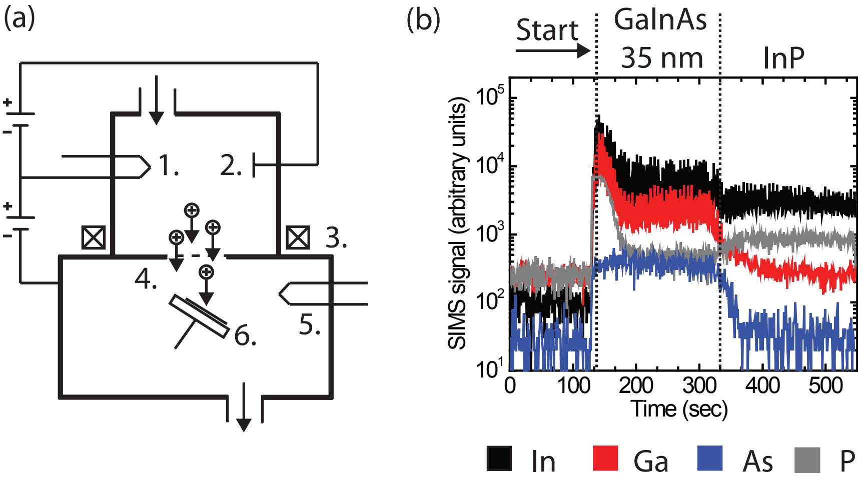


Figure 3.17 (a) Schematic of the ion milling system. Legend: 1. Cathode 2. Anode 3. Focusing Coil 4. Accelerating electrode 5. Hot filament neutralizer 6. Substrate holder (b) An example of the SIMS data coming from a sample as its ion milled. The epitaxial layers are (from top to bottom): GaInAs/InP. The goal was to stop the etch process after etching the GaInAs layer and over-etching into the InP layer

II system has an unstable rate and is not very reproducible. The etching rate decreases with an increased etching time because of the substrate charging effects: The sample is charged by Ar ions during sputtering and thus the etching rate varies. One possible way to attain a stable rate during emitter Ar sputtering is to use the ion milling system instead of the Plassys II system. The schematic of the ion milling system is given in Fig. 3.17 (a). The main advantage of the ion milling system is that the etched sample can be electrically neutralized by extracting low-energy electrons from a hot filament neutralizer, as shown in Fig. 3.17. Moreover, the ion milling system is equipped with a SIMS (Secondary Ion Mass Spectrometer) probe for the precise control of the thickness and the composition of the etched materials. Figure 3.17 (b) shows SIMS measurements during GaInAs/InP emitter sputtering. As shown, the etching process of the GaInAs layer can be monitored by counting the corresponding secondary ejected ions of each element. Consequently, the etch can be reliably stopped when the end point is detected.

The effect of the ion milling etching time on the etching behavior of

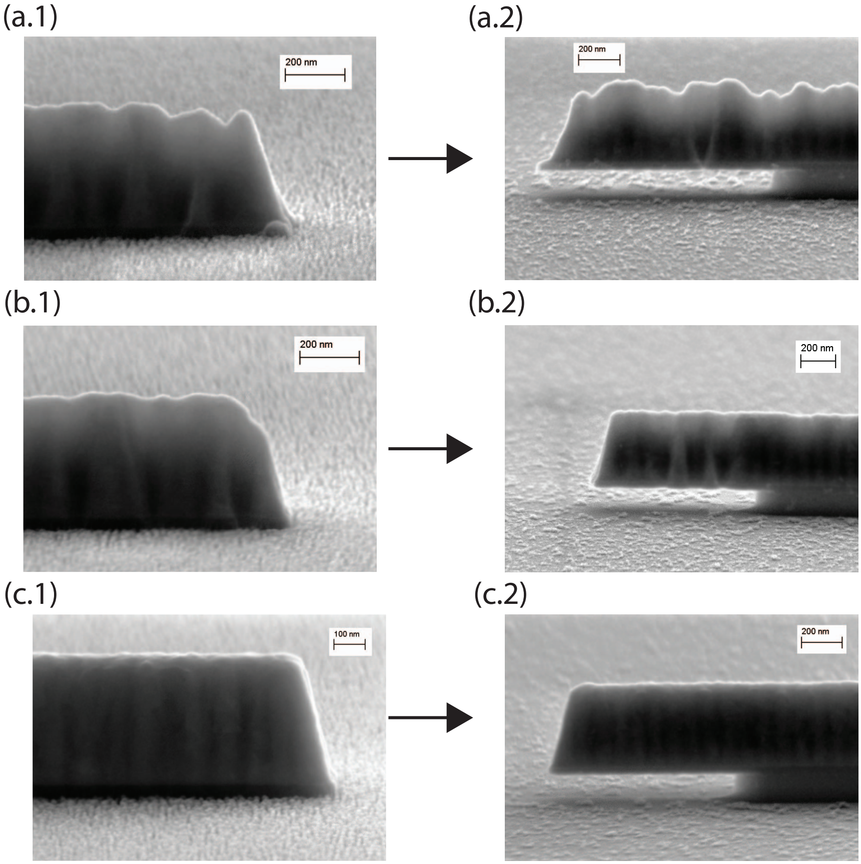

(a.1)
200 nm
(a.2)
200 nm
(b.1)
200 nm
(b.2)
200 nm
(c.1)
100 nm
(c.2)
200 nm

Figure 3.18 SEM images of the resulting emitter mesa after ion milling of 50 (a.1), 60 (b.1) and 70 (c.1) nm of the GaInAs/InP emitter thickness. The ion milling is followed by isotropic wet etching of the remaining InP using an HCl/H_3PO_4 solution (Fig. (a.2), (b.2) and (c.2))

the sub-micron GaInAs/InP emitter mesas was investigated in order to develop a well-controlled process for the DHBTs fabrication. A constant accelerating voltage of 250 V and an anode current of 250 mA were used in all presented experiments. The etched depth was controlled by the SIMS measurements and confirmed by SEM inspection of the samples. The emitter metal stripes featuring a width of ≈ 300 nm are defined by EBL and fabricated on the epitaxial layers described in Section 3.1. The emitter metal stack of the test structures consists of Ti (5 nm), Pt (30 nm) and Au (400 nm). Figure 3.18 demonstrates the SEM images of the resulting emitter mesa after ion milling 50 (a.1), 60 (b.1) and 70 (c.1) nm of the GaInAs/InP emitter thickness. The ion milling is followed by isotropic wet etching of the remaining InP using an HCl/H_3PO_4 solution (Fig. 3.18 (a.2), (b.2) and (c.2)). It can be observed that the surface roughness decreases with an increasing etching time. However, the base surface remains rough for all samples after the etching using a HCl/H_3PO_4 solution.

To investigate the origin of the surface roughness, samples without emitter metal stripes were ion milled. The ion milled samples were cleaved and examined in the SEM, as shown in Fig. 3.19 (a)-(d). For the samples depicted in Fig. 3.19 (b)-(d), the etching conditions were the same as for the ion milled samples with emitter stripes 50 (b), 60 (c) and 70 (d) nm of the etching depth, respectively. The sample shown in Fig. 3.19 (a) was etched with a reduced accelerating voltage of 150 V in order to exclude the dependency of the surface roughness on the ion energy. As shown in Fig. 3.19 (a)-(d), ion milling the emitter results in a surface covered by vertical *pillars* that are 30, 37, 48 and 50 nm high. Most probably, the pillars originate from the physical nature of the ion milling process. A schematic representation of the pillar profile formation process is depicted in Fig. 3.19 (e.1)-(e.3): The pillars are formed after the ion milling (Fig. 3.19 (e.2)) and consist of the InP layer with GaInAs caps. After the remaining InP is etched using a HCl/H_3PO_4 solution, the GaInAs residuals (the caps of the pillars) are deposited on the surface of the sample (Fig. 3.19 (e.2)). The GaAsSb base surface should be pristine prior to the base metal evaporation in order to fabricate low resistance base ohmic contacts. Therefore, the emitters, after ion milling, were etched in a H_3PO_4/H_2O_2/DI solution, as shown in Fig. 3.20 (a)-(b). The samples in Fig. 3.20 (a) and (b) are etched using ion milling for an etch depth of 50 and 70 nm, respectively.

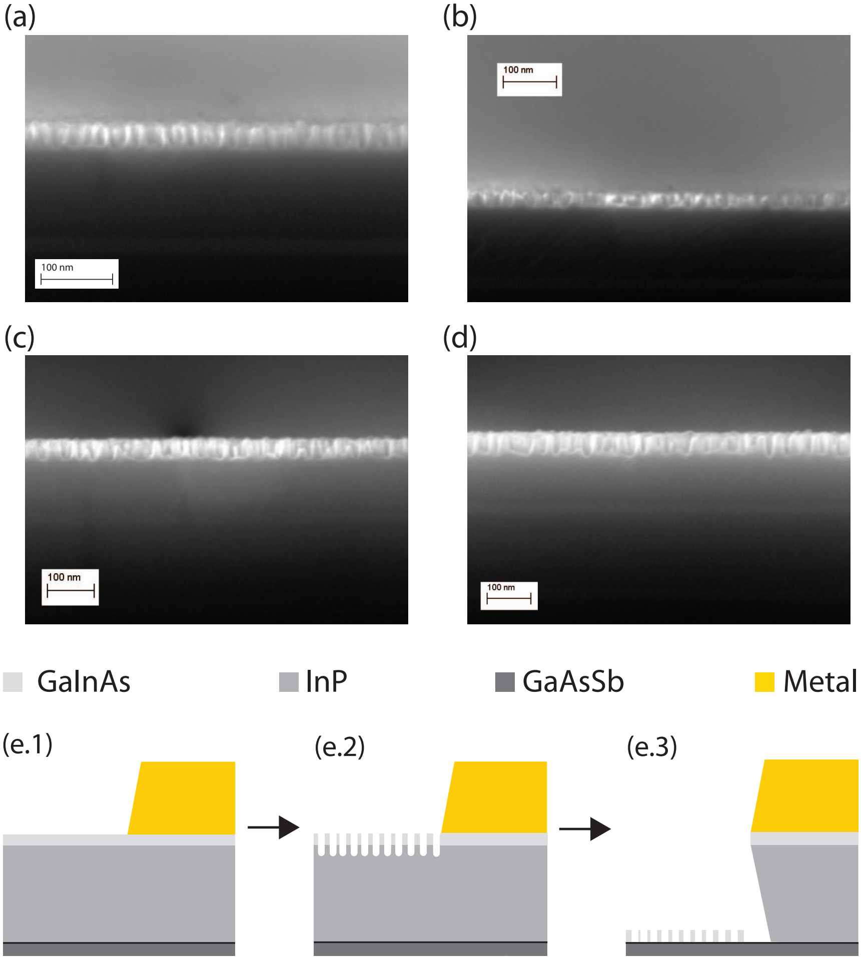


Figure 3.19 SEM images of the cross-section of the ion milled samples (a) accelerating voltage 150 V, etching thickness 60 nm (b) accelerating voltage 250 V, etching thickness 50 nm (c) accelerating voltage 250 V, etching thickness 60 nm (d) accelerating voltage 250 V, etching thickness 70 nm (e.1)-(e.3) A schematic of the pillar profile formation process is depicted: The pillars are formed after the ion milling (e.2) and they consist of the InP layer with the GaInAs caps. After the remaining InP is etched using an HCl/H_3PO_4 solution, the GaInAs residuals (the caps of the pillars) are left or transferred on the surface of the sample (Fig. 3.19 (e.3))

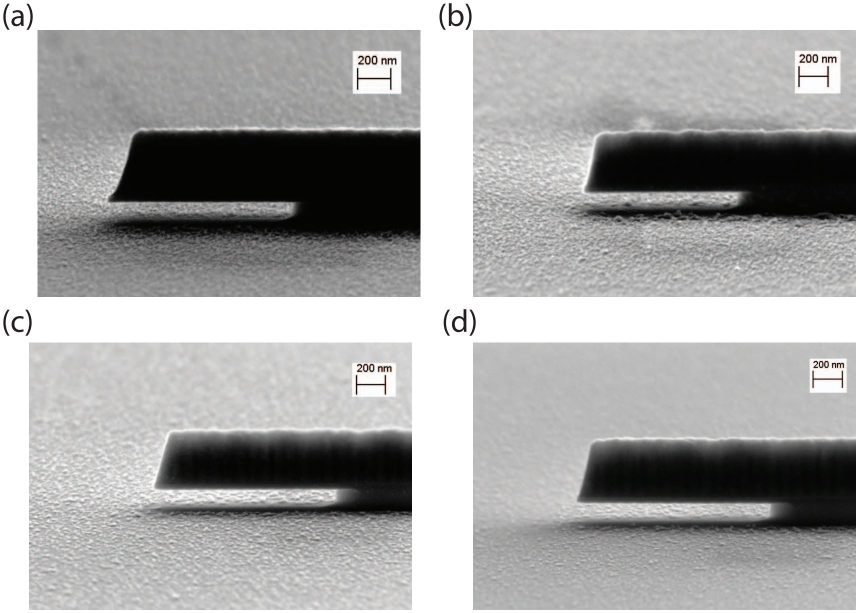


Figure 3.20 (a)-(b) SEM images of the emitter mesa etched with a combination of ion milling, wet etching using an H_3PO_4/H_2O_2/DI solution and wet etching using an HCl/H_3PO_4 solution ((a) Ion milling depth 50 nm (b) Ion milling depth 70 nm) (c)-(d) SEM images of the emitter mesa etched with combination of ion milling, ICP etching using O_2 plasma and wet etching using an HCl/H_3PO_4 solution ((c) Ion milling depth 50 nm (d) Ion milling depth 70 nm)

The resulting base surface roughness is higher than before using the additional GaInAs wet etching step. This effect is probably related to the high volatility of the GaInAs wet etching solution. Another attempt to etch away the GaInAs residuals from the base surface was made by using ICP dry etching by O_2 plasma. The resulting base surface morphology after the combined etching process of ion milling, ICP O_2 plasma etching and wet etching using an HCl/H_3PO_4 solution is shown in Fig. 3.20 (c)-(d). The roughness of the base surface was indeed reduced. However, the surface still retained a certain roughness associated with GaInAs residuals. This suggests, however, that ICP O_2 plasma etching is not aggressive enough to remove the GaInAs residuals completely. Therefore, after ion milling, the emitters are etched using ICP with a $CH_4/Ar/Cl_2/H_2$ gas mixture. Figure 3.21 (a)-(b) demonstrates the resulting emitter mesa. Ion milling

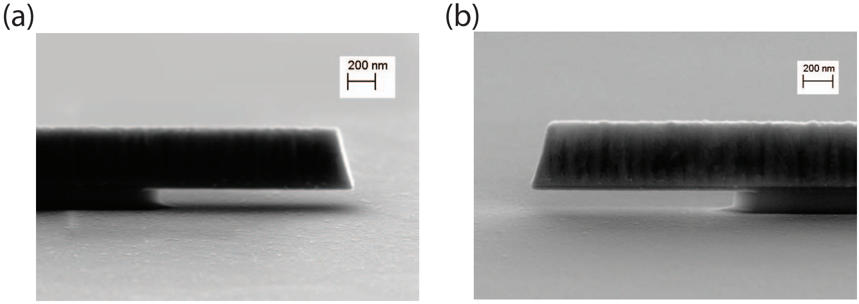


Figure 3.21 SEM images of the emitter mesa etched in combination of the ion milling, the ICP etching using $CH_4/Ar/Cl_2/H_2$ gas mixture and the wet etching using HCl/H_3PO_4 solution (a) Ion milling depth 70 nm (b) Ion milling depth 50 nm

for 50 nm, followed by ICP etching with a $CH_4/Ar/Cl_2/H_2$ gas mixture and wet etching using a HCl/H_3PO_4 solution gives a pristinely clean and smooth base surface, as shown in Fig. 3.21 (b).

Figure 3.22 shows the SEM image and the RF characteristics of a device fabricated with the emitter ion milling method. The devices use a 125-nm-thick InP:Si collector doped at 1.5×10^{17} cm ^{3}, which is higher than the the epitaxial transistor layers described in Section 3.1. The other layers are unchanged. The device with a 0.25×4.4 µm^2 emitter area and a 0.40×5.5 µm^2 collector area features a base access distance of $W_{\mathrm{GAP}} \approx 40\,\mathrm{nm}$, as shown in Fig. 3.22 (a). The obtained excess distance is uniform along the emitter finger. Also, the emitter mesa has smooth edges. Figure 3.22 (b) illustrates the dependence of f_{T} and f_{MAX} on the collector current for $V_{\mathrm{CE}} = 1.0$ and 1.2 V. The f_{T} and f_{MAX} are plotted against frequency in Fig. 3.22. (c). Extrapolations based on single-pole fits yield an $f_{\mathrm{MAX}} = 696\,\mathrm{GHz}$ with a simultaneous $f_{\mathrm{T}} = 476\,\mathrm{GHz}$ at $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$. The achieved base access distance and the resulting high frequency performance is comparable to the results achieved using the emitter Ar sputtering method. The developed method is a highly reproducible and stable process. Therefore, the fabricated devices demonstrate higher yield and greater manufacturability.

Ion milling is a physical etching process. Therefore, there is a danger to damage the semiconductor surface by bombarding it with Ar atoms. Efforts to characterize this effect and to further optimize the emitter mesa

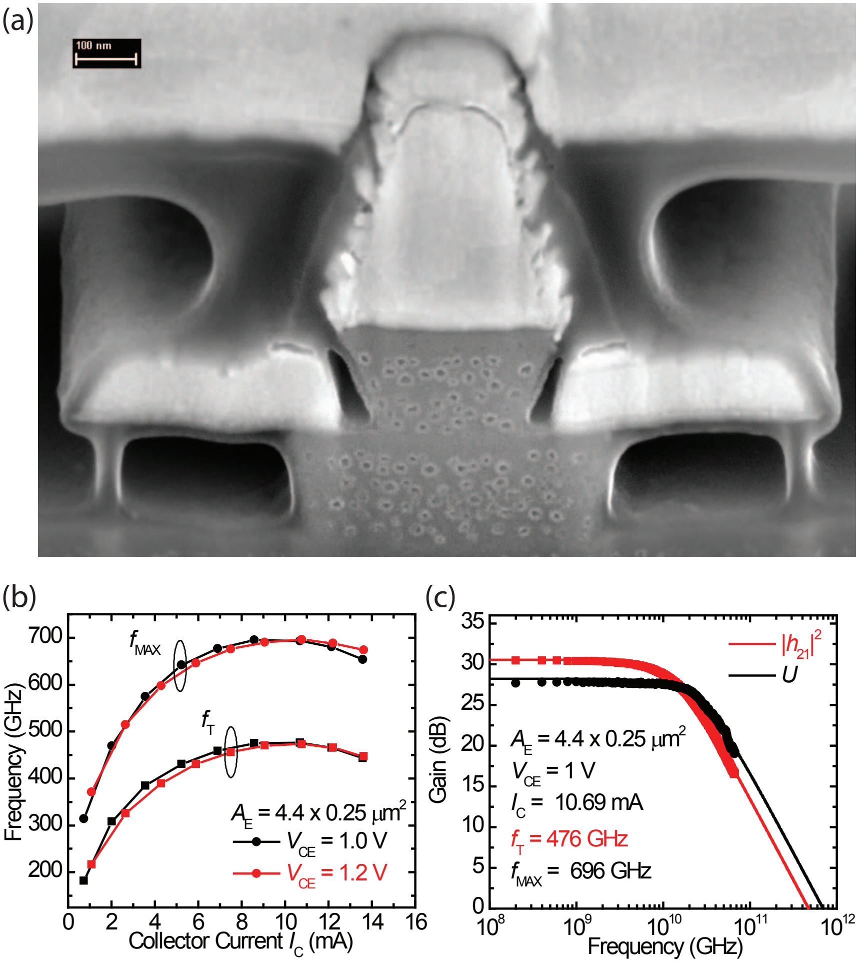


Figure 3.22 (a) SEM image of the FIB cross-section of the device fabricated using ion milling (b) Dependence of f_{MAX} and f_T on the collector current I_C (c) Extrapolation of f_{MAX} and f_T by single-pole transfer function fits

etching process have been made and are ongoing.

3.6 Emitter End Undercut Control

The RF bandwidth of the transistors decreases when the ratio of the collector to the emitter area $A_{\mathrm{C}}/A_{\mathrm{E}}$ grows. There are two reasons for this effect: Firstly, the f_{T} decreased because of the increasing emitter-collector transit delay τ_{EC}. Secondly, the f_{MAX} decreased due to a lower f_{T} and an increasing C_{BC}. One of the reasons for the growing ratio is the reduced emitter length L_{E}: The wet etching solutions during the emitter-base mesa fabrication process greatly underetch the emitter ends. The reason is the crystallografic nature of the InP wet etching: The emitter electrode is parallel to the [011] crystal plane so that after the emitter mesa is wet etched using an HCl/H_3PO_4 solution the emitter width W_{E} is $\approx 100\,\mathrm{nm}$ narrower than the emitter metal contact width. On the other hand, the longitudinal emitter ends are etched along fast etch facets ([001] and [010] crystal directions), and thus the emitter is rapidly underetched from its ends. Figure 3.23 shows a SEM image of the FIB cross-section of the DHBT along the emitter where the emitter length is much shorter than the collector length. To keep the $A_{\mathrm{C}}/A_{\mathrm{E}}$ ratio small, the base-emitter and base-collector junctions ideally should be of equal length. Therefore, the emitter electrode geometry needs to be optimized in order to prevent aggressive emitter end undercutting.

In the conventional process there are two different emitter contact geometries: the rectangular and the *bone-shape* emitter electrodes. The bone-shape emitter contact has a wide stripe on each end of the emitter. In Figure 3.24 shown the bone-shape emitter contact ((a) and (b)) and the rectangular one (c). The yield of the bone-shape emitter devices is generally higher than the one of the devices fabricated with rectangular emitters. The reason is the anisotropic etching properties of the emitter semiconductor material: It takes more time to etch the wide bone-shape emitter end and thus emitter length is not shortened. Therefore, the optimum geometrical parameters for the bone-shape emitter electrode need to be determined in order to accommodate the emitter mesa wet etching and base surface treatment. The test emitter structures were defined by electron beam lithography and have bone angles of $\alpha_{\mathrm{E,B}} = 30^\circ$ and 45° and

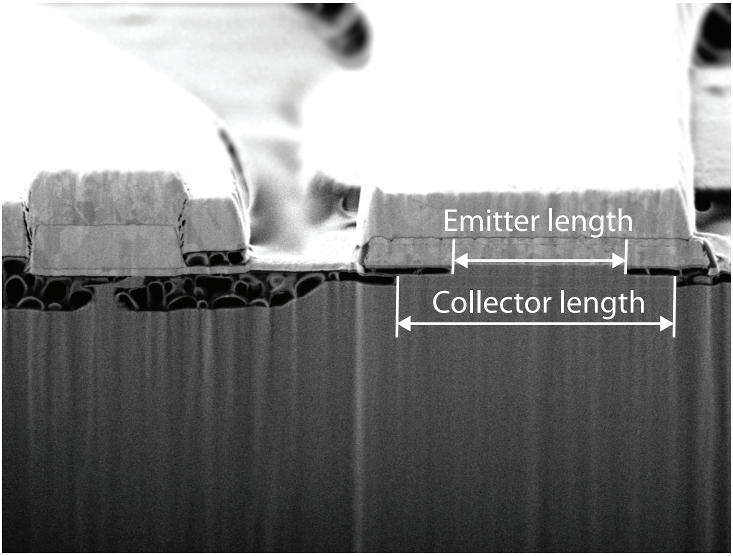


Figure 3.23 SEM image of the FIB cross-section of the DHBT along the emitter. The emitter length L_E is much shorter than collector length L_C

bone end width of $W_{\mathrm{E,B}} = 600$, 700, 800 and 900 nm. All samples were processed in one batch in order to minimize experimental variations. Figure 3.25 (a) shows the mean width of the emitter undercut $W_{\mathrm{E,U}}$ and a linear fit to the experimental data. If the emitter end undercut is insufficient, the InP protrudes from the emitter metal stripe, causing an emitter-base short circuit, as shown in Fig. 3.25. (b). When the emitter undercut is too large, the $A_{\mathrm{C}}/A_{\mathrm{E}}$ ratio grows, as shown in Fig. 3.25. (d). The best bone-shape emitter has a bone angle of $\alpha_{\mathrm{E,B}} = 30°$ and a $W_{\mathrm{E,B}} = 800$ nm, as illustrated on Fig 3.25 (c). As a result, the emitter end undercut has a width of ≈ 200 nm per end. The repeatable and reproducible emitter end undercut improves the device yield and prevents the degradation of the high-frequency device performance by keeping the $A_{\mathrm{C}}/A_{\mathrm{E}}$ ratio constant for a fixed emitter electrode length.

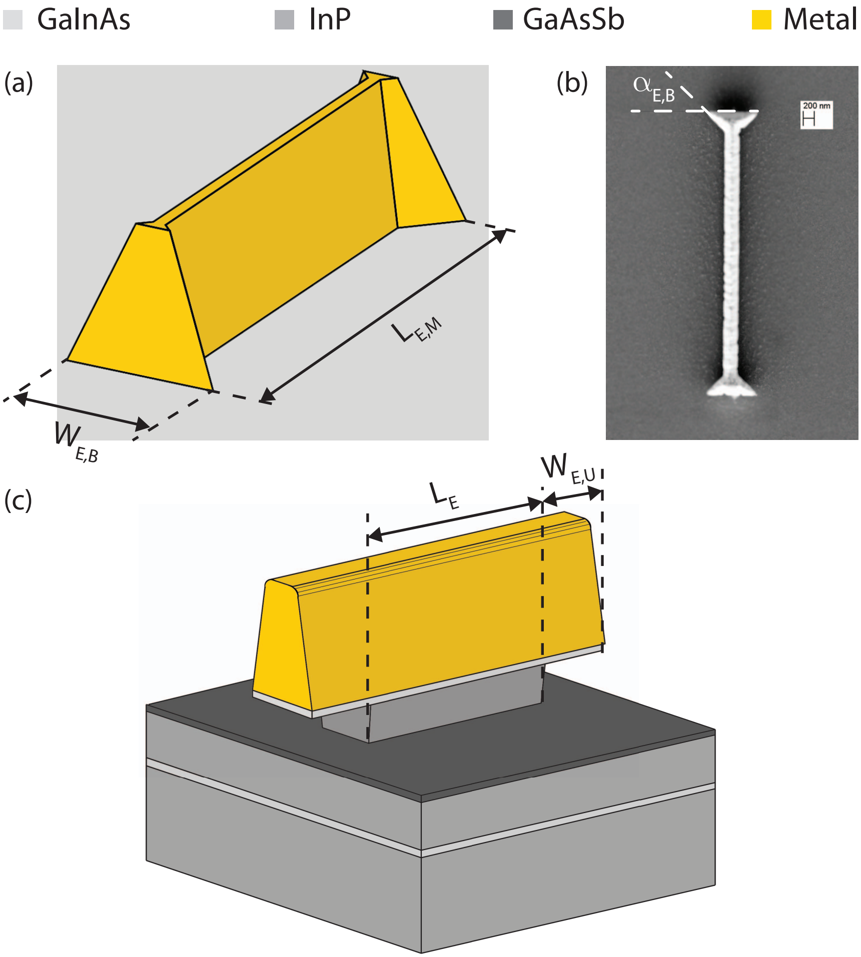

GaInAs
InP
GaAsSb
Metal
(a)
(b)
(c)
W_E,B
L_E,M
α_E,B
200 nm
L_E
W_E,U

Figure 3.24 (a) Schematic representation of the bone-shape emitter electrode (b) SEM image of the bone-shape emitter electrode (top view) (c) Schematic representation of the rectangular-shape emitter electrode. Important geometrical dimensions are labeled

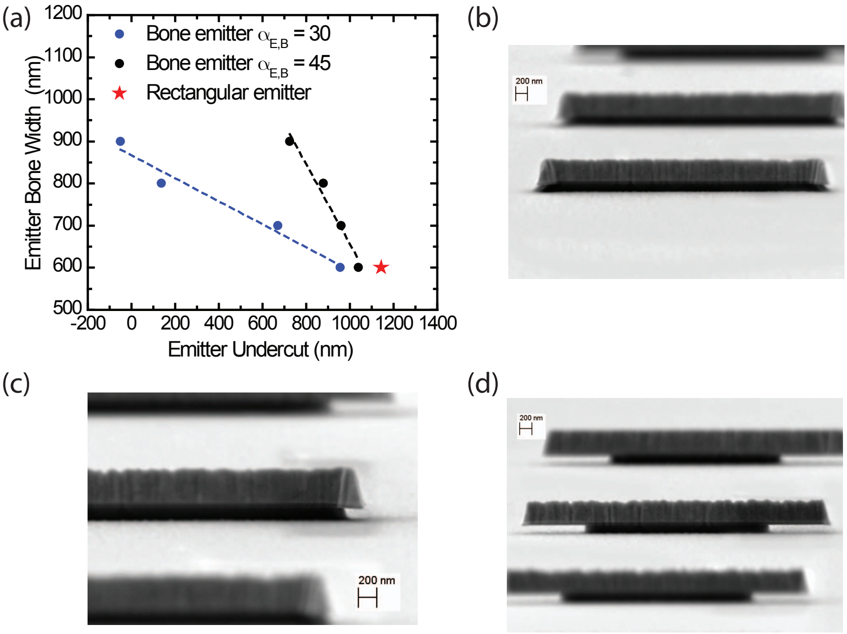


Figure 3.25 (a) Dependence of the emitter end undercut on the geometrical parameters of the bone-shape emitter electrode (b) SEM image of the device with the insufficient emitter end undercut (side view) (c) SEM image of the device with the emitter end undercut ≈ 200 nm per end (side view) (d) SEM image of the device with the excessive emitter end undercut (side view)

3.7 Base-Collector Mesa Passivation

The aggressive vertical scaling of the devices is a promising strategy to improve the high-frequency performance of DHBTs. However, to improve the $f_{\mathrm{T}} \times BV_{\mathrm{CEO}}$ product for the thin-collector devices, BV_{CEO} should not be appreciably reduced from the reduced collector thickness. One possible solution is to improve the open-base collector-to-emitter break down voltage BV_{CEO} by the passivation of the base-collector mesa with conformal SiN_x layer [11]. The SiN_x passivation layer seems to reduce the surface state charge density on the InP semiconductor surface, and, therefore, to increase the breakdown. This effect is associated with the Fermi level position at the SiN_x/InP interface: It is near the midgap level, and thus no electron accumulation layer formed at the interface [61]. An additional advantage of the passivation is that the SiN_x layer provides a mechanical support for the overhanging ledge of the base semiconductor layer with the base metal contact posts. This enables an underetching of the extrinsic collector material, and thus reducing the base-collector capacitance.

Devices were fabricated in a conventional fabrication process up to the base-collector mesa etching. After the base-collector mesa is formed, a $\approx 30\,\mathrm{nm}$ thick SiN_x layer is deposited by PECVD. To remove the SiN_x from the metal contacts and the base semiconductor surface, it is over-etched using the RIE system with CF_4 gas. Figure 3.26 shows the SEM image of the device after the SiN_x over-etch. The arrows indicate the SiN_x under the base metal contact. Once the SiN_x base-collector mesa passivation is finished, the fabrication of the device is accommodated according to the conventional process described in Section 3.2.

The devices feature a 125-nm-thick InP:Si collector doped at $1.5 \times 10^{17}\ \mathrm{cm}^{-3}$, which is higher than the the epitaxial transistor layers described in Section 3.1. Therefore, the value of te BV_{CEO} is slightly lower than previously reported in this Chapter. Figure 3.27 (a) shows the dependence of I_{C} on V_{CE}. The black curve corresponds to a device fabricated according to the conventional fabrication process, and the red curve corresponds to a device identical in epitaxial structure and comparable in fabrication except for the SiN_x base-collector passivation. For the devices with the $A_{\mathrm{E}} = 0.25 \times 4.4\ \mu\mathrm{m}^2$ and base contact width $W_{\mathrm{B,C}} = 0.35\ \mu\mathrm{m}$, the BV_{CEO} was

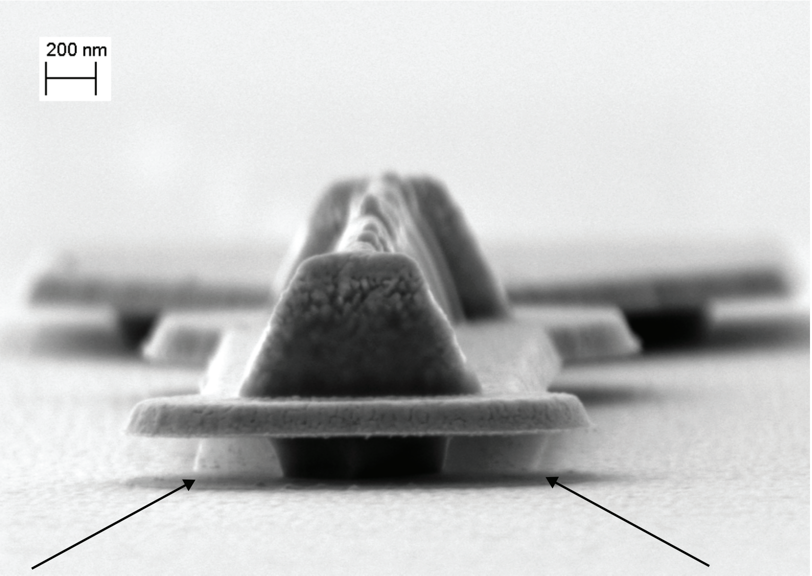


Figure 3.26 SEM image of the device after the SiN_x over-etch, the arrows indicate the SiN_x under the base metal contact

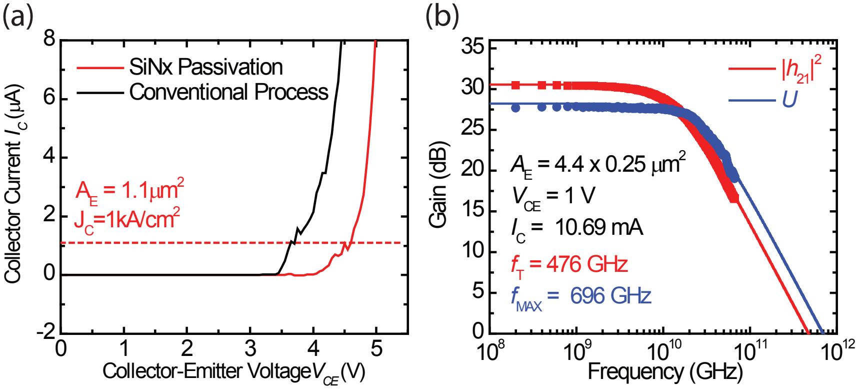


Figure 3.27 (a) Breakdown Voltage BV_{CEO}. The black curve corresponds to a device fabricated according to the conventional fabrication process and the red curve corresponds to a device identical in epitaxial structure and similar in fabrication except with the SiN_x base-collector passivation (b) Extrapolations based on single-pole fits yield f_{MAX} = 696 GHz with a simultaneous f_T = 476 GHz at V_{CE} = 1.0 V

increased from 3.6 to 4.1 V by the SiN_x base-collector junction passivation. Extrapolations based on single-pole fits yield a $f_{\mathrm{MAX}} = 696\,\mathrm{GHz}$ with a simultaneous $f_{\mathrm{T}} = 476\,\mathrm{GHz}$ at $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$, as shown in Fig. 3.27 (b). The $f_{\mathrm{T}} \times BV_{\mathrm{CEO}}$ product thus exceeds 1950 GHz-V.

Chapter 4

Optimization of the DHBT Epitaxial Layer Structure

The transistor material design defines the transport properties of the carriers in the device. Hence, in order to improve f_{T} and thus f_{MAX}, it is necessary to understand the possibilities and limitations of a given epitaxial layer structure. The main focus of this chapter lies on the reduction of the transistor transit time through the optimization of the epitaxial layer structure. The epitaxial structures presented in this chapter incorporate tree main variations compared to the conventional InP/GaAsSb DHBT epitaxial layer structure (described in Section 3.1): Firstly, an energy launcher for the hot electron injection at the emitter/base interface is introduced. To create a ramp in the conduction band at the emitter/base interface layer, the Ga content in the InP/GaInAs emitter layer is changed. Secondly, the thickness of the base layer is reduced. Thirdly, in order to generate a built-in quasielectric field in the base, and thus to accelerate the carrier transport, a stronger base grading is implemented.

The DHBTs produced on the optimized epitaxial layers were fabricated using the conventional fabrication process based on the emitter ion milling method described in Section 3.5.4.

4.1 Emitter Launcher

The composite emitter consists of three main parts: the GaInAs contact layer, the InP layer and the GaInP/InP grading layer adjacent to the base. The contact layer allows fabricating the ohmic contacts with a low resistivity. The InP layer provides the mesa height needed to avoid the emitter-base short circuit. The GaInP layer at a Ga concentration of 22% provides a conduction band alignment with a $\mathrm{GaAs_{0.59}Sb_{0.41}}$ base layer. However, GaAsSb-based DHBTs exhibiting a type-I emitter-base have demonstrated an increase of the common-emitter current gain β and f_{T} [67,68]. The improvement in the device performance is attributed to the AlInP layer at the emitter/base interface, which is used to create an energy launcher for the hot electron injection. However, devices with an AlInP emitter layer have demonstrated a stronger emitter size effect (ESE) and a higher base surface recombination velocity in comparison to devices with GaInP emitters [30, 55, 69]. Therefore, the scalability of the devices with AlInP emitters is less promising than the one of the devices with GaInP emitters. In order to benefit from the type-I emitter-base conduction band alignment and to keep the potential advantage in device scalability, DHBTs with the $\mathrm{Ga_{0.1}In_{0.9}P/GaAs_{0.7}Sb_{0.3}}$ and $\mathrm{Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}}$ emitter/base interface layer were fabricated. The epitaxial structures are shown in Figure 4.1 (a).

The epitaxial structures have two different compositions at the emitter adjacent to the base layer: $\mathrm{Ga_{0.1}In_{0.9}P/GaAs_{0.7}Sb_{0.3}}$ and $\mathrm{Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}}$. In both cases, the emitter consists of 15 nm $\mathrm{Ga}_y\mathrm{In}_{1-y}\mathrm{P}$, where the first 5 nm next to the base have a constant composition and the following 10 nm are linearly graded to $y = 0$. The intermediate n^+ InP layer and the GaInAs cap were doped at densities of $\sim 1.3 \times 10^{19}$ cm^{-3} and $\sim 3.8 \times 10^{19}$ cm^{-3}, respectively. The transistors have a 15-nm-thick $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base with $R_{\mathrm{SH}} \approx 1430\Omega/\square$ and an average doping $N_{\mathrm{B,AV}} \approx 1.2 \times 10^{20}$ cm^{-3}. The DHBTs feature a graded base, where the first 4 nm next to the emitter have a constant composition of $x = 0.7$ and the following 11 nm are linearly graded from $x = 0.6$ on the emitter side to $x = 0.3$ on the collector side.

Fig. 4.1 (b) shows the conduction band discontinuity ΔE_{C} between GaAsSb and GaInP as a function of the As content x for $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$

(a)

	Structure 1	Structure 2	Doping (cm^{-3})	(nm)
Emitter Contact Layer	$Ga_{0.25}In_{0.75}As$	$Ga_{0.25}In_{0.75}As$	Si: 3.8 x 10^{19}	5
	$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	Si: 3.8 x 10^{19}	10
	$Ga_{0.47}In_{0.53}As$	$Ga_{0.47}In_{0.53}As$	Si: 3.8 x 10^{19}	20
Emitter	InP	InP	S: 1.3 x 10^{19}	130
	InP	InP	Si: 2.5 x 10^{16}	5
	$Ga_{0.1}In_{0.9}P \rightarrow InP$	$Ga_{0.27}In_{0.73}P \rightarrow InP$	Si: 2.5 x 10^{16}	10
	$Ga_{0.1}In_{0.9}P$	$Ga_{0.27}In_{0.73}P$	Si: 2.5 x 10^{16}	5
Base	$GaAs_{0.7}Sb_{0.3}$	$GaAs_{0.7}Sb_{0.3}$	C: 1.2 x 10^{20}	4
	$GaAs_{0.6}Sb_{0.4} \rightarrow GaAs_{0.3}Sb_{0.7}$	$GaAs_{0.6}Sb_{0.4} \rightarrow GaAs_{0.3}Sb_{0.7}$	C: 1.2 x 10^{20}	11

(b)

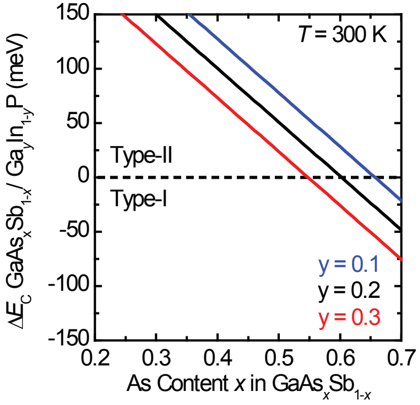


Figure 4.1 (a) Epitaxial layer structures with $Ga_{0.1}In_{0.9}P/GaAs_{0.7}Sb_{0.3}$ and $Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}$ emitter/base interface layers. The InP collector, buffer and substrate are not shown (b) The conduction band discontinuity between $GaAs_xSb_{1-x}$ and $Ga_yIn_{1-y}P$ determined from [70, 71] as a function of the As content x in GaAsSb with the Ga content y in GaInP as a parameter

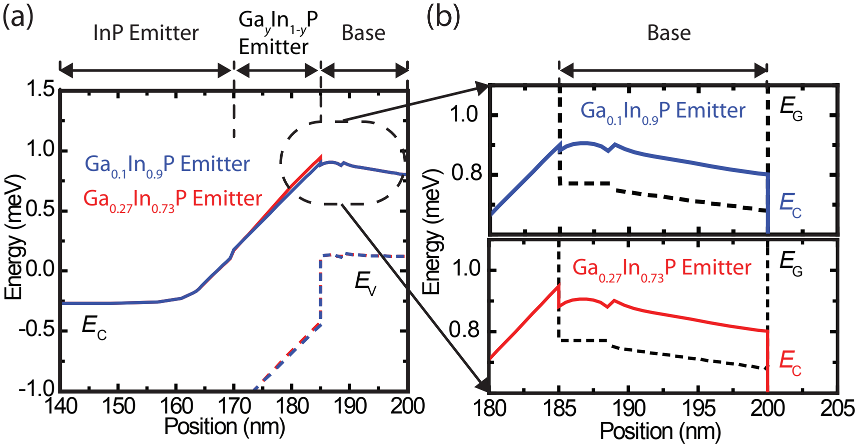


Figure 4.2 Simulated equilibrium band diagram of a DHBT with an epitaxial layer structure as described in Fig. 4.1 (shown without the InP collector, buffer and substrate) $Ga_yIn_{1-y}P/GaAs_{0.7}Sb_{0.3}$ and $Ga_yIn_{1-y}P/GaAs_{0.7}Sb_{0.3}$

and $Ga_yIn_{1-y}P$ with Ga contents of $y = 0.1$, 0.2, and 0.3. The values for the conduction band discontinuity are determined from the GaInP/InP and GaAsSb/InP band offsets reported in [71] and [70]. The negative value of the of ΔE_C corresponds to a type-I band lineup. Increasing the Ga content of the GaInP results in a larger ΔE_C, and thus in a more significant electron energy ramp. The heterojunction between $Ga_yIn_{1-y}P$ and $GaAs_{0.7}Sb_{0.3}$ for $y = 0.1$ has a type-I band alignment with $\Delta E_C \approx +20$meV. For $y = 0.27$ it has a type-I band alignment with $\Delta E_C \approx +75$meV. The simulated equilibrium band structures of the DHBTs with a $Ga_{0.1}In_{0.9}P/GaAs_{0.7}Sb_{0.3}$ (blue line) and a $Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}$ (red line) emitter/base are shown in Fig. 4.2.

The effect of the emitter energy launcher on the DHBTs DC and RF performance is investigated using devices featuring a 0.25×4.4 µm^2 emitter area. On the QDHBTs DC performance, it is investigated using devices featuring a 20×30 µm^2 emitter area. The dependence of the common-emitter current gain β on the collector current density J_C at $V_{BC} = 0\,$V for DHBTs featuring a 0.25×4.4 µm^2 emitter area and the QDHBTs featuring a 20×30 µm^2 emitter area are presented in Fig. 4.3 (a). Devices with $Ga_{0.1}In_{0.9}P$ and $Ga_{0.27}In_{0.73}P$ emitters show a very similar ESE: As

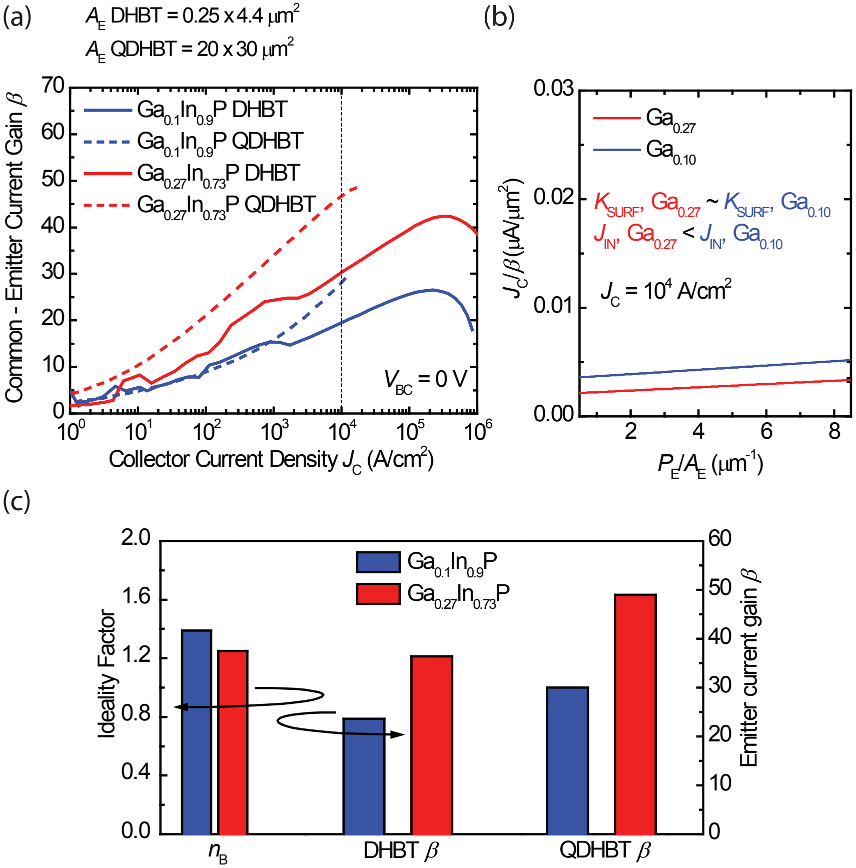


Figure 4.3 (a) Common-emitter current gain β versus the collector current density J_C at $V_{BC} = 0\,\mathrm{V}$ for DHBTs featuring a 0.25×4.4 $\mu\mathrm{m}^2$ emitter area and QDHBTs featuring a 20×30 $\mu\mathrm{m}^2$ emitter area (b) The ratio of J_C/β plotted versus P_E/A_E at $J_C = 10^4$ A/cm^2 for DHBTs with $\mathrm{Ga_{0.1}In_{0.9}P}$ and $\mathrm{Ga_{0.27}In_{0.73}P}$ emitters (c) Left: The mean deviation of the base ideality factor of the DHBTs with 10 and 27% Ga content in the emitter layer featuring the 0.20×4.4 $\mu\mathrm{m}^2$ emitter area. Right: The mean deviation of the current gain cutoff frequency of the DHBTs featuring the 0.20×4.4 $\mu\mathrm{m}^2$ emitter area and QDHBTs featuring the 20×30 $\mu\mathrm{m}^2$ emitter area with 10 and 27% Ga content in the emitter layer

the emitter area is reduced from 20×30 µm^2 to 0.25×4.4 µm^2 at $J_\mathrm{C} = 10^4\,\mathrm{V/cm^2}$, β is reduced by $\approx 35\,\%$ for the devices with $\mathrm{Ga_{0.1}In_{0.9}P}$ and by $\approx 30\,\%$ for the devices with $\mathrm{Ga_{0.27}In_{0.73}P}$. Two important parameters that are influencing the ESE and the difference in the DC performance of the devices are the base surface recombination current density K_SURF and the intrinsic recombination current density J_IN. Those parameters can be extracted from the equation [33]:

$$\frac{J_\mathrm{C}}{\beta} = J_\mathrm{IN} + K_\mathrm{SURF}\frac{P_\mathrm{E}}{A_\mathrm{E}}, \tag{4.1}$$

where P_E is the emitter periphery. Figure 4.3 (b) shows the ratio of J_C/β plotted versus $P_\mathrm{E}/A_\mathrm{E}$ at $J_\mathrm{C} = 10^4\,\mathrm{A/cm^2}$ for DHBTs with $\mathrm{Ga_{0.1}In_{0.9}P}$ and $\mathrm{Ga_{0.27}In_{0.73}P}$ emitters. The slope of the linear fit through the data corresponds to the size parameter: The base surface recombination current density K_SURF and the intersect of a linear fit with the ordinate axis corresponds to the intrinsic recombination current density J_IN. The data reveal comparable values of K_SURF for both emitter compositions, and thus confirm the ESE demonstrated in Fig. 4.3 (a). However, the $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter shows a lower intrinsic recombination current density in comparison to the $\mathrm{Ga_{0.1}In_{0.9}P}$ emitter. This can be explained by the higher injection velocity due to the larger electron launcher at the $\mathrm{Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}}$ base/emitter interface. Figure 4.3 (c) reports the comparison of the mean deviation of the base current ideality factor and common-emitter current gain β of the DHBTs and QDHBTs. The base ideality factors n_B for the devices with 0.25×4.4 µm^2 emitter area are 1.39 ±0.05 with the $\mathrm{Ga_{0.1}In_{0.9}P}$ emitter and 1.25 ±0.02 with the $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter, whereas the collector ideality factors n_C are 1.03 in both cases. The base ideality factor corresponds to the potential height of the ΔE_C. The decrease of the ideality factor indicates that the recombination current decreases [68]. Therefore, at the $\mathrm{Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}}$ emitter-base junction, the injection of the electrons into the base is enhanced, and thereby the common-emitter current gain β is increased as demonstrated in Fig. 4.3 (c).

For the DHBTs with the two different Ga contents in the emitter layer, the mean and the standard deviation of the base and the collector delay times $\tau_\mathrm{B} + \tau_\mathrm{C}$ calculated using values extracted from the S-parameter data

Emitter/Base layer material	$\tau_B + \tau_C$ [fs]	f_T [GHz]
$Ga_{0.1}In_{0.9}P/GaAs_{0.7}Sb_{0.3}$	178 ±9	458 ±15
$Ga_{0.27}In_{0.73}P/GaAs_{0.7}Sb_{0.3}$	164 ±11	483 ±12

Table 4.1 The mean and the standard deviation of the base and collector transit delay $\tau_B + \tau_C$ and f_T determined at V_{CE}= 1.2 V and $I_C = I_{C,Kirk}$ for DHBTs featuring 10% and 27% Ga content in the emitter layer with the 0.20 × 4.4 μm² emitter area

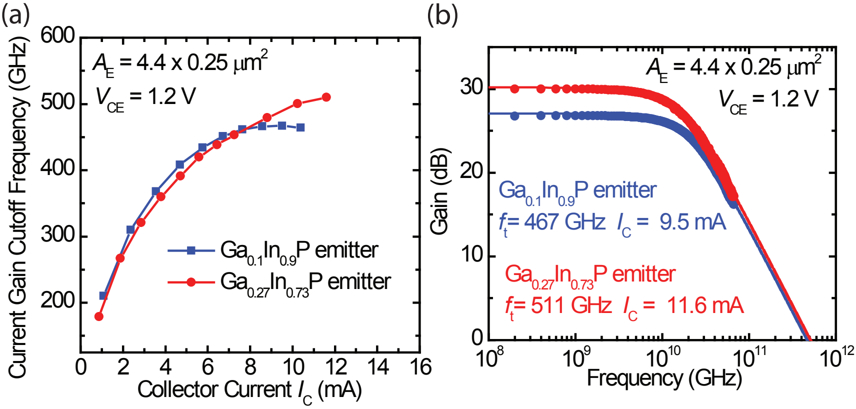


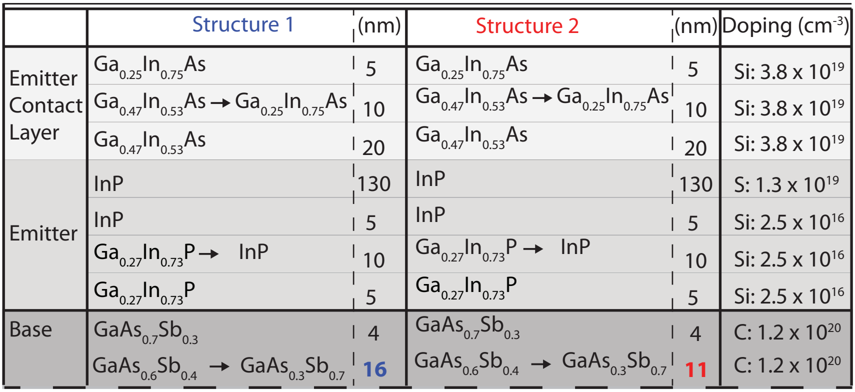
Figure 4.4 (a) The dependence of f_T on the collector current I_C for DHBTs featuring a 10 and a 27% Ga content in the emitter layer with the 0.20 × 4.4 μm² emitter area (b) Extrapolation of the f_T by the single-pole transfer function fit of the DHBT featuring $Ga_{0.27}In_{0.73}P$ emitter with the 0.20 × 4.4 μm² emitter area. Inset table: Individual contributions of the base transit time and collector delay time to the total delay time calculated from the extracted small-signal equivalent circuit

as well as the mean and the standard deviation of the measured f_T are shown in Table 4.1. The decrease in the base and the collector delay times $\tau_\mathrm{B} + \tau_\mathrm{C}$ can be observed in the devices with a higher Ga content. The decrease in the $\tau_\mathrm{B} + \tau_\mathrm{C}$ is attributed to the higher electron energy ramp at the base-emitter interface, which enables a higher electron injection velocity at the emitter-base interface. For the DHBT with the $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter and with the $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area, the extraction of the small-signal equivalent circuit gives the value of $\tau_\mathrm{B} \approx 60\,\mathrm{fs}$ and the value of $\tau_\mathrm{C} \approx 99\,\mathrm{fs}$. Furthermore, the devices with a $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter show an increase in the current gain cutoff frequency f_T from 458 ±15 to 483 ±12 GHz. Fig. 4.4 (a) shows the dependence of f_T on the collector current for a DHBT with a 10 and a 27% Ga content in the emitter layer. In Fig. 4.4 (b), the extrapolation of the f_T with either a $\mathrm{Ga_{0.1}In_{0.9}P}$ or a $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter is shown.

In conclusion, a similar emitter size effect is observed for DHBTs built with a 10% and a 27% Ga content in the emitter layer. Therefore, in terms of scalability, devices with different Ga content are comparable. However, the $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter results in a higher f_T as well as a higher β compared to $\mathrm{Ga_{0.1}In_{0.9}P}$ emitter. Thus, the high-speed performance of the transistor as well as the common-emitter current gain are improved via hot electron injection at the emitter/base interface. It is worth pointing out that one of the devices with the $\mathrm{Ga_{0.27}In_{0.73}P}$ emitter and with the $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area achieved an exceptionally high f_T of 511 GHz, as shown in Fig. 4.4 (b).

4.2 Base Thickness

Further improving the device performance (in particular high-frequency figures-of-merit such as f_T and f_MAX) is not possible without vertical device scaling [22]. The f_T is inversely proportional to the total emitter-collector delay τ_EC (Eqn. 2.6), which equals to the sum of the transistor transit time and the RC-time delays (Eqn. 2.7). Therefore, a reduction of the DHBT layer thicknesses reduces the electron travel time through the device, and thus increases the f_T up to the point where RC contributions begin to dominate [72, 73]. In this Section, the effect of the reduced base layer thickness on the base transit time τ_B is first presented. Secondly, the



	Structure 1	(nm)	Structure 2	(nm)	Doping (cm^{-3})
Emitter Contact Layer	$Ga_{0.25}In_{0.75}As$	5	$Ga_{0.25}In_{0.75}As$	5	Si: 3.8 x 10^{19}
	$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	10	$Ga_{0.47}In_{0.53}As \rightarrow Ga_{0.25}In_{0.75}As$	10	Si: 3.8 x 10^{19}
	$Ga_{0.47}In_{0.53}As$	20	$Ga_{0.47}In_{0.53}As$	20	Si: 3.8 x 10^{19}
Emitter	InP	130	InP	130	S: 1.3 x 10^{19}
	InP	5	InP	5	Si: 2.5 x 10^{16}
	$Ga_{0.27}In_{0.73}P \rightarrow$ InP	10	$Ga_{0.27}In_{0.73}P \rightarrow$ InP	10	Si: 2.5 x 10^{16}
	$Ga_{0.27}In_{0.73}P$	5	$Ga_{0.27}In_{0.73}P$	5	Si: 2.5 x 10^{16}
Base	$GaAs_{0.7}Sb_{0.3}$	4	$GaAs_{0.7}Sb_{0.3}$	4	C: 1.2 x 10^{20}
	$GaAs_{0.6}Sb_{0.4} \rightarrow GaAs_{0.3}Sb_{0.7}$	**16**	$GaAs_{0.6}Sb_{0.4} \rightarrow GaAs_{0.3}Sb_{0.7}$	**11**	C: 1.2 x 10^{20}

Figure 4.5 The epitaxial layer structures with a 20 nm (Structure 1) and a 15 nm (Structure 2) base layer thickness. The InP collector, the buffer and the substrate are not shown

DC current gain and the RF performance of the DHBTs are compared.

Transistors with $T_B = 20$ nm (Structure 1) and $T_B = 15$ nm (Structure 2) are used in this comparison. The epitaxial structures used for the DHBT fabrication are presented in Fig. 4.5. In both cases, the emitter consists of 15 nm $Ga_{0.27}In_{0.73}P$. The first 5 nm next to the base have a constant composition and the following 10 nm were linearly graded to a pure InP. The intermediate n^+ InP layer and the GaInAs cap were doped at densities of $\sim 1.3 \times 10^{19}$ cm ^{3} and $\sim 3.8 \times 10^{19}$ cm ^{3}, respectively. The DHBTs feature a graded $GaAs_xSb_{1\ x}$ base. The first 4 nm next to the emitter have a constant composition of $x = 0.7$ and the following 16 or 11 nm are linearly graded from $x = 0.6$ on the emitter side to $x = 0.3$ on the collector side. The comparison of the mean and the standard deviation of the common-emitter current gain β at $V_{BC} = 0$ V is presented in Fig. 4.6. The comparison is done for DHBTs featuring a 0.25×4.4 μm^2 emitter area and QDHBTs featuring a 20×30 μm^2 emitter area. Due to the reduced bulk recombination, the common-emitter current gain β increases with decreasing T_B from 20 to 15 nm for both device sizes. However, for the large area devices, the bulk recombination current has a stronger influence than for small area devices. Therefore, the improvement of the common-emitter current gain β for the QDHBTs is larger than for the DHBTs. The reason is that the emitter periphery-to-area ratio P_E/A_E for the small area devices is increasing, and thus the base surface recombination current

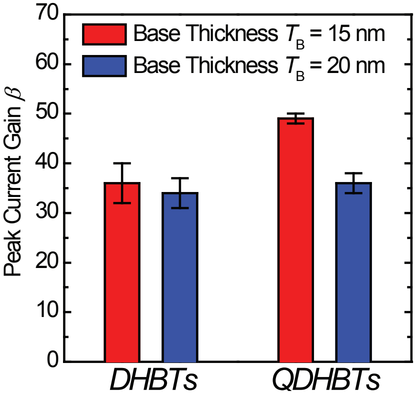


Figure 4.6 The mean and the standard deviation of the current gain cutoff frequency of the DHBTs featuring the 0.20×4.4 µm^2 emitter area and QDHBTs featuring a 20×30 µm^2 emitter area with a 15 and a 20 nm base layer thickness

dominates over the bulk recombination current. Hence, the effect of the reduced base thickness on the small area devices is less pronounced than for the QDHBTs.

Table 4.2 shows the mean and the standard deviation of the $\tau_B + \tau_C$ and the corresponding f_T for 0.25×4.4 µm^2 emitter DHBTs with a base thicknesses of $T_B = 15$ and 20 nm. Thinning the base layer from 20 to 15 nm results in an increase of the f_T from 414 ±12 to 492 ±13 GHz. The improvement in the f_T is attributed to a reduction of the base transit time τ_B. This conclusion is firstly based on the fact that the base composition and the base doping gradients are the same for both base thicknesses. Therefore, the collector delay time is not expected to be influenced by the base thickness, and thus is equal in both cases [74, 75]. Secondly, it is confirmed by the collector delay time extraction from the SSEC of the 0.25×4.4 µm^2-emitter DHBT: For a base layer thickness of $T_B = 20$ nm, τ_C results in 93 fs. For the base layer thickness $T_B = 15$ nm, τ_C equals to 95 fs. The base transit time extraction for the same devices shows $\tau_B = 119$ fs for $T_B = 20$ nm, and $\tau_B = 73$ fs for $T_B = 15$ nm. Hence, reducing T_B from 20 to 15 nm shortens the base transit time by 46 fs. Figure 4.7 shows the extrapolations of the f_T based on single-pole fits. By reducing the base thickness from 20 to 15 nm, the f_T increases from 418 to 495 GHz, which agrees well with the decrease observed in τ_B.

Base Layer	$\tau_{\mathrm{B}}+\tau_{\mathrm{C}}$ [fs]	f_{T}[GHz]
T_{B}=15 nm	159 ±11	492 ±13
T_{B}=20 nm	201 ±6	414 ±12

Table 4.2 The mean and standard deviation of the base and collector transit delay $\tau_{\mathrm{B}}+\tau_{\mathrm{C}}$ and the corresponding f_{T} for 0.25×4.4 $\mu\mathrm{m}^2$-emitter DHBTs with base thicknesses T_{B} of 15 and 20 nm

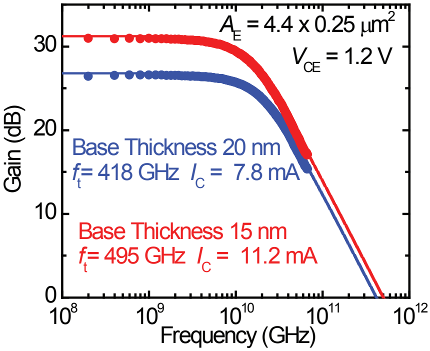


Figure 4.7 Extrapolation of the f_{T} by single-pole transfer function fits for the 0.25×4.4 $\mu\mathrm{m}^2$ emitter DHBTs with T_{B} = 20 nm and T_{B} = 15 nm. The base transit time extraction results in τ_{B} = 119 fs for T_{B} = 20 nm and τ_{B} = 73 fs for T_{B} = 15 nm

However, reducing the base thickness also affects the base resistance R_{B}: The intrinsic and extrinsic base resistances are increasing when the base thickness is reduced. The reason for this is that $R_{\mathrm{B,I}}$ and $R_{\mathrm{B,E}}$ are dependent on the base sheet resistance R_{SH}, as stated in the Eqn. 2.10 - 2.13. The base sheet resistance can be described by the following expression

$$R_{\mathrm{SH}} = \frac{1}{q \int_0^{T_{\mathrm{B}}} \mu_{\mathrm{n}}(x) N_{\mathrm{B}}(x) dx}, \tag{4.2}$$

where N_{B} is the base doping and μ_{n} is the electron mobility. The doping profile and the doping level were previously optimized and discussed in detail in other theses in our group [36]. Hence, the base doping was kept unchanged for both transistor structures. Therefore, by decreasing the base thickness T_{B}, the sheet resistance R_{SH} is increasing. As the f_{MAX}

Base Layer	R_{SH} [$\Omega/\square$]	R_{B} [Ω]	f_{MAX} [GHz]
T_{B}=15 nm	1436 ±18	28 ±4	583 ±18
T_{B}=20 nm	1082 ±7	31 ±4	532 ±41

Table 4.3 The mean and standard deviation of the R_{SH}, total base resistance R_{B} and corresponding the f_{MAX} for 0.25×4.4 µm^2-emitter DHBTs with base thicknesses T_{B} of 15 nm and 20 nm

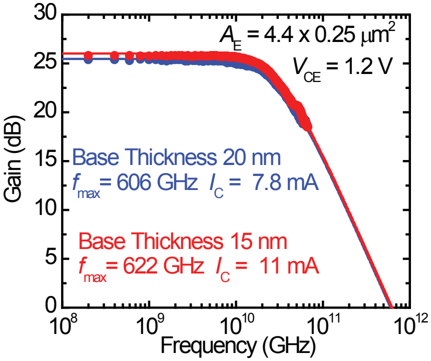


Figure 4.8 Extrapolation of the f_{MAX} by single-pole transfer function fits for the 0.25×4.4 µm^2 emitter DHBTs with T_{B} = 20 nm and T_{B} = 15 nm

is proportional to $\sqrt{f_{\mathrm{T}}/(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}}$, there is a tradeoff in the f_{MAX} improvement: Both f_{T} and $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ are higher for thinner bases.

The sheet resistance and the calculated values of the total base resistance R_{B} ($R_{\mathrm{B}} = R_{\mathrm{B,I}} + R_{\mathrm{B,E}}$) as well as the corresponding f_{MAX} are presented in Table 4.3. The comparison is made for the 0.25×4.4 µm^2 emitter DHBTs with a base thickness T_{B} of 15 and 20 nm. As expected, R_{SH} is increasing for devices with a thinner base. However, the R_{B} for both base thicknesses are comparable. A possible reason is that the base contact resistance $R_{\mathrm{B,C}}$ is much higher for the DHBTs with a 20 nm base, which is believed to originate from process related issues. As a consequence of the high base resistance, the f_{MAX} of the DHBTs with a base thickness of $T_{\mathrm{B}} = 20$ nm is lower than the f_{MAX} of the DHBTs with a 15 nm base. Extrapolations of the f_{MAX} at $V_{\mathrm{CE}} = 1.2$ V for the devices with $T_{\mathrm{B}} = 20$ nm and $T_{\mathrm{B}} = 15$ nm are shown in Fig. 4.8. For the 0.25×4.4 µm^2 emitter DHBTs with the base thickness $T_{\mathrm{B}} = 20\,\mathrm{nm}$ and $R_{\mathrm{SH}} = 1081 \pm 7\,\Omega/\square$ (epistructure described in Section 3.1), R_{B} is $\approx 20\,\Omega$. Assuming that C_{BC} and the f_{T} are constant and R_{B} equals to $20\,\Omega$, the value of the f_{MAX} should be $\approx 660\,\mathrm{GHz}$.

In conclusion, due to the reduced bulk recombination, the common-emitter current gain β increases with decreasing a T_{B} from 20 to 15 nm. Also, by decreasing the base thickness, the base transit time is reduced, thus enhancing the transit frequency. If the increased base resistance is outweighed by a higher f_{T}, the f_{MAX} can be improved as well.

4.3 Strong Base Grading

The base transit time τ_{B} is a significant part of the total emitter-collector delay τ_{EC}. Therefore, reducing the τ_{B} is essential for improving the f_{T}. The base transit time τ_{B} for the DHBTs can be described by the following expression

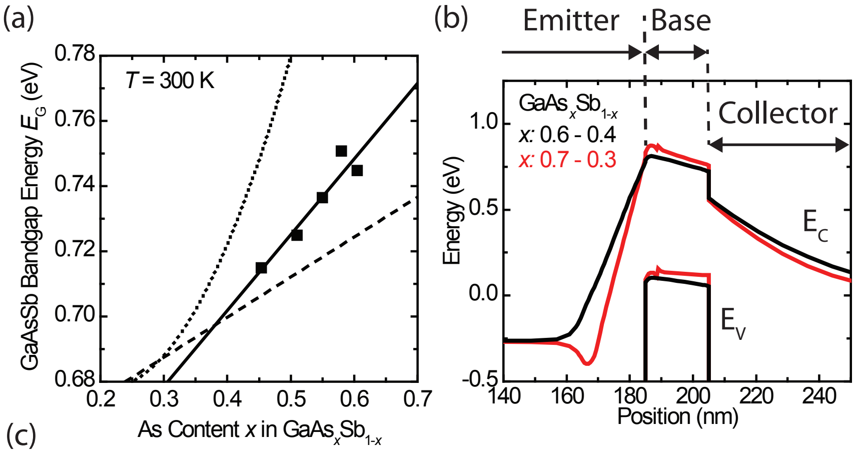
$$\tau_{\mathrm{B}} = \frac{T_{\mathrm{B}}}{v_{\mathrm{B}}} F_1 + \frac{T_{\mathrm{B}}^2}{2D_{\mathrm{n}}} F_2, \tag{4.3}$$

where the parameters F_1 and F_2 are determined by the composition and doping profiles, T_{B} is the base layer thickness, v_{B} is the electron velocity at the base-collector heterointerface and D_{n} is the electron diffusivity [36, 76]. Hence, the composition and doping profiles in graded GaAsSb bases strongly affect both the DC and the RF device performance. In a previous dissertation [36], it was shown that DHBTs with linearly graded bases from $\mathrm{GaAs}_{0.6}\mathrm{Sb}_{0.4}$ on the emitter side to $\mathrm{GaAs}_{0.4}\mathrm{Sb}_{0.6}$ on the collector side demonstrate a higher f_{T} in comparison to devices with a uniform $\mathrm{GaAs}_{0.61}\mathrm{Sb}_{0.39}$ base. Figure 4.9 (a) shows the bandgap of $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ as a function of the As content x at 300 K. By decreasing the As content along the width of the base T_{B}, the bandgap of GaAsSb is reduced. This is equivalent to a negative slope in the conduction band E_{C}. Therefore, by varying the composition across the GaAsSb base, a quasi-electric field ξ_{B} is induced:

$$\xi_{\mathrm{B}} = q^{-1} \cdot \frac{dE_{\mathrm{C}}}{dz}. \tag{4.4}$$

The quasi-electric field pushes electrons towards the collector, and thus reduces the base transit time τ_{B}. In this Section, the influence of strong compositional grading across the GaAsSb base on the DHBT DC and RF performance was further investigated. The DHBTs were fabricated according to the method described in Section 3.5.2. Both device batches were fabricated in a single run in order to minimize experimental variations. In the comparison, the transistors with $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ bases with the As content x linearly graded from $x = 0.6$ on the emitter side to $x = 0.4$ on the collector side (Structure 1) and from $x = 0.7$ on the emitter side to $x = 0.3$ on the collector side (Structure 2) were used. The epitaxial layers of Structure 2 are presented in Fig. 4.9 (c). Structure 1 (conventional structure) is described in Section 3.1. In structure 2, the emitter consists of 15 nm of $\mathrm{Ga}_y\mathrm{In}_{1-y}\mathrm{P}$, where the first 5 nm next to the base have a constant composition and the following 10 nm are linearly graded to $y = 0$. The intermediate n^+ InP layer and the GaInAs cap were doped at densities of $\sim 1.3 \times 10^{19}$ cm^{-3} and $\sim 3.8 \times 10^{19}$ cm^{-3}, respectively. The DHBTs feature a 20-nm-thick $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ graded base, where the first 4 nm next to the emitter have a constant composition of $x = 0.7$ and the following 11 nm are linearly graded from $x = 0.6$ on the emitter side to $x = 0.3$ on the collector side. To exclude the effect of the doping on the DHBTs performance, the doping profile and the average doping are similar for both structures: $N_{\mathrm{B,AV}} \approx 1 \times 10^{20}$ cm^{-3} with $R_{\mathrm{SH}} \approx 1050 \pm 10\,\Omega/\square$. The simulated band structure of DHBTs at equilibrium with a $\mathrm{GaAs}_{0.6}\mathrm{Sb}_{0.4}$-$\mathrm{GaAs}_{0.4}\mathrm{Sb}_{0.6}$ base and a $\mathrm{GaAs}_{0.7}\mathrm{Sb}_{0.3}$-$\mathrm{GaAs}_{0.3}\mathrm{Sb}_{0.7}$ base is shown in Fig. 4.9. (b). For the DHBT structure with stronger base grading, the slope of the conduction band is steeper, therefore the induced quasi-electric field ξ_{B} is larger.

Fig. 4.10 (a) shows the comparison of the mean and the standard deviation of the common-emitter current gain β at $V_{\mathrm{BC}} = 0\,\mathrm{V}$. The comparison is done for DHBTs featuring an 0.20×4.4 µm^2 emitter area and QDHBTs with a 20×30 µm^2 emitter area. Fig. 4.10 (b) presents the dependence of the common-emitter current gain β on the collector current density J_{C} at $V_{\mathrm{BC}} = 0\,\mathrm{V}$ for DHBTs featuring a 0.20×4.4 µm^2 emitter area and QDHBTs featuring a 20×30 µm^2 emitter area. The common-emitter current gain β is lower for the transistors with the stronger base grading. Potential reasons for this fact is a lower collector current I_{C} due to a larger bandgap ΔE_{G} for the As-rich transistors, and/or transport impediments associated with the stronger grading.



(c)

	Material	Doping (cm^{-3})	Thickness (nm)
Emitter Contact Layer	$\mathrm{Ga_{0.25}In_{0.75}As}$	Si: 3.8×10^{19}	5
	$\mathrm{Ga_{0.47}In_{0.53}As} \rightarrow \mathrm{Ga_{0.25}In_{0.75}As}$	Si: 3.8×10^{19}	10
	$\mathrm{Ga_{0.47}In_{0.53}As}$	Si: 3.8×10^{19}	20
Emitter	InP	S: 1.3×10^{19}	130
	InP	Si: 2.5×10^{16}	5
	$\mathrm{Ga_{0.1}In_{0.9}P} \rightarrow \mathrm{InP}$	Si: 2.5×10^{16}	10
	$\mathrm{Ga_{0.1}In_{0.9}P}$	Si: 2.5×10^{16}	5
Base	$\mathrm{GaAs_{0.7}Sb_{0.3}}$	C: 1.2×10^{20}	4
	$\mathrm{GaAs_{0.6}Sb_{0.4}} \rightarrow \mathrm{GaAs_{0.3}Sb_{0.7}}$	C: 1.2×10^{20}	16
Collector	InP	S: 1.3×10^{17}	125
Collector Pedestal	InP	S: 2.2×10^{19}	50
Collector Contact Layer	$\mathrm{Ga_{0.40}In_{0.60}As}$	Si: 3.0×10^{19}	20

Figure 4.9 (a) The room-temperature bandgap of $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ versus the As mole fraction x. The squares show the bandgap of strained GaAsSb grown on InP in our laboratory. The solid line is a fit to the experimental data given by $E_G(x) = 0.61 + 0.23x$. The dashed line represents a fit to the bandgap energies of strained GaAsSb reported in [70] and the dotted line shows the bandgap of relaxed GaAsSb [77, 78]. Figure adapted from [36] (b) The simulated conduction and valence band for the DHBTs with an $\mathrm{InP/Ga_{0.1}In_{0.9}P}$ emitter and a $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base with As content varying from $x = 0.7$ to $x = 0.3$, and from $x = 0.6$ to $x = 0.4$ (c) The epitaxial layer structures with the $\mathrm{Ga_{0.1}In_{0.9}P/GaAs_{0.7}Sb_{0.3}}$ emitter/base interface layer. The buffer and the substrate are not shown

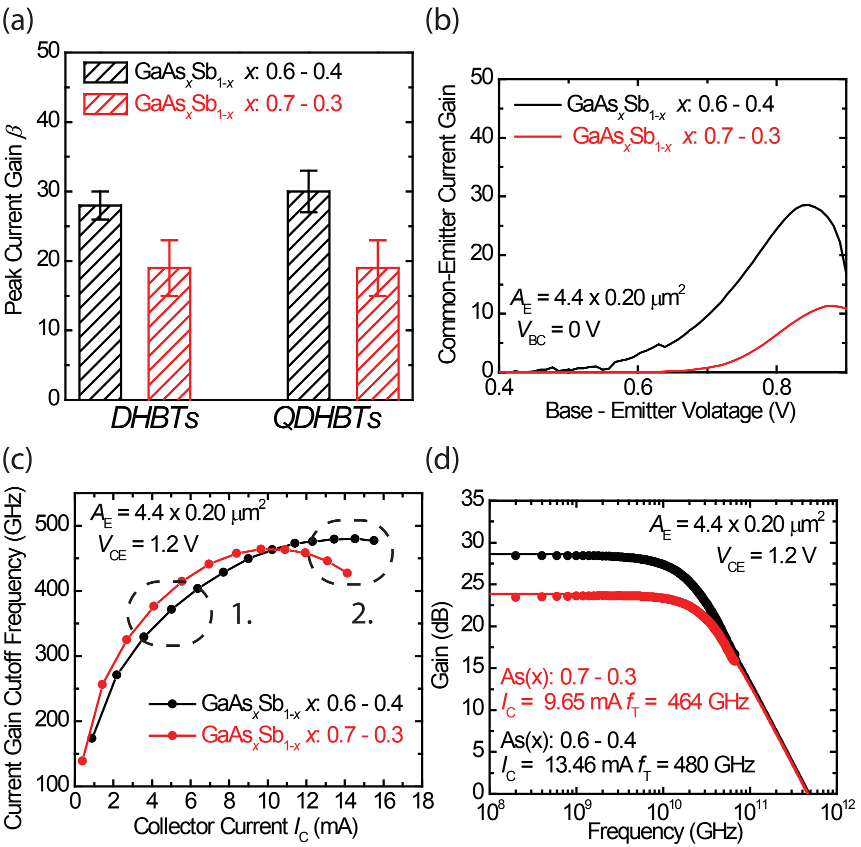
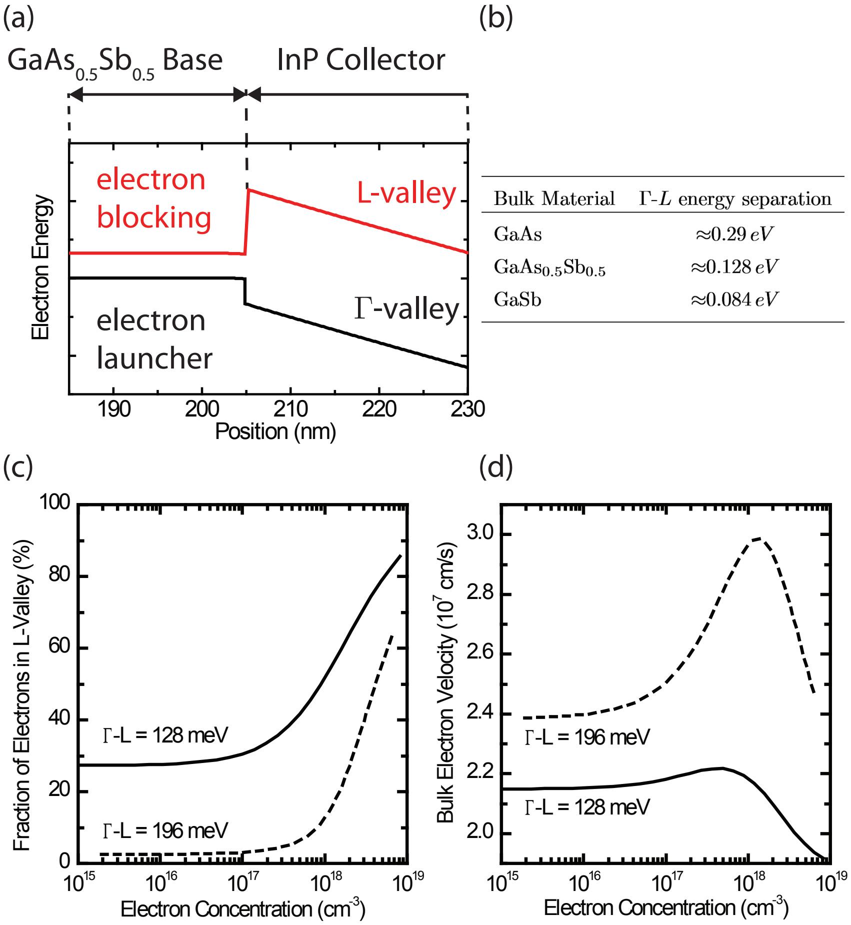


Figure 4.10 (a) The mean and the standard deviation of the current gain cutoff frequency of the DHBTs featuring a $0.20 \times 4.4\ \mu m^2$ emitter area and QDHBTs featuring a $20 \times 30\ \mu m^2$ emitter area with a $GaAs_{0.6}Sb_{0.4}$ and a $GaAs_{0.7}Sb_{0.3}$ base (b) Common-emitter current gain β versus the collector current density J_C at $V_{BC} = 0$ V for DHBTs featuring a $0.20 \times 4.4\ \mu m^2$ emitter area (c) The dependence of f_T on the collector current I_C for DHBTs featuring a $GaAs_{0.6}Sb_{0.4}$ and a $GaAs_{0.7}Sb_{0.3}$ base with the $0.20 \times 4.4\ \mu m^2$ emitter area (d) Extrapolation of the f_T by the single-pole transfer function fit of the DHBT featuring a $GaAs_{0.6}Sb_{0.4}$ and a $GaAs_{0.7}Sb_{0.3}$ base with a $0.20 \times 4.4\ \mu m^2$ emitter area



Bulk Material	Γ-L energy separation
GaAs	$\approx 0.29\,eV$
$GaAs_{0.5}Sb_{0.5}$	$\approx 0.128\,eV$
GaSb	$\approx 0.084\,eV$

Figure 4.11 (a) Band diagram at the GaAsSb/InP interface showing the alignment for the Γ- and *L*-valleys. Figure adapted from [37] (b) Approximate values of $\Delta E_{\Gamma L}$ for GaAs, $GaAs_{0.5}Sb_{0.5}$ and GaSb. The values are taken from [49, 79] (c) Fraction of electrons in the L-valley versus electron density for GaAsSb with Γ-L separations of 128 meV and 196 meV (d) Average velocity of electrons injected into a 20 nm thick slab of GaAsSb versus the electron density for Γ-L separations of 128 meV and 196 meV. Figures (c) and (d) are adapted from [79]

The dependence of the f_T on the collector current for the DHBTs with a $\mathrm{GaAs_{0.6}Sb_{0.4}}$ and a $\mathrm{GaAs_{0.7}Sb_{0.3}}$ base is shown in Fig. 4.10 (c). The DHBTs feature an $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area. Fig. 4.10 (d) shows the extrapolation of f_T with either a $\mathrm{GaAs_{0.6}Sb_{0.4}}$ or a $\mathrm{GaAs_{0.7}Sb_{0.3}}$ base. By increasing the compositional grading in the $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base from $x : 0.6 \rightarrow 0.4$ to $x : 0.7 \rightarrow 0.3$, the peak f_T *decreases* from 480 to 464 GHz, though the quasi-electric field ξ_B increasing. Moreover, at low I_C, As-rich DHBTs have a higher f_T (dashed circle 1.) but as I_C increases, the f_T of the DHBTs with weaker grading takes over (dashed circle 2.). A possible explanation for this discrepancy is that the GaAsSb has low-lying upper energy valleys: The energy separation between Γ and L valleys $\Delta E_{\Gamma\,\mathrm{L}}$ is $\approx 0.128\,\mathrm{eV}$ for the $\mathrm{GaAs_{0.5}Sb_{0.5}}$ at a p-type doping of $N_\mathrm{B} \approx 1 \times 10^{20}\ \mathrm{cm}^{-3}$ [79]. In the Γ-valleys between the GaAsSb base and the InP collector, there is a step down, and thus the electron velocity is enhanced due to an energy launcher at the base-collector junction. As for the L valleys, electrons at the GaAsSb/InP heterointerface suffer from the electron blocking effect, due to a type I band alignment, as shown in Fig. 4.11 (a) Thus, L-valley electrons in the GaAsSb base are not likely to be transferred to the InP collector. The electrons which cannot travel into the collector are reflected back to the base. Even when the material conduction bands at the heterointerface are aligned, the effective mass difference between GaAsSb and InP in the Γ valley produces a velocity mismatch that induces some reflection. However, the reflection in the Γ valley is much smaller in comparison to the L-valley. In Fig. 4.11 (b), the approximate values of $\Delta E_{\Gamma\,\mathrm{L}}$ are given. The energy separation of $\Delta E_{\Gamma\,\mathrm{L}}$ is increasing with an increasing As content in the $\mathrm{GaAs}_x\mathrm{Sb}_{1-x}$ base. Therefore, the DHBTs with a base grading from $x : 0.6 \rightarrow 0.4$ have less electrons blocked at the the L-valley than the devices with the base grading of $x : 0.7 \rightarrow 0.3$. Moreover, the effective mass of electrons in the L-valleys is much higher than in the Γ-valley, which means their mean free path and mobility are much lower [49]. Both of those factors lead to an increased base transit time, and thus to a reduced f_T. Hence, as shown in Fig. 4.10 (c) at low I_C, the quasi-electric field ξ_B is larger for the As-rich DHBTs, and thus f_T is higher (dashed circle 1.). As I_C increases, the f_T of the DHBTs with weaker grading takes over (dashed circle 2.) due to a smaller fraction of the electrons in the L-valley.

Full-band quantum transport simulations were performed in collaboration with the Integrated Systems Laboratory at ETH Zürich in order to investigate the effect of the energy separation between the Γ and L valleys on the electron transfer properties at the GaAsSb/InP heterointerface [79]. Figure 4.11 (c) and (d) agrees well with results presented in Fig. 4.10. The simulation results show a significant increase in the electron population in the L-valley when the Γ-L energy separation is shortened, which leads to a significant reduction of the electron velocity in the GaAsSb base.

In conclusion, the composition gradient of the GaAsSb base generates a quasi-electric field that was found to strongly affect both β and the f_{T} [36]. However, maximizing the composition gradient of the GaAsSb base appears to cause a considerable fraction of the electrons to populate the L-valley [49]. Thus, the base transit time is increasing and the f_{T} is decreasing. It was demonstrated that the As content in the base needs to stay at a high average level in order to avoid an injection of the electrons into the upper energy valleys.

Chapter 5

Conclusions

5.1 Summary of Results

During the course of this PhD thesis, the high-frequency performance of InP/GaAsSb DHBTs was improved: Two consecutive records for the highest f_{MAX} in InP/GaAsSb-based DHBTs were archived. The efforts were firstly focused on developing a novel fabrication process while maintaining reproducibility and a high yield in device fabrication. Secondly, the epitaxial layer structure was optimized in order to further extend the transistor RF bandwidth.

The most important achievements are summarized below:

- The first InP/GaAsSb DHBT with an f_{MAX} exceeding 700 GHz was achieved by decreasing the base contact resistivity. Compared with the conventional fabrication process, a reduction in the $(R_{\mathrm{B}}C_{\mathrm{BC}})_{\mathrm{EFF}}$ time constant by a factor of two was observed. Assuming that all other components remain unchanged, a fourfold reduction in the base contact resistance was achieved. The device was fabricated with the base Ar sputtering method with a $0.30 \times 4.4\ \mu\mathrm{m}^2$ emitter area. The base and collector current ideality factors are $n_{\mathrm{B}} = 1.53$ and $n_{\mathrm{C}} = 1.04$, respectively. The peak common-emitter current gain is $\beta = 11$ with $V_{\mathrm{BC}} = 0\,\mathrm{V}$. The common-emitter breakdown voltage BV_{CEO} is more than $5\,\mathrm{V}$ at a collector current density of $J_{\mathrm{C}} = 1\,\mathrm{kA/cm}^2$. The improved device shows an f_{MAX} that was 100 GHz higher than those previously reported with the same epitaxial layer structure [48].

- The first InP/GaAsSb DHBTs with a record f_{MAX} of 779 GHz with a simultaneous $f_{\mathrm{T}} = 503\,\mathrm{GHz}$ at $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$ was demonstrated. To the best of our knowledge, this is the highest f_{MAX} achieved to date for GaAsSb-based DHBTs. The record device featured a $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area and a $0.40 \times 5.5\ \mu\mathrm{m}^2$ collector area. The base and collector ideality factors are $n_{\mathrm{B}} = 1.43$ and $n_{\mathrm{C}} = 1.02$. The peak common-emitter current gain β is 17 with $V_{\mathrm{BC}} = 0\,\mathrm{V}$. The common-emitter current-voltage characteristics demonstrate a low offset voltage of $\approx 50\,\mathrm{mV}$. The common-emitter breakdown voltage is $BV_{\mathrm{CEO}} \approx 5\,\mathrm{V}$ at a collector current density of $J_{\mathrm{C}} = 1\,\mathrm{kA/cm}^2$. The improved self-aligned base contact formation process reduced the base access distance W_{GAP} from 60 to 30 nm compared to results previously reported by our group [48, 51]. Additionally, the reduction of the base access distance resulted in a narrower base-collector mesa, leading to a reduced base-collector capacitance. The combination of lower base access resistance and base-collector capacitance led to significant increases in both the f_{T} and the f_{MAX}. The improved high-frequency performance was achieved by a combination of Ar sputtering and wet etching in a self-aligned emitter formation process.

- The reproducibility of the device fabrication was improved by means of optimization of two fabrication steps: Firstly, the emitter Ar sputtering was substituted with emitter ion milling. The achieved base access distance and the resulting high-frequency performance are comparable to the results achieved using the emitter Ar sputtering method. The developed method is a highly reproducible and stable process. Therefore, the fabricated devices demonstrate a higher yield and a greater manufacturability. Secondly, the boned-shaped emitter was optimized in order to support a well-controlled emitter end undercut etching. The optimized, boned-shape emitter has a bone angle of $A_{\mathrm{E,B}} = 30°$ and a bone width of $W_{\mathrm{E,B}} = 800\,\mathrm{nm}$. As a result, the emitter end undercut has a width of $\approx 200\,\mathrm{nm}$ per end. The repeatable and reproducible emitter end undercut improves the yield of the fabricated devices and prevents the degradation of the high-frequency device performance by keeping the $A_{\mathrm{C}}/A_{\mathrm{E}}$ ratio constant for the fixed emitter electrode length.

- The open-base collector-to-emitter breakdown voltage BV_{CEO} was improved by passivating the base-collector mesa with a conformal SiN_x layer [11]. The SiN_x passivation layer seems to reduce the surface state charge density on the InP semiconductor surface and therefore to increase the breakdown. This effect is associated with the Fermi level position at the SiN_x/InP interface: It is near the mid-gap level, and thus no electron accumulation layer formed at the interface [61]. An additional advantage of the passivation is that the SiN_x layer provides a mechanical support to the overhanging ledge of the base semiconductor layer with the base metal contact posts. This enables underetching the extrinsic collector material, and thus reducing the base-collector capacitance. For the devices with an $A_{\mathrm{E}} = 0.25 \times 4.4\ \mu\mathrm{m}^2$ and a base contact width of $W_{\mathrm{B,C}} = 0.35\,\mu\mathrm{m}$, the BV_{CEO} was increased from 3.6 to 4.1 V by the SiN_x base-collector junction passivation. Extrapolations based on single-pole fits yield an $f_{\mathrm{MAX}} = 696\,\mathrm{GHz}$ with a simultaneous $f_{\mathrm{T}} = 476\,\mathrm{GHz}$ at $V_{\mathrm{CE}} = 1.0\,\mathrm{V}$. The $f_{\mathrm{T}} \times BV_{\mathrm{CEO}}$ product thus exceeds 1950 GHz-V.

- For the DHBTs featuring a 10% and a 27% Ga content in the emitter layer, a similar emitter-size effect was observed. Therefore, in terms of scalability, devices with different Ga content are comparable. However, the $\mathrm{Ga}_{0.27}\mathrm{In}_{0.73}\mathrm{P}$ emitter shows a lower recombination current density in comparison to the $\mathrm{Ga}_{0.1}\mathrm{In}_{0.9}\mathrm{P}$ emitter. This can be explained by the higher injection velocity due to the larger electron launcher at the $\mathrm{Ga}_{0.27}\mathrm{In}_{0.73}\mathrm{P}/\mathrm{GaAs}_{0.7}\mathrm{Sb}_{0.3}$ base/emitter interface. Therefore, a $\mathrm{Ga}_{0.27}\mathrm{In}_{0.73}\mathrm{P}$ emitter yields in a higher f_{T} as well as in a higher β compared to a $\mathrm{Ga}_{0.1}\mathrm{In}_{0.9}\mathrm{P}$ emitter. Thus, the high-speed performance of the transistor as well as the common-emitter current gain are improved via hot electron injection at the emitter/base interface. An exceptionally high f_{T} of 511 GHz was achieved for the devices with a $\mathrm{Ga}_{0.27}\mathrm{In}_{0.73}\mathrm{P}$ emitter and with a $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area.

- The influence of the base thickness reduction on DC and RF performance of the DHBTs was investigated. Firstly, it was found that the common-emitter current gain β increases with decreasing T_{B} from 20 to 15 nm. The improvement in β is attributed to the reduced bulk recombination. Secondly, the base transit time and collector delay time were extracted from the SSEC measurements for the DHBTs with the $0.20 \times 4.4\ \mu\mathrm{m}^2$ emitter area. By decreasing the base thickness from 20 to 15 nm, the base transit time was reduced by 46 fs when the collector delay time was unchanged. By reducing the base thickness from 20 to 15 nm, the f_{T} increases from 418 to 495 GHz, which agrees well with the decrease observed in the in the τ_{B}. Finally, if the increased base resistance is outweighed by a higher f_{T}, the f_{MAX} can be improved as well.

5.2 Outlook

The ETHZ Millimeter Wave Electronic group has been working on high-speed InP/GaAsSb DHBTs since 2006. Since then, the $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ was improved from $\approx$ 400/300 GHz to 503/780 GHz. The main goal of the project is to reach an f_{MAX} in excess of 1 THz with a simultaneous f_{T} in excess of 0.5 THz. THz bandwidth transistors could be achieved by optimizing four key factors:

Device Scaling: Further improvements in the f_{T} and the f_{MAX} can be made by lateral as well as vertical device scaling. Lateral device scaling by reducing the W_{GAP} (presented in Section 3.5.3) yielded a two-fold decrease of the total base resistance and led to a significant improvement of the f_{MAX}. In order to reduce the W_{GAP} from 20 to less than 10 nm, an alternative fabrication approach needs to be developed. Options include emitter sidewall spacers [4, 80] and T-shaped emitter electrodes [81]. Vertical profile scaling of the base and collector layers is expected to provide an additional substantial improvement of the high frequency performance. Reducing the base thickness from 20 to 15 nm as well as using a thinner collector of 75 instead of 125 nm decreases the total emitter-collector delay τ_{EC} by $\approx$ 80 fs. Therefore, it yields a significant improvement of both f_{T} and f_{MAX}.

Base Grading Optimization: The doping and composition gradients of the GaAsSb base generate a quasi-electric field that was found to profoundly affect both β and the f_T [36]. However, maximizing the composition gradient of the GaAsSb base causes a considerable fraction of the electrons to populate the L-valley [49]. Thus, the base transit time increases and the f_T decreases, as discussed in Section 4.1. Therefore, the base composition needs to be investigated more thoroughly in order to improve the DHBTs‘ figures-of-merit. Especially, the question of the Γ-L separation in the conduction band of the base material needs to be taken into consideration. Two ways to compositionally grade the base material appear to be promising and should hence be pursued: Firstly, the composition gradient of the GaAsSb base could be further refined (for example linear grading the GaAs$_x$Sb$_{1-x}$ base from $x = 0.7$ on the emitter side to $x = 0.4$ or 0.5 on the collector side). Secondly, adding In to the GaAsSb base material yielded a f_T that is comparable to a device with a constant GaAsSb base [37]. Therefore, a graded GaInAsSb base is expected to significantly improve the f_T, and thus the f_MAX.

Heat Dissipation: Device self-heating has a strong negative effect on the DC and RF performance of the transistors [37]. It causes a degradation of all the figures-of-merit and can permanently damage the device. Moreover, reducing the self-heating effect enables operating the devices at higher power densities and at elevated temperatures. Therefore, self-heating requires very serious and careful consideration. One approach to reduce the negative temperature influence on the DHBT operation is to use a thinner collector pedestal as well as a thinner collector contact layer. In this case, most of the heat produced by the electrons injected into the collector will be dissipated in the InP buffer. Additionally, in order to enhance heat dissipation, thinning down the InP substrate together with metallizing the sample backside seems to be a promising approach to reduce the DHBT self-heating.

Manufacturability: High-speed InP/GaAsSb DHBTs are very promising candidates for integrated millimeter-wave circuits. However, the reproducibility of the current fabrication process needs to be improved. A major reason for the low yield is the asymmetry of the devices. This is caused by two factors: Firstly, there is a large deviation of the base access distance caused by the limited mechanical precision of the electron beam evaporation system. Secondly, the base contact pad has an asymmetric shape, which leads to an uneven undercut of the collector mesa. Resolving these issues will improve the device manufacturability and fabrication yield, therefore making the ultra-high-speed InP/GaAsSb DHBT technology more mature and commercially attractive.

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List of Acronyms

DC Direct Current

DHBT Double Heterojunction Bipolar Transistor

EBL Electron Beam Lithography

ESE Emitter Size Effect

FIB Focused Ion Beam

GSG Ground-Signal-Ground

HBT Heterojunction Bipolar Transistor

ICP Inductively Coupled Plasma

MOCVD Metalorganic Chemical Vapour Deposition

PECVD Plasma-Enhanced Chemical Vapor Deposition

PMMA Poly-Methyl-Meth-Acrylate

QDHBT Quick Double Heterojunction Bipolar Transistor

RF Radio Frequency

RIE Reactive Ion Etching

SEM Scanning Electron Microscope

SHBT Single Heterojunction Bipolar Transistor

SIMS Secondary Ion Mass Spectrometer

S-parameter Scattering Parameter

SSEC Small-Signal Equivalent Circuit

THz TeraHertz

TLM Transmission Line Measurements

VNA Vector Network Analyzer

List of Variables

I	Current
I_{B}	Base current
I_{C}	Collector current
$I_{\mathrm{S,B}}$	Base saturation current
$I_{\mathrm{S,C}}$	Collector saturation current
$I_{\mathrm{C,Kirk}}$	Kirk current (I_{C} at peak f_{T})
n	Ideality factor
n_{B}	Base ideality factor
n_{C}	Collector ideality factor
β	Common-emitter current gain
J_{B}	Base current density
J_{C}	Collector current density
J_{IN}	Intrinsic recombination current density
K_{SURF}	Base surface recombination current density
V_{BE}	Base-emitter voltage
V_{BC}	Base-collector voltage
V_{CE}	Collector-emitter voltage
BV_{CEO}	Breakdown voltage
V_{OFFSET}	Offset voltage
V_{TH}	Thermal voltage
q	Elementary charge
k	Boltzmann constant
T	Absolute temperature
A_{E}	Emitter area
P_{E}	Emitter periphery
L_{E}	Emitter length
$L_{\mathrm{E,M}}$	Emitter electrode length
W_{E}	Emitter width
$\alpha_{\mathrm{E,B}}$	Boned-shape emitter angle
$W_{\mathrm{E,B}}$	Boned-shape emitter width
$W_{\mathrm{E,U}}$	Width of the emitter undercut
W_{GAP}	Base access distance

T_{B}	Thickness of the base layer
$T_{\mathrm{B,M}}$	Thickness of the base metal stack
A_{C}	Collector area
$L_{\mathrm{T,E}}$	Effective transfer length
$W_{\mathrm{B,C}}$	Width of the base contact area
$W_{\mathrm{B,M}}$	Width of the base metal contact
$W_{\mathrm{B,U}}$	Width of the base undercut
W_{C}	Collector width
W_{L}	Collector length
f_{T}	Current gain cutoff frequency
f_{MAX}	Maximum oscillation frequency
τ_{EC}	Emitter-collector transit time
τ_{B}	Base transit time
τ_{C}	Collector delay time
π	Mathematical constant (approximated as 3.14159)
S_{11} and S_{12}	Input S-parameters
S_{22} and S_{21}	Output S-parameters
C_{BE}	Base-emitter junction depletion region capacitance
C_{BC}	Base-collector junction depletion region capacitance
$C_{\mathrm{BC,E}}$	Extrinsic base-collector capacitance
$C_{\mathrm{BC,I}}$	Intrinsic base-collector capacitance
r_{E}	Dynamic emitter resistance
R_{EE}	Static emitter resistance
R_{C}	Collector series resistance
R_{B}	Base resistance
$R_{\mathrm{B,E}}$	Extrinsic base resistance
$R_{\mathrm{B,I}}$	Intrinsic base resistance
$R_{\mathrm{SH,B}}$	Base sheet resistance
R_{GAP}	Base access resistance
$R_{\mathrm{B,M}}$	Base metal resistance
$R_{\mathrm{B,C}}$	Base contact resistance
$\rho_{\mathrm{B,C}}$	Base contact resistivity
$\rho_{\mathrm{B,C}}$	Collector contact resistivity

N_{B}	Base doping
$N_{\mathrm{B,AV}}$	Average base doping
μ_{n}	Electron mobility
D_{n}	Electron diffusivity
v_{B}	Electron velocity at the base-collector heterointerface
ξ_{B}	Quasi-electric field
E_{C}	Energy at the bottom edge of the conduction band
ΔE_{C}	Difference in conduction band energies at a heterojunction
E_{V}	Energy at the top edge of the valence band
ΔE_{V}	Difference in valence band energies at a heterojunction
E_{G}	Bandgap energy
$\Delta E_{\Gamma\mathrm{L}}$	Energy separation for the Γ- and L-valleys

Curriculum Vitae

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List of Publications

Journal Articles

M. Alexandrova, R. Flückiger, R. Lövblom, O. Ostinelli, C. R. Bolognesi, "GaAsSb-based DHBTs with a reduced base access distance and $f_{\mathrm{T}}/f_{\mathrm{MAX}} = 503/780$ GHz," *Electron Device Letters, IEEE*, vol. 35, no. 5, pp. 602-604, 2014.

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