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Author(s):
Ziemann, Thomas; Grossner, Ulrike; Neuenschwander, Jürg

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Power Cycling of Commercial SiC MOSFETs

Thomas Ziemann
and Ulrike Grossner
Advanced Power Semiconductor Laboratory
ETH Zurich
Zürich, Switzerland
ziemann@aps.ee.ethz.ch

Jürg Neuenschwander
Swiss Laboratories
for Materials Science
and Technology
Dübendorf, Switzerland

***Abstract*—The robustness under power cycling of three comparable silicon carbide MOSFETs in TO-247 packages from three different manufacturers is investigated, with silicon IGBTs serving as reference. The power cycling method, especially the junction temperature measurement and best practices to ensure its accuracy, is described. The results give insight into reliability and variability as well as aging behavior and failure modes. We find a large variability between samples, both in initial characteristics and measured cycling lifetime, as well as signs of semiconductor device degradation. There is a significant spread in the extent of the variability, in the average and minimum observed lifetime, as well as in the failure mode. Some samples fail quickly due to bond wire defects, some due to semiconductor degradation, while others show very long lifetimes.**

I. Introduction

Silicon carbide (SiC) MOSFETs are pushing onto the market as a replacement of silicon IGBTs due to their favorable performance characteristics [1], [2]. Very low switching losses enable both highly efficient and highly compact converters. Smaller filters and cooling systems can present significant advantages, decreasing system cost and opening up new applications. Most of the manufacturers on the market deliver their SiC MOSFETs in standard TO-247 packages [3]–[6]. This package is small, low-cost and offers a lot of flexibility to the system designer, as individual devices can be arranged in any circuit. These are significant advantages over large modules.

However, performance and cost are only two of the parameters which are of interest for most applications, as reliability is very important as well. In many fields, guaranteed high reliability is a prerequisite for a new technology even to be considered, including markets such as automotive, rail transport or aerospace. In these fields, any failure can carry severe consequences, whether it is caused by the typical package failure mechanisms of bond wire liftoff and die attach degradation [7] or by aging of the semiconductor itself. Thus, knowledge on the reliability of SiC MOSFETs is crucial to enable wider use of the technology and to prevent failures in the field.

The behavior of the material and the MOSFET structure under normal operation as well as avalanche and short circuit condition are currently subject of numerous studies [8]–[10], but the behavior under repetitive and constant stress is still not fully understood. This subject is complex due to numerous influences coming from imperfections in the base material, issues in manufacturing of the die, as well as the package. Due to the different thermo-mechanical properties of the semiconductor material compared to silicon, SiC MOSFETs are also expected to behave differently on the package level [11].

Power cycling is a standard reliability test valued for its relevance for many applications and best reflects the real use of SiC devices. Therefore, power cycle testing of TO-247-packaged SiC MOSFETs can deliver important information for device and packaging engineers as well as system designers.

There is little publicly available information on power cycle testing done for TO-247 packages in general and even less on SiC MOSFETs in TO-packages. The limited work which has been published on power cycling of silicon dies in TO-247 packages [12] is not applicable to SiC, as the dies are much smaller. Package thermal testing without electrical operation of the device has been conducted [13], [14], but cannot be expected to activate the same failure mechanisms as real operation. Other cycling tests used repetitive high voltage switching without current and heating [14], which is also less representative of real applications than power cycling. Previous works on power cycling of SiC discretes do not disclose the test conditions such as cycle length and temperature swings [15], or claim that electrical determination of junction temperature is not possible for SiC [16]. Most packaging reliability research has focused on DCB-based and silicone-filled module packages, both for silicon IGBTs [7], [17] and SiC MOSFETs [18]. Modules offer many advantages, but have not been able to completely displace leadframe-based and epoxy-molded TO packages. The TO-247 package is still very widely used, even in demanding applications such as electric vehicle traction inverters [19].

To fill this gap, this work describes package-level testing in the form of power cycling to simulate realistic operating conditions of TO-247 packaged SiC MOSFETs. In the first section, the method employed will be described, supporting future power cycling investigations or thermal measurements. The second part deals with the reliability of the devices, focusing on the number of cycles the devices can withstand and the amount of variability between samples. Third, the findings on aging behavior and probable causes for the observed failures are discussed.

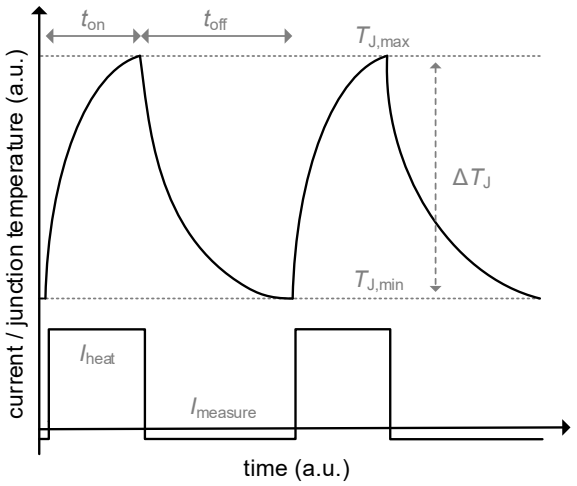

Fig. 1. Top: Typical temperature progression during power cycling, indicating timing and temperature definitions. Bottom: typical current waveform employed for this cycling profile, showing high heating current and small negative measurement current. The gate-source voltage follows the same pattern as the current.

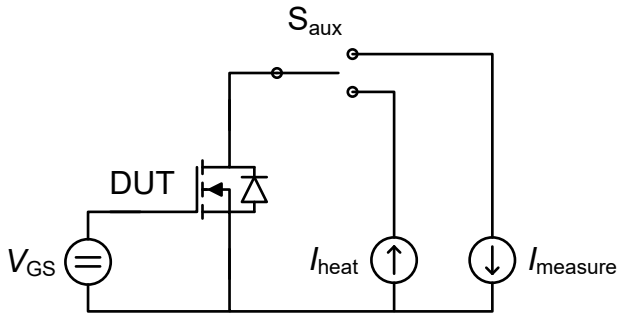

Fig. 2. Simplified test circuit for power cycling. For off-state V_{GS} is zero or negative and I_{measure} is connected; for on-state V_{GS} is positive and I_{heat} is connected.

II. Test Method

In a power cycling (PC) test the device is heated repeatedly by conducting a predetermined current in the on-state and then left to cool in the off-state, as illustrated in Fig. 1. This replicates the conditions encountered in many applications, such as an electric vehicle accelerating with high power, followed by a period of constant speed. The repeated heating and cooling cause expansion and contraction of all materials in the package, leading to thermo-mechanical stress between the materials. Accordingly, PC exposes the die to electrical, thermal and mechanical stress.

A suitable test circuit with a heating current source, measurement current source and gate voltage source is depicted in Fig. 2. The gate voltage source switches the DUT by applying bias for on-state and off-state. Auxiliary switches apply either heating or measurement current to the device.

A. Temperature measurement

For a power cycling test, it is necessary to know the junction temperature (T_{J}), as the junction temperature delta (ΔT_{J}) and the absolute junction temperature are the most important parameters influencing device lifetime [7], [17]. The measurement of the junction temperature should be done electrically without modifications to the device, requiring a stable thermo-sensitive electrical parameter (TSEP) that can be measured to determine the temperature. For IGBTs, the collector-emitter saturation voltage at a small, constant measurement current is used, which is approximately linearly dependent on temperature. In MOSFETs a similar method would be conceivable, as the on-resistance $R_{\mathrm{DS(on)}}$ is highly dependent on temperature [20]–[22]. However, the very low typical $R_{\mathrm{DS(on)}}$ and the absence of a knee voltage lead to very small signals at acceptably low measurement currents. While it would be possible to get a stronger response by significantly decreasing the gate-source voltage, this would result in an operating regime where variations of V_{GS} not only influence V_{DS}, but also change its temperature coefficient. In addition, there is evidence of threshold voltage shifting in response to gate bias [23], which also influences V_{DS}. V_{th} also shows a temperature dependence, but is not used as a TSEP either, to eliminate possible influence from threshold voltage shifting.

When a negative measurement current is applied the forward voltage of the body diode can be monitored, which also shows a temperature dependence. In contrast to the channel, the body diode has a knee voltage, giving a strong signal even with low currents. For these reasons, the body diode method is chosen for measurement of the junction temperature in this work. As degradation of the body diode cannot be ruled out, recalibration during the testing is done to monitor possible parameter shift. Further, an influence of the gate voltage is suspected, as the third quadrant of the output characteristic of all of the DUTs shows a difference between zero gate bias and negative gate bias. At zero gate bias, the channel of these devices is not completely off and the measured signal thus does not purely come from the body diode. To test this, cycling is run with both zero and negative gate bias. Negative bias will close the channel completely and give a signal free from channel influence, eliminating any related effects such as threshold voltage shift.

B. Heating

With the body diode selected for temperature measurement, the heating strategy also has to be chosen. The first option is applying positive current and positive gate bias to the channel, leading to losses determined by $R_{\mathrm{DS(on)}}$ and I_{D}^2, which rise significantly as the device heats up due to the positive temperature coefficient of $R_{\mathrm{DS(on)}}$. The other option is heating the body diode with a negative current and either zero or negative bias. The losses here are determined by V_{DS} and I_{D}, with the losses decreasing as the device heats up due to the negative temperature coefficient of the forward voltage. This would misrepresent the real behavior in an application with most losses occurring in forward operation, as channel

TABLE I
MANUFACTURER SPECIFICATIONS OF THE TESTED DEVICES

	Type A	Type B	Type C	Si IGBT
$V_{\mathrm{DS,max}}$				
$V_{\mathrm{CE,max}}$	1200 V	1200 V	1200 V	1200 V
$I_{\mathrm{D,100\,°C}}$	24 A	28 A	34 A	25 A
$R_{\mathrm{DS(on)}}$				
$V_{\mathrm{CE(sat)}}$	80 mΩ	80 mΩ	80 mΩ	1.7 V
$R_{\mathrm{th,JC}}$	0.6 K/W	0.44 K/W	0.65 K/W	0.65 K/W

heating causes accelerated aging. A degradation of the thermal path leads to higher temperatures and higher losses, which in turn causes even higher temperatures and faster degradation. For this reason, channel heating is selected as the more realistic and more demanding strategy.

C. Tested Devices

Three state-of-the-art types of SiC MOSFETs from the manufacturers Cree (C2M0080120D, [20]), Rohm (SCT2080KE, [21]) and ST Microelectronics (SCT30N120, [22]) are selected as devices under test (DUTs), all three rated for $V_{\mathrm{DS}} = 1200\,\mathrm{V}$ and $R_{\mathrm{DS(on)}} = 80\,\mathrm{m\Omega}$. These three types are from here on referred to as A, B and C, respectively. The identical rating shall serve to validate comparisons between the three types. Additionally, a standard silicon IGBT from Infineon (IGW25T120, [24]) is tested as reference, which was selected to have comparable on voltage class and current rating, as shown in Table I.

Two test campaigns are run, as summarized in TABLE II. Three samples of all types as well as the IGBTs are tested in the first set and 3 samples of all MOSFET types in the second. The sample count is low due to the long times necessary for the tests, so they do not allow quantitative statistical evaluation. They do, however, give a qualitative idea of the behavior which can be expected from SiC MOSFETs exposed to power cycles. Significant variation of the characteristics between devices of a single type has been observed [25], as shown for type A in Fig. 3. These variations are expected to result in somewhat different heating behavior and may also affect the test results.

D. Test conditions

Three samples of each type are tested at the same time, under the same conditions. They are mounted to a large cold plate with an electrically isolating thermal interface material and pressed down with equally torqued screws, as shown in Fig. 4. A relatively long cycle time is chosen, $t_{\mathrm{on}} = 5\,\mathrm{s}$ followed by $t_{\mathrm{off}} = 15\,\mathrm{s}$ for the first set of devices and $t_{\mathrm{off}} = 10\,\mathrm{s}$ for the second. These long times should allow the whole package to heat up and cool down, and do not limit the degradation to the bond wires. They also allow the use of currents close to the rated DC-current while still reaching the high temperatures desired. For the initial ΔT_{J}, a target value of 125 K, from 25 °C to 150 °C, is chosen, to emulate a demanding application and to accelerate the test. The current value is chosen per device type at the start of the test to reach the desired initial ΔT_{J}. t_{on}, t_{off}

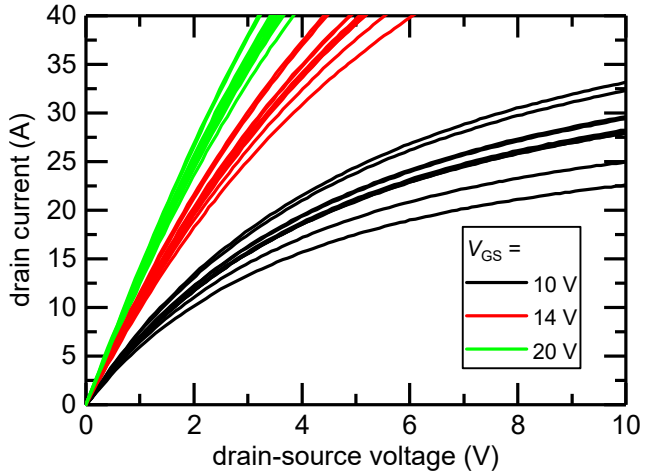

Fig. 3. Output curves of 10 devices of type A, showing variability of individual devices, measurements from [25].

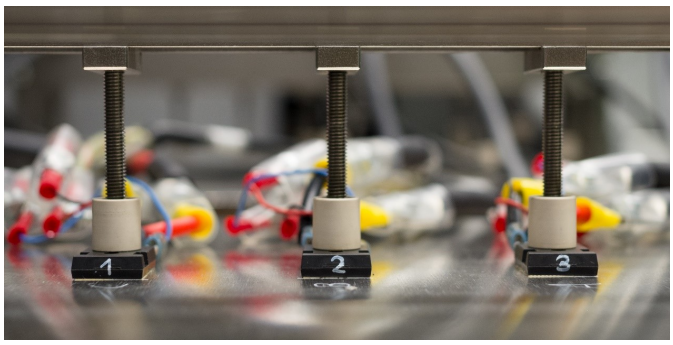

Fig. 4. Measurement setup with three DUTs mounted to the cold plate.

and current are kept constant during the test. Under identical conditions, device variations lead to differences in initial ΔT_{J} reached by each individual device, so the current is selected to achieve the desired temperature swing on average over the sample set. This reflects application use, where all devices would have to withstand the same conditions, independent of their individual characteristics. For the second set the off-period is shortened to decrease the test time. At the same time, the thermal interface material is changed to a type with lower thermal resistance to improve R_{th} measurement, necessitating higher currents to reach the same ΔT_{J}. In addition, negative gate bias as recommended by the manufacturer is used for the second set.

E. Equipment

The test equipment used is a MicReD Industrial Power Tester 1500A, which performs heating, temperature measurement and calibration. Regular measurements of Z_{th} can be conducted automatically without removal of the DUT. Three devices can be tested at a time. The cold plate is kept at a constant temperature by an external thermostat, which also allows calibration up to 150 °C without removal of the devices. The equipment can monitor device temperatures and voltages during

TABLE II
CYCLING CONDITIONS FOR ALL TESTED SAMPLES

Samples	ΔT_{J} (K)	t_{on} (s)	t_{off} (s)	I_{D} (A)
A 1-3	125	5	15	22
B 1-3	125	5	15	22.9
C 1-3	125	5	15	28.5
IGBT 1-3	125	5	15	25
A 4-6	125	5	10	26.7
B 4-6	125	5	10	26
C 4-6	125	5	10	34

the test, allowing the test to be stopped when failure criteria are reached. It does not allow direct measurement of the $R_{\mathrm{DS(on)}}$ and failure cannot be defined based on this parameter.

F. Failure criteria

The primary failure criterion is $20\,\%$ increase of ΔT_{J}, as used in previous works [26]. Junction temperature above $175\,^{\circ}\mathrm{C}$ or reaching the limits of the heating voltage due to strong ($20\,\%$) increase of $R_{\mathrm{DS(on)}}$ are also considered to determine failure.

G. Tests and Measurements

In addition to the continuous monitoring of electrical and thermal parameters during the test and Z_{th}-measurements every 500 cycles, detailed characterization of devices is carried out before and after testing. This includes I-V-measurements (channel, body diode, threshold voltage, leakage currents and breakdown voltage) as well as C-V curves for examination of the MOS-interfaces. Non-destructive imaging with ultrasound and X-ray is also conducted to investigate package failure modes. Due to the multitude of results for all samples, only a selection are displayed as figures.

III. RESULTS

The investigation yielded results in several areas, firstly concerning the methodology, secondly about the reliability and variability of the compared devices, and third about observed aging behavior and failure modes.

A. Measurement methodology

1) Body diode spread between devices: In order to validate the junction temperature measurement method via the body diode, calibration curves are recorded for each individual device and calibration is repeated during the cycling test. The results show that, for all manufacturers, there is significant variation in body diode forward voltage between devices. The extent of the spread varies between types, visible in Fig. 5.

Type C shows the widest spread, with the same measured voltage corresponding to temperatures differing by almost $100\,\mathrm{K}$. For all types, however, significant temperature errors would result if calibration was carried out with one sample per type. This behavior is present both with negative gate bias, as shown by example of type A in Fig. 5a, and zero gate bias, shown for type B and C in Fig. 5b and Fig. 5c. This result suggests, that sample specific calibration is necessary for any power cycling or Z_{th}-measurement.

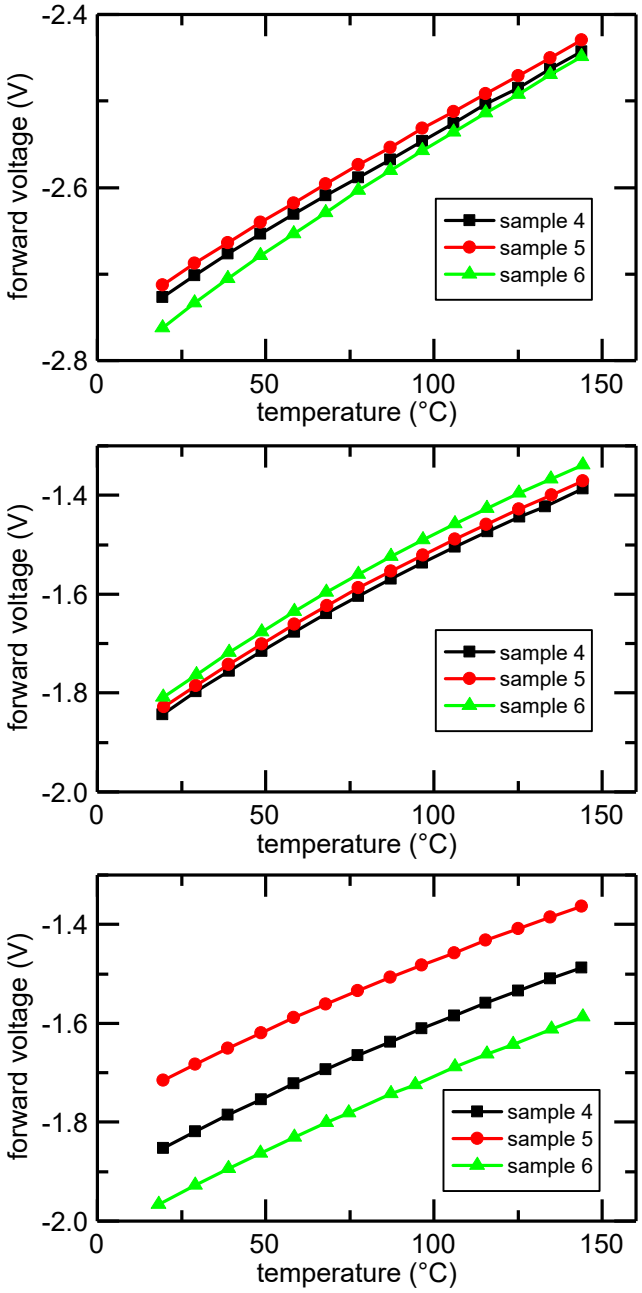

Fig. 5. Calibration curves of body diode forward voltage over temperature, showing variation between devices. Top: (a) type A, here with negative gate bias, middle: (b) type B, bottom: (c) type C, both with zero gate voltage.

2) Body diode aging: To account for possible body diode aging during the power cycling process, the calibration is repeated periodically in increasing intervals. It is observed that the calibration curve is often shifted after the first cycling interval, but that all further cycling does not have a marked influence. The measured curves are displayed in Fig. 6.

For brevity, not all combinations of gate voltage and type are included here. Type A, shown as an example of negative gate bias, does not exhibit any degradation, while type B and C, here as examples of zero bias, display moderate to strong

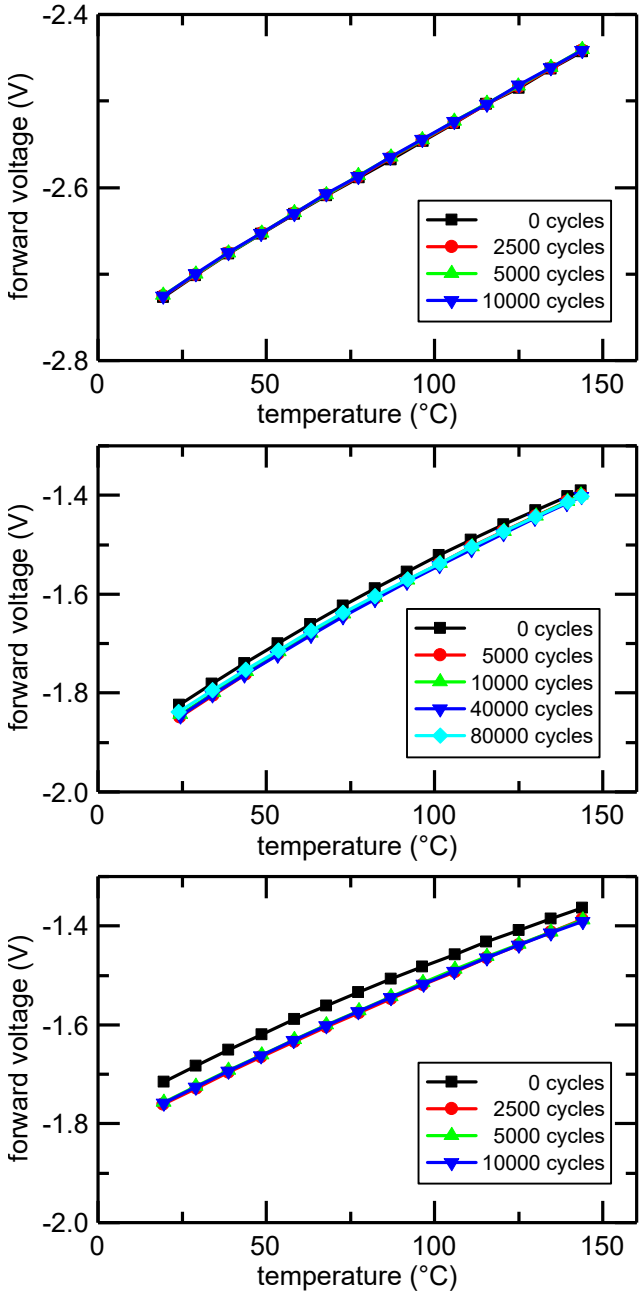

Fig. 6. Calibration curves of body diode forward voltage over temperature for one sample per type. Top: (a) type A, here with negative gate bias, middle: (b) type B, bottom: (c) type C, both with zero gate voltage.

degradation respectively. All types experienced aging with zero gate bias, but to varying degrees. The shift is always too strong for reliable measurements with only initial calibration. With negative gate bias the aging is much lower (type B and C) or nonexistent (type A), with the potential temperature error reduced significantly in all cases. The negative bias was chosen from the manufacturer recommendations and for some types, an even lower voltage is necessary to completely close the channel. The results suggest that a sufficient negative gate bias eliminates the observed aging behavior. Threshold voltage shift is a possible cause for channel-related parameter shift.

3) Transient temperature measurement error: It has been reported in [18] that the body diode temperature measurement method is susceptible to errors immediately after heating pulses, unless a negative gate bias is employed. The behavior was originally observed with large modules and is replicated with the test equipment used in this work for a different SiC power module. However, the issue can not clearly be seen in the small discrete devices investigated in this study.

B. Reliability and variability

From the initial characterization it is obvious that even with the small number of samples tested, there is significant variability between the tested MOSFETs of the same type. Variations in $R_{\mathrm{DS(on)}}$ translate into different heating power at the same current level, which is chosen to achieve the goal of 125 K initial ΔT_{J} on average for every type. The number of cycles to failure can also significantly vary between devices, as shown by the ΔT_{J} curves in Fig. 7.

Comparing the three different types, it can be noted that the observed lifetimes and also the spread within the sample set varies greatly, as listed in Table
reftab:results. The six devices of type A withstood between 8,000 and 200,000 cycles, showing significant variability (factor 25). The lowest cycle number is seen in the second set, which was run at higher currents, while the highest number is from a device in the first set, which did not fail until the test was stopped. The two groups of Type B delivered much more consistent and higher cycle numbers of 74,000-81,000 for the first three and 28,000-40,000 for the second group. Type C proved to be even more variable than type A with the first group coming in between 2,000 and 140,000, and the second group between 21,000 and 55,000. The low extreme of only 2000 cycles would present a significant problem for many applications. Only part of this large variation can be explained by differences in $R_{\mathrm{DS(on)}}$ leading to different ΔT_{J}, the impact of which is described for Si IGBTs in [7]. From this study, the measured 32 % difference in ΔT_{J} is expected to lead to a factor of 3.4 difference in lifetime, compared to a factor of 70 as observed. For comparison, the factor between extreme devices is 3.1 for type A and 2.9 for type B.

The silicon IGBTs tested for comparison under the same conditions as the first set of devices reached 200,000 cycles without signs of degradation in any of the three samples, whereupon cycling was ended.

C. Aging behavior and failure modes

From the ΔT_{J}-curves in Fig. 7, as well as other electrical and thermal parameters monitored during the test, it seems the aging behavior and the failure mode which caused the DUT to be classified as failed are highly variable, again both between types and devices.

1) Type A: Samples 4-6 of type A exhibit significant, instantaneous increases in the ΔT_{J}-curves (Fig. 7a), with the third one occurring at or just before failure. In devices 5 and 6 the magnitude of the step increases progressively. Liftoff

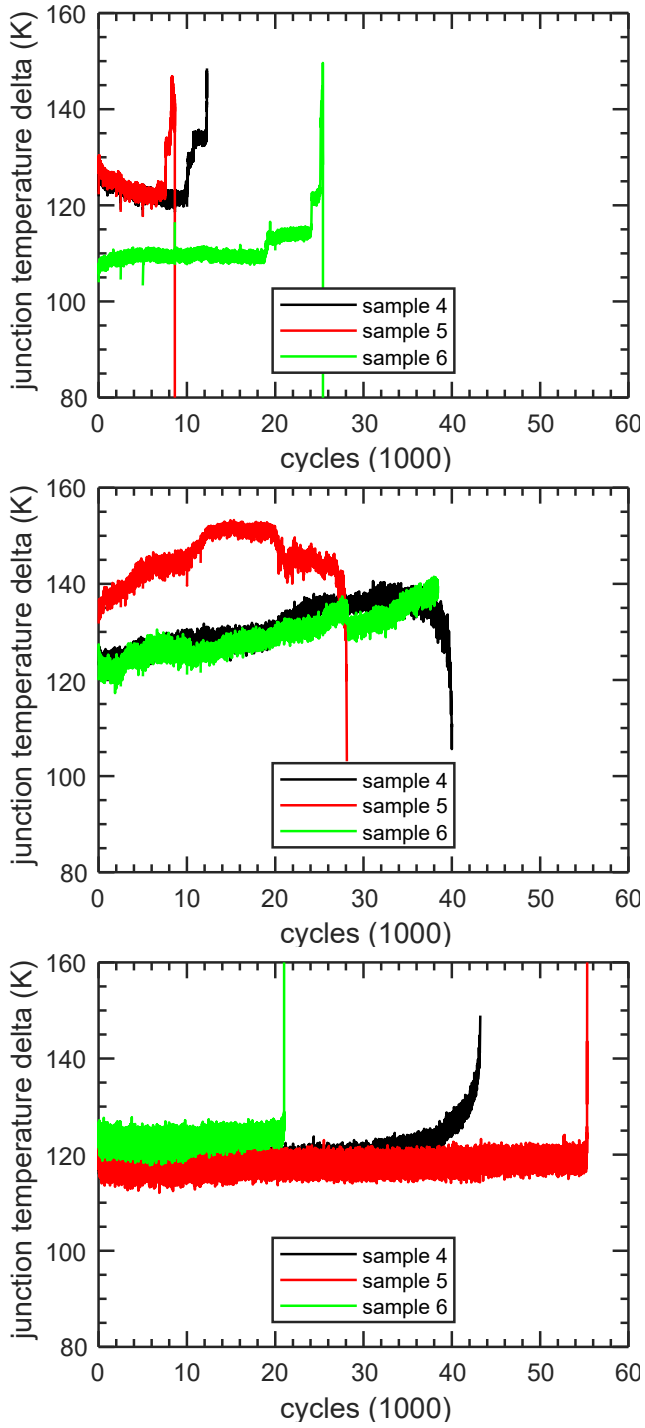

Fig. 7. Junction temperature delta over the lifetime of (a) type A (top), (b) type B (middle) and (c) type C (bottom), showing the variability and different failure modes observed.

or crack of a source wire-bond causes more current to be concentrated in the remaining wires, instantly leading to more heating. As the remaining number of bond wires decreases, the impact of a failed wire increases, leading to increasingly more heating until the remaining bond wires cannot manage the current any more. The behavior observed is thus consistent with

TABLE III
LIST OF SAMPLES WITH CYCLE NUMBER AND OBSERVED DEGRADATION

Device	Cycles tested	Degradation observed
A1	200000	No failure, test stopped
A2	63696	Reversible R_{DS} increase
A3	59293	Reversible R_{DS} increase
A4	12267	Bond wire failure
A5	8638	Bond wire failure
A6	25399	Bond wire failure
B1	81009	R_{DS} increase
B2	74174	R_{DS} increase
B3	75234	R_{DS} increase
B4	40004	R_{DS} increase
B5	38438	R_{DS} increase, gate failure
B6	28111	R_{DS} increase, gate failure
C1	10043	Reversible R_{DS} increase
C2	2001	Reversible R_{DS} increase
C3	140042	Reversible R_{DS} increase
C4	43216	Reversible R_{DS} increase
C5	55313	Reversible R_{DS} increase
C6	21002	Reversible R_{DS} increase

bond wire failure of the six source bond wires present in this device, a packaging problem that may be caused by underlying issues in bonding or stress exerted by the molding compound. Ultrasonic imaging seen in Fig. 8 shows delamination on top of the die and strong echoes in the area of the bond wires, confirming this diagnosis.

The post-failure I-V characterization shows an increase of $R_{\mathrm{DS(on)}}$ to more than $1\,\Omega$ for samples 5 and 6 (Fig. 9a), while sample 4 exhibits an increase of only $7\,\%$ compared to the initial characterization. It appears that a very large resistance is now in series with the die, and, as a result, the ΔT_{J} decreases to a very low value, since the heating source cannot maintain the desired current. The breakdown voltage and gate-source leakage seem to be unaffected, with a slight decrease of gate threshold voltage. This suggests no significant aging of the semiconductor structure and failure due to package degradation.

2) Type B: The devices of type B show a noticeably different behavior, with seemingly random fluctuations and no visible steps in the ΔT_{J}-curve shown in Fig. 7b. All devices initially show slow increase of temperature delta, consistent with either an increase of $R_{\mathrm{DS(on)}}$ due to die degradation or an increase of R_{th} due to degradation of the thermal path. However, neither R_{th}-measurements nor ultrasonic imaging (Fig. 8) found damage to the solder layer. For sample 5, which experienced larger temperature swings, the upward trend reverses after 20,000 cycles, with the device increasing in resistance until failure occurs, marked by a steep drop of ΔT_{J}. The failure behavior is similar for sample 4, with a longer lifetime due to lower temperature swings. Sample 6 does not show decreasing ΔT_{J}, it is deemed failed due to elevated voltage, temperature, and temperature delta.

The I-V characterization after the test reveals completely changed electrical parameters, shown for sample 5 in Fig. 9b.

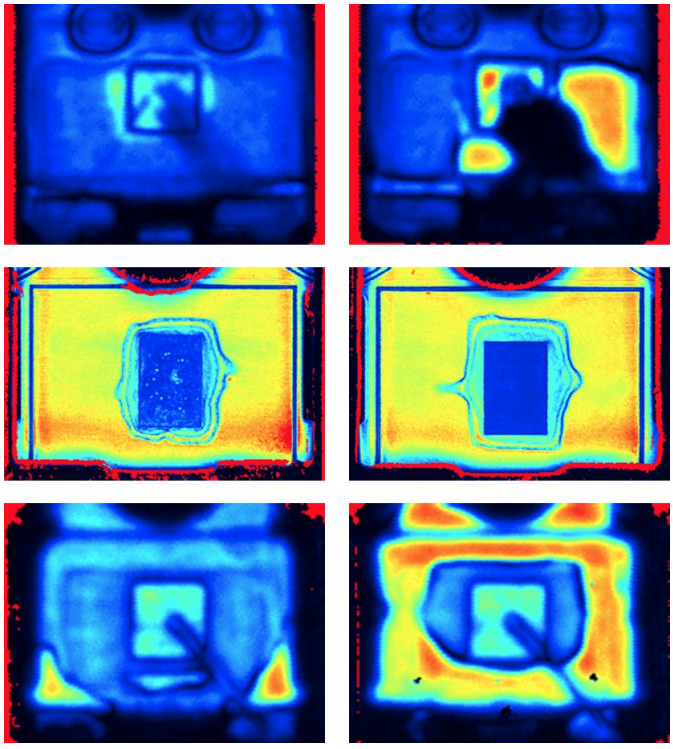

Fig. 8. Ultrasonic images of new samples (left) and cycled samples (right). Top: faults in epoxy around bond wires found in type A. Middle: undamaged solder layer as found in all types, here for type B. Bottom: delamination at copper/epoxy interface as seen in many samples, here for type C

Not only is the $R_{\mathrm{DS(on)}}$ strongly increased, but there is also severe gate-source leakage, sample 4 and 5 showing ohmic behavior with gate-source resistances of $100\,\Omega$ and $69\,\Omega$ respectively. This translates to $260\,\mathrm{mA}$ gate current at nominal bias. These are the only devices showing a marked change in C-V measurements, with decreased C_{GS} at all gate voltages.

The blocking behavior is also compromised, with the drain-source breakdown voltage ($I_{\mathrm{D}} = 1\,\mathrm{mA}$) decreasing significantly. Before PC, the breakdown voltage is above $2500\,\mathrm{V}$, more than twice the nominal voltage of $1200\,\mathrm{V}$. After PC, it is reduced to just above, and in one sample significantly below the nominal voltage. The gate threshold voltage at low currents is not strongly affected, with small increases of around $10\,\%$ or $0.2\,\mathrm{V}$ recorded for all devices. For high currents, the transfer curves also show the effect of increased $R_{\mathrm{DS(on)}}$ in affected devices.

Looking at the number of cycles to failure reveals that the first set shows $50\,\%$ shorter lifetime than the second, with the same ΔT_{J} and only $13.5\,\%$ higher current. Using the CIPS2008 algorithm, which considers current influence on bond wire degradation, $13.5\,\%$ more current correspond to $8.7\,\%$ shorter lifetime [7]. This may be an indication that the failure mode is strongly influenced by current, much more so than could be expected from studies on silicon IGBT package degradation. Overall it appears that these devices degrade severely on the semiconductor level while the package is relatively stable.

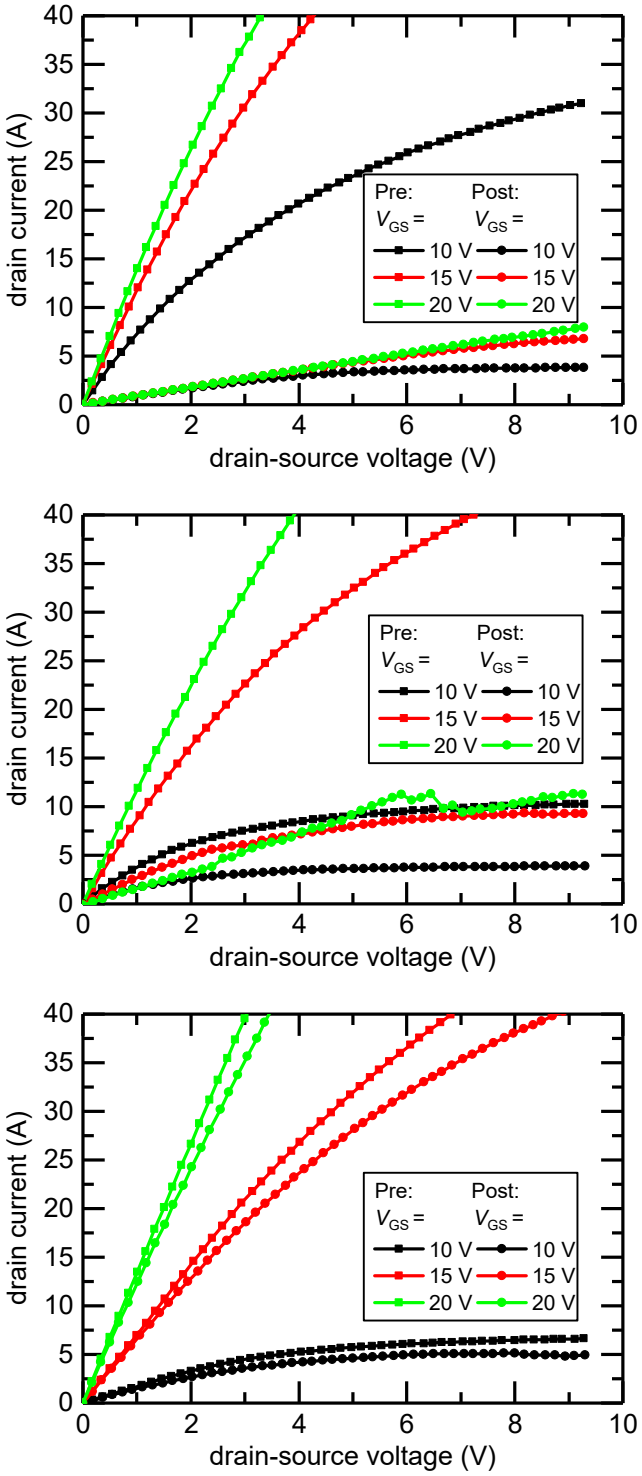

Fig. 9. Output curves showing drain current in dependence of drain-source voltage at three gate-source voltages, measured before and after cycling. (a) Type A at top, (b) type B in the middle, (c) type C at bottom.

3) Type C: Type C again shows different results, see Fig. 7c. These devices are closer to the expectation of a relatively constant ΔT_{J}, with two samples then failing rapidly and one more slowly by increasing ΔT_{J} until the failure criterion

is met. These devices also consistently show a permanent increase of $R_{\mathrm{DS(on)}}$ around $10\,\%$ (Fig. 9c), with no significant deviation visible in breakdown voltage or gate-source leakage and only minor increases of gate threshold voltage. As R_{th}-measurements indicate no degradation of the thermal path and ultrasonic imaging shows severe epoxy delamination but no damage to the die attach, the observed aging and failures cannot be explained consistently. The cause may be related to reversible degradation, which is not captured by the post-cycling measurements.

IV. Conclusion

This work shows that power cycling using the body diode to determine junction temperature is a viable method to investigate the aging behavior and reliability of SiC MOSFETs. The tests can be run on commercially available standard equipment with no changes to the hardware, only to the methodology. Long test times lead to low sample numbers which do not allow statistical evaluation, but nevertheless give a useful insight into the behavior of TO-packaged SiC MOSFETs under power cycling. Variability and initial degradation present problems which can be solved by individual calibration and the use of a negative gate bias. The result of this comparative investigation is that type A showed a packaging problem in many devices and relatively short median lifetime, but also the longest lifetime; type B reached the highest median and highest minimum cycle numbers before failing due to die degradation, while type C showed the strongest variability and the shortest lived samples.

All three types of MOSFETs showed degradation of the MOSFET die itself, specifically increased $R_{\mathrm{DS(on)}}$, leakage currents and decreased breakdown voltage, up to complete failure in type B. R_{th}-measurements and ultrasonic imaging found no degradation of the solder layer, in most devices the package aging was limited to epoxy delamination. A high degree of variability between samples of the same type was also found, both in initial characteristics and lifetime. All of these shortcomings show that SiC MOSFETs are not as mature as Si IGBTs. For the reference IGBTs, no degradation could be observed until the test was stopped at 200,000 cycles. The TO-packaging employed also seems to have potential for improvement, as shown by bond wire failures at low cycle numbers and widespread epoxy delamination, which could enable moisture ingress. Nevertheless, the SiC MOSFET technology has great potential, as 200,000 cycles with no degradation can be reached (see sample A1). While the variability is a problem for applications, this device shows that there is no systematic issue preventing SiC MOSFETs from reaching high reliability. Further investigation of the degradation mechanisms encountered should enable improvements leading to consistently high reliability in the future.

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