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Solid-State Modulator for Generating High Voltage Pulses in the ms-Range with High Output Power

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Abstract

Novel basic research, which will be carried out with the help of particle accelerator experiments at the new European Spallation Source (ESS) in Sweden, requires high-frequency amplifiers (klystrons), which are excited by high-precision high-voltage pulses. These highly accurate voltage pulses are generated by means of so-called long-pulse modulators. The aim of this thesis is to investigate novel modular long pulse sources with a focus on an easily expandable and compact design with the highest possible efficiency. The proposed pulse source has to generate a voltage pulse with a pulse voltage amplitude of 115 kV with a repetition rate of 14 Hz and a pulse power of 2.88 MW during a pulse length of 3.5 ms.

With existing modulator topologies all the demanding requirements like a fast pulse rise time, a low voltage ripple and a long pulse length can hardly be satisfied at the same time in a compact way. For example, conventional concepts which are employing pulse transformers become huge for long pulses since the volt-seconds product of the pulse is high. Therefore, the proposed modulator concept is based on a series parallel resonant converter (SPRC) topology, which avoids this drawback as the transformer is operated at high frequencies. This modular topology employs SPRC base modules (SPRC-Bms), which are connected in series to gain the given output voltage and are connected in parallel to deliver the output power. The single SPRC-Bm consists of a H-bridge, a resonant tank, a high-voltage high-frequency transformer and an output rectifier. In order to derive the highest efficiency along with a compact modulator system size, as well as to fulfill the demanding pulse specifications, an optimization procedure has been developed. This procedure contains a detailed electrical model of the resonant circuit and a thermal model of the semiconductors for an optimal number of semiconductors. Since one major key component of the modulator is the design of the high-frequency high-voltage transformers, the optimization procedure also includes a generalized calculation method for the leakage, the parasitic capacitance and all high frequency losses of the transformer. To ensure a long lifetime of the transformer, a com-

prehensive isolation design method and a detailed thermal model of the transformer is introduced. For an accurate temperature estimation a novel thermal resistance, which can be used either for solid or litz wire windings, has been derived. All models of the optimization routine are validated by measurements, which are in good accordance with the proposed models. The resulting modulator system consists of 18 modules in total, which are operated interleaved to reduce the voltage ripple to a minimum. In order to employ off-the-shelf 650 V breakdown voltage semiconductor switches for the H-bridges, two SPRC-Bms are connected in series at the input and in parallel at the output forming a stack. Nine of these stacks are then connected in series to generate the required output voltage.
Another key component is the investigation of a proper control system, which guarantees an equal output voltage sharing, respectively a balanced power sharing of the SPRC-Bms due to component tolerances of the resonant tanks. In addition, the control system has to compensate the input voltage droop due to the high power consumption during the pulse. Two suitable control methods have been presented and have been verified by measurements and simulations.
In conclusion, in this thesis a long pulse modulator system has been designed and has been verified by measurements at a full scale prototype, which is operated under nominal conditions. The finally presented modulator system is capable to fulfill all the given ESS modulator specifications with an achieved overall electrical system efficiency of 91.9 %.

Kurzfassung

Die mit Hilfe von Teilchenbeschleunigern an der europäischen Spallationsquelle (ESS) in Schweden durchgeführte neuartige Grundlagenforschung erfordert Hochfrequenzverstärker (Klystrons), die durch hochpräzise Hochspannungsimpulse angeregt werden. Diese hoch genauen Spannungsimpulse werden mittels sogenannter Langpulsmodulatoren erzeugt. Das Ziel dieser Arbeit ist die Untersuchung neuer modularer Langpulsquellen, mit dem Fokus auf ein leicht erweiterbares und kompaktes Design, sowie die Erreichung der höchstmöglichsten Effizienz. Die vorgeschlagene Pulsquelle muss einen 3.5 ms langen Spannungsimpuls mit einer Impulsspannungsamplitude von 115 kV, einer Wiederholungsrate von 14 Hz und einer Impulsleistung von 2.88 MW, erzeugen.
Mit bestehenden Modulatortopologien können anspruchsvolle Anforderungen wie eine schnelle Pulsanstiegszeit, eine geringe Spannungswelligkeit und eine grosse Pulslänge bei gleichzeitiger kompakter Bauweise, kaum erreicht werden. Herkömmliche Konzepte, die beispielsweise Pulstransformatoren verwenden, werden durch das hohe Spannungs-Zeit-Produkt des Impulses sehr gross für lange Impulse. Das vorgeschlagene Modulatorkonzept basiert auf einer Serien-Parallel-Resonanz-Konverter (SPRC) Topologie, die diesen Nachteil vermeidet, da der Transformator bei hohen Frequenzen betrieben wird. Diese modulare Topologie besteht aus SPRC-Basismodulen (SPRC-Bms), die um die gegebene Ausgangsspannung zu erreichen miteinander in Reihe geschaltet sind und um die geforderte Ausgangsleistung zu liefern in parallel geschaltet sind.
Das einzelne SPRC-Bm setzt sich aus einer H-Brücke, einem Resonanzkreis, einem Hochspannungs-Hochfrequenztransformator und einem Ausgangsgleichrichter zusammen. Ein Optimierungsverfahren wurde entwickelt um die maximale Effizienz zusammen mit einer kompakten Modulatorbaugrösse zu erreichen, wobei alle Pulsspezifikationen eingehalten werden. Dieses Verfahren enthält ein detailliertes elektrisches Modell des Resonanzkreises und ein thermisches Modell der Halbleiter, womit die optimale Anzahl an Halbleitern bestimmt werden kann. Eine wichtige Schlüsselkomponente des Modulators ist das Design der Hochfrequenz-Hochspannungstransformatoren. Die Opti-

mierungsroutine beinhaltet allgemeine Berechnungsmethoden für die Streuinduktivität, die parasitäre Kapazität und die Hochfrequenzverluste der Transformatoren. Um eine lange Lebensdauer des Transformators zu gewährleisten, wurde eine umfassende Methode für das Isolationsdesign konzipiert und ein detailliertes thermisches Modell des Transformators entwickelt.
Dieses Modell beinhaltet eine neue thermische Widerstandsbeschreibung von Rund- oder Litzendrahtwicklungen, welche eine relativ genaue Temperaturabschätzung ermöglichen. Alle Modelle der Optimierungsroutine wurden durch Messungen validiert und zeigen eine sehr gute Übereinstimmung mit den vorgeschlagenen Modellen. Das finale Modulatorsystem besteht aus insgesamt 18 Modulen die phasenverschoben betrieben werden, um die Spannungswelligkeit der Ausgangsspannung auf ein Minimum zu begrenzen.
Damit Standardhalbleiterschalter mit einer Durchbruchspannung von 650 V für die H-Brücken verwendet werden können, werden zwei SPRC-Bms am Eingang in Reihe und am Ausgang parallel geschaltet und bilden einen sogenannten Stapel. Um die benötigte Ausgangsspannung zu erreichen, werden neun dieser Stapel in Reihe geschaltet.
Eine weitere Schlüsselkomponente ist die Entwicklung eines Regelungskonzeptes, welches eine gleichmässige Ausgangsspannungs - bzw. Leistungsaufteilung der einzelnen SPRC-Bms garantiert. Ungleichmässige Aufteilungen können aufgrund der Bauteiltoleranzen der Resonanzkreiselemente in den einzelnen SPRC-Bms entstehen. Darüber hinaus muss das Regelungssystem den Eingangsspannungseinbruch kompensieren, der durch den hohen Leistungsbedarf während des Pulses entsteht. Zwei geeignete Regelungsmethoden werden vorgestellt und durch Messungen und Simulationen verifiziert. Zusammengefasst wird in dieser Arbeit ein Langpulsmodulatorsystem entwickelt und das Design und dessen Verhalten durch Messungen im Nennbetrieb überprüft und nachgewiesen. Das final präsentierte Modulatorsystem ist in der Lage alle angegebenen ESS-Modulatorspezifikationen zu erfüllen, wobei ein Gesamtsystemwirkungsgrad von 91.9 % erreicht wird.

Abbreviations

2D	...	Two Dimensional
3D	...	Three Dimensional
AC	...	Alternating Current
CICM	...	Core Image Charge Method
CSM	...	Charge Simulation Method
CSPI	...	Cooling System Performance Index
DC	...	Direct Current
DCM	...	Discontinuous Conduction Mode
DIL	...	Design Insulation Level
DTL	...	Drift Tube LINAC
DUT	...	Device Under Test
eFHA	...	extended First Harmonic Approximation
EMI	...	Electromagnetic Interferences
ESS	...	European Spallation Source
FEM	...	Finite Element Method
FET	...	Field Effect Transistor
FHA	...	First Harmonic Approximation
FMA	...	Fundamental Mode Approximation
HEBT	...	High Energy Beam Transport
HF	...	High Frequency
HV	...	High Voltage
ICS	...	Input Current Sharing
IGBT	...	Insulated Gate Bipolar Transistor
IOT	...	Inductive Output Tube
IPOS	...	Input Parallel Output Series
ISOP	...	Input Series Output Parallel
IVCU	...	Input Voltage Charging Unit
LEBT	...	Low Energy Beam Transport
LINAC	...	Linear Accelerator

MEBT	...	Medium Energy Beam Transport
MOSFET	...	Metal Oxide Field Effect Transistor
OP	...	Output Parallel
OS	...	Output Series
OVS	...	Output Voltage Sharing
PCB	...	Printed Circuit Board
PSM	...	Pulse Step Modulator
PWM	...	Pulse Width Modulation
RCFHA	...	Rectifier Compensated First Harmonic Approximation
RCFMA	...	Rectifier Compensated Fundamental Mode Analysis
RF	...	Radio Frequency
RFQ	...	Radio Frequency Quadrupole
RMS	...	Root Mean Square
SC	...	Superconducting
SPICE	...	Simulation Program with Integrated Circuit Emphasis
SPRC-Bm	...	Series Parallel Resonant Converter Basic module
tTEC	...	thermal T-Equivalent Circuit
ZCS	...	Zero Current Switching
ZVS	...	Zero Voltage Switching

Table of Contents

1 Introduction

In this thesis, a novel long pulse modulator system, which is used in the new European Spallation Source (ESS) is investigated, designed and verified by measurements on a full scale prototype. First ideas for ESS rises back in 1993 [1], but it lasts 17 years until the pre-construction of the ESS facility started in 2010. The final construction should be finished and under full operation until 2025 [2] in Lund, Sweden. ESS is a neutron beam source, which will host one of the most powerful linear accelerators (LINAC) ever built. Neutron science is used for the studies and investigations of new and smart materials e.g. in the fields of engineering materials, the chemistry of materials or to discover new magnetic and electronic phenomena. Due to the absence of charge, the neutrons have a relatively weak interaction with matter, which makes it possible to investigate condensed matter without damaging it [2]. Furthermore, its inherent magnetic moment can be used to study spin dynamics or the magnetic structure of matter [2]. However, such neu-

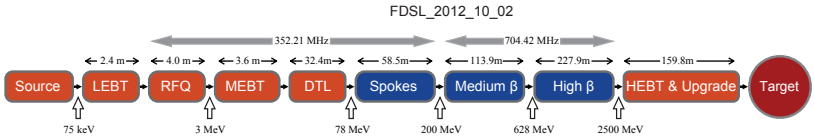


Figure 1.1: Block diagram of the ESS accelerator structure. A pulsed proton beam is created in the ion source, which is finally accelerated to a kinetic energy of 2.5 GeV. The orange blocks are normal conductive, while the blue blocks are superconducting. The target block is not part of the accelerator [2].

Table 1.1: High level accelerator parameters [2].

Parameter	Unit	Value
Energy	GeV	2.5
Current	mA	50
Pulse length	ms	2.86
Pulse repetition frequency	Hz	14
Average power	MW	5
Peak power	MW	125

tron beams are produced with the help of LINACs. The LINAC is one of the major parts of the ESS facility and will be explained in the following. The principle block diagram of the ESS LINAC is shown in Fig. 1.1. A pulsed proton beam is created in the ion source, which is finally accelerated to a kinetic energy of 2.5 GeV, with a repetition rate of 14 Hz and a pulse length of 2.86 ms resulting in an average beam power of 5 MW. The main high level accelerator parameters are summarized in Tab. 1.1. Afterwards, in the spallation process, the pulsed proton beam is collided with the tungsten target and neutron beams are emitted. These neutron beams are directed to the scientific instruments, which contains the material samples under investigation [3]. All blocks between the source and the target station (LEBT, RFQ, MEBT, DTL

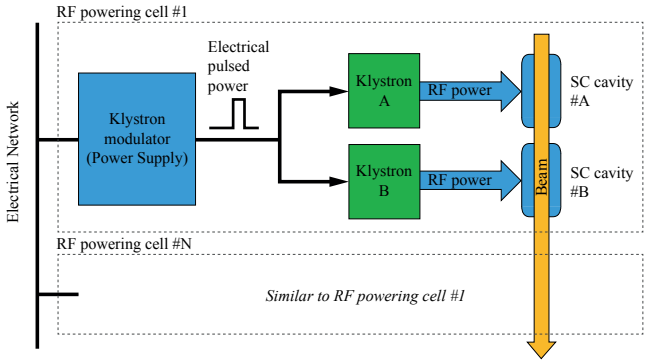


Figure 1.2: General powering scheme exemplary shown for the High-β block [2]. The klystrons provide the RF power for the SC cavities.

Table 1.2: Main klystron modulator specifications

Pulse voltage	V_K	$-115\,\mathrm{kV}$
Pulse current	I_K	$25\,\mathrm{A}$
Pulse power	P_K	$2.88\,\mathrm{MW}$
Pulse repetition rate	P_{RR}	$14\,\mathrm{Hz}$
Pulse width	T_P	$3.5\,\mathrm{ms}$
Pulse duty cycle	D	0.05
Pulse rise time (0..99 % of V_K)	t_{rise}	$150\,\mu\mathrm{s}$
Pulse fall time (100..10 % of V_K)	t_{fall}	$150\,\mu\mathrm{s}$
Short circuit energy	E_{arc}	$\leq 10\,\mathrm{J}$
Minimum efficiency	η	$\geq 90\,\%$

Spokes, Medium-β, High-β and HEBT & Upgrade) are used for bunching, focusing and acceleration of the beam. A detailed explanation of the before mentioned blocks is given in [2]. Due to the high peak power during the pulse, 98 % of the LINAC consists of super-conducting (SC) acceleration resonantors (cavities), which can be seen in Fig. 1.1 (blue blocks). The power for the acceleration cavities is provided by radio frequency (RF) sources called klystrons, which are operated at 352 MHz or 704 MHz. The general powering scheme for klystrons is demonstrated by showing the example of the High-β section in Fig. 1.2. The klystron pulse modulator, which is powered from the standard three phase AC low voltage grid, supplies the klystrons with a rectangular high voltage pulse. One pulse modulator should power at least two or more klystrons, whereas $\approx$ 130 klystron loads will be installed at the ESS facility side. Since the proton beam is a pulsed beam, the klystron modulators have to be operated pulsed as well. The modulator has to provide a 115 kV output voltage pulse with a rise and a fall time of lower than 150 µs and a pulse length of 3.5 ms. Furthermore, an efficiency of 90 % is of high demand. The main klystron modulator specifications are summarized in Tab. 1.2.
An overview of possible pulse generating topologies is presented in the following section.

1.1 Review of state of the art pulse modulators

In the literature, there exist many topologies to produce pulses in range of a few W to MW peak pulse power with a pulse length starting from the µs to the ms range pulse length. Following topologies, which are suitable candidates for the long pulse application are presented in the following.

- Direct switch topology
- Solid state Marx modulator
- Pulse transformer based
- Pulse step modulator topology
- Isolated DC-DC converter topologies

1.1.1 Direct switch topology

One of the simplest ways to produce a high voltage pulse is the direct or single switch topology. This is presented in Fig. 1.3 (a) [5, 6]. It shows a capacitor bank charged by a charging system to the desired output voltage. This voltage is then applied to the load R_L by turning on the high voltage switch. The HV-switch can be realized by a series connection of solid state based semiconductor switches, as for example IGBTs or FETs [7]. For providing a higher pulse energy, also arrays of series-parallel connected switches could be used [8]. The depicted snubber circuit limits the current in the case of an arcing and enables the HV-switch to interrupt the circuit before a critical arc energy is developed [6]. Due to the high power consumption, the capacitor bank is not able to keep the pulse flat top constant during the pulse. Therefore, Fig. 1.3 (b) shows a possible active droop [4] compensation, called LC-bouncer, where the bouncer capacitor C_B and the inductor form a resonant circuit. Starting at t_0, the HV-switch, as well as S_B are turned-off and the capacitor bank and C_B are initially charged by their sources to 150 kV and -35 kV, respectively. S_B is turned-on at t_1, which starts the resonant transition and discharges C_B through the inductor. The HV-switch is turned-on at t_2 and applies the pulse voltage to R_L. At t_3, the HV-switch is turned-off and disconnects the load from the capacitor bank. In order to compensate the droop of V_DC,

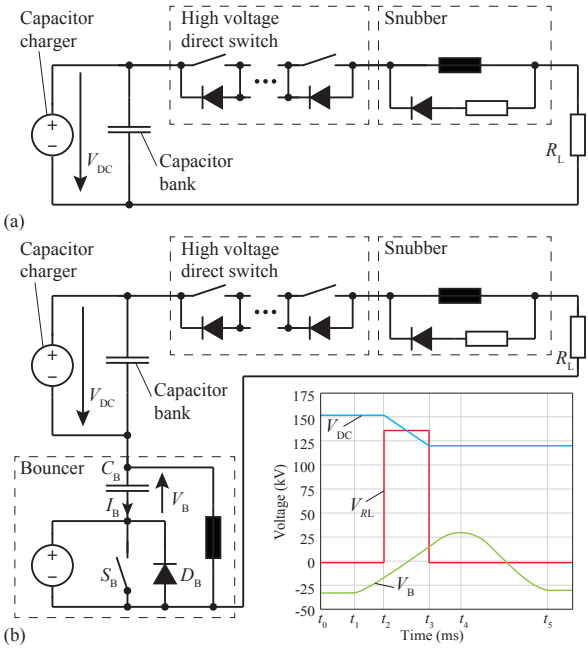


Figure 1.3: (a) Direct switch topology with snubber circuit. (b) Direct switch topology with snubber, active droop compensating LC-bouncer circuit and exemplary according voltage signals [4].

the bouncer is activated earlier, such as to be in the linear region of the discharging bouncer voltage, as can be seen in Fig. 1.3 (b). During the resonant swing back of the bouncer capacitor voltage V_B, namely at the maximum at t_4, the current I_B through C_B (not depicted in the signal diagram) crosses zero. Afterwards, I_B starts conducing through the bouncer diode D_B and recharges C_B nearly to its starting voltage. Therefore, the bouncer source just has to compensate the losses of the bouncer components before the next pulse is triggered. Finally, the bouncer switch S_B must be opened between t_4 and t_5 to prevent the start of a new resonant transition [9].

The advantages of this topology is the simple modular structure, which avoids a pulse transformer. The big disadvantage is the need of a high number of semiconductor switches for the HV-switch [10]. Since the HV-switch is in his simplest configuration a pure series connection of

semiconductor switches, there is the need of a proper voltage balancing across each switch for preventing over voltages. Hence, a supervision system and/or balancing circuits for all switches, which increases the complexity of the topology, has to be installed. Further, the main components such as the capacitor charger, the capacitor bank and the HV-switch have to isolate the full output voltage and therefore are placed in oil [9] to reduce the modulator size.

1.1.2 Solid state Marx modulator

The Marx topology [11–17] is a modular topology, where n Marx cells are connected in series dependent on the desired output voltage pulse, as can be seen in Fig. 1.4. This topology can be realized with air as insulation medium [13, 14] or for achieving a compact modulator size, oil is utilized as insulation material [12, 15]. One module mainly consists of a charging switch S_C, a capacitor C, a discharging switch S_D and a bypass diode D_B, whereas IGBTs or FETs are employed as high voltage switches [11]. During the charging process $S_{C1} - S_{Cn}$ are switched on and $S_{D1} - S_{Dn}$ are inactive. The capacitors $C_1 - C_n$ are connected in parallel to the charging source V_DC via the bypass diodes. Afterwards, to generate the high voltage pulse, $S_{C1} - S_{Cn}$ are inactive and $S_{D1} - S_{Dn}$ are switched on, connecting the capacitors $C_1 - C_n$ in series to the load. For short pulse lengths or low pulse duty cycles, the charging switches can be replaced by resistors or inductors [15]. The possibility for a droop compensation is inherently given, since the Marx modules can be turned-on shifted in time. To compensate the voltage droop, some of the Marx cells can be employed as compensation cells, which are turned-on distributed during the pulse, but lead to a high output voltage ripple [16]. Therefore, special cells are developed, which provide a lower output voltage [15], [12] or modulate their output voltage [17] for a fine tuning droop compensation. Each cell, which is switched on later, is first bypassed by its bypass diode $D_{\mathrm{B}i}$. Therefore, there is no requirement for such a strict synchronization between the switches as there is for example in the direct switch topology.
The advantages of this topology are the simple modular structure and the high voltages switches just have to isolate the charging voltage V_DC and not the full output voltage. Further, the pulse can be easily extended in height and width by putting more cells in series. However, additional measures have to be applied to limit the short circuit energy

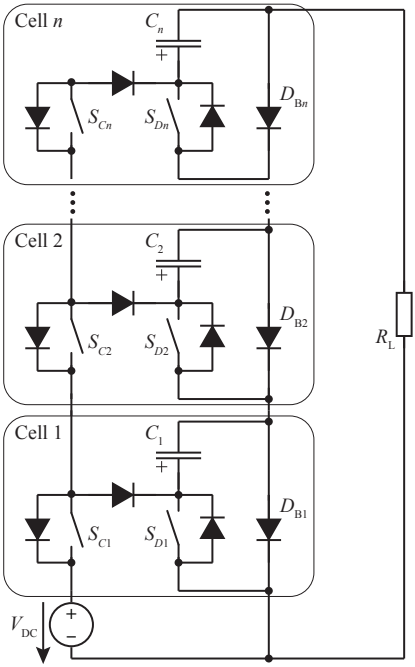


Figure 1.4: Modular solid state Marx modulator structure. In a first step, $S_{D1} - S_{Dn}$ are inactive and $S_{C1} - S_{Cn}$ are turned-on for charging $C_1 - C_n$. Afterwards, in a second step, $S_{C1} - S_{Cn}$ are turned-off and $S_{D1} - S_{Dn}$ are turned-on for generating the high voltage pulse [12].

in case of load arcing, like for example an inductor in series to the load.

1.1.3 Pulse transformer

Pulse transformers are often used in combination with the before mentioned topologies. So-called hybrid solutions are shown in Fig. 1.5. Figure 1.5 (a) shows the direct switch topology [19, 20] in series with a pulse transformer, whereas the Marx topology [21, 22] in combination with a pulse transformer is depicted in Fig. 1.5 (b). Stepping up the output voltage with the help of the pulse transformer winding ratio, results in a possible lower number of semiconductor switches in series

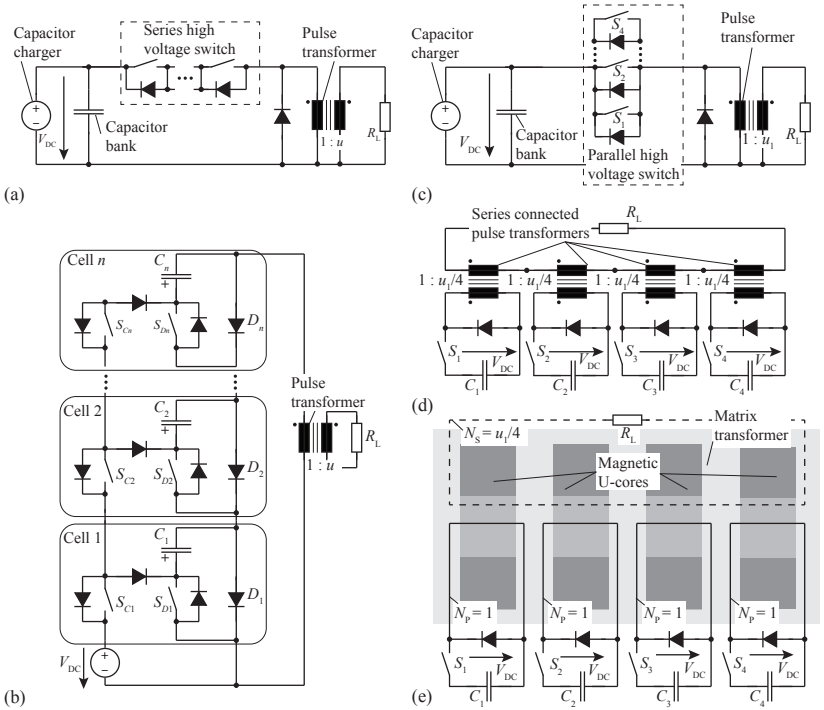


Figure 1.5: Hybrid pulse transformer topologies: (a) Direct series HV-switch + pulse transformer, (b) Marx generator + pulse transformer. (c) Direct parallel HV-switch + pulse transformer (d) Series connection of four single pulse transformers with the same output behaviour as in (c). (e) Matrix transformer solution with the same output behaviour as in (c) and (d), which results in lower transformer parasitics than in (c) and (d) [18].

for the HV-switch, in the case of the direct switch topology, respectively a lower number of cells in series in the case of the Marx generator topology. The transformer turns ratio also enables a reduction of the charging voltage V_{DC}. Since the transformers are often operated with unipolar pulse voltages, there is the need of a demagnetization circuit [10]. If a higher output pulse power is required, simply more switches are directly connected in parallel at the primary side of the transformer, as can be seen in Fig. 1.5 (c). A proper current balancing between the parallel connected switches has to be ensured by control [18]. In order

to avoid the current balancing control system, the single transformer is replaced by four transformers, each with a fourth of the turns ratio of the single transformer. The circuit shown in Fig. 1.5 (d) has the same electrical output behaviour as the circuit in Fig. 1.5 (c). Due to the series connection of the secondary windings, an equal current in the primary windings, respectively switches is automatically ensured, because the current through all secondary windings is the same [23].
One major issue, if employing pulse transformers, is the additional inductance which is integrated in the circuit in form of the leakage inductance. On the one hand, the leakage inductance L_σ automatically limits the current in case of load arcing, but on the other hand it negatively influences the rise time t_{rise} which follows the relation [18]

$$t_{\mathrm{rise}} \sim \sqrt{L_\sigma C_{\mathrm{d}}} \tag{1.1}$$

where C_{d} is the stray capacitance of the transformer. In the case of Fig. 1.5 (d), the total leakage inductance of the four transformers is a fourth compared to the single transformer in Fig. 1.5 (c). The total stray capacitance is four times higher compared to the single transformer in Fig. 1.5 (c), if a similar voltage distribution is assumed. Hence, the rise time stays the same. The so-called Matrix transformer [23] is an enhanced transformer which further reduces the rise time by achieving the same electrical output behavior and the automatically current distribution in the primary switches. The depicted Matrix transformer in Fig. 1.5 (e) consists of four cores, which are enclosed by the secondary winding. The flux in the secondary winding is the sum of the fluxes of the primary windings. Therefore, the turns ratio is the same as in Fig. 1.5 (d) [18]. The big advantage of the Matrix transformer compared to the series connection of single transformers is that the cores can be arranged close to each other, which results in smaller parasitics, a reduced volume, as well as an improved rise time.
However, a big disadvantage of the pulse transformer based topology is the size of the pulse transformer itself. Due to the design constraint of the high voltage-time product, the transformer becomes huge and is therefore limited to a maximal pulse length, once it is built. Further, the modularity of the hybrid direct switch topology and the hybrid Marx generator based topology is also lost due to the single transformer.

1.1.4 Pulse step modulator

The pulse step modulator (PSM) topology is shown in Fig. 1.6. There, n modules are connected in series at the output, which supply a pulse transformer for achieving the output voltage [24]. Alternatively, the transformer can be avoided by simply putting more modules in series [25, 26]. Each PSM-module is supplied from a winding system which is part of a special multi-secondary winding transformer and provides the galvanic isolation. A single module consists of an input rectifier with boost converter for charging the DC-link capacitors and a semiconductor half bridge. The boost converter ensures a constant input power consumption, which reduces the flicker emissions of the modulator. If a pulse transformer is employed for the final pulse voltage generation, some modules can be employed as active demagnetization\reset circuits (see the special wiring of the top module in Fig. 1.6). For generating the output pulse, the switches with the sub-indexes $_{\mathrm{p}}$ are turned-on and connecting the outputs of the modules in series. For achieving a more accurate pulse shape, a PWM is superimposed [27], which is also used for the droop compensation [24]. The switching frequency, as well as the harmonics are then reduced by the output filter. At the end of the pulse, the switches with the sub-indexes $_{\mathrm{p}}$ are simply turned-off. Con-

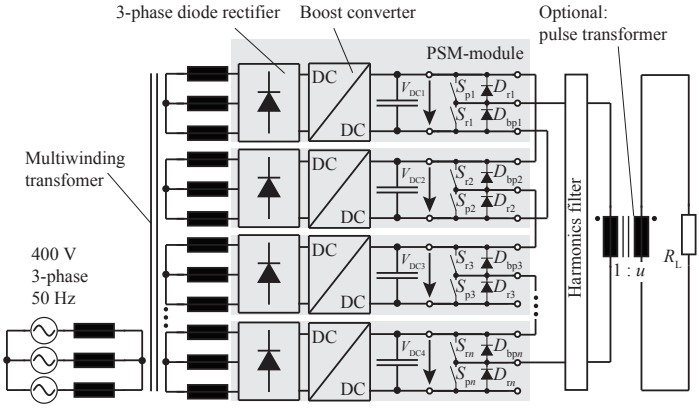


Figure 1.6: Pulse step modulator with input transformer, n-PSM modules in series, harmonics filter and pulse transformer. A single PSM module consists of an input rectifier with boost converter, a DC-link capacitor and a semiconductor half bridge with bypass diodes [24].

sequently, the bypass diodes with sub-index $_{bp}$ start conducting and an automatic passive demagnetization of the transformer occurs. If an active demagnetization is required, the switches with the sub-indexes $_{r}$ are turned-on at the beginning of the pulse break. A negative voltage is applied to the transformer and the recovered energy is charged back into the DC-link capacitors. The big disadvantage of this topology is the loss of the modularity because of the special input transformer and the output pulse transformer, which also increase the complexity of the system.

1.1.5 Isolated DC-DC converter topologies

High voltage pulses in the ms-range and longer can be also generated with isolated DC-DC-converter based topologies. Figure 1.7 shows the principle modulator structure. An AC-DC capacitor charging unit, which is supplied from the common 3-phase grid, supplies the DC-link capacitors. This common DC-link feeds multiple isolated DC-DC converter modules in parallel, which are connected in series at the output for generating the high output voltage pulse. Due to the series connection, the bulky pulse transformer can be avoided. The full modular

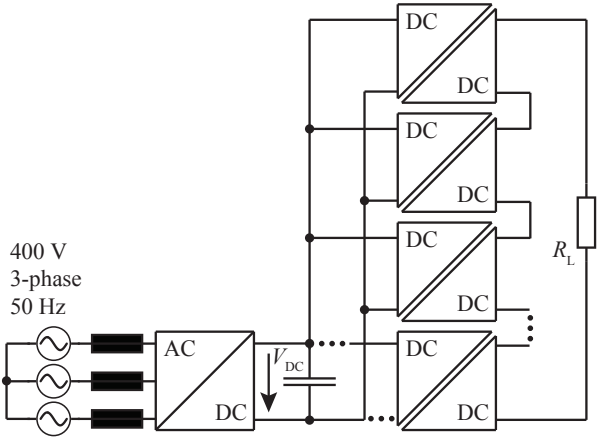


Figure 1.7: Principle structure of a DC-DC-converter based long pulse modulator.

design enables an easy achievable increase of the output voltage by simply putting additional modules in series, as well as a higher redundancy with additional modules can be provided. For reducing the output voltage ripple, the modules can be operated interleaved. The droop of the output voltage is compensated in a closed loop regulation by adapting the duty-cycle or the switching frequency of the modules.
Typical isolated DC-DC modules are for example the single active bridge converter, which is formed by a semiconductor H-bridge, a transformer and an output rectifier, as presented in [28, 29], or resonance converters, as presented in [30–34]. A typical series parallel resonance converter (SPRC) module is shown in Fig. 1.8. In case of the SPRC, the HV-HF transformer is loaded with almost sinusoidal waveforms due to the resonant tank. This results in a low number of high frequency losses compared to the single active approach in which the transformer is operated with rectangular shaped waveforms. Further, the SPRC approach naturally provides soft switching, which reduces the EMI and enables high switching frequencies. Usually, off-the-shelf components as IGBTs or MOSFETs are used for the H-bridge switches with a chosen break down voltage depending on the DC-link voltage. In both converter types, the modules are switched with high frequencies in the upper kHz-range, which results in a small voltage time product for the transformers and therefore a compact small size of the transformers. Since the module transformers are exited with an alternating voltage, the size of the transformer is not depending on the pulse length and the reset- or demagnetization circuits for the transformers are not required. Further, regarding a single module, the active switched power electronic is placed on the primary side of the HF-transformer, which simplifies the gate controller design and reduces the repair time in case of a switching failure.

The SPRC consists of a H-bridge, the resonant tank with series inductor L_S, the series capacitor C_S, the parallel capacitor C_P, the high-voltage, high-frequency transformer, the output rectifier, the harmonics filter and the load, as can be seen in Fig. 1.8. The SPRC is a combination of the series resonance converter (SRC) and the parallel resonance converter (PRC). It combines the advantages of both, because it is still controllable in the case of an open loop at the output, which is not possible in the case of the SRC, and if proper designed, a lower circulating reactive power occurs, as compared with the PRC [35]. The circuit acts similar like a SRC if the ratio $C_\mathrm{P}/C_\mathrm{S} \ll 1$ and like an PRC if the ratio

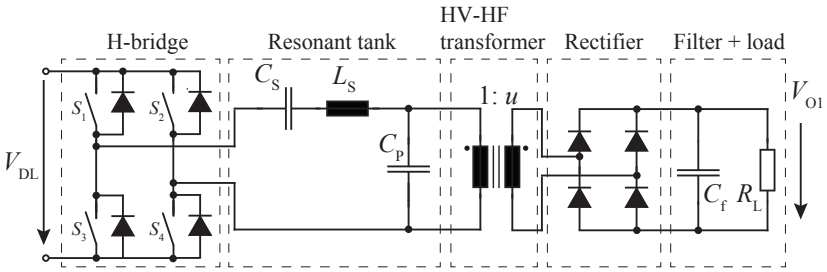


Figure 1.8: Series parallel resonance converter formed by a H-bridge, a resonant tank, a high-voltage, high-frequency transformer and the output rectifier stage with filter and load.

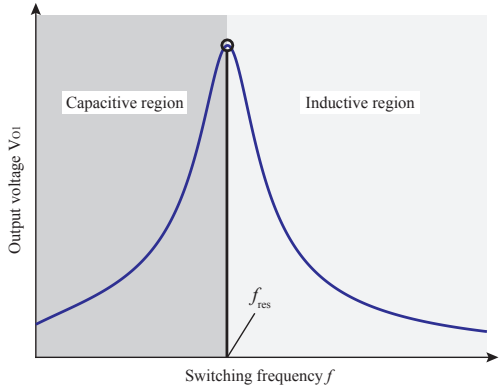


Figure 1.9: Output voltage characteristic of the SPRC.

$C_P/C_S \gg 1$ [36]. In addition, the leakage inductance and the stray capacitance of the HV-HF transformer can be integrated in the resonant tank. Further, in the case of load arcing, the SPRC is naturally short circuit proof due to the resonant inductor. Figure 1.9 shows the typical output voltage characteristic of the SPRC. The magnitude of the ouput voltage can be controlled eihter by changing the switching frequency, as can be seen in Fig. 1.9, or\and by phase shift control of the H-bridge switches [37]. For reducing the losses, zero current switching (ZCS) can be achieved for all switches of the H-bridge if operated with a switching frequency below the resonance frequency, whereas zero voltage switching (ZVS) can be achieved, if operated above the resonance frequency

[38]. Also a combination of ZVS-ZCS is possible, if the SPRC is operated close to the resonance frequency. There, one leg of the H-bridge is turned-off with ZCS and the other one is turned-on with ZVS. More information on this topic is given in [39, 40].

Comparing the presented topologies leads to following conclusions. The direct switch topology, the Marx modulator topology and the isolated DC-DC converter based topology are fulfilling the criteria of a full modular approach, which leads to reduced production costs and additionally allows for an easy achievable safety redundancy. This is of high interest because of the huge number of modulators which will be installed at ESS. The full modularity is lost in any case if a single pulse transformer is employed. The big problem of the direct switch topology is the exact synchronization of the series connected switches, which, if not ensured, leads to the destruction of the HV-switch, hence to a fail of the modulator system. The main disadvantage of the Marx modulator approach, as well as for the direct switch topology, is the need for additional measures to detect and limit the current in case of a load arcing. The isolated DC-DC topology overcomes this problem if SPRC-modules are used as modules. Further, no active controlled power electronics are applied to the high voltage, which results in a high reliability. Therefore, the modular isolated DC-DC converter topology with SPRC modules is chosen for the considered modulator system.

1.2 Objectives and contributions of the thesis

The main objective in this thesis is the development and the investigation of fast and accurate models, which are used for the design of a long pulse modulator system with an output voltage of 115 kV and an output power of 2.88 MW during the pulse. After the identification of a suitable topology, a new concept, which is based on series parallel resonance converter modules, is presented for achieving the given output pulse power and the output voltage. Due to the high output power, it is of major interest to obtain a high efficiency in addition with a compact modulator size. Therefore, the design process is carried out with the help of a developed multi-objective optimization procedure. In addition, the focus lies on the proof of the derived models, which finally are validated by a full scale prototype system. In the following, the main contributions of the thesis are summarized.

- *Identification of a suitable long pulse modulator topology:* A range of long pulse modulator topologies exist, which can be employed for producing pulses in the ms-range, but only the isolated DC-DC resonant converter based topology provides the demanding full modularity with the ability to be short circuit proof at the same time without any additional measures. The identified resonant topology is discussed and a new concept for achieving the given output specifications from Tab. 1.2 is presented.

- *Multi-objective long pulse modulator optimization design procedure:* Due to the high number of degrees of freedom like for example the number of semiconductors of the H-bridge or the geometric parameters of the high-voltage high-frequency transformer, an optimization procedure for designing the SPRC-Bm is developed. This procedure includes the relevant models like an electrical and a thermal model and additionally an insulation design procedure, as well as a loss model for the SPRC-Bm components. The design of the single module is then verified with the constraints of the global specifications of the overall system and this finally leads to the optimal number of single SPRC-Bms which are connected in parallel and in series.

- *Design of a high-frequency transformer with a high isolation voltage:* Since the high-voltage high-frequency transformers are major key components of the modulator system, a transformer design

procedure, which is part of a multi-objective optimization procedure, is developed. The design procedure of the transformer includes a generalized magnetic model for the leakage and the high frequency loss calculations, as well as an electrical model for the parasitic capacitance estimation for the transformer. Both parasitics models show a good match compared with measurement results. Additionally, an alternative approach, which is based on conductor arrays, for the determination of the parasitics, is discussed. Due to the series connection of the SPRC-Bms, the insulation of the last oil isolated transformer in the row has to withstand the full pulse voltage of 115 kV. Therefore, for designing the insulation, a comprehensive design method based on an analytical maximum electrical field evaluation and an electrical field conform design is used. The resulting insulation design is verified by long and short term partial discharge measurements on a prototype transformer.

- *Development of a novel thermal resistance model for solid and litz wire windings:* At the end of the high-voltage high-frequency transformer design procedure, a valid design has to fulfill the maximal temperature constraints. Hence, for an accurate temperature estimation of each part of the transformer, an equivalent thermal circuit of the transformer is required. There, the main components of the transformer are modeled by thermal resistors. Although, thermal models for the transformer core or the bobbins are available, there exists a lack of a proper thermal description of the windings. Therefore, for an accurate temperature estimation of the windings, a novel thermal resistance model has been derived. The proposed model can be used for litz wire windings, as well as for solid wire windings and has been validated by measurements of non- and epoxy-casted test winding setups. The derived thermal winding model is then employed in the equivalent thermal circuit of the transformer and the so analytically estimated winding temperatures show good accordance to measurements.

- *Control concept for the long pulse modulator system:* Two control strategies for the voltage balancing and an equal power sharing of the SPRC-Bms are developed. Such unbalances occur due to resonant tank component tolerances of the SPRC-Bms. In addition, the control systems have to compensate the output voltage

droop by varying the switching frequency, because the input voltage source is not able to keep the input voltage constant due to the high power consumption during the pulse. The influence on the possible ZVS range due to the proposed droop compensation is shown. For the determination of the control parameters values a small and a large signal model of the modulator system is derived. The performance of the investigated control systems is verified with measurements, respectively with simulations.

- *Validation of the developed models with a full scale prototype system:* The final built prototype system confirms the results of the developed models with measurements and a 7 and 2/3 hours heat run test. The system achieves a pulse efficiency (determined by the pulse shape) of 96.78 %, an overall electrical system efficiency of 91.9 % and a combined pulse system efficiency of 89 %.

1.3 Outline of the thesis

In this thesis the comprehensive design of a 2.88 MW long pulse modulator system with an output voltage of 115 kV and the development of the modulator control system is presented. The current work is based on already published or submitted scientific international journals and conference proceedings and is organized as follows.

Chapter 1 starts with an introduction, which guides through the field of pulse power research and gives an overview of possible pulse generating topologies.

Chapter 2 conducts the design of the SPRC-Bm components with the help of an optimization procedure.

- In section 2.1, which is based on Journal VII, a procedure for an optimal design of the SPRC-Bm components is developed. All relevant models as a thermal semiconductor model, a model for the calculations of the leakage inductance and the stray capacitance inside the transformer, as well as a simple thermal model of the transformer are basically introduced and analytically described.
- In section 2.2, the electrical model of the SPRC-Bm is analytically derived and compared with an alternative approach. Based

on this analysis the determination of the loss equations for each SPRC-Bm component are given.

- Section 2.3, which is based on Journal V, discusses possible series inductor realisations, which are compared by losses and volume. Further, an extension of the parasitics models, which additionally covers the region outside the transformer is obtained. A full scale prototype of a single SPRC-Bm and according pulse measurement results are presented.

- Section 2.4, which is based on Journal IV, focuses on the detailed design of the high-voltage high-frequency transformer, which is one major key component of the overall system. The calculation of the high frequency losses and a comprehensive insulation design procedure are carried out. In addition, an alternative approach for calculating the transformer parasitics is presented and a comparison between FEM simulations, the approaches from Section 2.1 and Section 2.3 and measurements, is given. Finally, high voltage tests, as well as partial discharge measurement results, which validate the insulation design, are shown.

- In Section 2.5, which is based on Conference I, an analytical approach for the determination of the output ripple voltage of output series, output parallel or output parallel-output series connected SPRC-Bms, is presented.

Chapter 3 is based on Journal II. General analytical expressions for the thermal resistance of windings made of solid or litz wire are presented. The analysis is verified by measurements on non- and epoxy-potted winding test setups, whereas the given approach is based on the electrothermal analogy. Finally, the derived equations are employed in an equivalent thermal circuit of the high-voltage high frequency transformer and show good accordance to measurements.

Chapter 4 is based on Journal III. Two control systems are investigated and verified by measurements respectively simulations. The proposed control systems ensure a proper input and output voltage balancing, as well as an equal power sharing between the SPRC-Bms due to component tolerances. In addition, the control systems also provide an output voltage droop compensation, because the input voltage source is not able to keep the input voltages of the SPRC-Bms constant

during the pulse. In order to find appropriate values for the control parameters, a small and a large signal model of the modulator system is analytically derived.

Chapter 5 is based on Journal I. It summarizes the pulse modulator system design and presents the final built full scale prototype system. The final output voltage pulse performance, in terms of efficiency, is derived based on measurements. An evaluation of the achieved rise and fall times, as well as an detailed evaluation of the achieved pulse ripple spectrum, is given. Further, the system design has been proven by a 7 and 2/3 hours heat run test resulting in the final temperature distribution of the high-voltage high-frequency transformer under worst case conditions.

Chapter 6 recapitulates the major achievements of this thesis and gives an outlook for future research work.

1.4 List of publications

The main parts of the following chapters have been already published in scientific international journals and conference proceedings. A complete list of the publications is given in chronological order below.

1.4.1 Journal papers

I. M. Jaritz and J. Biela, "System Design and Measurements of a 115 kV/3.5 ms Solid State Long Pulse Modulator for the European Spallation Source," *Accepted for publication in the IEEE Transactions on Plasma Science.*

II. M. Jaritz, A. Hillers and J. Biela, "General Analytical Model for the Thermal Resistance of Windings Made of Solid or Litz Wire," *Accepted for publication in the IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1 – 1, 2018.

III. M. Jaritz, T. Rogg and J. Biela, "Analytical Modelling and Controller Design of a Modular Series Parallel Resonant Converter System for a Solid State 2.88MW/115-kV Long Pulse Modulator," *Accepted for publication in the IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1 – 1, Dec. 2017.

IV. M. Jaritz and J. Biela, "Design Procedure of a 14.4 kV, 100 kHz Transformer with a High Isolation Voltage (115 kV)," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 24, no. 4, pp. 2094–2104, Sep. 2017.

V. M. Jaritz, S. Blume, D. Leuenberger and J. Biela, "Experimental Validation of a Series Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator," *IEEE Transactions on Plasma Science*, vol. 43, no. 10, pp. 3392–3398, Oct. 2015.

VI. S. Blume, M. Jaritz and J. Biela, "Design and Optimization Procedure for High-Voltage Pulse Power Transformers," *IEEE Transactions on Plasma Science*, vol. 43, no. 10, pp. 3385–3391, Oct. 2015.

VII. M. Jaritz and J. Biela,"Optimal Design of a Modular Series Parallel Resonant Converter for a Solid State 2.88 MW/115-kV Long Pulse Modulator," *IEEE Transactions on Plasma Science*, vol. 42, no. 10, pp. 3014–3022, Oct. 2014.

1.4.2 Conference papers

I. M. Jaritz and J. Biela, "Output Voltage Ripple Analysis for Modular Series Parallel Resonant Converter Systems with Capacitive Output Filter," *Accepted for publication in the 20th European Conference on Power Electronics and Applications (EPE'18 ECCE-Europe)*, 2018.

II. M. Jaritz and J. Biela, "115 kV Solid state long pulse modulator for the european spallation source (ESS)," *Accepted for publication in the Proc. 21st IEEE Pulsed Power Conference (PPC)*, 18-22 June 2017.

III. M. Jaritz and J. Biela, "Optimal design of a medium voltage high frequency transformer with a high isolation voltage (115 kV)," in *IEEE International Power Modulator and High Voltage Conference (IMPHVC)*, 5-9 July 2016.

IV. M. Jaritz, T. Rogg and J. Biela, "Control of a Modular Series Parallel Resonant Converter System for a Solid State 2.88 MW/115-kV Long Pulse Modulator," in *Proc. 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 8-10 Sept. 2015, pp. 1–11.

V. M. Jaritz, S. Blume and Biela, "Experimental Validation of a Serial Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator," in *Proc. 5th Euro-Asian Pulsed Power Conference (EAPPC)*, 8-12 Sept. 2014.

VI. S. Blume, M. Jaritz and Biela, "Design and Optimization Procedure for High Voltage Pulse Power Transformers," in *Proc. of the 5th Euro-Asian Pulsed Power Conference (EAPPC)*, 8-12 Sept. 2014.

VII. M. Jaritz and J. Biela, "Analytical model for the thermal resistance of windings consisting of solid or litz wire," in *IEEE 15th European Conference on Power Electronics and Applications (EPE)*, 2-6 Sept. 2013, pp. 1–10.

VIII. M. Jaritz and Biela, "Optimal design of a modular 11 kW series parallel resonant converter for a solid state 115-kV long pulse modulator ," in *Proc. 19th IEEE Pulsed Power Conference (PPC)*, 16-21 June 2013, pp. 1–6.

IX. M. Jaritz and Biela, "Optimal Design of a Series Parallel Resonant Converter for a Solid State Long Pulse Modulator," in *Proc. 4th Euro-Asian Pulsed Power Conference (EAPPC)*, 30 Sept.- 4 Oct. 2012.

1.4.3 Poster publications

I. S. G. Keens, M. Frei, M. Bader, B. Fritsche, S. Choroba, H. J. Eckoldt, R. Wenndorff, G. Blokesch, W. Kaesler, J. Biela, D. Gerber and M. Jaritz, "Modulators for Cutting Edge FELs and LINACs: An Overview of State-of-the-Art Design and Topologies," in *37th International Free Electron Laser Conference (FEL)*, 23-28 Aug. 2015.

2

Multi-objective optimization design procedure of the modulator system

In this chapter, the derivation of the models for designing the pulse modulator, with the help of a multi-objective optimization procedure, is presented. The procedure delivers all component values of the resonant tank, the number of semiconductor switches and finally the number of modules, which has to be connected in parallel and series. The presentation of the used models is organized as follows. In section 2.1, the developed optimization procedure is presented and all relevant models are basically introduced. The main parts of the procedure are:

- The electrical model of the SPRC-Bm
- A thermal model of the semiconductor switches
- High frequency loss models
- An approach for the calculation of the transformer parasitics (leakage inductance, stray capacitance)
- A basic thermal model of the transformer (A detailed model is presented in chapter 3)
- A basic isolation design procedure of the transformer

The detailed analysis of the electrical model of a SPRC-Bm, is then given in section 2.2 and section 2.3 presents first measurement results of a single SPRC-Bm prototype. Additionally, extended parasitic models, as well as an important improvement for designing the isolation of

the transformer, are given in this section. The detailed transformer design, which includes the high frequency loss models and a full isolation design procedure, which is verified by long term high voltage tests, is carried out in section 2.4. In addition, an alternative approach for calculating the transformer parasitics is presented in this section. Finally, an analysis for the estimation of the output voltage ripple is presented in section 2.5. All presented models are verified by simulations and measurements.

2.1 Journal VII.: Optimal Design of a Modular Series Parallel Resonant Converter for a Solid State 2.88MW/115-kV Long Pulse Modulator

Michael Jaritz and Juergen Biela
IEEE Transactions on Plasma Science, Volume: 42, Issue: 10, Page(s): 3014 - 3022, October 2014.
DOI: 10.1109/TPS.2014.2332880

Abstract

Modern accelerator driven experiments like linear colliders or spallation sources are supplied by RF amplifiers using klystrons. The cathode voltage for these klystrons can be generated by long pulse modulators generating highly accurate voltage pulses in the length of milliseconds. Conventional designs using pulse transformers become huge for long pulses. The series parallel resonant converter (SPRC) topology avoids this drawback as the transformer is operating at high frequencies. This paper presents a comprehensive design approach for SPRC modules, which is based on an optimization procedure containing an electrical model of the resonant circuit and a thermal model of the semiconductors. Additionally an insulation and a leakage design procedure and a thermal model of the transformer is also presented. Finally, this procedure provides the optimal design parameters of the resonant circuit elements. With these parameters a global optimizer chooses the optimum amount of modules connected in series and/or in parallel to fulfill the given restrictions. The efficiency of a basic SPRC-module is 94.7 % with a pulsed power density of 4.63 kW/l.

2.1.1 Introduction

In literature exist several approaches to create accurate high voltage pulses with pulse specifications listed in Tab. 2.1. The classical Bouncer Modulator topology generates its pulse voltage by charging a capacitor bank and amplifies this voltage with a single pulse transformer [41], [42]. The main disadvantage of this topology is the use of one single huge pulse transformer which has to be designed for the whole pulse voltage time area.

Table 2.1: Pulse specifications

Pulse voltage	V_K	115 kV
Pulse current	I_K	25 A
Pulse power	P_K	2.88 MW
Pulse repetition rate	P_{RR}	14 Hz
Pulse width	T_P	3.5 ms
Pulse duty cycle	D	0.05
Pulse rise time (0 ... 99 % of V_K)	t_{rise}	150 μs
Pulse fall time (100 ... 10 % of V_K)	t_{fall}	150 μs
Short circuit energy	E_{arc}	$\leq$ 10 J

The Marx Modulator topology uses a modular approach [43]. This topology avoids a pulse transformer and the modular design is an advantage considering the increase of the pulse voltage. To overcome the droop problem some modules are used for active compensation [17]. Unfortunately, it is not short circuit proof without additional measures. The Pulse Step Modulator also utilises a modular design [44]. There, DC/DC-modules are connected in series to generate the pulse voltage, which is amplified with a single pulse transformer to its nominal magnitude. This design allows droop regulation during the pulse duration, but also requires a single pulse transformer. The SPRC topology (see Fig. 2.1) is a modular design which needs no pulse transformer. The series parallel resonant converter is a modular topology which avoids this drawback as the transformer is operated at high frequencies. The considered nominal pulse voltage amplitude is 115 kV with a pulse power of 2.88 MW and a pulse length of 3.5 ms. In order to meet these highly demanding specifications listed in Tab. 2.1, the modulator is based on interleaved SPRC modules. A SPRC module [45] contains a full bridge connected to a series parallel circuit followed by a transformer a rectifier and a filter capacitor. In this paper, an optimal design of a single module is presented. The basic modules of the SPRC can be connected in series or in parallel depending on the output power and ripple specifications and can also be interleaved. By reason that the pulse shaping is achieved with a rectifier and a filter on the secondary side

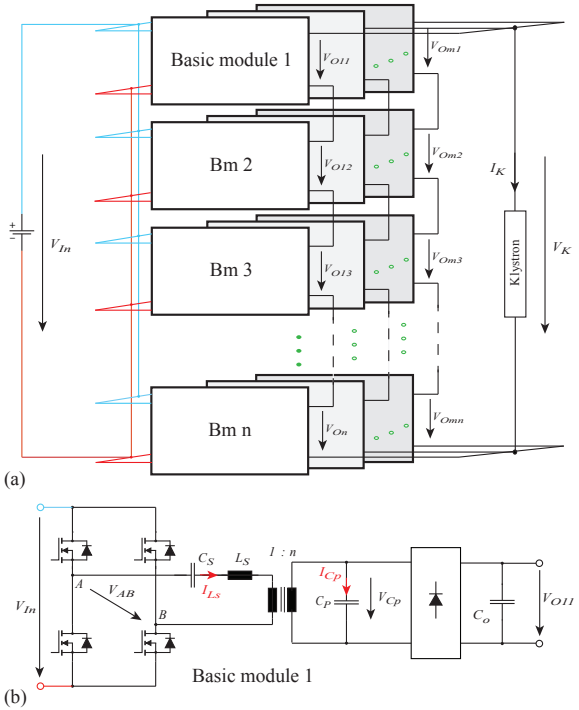


Figure 2.1: (a) SPRC topology and (b) SPRC basic module.

of the transformer, the pulse duration is relatively independent from the transformer size. Furthermore, the SPRC is naturally short circuit proof and provides zero voltage switching (ZVS). Additionally, the series inductance L_S can be partly integrated by the leakage inductance of the transformer. Due to those advantages, the SPRC topology is investigated in the following. A straight forward design is difficult due to the high number of degrees of freedom and geometric parameters of the transformer. Thus, in this paper an optimization procedure with given design constraints is presented in section 2.1.2. As the electrical models is already commonly introduced in [45] section 2.1.3 only summarizes the electrical SPRC model shortly, but put a detailed emphasis on the thermal semiconductor model, the thermal transformer model as well on the leakage and isolation design procedures. Finally, section 2.1.4

presents the optimization results.

2.1.2 Optimization procedure

Based on the specifications of the pulse in Tab. 2.1, Fig. 2.2 shows the optimal design procedure of the SPRC. In a first step, the optimizer varies the free parameters in the single module design with respect to the chosen design constraints in Tab. 2.2. This single module design procedure consists of an electrical and a thermal model, and additionally of an insulation and leakage design procedure. The design of the single module is then verified with the constraints of the global specifications and this finally leads to the optimal number of single SPRC modules which are connected in series and/or in parallel.

Table 2.2: Optimization parameters and constraints

Optimization parameters		
Transformer core	**Windings**	**Semiconductors**
l,t,h (see Tab. 2.3)	# of turns # of litz wire strands	# of switches
Constraints		
Maximum magnetic flux density B_{max}		150 mT
Maximum winding temperatures T_1, T_2		120 °C
Maximum temperatures in core parts T_3, T_4		120 °C
Maximum change of junction temperature ΔT_J		20 °C
Maximum electrical field strength E_{max}		15 kV/mm

2.1.3 Single module design models

The following section shortly summarizes the electrical model of the single SPRC-module. Afterwards the thermal semiconductor model is explicitly investigated and the design procedures for the transformer

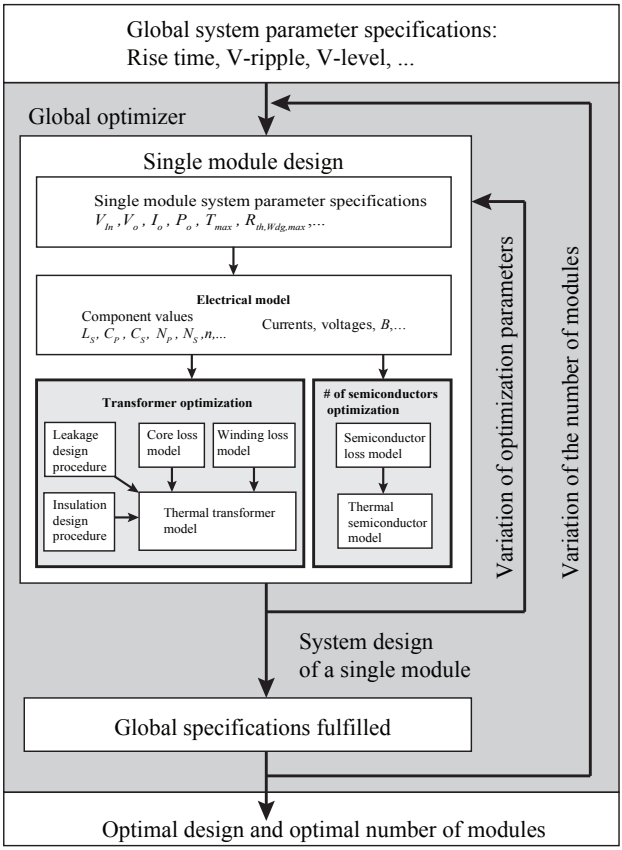


Figure 2.2: Proposed optimization procedure which leads to an optimal design of a single SPRC-module and an optimal number of modules of the overall system.

insulation, leakage inductance and the thermal model of the transformer are given in detail.

2.1.3.1 Electrical model

The electrical model of the SPRC basic module (see Fig. 2.1 (b)) is described with a first harmonic analysis [45], which also takes the output capacitor and rectifier into account. This model considers the trans-

former just as a voltage amplifier with turns ratio n and determines all parameters of the resonant circuit (C_S, C_P, L_S, n) respectively delivers all voltages and currents.

2.1.3.2 Semiconductor thermal model

In this model, the resonant current calculated from the electrical model is used to determine the number of switches which leads to minimum losses with the constraint of a maximum ΔT_J. The losses P_V include conduction and switching losses. The conduction losses can be calculated directly from data sheet and the switching losses either are included from measurements or estimated also from data sheet. ΔT_J is used for lifetime estimations due to [46]. In order to determine ΔT_J in the most exact way, the heat sink is also considered in the thermal model. Unfortunately, only the Foster elements as depicted in Fig. 2.3 (a) are given in most semiconductor data sheets. It is not allowed to connect the semiconductor Foster elements directly with the Cauer heat sink elements (see Fig. 2.3 (b)) in series. Therefore, the Foster elements of the semiconductor are first transformed analytically into Cauer elements [47]. Afterwards both Cauer models are added in series forming the model shown in Fig. 2.3 (c). The overall Foster thermal impedanz $Z_{thF,N}(s)$ in the Laplace domain can be written as:

$$Z_{thF,N}(s) = \sum_{k=1}^{N} \frac{R_{thF,k} \cdot C_{thF,k}}{s \cdot R_{thF,k} \cdot C_{thF,k}^2 + C_{thF,k}} = \frac{p_n(s)}{q_n(s)} \tag{2.1}$$

By building the inverse of (2.1) and performing a polynom division leads to a linear, a constant and the reminder part rem_n of the polynom division.

$$\frac{q_n(s)}{p_n(s)} = s \cdot a_n + b_n + \frac{rem_n}{p_n(s)} \tag{2.2}$$

The first Cauer elements for $n = N$ are

$$R_{thC,n} = 1/b_n \quad \text{and} \quad C_{thC,n} = a_n \tag{2.3}$$

In order to determine the next Cauer elements $R_{thC,n-1}$ and $C_{thC,n-1}$ the new fraction is formed by

$$q_{n-1}(s) = b_n p_n(s) + rem_n(s) \text{ and } p_{n-1}(s) = \frac{-rem_n(s)}{b_n} \tag{2.4}$$

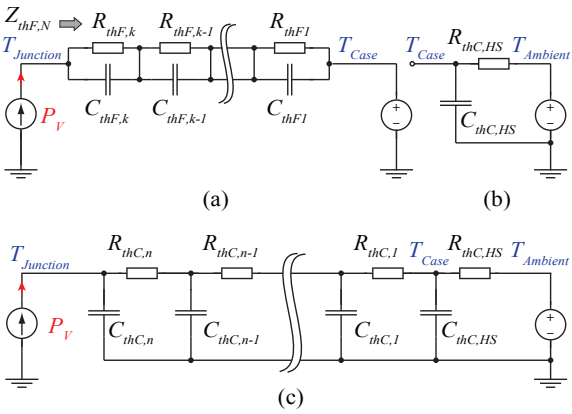


Figure 2.3: (a) Foster model of the semiconductor switch. (b) Cauer circuit elements of the heat sink. (c) Combined Cauer model consisting of semiconductor and heat sink.

and a polynom division has to be performed again. Equations (2.2), (2.3) and (2.4) have to be repeated until $p_0(s) = 0$. An additional advantage of the Cauer representation is that parts like insulation foils or heat sinks can now be easily integrated into the thermal model.
For IGBT modules, ΔT_J should not exceed 20 °K under the constraint

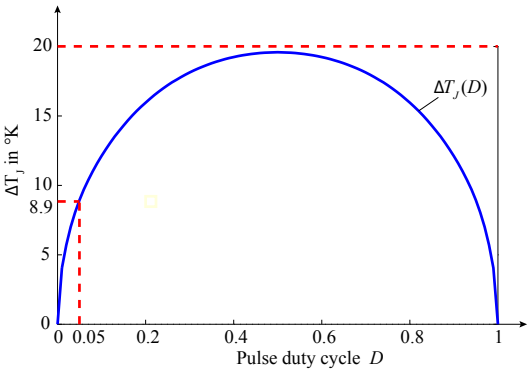


Figure 2.4: ΔT_J versus pulse duty cycle D. The calculated ΔT_J for one MOSFET is 8.9°K at nominal pulse duty cycle 0.05.

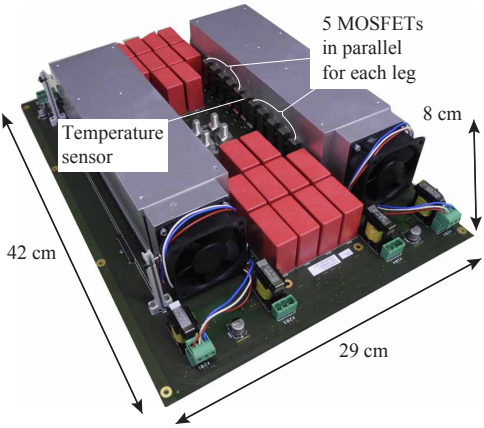


Figure 2.5: Prototype modulator each leg with 5 switches in parallel, with two legs on one heat sink.

of a maximum junction temperature of 125 °C to reach more than 10^8 pulses. The same maximum limits will be used for MOSFETs, what results in an optimal number of switches in parallel of 5. Fig. 2.4 depicts ΔT_J versus pulse duty cycle D. The calculated ΔT_J for one MOSFET is 8.9 °K at nominal pulse duty cycle 0.05. The investigated MOSFET is the STY139N65M5 from ST [48]. The required heat sink volume can be calculated with the Cooling System Performance Index (CSPI) as introduced in [49]. Fig. 2.5 shows the built modulator prototype, each leg consists of 5 switches in parallel.

2.1.3.3 Insulation design procedure

High electrical field strengths can harm the insulation of the transformer permanently and lead to arcs between the windings or the core. Therefore, a proper insulations design is unavoidable. Following assumptions are made for the insulation design. The borders of the winding window are grounded and the space between the windings and the rest of the winding window is completely filled with a homogenous isolation material. To calculate the electrical field inside the winding window the so called charge simulation method (CSM) (also called mirror charge method or image charge method) described in [50] is applied and is shortly explained in the case of one conductor. In Fig. 2.6 (a) the

conductor in the original window is represented by n image charges Q_j located inside the conductor on a radius d and belonging contour points on the radius r of the conductor each with the same conductor potential Φ_C. Φ_C is formed by the superposition of these image charges in

$$\Phi_C = \sum_{j=1}^{n} p_j \cdot Q_j \tag{2.5}$$

where p_j are the potential coefficients which contain the geometric locations of the images charges. By mirroring the original window three times counterclockwise gives the original box depicted in Fig. 2.6 (b). To build the basic box it would be also possible to mirroring around the original window but then the automated extension of mirrored basic boxes as seen in Fig. 2.6 (c) is much more complicated. Applying (2.5) to all windows in all basic boxes and corresponding image charges leads to a system of linear equations which has to be solved for the unknown charges Q

$$[Q] = [p]^{-1} \cdot [\Phi_C] \tag{2.6}$$

Afterwards is it possible to calculate the electrical field strength E at every location x and y inside the original window.

$$E = \sqrt{E_x^2 + E_y^2} \tag{2.7}$$

with

$$E_x = \sum_{j}^{n} \frac{Q_j}{2\pi\epsilon}(A1 + A2 + \ldots + Am) \tag{2.8}$$

$$A1 = \frac{x - x_j}{(x-x_j)^2+(y-y_j)^2} - \frac{x + x_j}{(x+x_j)^2+(y-y_j)^2} + \\ + \frac{x + x_j}{(x+x_j)^2+(y+y_j)^2} - \frac{x - x_j}{(x-x_j)^2+(y+y_j)^2} \tag{2.9}$$

$$A2 = \frac{x - x_j - 2\mathrm{X}}{(x-x_j-2\mathrm{X})^2+(y-y_j)^2} - \frac{x + x_j - 2\mathrm{X}}{(x+x_j-2\mathrm{X})^2+(y-y_j)^2} + \\ + \frac{x + x_j - 2\mathrm{X}}{(x+x_j-2\mathrm{X})^2+(y+y_j)^2} - \frac{x - x_j - 2\mathrm{X}}{(x-x_j-2\mathrm{X})^2+(y+y_j)^2} \tag{2.10}$$

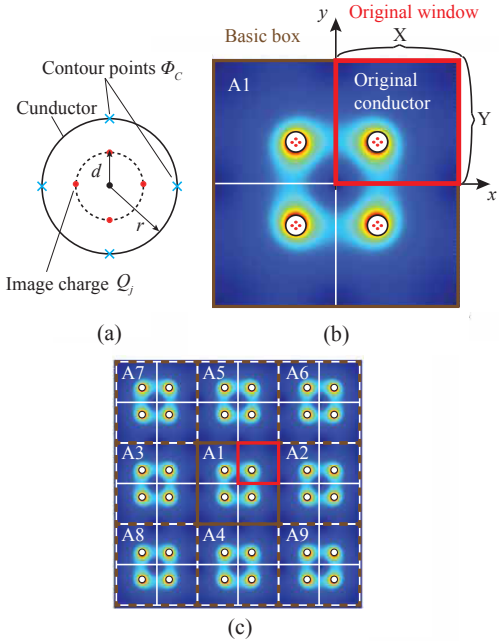


Figure 2.6: Charge simulation method based on mirror charges. (a) Conductor represented by image charges, (b) basic box which contains the original window and three mirrorings of it and (c) full set of used mirrorings.

and

$$E_y = \sum_{j}^{n} \frac{Q_j}{2\pi\epsilon}(B1 + B2 + \ldots + Bm) \tag{2.11}$$

$$B1 = \frac{y-y_j}{(x-x_j)^2+(y-y_j)^2} - \frac{y-y_j}{(x+x_j)^2+(y-y_j)^2} + \\ + \frac{y+y_j}{(x+x_j)^2+(y+y_j)^2} - \frac{y+y_j}{(x-x_j)^2+(y+y_j)^2} \tag{2.12}$$

$$B2 = \frac{y-y_j}{(x-x_j-2\mathrm{X})^2+(y-y_j)^2} - \frac{y-y_j}{(x+x_j-2\mathrm{X})^2+(y-y_j)^2} + \\ + \frac{y+y_j}{(x+x_j-2\mathrm{X})^2+(y+y_j)^2} - \frac{y+y_j}{(x-x_j-2\mathrm{X})^2+(y+y_j)^2} \tag{2.13}$$

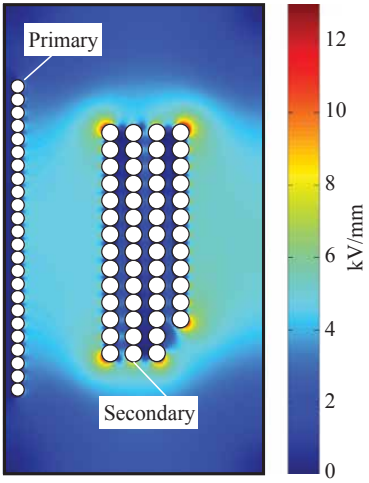


Figure 2.7: E-field distribution in grounded winding window.

where $A1$, $B1$ are the series of the positions of the image charges depending on the considered point x and y in the original box and $A2 - Am$, $B2 - Bm$ are according to the shifted boxes (see Fig. 2.6 (c) doted brown boxes). The variables x_j and y_j are the given positions of the image charges whereas X and Y are the width and the length of the original window. For computational reasons m is chosen 9 and the number of image charges is 16. This results in a quite high accuracy. Fig. 2.7 shows the E-field distribution of the final optimized design with an average field of 5.75 kV/mm and a maximum field of lower than 15 kV/mm. Depicted design has been also compared to FEM and gives a deviation of lower than 8 %.

2.1.3.4 Leakage design procedure

Basically, the transformer is designed to minimum isolation spaces which leads to a given leakage inductance that is calculated with the current mirror method. Here, each conductor is represented by a single current in the original window (see Fig. 2.8 (a)) which then is mirrored in the same way as described in the previous section (see Fig. 2.8 (b) and (c)). In contrast to the mirror charge method where in a first step all unknown charges have to be calculated, the current is inherently given.

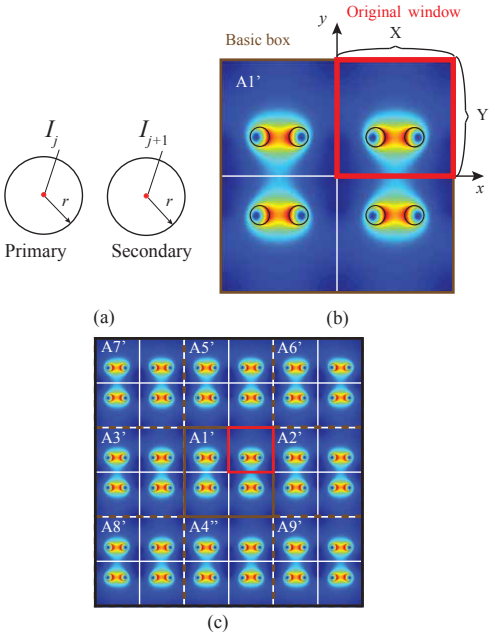


Figure 2.8: (a) Two conductors representing primary and secondary windings by conductor currents I_j and I_{j+1}, (b) basic box which contains the original window and three mirrorings of it and (c) full set of used mirrorings

Therefore

$$H = \sqrt{H_x^2 + H_y^2} \tag{2.14}$$

with

$$H_x = \sum_j^k \frac{I_j}{2\pi}(A1' + A2' + \ldots + Am') \tag{2.15}$$

$$H_y = \sum_j^k \frac{I_j}{2\pi}(B1' + B2' + \ldots + Bm') \quad . \tag{2.16}$$

The terms Am, Bm and Am', Bm' are almost the same with the difference that all fractional terms have plus-signs. Finally to get the leakage inductance referred to the primary side

$$L_{leak,P1} = \frac{2W_m}{I_P^2} \quad \text{with} \quad W_m = \frac{l_W \mu}{2} \iint H^2 dxdy \tag{2.17}$$

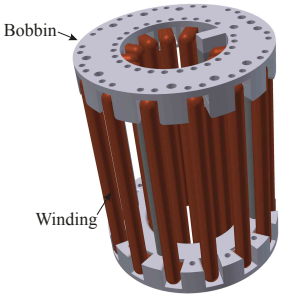


Figure 2.9: Auxiliary inductance $L_{toroid,Aux}$ formed by an air toroid.

where I_P is the total primary current and l_W the mean winding length. In order to get the final requested series inductance L_S an auxiliary inductance as shown in Fig. 2.9 delivers the missing inductance value $L_{toroid,Aux}$.

$$L_S = L_{leak,P1} + L_{toroid,Aux} \tag{2.18}$$

$L_{toroid,Aux}$ is formed by an air toroid which gives the advantages of no additional core losses, no saturation effects and low stray field.

2.1.3.5 Transformer thermal model

Based on the proposed transformer thermal model in [51], the model in Fig. 2.10 returns all critical temperatures. It contains all types of heat transfer represented in an equivalent thermal resistor:

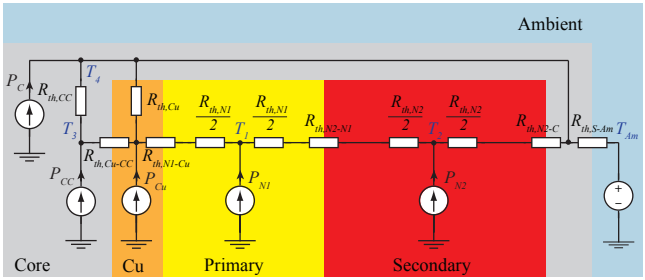


Figure 2.10: Thermal equivalent circuit of the transformer depicted in Fig. 2.11.

- Conduction [51]
  - $R_{th,N1-N2}$: acts between N_1 and N_2
  - $R_{th,Nx}$: N_1, N_2 thermal winding resistances
  - $R_{th,Cu-CC}$: acts between the copper cooling plate and the covered core part
  - $R_{th,CC}$: covered core part thermal resistance
  - $R_{th,Cu}$: thermal cooling plate resistance
  - $R_{th,N1-Cu}$: acts between N_1 and the copper cooling plate
  - $R_{th,N2-C}$: acts between N_2 and core
- Radiation and natural convection [51]
  - $R_{th,S-Am}$: acts between transformer surface and ambient

Furthermore, all losses are modelled by current sources. Fig. 2.11 shows a fully assembled transformer where thin copper plates with a thickness of 0.5 mm are used as heat bypasses to conduct the heat out of the

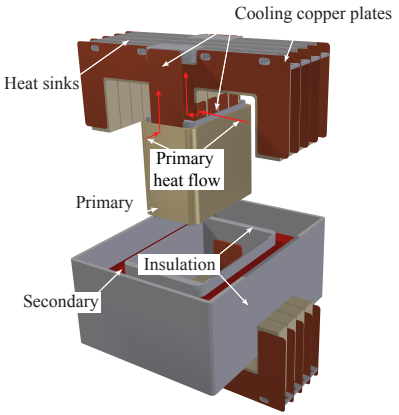


Figure 2.11: Fully assembled transformer with cooling plates used as heat bypass, conducting the primary losses out of the core towards the heat sinks and ambient. The marked insulation parts are also used as bobbins.

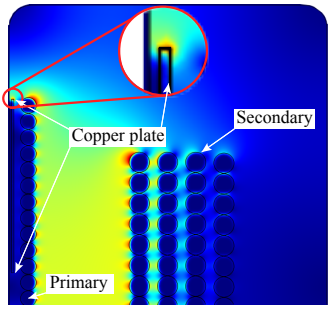


Figure 2.12: H-field exposition of a cooling copper plate in the transformer winding window at a current stimulation of 100 kHz simulated with FEM.

transformer and pass it either directly or through the heat sinks to ambient. There occur additional losses caused by the cooling copper plates but they are quite low (see Fig. 2.16 (a)). The copper plates are almost shielded by the primary winding and the plates are exposed to the H-field just at their upper edges, as it can be seen for one plate in Fig. 2.12.
Most of the thermal resistors used in Fig. 2.10 are well described in literature [51], but there exists a lack concerning the thermal winding

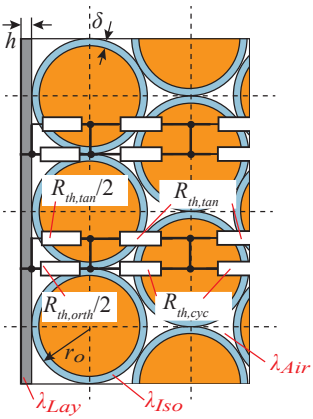


Figure 2.13: Cross section of a solid wire winding.

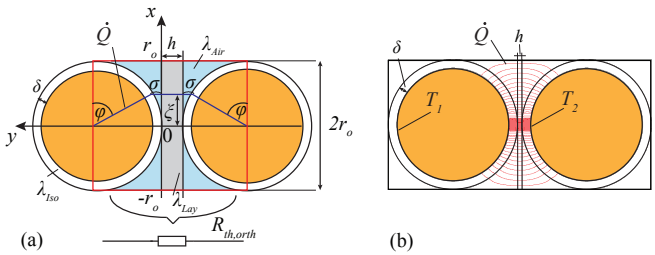


Figure 2.14: (a) Two orthogonal arranged wires with ideal assumed thermal heat flow lines. (b) Thermal heat flow between two wires simulated with FEM.

resistor $R_{th,Nx}$. A short explanation in the case of solid wire is given below, the full derivation of the thermal resistance of solid and litz wire can be found in [52]. Fig. 2.13 shows a typical solid wire winding containing different heat transition resistors.

First, a tangential part which represents the heat flow along the winding from layer to layer and second there are two different parts in radial direction. The tangential part can be easily calculated by

$$R_{th,tan} = \frac{l_W \cdot N_{pL}}{\lambda_{Cu} r_o^2 \pi k_L} \tag{2.19}$$

where N_{pL} is the number of turns per layer and l_W is the mean length per turn. In radial direction there exists an orthogonal part which is formed by both halves of the outer layers and an orthocyclic part which represents the heat transition in the inner winding layers. In orthogonal wire arrangements the wires in two neighbouring layers are laying directly side by side (see Fig. 2.14). The thermal resistance then is [52]

$$R_{th,orth} = \frac{1}{\left[\frac{2\lambda_{Air} l_W}{\alpha}\left(V + \frac{1}{8\lambda_{Iso}/\lambda_{Air}}\left(\frac{2\delta}{r_o}\right)^2 \frac{Z}{\alpha}\right)\right]} \tag{2.20}$$

with

$$V = \arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right)\frac{\beta}{\sqrt{\beta^2-1}} - \frac{\pi}{4} \tag{2.21}$$

$$Z = \frac{\beta\left(\beta^2-2\right)}{\left(\beta^2-1\right)^{3/2}} \arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right) - \frac{\beta}{2\,\beta^2-2} - \frac{\pi}{4} \tag{2.22}$$

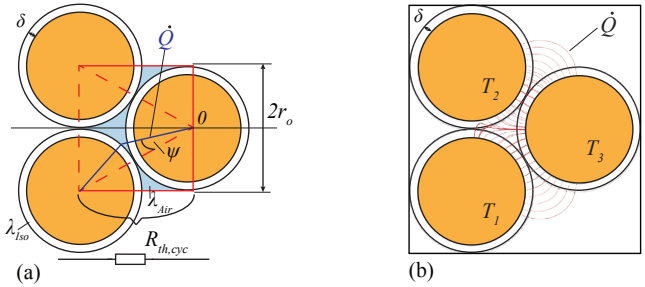


Figure 2.15: (a) Three orthocyclic arranged wires with ideal assumed thermal heat flow lines. (b) Thermal heat flow between three wires simulated with FEM.

and

$$\alpha = 1 - \frac{\delta}{r_o \lambda_{Iso}/\lambda_{Air}} \quad ; \quad \beta = \frac{1}{\alpha}\left(1 + \frac{h_Z}{2 r_o \lambda_{Lay}/\lambda_{Air}}\right). \tag{2.23}$$

In orthocyclic windings the wires in the neighbouring layers are laying directly in the gap of the previous layer (see Fig. 2.15). $R_{th,cyc}$ can be obtained as [52]

$$R_{th,cyc} = \frac{1}{\left[4\lambda_{Air} l_W \left(M_{Air} + M_{Iso}\left(\frac{\delta \lambda_{Air} r_o^2}{\lambda_{Iso}}\right)\left(r_o - \frac{\delta}{2}\right)\right)\right]} \tag{2.24}$$

with

$$M_{Air} = \int_0^{\frac{\pi}{6}} \frac{\cos^2\psi - \cos\psi\sqrt{\cos^2\psi - 0.75} - 0.5}{\left[\cos\psi - \alpha\left(\sqrt{\cos^2\psi - 0.75} + 0.5\right)\right]^2} d\psi \tag{2.25}$$

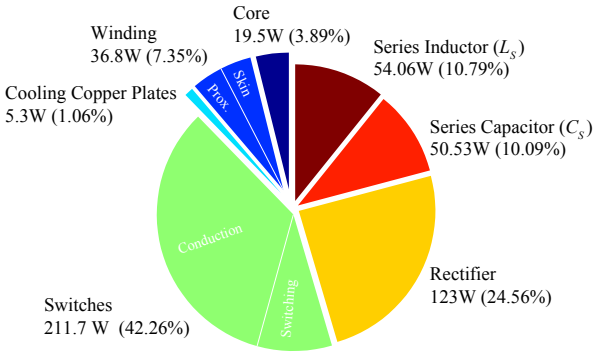
$$M_{Iso} = \int_0^{\frac{\pi}{6}} \frac{\sin^2\psi + \cos\psi\sqrt{\cos^2\psi - 0.75}}{\left[\cos\psi - \alpha\left(\sqrt{\cos^2\psi - 0.75} + 0.5\right)\right]^2} d\psi. \tag{2.26}$$

This finally leads to the general form of $R_{th,Nx}$

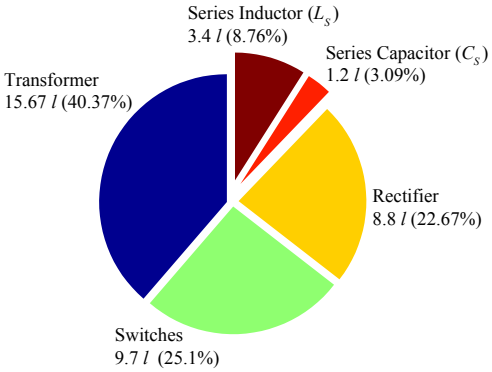
$$\begin{aligned} R_{th,Nx} = (R_{th,tan} || R_{th,cyc}) \frac{N_L - 1}{N_{pL}} + \\ + (R_{th,tan} || R_{th,orth}) \frac{1}{N_{pL}} \end{aligned} \quad . \tag{2.27}$$

2.1.4 Optimization results

Figure 2.16 and Tab. 2.3 sum up the results of a single SPRC-module optimization as well as the simulated pulse parameters and the final number of modules of the overall system. The major losses arise in the switches due to high conduction losses. Because of the much more complex structure of the transformer which results in more complicated



(a)



(b)

Figure 2.16: (a) Comparison of losses and (b) comparison of volume of a single SPRC-module.

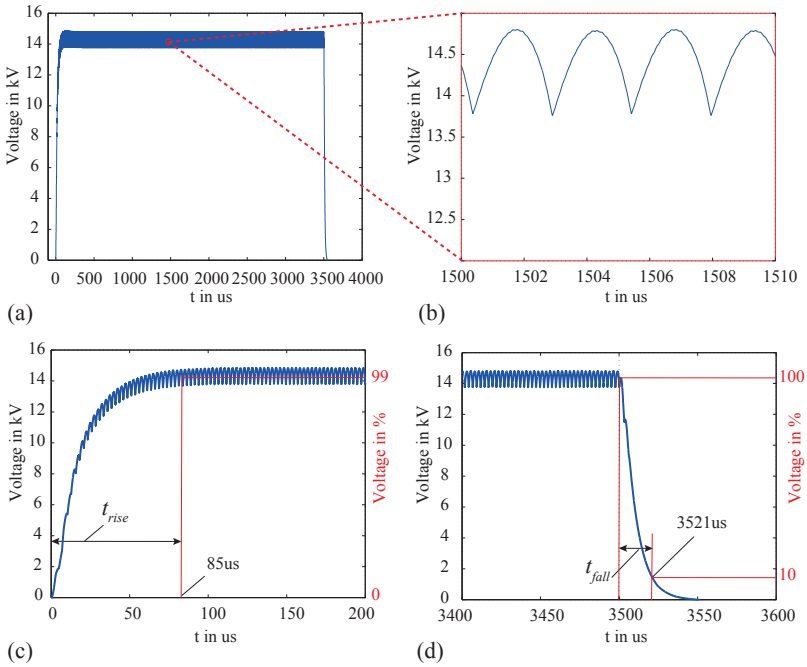


Figure 2.17: (a) Simulated pulse voltage V_{O11} of a single SPRC module, (b) pulse ripple at flat top, (c) pulse rise time and (d) pulse fall time.

cooling efforts, the volume of the transformer is significantly higher than that of the modulator switches (see Fig. 2.16 (a) and (b)). Comparing the given constraints in Tab. 2.2 with the results in Tab. 2.3 all values concerning temperatures, flux density, electrical field strengths, rise time, fall time and short circuit energy fulfill the limits. For the entire system 16 SPRC-modules are required. Fig. 2.17 (a) and Fig. 2.18 (a) show the simulated output voltage pulse V_{O11} of a single SPRC module and the pulse voltage V_K of the entire system which is formed by a stack of 2 single SPRC modules in parallel and 8 in series. Operating 8 SPRC stacks interleaved results in a much lower ripple with higher frequency components at the pulse flat top for the entire system than in the single module as can be seen by comparing Fig. 2.17 (b) and Fig. 2.18 (b). In both cases t_{rise} as well as t_{fall} stay quite below the

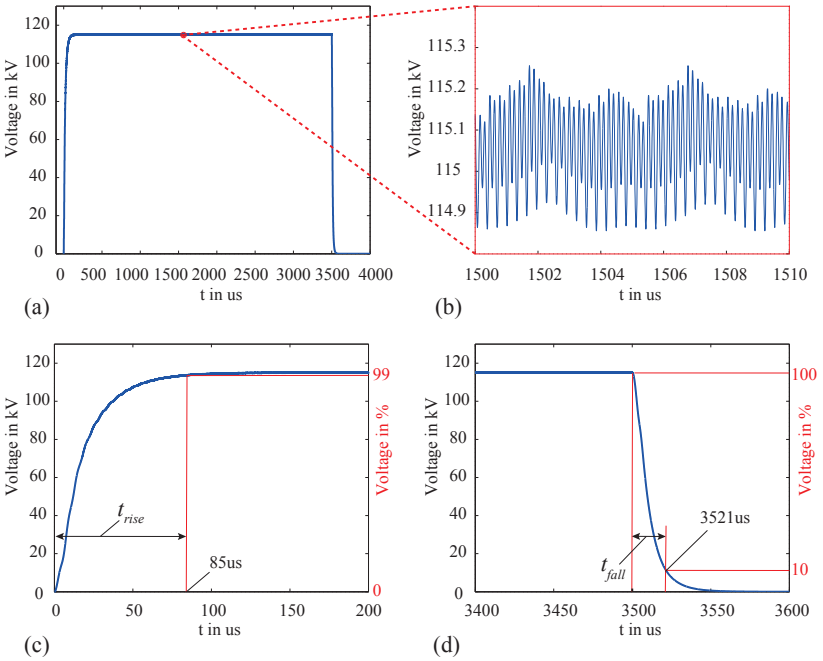
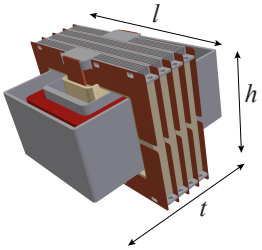


Figure 2.18: (a) Simulated pulse voltage V_K of the whole SPRC-system (stack of 2 single modules in parallel, 8 of these stacks in series), (b) pulse ripple at flat top, (c) pulse rise time and (d) pulse fall time.

given constraints in Tab. 2.2 (see Fig. 2.17 (c), (d) and Fig. 2.18 (c), (d)).

Table 2.3: Optimization results of a single SPRC-module and optimal number of modules.

Resonant Circuit					
$V_{OutPulsed}$	14.375 kV	L_S	5.1 μH	n	18
$I_{OutPulsed}$	12.5 A	C_S	0.837 μF		
$P_{OutPulsed}$	179.7 kW	C_P	2.58 nF		
# of capacitors for C_S				Type: SMD 2225	
896				C2225N153J102T	
# of capacitors for C_P				Type: SMD 2220	
624				C5750C0G2J104J280KC	
Semiconductors					
# of parallel switches				Type: MAX247	
5 x 4				STY139N65M5	
# of rectifier diodes				Type: SMD D^3PAK	
156				APT40DQ120SG	
Transformer					
# of cores				Type: Ferrite K2008	
16				U126/91/20	
Windings				Litz wire	
Primary	3			8 x 2000 x 0.05	
Secondary	54			3500 x 0.05	



Transformer dimensions	
t	26.4 cm
h	21.2 cm
l	28 cm
Temperatures	
T_1	93 °C
T_2	101.6 °C
T_3	67.1 °C
T_4	58.7 °C
Flux density	
B_{max}	150 mT
Electrical field strengths	
E_{max}	13.47 kV/mm
E_{avg}	5.75 kV/mm

Performance of a single module		
Volume	Pulsed power density	Efficiency
38.77 l	4.63 kW/l	94.7 %
t_{rise}	t_{fall}	
85 μs	21 μs	
Overall system		
t_{rise}	t_{fall}	Short circuit energy
85 μs	21 μs	3.7 J
# of SPRC-modules in parallel and series		2 x 8

2.1.5 Conclusions

Due to a large number of degrees of freedom (e.g. number of switches or geometric parameters of the transformer), an optimal straight forward design for the resonant converter system for a pulse modulator is difficult. Therefore, in this paper an optimization procedure is presented, which is based on an electrical and a thermal model of the SPRC converter. Additionally, an insulation design procedure for the transformer and a thermal model for the switches is provided. With this approach an optimal design for minimum losses is achieved. The overall system consists of a stack of 2 resonant converter modules connected in parallel. To build up the voltage up to 115 kV, 8 of these stacks are connected in series. The total number of modules is 16. Each single modulator module has 5 MOSFETs connected in parallel. The efficiency of a single SPRC-module is 94.7 % with a pulsed power density of 4.63 kW/l.

Acknowledgement

The authors would like to thank the project partner Ampegon AG very much for their strong support of the CTI-research project 13135.1 PFFLR-IW.

Note:

The presented optimization results in Tab. 2.3 are preliminary results. In order to achieve a higher safety margin, the number of semiconductor switches of the H-bridge is finally increased. The final optimization results are listed in chapter 5 in Tab. 5.2. Also, the presented design of the air toroid and the HV-HF transformer changed during the design process. The final toroid design is presented in chapter 5, whereas the final transformer design is presented in section 2.4.

2.2 General electrical model of the series parallel resonance converter

In this section, the governing steady-state equations of a single series parallel resonant converter basic module (SPRC-Bm) (in the literature also called LCC resonance converter) are presented. These analytical steady-state equations can then be easily implemented in the optimization algorithm for determining the resonant elements with respect to the calculated losses and the required output characteristics. Figure 2.19 shows the SPRC-Bm, which is formed by an H-bridge, the resonant tank with the series capacitor C_S, the series inductor L_S and the parallel capacitor C_P, the high-voltage, high-frequency transformer and the output rectifier stage with load and filter capacitor.
In the literature, the SPRC-Bm is often modeled by the fundamental mode approximation (FMA) method, also known as the first harmonic approximation (FHA) method, which is presented in [35] and [53]. There, all signals are considered with the first harmonic amplitude and the behaviour between the output rectifier, the output filter (pure capacitive or inductive-capacitive) and the load resistor are represented by an equivalent resistive element. A more accurate approach is derived in [45, 54] for pure capacitive output filters and in [55] for inductive-capacitive output filters. This more accurate method is known as e.g extended first harmonic approximation (eFHA), rectifier-compensated fundamental mode analysis (RCFMA) or rectifier-compensated first harmonic approximation (RCFHA). It is based on the FHA method,

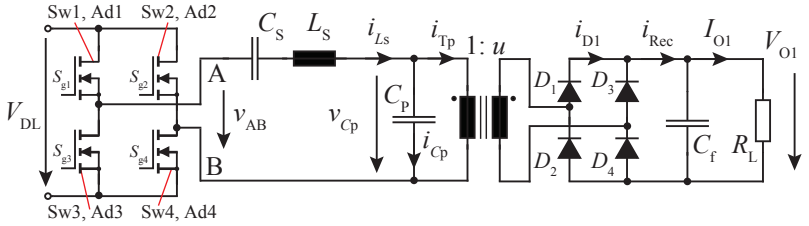


Figure 2.19: Single SPRC-Bm formed by a H-bridge, a resonant tank (with the series capacitor C_S, the series inductor L_S and the parallel capacitor C_P), a high-voltage, high-frequency transformer and the output rectifier stage with pure capacitive output filter and load.

but also considers the charging and discharging transitions of the parallel capacitance C_{P}. There, the output rectifier, the filter stage and the load are represented by an equivalent combination of a resistive-capacitive element. Further, in [56] and [57] the eFHA approach is applied in an iterative model refinement procedure. Although this approach results in slightly more accurate results than the FHA method, it is not further investigated due to the higher additional computational effort when used in an optimization procedure. The authors in [58–60] are also employing the eFHA method, but in combination with more detailed transformer models. They include the main inductance of the transformer or the transformer is modeled with a reluctance model. In the present case, the main inductance of the transformer is assumed to be far larger than the leakage inductance and can be therefore neglected in the following analysis.
Due to the fact that the FHA method is a special case of the eFHA method, the analysis is given first for the eFHA and afterwards the transition to the FHA method is derived.
In the following the analysis is given for a pure capacitive output filter. The analysis given next is derived based on the analysis from [54] and [35] under following assumptions:

- All components of the SPRC-Bm as e.g. the H-bridge switches and diodes, the rectifier diodes, the resonant tank elements and the transformer are considered as ideal.
- The value of the filter capacitor C_{f} (with respect to the primary side of the transformer) is much larger than the series capacitor C_{S} and the parallel capacitor C_{P}, $C_{\mathrm{f}} \gg C_{\mathrm{S}}$ and $C_{\mathrm{f}} \gg C_{\mathrm{P}}$.
- Due to filter effect of the resonant tank, the resonant current i_{Ls} is assumed to be sinusoidal.
- The SPRC-Bm is operated above resonance

2.2.1 SPRC-Bm extended first harmonic approximation (eFHA) method

The definitions of the used variables and components are given in Fig. 2.19 and Fig. 2.20, respectively. Figure 2.20 shows the basic signals of the resonant tank and the output rectifier of a single SPRC-Bm (see

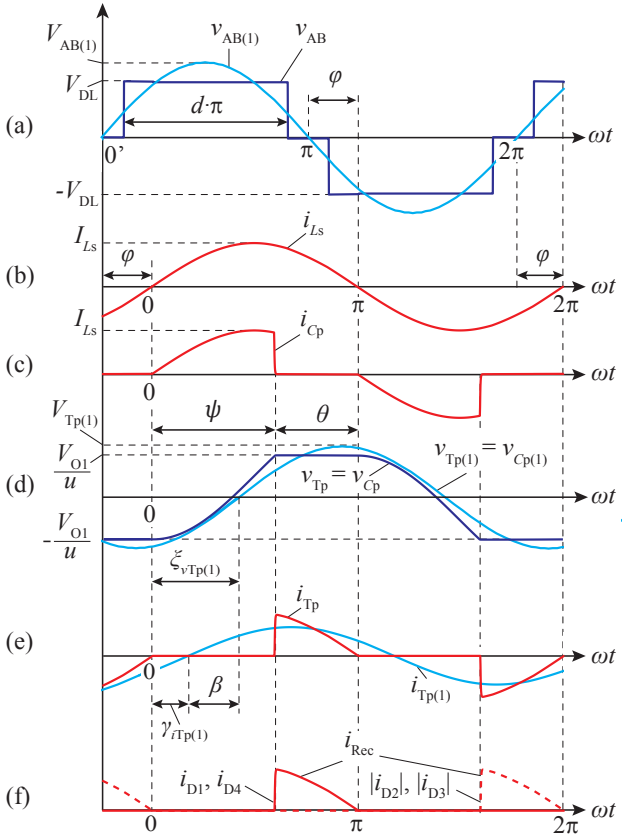


Figure 2.20: Basic signals of the resonant tank and the output rectifier of a single SPRC-Bm (see Fig. 2.19). (a) Full bridge output voltage v_{AB} with first harmonic $v_{\mathrm{AB}(1)}$. (b) Resonant current i_{Ls}. The angle φ represents the phase shift between the first harmonics of $v_{\mathrm{AB}(1)}$ and i_{Ls}. (c) Parallel capacitor current $i_{C\mathrm{p}}$. (d) Primary transformer voltage v_{Tp} and the first harmonic voltage $v_{\mathrm{Tp}(1)}$ with the first harmonic angle $\xi_{v\mathrm{Tp}(1)}$. The angles ψ and θ are the non-conduction angle and the conduction angle of the rectifier, respectively. (e) Primary transformer current i_{Tp} and the first harmonic current $i_{\mathrm{Tp}(1)}$ with the first harmonic angle $\gamma_{i\mathrm{Tp}(1)}$. The angle β is the angle between the first harmonics of the primary voltage $v_{\mathrm{Tp}(1)}$ and primary current $i_{\mathrm{Tp}(1)}$. (f) Output rectifier current i_{Rec}.

Fig. 2.19). Note: For the sake of simplicity, in the following analysis, the signals of Fig. 2.20 (b)-(f) are also defined from 0 and the phase shift angle φ is introduced then in the end of this section. The rectangular H-bridge output voltage $v_{\mathrm{AB}}(\omega t)$ (see Fig. 2.20 (a)), which is applied to the resonant tank, is given as

$$v_{\mathrm{AB}}(\omega t) = \begin{cases} 0 & 0' \leq \omega t < \frac{\pi}{2}(1-d) \\ V_{\mathrm{DL}} & \frac{\pi}{2}(1-d) \leq \omega t < \frac{\pi}{2}(1+d) \\ 0 & \frac{\pi}{2}(1+d) \leq \omega t < \pi + \frac{\pi}{2}(1-d) \\ -V_{\mathrm{DL}} & \pi + \frac{\pi}{2}(1-d) \leq \omega t < \pi + \frac{\pi}{2}(1+d) \\ 0 & \pi + \frac{\pi}{2}(1+d) \leq \omega t < 2\pi \end{cases} \tag{2.28}$$

where d is the duty cycle and V_{DL} is the DC-link voltage from Fig. 2.19. The almost sinusoidal resonant current i_{Ls} (see Fig. 2.20 (b)) is defined as

$$i_{Ls}(\omega t) = I_{Ls} \sin(\omega t) \tag{2.29}$$

For calculating the first harmonic voltage $v_{\mathrm{AB}(1)}$ of the H-bridge output voltage v_{AB}, the well known fourier series [61] is applied

$$S(\omega t) = \frac{a_{\mathrm{o}}}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t) + b_n \sin(n\omega t) \tag{2.30}$$

with

$$a_n = \frac{1}{\pi} \int_{0',0}^{2\pi} S(\omega t) \cos(n\omega t) \mathrm{d}(\omega t) \tag{2.31}$$

and

$$b_n = \frac{1}{\pi} \int_{0',0}^{2\pi} S(\omega t) \sin(n\omega t) \mathrm{d}(\omega t) \tag{2.32}$$

Because v_{AB} is an odd function, the coefficients $a_n, a_{\mathrm{o}} = 0$ and the first harmonic voltage $v_{\mathrm{AB}(1)}$ can be written as

$$v_{\mathrm{AB}(1)}(\omega t) = b_1 \sin(\omega t) = V_{\mathrm{AB}(1)} \sin(\omega t) \tag{2.33}$$

with the amplitude

$$V_{\mathrm{AB}(1)} = \frac{4}{\pi} V_{\mathrm{DL}} \sin\left(\frac{d\pi}{2}\right). \tag{2.34}$$

During the non-conduction interval ψ of the output rectifier, the resonant current i_{Ls} flows as i_{C_P} through the parallel capacitor C_P and charges the capacitor from $-V_{\mathrm{O1}}/u$ to V_{O1}/u, as can be seen in Fig. 2.20 (c) and Fig. 2.20 (d). The capacitor voltage v_{C_P} is derived by the integration of the current i_{C_P} in the interval $(0 \leq \omega t < \omega t')$ as

$$\begin{aligned} v_{C_\mathrm{P}}(0 \leq \omega t < \omega t') &= \frac{1}{\omega C_\mathrm{P}} \int_0^{\omega t'} I_{Ls} \sin(\omega t) \mathrm{d}(\omega t) + V_{C_\mathrm{P}}(0) = \\ &= \frac{I_{Ls}}{\omega C_\mathrm{P}} (1 - \cos(\omega t')) - \frac{V_{\mathrm{O1}}}{u} \end{aligned} \tag{2.35}$$

with the initial condition at $\omega t = 0$

$$V_{C_\mathrm{P}}(0) = -\frac{V_{\mathrm{O1}}}{u} \tag{2.36}$$

In the interval $(\pi \leq \omega t < \omega t')$ the capacitor voltage v_{C_P} is derived as

$$\begin{aligned} v_{C_\mathrm{P}}(\pi \leq \omega t < \omega t') &= \frac{1}{\omega C_\mathrm{P}} \int_\pi^{\omega t'} I_{Ls} \sin(\omega t) \mathrm{d}(\omega t) + V_{C_\mathrm{P}}(\pi) = \\ &= -\frac{I_{Ls}}{\omega C_\mathrm{P}} (1 + \cos(\omega t')) + \frac{V_{\mathrm{O1}}}{u} \end{aligned} \tag{2.37}$$

with the initial condition at $\omega t = \pi$

$$V_{C_\mathrm{P}}(\pi) = +\frac{V_{\mathrm{O1}}}{u} \tag{2.38}$$

For the sake of a well readability $\omega t'$ is substituted with ωt and finally, the capacitor voltage v_{C_P} can be written as

$$v_{C_\mathrm{P}}(\omega t) = \begin{cases} \dfrac{I_{Ls}}{\omega C_\mathrm{P}}(1 - \cos(\omega t)) - \dfrac{V_{\mathrm{O1}}}{u} & 0 \leq \omega t < \psi \\ +\dfrac{V_{\mathrm{O1}}}{u} & \psi \leq \omega t < \pi \\ -\dfrac{I_{Ls}}{\omega C_\mathrm{P}}(1 + \cos(\omega t)) + \dfrac{V_{\mathrm{O1}}}{u} & \pi \leq \omega t < \pi + \psi \\ -\dfrac{V_{\mathrm{O1}}}{u} & \pi + \psi \leq \omega t < 2\pi \end{cases} \tag{2.39}$$

The peak current I_{Ls} is calculated by first evaluating (2.35) at $\omega t = \pi - \theta = \psi$ and equating it with the parallel capacitor voltage at $\omega t = \pi - \theta = \psi$

$$V_{C_\mathrm{P}}(\pi - \theta) = V_{C_\mathrm{P}}(\psi) = +\frac{V_{\mathrm{O1}}}{u}. \tag{2.40}$$

and after some manipulations the peak resonant current I_{Ls} results in

$$I_{Ls} = \frac{2V_{O1}\omega C_P}{u(1+\cos(\theta))} = \frac{2V_{O1}\omega C_P}{u(1+\cos(\pi-\psi))} \tag{2.41}$$

During the conduction interval $\theta = \pi - \psi$, the resonant current i_{Ls} flows as primary transformer current i_{Tp} through the transformer and therefore also as i_{Rec} through the rectifier as depicted in Fig. 2.20 (e) and Fig. 2.20 (f). The rectifier current i_{Rec} is given as

$$i_{Rec}(\omega t) = \begin{cases} 0 & 0 \le \omega t < \psi \\ \dfrac{I_{Ls}}{u}\sin(\omega t) & \psi \le \omega t < \pi \\ 0 & \pi \le \omega t < \pi + \psi \\ -\dfrac{I_{Ls}}{u}\sin(\omega t) & \pi + \psi \le \omega t < 2\pi \end{cases} \tag{2.42}$$

The load current I_{O1} is the average current of the output rectifier current i_{Rec} during a switching period

$$I_{O1} = \frac{1}{\pi}\int_{\psi}^{\pi} i_{Rec}\,\mathrm{d}(\omega t) = \frac{I_{Ls}}{\pi u}(1+\cos(\psi)). \tag{2.43}$$

The non-conduction angle ψ of the rectifier (see Fig. 2.20 (d)) is given by inserting (2.41) into (2.43), using the relation $V_{O1} = R_L I_{O1}$ and solving for ψ results in

$$\begin{aligned} \psi = \pi - \theta = \pi - 2\arctan\left(\sqrt{\frac{\pi}{2}\frac{u^2}{\omega C_P R_L}}\right) = \\ = \arccos\left(\frac{\pi u^2 - 2\omega R_L C_P}{\pi u^2 + 2\omega R_L C_P}\right). \end{aligned} \tag{2.44}$$

The first harmonic primary transformer voltage peak value $V_{Tp(1)}$, which is equal to the voltage peak value V_{CP} of the parallel capacitor C_P, is derived by applying (2.139) on (2.39) with

$$V_{Tp(1)} = V_{Cp(1)} = \frac{V_{O1}}{u}k_v \tag{2.45}$$

and

$$k_v = \sqrt{a^2_{v_{CP}(1)} + b^2_{v_{CP}(1)}}. \tag{2.46}$$

The fourier coefficients are

$$a_{v_{\mathrm{CP}}(1)} = -\frac{2}{\pi}\left(\frac{\sin(\psi)\cos(\psi)-\psi}{(\cos(\psi)-1)}\right) \tag{2.47}$$

$$b_{v_{\mathrm{CP}}(1)} = \frac{2}{\pi}(\cos(\psi)+1). \tag{2.48}$$

The first harmonic transformer voltage angle $\xi_{v_{\mathrm{Tp}}(1)}$ is defined due to the sinusoidal spectral representation of the signal as [61]

$$\xi_{v_{\mathrm{Tp}}(1)} = \xi_{v_{\mathrm{CP}}(1)} = \arctan\left(\frac{a_{v_{\mathrm{CP}}(1)}}{b_{v_{\mathrm{CP}}(1)}}\right) = \arctan\left(\frac{\sin(\psi)\cos(\psi)-\psi}{\sin^2(\psi)}\right) \tag{2.49}$$

The primary transformer current i_{Tp} is defined as

$$i_{\mathrm{Tp}}(\omega t) = \begin{cases} 0 & 0 \le \omega t < \psi \\ I_{Ls}\sin(\omega t) & \psi \le \omega t < \pi \\ 0 & \pi \le \omega t < \pi+\psi \\ I_{Ls}\sin(\omega t) & \pi+\psi \le \omega t < 2\pi \end{cases} \tag{2.50}$$

Again, the first harmonic primary transformer current peak value $I_{\mathrm{Tp}(1)}$, is derived by applying (2.139) on (2.50), which results in

$$I_{\mathrm{Tp}(1)} = \sqrt{a^2_{i_{\mathrm{Tp}}(1)} + a^2_{i_{\mathrm{Tp}}(1)}} \tag{2.51}$$

with the fourier coefficients

$$a_{i_{\mathrm{Tp}}(1)} = -\frac{2V_{\mathrm{O1}}\omega C_{\mathrm{P}}}{\pi u}(\cos(\psi)+1) \tag{2.52}$$

$$b_{i_{\mathrm{Tp}}(1)} = -\frac{2V_{\mathrm{O1}}\omega C_{\mathrm{P}}}{\pi u}\left(\frac{\sin(\psi)\cos(\psi)-\psi+\pi}{(\cos(\psi)-1)}\right) \tag{2.53}$$

and the first harmonic transformer current angle $\gamma_{i_{\mathrm{Tp}}(1)}$ as

$$\gamma_{i_{\mathrm{Tp}}(1)} = \arctan\left(\frac{a_{i_{\mathrm{Tp}}(1)}}{b_{i_{\mathrm{Tp}}(1)}}\right) = -\arctan\left(\frac{\sin^2(\psi)}{\sin(\psi)\cos(\psi)-\psi+\pi}\right). \tag{2.54}$$

Since the first harmonic of the transformer current is leading the first harmonic of transformer voltage (see Fig. 2.20 (d) and Fig. 2.20 (e)), the output rectifier, the capacitive filter stage and the load can be modelled

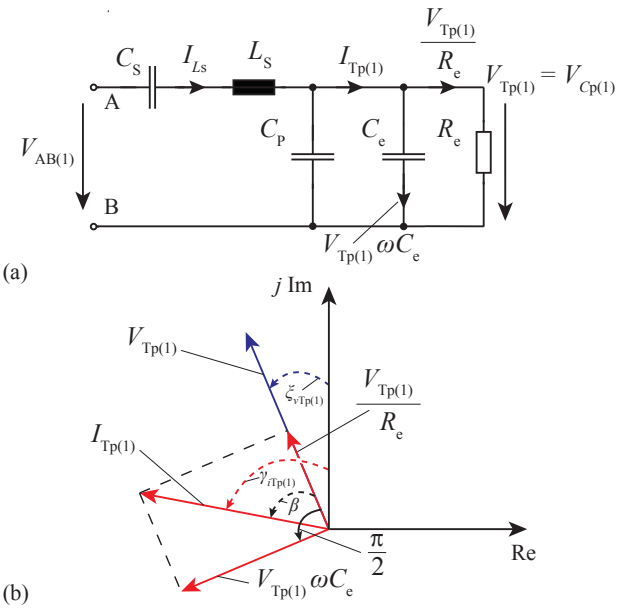


Figure 2.21: (a) Equivalent circuit of the SPRC-Bm from Fig. 2.19 and (b) vector diagram representation of the output rectifier according to the extended first harmonic approximation (eFHA).

by an equivalent capacitance C_e and an equivalent resistance R_e, as depicted in the equivalent eFHA circuit of the SPRC-Bm in Fig. 2.21 (a). The according vector diagram is shown in Fig. 2.21 (b), in which the enclosed angle β between $V_{Tp(1)}$ and $I_{Tp(1)}$ is given as

$$\beta = \xi_{v_{CP}(1)} - \gamma_{i_{Tp}(1)} \tag{2.55}$$

The equivalent resistance R_e is determined from the relationship

$$\frac{V_{O1}^2}{R_L} = \frac{\left(\frac{V_{Tp(1)}}{\sqrt{2}}\right)^2}{R_e} = \frac{{V_{Tp(1)}}^2}{2R_e} \tag{2.56}$$

Substituting (2.45) into (2.56) and solving for the equivalent resistor R_e, results in

$$R_e = R_L \frac{k_v^2}{2u^2}. \tag{2.57}$$

The equivalent capacitance C_e is obtained from the geometric relation in Fig. 2.21 (b) as

$$\tan(|\beta|) = \frac{V_{\mathrm{Tp}(1)}\omega C_\mathrm{e}}{\frac{V_{\mathrm{Tp}(1)}}{R_\mathrm{e}}} = \omega C_\mathrm{e} R_\mathrm{e}. \tag{2.58}$$

Substituting (2.57) into (2.58) and solving for the equivalent capacitance C_e, results in

$$C_\mathrm{e} = \frac{2u^2}{\omega R_\mathrm{L} k_\mathrm{v}^2}\tan(|\beta|). \tag{2.59}$$

The voltage ratio k_{21} is derived from the complex voltage divider, which is shown in Fig. 2.21 (a), as

$$k_{21} = \frac{V_{\mathrm{Tp}(1)}}{V_{\mathrm{AB}(1)}} = \\ = \frac{1}{\sqrt{\left\{1-\frac{C_\mathrm{P}}{C_\mathrm{S}}\left[\left(\frac{\omega}{\omega_\mathrm{S}}\right)^2-1\right]\left(1+\frac{C_\mathrm{e}}{C_\mathrm{P}}\right)\right\}^2+\left\{\frac{C_\mathrm{P}}{C_\mathrm{S}}\left[\left(\frac{\omega}{\omega_\mathrm{S}}\right)^2-1\right]\frac{1}{\omega C_\mathrm{P} R_\mathrm{e}}\right\}^2}} \tag{2.60}$$

with

$$\omega_\mathrm{S} = \frac{1}{\sqrt{L_\mathrm{S} C_\mathrm{S}}}. \tag{2.61}$$

Finally, the output-to-input voltage DC-DC transfer function M_V is obtained as

$$M_\mathrm{V} = \frac{V_{\mathrm{O1}}}{V_\mathrm{DL} u} = \frac{V_{\mathrm{AB}(1)}}{V_\mathrm{DL}}\frac{V_{\mathrm{Tp}(1)}}{V_{\mathrm{AB}(1)}}\frac{V_{\mathrm{O1}}}{V_{\mathrm{Tp}(1)} u} = \frac{4}{\pi}\sin\left(\frac{d\pi}{2}\right)\frac{k_{21}}{k_v} \tag{2.62}$$

and the SPRC-Bm output voltage is given as

$$V_{\mathrm{O1}} = \frac{4}{\pi} V_\mathrm{DL}\sin\left(\frac{d\pi}{2}\right)\frac{u}{k_v} k_{21}. \tag{2.63}$$

The input impedance of the shown equivalent eFHA circuit in Fig. 2.21 (a) is given as

$$\underline{Z}_{\mathrm{In}(1)} = |Z_{\mathrm{In}(1)}| e^{j\varphi} = \frac{V_{\mathrm{AB}(1)}}{I_{L\mathrm{s}}} e^{j\varphi} = \\ = j\omega L_\mathrm{S} - \frac{j}{\omega C_\mathrm{S}} + \frac{1}{\left(j\omega C_\mathrm{P} + j\omega C_\mathrm{e} + \frac{1}{R_\mathrm{e}}\right)} \tag{2.64}$$

and the angle φ, which represents the phase shift between the first harmonics $V_{\mathrm{AB}(1)}$ and I_{Ls} (see Fig. 2.19 (a) and Fig. 2.19 (b)) is derived from (2.64) as

$$\varphi = \arctan\left\{\frac{1}{\omega R_{\mathrm{e}} C_{\mathrm{S}}}\left[\left(\frac{\omega}{\omega_{\mathrm{S}}}\right)^2\left[1+\omega^2(C_{\mathrm{P}}+C_{\mathrm{e}})^2 R_{\mathrm{e}}^2\right]-1\right]+ \right. \\ \left. -[\omega(C_{\mathrm{P}}+C_{\mathrm{e}})R_{\mathrm{e}}]\left(1+\frac{C_{\mathrm{P}}+C_{\mathrm{e}}}{C_{\mathrm{S}}}\right)\right\}. \tag{2.65}$$

The resonance frequency f_{res} is determined by equating the imaginary part of (2.64) to zero

$$\Im(\underline{Z}_{\mathrm{In}(1)}) = 0 \tag{2.66}$$

and solving for the frequency results in the resonance frequency

$$f_{\mathrm{res}} = \frac{\omega_{\mathrm{S}}}{4\pi}\frac{\sqrt{2}}{A}\sqrt{\sqrt{B^2C_{\mathrm{S}}^2+2A^2\left(AR_{\mathrm{e}}+L_{\mathrm{S}}\right)C_{\mathrm{S}}+A^4}+BC_{\mathrm{S}}+A^2} \tag{2.67}$$

with

$$A = (C_{\mathrm{P}}+C_{\mathrm{e}})R_{\mathrm{e}} \quad \text{and} \quad B = AR_{\mathrm{e}} - L_{\mathrm{S}} \tag{2.68}$$

2.2.2 SPRC-Bm first harmonic approximation (FHA) method

Although, the FHA method is presented earlier in the literature than the eFHA method, the FHA method can be seen as a special case of the eFHA method. Therefore, the FHA method is derived from the eFHA method. Figure 2.23 shows the basic waveforms of a SPRC-Bm according to the FHA method.

The major simplification of the FHA method is the assumption that the transformer voltage v^*_{Tp} is a perfect rectangle and the non-conduction interval of the rectifier $\psi = 0$. Hence, the primary transformer current i^*_{Tp} is assumed to be equal to the resonant current i^*_{Ls}, which results in a zero phase shift between the first harmonic of the transformer primary voltage $v^*_{\mathrm{Tp}(1)}$ and the primary transformer current i^*_{Tp} (see Fig. 2.23 (b) and Fig. 2.23 (c)). Therefore, the behaviour of the rectifier, the filter stage and the load can be modelled in an equivalent ohmic resistance R^*_{e}, as can be seen in Fig. 2.22. The same equation as for the eFHA can be used for the first harmonic of the H-bridge output voltage $V_{\mathrm{AB}(1)}$ (2.34) (compare Fig. 2.20 (a) with Fig. 2.23 (a)). Applying $\psi = 0$ in (2.45)

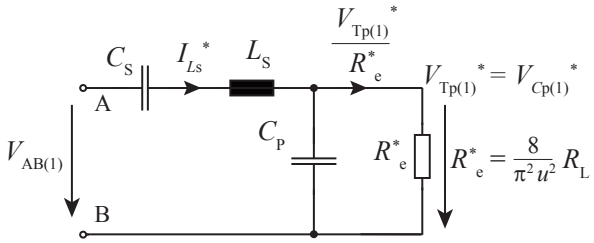


Figure 2.22: Equivalent circuit of the SPRC-Bm from Fig. 2.19 according to the first harmonic approximation (FHA).

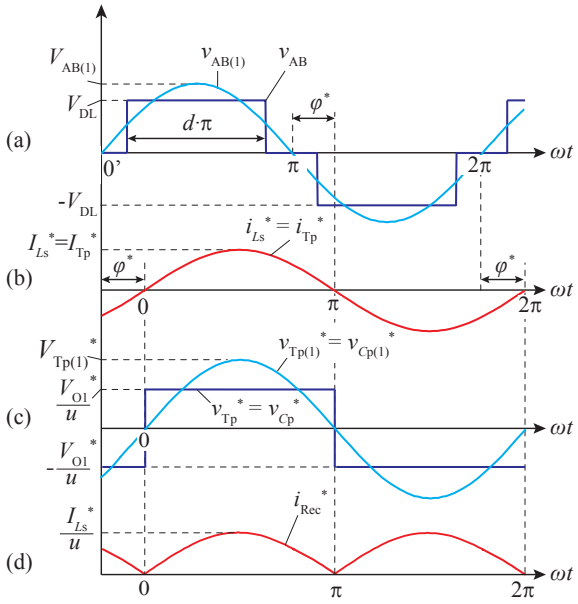


Figure 2.23: Basic signals of the resonant tank and the output rectifier of a single SPRC-Bm (see Fig. 2.19) according to the first harmonic order approach (FHA). The signal in (a) is the same as in Fig. 2.20 (a). (a) Full bridge output voltage v_{AB} with first harmonic $v_{AB(1)}$. (b) Resonant current i_{Ls}^*. The angle φ^* represents the phase shift between the first harmonics of $v_{AB(1)}$ and i_{Ls}^*. (c) Primary transformer voltage v_{Tp}^* and the first harmonic voltage $v_{Tp(1)}^*$. (d) Output rectifier current i_{Rec}^*.

and (2.46) results for the first harmonic of the primary transformer voltage in

$$V_{\mathrm{Tp(1)}}{}^{*} = \frac{V_{\mathrm{O1}}{}^{*}}{u} k_{\mathrm{v}}^{*} \tag{2.69}$$

with

$$k_{\mathrm{v}}^{*} = \frac{4}{\pi} \tag{2.70}$$

Reintroducing the relation of (2.56) gives

$$\frac{V_{\mathrm{O1}}^{2}{}^{*}}{R_{\mathrm{L}}} = \frac{\left(\frac{V_{\mathrm{Tp(1)}}{}^{*}}{\sqrt{2}}\right)^{2}}{R_{\mathrm{e}}^{*}} = \frac{V_{\mathrm{Tp(1)}}{}^{*2}}{2R_{\mathrm{e}}^{*}} \tag{2.71}$$

and by substituting (2.69) into (2.71), the effective resistance is obtained as

$$R_{\mathrm{e}}^{*} = R_{\mathrm{L}} \frac{k_{\mathrm{v}}^{*2}}{2u^{2}} = R_{\mathrm{L}} \frac{8}{\pi^{2} u^{2}} \tag{2.72}$$

The voltage ratio $k_{21}{}^{*}$ is derived from the voltage divider depicted in Fig. 2.22

$$k_{21}{}^{*} = \frac{V_{\mathrm{Tp(1)}}{}^{*}}{V_{\mathrm{AB(1)}}} = \\ = \frac{1}{\sqrt{\left(1 + \frac{C_{\mathrm{P}}}{C_{\mathrm{S}}}\right)^{2} \left(1 - \frac{\omega^{2}}{\omega_{0}{}^{2}}\right)^{2} + \frac{1}{Q_{\mathrm{L}}{}^{2}} \left[\frac{\omega}{\omega_{0}} - \frac{\omega_{0} \frac{C_{\mathrm{P}}}{C_{\mathrm{S}}}}{\omega \left(1 + \frac{C_{\mathrm{P}}}{C_{\mathrm{S}}}\right)}\right]^{2}}} \tag{2.73}$$

with

$$\omega_{0} = \left(\sqrt{\frac{L_{\mathrm{S}} C_{\mathrm{S}} C_{\mathrm{P}}}{C_{\mathrm{P}} + C_{\mathrm{S}}}}\right)^{-1} \tag{2.74}$$

and

$$Q_{\mathrm{L}} = \frac{R_{\mathrm{e}}^{*}}{\omega_{0} L_{\mathrm{S}}}. \tag{2.75}$$

Finally, applying (2.70) and (2.2.2) in (2.62) results in the output-to-input DC-DC voltage transfer function

$$M_{\mathrm{V}}^{*} = \frac{V_{\mathrm{O1}}{}^{*}}{V_{\mathrm{DL}} u} = \frac{V_{\mathrm{AB(1)}}}{V_{\mathrm{DL}}} \frac{V_{\mathrm{Tp(1)}}{}^{*}}{V_{\mathrm{AB(1)}}} \frac{V_{\mathrm{O1}}^{*}}{V_{\mathrm{Tp(1)}}{}^{*} u} = \frac{4}{\pi} \sin\left(\frac{d\pi}{2}\right) \frac{k_{21}{}^{*}}{k_{v}{}^{*}} \tag{2.76}$$

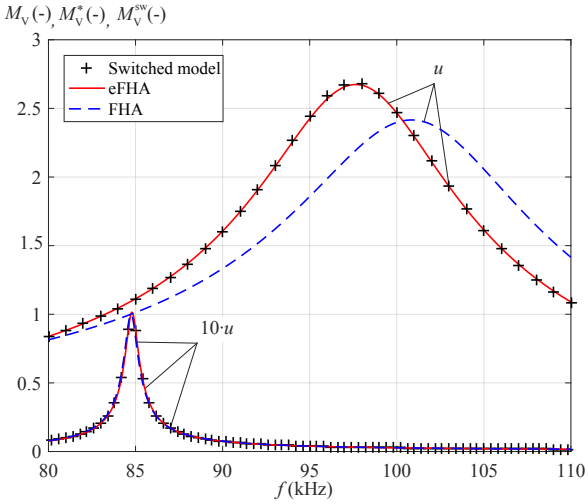


Figure 2.24: Comparison of the output-to-input DC-DC voltage transfer functions between the switched model (black crosses) M_V^{sw}, the eFHA (solid red lines) M_V and the FHA (dashed blue lines) M_V^* methods for different transformer ratios u.

and the SPRC-Bm output voltage is given as

$$V_{O1}^* = \frac{4}{\pi} V_{DL} \sin\left(\frac{d\pi}{2}\right) \frac{u}{{k_v}^*} {k_{21}}^* \tag{2.77}$$

A comparison between the DC-DC voltage transfer functions of a switched reference SPRC-Bm (circuit simulator model) (M_V^{sw}), the FHA method (M_V^*) and the eFHA method (M_V), is shown in Fig. 2.24 for different transformer ratios u. The higher the transformer ratio u, the lower is the non-conduction angle ψ (see (2.44)) and the lower is the resulting difference between the switched reference SPRC-Bm, the FHA method and eFHA method. Whereas, for small transformer ratios, respectively large conduction angles ψ, a high deviation occurs between the reference system and the FHA method, but still a high match between the switched system and the eFHA method is achieved, as can be seen in Fig. 2.24. A detailed comparison between the FHA method and the eFHA method, applied for resonant systems, is also given in [62–64], which confirms the presented results additionally. Therefore, only the

Table 2.4: Component values and input values of a single SPRC-Bm (see Fig. 2.19) used for the results depicted in Fig. 2.24, Fig. 2.25, Fig. 2.26, Fig. 2.27, Fig. 2.29 and Fig. 2.28 .

L_S (µH)	C_S (nF)	C_P (µF)	C_f (nF)	R_L (Ω)	V_{DL} (V)	d (−)	u (−)
4.2	840	1.716	429	1000	400	1	20

eFHA method is applied for all following calculations in this thesis. The used component and input values, for the comparison, are listed in Tab. 2.4.
In order to study the behavior of the DC-DC voltage transfer function M_V and the resonant peak current I_{Ls} of the SPRC-Bm, a component variation of the resonant tank elements L_S (see Fig. 2.25), C_S (see Fig. 2.26), C_P (see Fig. 2.27), the transformer ratio u (see Fig. 2.28) and the load R_L (see Fig. 2.29), is carried out. The nominal values are taken from Tab. 2.4. It can be seen that a change in the series inductor L_S or the series capacitor C_S leads to a large shift of the resonant frequency in the transfer function M_V and the current I_{Ls}. Whereas, the change of the parallel capacitor C_P, the transformer ratio u or the load R_L, results in a comparably higher increase or decrease of the resonant peak of the transfer function M_V and/or the current I_{Ls}, rather than in a change of the resonant frequency. Another important conclusion is that an increasing or decreasing of the load R_L does not lead to a linear increase or decrease of the resonant current I_{Ls}, which is especially important if SPRC-Bms are connected in parallel/series or for loss estimations.

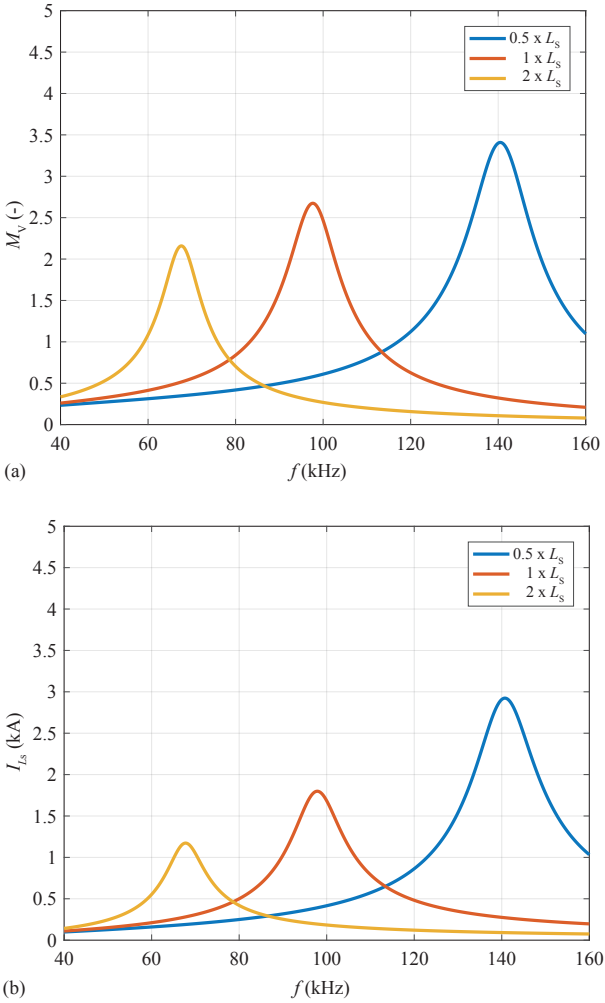


Figure 2.25: (a) DC-DC voltage transfer functions M_V (according to (2.62)) over the switching frequency f, given for different series inductors L_S. (b) First harmonic peak resonant currents I_{Ls} (according to (2.41)) over the switching frequency f, given for different series inductors L_S.

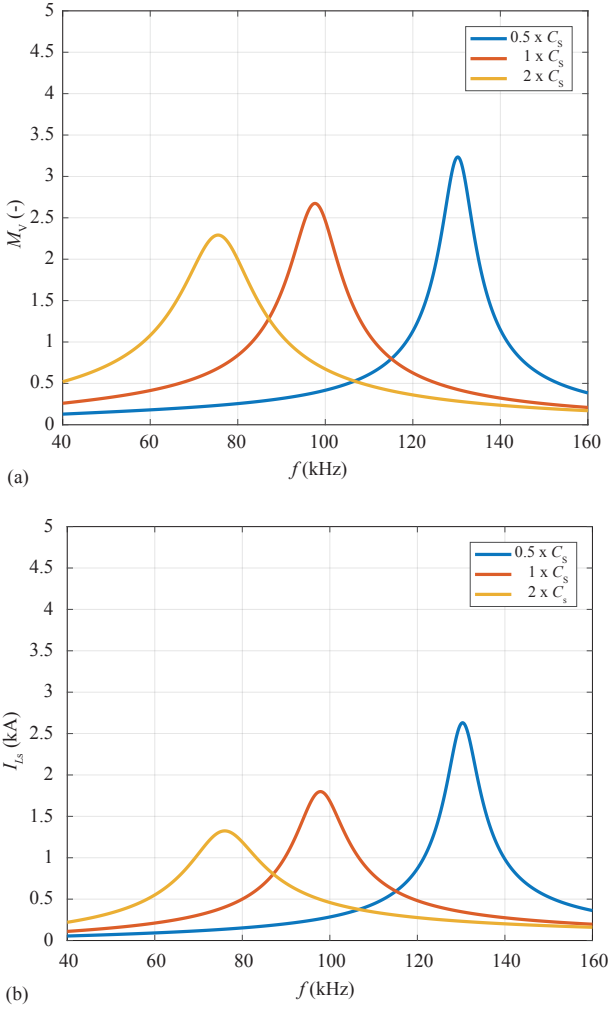


Figure 2.26: (a) DC-DC voltage transfer functions M_V (according to (2.62)) over the switching frequency f, given for different series capacitors C_S. (b) First harmonic peak resonant currents I_{Ls} (according to (2.41)) over the switching frequency f, given for different series capacitors C_S.

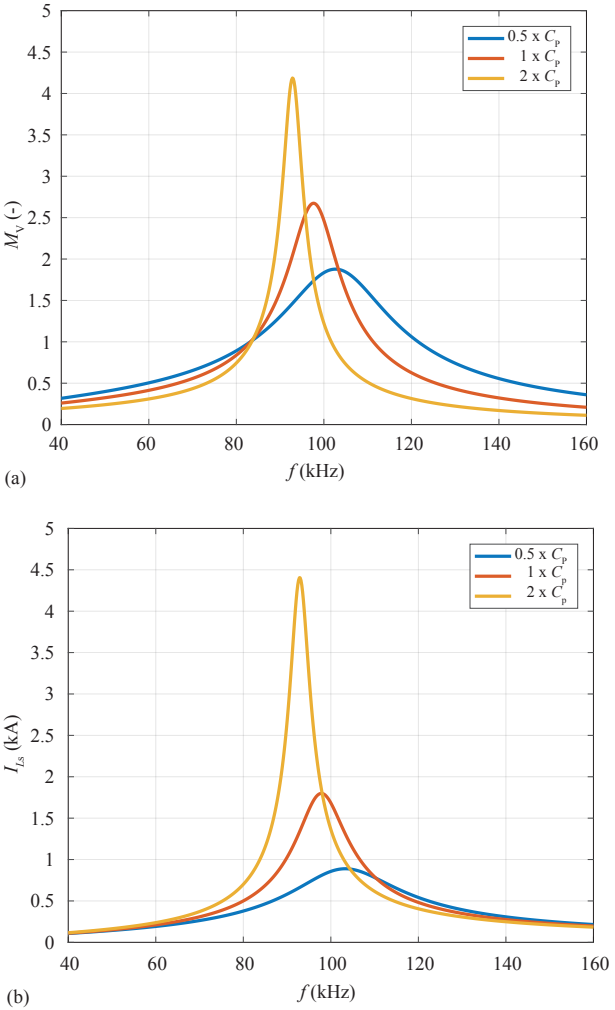


Figure 2.27: (a) DC-DC voltage transfer functions M_V (according to (2.62)) over the switching frequency f, given for different parallel capacitors C_P. (b) First harmonic peak resonant currents I_{Ls} (according to (2.41)) over the switching frequency f, given for different parallel capacitors C_P.

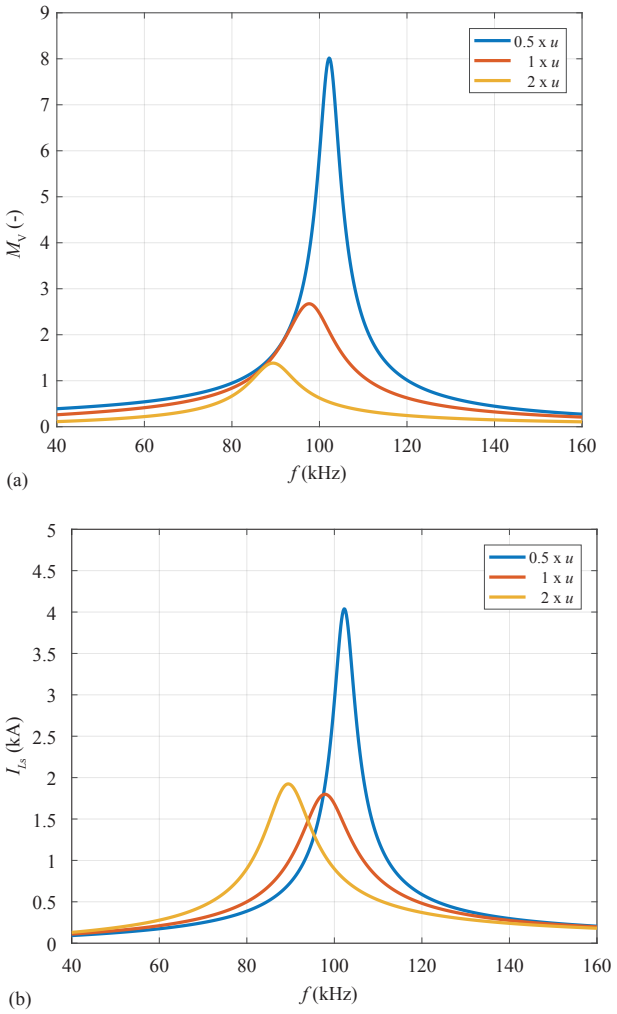


Figure 2.28: (a) DC-DC voltage transfer functions M_V (according to (2.62)) over the switching frequency f, given for different transformer ratios u. (b) First harmonic peak resonant currents I_{Ls} (according to (2.41)) over the switching frequency f, given for different transformer ratios u.

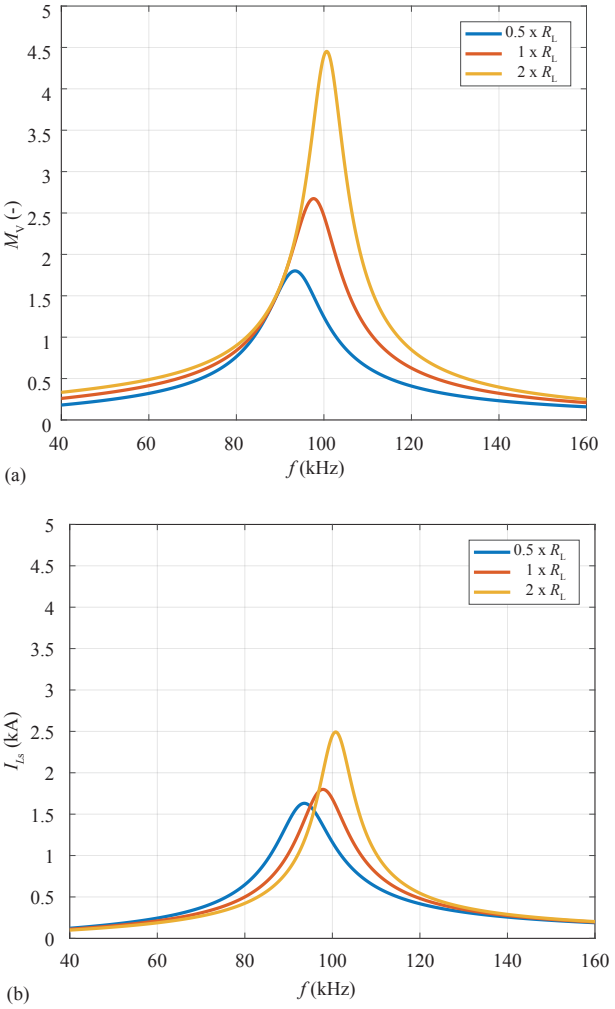


Figure 2.29: (a) DC-DC voltage transfer functions M_{V} (according to (2.62)) over the switching frequency f, given for different load resistors R_{L}. (b) First harmonic peak resonant currents I_{Ls} (according to (2.41)) over the switching frequency f, given for different load resistors R_{L}.

A discussion of the H-bridge and the output rectifier signals is given as follows.

2.2.3 SPRC-Bm H-bridge and output rectifier analysis

The SPRC topology naturally enables zero voltage switching (ZVS), if it is operated above the resonance frequency f_{res}. The voltage v_{AB} is leading the current i_{Ls}, which can be seen in Fig. 2.30 (a) and Fig. 2.30 (b). The currents conducted by the H-bridge switches Sw1 - Sw4 and their anti-parallel diodes Ad1 - Ad4 are depicted in Fig. 2.30 (d) to Fig. 2.30 (g). The according switching signals $S_{\mathrm{g1}} - S_{\mathrm{g4}}$ are shown in Fig. 2.30 (c). The general switching cycle is described next. Starting at 0', the current is conducted by Ad1 and Sw2. It is possible to turn-on Sw1 under ZVS, until the current crosses zero at 0. At the angle ωt_1, Sw2 is turned-off hard, the current commutates to Ad4 and Sw4 can be also turned-on under ZVS until the current crosses zero at 0. Between the zero crossing of the current at 0 and the angle ωt_2, the current flows through Sw1 and Sw4. At the angle ωt_2, Sw1 is turned-off hard, the current commutates to Ad3 and during the angle α, Sw3 can be turned-on under ZVS conditions. At the angle ωt_3, Sw4 is turned-off hard and the current commutates to Ad2. Now, during σ, Sw2 can be turned-on with ZVS conditions. Between the zero crossing of the current at π and the angle ωt_4, the current flows through Sw2 and Sw3. At the angle ωt_4, Sw3 is turned-off hard, the current commutates to Ad1 and during the angle α, Sw1 can be turned-on under ZVS conditions. The switching cycle is restarted at the angle ωt_5.

Note that only the turn-off of the switches is forced by the driver, whereas the turn-on of the switches is forced by the turn-off of the opposite switch of the bridge leg. No turn-on switching losses occur in the switches, if they are turned on during the ZVS intervals α and σ. The angle α is given as

$$\alpha = \frac{\pi}{2}(1-d) + \varphi. \tag{2.78}$$

and the angle σ as

$$\sigma = \varphi - \frac{\pi}{2}(1-d). \tag{2.79}$$

The angle σ indicates the maximal possible duration, in which ZVS can be achieved for all switches of the H-bridge, if the same interlocking

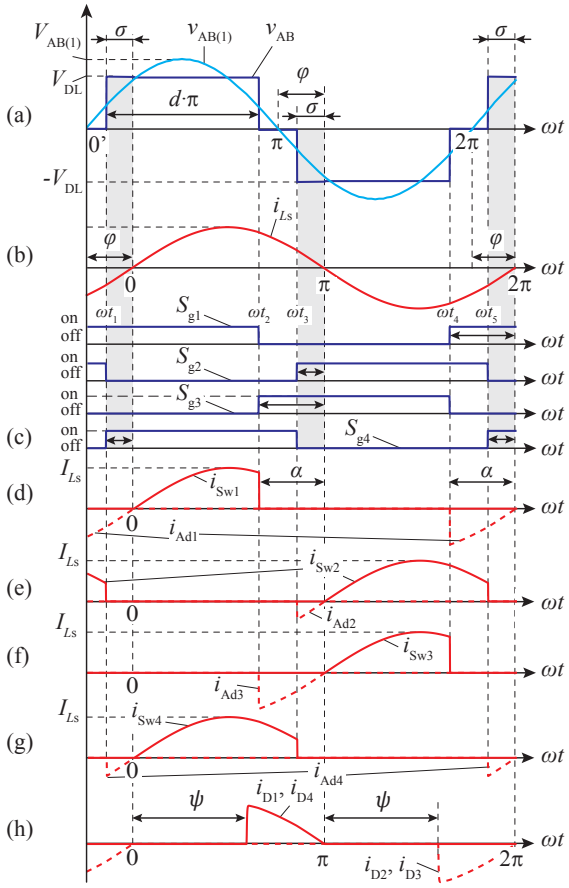


Figure 2.30: Basic H-bridge and output rectifier signals of a single SPRC-Bm (see Fig. 2.19). The signals in (a) and (b) are the same as in Fig. 2.20 (a). (a) Full bridge output voltage v_{AB} with first harmonic $v_{AB(1)}$. (b) Resonant current i_{Ls}. The angle φ represents the phase shift between the first harmonics of $v_{AB(1)}$ and i_{Ls}. (c) Switching signals $S_{g1} - S_{g4}$. (d) - (g) Current waveforms of the H-bridge switches Sw1 - Sw4 and their anti-parallel diodes Ad1 - Ad4 and (h) currents $i_{D1} - i_{D4}$ of the output rectifier diodes. The angle ψ is the non-conduction angle of the rectifier, whereas the angles σ and α indicate the durations, in which zero voltage switching (ZVS) can be achieved in the switches.

times are implemented for all them. The influences of the duty cycle d and the component tolerances of the resonant tank on the possible the ZVS range is investigated in section 4.1.3. The anti-parallel diodes are conducting the current and the voltage across the switches is zero, except the negligible low forward voltage of the anti-parallel diodes. Therefore, the switches can be turned-on with zero voltage before conducting forward current, as can be seen in Fig. 2.30 (e) to (g). The ZVS condition is fulfilled until the current through the anti-parallel diodes crosses the zero line. The switching losses (reverse recovery losses) of the anti-parallel diodes are assumed also to be negligible, because the diodes turn-off at a very low di/dt and the available turn-off time (reverse recovery time) is equal to the conduction time of the parallel switch before forward voltage is applied to the anti-parallel diodes [35]. These facts enable the comparable slow MOSFET body-train diode to be used as free wheeling diode. However, there occur losses during the hard turn-off transition of the switches, which can be reduced by employing lossless snubber capacitors in parallel to the switches and introducing a interlocking time in the switching signals [65]. In addition, the output capacitances of the switches and the anti-parallel diodes do not lead to switching losses [37].The output rectifier current is shown in Fig. 2.30 (h). Again, due to the low di/dt, small reverse recovery losses will occur and for further reduction of these losses, ultra fast soft recovery diodes are used for the output rectifier.
The equations of the SPRC-Bm H-bridge and the output rectifier current waveforms, which are used for calculating the losses of the applied semiconductors, as well as for the resonant tank components and the high-voltage high-frequency transformer, are given in the following. The currents through the switches Sw1 and Sw2 are defined as

$$i_{\mathrm{Sw1}}(\omega t) = \begin{cases} I_{Ls}\sin(\omega t) & 0 \leq \omega t < \pi - \alpha \\ 0 & \pi - \alpha \leq \omega t < 2\pi \end{cases} \tag{2.80}$$

and

$$i_{\mathrm{Sw2}}(\omega t) = \begin{cases} 0 & 0 \leq \omega t < \pi \\ -I_{Ls}\sin(\omega t) & \pi \leq \omega t < 2\pi - \sigma \\ 0 & 2\pi - \sigma \leq \omega t < 2\pi \end{cases} \tag{2.81}$$

The currents through the anti-parallel diodes Ad1 and Ad2 are defined as

$$i_{\mathrm{Ad1}}(\omega t) = \begin{cases} 0 & 0 \leq \omega t < 2\pi - \alpha \\ I_{Ls} \sin(\omega t) & 2\pi - \alpha \leq \omega t < 2\pi \end{cases} \tag{2.82}$$

and

$$i_{\mathrm{Ad2}}(\omega t) = \begin{cases} 0 & 0 \leq \omega t < \pi - \sigma \\ -I_{Ls} \sin(\omega t) & \pi - \sigma \leq \omega t < \pi \\ 0 & \pi \leq \omega t < 2\pi \end{cases} \tag{2.83}$$

The definitions of the currents through the other switches Sw3 and Sw4, as well as for the anti-parallel diodes Ad3 and Ad4, are the same as for the switches Sw1 and Sw2, respectively the anti-parallel diodes Ad1 and Ad2, but shifted by π (compare Fig. 2.30 (d) and (e) with Fig. 2.30 (f) and (g)). The currents through the output rectifier diodes (see Fig. 2.19 and Fig. 2.30 (h)) are defined as

$$i_{\mathrm{D1,4}}(\omega t) = \begin{cases} 0 & 0 \leq \omega t < \psi \\ \dfrac{I_{Ls}}{u} \sin(\omega t) & \psi \leq \omega t < \pi \\ 0 & \pi \leq \omega t < 2\pi \end{cases} \tag{2.84}$$

and

$$i_{\mathrm{D2,3}}(\omega t) = \begin{cases} 0 & 0 \leq \omega t < \pi + \psi \\ \dfrac{I_{Ls}}{u} \sin(\omega t) & \pi + \psi \leq \omega t < 2\pi \end{cases} \tag{2.85}$$

For calculating the losses, the root mean square (RMS) and the average current formulations are derived in the following. The RMS currents of the switches can be obtained as

$$\begin{aligned} I_{\mathrm{Sw1,3,RMS}} =& \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_{\mathrm{Sw1,3}}^2(\omega t) \mathrm{d}(\omega t)} = \\ =& \frac{I_{Ls}}{2} \sqrt{\frac{\cos(\alpha) \sin(\alpha) + \pi - \alpha}{\pi}} \end{aligned} \tag{2.86}$$

and

$$\begin{aligned} I_{\mathrm{Sw2,4,RMS}} =& \sqrt{\frac{1}{2\pi} \int_0^{2\pi} i_{\mathrm{Sw2,4}}^2(\omega t) \mathrm{d}(\omega t)} = \\ =& \frac{I_{Ls}}{2} \sqrt{\frac{\cos(\sigma) \sin(\sigma) + \pi - \sigma}{\pi}}. \end{aligned} \tag{2.87}$$

The anti-parallel diode RMS currents are given as

$$\begin{aligned} I_{\mathrm{Ad1,3,RMS}} =& \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{Ad1,3}}^2(\omega t)\mathrm{d}(\omega t)} = \\ =& \frac{I_{Ls}}{2}\sqrt{\frac{\alpha - \cos(\alpha)\sin(\alpha)}{\pi}} \end{aligned} \tag{2.88}$$

and

$$\begin{aligned} I_{\mathrm{Ad2,4,RMS}} =& \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{Ad2,4}}^2(\omega t)\mathrm{d}(\omega t)} = \\ =& \frac{I_{Ls}}{2}\sqrt{\frac{\sigma - \cos(\sigma)\sin(\sigma)}{\pi}}. \end{aligned} \tag{2.89}$$

The average anti-parallel diode currents are calculated as

$$I_{\mathrm{Ad1,3,avg}} = \frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{Ad1,3}}(\omega t)\mathrm{d}(\omega t) = \frac{I_{Ls}}{2\pi}(\cos(\alpha) - 1) \tag{2.90}$$

and

$$I_{\mathrm{Ad2,4,avg}} = \frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{Ad2,4}}(\omega t)\mathrm{d}(\omega t) = \frac{I_{Ls}}{2\pi}(\cos(\sigma) - 1). \tag{2.91}$$

The output rectifier currents are derived as

$$\begin{aligned} I_{\mathrm{D1\text{-}4,RMS}} =& \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{D1\text{-}4}}^2(\omega t)\mathrm{d}(\omega t)} = \\ =& \frac{I_{Ls}}{2u}\sqrt{\frac{\cos(\psi)\sin(\psi) + \pi - \psi}{\pi}} \end{aligned} \tag{2.92}$$

and

$$I_{\mathrm{D1\text{-}4,avg}} = \frac{1}{2\pi}\int_0^{2\pi} i_{\mathrm{D1\text{-}4}}(\omega t)\mathrm{d}(\omega t) = \frac{I_{Ls}}{2\pi u}(1+\cos(\psi)) = \frac{I_{\mathrm{O1}}}{2} \tag{2.93}$$

The momentary turn-off currents of the switches are defined as

$$I_{\mathrm{OFF,Sw1,3}} = I_{Ls}\sin(\sigma) \tag{2.94}$$

and

$$I_{\mathrm{OFF,Sw2,4}} = I_{Ls}\sin(\alpha). \tag{2.95}$$

The determination of the SPRC-Bm component losses, based on the before derived current equations, is presented in the next section.

2.2.4 SPRC-Bm component losses

For calculating the losses in each SPRC-Bm component, simplified fast models are applied, in order to reduce the computational effort, when used in the optimization procedure.

2.2.4.1 Anti-parallel H-bridge diodes

The conduction losses in each anti-parallel diode of the H-bridge can be estimated by [66]

$$P_{\mathrm{Con,Ad}} = R_{\mathrm{d}} I^2_{\mathrm{Ad,RMS}} + V_{\mathrm{F}} |I_{\mathrm{Ad,avg}}|. \tag{2.96}$$

where V_{F} and R_{d} are the forward voltage droop and the differential resistance, which can be taken from the data sheet for a specified operation point.

2.2.4.2 Switches (MOSFETs)

The conduction losses in each switch of the H-bridge switches is given by

$$P_{\mathrm{Con,Sw}} = I^2_{\mathrm{Sw,RMS}} \cdot R_{\mathrm{DS,On}} \tag{2.97}$$

and the hard-switched turn-off losses are estimated as [65]

$$P_{\mathrm{OFF}} = f \cdot V_{\mathrm{DS}} \cdot I_{\mathrm{OFF,Sw}} \left(\frac{t_{\mathrm{r}}}{3} + \frac{t_{\mathrm{f}}}{2} \right) \tag{2.98}$$

where the drain-source on-state resistance $R_{\mathrm{DS,On}}$, the drain-source voltage V_{DS}, the voltage rise time t_{r} and the current fall time t_{f} are data sheet parameters of the used switches.

2.2.4.3 Series and parallel capacitances

The losses of the series capacitance C_{S}, as well as the losses of the parallel capacitance C_{P} are given as [67]

$$P_{C_{\mathrm{S}}} = ESR \cdot \frac{I^2_{L\mathrm{s}}}{2} = \frac{\tan\delta_{C_{\mathrm{S}}}}{2\pi f C_{\mathrm{S}}} \frac{I^2_{L\mathrm{s}}}{2} \tag{2.99}$$

and

$$P_{C_{\mathrm{P}}} = 2\pi f C_{\mathrm{P}} \frac{V^2_{C_{\mathrm{P}}(1)}}{2} \tan\delta_{C_{\mathrm{P}}} \tag{2.100}$$

where, instead of the equivalent series resistance (ESR), the loss factor $\tan\delta$ is used for the calculations. The loss factors $\tan\delta_{C_\mathrm{S}}$ and $\tan\delta_{C_\mathrm{P}}$ of the used dielectricum are given in the data sheets.

2.2.4.4 Series inductor and high-voltage high frequency transformer

The high frequency losses for inductors and transformers can be divided into core and winding losses. A detailed description of both loss components is given in the subsubsections 2.4.2.1 and 2.4.2.2.

2.2.4.5 Output rectifier diodes

The conduction losses in each diode of the output rectifier can be estimated again by [66]

$$P_{\mathrm{Con,Rec}} = R_\mathrm{d} I^2_{\mathrm{D,RMS}} + V_\mathrm{F} |I_{\mathrm{D,avg}}|. \tag{2.101}$$

where V_F and R_d are the forward voltage droop and the differential resistance, which can be taken from the data sheet for a specified operation point.

2.3 Journal V.: Experimental Validation of a Serial Parallel Resonant Converter Model for a Solid State 115-kV Long Pulse Modulator

Michael Jaritz, Sebastian Blume, David Leuenberger and Juergen Biela
IEEE Transactions on Plasma Science, Volume: 43, Issue: 10, Page(s): 3392 - 3398, October 2015.
DOI: 10.1109/TPS.2015.2390258

Abstract

Medium and high beta cavities used in linear colliders or spallation sources are supplied by klystrons or inductive output tubes (IOT) amplifiers. The cathode voltage for these amplifiers can be generated by long pulse modulators generating highly accurate, high voltage pulses in the length of milliseconds. With existing modulator topologies all the demanding requirements like fast pulse rise time, high accuracy and low voltage ripple hardly can be satisfied at the same time. Common designs like bouncer modulator topologies using pulse transformers become huge for long pulses. The series parallel resonant converter (SPRC) avoids this drawback as the transformer is operated at high frequencies. In this paper, the comprehensive multi domain model of a SPRC converter including an electrical model of the inverter, a magnetic model, and an isolation design procedure of the transformer is verified with a prototype of a single module operated under full load conditions. In addition, a comparison between the predicted parasitics like leakage inductance and stray capacitance of the transformer and measured values is given. An evaluation of the isolation of the transformer, which is especially crucial for a series connection of the modules is also performed. Additionally, different possibilities to realize the desired series inductance are discussed.

2.3.1 Introduction

Based on the optimization procedure presented in [68] a single SPRC module has been designed. A single SPRC module [54] contains a full bridge connected to a series-parallel resonant circuit followed by a transformer, a rectifier, and a filter capacitor (see Fig. 2.31). Two single

Table 2.5: Pulse specifications

Pulse voltage	V_K	115 kV
Pulse current	I_K	25 A
Pulse power	P_K	2.88 MW
Pulse repetition rate	P_{RR}	14 Hz
Pulse width	T_P	3.5 ms
Pulse duty cycle	D	0.05
Pulse rise time (0...99 % of V_K)	t_{rise}	150 μs
Pulse fall time (100...10 % of V_K)	t_{fall}	150 μs
Short circuit energy	E_{arc}	$\leq$ 10 J

SPRC modules are connected in parallel at the output and in series at the input forming a stack. Eight of these stacks have to be connected in series at the output to obtain the required pulse voltage (see specifications in Tab. 2.5) and are connected in parallel at the input (see Fig. 2.31). In this paper, the comprehensive multi domain model of a single SPRC module including an electrical model of the inverter, a magnetic model, and an isolation design procedure of the transformer are verified with a prototype of a single module operated under full load conditions. Section 2.3.2 shortly discusses the results of a single SPRC module with its optimized parameters including the resonant tank, the transformer and the output rectifier. Different possibilities to realize the desired series inductance (integrated or separately) are presented in section 2.3.3. In section 2.3.4 a comparison between the analytical approach which is used in the optimization procedure and FEM calculations of the leakage inductance and the stray capacitance is given and compared to measurements. Section 2.3.5 presents the E-field conform isolation design of the transformer. All built components are discussed in section 2.3.6 and finally, section 2.3.7 presents pulse measurements of the prototype.

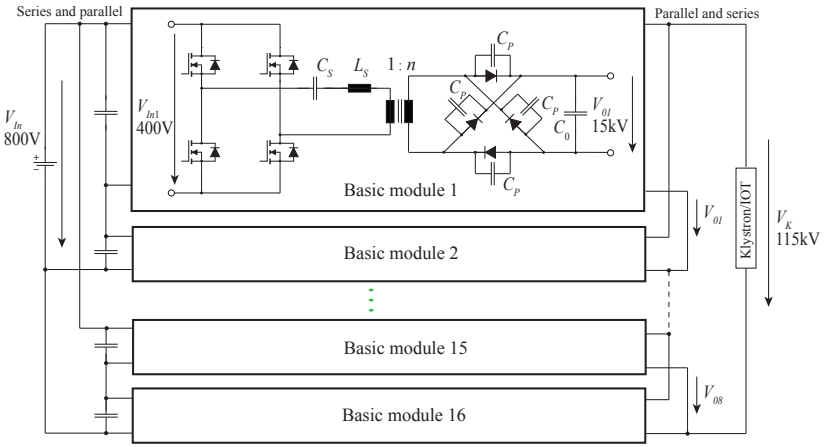


Figure 2.31: Full system with 2 single SPRC modules connected in series at the input and in parallel at the output forming a stack. 8 of this stacks are connected in series at the output to obtain the required pulse voltage.

2.3.2 Optimization results

Because of the high number of degrees of freedom during the design process as e.g. geometric parameters of the transformer or the design of the resonant tank, the optimization procedure presented in [1] has been developed for optimally designing the modulator (see Fig. 2.32). Tab. 2.6 summarizes the optimization results of the resonant tank and the transformer. To achieve a proper insulation design the isolation distance is determined according to an E-max design by varying the distance between primary and secondary winding in a first step. Afterwards in a post insulation design check an E-field conform design is carried out. Before starting modelling the optimization a model for the series inductance either included in the transformer or formed by an separately inductor has to be chosen. It turned out that due to the high resonant current I_{Ls} the best way to realize the series inductance Ls is an air toroid plus the leakage inductance of the transformer. A comparison of the evaluated structures between volume and losses is given in the next section.

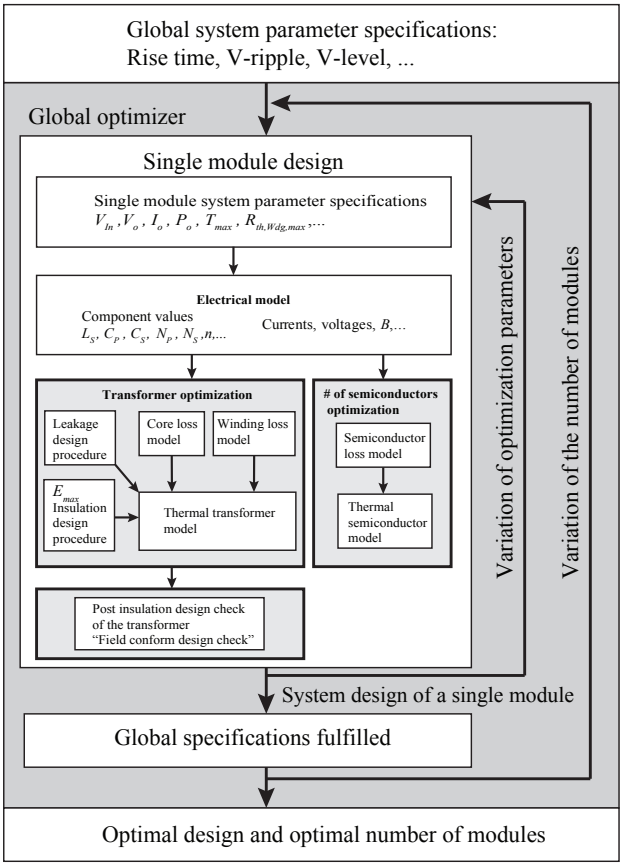


Figure 2.32: Proposed optimization procedure which leads to an optimal design of a single SPRC-module and an optimal number of modules of the overall system

2.3.3 Alternative ways to realize the series inductance

The series inductance in the optimization procedure is modelled as an air toroid. Alternative ways to realize the series inductance and a comparison of them by volume and losses is shown next. The following discussion is based on the results in Tab. 2.6 and all transformers are

Table 2.6: Optimization results of a single SPRC-module and optimal number of modules.

Resonant circuit					
$V_{OutPulsed}$	14.375 kV	L_S	5.1 μH	n	18
$I_{OutPulsed}$	12.5 A	C_S	0.837 μF	f	100 kHz
$P_{OutPulsed}$	179.7 kW	C_P	2.58 nF	I_{Ls}	800 A
Transformer					
Primary turns		3			
Secondary turns		54			
Overall system					
# of SPRC-modules in parallel and series					2 x 8

designed to the same isolation distances and turn ratios. A possible way to realize the series inductance L_S is to integrate it completely with the transformer leakage inductance (see Fig. 2.33 (a)). By adapting Δx and Δy in the case of the U-core transformer or only Δy in the case of the E-core transformer, the leakage inductance can be modified. This leads to a high boxed volume. Another possibility is to use an additional stray core wound by the primary or the secondary winding [69] (see Fig. 2.33 (b)). The inductance is set by varying the air gap of the stray core. If it is possible to use all turns of the secondary winding the isolation distance x_{min} has a minimum. Otherwise, if not all turns of the secondary could be used to keep the air gap as short as possible two times of the insulation distances have to be added to x_{min} and increases the volume. Additionally, using a stray core leads to

Table 2.7: Comparison between volume and losses

	Losses [W]	**Volume [l]**
(a) U-Core	82	48
(a) E-Core	66.1	46
(b)	361.7	25.1
(c)	109.5	12.21

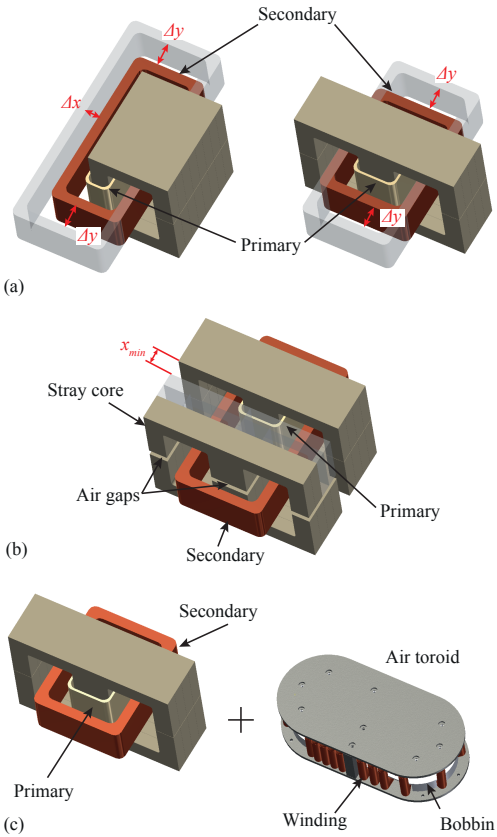


Figure 2.33: Different possibilities to realize the series inductance. (a) integrated in the transformer as leakage inductance either as U- or E-core, (b) using a stray core wounded by the secondary winding, inductance adaptations can be made by varying the air gap of the stray core and (c) the transformer is designed with respect to minimum insulation distances and the desired series inductance is formed by the transformers leakage inductance plus a non saturable air toroid.

higher losses due to the high resonant current I_{Ls}. The third option to realize the series inductance L_S is an air toroid (see Fig. 2.33 (c)). The transformer is designed with respect to minimum insulation distances and the air toroid causes no core losses. Thus, using a transformer and

an air toroid it is the best compromise between volume and losses to realize the series inductance. In Tab. 2.7 a comparison of the discussed possibilities between volume and losses is listed. As the output characteristic of the SPRC converter is directly influenced by the parasitics of the transformer, it is necessary to accurately know the leakage and the stray capacitance of the transformer. An evaluation of the transformer parasitics calculations compared to measurements is given in the next section.

2.3.4 Transformer parasitics validation

2.3.4.1 Leakage inductance

As presented in [68] the calculation of the leakage inductance is based on the mirror current method. To increase the accuracy of this method different mirror planes are used inside and outside the core. Inside the core window mirroring on all 4 core walls is applied (see Fig. 2.34 (b)) and for the region outside the core mirroring just to the left wall is used (see Fig. 2.34 (c). Therefore, (15) and (16) in [68] can be simplified in the left mirroring case to

$$H_x = \frac{I_j}{2\pi}\left(\frac{x-x_j}{(x-x_j)^2+(y-y_j)^2}+\frac{x+x_j}{(x+x_j)^2+(y-y_j)^2}\right) \tag{2.102}$$

$$H_y = \frac{I_j}{2\pi}\left(\frac{y-y_j}{(x-x_j)^2+(y-y_j)^2}+\frac{y-y_j}{(x+x_j)^2+(y-y_j)^2}\right) \tag{2.103}$$

and using (17) from [68] leads to the desired leakage inductance, where l_W is the integration length inside the core $l_{W,in}$ and outside the core $l_{W,out}$ (see Fig. 2.34 (a)). Finally, with this method it is possible to calculate the magnetic energy W_m inside the transformer window (see Fig. 2.34 (b)), in the air box outside the transformers' front (see Fig. 2.34 (a)), but it is not possible to consider the energy above and under the transformer core. It is assumed that there is a negligible amount of energy inside the core due to the high permeability of the core material. Table 2.8 compares the error between FEM and the mirror current method related to the mesured leakage inductance by varying the parameter n_1. If the areas in the core, above and below the transformer are also considered in the FEM evaluation the leakage inductance results in 1.59 μH and leads to an error of -0.94 % related to the measured value.

2.3.4.2 Stray capacitance

As presented in [68] the calculation of the electrical field is based on the mirror charge method, with mirroring inside the core at all 4 walls. Another possibility to calculate the electrical field inside and outside the transformer is to use additional core image charges [70], [50]. Their contour points are placed at the edges of the core window in Fig. 2.35 (a) and at the outer edges of the core as shown in Fig. 2.35 (b). They provide the ground potential and form the geometry. With this methode

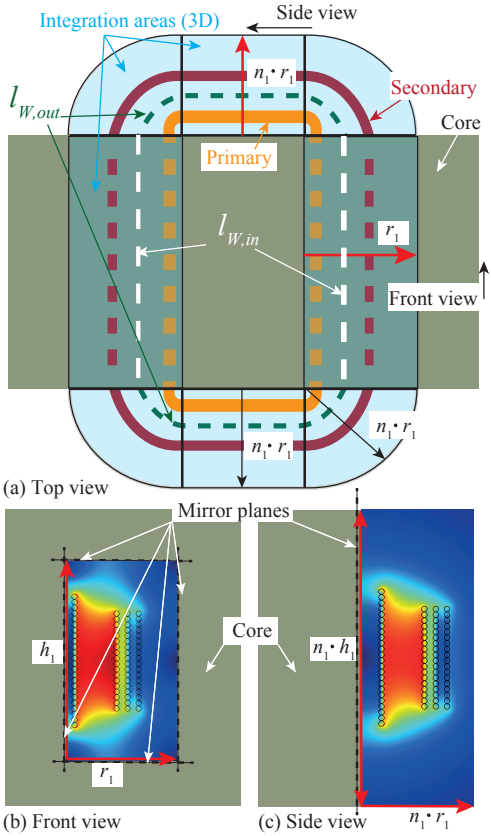


Figure 2.34: Integration areas and paths for 3D, 2D FEM and 2D numerical parasitics calculations of the transformer.

Table 2.8: Comparison between 3D FEM, Mirror method and the measured leakage inductance

n_1	**3D FEM**	**Mirror**	**Meas.**	**error FEM**	**error mirror**
	[μH]			[%]	
1	1.39	1.5068	1.6	−13.12	−5.8
3	1.4177	1.5379	1.6	−11.37	−3.9
6	1.418	1.54	1.6	−11.39	−3.75

the areas above and below the transformer can be taken into account. Additionally arbitrary core geometries as well as winding arrangements can be included into optimization procedures minimizing the stray capacitance. The calculations are performed in free space, therefore Equ. (8) and (11) in [68] can be simplified to

$$E_x = \frac{Q_j}{2\pi\epsilon}\left(\frac{x-x_j}{(x-x_j)^2+(y-y_j)^2}\right) \tag{2.104}$$

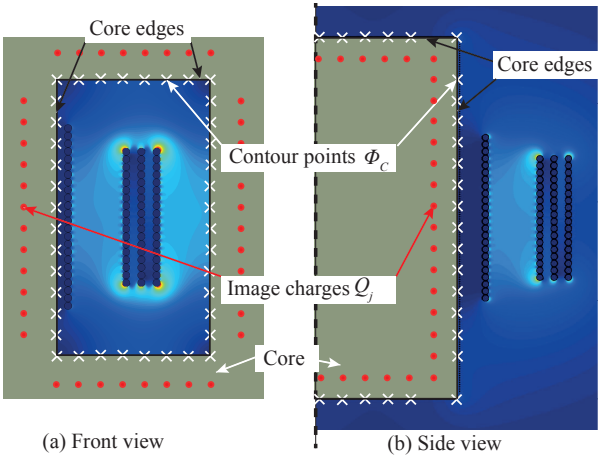


Figure 2.35: (a) Arrangement of the image charges and their contour points inside the transformer at the core window and (b) at the outer edges of the transformer core.

$$E_y = \frac{Q_j}{2\pi\epsilon}\left(\frac{y-y_j}{(x-x_j)^2+(y-y_j)^2}\right). \tag{2.105}$$

Using the same integration lengths as for the leakage inductance the stray capacitance related to the secondary side of the transformer then is determined by

$$C_{stray} = \frac{2W_e}{V^2_{VoutPulsed}} \quad \text{with} \quad W_e = \frac{l_W \epsilon_r \epsilon_0}{2}\iint(E_x^2+E_y^2)dxdy \tag{2.106}$$

where ϵ_r is the permittivity of the dielectric. A comparison is given between 2D FEM, the core image charge method and measurements in Tab. 2.9. No values are given for 3D FEM because little deviations of the turns arrangement or the radiuses of the winding edges in the 3D model lead to high deviations in the electrical field, respectively in the capacitance.

Table 2.9: Comparison between 2D FEM, Core Image Charge Method(CICM) and the measured stray capacitance in air

2D FEM	**CICM**	**Measured**	**error FEM**	**error CICM**
[pF]			[%]	
45.57	46	59.9	−23.9	−23.2

2.3.5 Insulation design procedure

The following section describes an insulation post design check which is performed after the transformer optimization procedure in Fig. 2.32. It is not possible to integrate a full analytical model of the transformer in all details e.g. bobbins and winding fastenings (see Fig. 2.36) in the procedure. A basic insulation design is included in the optimization procedure by calculating the maximum electrical field and varying the distances between primary and secondary [68].
Partial discharges as well as sliding discharges can harm the insulation of the transformer permanently and lead to arcs between the windings or the core. Additionally the electrical strength of long oil gaps is decreasing due to the volume and the area effect [71]. Therefore, for long life times a proper insulations design is necessary and a detailed analysis of the electrical field distribution along creepage paths and long

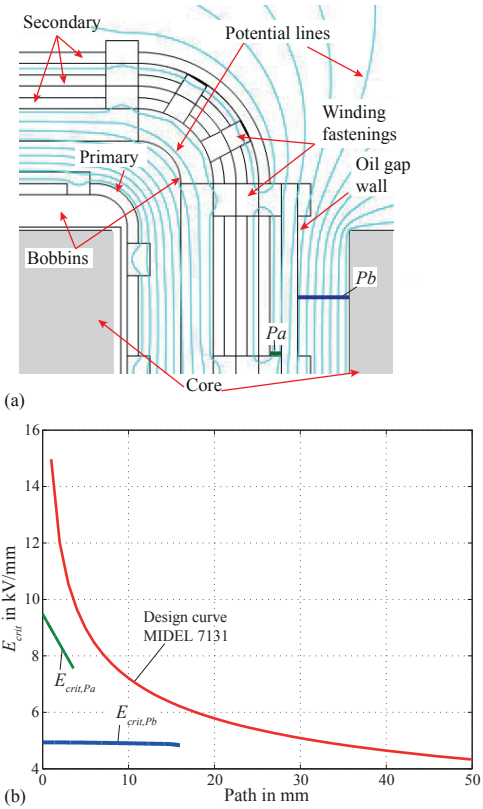


Figure 2.36: (a) Potenial lines with evaluated critical paths, (b) design curve and averaged cumulated electrical field strengths of the investigated paths Pa and Pb.

oil paths inside the transformer was carried out with the help of the Weidmann design curve method [72]. This design method is based on oil design curves which are derived from homogenous electrical breakdown tests [73]. These are then compared with the averaged cumulated electrical field strength $E_{avg,cum}$ along certain paths. Fig. 2.36 shows in (a) an evaluated oil gap P_b and a creepage path P_a. For a valid design $E_{avg,cum}$ both paths have to be below the design curve in (b). The design curves of the used transformer oil MIDEL7131 [74] are derived from

[75] and [76]. With this method, insulations designs with homogenous as well as inhomogenous field distributions can be investigated. Finally, applying this method leads to an electrical field conform design, which means that the potential lines just have a tangential component along insulation fastenings (see Fig. 2.36 (a)). Hence, the insulator is stressed in normal direction by the electrical field and has its maximum electrical strength. Fig. 2.40 (a) shows the built transformer prototype without any mountings between primary and secondary bobbins inside the transformer to avoid creepage paths between them as depicted in Fig. 2.40 (b). The bobbins are fixed outside the transformer, leading to a longer creepage distance between the windings.
The next section summarizes the built components of a single SPRC module.

2.3.6 Components of a single SPRC module

Following discussed components are related to the single SPRC module depicted in Fig. 2.31 and are the results of the optimization procedure.

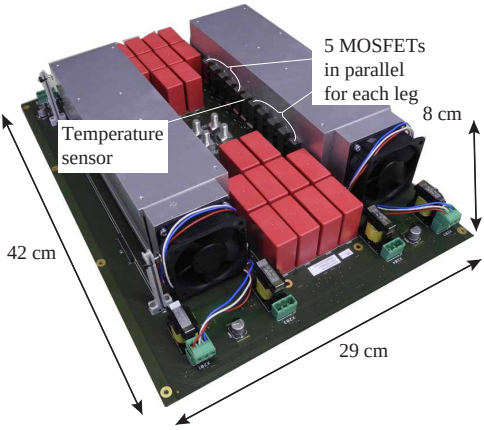


Figure 2.37: Prototype modulator each leg with 5 switches in parallel, with two legs on one heat sink. Photo: Ampegon AG

2.3.6.1 HF-MOSFET Modulator

The modulator in Fig. 2.37 is operated at 100 kHz and consists of 20 MOSFET switches, each leg with 5 switches in parallel, with two legs on one heat sink. For high lifetime the calculated junction temperature swing ΔT_J of a single MOSFET is kept below 12 °K at nominal pulse duty cycle [68].

2.3.6.2 Resonant Tank: Series capacitance and series inductance

Due to the high resonant current the series capacitor C_S is designed with respect to a balanced current sharing and thus four double layered circuit boards are used. (see Fig. 2.38). NP0 dielectric ceramic capacitors are utilised for C_S which are stable in a wide range of temperature and frequency and also does not suffer from DC voltage derating. The series inductance in Fig. 2.39 is built as an air toroid coil to avoid saturation and to minimize the losses due to the high current. Its winding consists of Litz wire with 2000 x 0.05 mm strands, 8 wires in parallel and 22 turns.

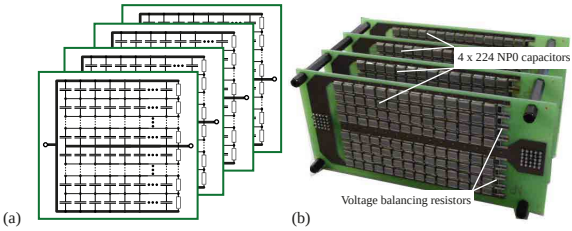


Figure 2.38: (a) Simplified diagram of the series capacitance, 896 NP0 capacitances and corresponding balancing resistors are distributed on 4 PCBs to provide optimal current sharing and (b) built series capacitance C_S.

2.3.6.3 HV-HF-transformer

The high voltage, high frequency transformer is shown in Fig. 2.40 (a) and 2.40 (b). To keep the losses low ferrite as core material and Litz wire for the windings are used due to the high operating frequency. Thin copper plates are used to transfer the heat out of the transformer to ambient.

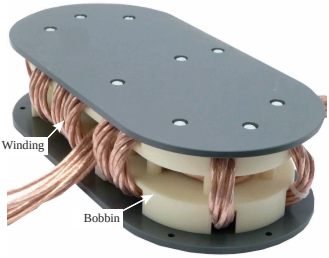


Figure 2.39: Prototype of the HF-air toroid coil L_S formed by 22 turns.

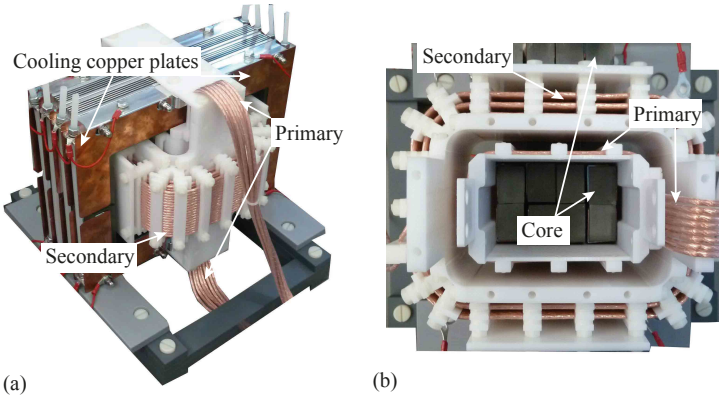


Figure 2.40: (a) Built transformer prototype, (b) top view of the transformer without any mountings between primary and secondary inside the transformer.

2.3.6.4 Rectifier, parallel capacitance and output filter

The rectifier is built of 156 diodes, 39 in series in each leg. Each layer of one circuit board is used for one diode leg and has to isolate the full output voltage of a single SPRC module. The parallel capacitance C_P is built with 624 NP0 ceramic capacitors which are also used to symmetrize the voltage over each rectifier diode (see Fig. 2.41(a)). Additionally balancing resistors are also used to symmetrize the voltage over each diode and the output filter C_0 is realized as an series parallel connection of NP0 capacitors.

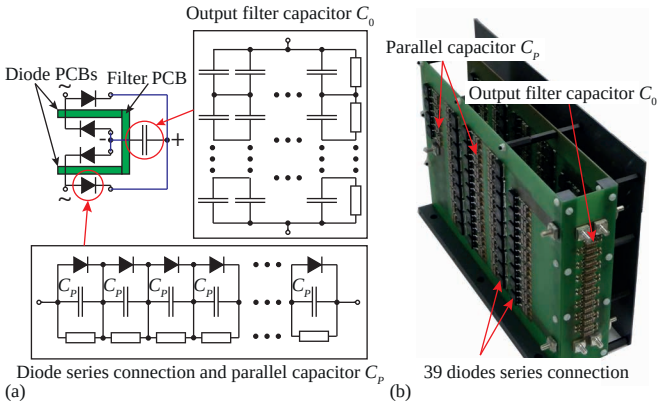


Figure 2.41: (a) Simplified diagram of the rectifier including the parallel capacitance and the output filter and (b) built rectifier with parallel capacitance C_P and the output filter.

2.3.7 Measurements

In the following measurement results are presented. The green curve $V_{Out,meas}(t)$ in Fig. 2.42 depicts the measured output voltage pulse V_{O1} of a single SPRC module. The simulated blue curve $V_{Out,sim}(t)$ shows good accordance with the measured one and the red curve $V_{Out,avg}(t)$ is the mean average of $V_{Out,meas}(t)$, used to determine the rise and the fall time. Rise and fall times are well below the given limits in Tab. 2.5. Just a 300 μs pulse is depicted in Fig. 2.42 to show the pulse rise and fall time in one picture.

2.3.8 Conclusion

In this paper, a comprehensive multi domain model of the SPRC converter is verified with a prototype of a single module by measurements. The simulated data shows good accordance with the measured one. In addition, a comparison between the predicted parasitics like leakage inductance and stray capacitance of the transformer and the measured ones is given. The error between calculated and measured parasitics is low. An evaluation of the isolation of the transformer is also carried out. Additionally, different possibilities to realize the desired series inductance are discussed and compared by volume and losses.

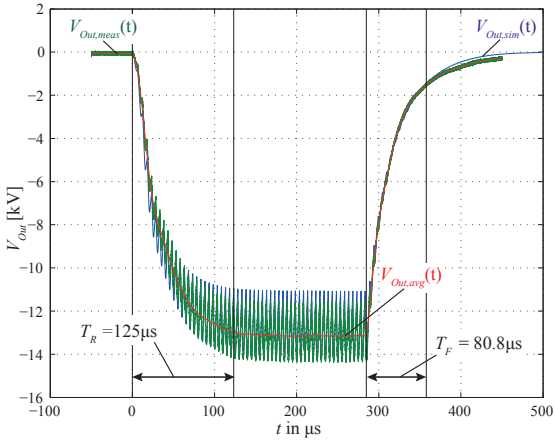


Figure 2.42: Measured pulse $V_{Out,meas}(t)$ (50 MHz low pass filtered), simulated pulse $V_{Out,sim}(t)$ and averaged pulse $V_{Out,avg}(t)$.

Acknowledgment

The authors would like to thank the project partners CTI and Ampegon AG very much for their strong support of the CTI-research project 13135.1 PFFLR-IW.

Note:

The components of the presented single SPRC-Bm prototype is a preliminary prototype, which was used for the validation of the proposed models. The single SPRC-Bm which was finally built is shown in chapter 5 in Fig. 5.4.

2.4 Journal IV.: Design Procedure of a 14.4 kV, 100 kHz Transformer with a High Isolation Voltage (115 kV)

Michael Jaritz, Sebastian Blume and Juergen Biela
IEEE Transactions on Dielectrics and Electrical Insulation , Volume: 24, Issue: 4, Page(s): 2094 - 2104, September 2017.
DOI: 10.1109/TDEI.2017.006279

Abstract

In this paper, the design procedure of a 14.4 kV output voltage, 100 kHz transformer with an isolation voltage of 115 kV using Litz wire is presented. All design models, including a generalized magnetic model for the leakage and the loss calculations as well as an electrical model for the parasitic capacitance estimation for the transformer are derived and proven by measurements. For designing the insulation, a comprehensive design method based on an analytical maximum electrical field evaluation and an electrical field conform design is used. The resulting design is verified by long and short term partial discharge measurements on a prototype transformer.

2.4.1 Introduction

For the new linear collider at the European Spallation Source (ESS) in Lund, 2.88 MW pulse modulators with pulsed output voltages of 115 kV and pulse lengths in the range of a few milliseconds are required (pulse specifications see Tab. 2.10). For generating such pulses, a long pulse modulator based on a modular series parallel resonant converter (SPRC) topology has been developed [68]. This converter is operated at high switching frequencies 100 kHz - 110 kHz in order to minimize the dimensions of the reactive components and the transformer. To achieve the required output voltage of 115 kV, 8 SPRC basic modules (SPRC bm) each with an output of 14.4 kV are connected in series [77], see Fig. 2.43. Due to the series connection of the SPRC basic modules, the insulation of the last oil isolated transformer in the row has to withstand the full pulse voltage. Therefore, in this paper additionally a comprehensive transformer design and optimization procedure is presented. This design procedure includes a generalized calculation

Table 2.10: Pulse specifications

Pulse voltage	V_K	115 kV
Pulse current	I_K	25 A
Pulse power	P_K	2.88 MW
Pulse repetition rate	P_{RR}	14 Hz
Pulse width	T_P	3.5 ms
Pulse duty cycle	D	0.05
Pulse rise time (0...99 % V_K)	t_{rise}	150 µs
Pulse fall time (100...10 % V_K)	t_{fall}	150 µs

method for the leakage, the parasitic capacitance and all high frequency losses.
In the literature, several approaches are presented for designing high voltage, high frequency transformers. In [78–80] designs with nominal output voltages between 50 kV-60 kV and a switching frequency of 20 kHz, but no partial discharge tests have been performed. The same is true for the transformer presented in [81], which is designed with respect to an isolation voltage of 15 kV, a nominal output voltage of 3.8 kV and 3 kHz operation frequency. In [82] the design is carried out for a nominal output voltage of 3 kV, a switching frequency of 10 kHz and only provides partial discharge measurements for short term tests (1 min, test voltage 28 kV).
However, all of these transformers are either tested only under nominal field conditions [78]-[81] and/or no values for long term partial discharge measurements which are an essential life time parameter for high voltage components [83], are given [82]. In addition, the isolation voltage of 115 kV and the switching frequency range of 100 kHz - 110 kHz exceed by far the designs presented in [78]-[82]. Therefore, in this paper a comprehensive design procedure of a 14.4 kV nominal output voltage, 100 kHz transformer, is presented. The procedure consists of a detailed insulation design method for an isolation voltage of 115 kV, which is verified by long term (60 min) 115 kV test voltage and short term (5 min) extended test voltage (up to 136 %) partial discharge measurements. It

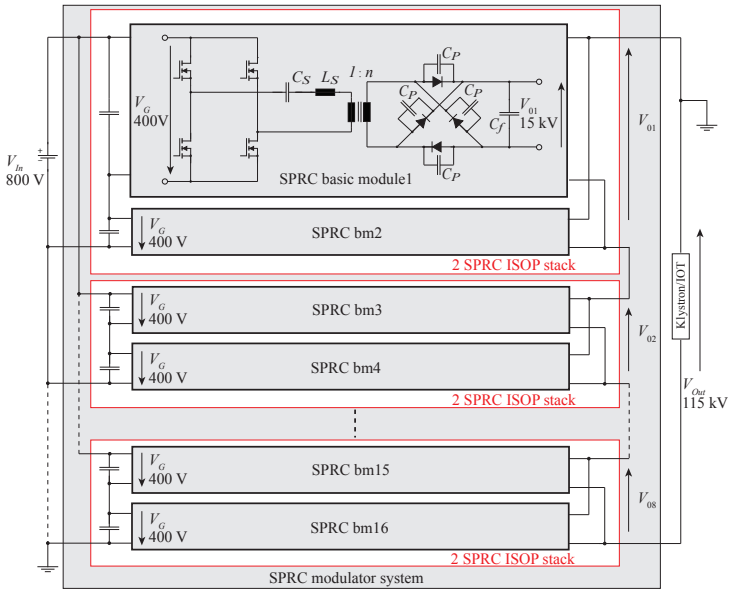


Figure 2.43: SPRC modulator system with 2 SPRC basic modules forming an ISOP stack [77] and 8 of them are connected in series to achieve the required output voltage.

further contains a generalized magnetic model for the leakage and loss calculations, as well as an electrical model for the parasitic capacitance estimation. Finally, this procedure is employed in an optimization algorithm, which leads to an optimal design and minimized development times and costs of the high voltage high frequency transformer.
In section 2.4.2, first, the transformer design procedure including the models for the parasitics, the high frequency loss calculations and a comprehensive insulation design procedure is given in detail. In section 2.4.3, the resulting insulation design is evaluated by long term nominal voltage and short term over-voltage partial discharge measurements. For verifying the losses and the parasitics, in addition, pulse measurement of a single SPRC bm are presented.

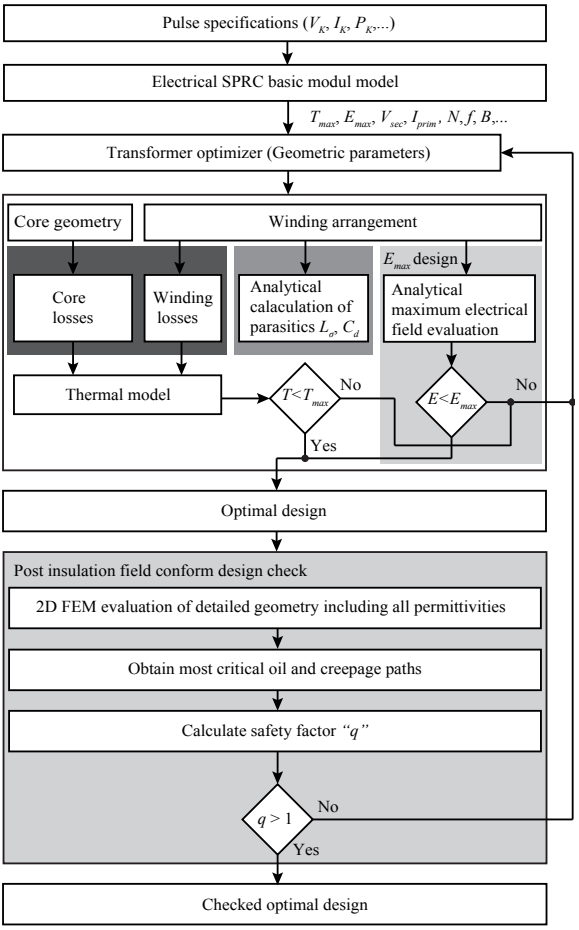


Figure 2.44: Transformer optimization with high frequency loss calculations (dark gray shown area), parasitics models (medium gray shown area) and integrated insulation design procedure (light gray shown areas).

2.4.2 Transformer design procedure

Due to the high number of degrees of freedom encountered in the transformer design process as for example the geometric parameters of the core or the windings, an optimization procedure has been developed

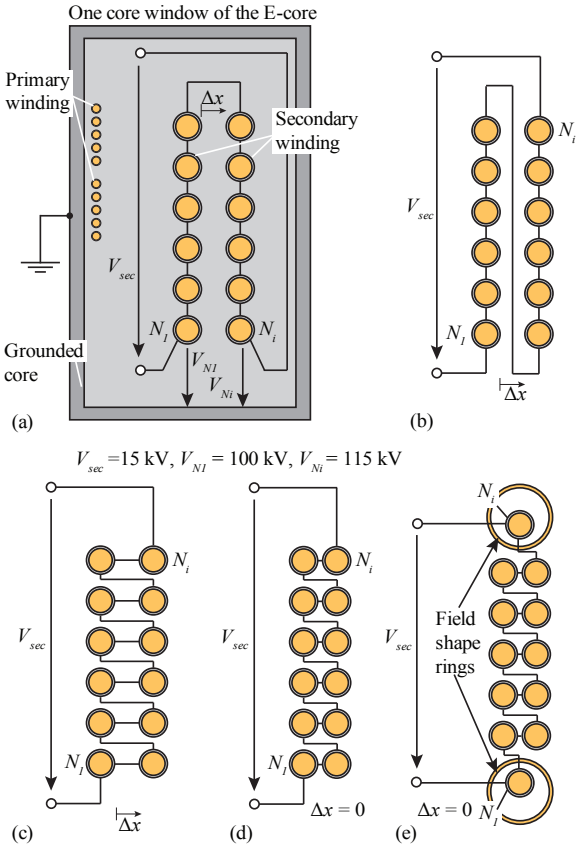


Figure 2.45: Five basic winding configurations inside grounded core window of the E-core: (a) Standard winding, (b) flyback winding, (c) s-winding, (d) s-winding with $\Delta x = 0$, and (e) s-winding arrangement with field shape ring and $\Delta x = 0$.

for optimally designing the transformer (see Fig. 2.44) [68]. In the first step, with an electrical model of the SPRC bm the input parameters (e.g. primary current I_{prim} or secondary voltage V_{sec}) and constraints (e.g. maximum temperature T_{max} or flux density B_{max}) for the transformer optimization are determined for the given pulse specifications. In the next step, a specific core and winding geometry has to be chosen before the transformer optimization is started. In order to minimize

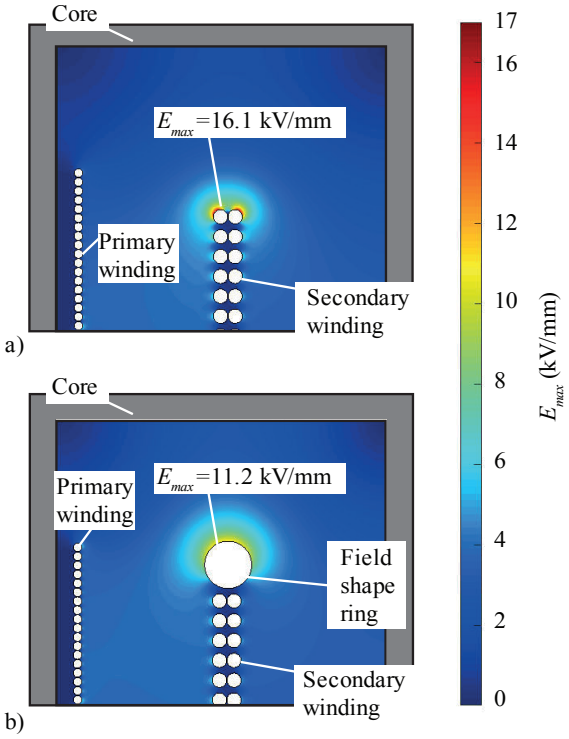


Figure 2.46: (a) Maximum E-field of s-winding and (b) maximum E-field of s-winding with a field shape ring (10 mm diameter) inside the core window.

the magnetic stray field outside the transformer, an E-type core is used as core geometry, where two windings are wound around the center leg. For the winding geometry, there are five possible basic winding configurations (Fig. 2.45). These are investigated in the following, with respect to the maximum electrical field, lowest electrical energy per length W'_E and maximum wire to wire withstand voltage V_{WS} by varying the distance Δx. The standard and the flyback winding configurations (see Fig. 2.45 (a) and (b)) result in high E_{max}, W'_E and V_{WS} values [84]. The s-winding configuration (see Fig. 2.45 (c) and (d)) has the advantage of a minimum withstand voltage, but still high E_{max} values occur. Adding a field shape ring to the configuration in Fig. 2.45 (d) results

Table 2.11: E_{max} evaluation results

Config.	$\boldsymbol{\Delta x}$ (mm)	$\boldsymbol{E_{max}}$ (kV/mm)	$\boldsymbol{W'_E}$ (mJ/m)	$\boldsymbol{V_{WS}}$ (kV)
(a)	6.1	16.53	435.22	V_{sec}
(b)	6.1	15.8	433.66	$V_{sec}/2$
(c)	2.1	15.96	401.28	$4V_{sec}/N_i$
(d)	0	16.11	385.86	$4V_{sec}/N_i$
(e)	0	11.24	461.64	$4V_{sec}/N_i$

in the winding arrangement given in Fig. 2.45 (e). The first and the last turn of the winding are placed inside field shape rings leading to a reduced E_{max}. Fig. 2.46 (a) and (b) show the electrical field distribution of the s-winding configuration with and without field shape rings. Comparing the maximal electrical fields for cases (d) and (e) given in Tab. 2.11, it could be seen that the occurring peak field is reduced by 43.3 %. The field shape rings are on the same potential as the respective turn and one end of the turn is soldered to the corresponding field shape ring, see Fig. 2.49 (d). Due to this arrangement the high frequency losses do not increase much because most of the load current is still conducted by the Litz wire inside the field shape ring and not by the field shaping ring.
Based on the chosen core and winding geometry (Fig. 2.45 (e)) all losses and parasitics are calculated and also the maximum electrical peak field is estimated. Afterwards, a detailed model of the transformer is evaluated regarding oil gap widths and creepage paths in a FEM based post design check.
The first step of the transformer design are the core losses, which are discussed in the following.

2.4.2.1 Core losses

Due to the high switching frequency f =100 kHz, ferrite K2008 is used as core material. Since the flux density has an approximately sinusoidal waveform, the volume depended core losses are calculated with the standard Steinmetz equation [85]

$$P_V = k f^{\alpha} \hat{B}^{\beta}. \tag{2.107}$$

Table 2.12: Operating points and Steinmetz parameters of the core material K2008 at 100 °C

Operating points		
(Hz)	(T)	(W/m^3)
$f_1 = 90 \cdot 10^3$	$B_1 = 0.1$	$P_{V1} = 35.81 \cdot 10^3$
$f_2 = 90 \cdot 10^3$	$B_2 = 0.2$	$P_{V2} = 328.11 \cdot 10^3$
$f_3 = 200 \cdot 10^3$	$B_3 = 0.1$	$P_{V3} = 138.73 \cdot 10^3$
Steinmetz parameters		
$\alpha(-)$	$\beta(-)$	$k(W/(HzTm^3)$
1.6959	3.1955	0.2228

Solving equation (2.107) at three operating points (see Tab. 2.12), extracted from the losses versus frequency curve in [86], gives the Steinmetz parameters α, β and k [87]. The Steinmetz parameters for K2008 at a core temperature of 100 °C are listed in Tab. 2.12. The core losses have to be additionally scaled by a correction factor c_0. This factor is the ratio between the core losses, measured on R34 toroids, taken from the material (K2008) data sheet [86] and the losses taken from the chosen core shape (U126/20) data sheet [88], given for an identical operating point. In the case of the U126/20 core, $c_0 = 2.56$. The total averaged core losses for the E-core made of 16 U-cores

$$P_C = P_V V_C c_0 D, \tag{2.108}$$

where V_C is the core volume.
In the next step, the high frequency losses are calculated as explained in the following.

2.4.2.2 Winding losses

In order to minimize the high frequency losses, which include skin and proximity losses, HF-Litz wire is used for the primary and secondary winding to ensure an approximately homogenous current density across the cross section of the turn. The high frequency losses per length in a

Litz wire bundle are calculated by [89]

$$P'_{Bundle} = N_S \left(F_{St} \frac{I^2}{N_S^2} + \frac{G_{St}}{\pi r_a^2} \int |H|^2 dA \right) \tag{2.109}$$

$$= N_S \left(F_{St} \frac{I^2}{N_S^2} + G_{St} H_{avg} \right), \tag{2.110}$$

where F_{St} and G_{St} are the skin respectively the proximity effect factors, N_S is the number of strands per bundle, I is the total peak current of the winding and H is the peak magnetic field of each bundle. Figure 2.47 (d) shows the norm of the total magnetic field $|H|$ inside the core window. For calculating the high frequency losses, this field can be calculated by the superposition of the internal Field H_{int} (Fig. 2.47 (a)) and the external field H_{ext} (Fig. 2.47 (b)) inside the turns. Considering additionally the field in the space outside the turns H_S (Fig. 2.47 (c)), also the leakage inductance can be calculated. The internal Field H_{int} is a radial field inside each Litz wire, caused by the current in each wire and it is not effected by any other field, see Fig. 2.47 (a). The external field H_{ext} inside a considered wire is caused by the currents respectively the fields of all other wires but not by the considered wire itself and the field H_S in the space outside the wires is caused by the currents of all conductors.
All field components can be calculated directly with the help of the mirror current method [68]. For the external field components, equations (15) and (16), from [68] can be used inside the core window and for the region outside the core window, these equations can be simplified for the x-component to

$$H_{ext,x} = \sum_{j=1}^{N} \frac{I_j}{2\pi} \left(\frac{y - y_j}{(x - x_j)^2 + (y - y_j)^2} + \frac{y - y_j}{(x + x_j)^2 + (y - y_j)^2} \right) \tag{2.111}$$

$$H_{ext,y} = \sum_{j=1}^{N} \frac{I_j}{2\pi} \left(\frac{x - x_j}{(x - x_j)^2 + (y - y_j)^2} + \frac{x + x_j}{(x + x_j)^2 + (y - y_j)^2} \right). \tag{2.112}$$

These equations can be also applied for H_S. For the radial internal field component H_{int} inside the core window as well as outside the core window

$$H_{int,x} = \frac{I_j}{2\pi} \left(\frac{y - y_j}{r_a^2} \right) \tag{2.113}$$

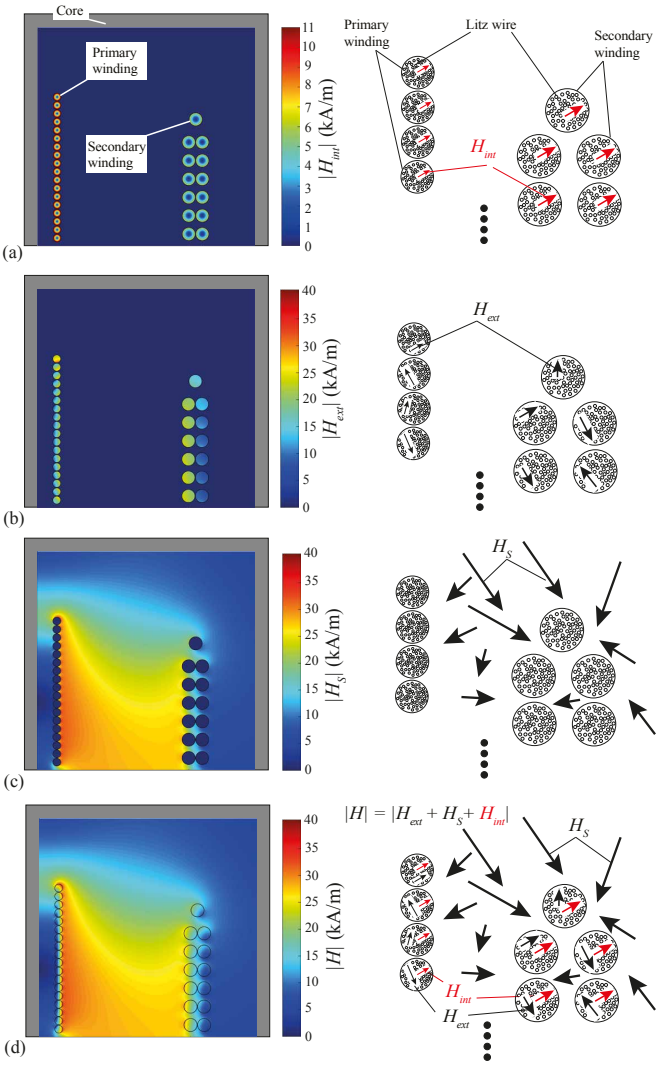


Figure 2.47: (a) Radial magnetical field component H_{int} inside the turns, (b) external field component H_{ext} inside the turns, (c) field component H_S in the space outside the turns and (d) the total magnetic field H, which is the superposition of the three components.

$$H_{int,y}= \frac{I_j}{2\pi}\left(\frac{x-x_j}{r_a^2}\right) \tag{2.114}$$

are employed.
The total magnetic field $|H|$ is the norm of the superposition of the three magnetic field component vectors

$$|H| = \sqrt{H_x^2 + H_y^2} \tag{2.115}$$

with

$$\begin{aligned} H_x &= H_{int,x} + H_{ext,x} + H_{S,x} \\ H_y &= H_{int,y} + H_{ext,y} + H_{S,y} \end{aligned} \tag{2.116}$$

The high frequency losses then are given by

$$P_{Wdg} = N_S l_m \left(\frac{N F_{St} I^2}{N_S^2} + \sum_{n=1}^{N} G_{St} H_{avg,n} \right) D, \tag{2.117}$$

with

$$H_{avg,n} = \frac{1}{\pi r_a^2} \int |H|^2 dA_n, \tag{2.118}$$

where N is the number of turns and l_m is the mean winding length of the considered winding. $H_{avg,n}$ is the mean averaged field, calculated for each turn cross section A_n separately.

2.4.2.3 Transformer parasitics calculation based on conductor arrays

In order to design the components of the resonant tank of a SPRC bm correctly, the parasitics of the transformer have to be estimated accurately.
The image charge method [68] matches well with the 2D-FEM based analysis when calculating the transformer parasitics, but the analysis of large geometries results in a high computational effort for the image charge method. This effort originates from a high number of calculation points, which must be derived to approximate the surface integral with the desired high accuracy. Thus, for larger geometries the application of the image charge method for calculating the transformer parasitics

is not beneficial in comparison to a 2D-FEM based analysis.
In order to have a fast calculation of the parasitics multi-conductor arrays can be used. In this case, all capacitances and inductances between the conductors are derived by solving the corresponding field quantity integrals directly with the given geometric distances of the conductors (see Fig. 2.48). The core acts as an electric mirror due to its the electrical conductivity, so that the conductors can be mirrored as described in [68]. This analysis is conducted in the two dimensional space. The calculation method of the stray capacitance C_d via multi-conductor arrays including image charges has been presented in [90] and therefore is only shortly repeated in the following.

Stray capacitance calculation based on conductor arrays The potential coefficient p_{kl} between conductor k and l, considering image charges due to grounded surfaces, can be described by

$$p_{kl} = \frac{1}{2\pi\epsilon_0\epsilon_r}\left(\ln\left(\frac{d_{kl}}{r_c}\right) + \sum_{mp_l=mn_l=1}^{N/2} \ln\left(\frac{d_{k,mp_l}}{d_{k,mn_l}}\right)\right), \quad k \neq l, \tag{2.119}$$

where d_{kl} is the distance from conductor k to conductor l, r_c is the conductor's radius, d_{k,mp_l} is the distance of conductor k to all positive image charges and d_{k,mn_l} to all negative image charges of conductor l. With this equation the potential coefficient matrix can be derived, which can be transformed to the capacitance coefficient matrix by a matrix inversion. This inverted matrix contains the inter-conductor capacitances, which can be used to derive the equivalent stray capacitance of the system by summation of the energy stored in each of the inter-conductor capacitances.
Next, the calculation of the leakage inductance based on multi-conductor arrays is presented.

Leakage inductance calculation based on conductor arrays Assuming a multi-conductor system the magnetic flux per unit length Φ'_B is obtained by

$$[\Phi'_B] = [L'] \cdot [I]. \tag{2.120}$$

Since the analysis is limited to the two-dimensional space, the interconnection of the conductors does not matter [91]. The external inductance

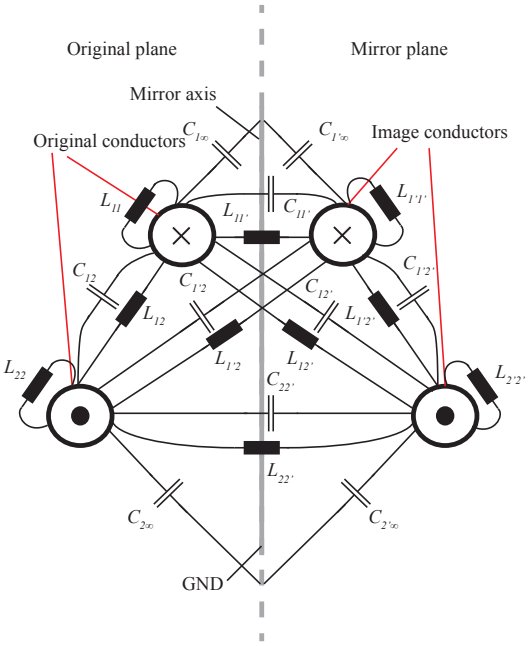


Figure 2.48: Two conductors in the original plane and their corresponding image conductors in the mirror plane with all related inductances and capacitances.

$L'_{kl,ex}$ between conductor k and conductor l, assuming both conductors with equal radius r_c, can be described by

$$L'_{kl,ex} = \frac{\mu_r}{2\pi} \ln\left(\frac{d_{kl}}{r_c}\right) \quad k \neq l, \tag{2.121}$$

where d_{kl} is the distance between the two conductors. The internal inductance L'_{kk} caused by the conductor itself can be described by

$$L'_{kk} = \frac{\mu_r}{8\pi} \tag{2.122}$$

Since the magnetic core has a very high relative permeability μ_r, it can be considered as magnetic mirror [92]. In order to take this effect into account, the conductors can be mirrored analogously with the image

Table 2.13: Comparison between FEM, image method, conductor array method and the measured parasitics

FEM I	**FEM II**	**Image**	**Cond. array**	**Measurement**
		$\boldsymbol{C_d}$ (pC)		
16.7	22.1	16.4	17.2	21.7
		Error (%)		
−23	+1.8	−24.4	−20.7	–
FEM		**Image**	**Cond. array**	**Measurement**
		$\boldsymbol{L_\sigma}$ (µH)		
0.84		0.84	0.84	0.83
		Error (%)		
+1.2		+1.2	+1.2	–

charge method. In contract to the image charges in case of the stray capacitance C_d, the direction of the current flow remains equal for the mirrored conductors. Considering the image conductors, the total self inductance $L_{kk,box}$ inside the core window can be described by

$$L'_{kk,box} = \frac{\mu_r}{2\pi} \left(\frac{1}{4} + \sum_{mc_l=1}^{N} \ln \left(\frac{d_{k,mc_k}}{r_c} \right) \right), \tag{2.123}$$

where d_{k,mc_k} is the distance of conductor k to all its image conductors. The external inductance in this case is

$$L'_{kl,ex} = \frac{\mu_r}{2\pi} \left(\ln \left(\frac{d_{kl}}{r_c} \right) + \sum_{mc_l=1}^{N} \ln \left(\frac{d_{k,mc_l}}{r_c} \right) \right) \; k \neq l, \tag{2.124}$$

where d_{kl} is the distance of conductor k to conductor l, d_{k,mc_l} the distance of conductor k to all image conductors of conductor l. If a homogeneous current distribution over all conductors is assumed, the total inductance per unit length of the geometry can be obtained by

$$L'_\sigma = \sum_k \sum_l L'_{kl}. \tag{2.125}$$

Both quantities, the capacitance per unit length C'_d and the leakage inductance per unit length L'_σ, must be multiplied with its associated

length, to obtain the desired quantities C_d and L_σ.
A comparison between FEM calculations, the image charge method and the conductor array method with respect to measurements is given in Tab. 2.13. The error is smaller than 2 % in the case of the leakage inductance for all methods in relation to the conducted measurement. In the case of the stray capacitance, it can be noticed that FEM I calculations, image charge and the conductor array method result in similar values, but the error to measurement is in the range of −25 %. This can be explained by the fact that only a single permittivity value for the geometry is assumed. The error is reduced below 2 % in FEM II if all permittivities of the different insulation materials are considered.
Based on the image charge method and the FEM evaluations an insulation design procedure is introduced in the following section.

2.4.2.4 Insulation design procedure

In the following, the insulation design procedure (areas highlighted in gray in Fig. 2.44) which can be divided into an analytical maximum electrical field evaluation and a FEM supported post insulation field conform design check are described more in detail.

Evaluation of the maximum electrical field Due to the complexity of the transformer insulation structure, it is not computationally efficient to use a comprehensive analytical model of the transformer including all details as e.g. bobbins, winding fastenings and oil gap barriers (see Fig. 2.49) in the optimization procedure. Instead an analytical maximum electrical field calculation is used, which is based on the image charge method [68] and which allows a fast basic insulation design check considering the maximal electrical field that has to be below a certain constraint value (see Fig. 2.44). This method considers a single insulation material permittivity and is more than 7 times faster than FEM, because only a few points along the surface of the turn with the highest potential are evaluated to estimate the highest E_{max} value.

FEM supported field conform design In the following, the FEM supported field conform post design procedure is discussed. The main insulation material is the transformer oil MIDEL7131 [74] with a relative permittivity of 3.2. All other insulation materials are chosen with

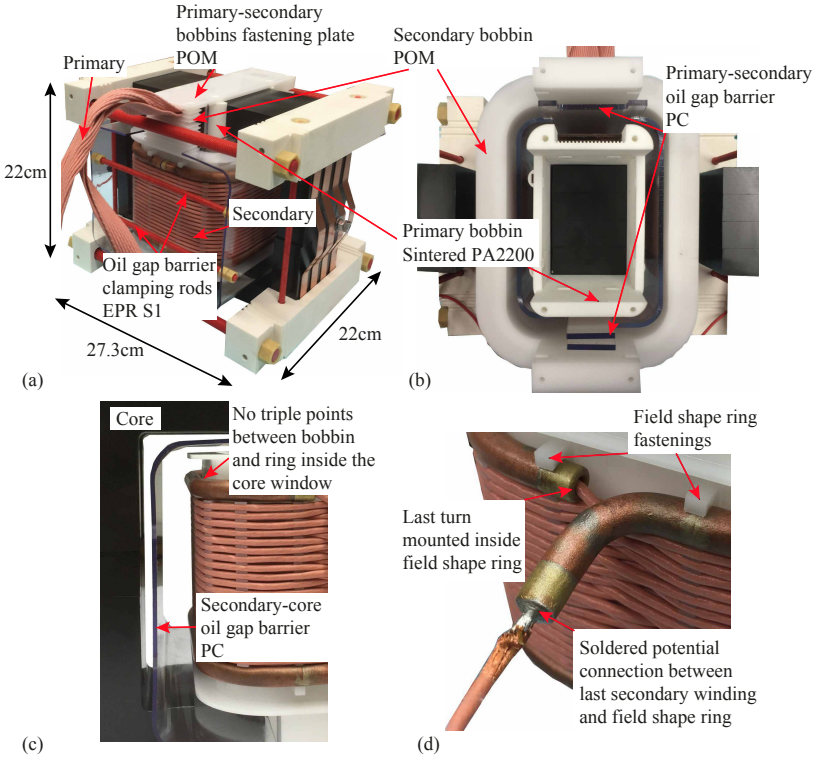


Figure 2.49: (a) Transformer prototype (built by AMPEGON AG). (b) Top view of the transformer, which has no mountings between primary and secondary inside the transformer, (c) core window with oil gap barrier and (d) last turn mounted inside the field shape ring.

respect to the transformer oil such that they have a similar permittivity (see Tab. 2.14) to avoid local field enhancements at the boundary layer of different materials and maximum electrical strength.
Fig. 2.49 (a) shows the transformer prototype, which has no fastenings between the primary and the secondary bobbin inside the transformer in order to avoid creepage paths (see Fig. 2.49 (b)). The bobbins are fastened outside of the core window at the top and the bottom of the transformer, resulting in a longer creepage distance between the windings (see Fig. 2.50 (a) and (b)). The maximum field strength occurs at

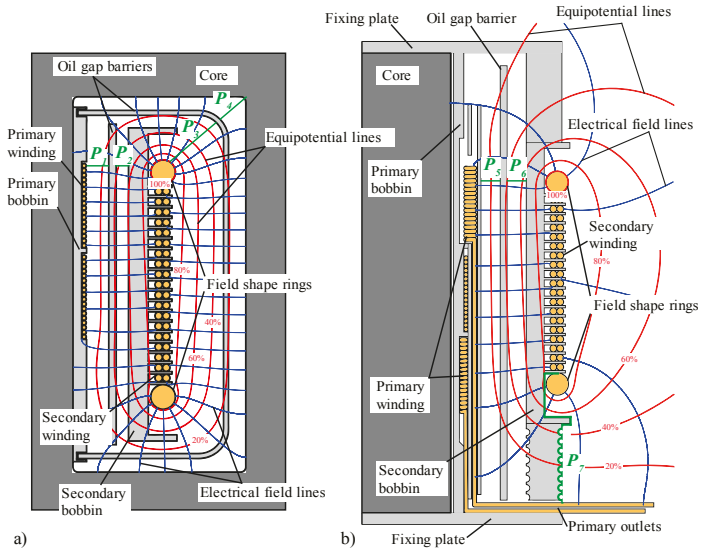


Figure 2.50: Electrical field and potential distribution (a) inside the core window and (b) at the front side of the transformer with the considered oil (P_1-P_6) and creepage paths (P_7).

the field shape ring inside the core window. Hence, triple points [71] between the field shape rings and the secondary bobbin inside the core window must be avoided (see Fig. 2.49 (c)). Thus, all field shape ring fastenings are located in a region of weak E-field outside the core win-

Table 2.14: Material parameters

Material	**Permitivity**	**Electrical strength (kV/mm)**
POM [93]	3.5	50
PC [94]	3	30
PA2200 [95]	3.8	92
EPR S1 [96]	5	10
Material	**Permitivity**	**Breakthrough voltage (kV)**
MIDEL7131 [74]	3.2	75

dow at the front of the secondary bobbin as can be seen in Fig. 2.49 (d). The primary bobbin is completely sintered of PA2200 material in a 3D printing process. This process allows complex designs but the resulting components are not void free [97], so this material is used only in non critical electrical field areas. The secondary bobbin is milled out of a single solid POM block to minimize voids and component intersections (see Fig. 2.49 (b)). Additionally, silk wrapped Litz-wire is used instead of foil so that no air bubbles are trapped beneath the foil.
An inappropriate design of the insulation causes partial discharges as well as sliding discharges which can harm the insulation of the transformer permanently and lead to arcs between the windings or the core. Oil gap barriers between primary and secondary winding as well as between the secondary winding and the core are used to counter the decreasing electrical strength of long oil gaps due to the volume and the area effect [71]. Therefore, for long life times a proper insulation design is necessary and a detailed analysis of the electrical field distribution along long oil paths (P_1-P_6, see Fig. 2.50 (a) and (b)) and critical creepage paths (P_7, see Fig. 2.50 (b)) was carried out with the help of the Weidmann design curve method [72]. There, the ratio of oil design curves ($E_d(z)$) which are derived from homogenous electrical breakdown tests [73] and the averaged cumulated electrical field strength E_{avg} along certain path lenghts (z) is calculated, resulting in safety factor curves q [71].

$$E_{avg}(z) = \frac{1}{z}\int_0^z E(z')dz' \tag{2.126}$$

$$q = \frac{E_d(z)}{E_{avg}(z)} \tag{2.127}$$

$E(z')$ is the electrical field at point z'. The factor q has to be multiplied by 0.7 if used for creepage paths [71]. The used design curve is derived from lightning impulse tests and downscaled by a design insulation level (DIL) factor of 2 to 50 Hz conditions in [75], which is in the same frequency range as the pulse repetition rate of 14 Hz. For a valid design, the q-values of all evaluated paths have to be above 1 (see Fig. 2.51). With this method, insulation designs with homogenous as well as with strongly inhomogenous field distributions can be investigated. Finally, applying this method results in an electrical field conform design, which means that the equipotential lines have mostly tangential components

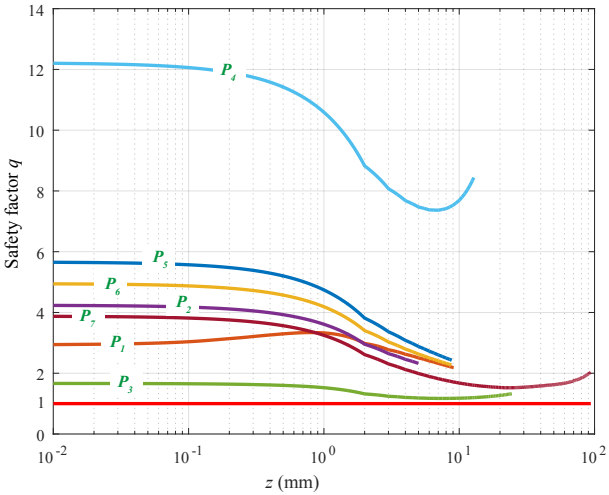


Figure 2.51: Evaluated oil gap (P_1-P_6) and creepage paths (P_7). For a valid design all q curves have to be above 1.

along the surface of insulation boundaries, e.g. oil gap barriers (see Fig. 2.50). Hence, the insulator is stressed mostly by the normal component of the electrical field and has its maximum electrical strength.

2.4.3 Measurement results

For verifying the design, partial discharge and output pulse measurement results are presented in the following.

2.4.3.1 Partial discharge measurements

For long life times, it is not sufficient to know if the transformer withstands a certain voltage level without any breakthroughs. It is also of high importance to know if the transformer is suffering from partial discharges. Such discharges can harm the insulation permanently during normal operation and may lead to serious failures. Therefore, in this section the results of comprehensive partial discharge tests are presented.
The insulation of a single SPRC bm transformer has to withstand an

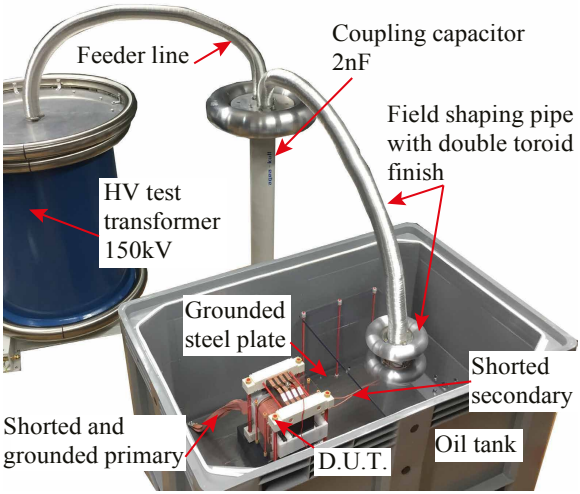


Figure 2.52: Partial discharge measurement system

operating voltage of 14.4 kV. Due to the series connection of the basic modules (see Fig. 2.43) the required isolation voltage is increasing by 14.4 kV per SPRC bm. Hence, the last transformer in the series connection has to isolate the full output voltage of 115 kV (= 8 x 14.4 kV). Fig. 2.52 shows the partial discharge measurement setup. The transformer (DUT) is placed inside the oil tank where its primary is shorted and grounded via the metal plate. The secondary is also shorted and connected to the high voltage electrode inside the double toroid. This double toroid is used to compensate the different material intersections at the end of the field shaping pipe, which could lead to additional external partial discharges. The whole setup is placed in a Faraday cage and has a ground noise level of about 300 fC. For optimal test conditions, the oil has been processed through a filtration system resulting in a relative moisture level lower than 6 %. To reduce possible partial discharges to a minimum, it is important to remove the air out of the DUT. Therefore, the oil tank has been filled under a pressure of 200 mbar below atmospheric pressure. Further reduction of air bubbles has been achieved by rotating the DUT within the oil. All measurements have been carried out at a room temperature of 23.5 °C. The partial discharges Q are recorded with an Omicron MPD600 measure-

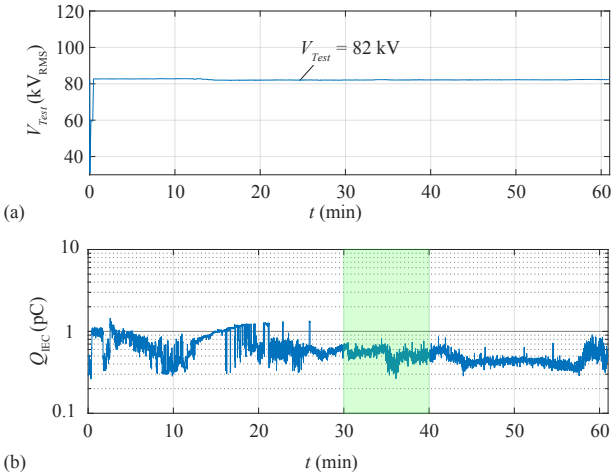


Figure 2.53: (a) Applied stress voltage $V_{Test} = 82\,\mathrm{kV_{RMS}}$ with a test duration of 60 min and (b) averaged measured partial discharges level Q_{IEC} which has been weighted considering [98]. The green interval is used for Fig. 2.54

ment system [99] and are evaluated according to the IEC 60270:2000 standard [98] leading to Q_{IEC}.

For a valid insulation design, the DUT has to pass the following test procedure. First, the nominal operation voltage ($115\,\mathrm{kV}/\sqrt{2} = 82\,\mathrm{kV_{RMS}}$, frequency $f = 50\,\mathrm{Hz}$) is applied as test voltage V_{test} to the DUT for 60 min. No breakthrough should occur and the partial discharge level Q_{IEC} should be below 2 pC. Afterwards, V_{test} is increased stepwise up to a voltage of $110\,\mathrm{kV_{RMS}}$ (136 %) with a test duration T_{Test} of 5 min for each step. To pass the test, no breakthrough must occur. The DUT passed the first test with a Q_{IEC} value far lower than 2 pC, as can be seen in Fig. 2.53. Fig. 2.54 shows a typical phase resolved discharge pattern which has been recorded during the green time interval in Fig. 2.53 (b). Most of the discharges occur at or near the positive or the negative half wave maximum of the test sinus. This could be interpreted as a combination of corona and void or surface discharges with single ended contact to one electrode according to [71]. Also the second test is passed successfully as depicted in Fig. 2.55. In the next step, V_{Test} is increased stepwise (+9 %) from +100 % to

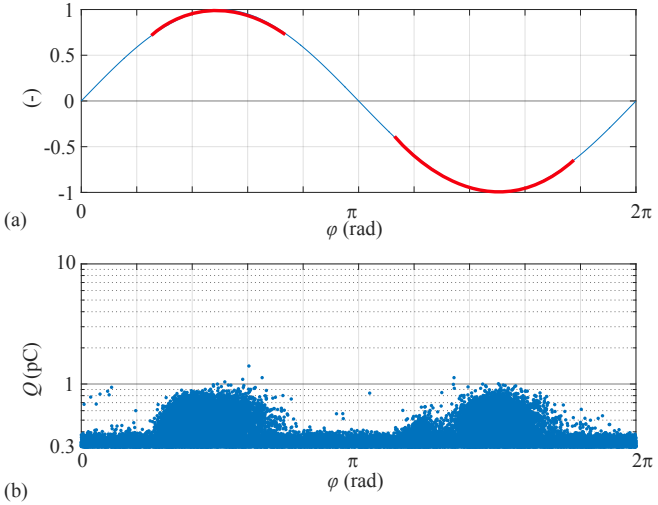


Figure 2.54: (a) Red high lighted parts show the region of the normalized test voltage sinus where discharges mostly occur and (b) phase resolved non averaged partial discharges Q measured during the green time interval in Fig. 2.53 (b).

+136 % (see Fig. 2.55 (a)). There, also and no breakthrough occurred (see Fig. 2.55 (b)). The Q_{IEC} level still remains below 2 pC for the first two voltage steps. The peaks in A', A" and A"' are caused by the variable ratio transformer which is the controlled primary main supply of the HV test transformer.

2.4.3.2 Pulse measurements

Figure 2.56 (a) shows the measured pulsed output voltage $V_{01,meas}(t)$ of a single SPRC bm operated under nominal conditions, with a pulse length of 3.5 ms and a repetition rate of 14 Hz. The module is open loop controlled and no droop compensation is active. The green curve is the mean average voltage $V_{01,avg}(t)$ of the measured output voltage and is shown to determine the rise and the fall time. Both times in Fig. 2.56 (b) and (c) are well below the given limits in Table 2.10. No breakthroughs occurred and all temperatures of the oil-immersed

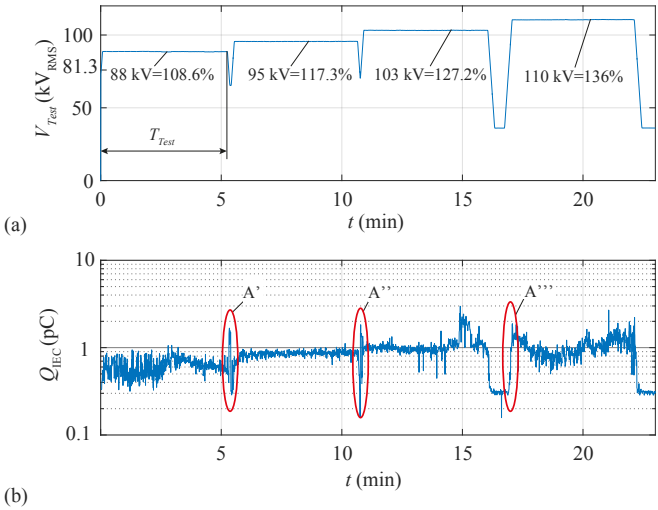


Figure 2.55: (a) Stepwise increased stress voltage with a test interval $T_{Test} \geq 5$ min and (b) averaged measured partial discharges level Q_{IEC} which has been weighted considering [98]. The peaks A', A" and A"' are caused by the main supply of the HV test transformer.

transformer did not exceed the temperature limits during the test duration of 60 min. Tab. 2.15 summarizes the optimized parameters of the transformer.

2.4.4 Conclusion

In this paper, a design procedure of a 14.4 kV nominal output voltage, 100 kHz transformer with an isolation voltage of 115 kV is presented. The procedure contains a generalized magnetic model for the leakage and an electrical model for the parasitic capacitance estimation which are proven by measurements and FEM calculations. The error is lower than 2 % in the case of the leakage inductance whereas in the case of the stray capacitance the error is in the range of −25 % if only the permittivity of air is used for the calculations. The error is decreased below 2 % if all permittivities of the different insulation materials are considered. In addition, a comprehensive insulation design procedure which is also part of the transformer optimization is derived in detail.

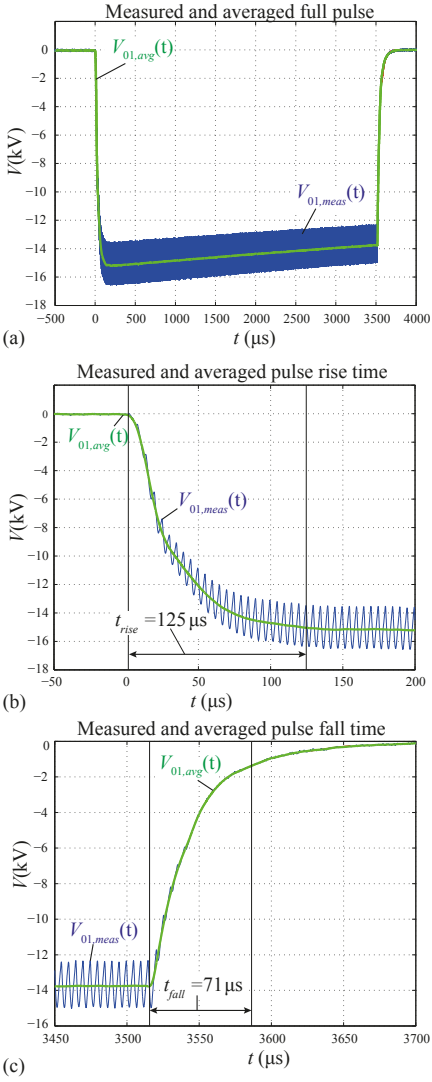


Figure 2.56: (a) Measured full pulse voltage $V_{01,meas}(t)$ and mean averaged pulse voltage $V_{01,avg}(t)$. (b) Rise time t_{rise} and (c) fall time t_{fall} of the measured pulse.

Table 2.15: Optimization results of the SPRC-bm transformer in the nominal operation point given in Tab. 2.10.

Electric and magnetic parameters		**Dimensions**	
V_{Sec}	14.4 kV	l	27.3 cm
I_{Prim}	1200 A	w	22 cm
f	100 kHz – 110 kHz	h	22 cm
E_{max}	< 12 kV/mm	V_C	2.1504 dm^3
B_{max}	<= 200 mT		
Core			
Type:		Ferrite K2008 U126/20	
# of cores:		16	
Windings			
Type:		HF-Litz wire	
Primary Wndg.	2	18 x 405 x 0.071 mm	
Secondary Wndg.	40	1125 x 0.071 mm	
Losses			
Core:	108 W	Windings:	28.5 W
Parasitics in air			
C_d	21.7 pC	L_σ	0.83 µH

It consists of a fast analytical maximum electrical field evaluation used during the automatic optimization of the transformer and a field conform post processing isolation design check. The resulting insulation system is verified by partial discharge measurements. First, a 60 min long test at nominal voltage is performed and afterwards the test voltage has been increased from 100 % to 136 % in 9 % voltage steps. Each voltage step is applied for 5 min. Both tests are passed with no breakthroughs and the partial discharge level is lower then 2 pC at nominal voltage. For validating the design additionally, pulse measurements of a SPRC bm, with a pulse length of 3.5 ms and a repetition rate of 14 Hz are presented. No breakthroughs occurred and all temperatures of the oil-immersed transformer did not exceed the temperature limits during the test duration of 60 min.

ACKNOWLEDGMENT

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2.5 Conference I.: Output Voltage Ripple Analysis for Modular Series Parallel Resonant Converter Systems with Capacitive Output Filter

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Accepted for publication in the 20th European Conference on Power Electronics and Applications 2018 (EPE'18 ECCE-Europe)

Abstract

In this paper, an analysis of the output voltage ripple of modular series parallel resonant converter systems with capacitive output filter is presented. An analytical description of the output voltage ripple of output series, output parallel as well as output parallel-output series connections of series parallel resonant converter basic modules is given. The derived equations can be used for investigating the voltage ripple due to component tolerances and non-optimal interleaving angles. The analytical results obtained by simulations and calculations match well with the measurement results. The verification of the determined equations is performed for different switching frequencies over the full range of possible interleaving angles. The measured results also match well for the time dependent waveforms.

2.5.1 Introduction

Series parallel resonant converter systems are used in many industrial applications, as e.g. telecom power supplies [100] or high output DC voltage generators [40]. Often only a single series parallel resonant converter basic module (SPRC-Bm) is applied as depicted in Fig. 2.57 (a) and the output filter C_f is sufficient to keep the output voltage ripple low. However, in high voltage pulsed power applications several modules are required [101]. An example is the european spallation source (ESS) modulator system [68], where eight SPRC-Bms stacks are connected in series at the output in order to generate the required output voltage of V_Out =115 kV and to keep the output voltage ripple low. Each stack is formed by two SPRC-Bms connected in parallel, to achieve an output power of 2.88 MW. In the considered system, a maximum output voltage ripple of $\Delta v_{C\mathrm{f}} \leq 1\,\%$ of V_Out and a maximum

energy $E \leq 10\,\mathrm{J}$, which is stored in the filter capacitor is allowed. To reduce the ripple voltage, all modules are interleaved. The value of the output capacitor C_f is limited to a maximal value due to the maximum stored energy constraint, resulting in a minimal voltage ripple.
In the literature, the ripple analysis for a single SPRC-Bm is explained in [102] and an estimation is presented in [103], but there is a lack for systems with an arbitrary number of modules and arbitrary output connections. Therefore, a general detailed analysis of the output voltage ripple of SPRC-Bms with arbitrary output connections and interleaved operation is derived in this paper.
In section 2.5.2, the ripple derivation of a single SPRC-Bm (Fig. 2.57 (a)) is given and the formulas for a pure output series (OS) (Fig. 2.57 (b)), a pure output parallel (OP) (Fig. 2.57 (c)) and an output parallel-output series (OP-OS) (Fig. 2.57 (d)) systems are derived. The models are verified by measurement and simulation results in section 2.5.3.

2.5.2 Output voltage ripple analysis

In this section, the output voltage ripple analysis of a single SPRC-Bm is given. Afterwards, equations for series and parallel output connections of an arbitrary number of SPRC-Bms are derived.

2.5.2.1 Output voltage ripple of a single SPRC-Bm

The analysis of the output voltage ripple of a SPRC-Bm is based on the analysis presented in [102]. For the sake of completeness, the main governing equations, which are used for the further analysis in sections 2.5.2.2 and 2.5.2.3, are shortly repeated. The definition of the used variables and components are given in Fig. 2.57 (a) and Fig. 2.57 (e). The output current of the rectifier i_Rec is defined by:

$$i_\mathrm{Rec}(\omega_\mathrm{s}t) = \begin{cases} 0 & 0 \leq \omega_\mathrm{s}t < \psi \\ I_{Ls}\sin(\omega_\mathrm{s}t) & \psi \leq \omega_\mathrm{s}t < \pi \\ 0 & \pi \leq \omega_\mathrm{s}t < \pi + \psi \\ -I_{Ls}\sin(\omega_\mathrm{s}t) & \pi + \psi \leq \omega_\mathrm{s}t < 2\pi \end{cases} \tag{2.128}$$

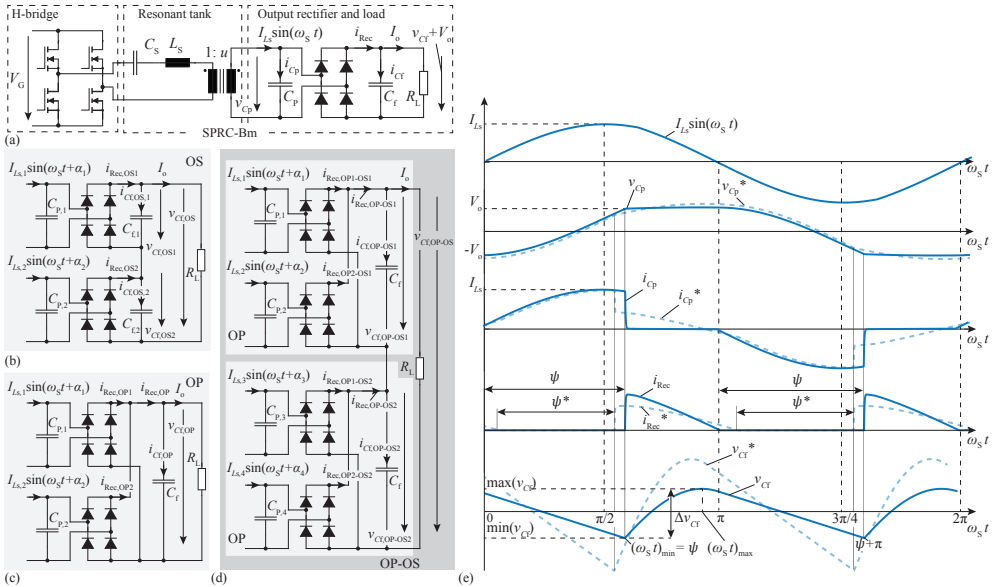

Figure 2.57: (a) Single SPRC-Bm formed by a H-bridge, a resonant tank and the output rectifier stage with load. The total output voltage is the superposition of the ripple voltage v_{Cf} and the average voltage V_o. Output rectifier stages of (b) an output series connected (OS) system, of (c) an output parallel connected (OP) system and of (d) an output parallel-output series connected (OP-OS) system. The averaged output voltages V_o are not shown in (b) to (d), because only the ripple voltages $v_{Cf,Oxx}$ are in the scope of interest. (e) Simulated typical basic current and voltage output circuit waveforms of a SPRC-Bm (see Fig. 2.57 (a)). The solid line waveforms are of a SPRC-Bm, where $C_f \gg C_P$ and the dashed line waveforms are if $C_f \approx C_P$. The averaged output voltage V_o is not shown, because just the ripple voltage v_{Cf} is in the scope of interest.

with

$$\psi = \arccos\left(\frac{\pi - 2\omega_\mathrm{s} R_\mathrm{L} C_\mathrm{P}}{\pi + 2\omega_\mathrm{s} R_\mathrm{L} C_\mathrm{P}}\right), \tag{2.129}$$

where ψ is the non-conduction angle of the rectifier as shown in Fig. 2.57 (e) and ω_s is the angular switching frequency. The peak secondary transformer current I_{Ls} is calculated based on (3) in [54]

$$I_{Ls} = \frac{2V_\mathrm{o}\omega_\mathrm{s} C_\mathrm{P}}{1 + \cos(\pi - \psi)}, \tag{2.130}$$

and also the average output voltage V_o is taken from [54]. The load current I_o is the average current of the output rectifier current i_Rec during a switching period

$$I_\mathrm{o} = \frac{1}{\pi}\int_{\psi}^{\pi} i_\mathrm{Rec}\,\mathrm{d}(\omega_\mathrm{s} t) = I_{Ls}(1 + \cos(\psi))\frac{1}{\pi}. \tag{2.131}$$

Applying Kirchhoff's law, the current $i_{C\mathrm{f}}$ of the filter capacitor C_f can be calculated as

$$i_{C\mathrm{f}}(\omega_\mathrm{s} t) = i_\mathrm{Rec}(\omega_\mathrm{s} t) - I_\mathrm{o}. \tag{2.132}$$

where the load current I_o is the average current of the output rectifier current i_Rec during a switching period. Using (2.132) and solving the integral results in the filter capacitor voltage $v_{C\mathrm{f}}$

$$\begin{aligned} v_{C\mathrm{f}}(\omega_\mathrm{s} t) &= \frac{1}{\omega_\mathrm{s} C_\mathrm{f}}\int i_{C\mathrm{f}}(\omega_\mathrm{s} t)\,\mathrm{d}(\omega_\mathrm{s} t) \\ &= \begin{cases} -\dfrac{I_\mathrm{o}(\omega_\mathrm{s} t)}{C_\mathrm{f}\omega_\mathrm{s}} + X_1 & 0 \le \omega_\mathrm{s} t < \psi \\ -\dfrac{I_\mathrm{o}}{C_\mathrm{f}\,\omega_\mathrm{s}}\left(\dfrac{\pi\cos(\omega_\mathrm{s} t)}{1+\cos(\psi)} + (\omega_\mathrm{s} t)\right) + X_2 & \psi \le \omega_\mathrm{s} t < \pi, \end{cases} \end{aligned} \tag{2.133}$$

where X_1 and X_2 are integration constants. The angle $(\omega_\mathrm{s} t)_\mathrm{max}$ related to the maximum of $v_{C\mathrm{f}}$ is calculated by setting the derivative of the second part of (2.133) to zero

$$\frac{\mathrm{d}}{\mathrm{d}(\omega_\mathrm{s} t)}\left(\frac{-I_\mathrm{o}}{C_\mathrm{f}\,\omega_\mathrm{s}}\left(\frac{\pi\cos(\omega_\mathrm{s} t)}{1+\cos(\psi)} + (\omega_\mathrm{s} t)\right) + X_2\right) = 0 \tag{2.134}$$

and solving (2.134) for $\omega_\mathrm{s} t$. To find the maximum, the result has to be shifted by π, what results in

$$(\omega_\mathrm{s} t)_\mathrm{max} = \pi - \arcsin\left(\frac{1+\cos(\psi)}{\pi}\right). \tag{2.135}$$

Table 2.16: Component values of a single SPRC-Bm used for the calculations in Fig. 2.58 and in Fig. 2.59.

L_S (μH)	C_S (nF)	C_P (nF)	R_L (Ω)	V_G (V)	u (−)
4.24	840	4.24	1150	400	20

The angle related to the minimum of v_{Cf} is

$$(\omega_s t)_{\min} = \psi. \tag{2.136}$$

Finally, the output voltage ripple Δv_{Cf} is given by

$$\begin{aligned}\Delta v_{Cf} &= v_{Cf}((\omega_s t)_{max}) - v_{Cf}((\omega_s t)_{min}) = \\ &= \frac{I_o}{\omega_s C_f}\left[\frac{\left[\arcsin\left(\frac{1+\cos(\psi)}{\pi}\right)+\psi\right][1+\cos(\psi)]}{(1+\cos(\psi))}+\right. \\ &\left.+\ \frac{\sqrt{\pi^2-(1+\cos(\psi))^2}-\pi}{(1+\cos(\psi))}\right].\end{aligned} \tag{2.137}$$

Equation (2.137) is derived based on the assumption that $C_f \gg C_P$, which results in a nearly perfectly clamped parallel capacitor voltage v_{Cp} during the rectifier conduction interval as can be seen in Fig. 2.57 (e)). If $C_f \approx C_P$, the voltage ${v_{Cp}}^*$ is not strictly constant during the rectifier conduction interval (compare v_{Cp} and ${v_{Cp}}^*$ in Fig. 2.57 (e)) and the current $I_{Ls}\sin(\omega_s t)$ is divided into ${i_{Cp}}^*$ and ${i_{Rec}}^*$, as can be seen in Fig. 2.57 (e). This results in a different non-conduction angle ψ^* and leads to a larger error of (2.137). Figure 2.58 (a) shows the relative error between the simulated and the calculated output voltage ripple and Fig. 2.58 (b) shows the relative error between the simulated and the calculated averaged output voltage V_o related to C_f/C_P for different switching frequencies f_s of a single SPRC-Bm. It is clearly shown in Fig. 2.58 (b) that the variation of the filter capacitor C_f only has a minor effect (approx. ± 10 % in the worst cases) on the averaged output voltage and can be therefore neglected. The frequency range (100 kHz - 110 kHz) is chosen with respect to the design in [68]. The specifications for the calculations and the simulations, are given in Tab.2.16. Figure 2.59 shows the relative deviation between the fourier series (2.139) and

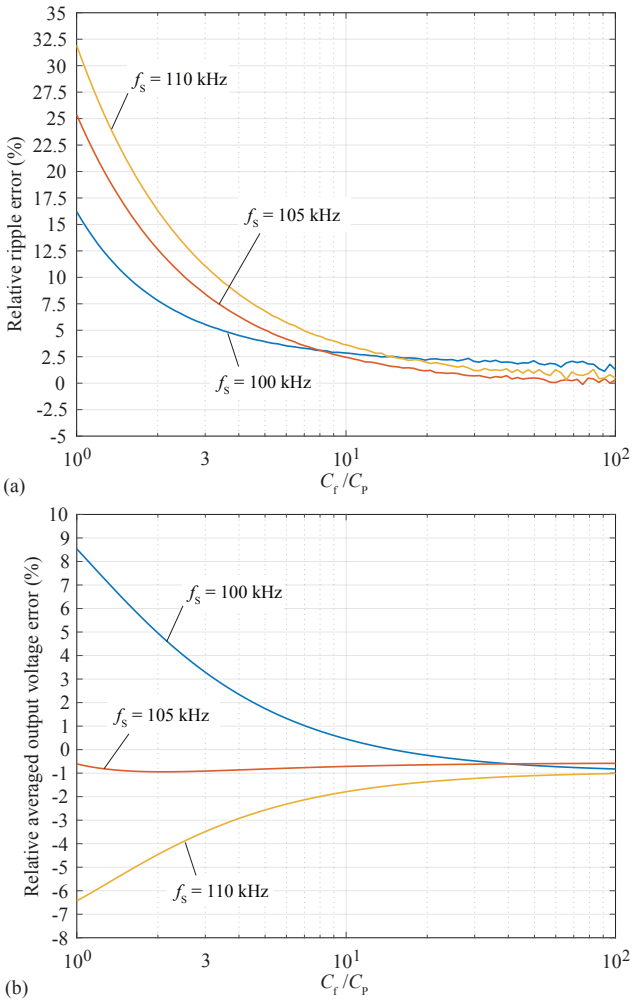

Figure 2.58: (a) Relative error between the calculated (with (2.137)) and the simulated output voltage ripple of a single SPRC-Bm for different switching frequencies. (b) Relative error between the calculated and the simulated averaged output voltage V_o of a single SPRC-Bm for different switching frequencies.

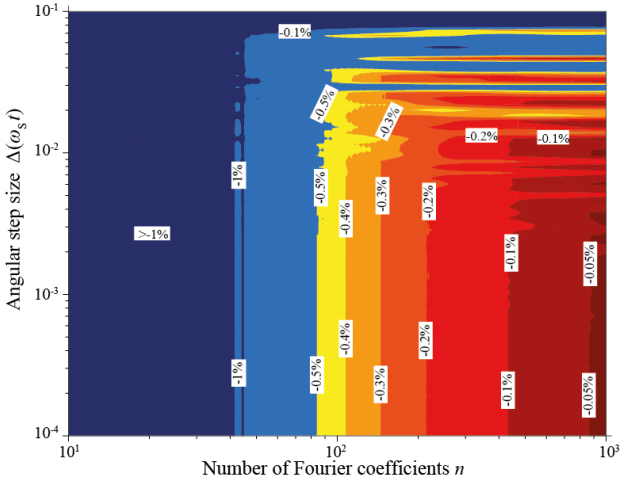

Figure 2.59: Relative deviation of the fourier series (2.139) and the exact solution (2.137) of the output voltage ripple Δv_{Cf} in dependance of the angular step size $\Delta(\omega_s t)$ used in (2.139) and the number of fourier coefficients n.

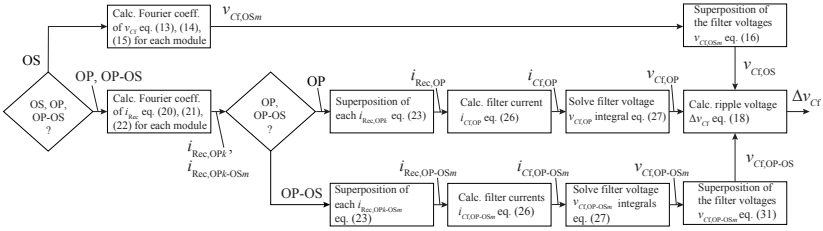

Figure 2.60: Principle ripple calculation flow chart of the output series (OS), output parallel (OP) and the output parallel-output series (OP-OS) system.

the exact solution (2.137) of the output voltage ripple Δv_{Cf} in dependance of the angular step size $\Delta(\omega_s t)$ used in (2.139) and the number of fourier coefficients n. The principle ripple calculation procedure for an OS, an OP and an OP-OS system is depicted in the flow chart of Fig. 2.60, as a kind of ripple calculation guide. The detailed derivations according to the flow chart are given in the following.

2.5.2.2 Output voltage ripple of an OS system

Figure 2.57 (b) shows the output circuit of an OS system. There, both rectifiers are connected in series. In order to investigate an interleaved operation, (2.133) has to be developed into its fourier series. The integration constants X_1 and X_2 are calculated by

$$v_{Cf}(\psi) = 0 \rightarrow \begin{cases} X_1 = \dfrac{I_o \psi}{\omega_s C_f} \\ X_2 = \dfrac{I_o}{C_f \omega_s} \left(\dfrac{\pi \cos(\psi)}{1 + \cos(\psi)} + \psi \right) \end{cases} \tag{2.138}$$

The time dependent fourier series of the output voltage ripple $v_{Cf}(\omega_s t)$ is given by

$$v_{Cf}(\omega_s t) = \frac{a_o}{2} + \sum_{n=2}^{\infty} a_n \cos(n\omega_s t) + b_n \sin(n\omega_s t) \tag{2.139}$$

with its fourier coefficients

$$a_o = \frac{I_o \left[\pi \cos(\psi) - \pi + 2\sin(\psi) + 2\psi\right]}{\omega_s C_f \left(\cos(\psi) + 1\right)} \tag{2.140}$$

$$a_n = \frac{I_o \left[1 + (-1)^n\right] \left[\frac{\sin(n\psi - \psi)(n+1) + \sin(n\psi + \psi)(1-n)}{2}\right]}{n C_f \omega_s \left(\cos(\psi) + 1\right)\left(n^2 - 1\right)} \tag{2.141}$$

$$b_n = -\frac{I_o \left[1 + (-1)^n\right] \left[\frac{\cos(n\psi - \psi)(n+1) + \cos(n\psi + \psi)(1-n)}{2} + 1\right]}{n C_f \omega_s \left(\cos(\psi) + 1\right)\left(n^2 - 1\right)}. \tag{2.142}$$

The total output voltage ripple is determined by the superposition of the output voltages of each SPRC-Bm

$$v_{Cf,OS}(\omega_s t) = \sum_{m=1}^{M} v_{Cf,OSm}(\omega_s t + \alpha_m) \tag{2.143}$$

with

$$\alpha_m = \kappa_m - \varphi_m \quad \text{and} \quad \kappa_m = \frac{(m-1)\pi}{M}. \tag{2.144}$$

The angle α_m is the difference between the optimal interleaving angle κ_m of each SPRC-Bm and its input impedance angle φ_m, which is calculated with (35) in [54]. M is the number of SPRC-Bm in series at

the output. Computing the maximum and the minimum of the output ripple voltage $v_{Cf,OS}$ results in the output voltage ripple Δv_{Cf}

$$\Delta v_{Cf} = \max(v_{Cf,OS}) - \min(v_{Cf,OS}). \tag{2.145}$$

2.5.2.3 Output voltage ripple of an OP system

Figure 2.57 (c) shows the output circuit of an OP system. There, both rectifiers are connected in parallel. In order to investigate an interleaved operation, (2.128) has to be developed into its fourier series. The time dependent fourier series of the output rectifier current i_{Rec} is given by

$$i_{Rec}(\omega_s t) = \frac{a_o}{2} + \sum_{n=2}^{\infty} a_n \cos(n\omega_s t) + b_n \sin(n\omega_s t), \tag{2.146}$$

with its fourier coefficients

$$a_o = I_{Ls} \frac{2(\cos(\psi) + 1)}{\pi} \tag{2.147}$$

$$a_n = -\frac{I_{Ls}\left[1 + (-1)^n\right]\left[\frac{\cos(n\psi-\psi)(n+1)+\cos(n\psi+\psi)(1-n)}{2} + 1\right]}{\pi\left(n^2 - 1\right)} \tag{2.148}$$

$$b_n = \frac{I_{Ls}\left[1 + (-1)^n\right]\left[\frac{-\sin(n\psi-\psi)(n+1)+\sin(n\psi+\psi)(n-1)}{2}\right]}{\pi\left(n^2 - 1\right)}. \tag{2.149}$$

The total output rectifier current $i_{Rec,OP}$ is determined by the superposition of the rectifier currents of each SPRC-Bm

$$i_{Rec,OP}(\omega_s t) = \sum_{k=1}^{K} i_{Rec,OPk}(\omega_s t + \alpha_k) \tag{2.150}$$

with

$$\alpha_k = \kappa_k - \varphi_k \quad \text{and} \quad \kappa_k = \frac{(k-1)\pi}{K}. \tag{2.151}$$

The angle α_k is the difference of the optimal interleaving angle κ_k of each SPRC-Bm and its input impedance angle φ_k. K is the number of SPRC-Bm in parallel at the output. The integral of the load current I_o

$$I_o = \frac{1}{\pi} \int_0^{\pi} i_{Rec,OP}\, \mathrm{d}(\omega_s t) \tag{2.152}$$

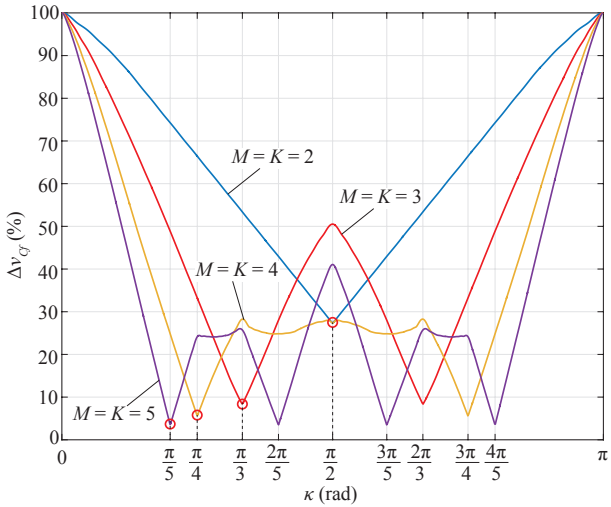

Figure 2.61: Optimal interleaving angles (red circles) for OP or OS system with two to five SPRC-Bms. The component values are given in Tab.2.16 and are the same for all modules. The used switching frequency is 104.5 kHz and the filter capacitor C_f is 15.49 nF.

has to be solved numerically and the filter current $i_{Cf,\mathrm{OP}}$ is given by

$$i_{Cf,\mathrm{OP}}(\omega_\mathrm{s}t) = i_{\mathrm{Rec,OP}}(\omega_\mathrm{s}t) - I_\mathrm{o}. \tag{2.153}$$

The output voltage $v_{Cf,\mathrm{OP}}$ is calculated numerically by

$$v_{Cf,\mathrm{OP}}(\omega_\mathrm{s}t) = \frac{1}{\omega_\mathrm{s}C_\mathrm{f}} \int i_{Cf,\mathrm{OP}}(\omega_\mathrm{s}t)\,\mathrm{d}(\omega_\mathrm{s}t) + X_3, \tag{2.154}$$

where the integration constant X_3 is set to zero, because the offset in the output voltage is not in the scope of interest for the ripple calculation. Inserting (2.154) in (2.145) results in the total output ripple voltage Δv_{Cf}.
The optimal interleaving angle κ, which results in a minimum voltage ripple is exemplary given in Fig. 2.61 for 2 to 5 OS or OP systems. The component values for the calculations are given in Tab.2.16 and are the same for all modules. The switching frequency is 104.5 kHz and the filter capacitance C_f is 15.49 nF.

Table 2.17: Component and input values of the OP prototype system with parallel connected outputs used for the calculation and simulation results in Fig. 2.63.

C_{f1}(nF)		8.48		f_{s1}(kHz)		104.5	
C_{f2}(nF)		28.48		f_{s2}(kHz)		104	
L_{S} (μH)	C_{S} (nF)	C_{P} (nF)	V_{G} (V)	u (−)	R_{L} (Ω)	n (−)	$\Delta\omega_{\mathrm{s}}t$ (mrad)
4.29	840	4.24	400.3	20	1118	200	0.318

2.5.2.4 Output voltage ripple of an OP-OS system

Figure 2.57 (d) shows the rectifier circuit of an OP-OS system, which is a series connection of OP systems. The output voltage for each OP system is calculated using (2.146) to (2.154), where (2.151) is replaced by the following (2.155), which determines the optimal interleaving angle of each SPRC-Bm and its input impedance angle $\varphi_{k,m}$. It is assumed that each OP system consists of K SPRC-Bms and M is the number of OP systems in series.

$$\alpha_{k,m} = \kappa_{k,m} - \varphi_{k,m} \tag{2.155}$$

with

$$\kappa_{k,m} = \frac{(k-1)\pi}{K} + \frac{(m-1)\pi}{MK} \tag{2.156}$$

and

$$k = [1 \dots K], \quad m = [1 \dots M]. \tag{2.157}$$

The total output voltage $v_{\mathrm{Cf,OP\text{-}OS}}$ is calculated by the superposition of each OP output voltage by

$$v_{\mathrm{Cf,OP\text{-}OS}}(\omega_{\mathrm{s}}t) = \sum_{m=1}^{M} v_{\mathrm{Cf,OP\text{-}OS}m}(\omega_{\mathrm{s}}t + \alpha_{k,m}). \tag{2.158}$$

Again, using (2.158) in (2.145) results in the output ripple voltage Δv_{Cf}.

2.5.3 Simulation and measurement results

In this section, the analysis is verified by comparing measurement and simulation results of an OP prototype system, which consists of two

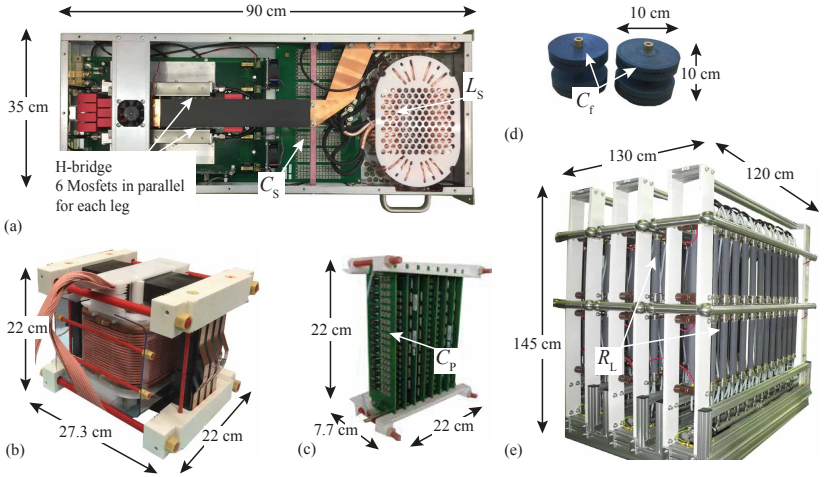

Figure 2.62: (a) Single SPRC-Bm with H-bridge, series inductor L_S and capacitor C_S. (b) High voltage high frequency transformer. (c) Output rectifier with parallel capacitor C_P, (d) filter capacitors C_f and (e) high voltage load R_L. For the measurements, two SPRC-Bms are connected in parallel at the output according to Fig. 2.57 (c).

SPRC-Bms. The pictures of a single SPRC-Bm with series inductor L_S and capacitor C_S, of the output rectifier with the parallel capacitor C_P, of the output filter C_f and of the high voltage load R_L are shown in Fig. 2.62. The component and input voltage values for both prototype SPRC-Bms, which are used for the ripple simulations and calculations, are given in Tab.2.17. Figure 2.63 (a) shows the total output voltage ripple Δv_{Cf} of the OP system, which is operated with different interleaving angles α. The evaluation is given for different filter capacitors and switching frequencies. The calculated total ripple values are in good accordance with the simulated and the measured values. Also, the calculated time dependent waveforms match well with the simulated and the measured waveforms, as could be seen in Fig. 2.63 (b). There, the OP system is operated in non interleaved mode and with a switching frequency f_s of 104 kHz.

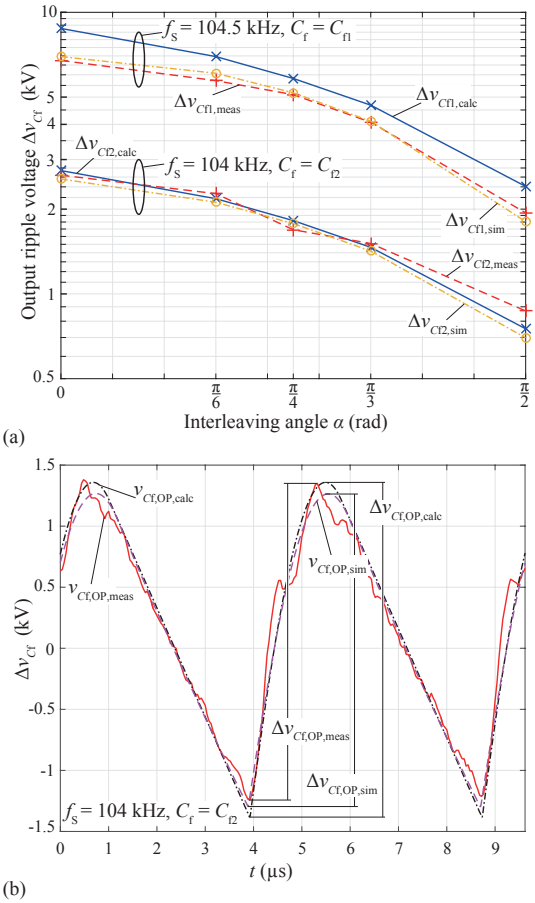

Figure 2.63: (a) Calculated $\Delta v_{Cfi,\mathrm{calc}}$, simulated $\Delta v_{Cfi,\mathrm{sim}}$ and measured $\Delta v_{Cfi,\mathrm{meas}}$ total output voltage ripple of an OP system with two modules, operated with different angels α. The comparison is given for different output filter capacitors $C_{\mathrm{f1}}/2 = C_{\mathrm{P}}$ and $C_{\mathrm{f2}}/2 = 3.35 \cdot C_{\mathrm{P}}$ (compare the relative error in Fig. 2.58 (a)). (b) Calculated $v_{Cf,\mathrm{OP,calc}}$, simulated $v_{Cf,\mathrm{OP,sim}}$ and measured $v_{Cf,\mathrm{OP,meas}}$ output voltage ripple of an output parallel (OP) prototype system with two modules, which is operated non interleaved at a switching frequency f_{s} of 104 kHz and an output filter capacitor $C_{\mathrm{f}} = C_{\mathrm{f2}}$.

2.5.4 Conclusion

In this paper, the ripple model of arbitrary output connections of series parallel resonant converter basic modules (SPRC-Bms) are derived. The analysis is based on the ripple calculations of a single SPRC-Bm and is then extended to either output parallel, output series, or output parallel and series connections of SPRC-Bms. The calculated output voltage ripple is verified by simulations and measurements of an output parallel (OP) prototype system. The analytical results match very well with the simulated and the measured results and also match well to the time dependent waveforms. The derived formulas can be used for ripple investigations caused by component tolerances or by the interleaved operation of the SPRC-Bms in order to determine the minimum required filter capacitor value.

Acknowledgment

The authors would like to thank the project partners CTI and Ampegon AG very much for their strong support of the CTI-research project 13135.1 PFFLR-IW.

List of symbols

OS	Output series connected
OP	Output parallel connected
OP-OS	Output parallel-output series connected
SPRC-Bm	Series parallel resonance converter basic module
V_{G}	Input voltage of a SPRC-Bm
V_{Out}	Output voltage of SPRC-system
V_{o}	Output voltage of a SPRC-Bm
I_{Ls}	Peak secondary transformer current
I_{o}	Load current
ψ, ψ^*	Non conduction angle of the rectifier
$\Delta(\omega_{\mathrm{s}}t)$	Angular step size
$v_{C\mathrm{p}}$,$v_{C\mathrm{p}}{}^*$	Parallel capacitor voltage
$v_{C\mathrm{f}}$	Ripple voltage
$v_{C\mathrm{f,OS}}$	Ripple voltage of an OS-system
$v_{C\mathrm{f,OP}}$	Ripple voltage of an OP-system
$v_{C\mathrm{f,OP\text{-}OS}}$	Ripple voltage of an OP-OS-system
$v_{C\mathrm{f,OS}m}$	m-th ripple voltage of an OS-system
$v_{C\mathrm{f,OP\text{-}OS}m}$	m-th ripple voltage of an OP-OS-system
i_{Rec}, $i_{\mathrm{Rec}}{}^*$	Rectifier current
$i_{\mathrm{Rec,OP}}$	Rectifier current of an OP-system
α	Phase shift angle
α_m	m-th phase shift angle of an OS-system
α_k	k-th phase shift angle of an OP-system
$\alpha_{k,m}$	k-th, m-th phase shift angle of an OP-OS-system
a_{o}, a_n, b_n	Fourier coefficients
φ	Input impedance angle
φ_m	m-th input impedance angle of an OS-system
φ_k	m-th input impedance angle of an OP-system
$\varphi_{k,m}$	k-th, m-th input impedance angle of an OP-OS-system
C_{S}	Series capacitor
L_{S}	Series inductor
C_{P}	Parallel capacitor
C_{f}	Output filter capacitor
R_{L}	Load resistor
u	Transformer ratio
E	Energy stored in the system
ω_{s}	Angular switching frequency
f_{s}	Switching frequency

$\Delta v_{C\mathrm{f}}$	Maximal voltage ripple
t	Time
$i_{C\mathrm{p}}$, $i_{C\mathrm{p}}{}^{*}$	Parallel capacitor current
$i_{C\mathrm{f}}$	Filter capacitor current
$i_{C\mathrm{f,OS}m}$	m-th filter capacitor current of an OS-system
$i_{C\mathrm{f,OP}}$	Filter capacitor current of an OP-system
$i_{C\mathrm{f,OP\text{-}OS}m}$	m-th filter capacitor current of an OP-OS-system
$i_{\mathrm{Rec,OS}m}$	m-th rectifier current of an OS-system
$i_{\mathrm{Rec,OP\text{-}OS}m}$	m-th rectifier current of an OP-OS-system
$i_{\mathrm{Rec,OP}k}$	k-th rectifier current of an OP-system
$i_{\mathrm{Rec,OP}k\text{-}\mathrm{OS}m}$	k-th, m-th rectifier current of an OP-OS-system
κ	Interleaving angle
κ_m	m-th interleaving angle of an OS-system
κ_k	k-th interleaving angle of an OP-system
$\kappa_{k,m}$	k-th, m-th interleaving angle of an OP-OS-system
n	Number of fourier coefficients
K	Number of SPRC-Bms in parallel
M	Number of OP-systems or SPRC-Bms in series
X_1, X_2, X_3	Integration constants

3

Thermal model of the high-voltage high-frequency transformer

This chapter presents the detailed analysis of a novel thermal resistance model, which is used in the thermal model of the transformer in section 2.1.3.5. The resulting expressions for solid and litz wire windings are derived based on an electrothermal analogy and only rely on data sheet parameters of the utilized wires and the insulation materials. The performance of the approach is benchmarked by two other analytical methods and the final resulting equations are validated by measurements. Finally, the developed model is employed in the equivalent thermal circuit of the finally built high-voltage high-frequency transformer, which results in a good match between the measured and the predicted temperature distribution.

3.1 Journal II.: General Analytical Model for the Thermal Resistance of Windings Made of Solid or Litz Wire

Michael Jaritz, Andre Hillers and Juergen Biela
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Abstract

In this paper, an analytical method to model the thermal resistance of windings made either of solid or litz wire is presented and validated by measurements. In addition, an extended numerical approach for litz wire windings, which also considers the twist pitch, is shown. With the presented model it is possible to describe the thermal resistance of arbitrary wire arrangements. This approach can be used in straight forward thermal designs of magnetic devices, or it can be integrated in optimization procedures to improve the thermal designs of magnetic components. The analytical models are verified by measurements with non-potted and epoxy-potted solid wire test setups and test setups for litz wire, which all show a good matching between calculated and measured values. Besides the models for the thermal resistance between the winding layers, also a method to simplify the thermal network of multi-layer windings is presented. Finally, a thermal equivalent circuit of a test transformer has been calculated, which shows a good match between the measured and the predicted temperature distribution.

3.1.1 Introduction

In many converter systems, the design of magnetic components is an important step of the overall system design. Due to the high number of degrees of freedom and geometric parameters this is often performed with the help of optimization procedures (see for example Fig. 3.1 (a)) [68]. With the core and the winding losses, the critical operating temperatures are calculated, which determine if the design is valid or if the geometry has to be modified by the optimizer. Since the winding and core losses are temperature dependent, as shown in [105], [106] and [86], it is of high importance to estimate the occurring winding and core

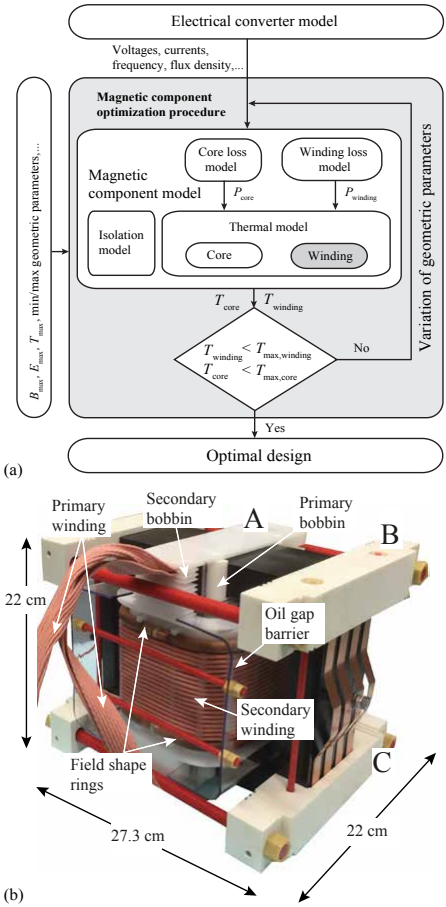

Figure 3.1: (a) General magnetic component optimization procedure. With the core and the winding losses, the critical operating temperatures are calculated, which determine if the design is valid or if the geometry has to be modified by the optimizer. (b) Example for an optimized transformer geometry (Output voltage: 14.4 kV, turns ratio: 20, output power: 9 kW, operation frequency: 100 kHz-110 kHz and isolation voltage: 115 kV). A detailed design procedure of the transformer is given in [104]. The designators A, B, and C are at the same position as in Fig. 3.12. The transformer is built by AMPEGON AG.

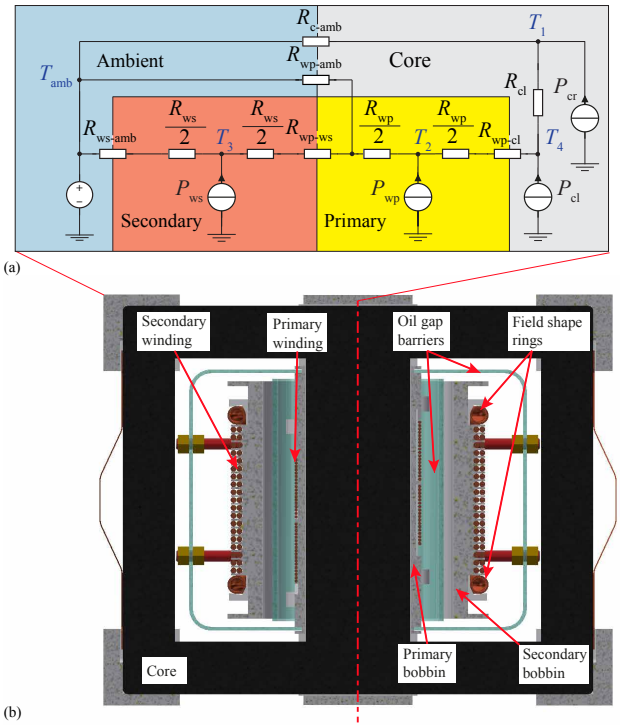

Figure 3.2: (a) Thermal equivalent circuit of the transformer from Fig. 3.1 (b). The thermal transition between core parts and windings ($R_{\text{wp-cc}}$), the heat transfer within the core (R_{cl}), between primary and secondary winding ($R_{\text{wp-ws}}$) respectively, as well as within the windings ($R_{\text{w},x}$) is performed by heat conduction. The thermal resistances between core and ambient ($R_{\text{c-amb}}$) or winding and ambient ($R_{\text{ws-amb}}$, $R_{\text{wp-amb}}$) are based on radiation and convection. The losses in the windings ($P_{\text{wp}}, P_{\text{ws}}$) and the losses in the center leg and the rest of the core ($P_{\text{cl}}, P_{\text{cr}}$) are modelled by current sources. (b) Cross section of the transformer from Fig. 3.1 (b). The circuit is valid for the symmetric half of the transformer in (b).

temperatures properly. For obtaining the temperatures in each part of the magnetic component, thermal equivalent circuits are required (see Fig. 3.2 (a)). The thermal model contains all types of heat transfer (conduction, convection and radiation) represented by equivalent thermal resistors and the losses are modeled by equivalent current sources.

Thermal capacitances are not considered in this model, because in many designs only the final temperature distribution is of interest and therefore, the thermal model in Fig. 3.2 (a) represents a steady-state model. One major challenge is the correct estimation of the winding resistance. For foil windings this is a relatively straight forward calculation as presented in [107]. However, there is a lack concerning fast and accurate analytically models for the thermal winding resistance $R_{\mathrm{w},x}$ of round solid windings and litz wire windings, which can be used in optimization procedures.

In order to obtain a time and a computational effort optimized result for the thermal behaviour of the windings, the windings are modeled with the help of thermal lumped resistor models [108–112] or simplified finite element method (FEM) models [113–117]. There, winding homogenization techniques are applied to combine the different thermal conductivities of the complex structure of a winding (e.g. the randomly distributed copper wires, the insulation material of the wires and the bonding material between the wires) into a single effective thermal conductivity, which is needed for the lumped parameter model, as well as for the simplified FEM model. Following homogenization techniques are given in the literature:

1) The authors in [118, 119] propose analytical approaches to derive the effective thermal conductivity based on the equations given by Hashin and Shtrikman (H&S) in [120], which are restricted to two components winding amalgams. In this model, it is assumed that the windings consist of copper wires and bonding material. The thermal conductivity of the thin isolation around the wires is assumed to be close to the one of the bonding material and is therefore neglected. In order to overcome the restriction to two components, the H&S approach is extended to three components amalgams in [121]. The H&S and the extended H&S (H&S+) approaches are valid for circular wire profiles and are not applicable to general conductor shapes [121]. In [122], a method is presented, which can be applied for rectangular conductor profiles. For litz wire windings a two step homogenization based on the H&S+ approximation is presented in [123]. First, the equivalent conductivity of a single litz wire bundle is calculated and in a second step, the equivalent conductivity of the litz wire bundle winding is derived, employing the effective thermal conductivity of the bundle from step one.

2) The thermal conductivity is extracted by measurements as presented in [115, 124, 125].

3) The equivalent conductivity is derived from FEM simulations, where parts of the windings are modeled in their full complexity, including all isolation components as given in [126].
The methods presented in 2) and 3) are either make use of measurements or are essentially too time consuming to be applied in optimization routines. Therefore, the focus in this paper, is the derivation of an accurate analytical expression for the thermal winding resistance $R_{\mathrm{w},x}$, which can be used in fast optimization algorithms for transformer or inductance design. The resulting expressions for solid and litz wire windings are derived based on an electrothermal analogy and only rely on data sheet parameters of the wires and the insulation materials. In order to justify the new contributions of this paper, the determined expressions are benchmarked with the H&S and the H&S+ approaches for solid wire, as well as for litz wire with the two step homogenization from method 1).
This paper is organized as follows. The derivation of the thermal resistance $R_{\mathrm{w},x}$ is given in detail in section 3.1.2. Afterwards, a simplified thermal T-equivalent circuit model for multi-layer windings is derived in section 3.1.3. In section 3.1.4 measurement results are presented. First, in section 3.1.4.1, a measurement setup to verify the results of section 3.1.2 is presented. Then, the results from the proposed calculation are compared with measurements and benchmarked with the H&S and H&S+ approximations insection 3.1.4.2. Finally, in section 3.1.4.3, the temperature distribution in a transformer is compared with the analytically predicted temperature distribution, using the new thermal winding description.

3.1.2 Derivation of the thermal resistance

To describe the heat flow in windings of transformers or inductors, a model for the heat flow paths is necessary. This path can be represented by the thermal resistance $R_{\mathrm{w},x}$, which is derived based on the electrothermal analogy. The thermal resistance $R_{\mathrm{w},x}$ is composed of a parallel connection of a tangential resistance R_{tan}, a radial resistance R_{rad} and an axial-radial part $R_{\mathrm{ax,rad}}$ (see Fig. 3.3). First, the relations of the electrothermal analogy are recapitulated and then the calculation of the tangential part and the radial part is presented.

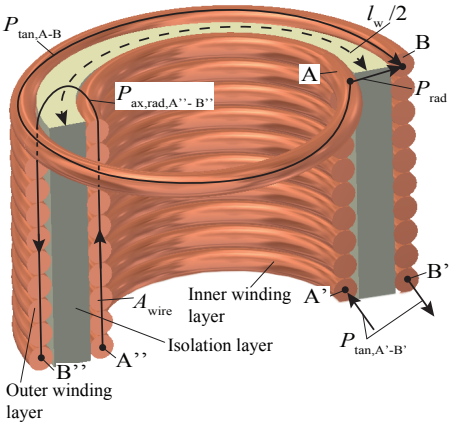

Figure 3.3: Tangential heat flows $P_{\mathrm{tan,A\text{-}B}}$, $P_{\mathrm{tan,A'\text{-}B'}}$, radial heat flow P_{rad} and axial-radial heat flow $P_{\mathrm{ax,rad,A"\text{-}B"}}$ in multi-layer windings [107].

3.1.2.1 Electrothermal analogy

In the literature, the electrothermal analogy is often described with the help of the electrical flow field and the thermal flow field, which leads to the thermal equivalent circuit as, for example, depicted in Fig. 3.2 (a) [127]. In this analogy, the thermal resistance $R_{\mathrm{th,aw}}$ directly corresponds to the electrical resistance $R_{\mathrm{el,aw}}$ along a wire and can be determined by replacing the specific electrical conductivity by the thermal conductivity.

$$R_{\mathrm{el,aw}} = \frac{s}{\gamma A} \iff R_{\mathrm{th,aw}} = \frac{s}{\lambda A} \tag{3.1}$$

The variables s and A are the length and the cross section of the wire, respectively. This analogy is applied to the calculation of the tangential thermal resistance R_{tan}.
Another analogy, which is applied for the determination of the radial thermal resistance R_{rad}, is between the static electrical field and the thermal flow field. Both field problems can be described by elliptical partial differential equations (PDE). In the case of an electrostatic field problem, the PDE [128] is given as

$$-\mathrm{div}(\mathrm{grad}(p)) = \frac{\rho}{\epsilon} \tag{3.2}$$

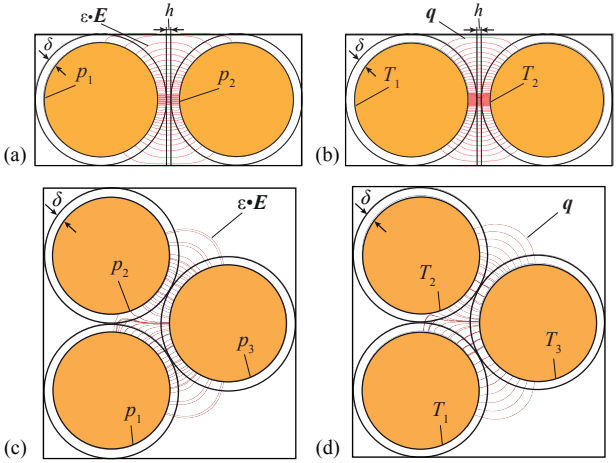

Figure 3.4: Comparison of the FEM simulated electrical and thermal field distributions. (a) Electrical field lines between two orthogonally arranged solid wires wires with potential p_1 and p_2. (b) Thermal heat flux lines between two orthogonally arranged wires. (c) Electrical field lines between three orthocyclicly arranged wires with potentials p_1, p_2 and p_3. (c) Thermal heat flux lines between three orthocyclicly arranged wires.

and the steady-state heat conduction PDE [129] is formulated as

$$-\mathrm{div}(\mathrm{grad}(T)) = \frac{S}{\lambda}. \tag{3.3}$$

These equations are also called the well-known *Poisson's equations* [128], [129]. The material parameters, which are the permittivity ϵ and the thermal conductivity λ, are assumed to be independent regarding the potential p and the temperature T, respectively. Further, ϵ and λ are assumed to be isotropic. Comparing the coefficients in (3.2) and (3.3) results in following electrothermal analogies

$$p \iff T \tag{3.4}$$

$$\epsilon \iff \lambda \tag{3.5}$$

Since, the charge density ρ is directly proportional to the electrical field strength $E \cdot \epsilon$ and the heat source density S is directly proportional to

the heat flux q, the analogy is given as

$$E \cdot \epsilon \iff q \tag{3.6}$$

Hence, the electrical field lines represent the heat flux lines in a thermodynamic problem. The most important relations between these analogies are given in [107, 128, 130, 131] and are summarized in Tab. 3.1.
For the calculation of the radial thermal resistance, two basic winding arrangements are identified, which can be divided into orthogonally (see Fig. 3.4 (a) and (b)) and orthocyclicly arranged wires (see Fig. 3.4 (c) and (d)). In orthogonally arranged wires, the wires of the second layer are lying exactly on top or beside the next layer, whereas in orthocyclic windings the wires of the next layer are lying in the gaps of the previous layer. Figure 3.4 (a) shows the electrical field distribution between two orthogonally arranged wires and Fig. 3.4 (c) shows the electrical field distribution between three orthocyclicly arranged wires, each with an equipotential surface with a potential p_1, p_2 and p_3. The thermal heat flux lines are shown in Fig. 3.4 (b) and Fig. 3.4 (d). There, the conductor surfaces are approximately isothermal surfaces with given temperatures T_1, T_2 and T_3, respectively. Comparing Fig. 3.4 (a) and (b)), as well as Fig. 3.4 (c) and (d)), shows a good match between the electrical field and the thermal flux lines. Hence, the calculation of the radial thermal resistance R_{rad}, between orthogonally or orthocyclicly arranged wires, could be performed by calculating the electrical capacitance between the same arrangements as presented in [132]. For the sake of completeness, the derivation of the radial electrical capacitance in [132] is summarized and evaluated by FEM simulations in appendix A. Based on these results, the transition to the thermal resistance is given in the next section.
The heat flow P in multiple layer windings can be divided into three components [107] (see Fig. 3.3). First, in a tangential component P_{tan} which takes the flow along the winding from layer to layer into account. Second, in a radial component P_{rad} which represents the heat flow between two neighbouring winding layers through the isolation layer. Third, in a combined axial and radial component $P_{\mathrm{ax,rad}}$. There, the heat is conducted, e.g. from point A$''$, in axial direction through each wire of the inner winding. Afterwards, it is convectively transmitted into the outer winding layer and via conduction back to the corresponding wire in point B$''$. Due to the high thermal resistance caused by the convective heat transmission between the winding layers,

Table 3.1: Electrothermal analogy [107, 128, 130, 131]

Electrostatic field		**Electrical flow field**		**Thermal flow field**	
Capacitance (As/V)	C	Conductance (1/Ω)	G	Thermal conductance (W/K)	G_{th}
Voltage (V)	V	Voltage (V)	V	Temperature difference (K)	ΔT
Charge (As)	Q	Current (A)	I	Heat transfer rate, Heat flow (W)	P
$Q = C \cdot V$		$I = G \cdot V$		$P = G_{\mathrm{th}} \cdot \Delta T$	
Potential (V)	p	Potential (V)	p	Temperature (K)	T
Permittivity (As/Vm)	ϵ	Specific conductivity (1/Ωm)	γ	Thermal conductivity (W/Km)	λ
Space charge density (As/m^3)	ρ	Current density (A/m^2)	$\boldsymbol{J}$	Heat source density (W/m^3)	S
Field strength (V/m)	$\boldsymbol{E}$	Field strength (V/m)	$\boldsymbol{E}$	Temperature gradient (K/m)	$\nabla \boldsymbol{T}$
Flux density (As/m^2)	$\boldsymbol{D}$	Current density (A/m^2)	$\boldsymbol{J}$	Heat flux, Heat flow density (W/m^2)	$\boldsymbol{q}$
$\boldsymbol{D} = \epsilon \cdot \boldsymbol{E}$ $\boldsymbol{D} = -\epsilon \cdot \mathrm{grad}(p)$		$\boldsymbol{J} = \gamma \cdot \boldsymbol{E}$ $\boldsymbol{J} = -\gamma \cdot \mathrm{grad}(p)$		$\boldsymbol{q} = -\lambda \cdot \mathrm{grad}(T)$	

the heat flow $P_{\mathrm{ax,rad}}$ is comparably low and is therefore neglected. The derivation of the tangential and radial thermal resistance is given in the following.

3.1.2.2 Tangential thermal resistance

The tangential heat flow $P_{\text{tan,A'-B'}}$ from point A′ in Fig. 3.3 has to be conducted first along all wires of the inner winding layer, in the winding axial direction, and then back down to its consecutive point B′ along all wires of the outer winding layer. Whereas the tangential heat flow $P_{\text{tan,A-B}}$ from the wire in point A has to be conducted only one round along the inner and the outer winding to the corresponding wire in the point B in the next layer. Therefore, the tangential resistor R_{tan} between two wires on two consecutive winding layers is the average of all tangential paths between two consecutive winding layers and is given by

$$R_{\text{tan}} = \frac{1}{N_{\text{pl}}} \sum_{i=1}^{N_{\text{pl}}} \frac{l_{\text{w}} \cdot 2i}{\lambda_{\text{Cu}} A_{\text{wire}}} = \frac{l_{\text{w}}(N_{\text{pl}}+1)}{\lambda_{\text{Cu}} A_{\text{wire}}} \approx \frac{l_{\text{w}} \cdot N_{\text{pl}}}{\lambda_{\text{Cu}} A_{\text{wire}}}. \tag{3.7}$$

There, N_{pl} is the number of turns per layer, l_{w} is the mean length per turn, λ_{Cu} is the thermal conductivity of copper and A_{wire} is the cross sectional area of the wire. In the following sections, the thermal equivalent resistance is derived.

3.1.2.3 Radial thermal resistance

In order to determine the radial thermal resistance, the analogy between the electrostatic field and the thermal flow field from Tab. 3.1 is applied. By simply replacing all permittivities with the equivalent thermal conductivities and inverting (3.63) and (3.64), the radial thermal resistance can be obtained as

$$R_{\text{orth}} = \left[\frac{2\lambda_{\text{air}} l_{\text{w}}}{\alpha} \left(Y + \frac{\lambda_{\text{air}}}{8\lambda_{\text{iso}}} \left(\frac{2\delta}{r_{\text{o}}} \right)^2 \frac{Z}{\alpha} \right) \right]^{-1} \tag{3.8}$$

and

$$R_{\text{cyc}} = \left[4\lambda_{\text{air}} l_{\text{w}} \left(M_{\text{air}} + M_{\text{iso}} \frac{\delta \lambda_{\text{air}}}{\lambda_{\text{iso}} r_{\text{o}}^2} \left(r_{\text{o}} - \frac{\delta}{2} \right) \right) \right]^{-1} \tag{3.9}$$

with

$$\varepsilon_{\mathrm{o}} \iff \lambda_{\mathrm{air}} \tag{3.10}$$

$$\varepsilon_{\mathrm{lay}} \iff \frac{\lambda_{\mathrm{lay}}}{\lambda_{\mathrm{air}}} \tag{3.11}$$

$$\varepsilon_{\mathrm{iso}} \iff \frac{\lambda_{\mathrm{iso}}}{\lambda_{\mathrm{air}}}. \tag{3.12}$$

Where λ_{air} is the thermal conductivity of air, λ_{lay} the thermal conductivity of the isolation layer and λ_{iso} is the thermal conductivity of the wire isolation.
The derivation of the thermal resistance of multi-layer windings will be investigated in the next section.

3.1.2.4 Multi-layer thermal resistance model of round solid wire windings

For an either pure orthogonal or pure orthocyclic multi-layer winding the thermal resistance can be written as

$$R_{\mathrm{w},x} = (R_{\mathrm{tan}} || R_{\mathrm{rad}}) \frac{N_{\mathrm{l}}}{N_{\mathrm{pl}}}. \tag{3.13}$$

Since, R_{tan} and R_{rad} are per-turn resistances, the thermal per-turn parallel connection $(R_{\mathrm{tan}} || R_{\mathrm{rad}})$ in (3.13) must be divided by N_{pl}. N_{l} is the number of layers in series and N_{pl} is the number of turns per layer. In general, every winding is a combination of both thermal radial resistances (orthogonal and orthocyclic). Due to manufacturing reasons, the overall thermal resistance $R_{\mathrm{w},x}$ of a solid wire winding, as shown for example in Fig. 3.5 (a), is usually a combination of orthogonal and orthocyclic layers. At least both halves of the outer layers of the winding, which represents an orthogonal transition to the next medium, can be modeled as one orthogonal layer (see Fig. 3.5 (a) and (b)). This leads to the general form

$$R_{\mathrm{w},x} = (R_{\mathrm{tan}} || R_{\mathrm{cyc}}) \frac{N_{\mathrm{l}} - N_{\mathrm{orth}}}{N_{\mathrm{pl}}} + (R_{\mathrm{tan}} || R_{\mathrm{orth}}) \frac{N_{\mathrm{orth}}}{N_{\mathrm{pl}}} \tag{3.14}$$

where N_{orth} is the number of assumed orthogonal layers. The thermal resistance inside the wire is neglected due to the high thermal conductivity of the copper λ_{Cu} (see Tab. 3.2).

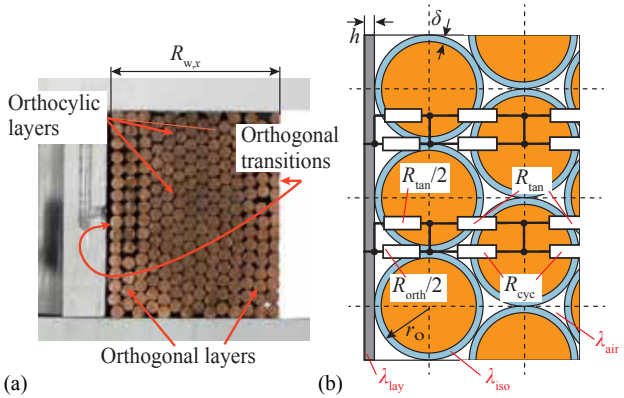

Figure 3.5: (a) Cross section of a solid wire winding with orthogonal and orthocyclic layers. (b) Resistive thermal circuit model of $R_{w,x}$ formed by the tangential and radial thermal components R_{tan}, R_{orth} and R_{cyc}. The thermal resistance inside the wire is neglected due to the high thermal conductivity of the copper.

3.1.2.5 Multi-layer thermal resistance model of litz wire windings

As litz wire is often used to reduce high frequency losses, two thermal models for a single litz wire bundle are presented in the following. First, a straight forward analytical model is determined and second, an extended numerical model, which also considers the twist pitch, is derived. Afterwards, the transition to the multi-layer thermal resistance model is given. Fig. 3.6 (a) shows the cross section of a litz wire winding with three orthocyclic layers and one orthogonal layer. The zoomed view shows a non-circular shaped litz wire bundle. The transition from the physical litz wire winding to its thermal model is shown in Fig. 3.6 (b) and can be devided in 3 steps. Step (A) starts with the transformation of the non-circular litz wire bundle with N_s strands into a square litz bundle with side length $\sqrt{N_s} \cdot 2 \cdot r_{o,litz}$. Due to the loose positions of the strands inside the litz bundle and the unknown force, which is applied to the litz wire bundle during the winding process, the exact litz strand positions inside the bundle are not available and the bundle shape usually differs from a circular shape, as can be seen in Fig. 3.6 (a). Therefore, to overcome this problem, in the new proposed model, the

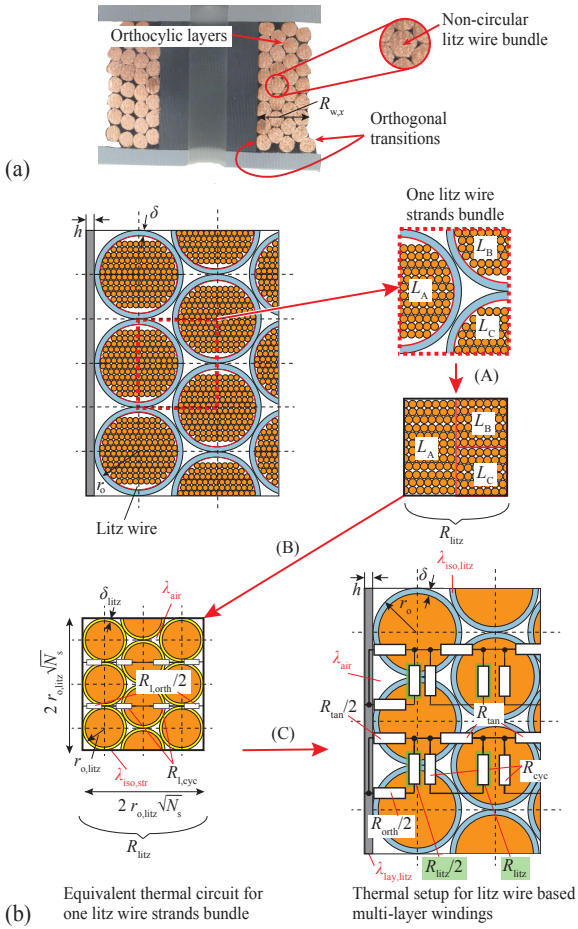

Figure 3.6: (a) Cross sections of a litz wire winding and a non-circular litz wire bundle. (b) Transition from the non-circular litz wire bundle into a square litz bundle (A). There, the litz strands of the doted red square are rearranged to a squared pattern and the outer isolation is removed. (B) Equivalent thermal network of one rearranged litz bundle. (C) Thermal setup of a litz wire based multi-layer winding, which also considers the thermal resistance inside the litz wire bundle.

litz strands are rearranged to an equivalent squared pattern, in order to

uniform the shape inside of each bundle, which reduces the complexity for deriving the equivalent resistance of the bundle. In step (B), the equivalent resistance of a litz bundle R_{litz} is calculated and finally in step (C) the thermal circuit of a multi-layer winding is derived. This model is based on the thermal network in Fig. 3.5 (b), but additionally considers the thermal resistance inside the litz wire bundle R_{litz}.

Analytical thermal resistance litz wire bundle model One way to model the thermal resistance of the litz wire bundle R_{litz} is the series connection of the orthocyclic contributions $R_{\mathrm{l,cyc}}$ between each litz strand and the orthogonal part $R_{\mathrm{l,orth}}$ at the edges (see Fig. 3.6 (b)). Both resistors are determined by using litz strand parameters and (3.9) for $R_{\mathrm{l,cyc}}$ and (3.8) for $R_{\mathrm{l,orth}}$. The thermal resistance of the litz wire is:

$$R_{\mathrm{litz}} = R_{\mathrm{l,cyc}} \left(1 - \frac{1}{\sqrt{N_{\mathrm{s}}}}\right) + \frac{R_{\mathrm{l,orth}}}{\sqrt{N_{\mathrm{s}}}}. \tag{3.15}$$

Extended numerical thermal resistance litz wire bundle model Litz wire consists of bundles and sub-bundles of strands, which are twisted to minimize the high frequency losses. Usually, the exact twisted bundle structure is not available and therefore, a modelling approach, which takes the twist pitch of the litz wire bundels into account, is presented in the following. The extended model of the litz wire bundle is depicted in Fig. 3.7. There, the heat flow is modeled by the already known radial part $P_{\mathrm{l,rad}}$ and, in addition, a part along a single litz strand P_{lay} caused by the lay. The thermal path along the strand can be described by

$$R_{\mathrm{lay}} = \frac{l_{\mathrm{lay}}/2}{\lambda_{\mathrm{Cu}} r_{\mathrm{o,litz}}^2 \pi} \tag{3.16}$$

where l_{lay} is the so called twist pitch, which is the length of lay of the litz wire and results in the network shown in Fig. 3.7 (b). The thermal resistors $R_{\mathrm{l,cyc}}^{'}$ and $R_{\mathrm{l,orth}}^{'}$ are also calculated for $l_{\mathrm{lay}}/2$ with

$$R_{\mathrm{l,cyc}}^{'} = \frac{l_{\mathrm{w}} R_{\mathrm{l,cyc}}}{l_{\mathrm{lay}}/2} \tag{3.17}$$

and

$$R_{\mathrm{l,orth}}^{'} = \frac{l_{\mathrm{w}} R_{\mathrm{l,orth}}}{l_{\mathrm{lay}}/2} \tag{3.18}$$

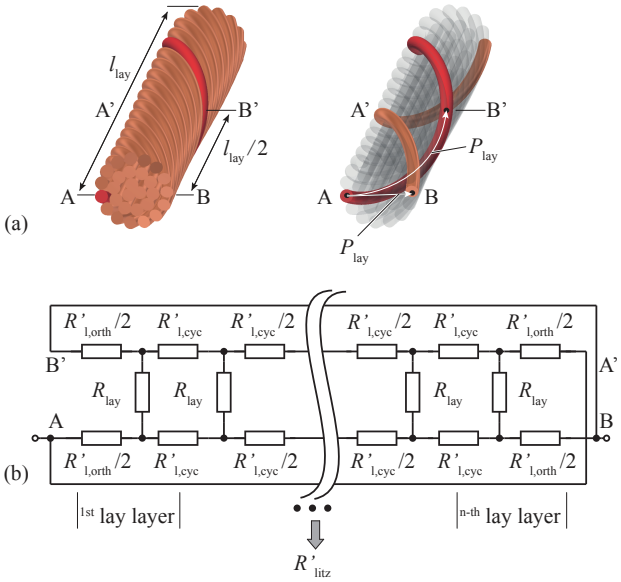

Figure 3.7: Extended model of the litz wire, which takes the twist pitch of the litz wire bundles into account. (a) Litz wire with two considered heat flow paths $P_{\mathrm{l,rad}}$ and P_{lay}. (b) Equivalent thermal network of one horizontal litz strand layer from A to B and A' to B'. One horizontal litz strand layer consists of $n = \lfloor\sqrt{N_{\mathrm{s}}}\rfloor$ lay layers.

where the thermal resistors $R_{\mathrm{l,orth}}$ and $R_{\mathrm{l,cyc}}$ are derived with litz strand parameters and equations (3.8) and (3.9), respectively. Because there is no compact equation for the resistance R'_{litz}, this network is solved numerically. The thermal resistor R'_{litz} represents one horizontal layer of litz wires from point A to B and in parallel from point A' to B'. One horizontal litz strand layer consists of $n = \lfloor\sqrt{N_{\mathrm{s}}}\rfloor$ lay layers. The resulting thermal resistance R_{litz} of a litz wire bundle with length l_{w} is given as

$$R_{\mathrm{litz}} = \frac{R'_{\mathrm{litz}} \cdot l_{\mathrm{lay}}/2}{\sqrt{N_{\mathrm{s}}} l_{\mathrm{w}}}. \tag{3.19}$$

Finally, using (3.15) or (3.19) with litz strand parameters and (3.7), (3.8) as well as (3.9) with litz bundle parameters gives the general form

of the thermal resistance of litz wire windings as

$$R_{\mathrm{w},x} = [R_{\mathrm{tan}}||(R_{\mathrm{cyc}} + R_{\mathrm{litz}})]\,\frac{N_{\mathrm{l}} - N_{\mathrm{orth}}}{N_{\mathrm{pl}}} + \\ + [R_{\mathrm{tan}}||(R_{\mathrm{orth}} + R_{\mathrm{litz}})]\,\frac{N_{\mathrm{orth}}}{N_{\mathrm{pl}}}. \tag{3.20}$$

The derivation of the thermal equivalent circuit model for multi-layer windings will be investigated in the next section.

3.1.3 Thermal T-equivalent circuit model of multi-layer windings

In the following, a simplified thermal T-equivalent model that allows to calculate the hotspot temperature and the hotspot location in multi-layer windings as the one shown in Fig. 3.8 (a) is presented. In this model, each layer-to-layer transition is described with a separate thermal resistor. The losses in each winding are represented by a heat-flux source. In the following, it is shown how the T-equivalent circuit model (tTEC) illustrated in Fig. 3.8 (f) can be used to predict the worst-case temperature based on the thermal resistances previously calculated for solid wire and litz wire.

At first, the contribution of the losses from each layer are superimposed to calculate the temperature T_k at all possible points k between two layers. Afterwards, an analytic expression for the location of the worst-case temperature point is derived by letting the number of winding layers go to infinity while the overall losses stay the same. The so-obtained result is used to derive a closed form-solution with a single lumped heat source, which provides a simplified way of calculating the worst-case temperature for arbitrary choices of R_{a}, R_{b} and R_{w}. It is worth noting, that this approach is mathematically accurate and is *not* equal to simply splitting the overall thermal resistance of the winding stack in half and placing a single lumped heat-source in between.

3.1.3.1 Modeling Assumptions

In the following, it is assumed that the inter-layer thermal resistance is

$$R_{\mathrm{l}} = \frac{R_{\mathrm{w}}}{N-1}. \tag{3.21}$$

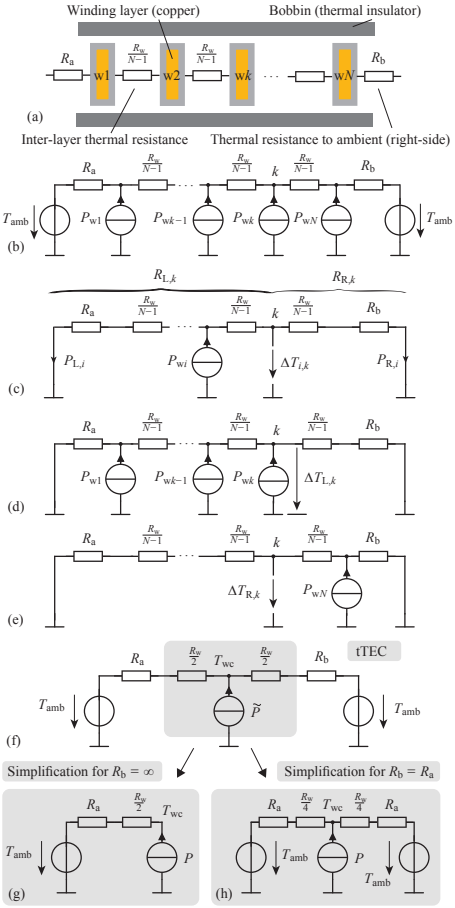

Figure 3.8: (a) Simplified layer stack of the winding, (b) corresponding thermal model with one heat flux source per winding layer, (c) left ($P_{L,i}$) and right ($P_{R,i}$) components of the heat flux generated by the i^{th} source as well as the temperature contribution $\Delta T_{i,k}$ of the i^{th} source at the k^{th} node, (d) temperature contribution $\Delta T_{L,k}$ of all sources to the left of the k^{th} node, including the source at the node, (d) temperature contribution $\Delta T_{R,k}$ of all sources to the right of the k^{th} node and (f) derived thermal T-equivalent circuit (tTEC) model with a lumped heat flux source, (g) special case for $R_b = \infty$, (h) special case for $R_b = R_a$.

In a first approximation, the losses P in the windings are assumed to be homogenous and evenly contribute to the heat flux in each layer:

$$P_{\mathrm{w}1} = \ldots = P_{\mathrm{w}N} = \frac{P}{N} \tag{3.22}$$

The lumped thermal resistors R_{a} and R_{b} denote the effective thermal resistances from the winding surfaces to ambient. These resistors are usually representing convection or radiation and their determinations are given in [133]. It is assumed that heat is only transferred through the faces of the winding[1] and that the temperature distribution is homogenous. The equivalent circuit of such a layer stack is shown in Fig. 3.8 (b).

3.1.3.2 Temperature Contribution of Each Layer

As can be inferred from the equivalent circuit shown in Fig. 3.8 (b), each heat source $P_{\mathrm{w}i}$ generates a heat-flux

$$P_{\mathrm{L},i} = \frac{P}{N} \frac{R_{\mathrm{b}} + (N-i)R_{\mathrm{l}}}{R_{\mathrm{a}} + R_{\mathrm{b}} + R_{\mathrm{w}}} \tag{3.23}$$

to its left and a heat flux

$$P_{\mathrm{R},i} = \frac{P}{N} \frac{R_{\mathrm{a}} + (i-1)R_{\mathrm{l}}}{R_{\mathrm{a}} + R_{\mathrm{b}} + R_{\mathrm{w}}} \tag{3.24}$$

to its right. This situation is illustrated in Fig. 3.8 (c). Consequently, the sources $P_1 \ldots P_{\mathrm{w}k}$ to the the left of node k contribute

$$\Delta T_{i,k}|_{i \leq k} = P_{\mathrm{R},i} \cdot R_{\mathrm{R},k} = P_{\mathrm{R},i} \cdot ((N-k)R_{\mathrm{l}} + R_{\mathrm{b}}) \tag{3.25}$$

to the temperature rise at node k, which is illustrated in Fig. 3.8 (d) while the sources $P_{\mathrm{w}k+1} \ldots P_N$ on the right of node k contribute

$$\Delta T_{i,k}|_{i > k} = P_{\mathrm{L},i} \cdot R_{\mathrm{L},k} = P_{\mathrm{L},i} \cdot ((k-1)R_{\mathrm{l}} + R_{\mathrm{a}}) \tag{3.26}$$

which is illustrated in Fig. 3.8 (d). According to the principle of superposition, the overall temperature at point k is equal to the sum of the individual contributions and the ambient temperature:

$$T_k = T_{\mathrm{amb}} + \underbrace{\sum_{i=1}^{k} \Delta T_{i,k}|_{i \leq k}}_{:=\Delta T_{\mathrm{L},k}} + \underbrace{\sum_{i=k+1}^{N} \Delta T_{i,k}|_{i > k}}_{:=\Delta T_{\mathrm{R},k}} \tag{3.27}$$

[1] The edges are thermally isolated by the bobbin.

The two sums in (3.27) can be rewritten in a closed form:

$$\Delta T_{\mathrm{L},k} = \frac{P}{N}\frac{(N-k)R_\mathrm{w}+R_\mathrm{b}}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}}\left(\frac{kR_\mathrm{a}}{N}+\frac{(k-1)kR_\mathrm{w}}{2}\right) \tag{3.28}$$

$$\Delta T_{\mathrm{R},k} = \frac{P}{N}\frac{(k-1)R_\mathrm{w}+R_\mathrm{a}}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}}\left(\frac{kR_\mathrm{b}}{N}+\frac{(N-k-1)kR_\mathrm{w}}{2}\right) \tag{3.29}$$

3.1.3.3 Location of the Worst-Case Temperature

In order to find the worst-case temperature, the relative location $\widetilde{k} = \frac{k}{N}$ at which the temperature is worst has to be determined. This is done analytically by letting N in (3.28) and (3.29) go to infinity:

$$\lim_{N\to\infty}\Delta T_{\mathrm{R},k} = \frac{\widetilde{k}P}{2}\frac{(2R_\mathrm{a}-\widetilde{k}R_\mathrm{w})(R_\mathrm{a}+(1-\widetilde{k})R_\mathrm{w})}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}} \tag{3.30}$$

$$\lim_{N\to\infty}\Delta T_{\mathrm{L},k} = \frac{(1-\widetilde{k})P}{2}\frac{(2R_\mathrm{a}-\widetilde{k}R_\mathrm{w})(R_\mathrm{a}+(1-\widetilde{k})R_\mathrm{w})}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}} \tag{3.31}$$

The relationship described in (3.22) ensures that the result stays finite. Fig. 3.9 (a) shows that this approximation is sufficiently accurate, even for low numbers of N. Adding (3.30) and (3.31) and maximizing the result with respect to $\widetilde{k}$ leads to the worst-case value for $\widetilde{k}$:

$$\widetilde{k}_\mathrm{wc} = \frac{1}{2}\frac{2R_\mathrm{b}+R_\mathrm{w}}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}} \tag{3.32}$$

3.1.3.4 Closed-Form Solution and tTEC-model

By inserting (3.32) into (3.30) and (3.31) and adding the results, a closed-form solution of the maximum temperature inside the winding is obtained:

$$T_\mathrm{wc} = T_\mathrm{amb} + \frac{\left(R_\mathrm{a}+\frac{R_\mathrm{w}}{2}\right)\left(R_\mathrm{b}+\frac{R_\mathrm{w}}{2}\right)}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}}P\frac{R_\mathrm{a}+R_\mathrm{b}+\frac{R_\mathrm{w}}{2}}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}} \tag{3.33}$$

The result corresponds to the tTEC-model shown in Fig. 3.8 (f), where the individual heat flux sources have been replaced by the lumped heat-flow source

$$\widetilde{P} = P\frac{R_\mathrm{a}+R_\mathrm{b}+\frac{R_\mathrm{w}}{2}}{R_\mathrm{a}+R_\mathrm{b}+R_\mathrm{w}}. \tag{3.34}$$

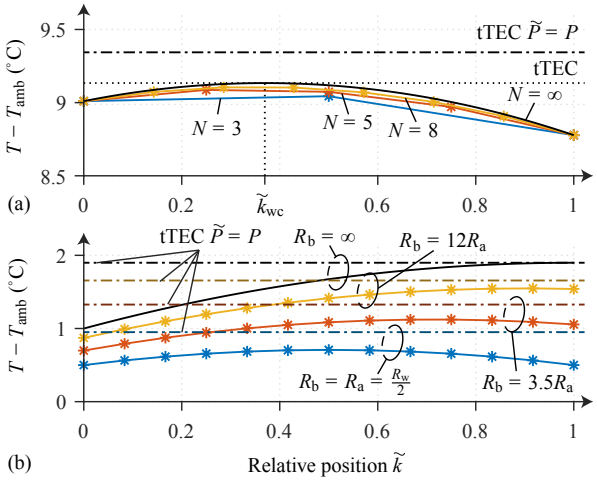

Figure 3.9: (a) Temperature profile for finite number of winding-layers N in relation to the prediction using the tTEC model and the simplified tTEC model where $\widetilde{P} = P$. The hottest point is always closest to $\widetilde{k}$. For the calculations, $R_w = R_{ws}$, $R_a = R_{wp\text{-}amb}$ and $R_b = R_{ws\text{-}amb}$ have been chosen. (b) Accuracy of the tTEC approach when $R_a + R_b \gg R_w$ is not fulfilled. The dashed-an-dotted lines show the respective hotspot temperature as calculated with the $\widetilde{P} = P$ tTEC approach. For the calculations, $R_w = R_{ws}$, $R_a = \frac{R_{ws}}{2}$ and $N = 13$ have been chosen.

Because $\widetilde{P} \leq P$, embedding the tTEC model directly into a larger overall thermal network such as the one shown in Fig. 3.2 (a) leads to lowered heat-fluxes in the overall model and therewith a reduced accuracy of the calculations. To overcome this drawback, the $\widetilde{P} = P$ approximation is proposed which delivers an upper bound for the winding temperature inside the stack without altering the overall heat fluxes in the rest of the network. As shown in Fig. 3.9 (a), the accuracy is high for $R_a + R_b \gg R_w$, which is the case for the transformer discussed in this analysis. The location of the hotspot temperature can be calculated as shown in (3.32).

3.1.3.5 Special Cases

For the case that either R_a or R_b are large, the tTEC model can be simplified to the model shown in Fig. 3.8 (g). In this case, the $\widetilde{P} \approx P$

approximation becomes an equality. Thus, the model can be directly embedded into a superordinate thermal network. The location of the hotspot temperature can again be calculated as shown in (3.32) without modifications. For cases where $R_\mathrm{a} = R_\mathrm{b}$, the tTEC model described by (3.33) can be simplified to the circuit shown in Fig. 3.8 (h):

$$\begin{aligned}\lim_{R_\mathrm{a}\to R_\mathrm{b}} T_\mathrm{wc} &= T_\mathrm{amb} + P\frac{\left(R_\mathrm{a}+\frac{R_\mathrm{w}}{4}\right)\left(R_\mathrm{a}+\frac{R_\mathrm{w}}{4}\right)}{R_\mathrm{a}+R_\mathrm{a}+\frac{R_\mathrm{w}}{2}} \\ &= T_\mathrm{amb} + \frac{P}{2}\left(R_\mathrm{a}+\frac{R_\mathrm{w}}{4}\right).\end{aligned} \tag{3.35}$$

Notice how the lumped resistors adjacent to the heat-source are now $\frac{R_\mathrm{w}}{4}$ instead of $\frac{R_\mathrm{w}}{2}$ in the regular tTEC model. The sensitivity analysis shown in Fig. 3.9 (b) reveals, that without this adjustment, the model would be inaccurate for cases where R_a and R_b are within the same order of magnitude as R_w. For the sake of clarity, the hotspot temperatures calculated with this approach are not explicitly shown in Fig. 3.9 (b), but are in perfect correspondence with peak of the colored curves.

3.1.4 Measurement results

3.1.4.1 Measurement setup

For validating the models depicted in Fig. 3.5 and Fig. 3.6, a test setup as shown in Fig. 3.10 has been developed. Three plastic layers are used for thermal isolation through which a negligible amount of heat is dissipated and the generated heat will be forced to flow in y-direction through the winding. The inner isolation layer is made of Polyethylenterephthalat (PET) because this material withstands continuous temperatures up to 100 °C but unfortunately has a relatively high thermal conductivity. To overcome this problem two additional layers of Polyvenylchlodrid (PVC) are attached on the top and bottom respectively.

Two power resistors were mounted to the inside of a square cross-section aluminium tube, which is also used as the winding bobbin. The tube can be seen as an isothermal interface due to the high thermal conductivity of aluminium (see Tab. 3.2), which leads to an uniform heat distribution on the surface of the tube. To determine the inner and the outer winding temperature two temperature sensors (K-type thermo

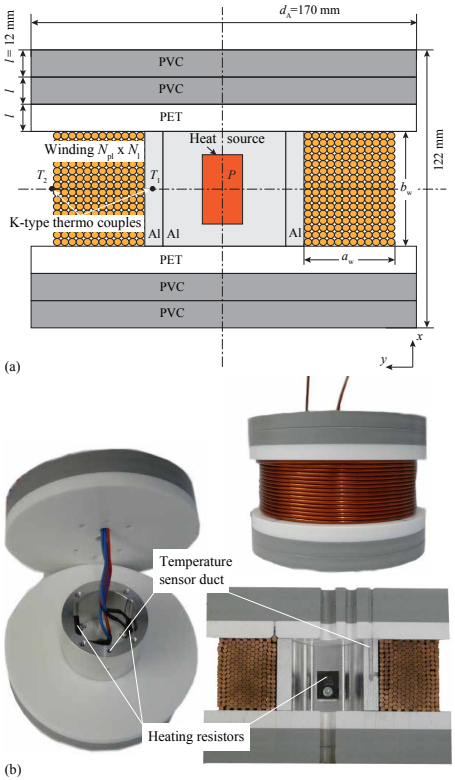

Figure 3.10: (a) Cross section of the thermal test setup cross section. (b) Manufactured thermal test setup, here of single solid wire.

couples) are mounted as shown in Fig. 3.10 (a) and (b). All material properties are listed in Tab. 3.2. The thermal resistance of the test setup in x-direction of the thermal isolation layer is

$$R_{\mathrm{PVC,PET}} = 2(2R_{\mathrm{PVC}} + R_{\mathrm{PET}}) = 18.5\,^{\circ}\mathrm{C/W} \tag{3.36}$$

where

$$R_{\mathrm{PVC}} = \frac{4l}{d_{\mathrm{A}}^2 \pi \lambda_{\mathrm{PVC}}} \quad \text{and} \quad R_{\mathrm{PET}} = \frac{4l}{d_{\mathrm{A}}^2 \pi \lambda_{\mathrm{PET}}}. \tag{3.37}$$

The photo of the test setup is shown in Fig. 3.10 (b), on the left hand side without the winding and with mounted heating resistor and com-

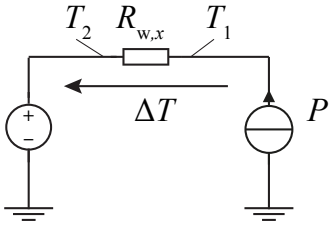

Figure 3.11: Simplified thermal equivalent circuit of the test setup.

pletely assembled on the right side.

3.1.4.2 Winding measurement results

The comparison between the measurements and the analytical model is given in the following for the single solid wire winding exemplarily (see Fig. 3.10 (b)).
In Tab. 3.2, $TS_{\mathrm{S,air}}$ and $TS_{\mathrm{L,air,1\text{-}2}}$ are the test setups (TS) with solid wire (S), or litz wire (L) and an air gap. $TS_{\mathrm{S,epoxy}}$ is the test setup (TS) with solid wire (S) and an epoxy potted winding (epoxy). $TW_{\mathrm{L,1}}$ and $TW_{\mathrm{L,2}}$ are the litz wire (L) transformer winding (TW) parameters of the high-voltage, high-frequency transformer, which is investigated in section 3.1.4.3. Using (3.14) and the winding parameters from the solid wire test setup $TS_{\mathrm{S,air}}$ given in Tab.3.2, results in $R_{\mathrm{w},x} = 1.63\,^{\circ}\mathrm{C/W}$. Concerning that the isolation of the wire is a combination of a PEI and a PAI material, the mean value of both of them will be used for the thermal conductivity λ_{iso}. Due to the fact that the ratio between $R_{\mathrm{PVC,PET}}$ and $R_{\mathrm{w},x}$ is about 11, the heat flow through the isolation layer could be neglected and the thermal setup could be described with the simplified thermal circuit as shown in Fig. 3.11. The measured thermal resistance $R_{\mathrm{w},x,\mathrm{m}}$ can be calculated by

$$R_{\mathrm{w},x,\mathrm{m}} = \frac{\Delta T}{P} = \frac{T_1 - T_2}{P}. \tag{3.38}$$

The comparison between the measured and the calculated thermal resistances of the tested winding setups is given in Tab. 3.3. Generally, the number of orthogonally (N_{orth}) and orthocycly arranged layers is usually not available. Therefore, in practical setups, N_{orth} is chosen to

be 1, because at least both halves of the outer layers can be regarded as one orthogonal transition and all other transitions are assumed as orthocyclic transitions. This results in a too low resistance in the case of solid wire (see Tab. 3.3, $TS_{\mathrm{S,air}}$ and $TS_{\mathrm{S,epoxy}}$). Using the correct number of orthogonal transitions ($N_{\mathrm{orth}} = 6$) results in a relatively small error between the calculated and the measured resistance, as can be seen in Tab. 3.3. In the case of a moulded/potted winding ($TS_{\mathrm{S,epoxy}}$), λ_{air} is replaced by λ_{epoxy}. A polyester foil (Mylar®, $\lambda_{\mathrm{iso,litz,1}}$) is used for the outer isolation of the litz wire windings. Due to the flexible outer shape of the litz wire bundle, the deviation of the thermal resistance in case of litz wire is higher. This can be explained by the fact that the analytical approach is assuming that the heat transition points towards the bobbin and between the litz wires bundles are pure contact points, not as seen in Fig. 3.6 (a) some kind of contact areas. Therefore, the calculated resistance is too high and can be seen as a worst case approximation, if it is used as e.g. in the lumped thermal resistance model in Fig. 3.12. Whereas, if the twist pitch is considered, the error is low. However, the proposed approach achieves a significantly better accuracy compared to the analytical H&S benchmark approach. In the case of solid wire $TS_{\mathrm{S,air}}$, H&S leads to a huge error (+319 %) if the thermal conductivity of the wire insulation material differs strongly from that of the winding impregnation material (compare λ_{air} with the mean value of $\lambda_{\mathrm{iso,1}}$ and $\lambda_{\mathrm{iso,2}}$ in Tab. 3.2). In the case that the thermal conductivities are similar ($TS_{\mathrm{S,epoxy}}$), the error is in the range of the proposed method (+28.3 %). The H&S+ approach achieves a higher accuracy for both solid wire setups (+9.7 % for $TS_{\mathrm{S,air}}$ and +19.6 % for $TS_{\mathrm{S,epoxy}}$) compared to the proposed approach in the case of $N_{\mathrm{orth}} = 1$ (−20.7 % for $TS_{\mathrm{S,air}}$ and −24.8 % for $TS_{\mathrm{S,epoxy}}$). If the exact number of N_{orth} is known, the proposed approach leads to more accurate results (+2.5 % for $TS_{\mathrm{S,air}}$ and +15.2 % for $TS_{\mathrm{S,epoxy}}$) than the H&S+ approach. In the case of litz wire, the H&S, as well as the H&S+ approach, leads in the best case to deviations, which are still larger than 76.1 %. Whereas the proposed analytical method results in +51.4 % for $TS_{\mathrm{L,air,1}}$ and +38.57 % for $TS_{\mathrm{L,air,2}}$ and the proposed numerical method results in −20.7 % for $TS_{\mathrm{L,air,1}}$ and −0.5 % for $TS_{\mathrm{L,air,2}}$.

Table 3.2: Material properties and solid or litz wire winding parameters

Material properties			
Material	Thermal conductivity λ in W/Km		Max. cont. temperature $T_{\max}$ in °C
Air [133]	λ_{air}	0.028	–
Araldite CY221 / HY2966 [134]	λ_{epoxy}	0.2	< 120
Copper (Cu) [133]	λ_{Cu}	401	~ 1000
Aluminium (Al) [133]	λ_{Al}	236	~ 600
Polyvenylchlodrid (PVC) [135]	λ_{PVC}	0.15	60
Polyethylenterephthalat (PET) [135]	λ_{PET}	0.24	100
Polyetherimid (PEI) [135]	$\lambda_{\text{iso,1}}$	0.24	170
Polyamidimid (PAI) [136]	$\lambda_{\text{iso,2}}$	0.26	250
Polyurethan (PU, PUR) [135]	$\lambda_{\text{iso,str}}$	0.245	120
Polyesterfilm (Mylar®) [137]	$\lambda_{\text{iso,litz,1}}$	0.155	< 200
Polyoxymethylen (POM) [138]	λ_{bws}	0.31	100
Polyamid (PA2200) [139]	λ_{bwp}	0.144	< 163
Ferrite [140]	λ_{core}	4	> 120
Natural silk [141]	$\lambda_{\text{iso,litz,2}}$	0.043	< 110

Winding parameters						
Wire type:	**Solid**		**Litz**			
Para. (Unit)	$TS_{\text{S,air}}$	$TS_{\text{S,epoxy}}$	$TS_{\text{L,air,1}}$	$TS_{\text{L,air,2}}$	$TW_{\text{L,1}}$	$TW_{\text{L,2}}$
r_{o}(mm)	1.563	1.563	2.5	0.959	1.035	1.4
δ(µm)	63	63	37.5	52	85	50
l_{w}(mm)	357.4	373.1	377	268.1	313.3	550.3
h(mm)	0	0	0	0	0	0
$N_{\text{l}}(-)$	14	6	10	8	1	2
$N_{\text{pl}}(-)$	16	15	10	22	36	20
$N_{\text{orth}}(-)$	1, 6	1, 6	1	1	1	1
$r_{\text{o,litz}}$(µm)	–	–	54	38.86	38	54
δ_{litz}(µm)	–	–	4	3.36	2.5	18.5
l_{lay}(mm)	–	–	47	53.02	28	63
$N_{\text{s}}(-)$	–	–	1260	420	405	1125
a_{w}(mm)	41.7	17.5	42.5	15.34	–	–
b_{w}(mm)	50	50	50	50	–	–

Table 3.3: Comparison of the proposed approach with winding measurements and benchmark approaches

Measurements:		**Solid wire**				**Litz wire**			
Parameter	Unit	$TS_{\mathrm{S,air}}$		$TS_{\mathrm{S,epoxy}}$		$TS_{\mathrm{L,air,1}}$		$TS_{\mathrm{L,air,2}}$	
ΔT	(°C)	45.6		7.4		52.6		22.1	
P	(W)	22.18		16		21		10.54	
$R_{\mathrm{w},x,\mathrm{m}}$	(°C/W)	2.06		0.46		2.51		2.1	
Analytical proposed:		**Solid wire**				**Litz wire**			
Parameter	Unit	$TS_{\mathrm{S,air}}$		$TS_{\mathrm{S,epoxy}}$		$TS_{\mathrm{L,air,1}}$		$TS_{\mathrm{L,air,2}}$	
$\boldsymbol{N_{\mathrm{orth}}}$	(−)	1	6	1	6	1	1	1	1
$R_{\mathrm{w},x}$	(°C/W)	1.63	2.11	0.35	0.53	3.8	1.99	2.91	2.09
Error	(%)	−20.7	+2.5	−24.8	+15.2	+51.4	−20.7	+38.57	−0.5
Equations	(−)	(3.14)		(3.14)		(3.15), (3.20)	(3.19), (3.20)	(3.15), (3.20)	(3.19), (3.20)
Analytical H&S:		**Solid wire**				**Litz wire**			
Parameter	Unit	$TS_{\mathrm{S,air}}$		$TS_{\mathrm{S,epoxy}}$		$TS_{\mathrm{L,air,1}}$		$TS_{\mathrm{L,air,2}}$	
$R_{\mathrm{w},x}$	(°C/W)	8.63		0.59		4.42		10.45	
Error	(%)	+319		+28.3		+76.1		+397.6	
Equations	(−)	(3.69),(3.70),(3.75)		(3.69), (3.70), (3.75)		(3.69), (3.70), (3.75)		(3.69), (3.70), (3.75)	
Analytical H&S+:		**Solid wire**				**Litz wire**			
Parameter	Unit	$TS_{\mathrm{S,air}}$		$TS_{\mathrm{S,epoxy}}$		$TS_{\mathrm{L,air,1}}$		$TS_{\mathrm{L,air,2}}$	
$R_{\mathrm{w},x}$	(°C/W)	2.26		0.55		12.47		8.01	
Error	(%)	+9.7		+19.6		+396		+281.4	
Equations	(−)	(3.70) − (3.75)		(3.70) − (3.75)		(3.70) − (3.75)		(3.70) − (3.75)	

Consequently, the new approach results in a similar accuracy, in the case of solid wire test setups, but gives a significantly more accurate estimation of the thermal winding resistance in the case of litz wire windings and is therefore, a serious alternative for fast thermal resistance estimations in optimization algorithms. The analysis of the thermal resistance of the H&S and H&S+ approaches are given in [121] and are summarized in appendix B.
The verification of the thermal resistance of the primary (R_{wp}) and the secondary (R_{ws}) litz wire winding of a high-voltage, high-frequency transformer is given in the next section.

3.1.4.3 Measured temperature distribution results of an high-voltage, high-frequency transformer

In the following, the measured temperatures of a high-voltage, high-frequency transformer are investigated and compared to the calculation results based on the thermal network shown in Fig. 3.12. The simplified thermal equivalent circuit is valid for the symmetric half of the transformer. Due to the high operation frequency (100 kHz - 110 kHz), ferrite is used as core material and Litz wire is used for the primary and the secondary winding to reduce the high frequency losses. The detailed design of the transformer is given in [104]. The thermal network consists of the above derived thermal resistors of the primary and the secondary windings (R_{wp} and R_{ws}, parameters see Tab. 3.2, $TW_{\mathrm{L},1}$ and $TW_{\mathrm{L},2}$) and the thermal resistors, which model the conductive and convective heat transfer for the rest of the transformer. The formulas for these types of heat transfer are taken from [133] and are just summarized in the following. The resistance for the conductive heat transfer is [133]

$$R_{\mathrm{cond}} = \frac{l}{\lambda A} \tag{3.39}$$

There, l is the effective length of the heat transfer and A is the effected cross section of the material. The thermal resistance R_{cl} through the center leg and the thermal resistance of the primary and the secondary bobbins (R_{bwp}, R_{bws}) are for example belonging to that type of heat transfer.
The resistance for the convective heat transfer is given in [133] as

$$R_{\mathrm{conv}} = \frac{l}{Nu\lambda A}. \tag{3.40}$$

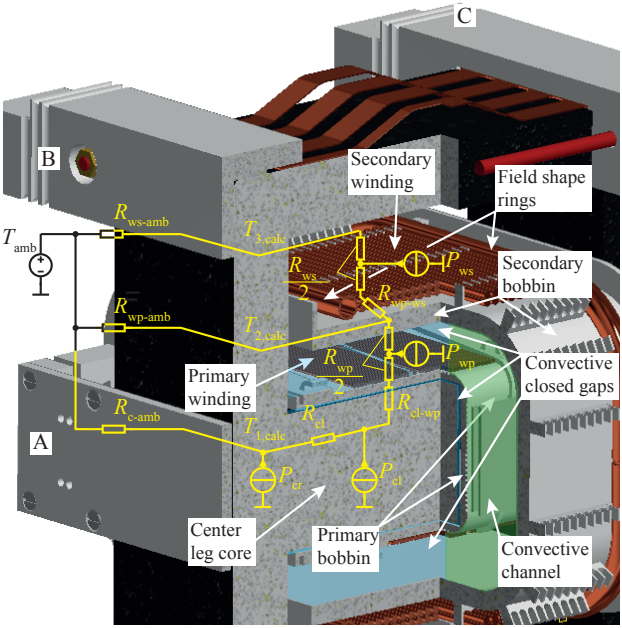

Figure 3.12: Cross section of the considered test transformer, which is rotated by 90 ° compared to Fig. 3.1 (b). The designators A, B, and C are at the same position as in Fig. 3.1 (b). The simplified thermal equivalent circuit is valid for the symmetric half of the transformer (compare Fig. 3.2). The green region represents a convective channel and the blue regions represent convective closed gaps.

with

$$Nu = f(T_\mathrm{s} - T_\mathrm{amb}). \tag{3.41}$$

The Nusselt number Nu is an empirical number, which is a measure of the improvement of the heat transfer compared to the case with static fluid [142]. Since, it is depending on the difference of the surface temperature T_s and the ambient temperature T_amb, thermal networks, which contain convective resistors, have to be solved iteratively until a stable surface temperature is reached. The convective heat resistance of the surface of the core to the ambient($R_\mathrm{c\text{-}amb}$) is a parallel connection of the horizontal surfaces with heat emission on the top and the bottom

Table 3.4: Values of thermal resistors and material parameters

Heat transfer: Conduction			
	R (K/W)	λ (W/Km)(see Tab.3.2)	
R_{cl}	5.64	λ_{core}	
R_{wp}	1	$\lambda_{\mathrm{iso,litz,2}}$, $\lambda_{\mathrm{iso,str}}$, λ_{air}	
R_{ws}	1.8	$\lambda_{\mathrm{iso,litz,2}}$, $\lambda_{\mathrm{iso,str}}$, λ_{air}	
R_{bwp}	2	λ_{bwp}	
R_{bws}	1.18	λ_{bws}	
Heat transfer: Convection			
	R (K/W)	λ (W/Km)	Equ. for Nu [133]
$R_{\mathrm{htop,c}}$	30.26		F2 (7), (8)
$R_{\mathrm{hbot,c}}$	39.82		F2 (10)
$R_{\mathrm{v,c}}$	8.77		F2 (1)
$R_{\mathrm{htop,ws}}$	51.48		F2 (7), (8)
$R_{\mathrm{hbot,ws}}$	67.74		F2 (10)
$R_{\mathrm{v,ws}}$	26.68	λ_{air} [133]	F2 (1)
$R_{\mathrm{hcgap,wp\text{-}bws}}$	65.22		F3 (4), (5)
$R_{\mathrm{hcgap,ws\text{-}bws}}$	12.6		F3 (4), (5)
$R_{\mathrm{vcgap,ws\text{-}bws}}$	29.86		F3 (8)
$R_{\mathrm{hcgap,cl\text{-}bwp}}$	14.08		F3 (4), (5)
$R_{\mathrm{vcgap,cl\text{-}bwp}}$	64.92		F3 (8)
$R_{\mathrm{wp\text{-}amb}}$	24.3		F4 (7), (8)
	R (K/W)	Equation	
$R_{\mathrm{ws\text{-}amb}}$	13.95	(3.43)	
$R_{\mathrm{c\text{-}amb}}$	5.81	(3.42)	
$R_{\mathrm{cl\text{-}wp}}$	13.57	(3.46)	
$R_{\mathrm{wp\text{-}ws}}$	75.26	(3.44)	
Ambient temperature			
T_{amb}		26 °C	

Table 3.5: Operation point of the test transformer

Electrical parameters			
V_{prim}	152 V	f	105.8 kHz
I_{prim}	450 A	f_{rr}	14 Hz
n	20	T_{p}	3.5 ms
High frequency losses			
P_{wp}	1.08 W	P_{ws}	0.92 W
P_{cl}	0.34 W	P_{cr}	0.79 W

plane ($R_{\text{htop,c}}, R_{\text{hbot,c}}$) and the vertical surface ($R_{\text{v,c}}$) of the core.

$$R_{\text{c-amb}} = \left(\frac{1}{R_{\text{htop,c}}} + \frac{1}{R_{\text{hbot,c}}} + \frac{1}{R_{\text{v,c}}} \right)^{-1} \tag{3.42}$$

The convective heat resistance of the secondary winding surface to the ambient ($R_{\text{ws-amb}}$) is a parallel connection of the horizontal surfaces with heat emission on the top and the bottom plane ($R_{\text{htop,ws}}, R_{\text{hbot,ws}}$) and the vertical surface ($R_{\text{v,ws}}$) of the winding.

$$R_{\text{ws-amb}} = \left(\frac{1}{R_{\text{htop,ws}}} + \frac{1}{R_{\text{hbot,ws}}} + \frac{1}{R_{\text{v,ws}}} \right)^{-1} \tag{3.43}$$

The convective heat resistance of the primary winding surface to ambient ($R_{\text{wp-amb}}$) is approximated as a convective channel [133] (the green region in Fig. 3.12), which is formed by the part of the primary surface outside the core window and the secondary bobbin. The thermal resistance between primary and secondary winding ($R_{\text{wp-ws}}$) is formed by the series connection of the secondary bobbin resistor (R_{bws}), the convective heat resistance of the primary winding surface to the secondary bobbin inside the core window (blue regions in Fig. 3.12) ($R_{\text{hcgap,wp-bws}}$) and the convective heat resistance related to the air layer between secondary bobbin and secondary winding ($R_{\text{ws-bws}}$).

$$R_{\text{wp-ws}} = R_{\text{bws}} + R_{\text{hcgap,wp-bws}} + R_{\text{ws-bws}} \tag{3.44}$$

The resistor $R_{\text{hcgap,wp-bws}}$ represents a convective horizontal closed gap

and the resistor $R_{\text{ws-bws}}$ is formed by the parallel connection of the thermal resistors $R_{\text{hcgap,ws-bws}}$ and $R_{\text{vcgap,ws-bws}}$, which represent the convective horizontal and vertical closed gaps between the secondary winding and the secondary bobbin [133].

$$R_{\text{ws-bws}} = \left(\frac{1}{R_{\text{hcgap,ws-bws}}} + \frac{1}{R_{\text{vcgap,ws-bws}}} \right)^{-1} \tag{3.45}$$

The heat transfer between the center leg core and primary winding ($R_{\text{cl-wp}}$) is formed by the series connection of the thermal resistors of the primary bobbin (R_{bwp}) and the air layer between the center core and the primary winding bobbin ($R_{\text{cl-bwp}}$).

$$R_{\text{cl-wp}} = R_{\text{bwp}} + R_{\text{cl-bwp}} \tag{3.46}$$

with

$$R_{\text{cl-bwp}} = \left(\frac{1}{R_{\text{hcgap,cl-bwp}}} + \frac{1}{R_{\text{vcgap,cl-bwp}}} \right)^{-1} . \tag{3.47}$$

The numerical values of the thermal resistors, which are used in the simulations, are given in Tab. 3.4. Additionally, the thermal conductivities for calculating the conductive heat resistances and the equations for the Nusselt numbers, in the case of convective heat transfer, are listed in Tab. 3.4. Table 3.5 shows the operation point for the heat run test in air and the calculated losses in the center leg of the core P_{cl}, the rest of the core P_{cr} and the windings $P_{\text{wp}}, P_{\text{ws}}$. All resistance and loss values are given for the symmetric half of the transformer. The main frequency of the input voltage is $f = 105.8\,\text{kHz}$ and the transformer is operated in pulse mode ($T_{\text{p}} = 3.5\,\text{ms}$) with a pulse repetition rate of $f_{\text{rr}} = 14\,\text{Hz}$ [68]. The high frequency losses are calculated as presented in [104].

Figure 3.13 shows a section of the transformer from Fig. 3.1 (b) during the heat run test. The thermal distribution in Fig. 3.13 (b) clearly shows the hot spots after 7.3 h operation around the primary winding. The white rectangles and the circle define the area of averaging for the temperature measurements (T_1, T_2, T_3), which are depicted in Fig. 3.14. Best fit curves ($T_{1,\text{bf}}$, $T_{2,\text{bf}}$, $T_{3,\text{bf}}$) are generated out of the measurement data and are used for extrapolation to estimate when a stable steady-state temperature is reached. The error is between +1.3 % and +12.5 %, comparing the extrapolated temperature values at a time after 20 h ($T_{1,\text{bf}}(20\,\text{h})$, $T_{2,\text{bf}}(20\,\text{h})$, $T_{3,\text{bf}}(20\,\text{h})$) with the calculated values ($T_{1,\text{calc}}$, $T_{2,\text{calc}}$, $T_{3,\text{calc}}$) in Tab.3.6.

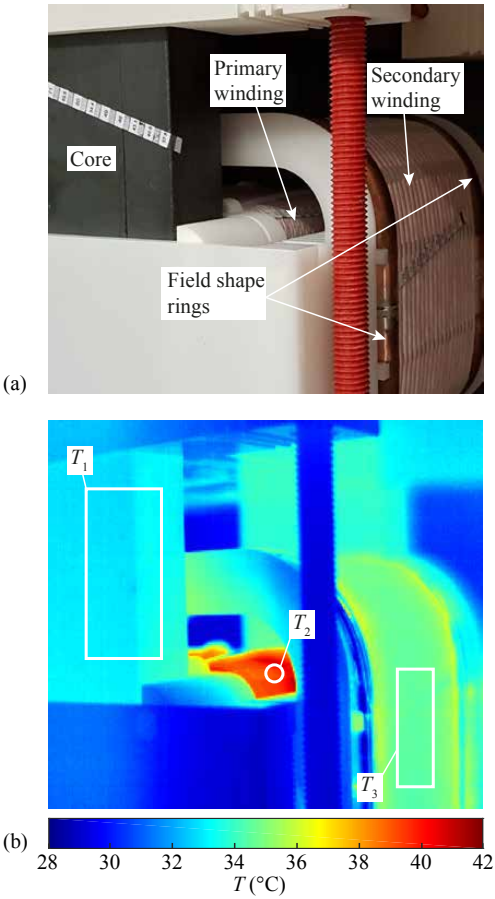

Figure 3.13: (a) Section of the transformer under test. The entire transformer is depicted in Fig. 3.1 (b). (b) Temperature distribution of the transformer after a heat run test of 7.3 h. All transparent oil gap barriers are removed during the measurements with the thermal camera. The white rectangles and the circle defines the area of averaging for the temperature measurements.

3.1.5 Conclusion

In this paper, the derivation of the thermal resistance of multi-layer windings with solid or litz wires has been presented and validated by

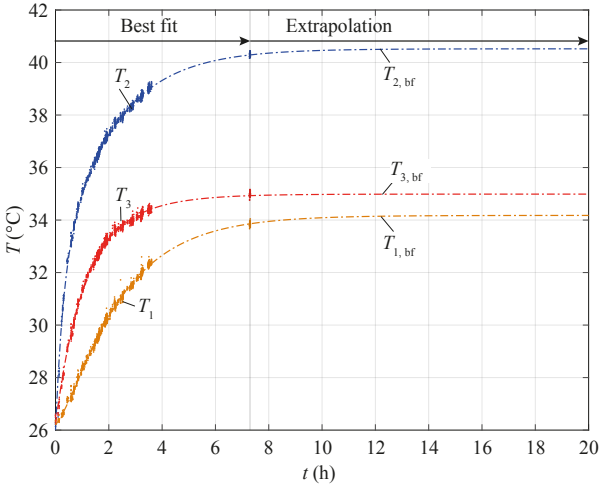

Figure 3.14: Averaged measured temperature sequences (T_1, T_2, T_3) recorded over 7.3 h and their according best fit curves ($T_{1,\mathrm{bf}}$, $T_{2,\mathrm{bf}}$, $T_{3,\mathrm{bf}}$), which are used for extrapolation until a stable steady-state temperature is reached. The measured signals are related to the measurement positions in Fig. 3.13 (b).

Table 3.6: Comparison between the measured and the calculated temperatures of the prototype transformer

Measured temperature		**Calculated temperature**		**Error**
$T_{1,\mathrm{bf}}(20\,\mathrm{h})$	34.18 °C	$T_{1,\mathrm{calc}}$	34.61 °C	+1.3 %
$T_{2,\mathrm{bf}}(20\,\mathrm{h})$	40.52 °C	$T_{2,\mathrm{calc}}$	42.97 °C	+6 %
$T_{3,\mathrm{bf}}(20\,\mathrm{h})$	35 °C	$T_{3,\mathrm{calc}}$	39.38 °C	+12.5 %

experimental measurements. In addition, the proposed approach has been benchmarked by two analytical approaches from literature regarding accuracy. This analytical approach can be used in straight forward designs of magnetic devices, or could be integrated in optimization procedures. With the determined approach also moulded windings can be considered. The relative error between the analytical solutions and measurements, in the case of non-casted solid wire, is in the range of

$-20.7\,\%$ to $+2.5\,\%$ and $-24.8\,\%$ to $+15.2\,\%$ for epoxy casted test setups. These results are similar, compared to the results of the benchmark approaches. In the case of litz wire, the derived formulas show a matching between the calculated and the measured values in the range of $+51.4\,\%$ to $-20.7\,\%$, which is remarkable better than the results of the benchmark approaches, where the deviation is in the range of $+76.1\,\%$ to $+397.6\,\%$. In addition, a thermal T-equivalent circuit (tTEC) model for multi-layer windings has been derived. An analytical temperature distribution prediction of a high frequency high voltage test transformer, based on the new thermal winding model, has been compared to measured temperature values and shows a highly accordance with the measured temperature distribution. The error between the calculated and the measured temperatures is between $+1.3\,\%$ and $+12.5\,\%$.

3.1.6 Appendix A

In the following, the analysis of the basic capacitance cells of multi-layer windings is summarized based on [132] and compared to FEM simulations.

The presented approach of the derivation of the radial thermal resistance is a 1D-approach, which assumes that the temperature in a single layer is equally distributed and the heat flow is directed only in one direction. For that reason, the electrical potential in a single layer is the same for each turn and the electrical capacitances between non-adjacent turns in the same layer are considered to be zero. The capacitances to turns in non-adjacent layers are also neglected because of the comparable high distance between the turns. Figure 3.15 shows the electrical field distribution of a four layer winding. The height of the layers $l_\mathrm{L} = 53\,\mathrm{mm}$, the radius r_o is given in Tab. 3.2, test setup $TS_{S,air}$ and the gap $h = 0.1\,\mathrm{mm}$. The minor influence is clearly shown, because the electrical field in the regions between non-adjacent layers is lower than $10\,\%$, compared to the field between two adjacent layers. Based on this assumptions, electrical multi-layer windings can be described with the help of independent basic orthogonal cells (see Fig. 3.16 (b)) and/or orthocyclic cells (see Fig. 3.17 (b)).

3.1.6.1 Orthogonal winding capacitance model

To derive the capacitance model for an orthogonal winding, two wires are considered, which are arranged next to each other, separated by an

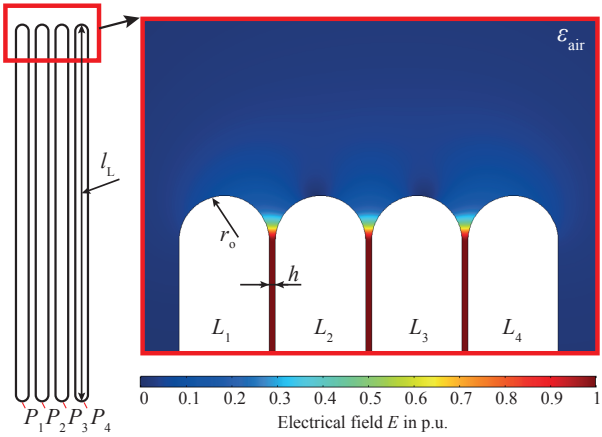

Figure 3.15: FEM simulation of the electrical field E distribution of a four layer winding for showing the minor influence of the capacitance between turns in non-adjacent layers. The winding arrangement is located in an infinite air box, whereas layer L_1 is set to potential $P_1 = 0\,\mathrm{V}$, layer L_2 is set to potential $P_2 = 1\,\mathrm{V}$, layer L_3 is set to potential $P_3 = 2\,\mathrm{V}$ and layer L_4 is set to potential $P_4 = 3\,\mathrm{V}$.

isolation layer (see Fig. 3.16 (a)). In a first step, the electrical field inside the rectangular basic cell (see Fig. 3.16 (a)) is calculated and then the energy inside the basic cell is derived by integration. By equating this energy with the energy stored in the equivalent capacitor, the value for the capacitance could be derived.
In Fig. 3.16 (a), the electrical field lines cross the boundary between cooper surface and the wire insulation perpendicularly. Further, the transition of the field lines at the boundary between wire insulation surface and the air is also perpendicular and afterwards, they are directed towards the other electrode. There, they hit the surface of the isolation layer h nearly perpendicularly and the symmetry line exactly perpendicularly. For determining the electrical field in the basic cell in Fig. 3.16 (a), following assumptions are made:

1. The thickness of the wire insulation is usually small, so the deviation inside the wire insulation towards the other electrode can be neglected and the field lines are assumed to run in radial direction with respect to the wire center.

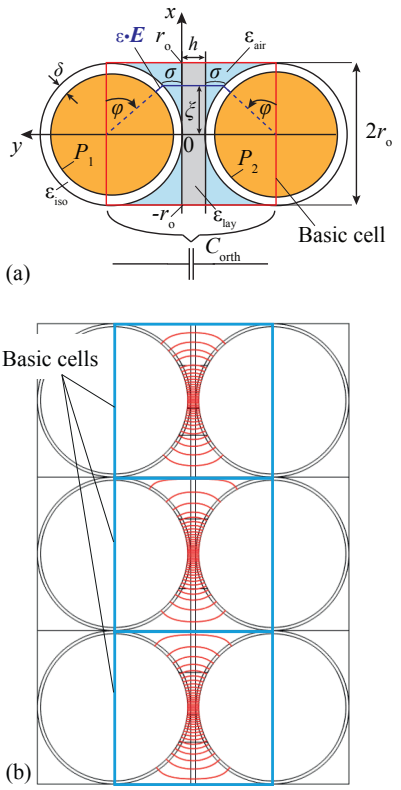

Figure 3.16: (a) Orthogonal basic cell (solid rectangle), which is formed by two orthogonally arranged solid wires with assumed simplified electrical field lines. (b) Electrical field lines between two layers of an orthogonally arranged winding simulated with FEM and the corresponding independent basic cells.

2. After their perpendicular transition from the wire insulation into air, the field lines are immediately bended towards the other electrode and hit the isolation layer exactly perpendicularly.

Hence, all electrical field components are normal components. Comparing Fig. 3.16 (a) and (b), the deviations of the field lines have their maximum at $\varphi = 0$ and a minimum at $\varphi = \pi/2$. Due to the fact that most of the field lines will run proximally to $\varphi = \pi/2$, the resulting error is low. The derivation of the electrical field is given in the following.

According to the boundary conditions between wire insulation and air follows

$$\varepsilon_{\mathrm{iso}} E_{\mathrm{iso}} = \varepsilon_{\mathrm{air}} E_{\mathrm{air}} \sin\varphi \tag{3.48}$$

where $\varepsilon_{\mathrm{iso}}$ is the relative permittivity of the wire insulation and $\varepsilon_{\mathrm{air}}$ is the relative permittivity of air, which is considered with a value of 1. E_{iso} is the electrical field strength of the wire insulation and E_{air} is the field strength in air. The perpendicular ingress of the field lines from air into the isolation layer leads to

$$\varepsilon_{\mathrm{lay}} E_{\mathrm{lay}} = \varepsilon_{\mathrm{air}} E_{\mathrm{air}} \tag{3.49}$$

where $\varepsilon_{\mathrm{lay}}$ is the relative permittivity and E_{lay} is the electrical field strength of the isolation layer. Performing the line integral of the voltage between the two conductors gives

$$V = 2E_{\mathrm{iso}}\delta + E_{\mathrm{lay}} h + 2E_{\mathrm{air}}\sigma. \tag{3.50}$$

Using (3.48), (3.49), (3.50) and

$$\sin\varphi = \frac{\sqrt{r_{\mathrm{o}}^2 - \xi^2}}{r_{\mathrm{o}}} \quad \text{as with at} \quad \sigma = r_{\mathrm{o}} - \sqrt{r_{\mathrm{o}}^2 - \xi^2} \tag{3.51}$$

and by substituting

$$\alpha = 1 - \frac{\delta}{\varepsilon_{\mathrm{iso}} r_{\mathrm{o}}} \quad \text{and} \quad \beta = \frac{1}{\alpha}\left(1 + \frac{h}{2\varepsilon_{\mathrm{lay}} r_{\mathrm{o}}}\right) \tag{3.52}$$

all field strengths can be calculated by

$$E_{\mathrm{lay}} = \frac{V}{2\varepsilon_{\mathrm{lay}}\alpha\left(\beta r_{\mathrm{o}} - \sqrt{r_{\mathrm{o}}^2 - \xi^2}\right)} \tag{3.53}$$

$$E_{\mathrm{iso}} = \frac{V\sqrt{r_{\mathrm{o}}^2 - \xi^2}}{2\varepsilon_{\mathrm{iso}} r_{\mathrm{o}}\alpha\left(\beta r_{\mathrm{o}} - \sqrt{r_{\mathrm{o}}^2 - \xi^2}\right)} \tag{3.54}$$

$$E_{\mathrm{air}} = \frac{V}{2\alpha\left(\beta r_{\mathrm{o}} - \sqrt{r_{\mathrm{o}}^2 - \xi^2}\right)}. \tag{3.55}$$

With the electrical field, the electrical energy stored in the isolation layer is

$$W_{\mathrm{lay}} = \frac{\varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{lay}}}{2} l_{\mathrm{w}} h \int_{-r_{\mathrm{o}}}^{+r_{\mathrm{o}}} E_{\mathrm{lay}}(\xi)^2 \mathrm{d}\xi. \tag{3.56}$$

The energy in the wire insulation in polar coordinates with the origin in the center of the left wire is

$$W_{\mathrm{iso}} = \varepsilon_{\mathrm{o}}\varepsilon_{\mathrm{lay}} l_{\mathrm{w}} \int_0^{\pi} \int_{r_{\mathrm{o}}-\frac{\delta}{2}}^{+r_{\mathrm{o}}} E_{\mathrm{iso}}(\varphi)^2 r \mathrm{d}r\mathrm{d}\varphi \tag{3.57}$$

and the energy in the air is

$$W_{\mathrm{air}} = \varepsilon_{\mathrm{o}} l_{\mathrm{w}} \int_{-r_{\mathrm{o}}}^{+r_{\mathrm{o}}} \int_0^{\sigma(x)} E_{\mathrm{air}}(x,y)^2 \mathrm{d}y\mathrm{d}x. \tag{3.58}$$

Consequently, the total electrical energy in a basic cell is then

$$W_{\mathrm{all}} = W_{\mathrm{lay}} + W_{\mathrm{iso}} + W_{\mathrm{air}}. \tag{3.59}$$

After solving the integrals and several steps of simplification, the following expression results

$$W_{\mathrm{all}} = \frac{\varepsilon_{\mathrm{o}} l_{\mathrm{w}} V^2}{\alpha} \left\{ Y + \frac{1}{8\varepsilon_{\mathrm{iso}}} \left(\frac{2\delta}{r_{\mathrm{o}}}\right)^2 \frac{Z}{\alpha} \right\} \tag{3.60}$$

with

$$Y = \arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right) \frac{\beta}{\sqrt{\beta^2-1}} - \frac{\pi}{4} \tag{3.61}$$

and

$$Z = \frac{\beta\left(\beta^2-2\right)}{\left(\beta^2-1\right)^{3/2}} \arctan\left(\sqrt{\frac{\beta+1}{\beta-1}}\right) - \frac{\beta}{2\,\beta^2-2} - \frac{\pi}{4}. \tag{3.62}$$

The capacitance can be found by comparison of the coefficients (3.60) with $W = C_{\mathrm{orth}} V^2/2$ which results in

$$C_{\mathrm{orth}} = \frac{2\varepsilon_{\mathrm{o}} l_{\mathrm{w}}}{\alpha} \left\{ Y + \frac{1}{8\varepsilon_{\mathrm{iso}}} \left(\frac{2\delta}{r_{\mathrm{o}}}\right)^2 \frac{Z}{\alpha} \right\}. \tag{3.63}$$

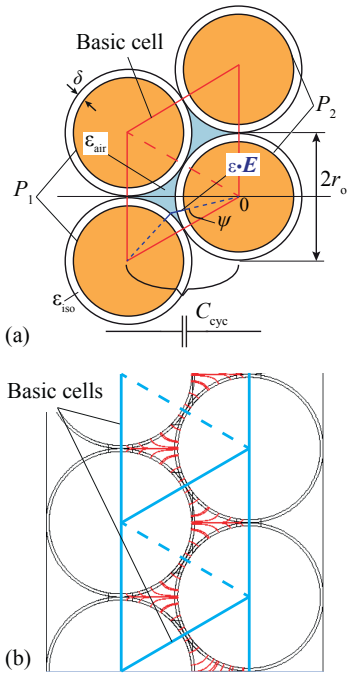

Figure 3.17: (a) Three orthocyclicly arranged wires with assumed simplified electrical field lines and basic cell (solid rhombus). (b) Electrical field lines between two layers of an orthocyclicly arranged winding simulated with FEM and the corresponding independent basic cells.

Orthocyclic winding capacitance model In case of orthocyclic layers, the basic capacitance describes the energy which is stored between the two neighbouring wires in the left layer and two wires in the right layer as shown in the dashed rhombus basic cell in Fig. 3.17 (a). Again, the paths of the electrical flux lines depicted in Fig. 3.17 (a) and (b) match very well. Taking the same assumptions into account for the electrical field lines like in the orthogonal case leads to [132]:

$$C_{\mathrm{cyc}} = 4\varepsilon_{\mathrm{o}} l_{\mathrm{w}} \left[M_{\mathrm{air}} + M_{\mathrm{iso}} \left(\frac{\delta}{\varepsilon_{\mathrm{iso}} r_{\mathrm{o}}^2} \right) \left(r_{\mathrm{o}} - \frac{\delta}{2} \right) \right] \tag{3.64}$$

Table 3.7: Single basic cell capacitance evaluation

Material parameter		
ϵ_o	$8.854\,187\,817 \times 10^{-12}$ (As/Vm)	
$\epsilon_{air}(-)$	ϵ_{iso} (PAI,[136])	ϵ_{lay} (PET,[135])
1	4.2(−)	3.4(−)
Capacitance		
Basic cell	**Orthogonal**	**Orthocyclic**
	C_{orth} (pF/m)	C_{cyc} (pF/m)
Analytical	121.04	322.65
FEM	123.25	331.58
Error	-1.8 %	-2.7 %

with

$$M_{air} = \int_0^{\frac{\pi}{6}} \frac{\cos^2\psi - \cos\psi\sqrt{\cos^2\psi - 0.75} - 0.5}{\left[\cos\psi - \alpha(\sqrt{\cos^2\psi - 0.75} + 0.5)\right]^2} \mathrm{d}\psi \tag{3.65}$$

and

$$M_{iso} = \int_0^{\frac{\pi}{6}} \frac{\sin^2\psi + \cos\psi\sqrt{\cos^2\psi - 0.75}}{\left[\cos\psi - \alpha(\sqrt{\cos^2\psi - 0.75} + 0.5)\right]^2} \mathrm{d}\psi. \tag{3.66}$$

In order to evaluate the accuracy of the analytically derived basic cell equations, a comparison with FEM simulations is carried out. The two setup models are surrounded by air and the used FEM software is COMSOL. The simulation model setup of the orthogonal basic cell is shown in Fig. 3.16 (a), whereas the left conductor is set to the potential $P_1 = 0\,\mathrm{V}$ and the right conductor is set to potential $P_2 = 1\,\mathrm{V}$. The simulation model setup of the orthocyclic basic cell is shown in Fig. 3.17 (a), whereas both conductors on the left side are set to potential $P_1 = 0\,\mathrm{V}$ and both conductors on the right hand side are set to potential $P_2 = 1\,\mathrm{V}$. After the calculation of the electrical field E with the FEM solver, the electrical energy density W inside the areas A of the basic cells is derived by

$$W = \int E^2 \mathrm{d}A \tag{3.67}$$

and finally, the capacitance per length is given as

$$C_{\mathrm{orth,cyc}} = \frac{2W}{(P_2 - P_1)^2} \tag{3.68}$$

The comparison between the analytical results and the FEM simulations of the orthogonal and the orthocyclic basic cell capacitances per length are given along with the used permittivities of the insulation materials in Tab. 3.7. For the evaluation, the geometric values δ and r_o are taken from the winding test setup $TS_{\mathrm{S,air}}$ given in Tab. 3.2. The width of the isolation layer h, in case of the orthogonal basic cell, is chosen as $h = 0.1\,\mathrm{mm}$. The error in both cases is sufficiently low, $-1.8\,\%$ for the orthogonal basic cell and $-2.7\,\%$ for the orthocyclic basic cell.

3.1.7 Appendix B

A summary of the Hashin and Shtrikman (H&S) approach [120] for the calculation of the effective thermal conductivity k_e of two components winding amalgams and the extended Hashin and Shtrikman approach [121] (H&S+), which considers three component winding amalgams, is given in the following. Both approaches are valid for round conductor shapes [122] and the same notation as in [121] is used. The variables v and k are the notations of the volume ratios and the thermal conductivities.

3.1.7.1 Effective thermal conductivity based on the Hashin and Shtrikman approach (H&S)

The effective thermal conductivity k_e of round solid wire windings is given as

$$k_\mathrm{e} = k_p \frac{(1+v_c)k_c + (1-v_c)k_p}{(1-v_c)k_c + (1+v_c)k_p} \tag{3.69}$$

where the subscript expressions c and p represent the conductor and the insulation/impregnation material between the conductors. The conductor volume ratio is calculated by

$$v_c = \frac{(r_\mathrm{o} - \delta)^2 \pi l_\mathrm{w} N_\mathrm{l} \cdot N_\mathrm{pl}}{a_\mathrm{w} b_\mathrm{w} l_\mathrm{w}} \tag{3.70}$$

where a_w is the width and b_w is the height of the winding, as can be seen in Fig. 3.10 (a).

The same equations can be used for litz wire windings, where the insulation around the strands is neglected and the whole bundle is considered as solid copper conductor with outer insulation.

3.1.7.2 Effective thermal conductivity based on the extended Hashin and Shtrikman approach (H&S+)

The effective thermal conductivity k_e of round solid wire windings is given as

$$k_e = k_p \frac{(1+v_c)k_c + (1-v_c)k_p}{(1-v_c)k_c + (1+v_c)k_p} \quad \text{with} \quad k_p = k_a \tag{3.71}$$

$$k_a = k_{ii}\frac{v_{ii}}{v_{ii}+v_{ci}} + k_{ci}\frac{v_{ci}}{v_{ii}+v_{ci}} \tag{3.72}$$

The subscript expressions c, ci, ii represent the conductor, the conductor insulation and the insulation/impregnation material between the conductors. The conductor volume ratio v_c is calculated by (3.70) and the conductor insulation volume ratio by

$$v_{ci} = \frac{(2r_\mathrm{o}\delta - \delta^2)\pi l_\mathrm{w} N_\mathrm{l} \cdot N_\mathrm{pl}}{a_\mathrm{w} b_\mathrm{w} l_\mathrm{w}} \tag{3.73}$$

Finally, the insulation/impregnation material between the conductors volume ratio v_{ii} is given as

$$v_{ii} = 1 - (v_c + v_{ci}) \tag{3.74}$$

In the case of round litz wire windings, the effective thermal conductivity k_e is calculated in two steps. First, (3.70) - (3.74) are applied with strand parameters, resulting in k_e^*. The parameters, r_o, δ are replaced by $r_\mathrm{o,litz}$, δ_litz, and $N_\mathrm{l} \cdot N_\mathrm{pl}$ and $a_\mathrm{w} b_\mathrm{w}$ are substituted by N_s and $(r_\mathrm{o} - \delta)^2\pi$, respectively. In a second step, (3.70) - (3.74) are used with litz bundle parameters, where in (3.70), k_c is replaced by k_e^*.
Finally, the thermal resistance, which is used for the bench mark test in section 3.1.4.2 is defined as

$$R_{w,x} = \frac{a_\mathrm{w}}{b_\mathrm{w} l_\mathrm{w} k_e} \tag{3.75}$$

All wire and material parameters, as well as all volume ratios are listed in Tab. 3.2 and Tab. 3.8, respectively.

Acknowledgment

The authors would like to thank the project partners CTI and AMPEGON AG very much for their strong support of the CTI-research project 13135.1 PFFLR-IW.

Table 3.8: Volume ratios (-) and thermal conductivities (W/Km) used for the bench mark evaluations

Solid wire											
	Analytic H&S				**Analytic H&S+**						
Parameter	v_c	k_p	k_c	$\boldsymbol{k_e}$	v_c	v_{ci}	v_{ii}	k_{ii}	k_{ci}	k_c	$\boldsymbol{k_e}$
$TS_{\mathrm{S,air}}$	0.812	λ_{air}	λ_{Cu}	0.27	0.812	0.067	0.121	λ_{air}	$(\lambda_{\mathrm{iso},1}+\lambda_{\mathrm{iso},2})/2$	λ_{Cu}	1.03
$TS_{\mathrm{S,epoxy}}$	0.776	λ_{epoxy}	λ_{Cu}	1.58	0.776	0.064	0.16	λ_{epoxy}	$(\lambda_{\mathrm{iso},1}+\lambda_{\mathrm{iso},2})/2$	λ_{Cu}	1.69

Litz wire																			
					Analytic H&S+														
	Analytic H&S				**Step 1**							**Step 2**							
Parameter	v_c	k_p	k_c	$\boldsymbol{k_e}$	v_c	v_{ci}	v_{ii}	k_{ii}	k_{ci}	k_c	k_e^*	v_{c2}	v_{ci2}	v_{ii2}	k_{ii2}	k_{ci2}	k_{c2}	$\boldsymbol{k_e}$
$TS_{\mathrm{L,air},1}$	0.896	λ_{air}	λ_{Cu}	0.51	0.519	0.086	0.395	λ_{air}	$\lambda_{\mathrm{iso,str}}$	λ_{Cu}	0.211	0.896	0.028	0.076	λ_{air}	$\lambda_{\mathrm{iso,litz},1}$	k_e^*	0.181
$TS_{\mathrm{L,air},2}$	0.593	λ_{air}	λ_{Cu}	0.11	0.643	0.128	0.229	λ_{air}	$\lambda_{\mathrm{iso,str}}$	λ_{Cu}	0.486	0.593	0.07	0.337	λ_{air}	$\lambda_{\mathrm{iso,litz},1}$	k_e^*	0.143

4

Control design of the modulator system

In this chapter, the control system for the modulator system is presented. Two control strategies for balancing the input, as well as the output voltage between the SPRC-Bms are derived and verified by measurements and simulations. Additionally, a method for compensating the output voltage droop, which occurs due to the huge power consumption during the pulse, is obtained. For balancing the output voltage, only a single control variable from the high voltage side is needed, namely the full output voltage. The rest of the control variables are obtained from the primary side of the transformer, which leads to a highly reduction of measurement effort, respectively costs.

4.1 Journal III.: Analytical Modelling and Controller Design of a Modular Series Parallel Resonant Converter System for a Solid State 2.88MW/115-kV Long Pulse Modulator

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Abstract

In this paper, two control strategies for voltage balancing in a modular serial parallel resonant converter modulator system, which is used in a high voltage pulsed power application, are presented and verified by simulations and measurements. The system is based on two series parallel resonant converter modules, forming an input series output parallel stack. To obtain the given output voltage pulse of 115 kV, 9 of these input series output parallel stacks are connected in parallel at the input and in series at the output, forming an input parallel output series system. A robust input voltage balancing by an auxiliary circuit and an output voltage balancing by control is introduced and proofen by measurements. In addition, an alternative approach, where the input and output voltage balancing is achieved purley by control, is given and verified by simulations. For designing the control of this system, a large and a small signal model is derived and the influence of component tolerances is investigated.

4.1.1 Introduction

Many enhanced fundamental physic experiments, like the investigation and development of new basic materials, are performed with the help of linear colliders or spallation sources. Medium and high beta cavities used in such linear colliders/spallation sources are supplied by klystron amplifiers or inductive output tube (IOT) amplifiers. The cathode voltage for these amplifiers can be generated with long pulse modulators generating high voltage pulses with pulse lengths in the range of mil-

Table 4.1: Pulse specifications

Pulse voltage	V_{K}	$-115\,\mathrm{kV}$
Pulse current	I_{K}	$25\,\mathrm{A}$
Pulse power	P_{K}	$2.88\,\mathrm{MW}$
Pulse repetition rate	P_{RR}	$14\,\mathrm{Hz}$
Pulse width	T_{P}	$3.5\,\mathrm{ms}$
Pulse duty cycle	D	0.05
Pulse rise time (0..99 % of V_{K})	t_{rise}	$150\,\mu\mathrm{s}$
Pulse fall time (100..10 % of V_{K})	t_{fall}	$150\,\mu\mathrm{s}$

liseconds. With existing modulator topologies all the demanding requirements like a fast pulse rise time, a low voltage ripple and a long pulse length can hardly be satisfied at the same time in a compact way. For example conventional concepts like bouncer modulator topologies [41], [42] using pulse transformers become huge for long pulses since the volt-seconds of the pulse are high.

Series parallel resonant converters (SPRCs) avoid this drawback as the transformer is operated at high frequencies. Based on the optimization procedure presented in [68], a SPRC base module [45], [54] has been designed (see Fig. 4.1) for the specifications of the long pulse modulator for ESS given in Tab. 4.1. There, two SPRC-Bms form an input series, output parallel (ISOP) stack. The 400 V inputs are connected in series to share the 800 V input supply voltage, which gives the advantage to use commercial off-the-shelf 650 V break down voltage silicon MOSFET switches for the full bridges. The presented control approach, however, is generally applicable. The outputs of the two modules are connected in parallel, resulting in a lower current stress and therefore, lower losses in the semiconductors and the resonant tanks of each SPRC-Bm. To generate the full system negative pulse voltage and provide the power given in Tab.I, 9 of these ISOP stacks are connected in parallel at the input and in series at the output, forming an input parallel output series (IPOS) system (see Fig. 4.1). Besides the crucial design of the transformer regarding the isolation design (presented in [104]) and the thermal design (presented in [143]), the control of the IPOS system with

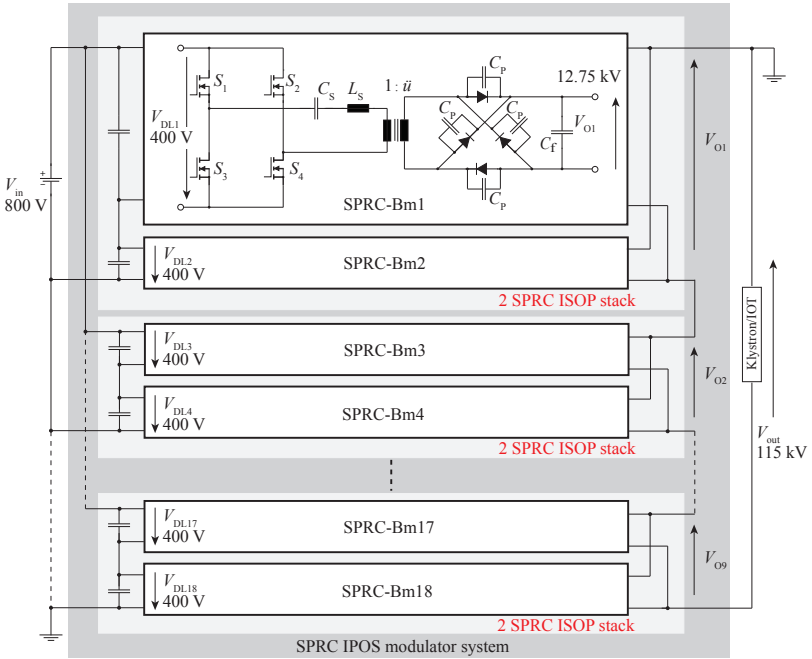

Figure 4.1: SPRC modulator system with 2 SPRC-Bm forming an ISOP stack and 9 of them are connected to an IPOS system.

an embedded ISOP system is a major challenge, which is the focus in this paper.

In the literature, several possibilities to control ISOP systems exist, as for example like the common duty ratio control [144], the charge control method for a two module ISOP system [145] or the three loop control method [146]. These methods are either working properly only for well-matched SPRC-Bms with small component tolerances, are relatively complicated or require three control loops. The methods presented in [147–149] overcome these problems and present an easily implementable strategy, which requires just two control loops for pure ISOP systems.

In contrast to ISOP systems, equal power sharing, respectively equal output voltage sharing has to be achieved for pure IPOS systems as presented in [148–151].

The tasks of a proper input/output voltage balancing, as well as an

equal power distribution between the SPRC-Bms of the combination of an IPOS system with an embedded ISOP system are not addressed by the methods given in [147–151].
In addition, in the combined IPOS-ISOP system, the input/output voltage droop due to the high power consumption during the pulse also has to be compensated, since the energy during the pulse is only provided by the DC-link capacitors.
In order to overcome this problem, the common large signal model of a single SPRC-Bm is extended in this paper, so that also changing DC-link voltages can be considered. Based on this new model, two control strategies for the entire modulator system are presented and verified by simulations as well as measurements.
In addition, an auxiliary circuit for input voltage sharing and a new method for balancing the output voltage by controlling the resonant current are presented and verified by measurements. Using the resonant currents instead of the output voltages as control variable for the output voltage balancing enables to avoid the measurement of the output voltage, so that no high voltage isolated measurement equipment is needed for the voltage balancing. An alternative, also a method, where the input and output balancing is achieved only by control, is described and verified by simulations.
Further, all large signal system and coupling equations, as well as the small system matrices for the IPOS system with an embedded ISOP system are given analytically. This representation can be used to investigate IPOS systems with an arbitrary number of ISOP systems in series, which are formed by an arbitrary number of SPRC-Bms in parallel.
First, in section 4.1.2 of this paper, the large and the small signal model of an IPOS system are derived. The proposed control systems are presented in section 4.1.3. In addition, component tolerances and their influences on the modulator behavior are discussed. Afterwards, measurement and simulation results of the controlled IPOS system are given in section 4.1.4. The detailed derivation of the large signal and the small signal model for the IPOS system is given in appendix A. All transfer functions used for the controller designs are derived in appendix B.

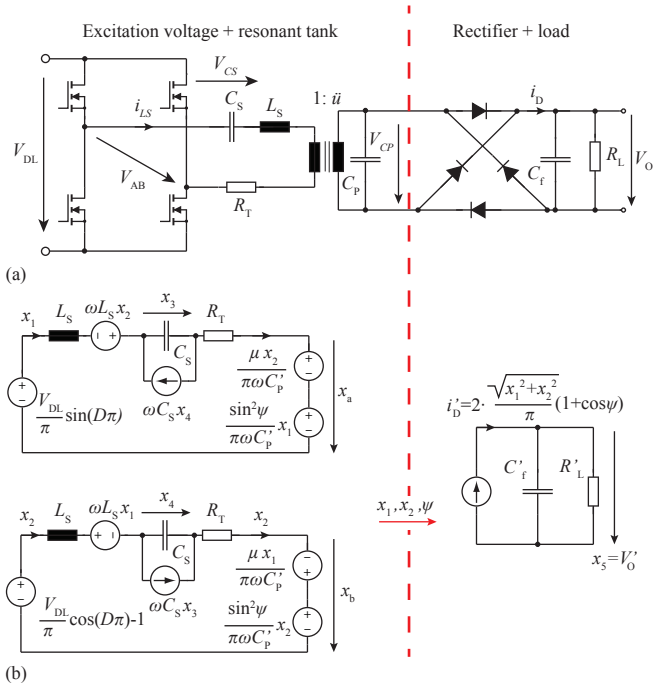

Figure 4.2: (a) Switched SPRC-Bm module model. (b) Large signal model of a single SPRC module. The left side represents the excitation voltage and the resonant tank and the right side represents the rectifier and the load.

4.1.2 Large and small signal model of the IPOS system with embedded ISOP systems

In this section, the large signal model of a SPRC-Bm is derived. Based on this model, the large signal model of the IPOS system with embedded ISOP systems is presented. Thereafter, the transition to the small signal model is discussed. There, the following definitions are made: V_O is used for the output voltage of a SPRC-Bm and V_{out} is used for the output voltage of the IPOS system.

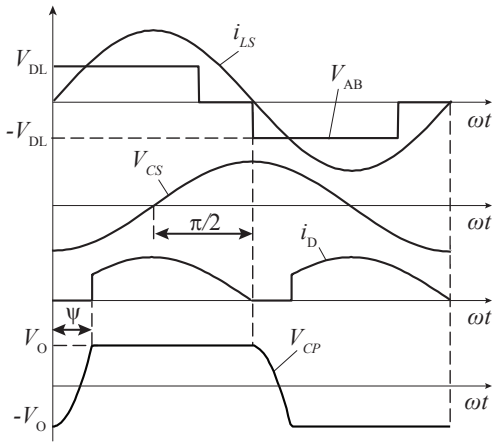

Figure 4.3: Basic voltage and current waveforms of a SPRC-Bm according to Fig. 4.2 (a).

4.1.2.1 Large signal model

A detailed derivation of the large signal model of the SPRC-Bm is given in [152–154], but for the sake of completeness, the derivation is shortly summarized below.

Large signal model of a SPRC-Bm Applying Kirchhoff's law to the SPRC-Bm in Fig. 4.2 (a) results in following nonlinear set of equations (4.1), where all magnitudes and components of the secondary transformer side are transferred to the primary ($R'_{\mathrm{L}} = R_{\mathrm{L}}/\ddot{u}^2$, $C'_{\mathrm{f}} = C_{\mathrm{f}}\ddot{u}^2$, $C'_{\mathrm{P}} = C_{\mathrm{P}}\ddot{u}^2$, $V'_{\mathrm{O}} = V_{\mathrm{O}}/\ddot{u}$, $i'_{\mathrm{D}} = i_{\mathrm{D}}\ddot{u}$, $V'_{CP} = V_{CP}/\ddot{u}$). The definitions of all parameters and components are given in Fig. 4.3 and Fig. 4.2 (a).

$$V_{\mathrm{AB}}(t) = V_{CS}(t) + V'_{CP}(t) + L_{\mathrm{S}}\frac{\mathrm{d}i_{LS}(t)}{\mathrm{d}t} + R_{\mathrm{T}}i_{LS}(t) \tag{4.1a}$$

$$\frac{\mathrm{d}V_{CS}(t)}{\mathrm{d}t} = \frac{1}{C_{\mathrm{S}}}i_{LS}(t) \tag{4.1b}$$

$$i'_{\mathrm{D}}(t) = C'_{\mathrm{f}}\frac{\mathrm{d}V'_{\mathrm{O}}(t)}{\mathrm{d}t} + \frac{V'_{\mathrm{O}}(t)}{R'_{\mathrm{L}}} \tag{4.1c}$$

It can be seen from (4.1) that there are six independent variables

(i.e. i_{LS}, V_{CS}, V_{CP}, V_{AB}, V_{O}, i_{D}) but just three equations. Therefore, additional relationships have to be found to solve the equation system. In case of the SPRC-Bm, the main waveforms in Fig. 4.3 are described with the extended describing function (E.D.F.) [155]. This means i_{LS}, V_{CS} and V_{AB} can be represented by their first harmonic terms i.e. the fundamental term of the fourier series. The output voltage V_{O} and the rectifier current i_{D} are represented by their DC fourier coefficient with sufficient accuracy [156]. This results in the equation set in (4.2) and its circuit representation in Fig. 4.2 (b). In this notation the large signal equations (4.2) can be easily solved by numerical solvers as the Runge Kutta algorithm and the circuit in Fig. 4.2 (b) can be directly implemented in a circuit simulation program like SPICE.

$$\dot{x_1} = \frac{1}{L_{\mathrm{S}}}\left(\frac{V_{\mathrm{DL}}}{\pi}\sin(D\pi) - R_{\mathrm{T}}x_1 - x_3 - x_{\mathrm{a}} + \omega L_{\mathrm{S}}x_2\right) \tag{4.2a}$$

$$\dot{x_2} = \frac{1}{L_{\mathrm{S}}}\left(\frac{V_{\mathrm{DL}}}{\pi}[\cos(D\pi) - 1] - R_{\mathrm{T}}x_2 - x_4 - x_{\mathrm{b}} - \omega L_{\mathrm{S}}x_1\right) \tag{4.2b}$$

$$\dot{x_3} = \frac{1}{C_{\mathrm{S}}}x_1 + \omega x_4 \tag{4.2c}$$

$$\dot{x_4} = \frac{1}{C_{\mathrm{S}}}x_2 - \omega x_3 \tag{4.2d}$$

$$\dot{x_5} = -\frac{x_5}{R'_{\mathrm{L}}C'_{\mathrm{f}}} + \frac{2\sqrt{x_1^2 + x_2^2}}{\pi C'_{\mathrm{f}}}[1 + \cos(\psi)] \tag{4.2e}$$

$$x_{\mathrm{a}} = \frac{1}{\pi C'_{\mathrm{P}}\omega}(x_1\sin(\psi)^2 + x_2\mu) \tag{4.2f}$$

$$x_{\mathrm{b}} = \frac{1}{\pi C'_{\mathrm{P}}\omega}(x_2\sin(\psi)^2 - x_1\mu) \tag{4.2g}$$

$$\cos\psi = 1 - \frac{x_5 C'_{\mathrm{P}}\omega}{\sqrt{x_1^2 + x_2^2}} \tag{4.2h}$$

$$\mu = \psi - \sin(\psi)\cos(\psi) \tag{4.2i}$$

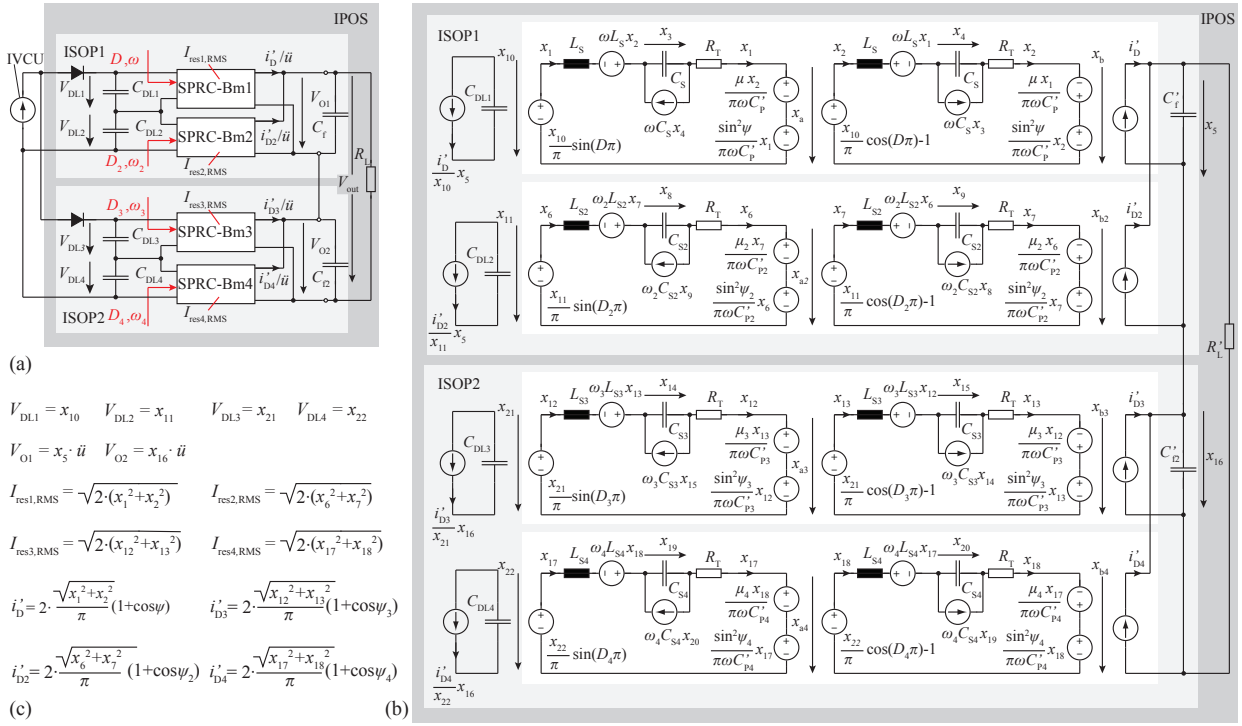

Figure 4.4: (a) Block diagram of the reduced IPOS system with embedded ISOP systems and the input voltage charging unit (IVCU). (b) Large signal model of the reduced IPOS system with variable input voltage. (c) Linking definitions between (a) and (b).

Employing state space theory on (4.2) directly results in the state vector $x(t)$ and the input vector $u(t)$ which are used for the controller design.

$$x(t) = \begin{bmatrix} x_1 & x_2 & x_3 & x_4 & x_5 \end{bmatrix}^T \tag{4.3}$$

$$u(t) = \begin{bmatrix} D & \omega & V_{\mathrm{DL}} \end{bmatrix}^T \tag{4.4}$$

Where x_1, x_2 are currents, x_3, x_4, x_5 are voltages, D is the duty cycle, ω is the angular switching frequency and V_{DL} is the DC link voltage respectively. The definitions of the elements of the $x(t)$ and $u(t)$ vectors is given in Fig. 4.4. It is worth mentioning that V_{CP} is not used as state space variable due to the fact that its signal form in Fig. 4.3 is neither sinusoidal nor differentiable without case distinctions. However, its influence on the system is fully described with (4.2f) and (4.2g) and leads to a reduction of the order of the system by 2. Based on the derived equations, the large signal model for the IPOS system is derived in the following.

Large signal model of the IPOS system For the sake of simplicity, the following investigations are performed for a reduced IPOS system as shown in Fig. 4.4 (a) and its corresponding large signal model in Fig. 4.4 (b). It is easily extendable to the full system and also the reduced system provides the conditions for a valid controller design. Figure 4.4 (a) shows the principle block diagram of the IPOS system, where two modules connected in parallel at the output and in series at the input forming a serial input parallel output system (ISOP). Furthermore, two of the ISOP systems are connected in series at the output and in parallel at the input forming a parallel input series output system (IPOS). Connecting 9 of these ISOP systems in series leads to the IPOS modulator depicted in Fig. 4.1. The input charging unit (IVCU, see Fig. 4.4 (a)) is not able to keep the input voltage constant, due to the high output power during the pulse. Therefore, for the ISOP system, the influence of the variable input voltage of each SPRC-Bm has to be considered additionally. This means that the input variable V_{DL} is described by a new state variable leading to an additional state space equation for each SPRC-Bm. The variable input voltage is modeled so that the input to output power equilibrium is fulfilled ($R_{\mathrm{T}} \ll$).

$$P_{\mathrm{out}} = P_{\mathrm{in}} \quad \longrightarrow \quad i'_{\mathrm{D}} x_5 = x_{10} i_{C_{\mathrm{DL}}} \tag{4.5}$$

$$\frac{dx_{10}}{dt} = \frac{1}{C_{\mathrm{DL1}}} \frac{x_5 i'_{\mathrm{D}}}{x_{10}}, \tag{4.6}$$

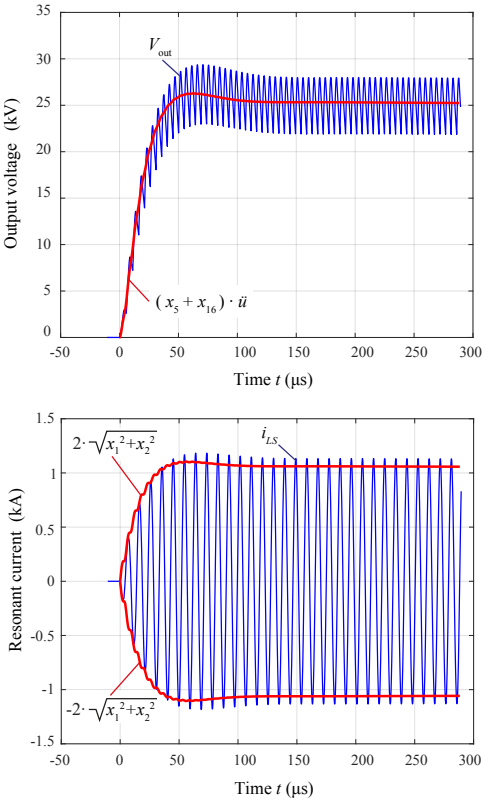

Figure 4.5: Comparison of the output voltages and resonant currents between the analytical large signal model (red) (see Fig. 4.4 (b)) and its related simulated switched signal model (blue) of the IPOS system with variable input voltage. The output voltage of the large signal model corresponds to the mean value of the output voltage V_{out} of the switched model. The resonant current of the large signal model corresponds to the peak current values of the switched system resonant current i_{LS}. The IVCU is inactive and the used simulation parameters are given in Tab. 4.2. The DC link capacitors $C_{\text{DL1}} - C_{\text{DL4}}$ are precharged to $x_{10,\text{init}} - x_{22,\text{init}}$.

where x_{10} represents the input voltage. Finally, the new state and input vectors of the reduced IPOS system are:

$$x(t) = \begin{bmatrix} x_1 & x_2 & \cdots & x_{22} \end{bmatrix}^T \tag{4.7}$$

Table 4.2: Component values of the SPRC Bms of an IPOS system with variable input voltage.

Bm1	Bm2	Bm3	Bm4		
Component and input values					
L_S	L_S2	L_S3	L_S4	(µH)	4.199
C_S	C_S2	C_S3	C_S4	(nF)	840
C'_P	C'_P2	C'_P3	C'_P4	(µF)	1.696
R_T	R_T	R_T	R_T	(Ω)	0.01
C'_f		C'_f2		(µF)	8
R'_L				(Ω)	2.875
C_DL1	C_DL2	C_DL3	C_DL4	(mF)	30
ω	ω_2	ω_3	ω_4	(krad/s)	$2\cdot\pi\cdot106$
D	D_2	D_3	D_4	(−)	0.8
$x_{10,\mathrm{init}}$	$x_{11,\mathrm{init}}$	$x_{21,\mathrm{init}}$	$x_{22,\mathrm{init}}$	(V)	400

$$u(t) = \begin{bmatrix} D & \omega & D_2 & \omega_2 & D_3 & \omega_3 & D_4 & \omega_4 \end{bmatrix}^T \tag{4.8}$$

All variables of the new state and input vectors can be identified in Fig. 4.4 (b). The complete set of equations and dependencies of the series connection of the reduced IPOS system is given in appendix A. The simulated output voltages and resonant currents from the switched model match well with the calculated large signal values as depicted in Fig. 4.5, where the output voltage V_out from the large signal model shows the mean value of the switched model and the large signal resonant current gives the envelopes of the switched system. The IVCU is inactive and the used simulation parameters are given in Tab. 4.2. The DC link capacitors $C_\mathrm{DL1} - C_\mathrm{DL4}$ are precharged to $x_{10,\mathrm{init}} - x_{22,\mathrm{init}}$. The derivation of the small signal model is given in the next section.

4.1.2.2 Small signal model

For determining the small signal model of the reduced IPOS system a valid operation point has to be calculated. Therefore, all equations in appendix A are solved until a certain point of time to obtain the operation point values of the state variables (see Tab. 4.5). By employing the well known Taylor series to the nonlinear large signal equations around

the chosen operation point, the linearized state space model is derived:

$$\begin{aligned} \Delta\dot{x} &= \mathbf{A}\Delta x + \mathbf{B}\Delta u \\ \Delta y &= \mathbf{C}\Delta x + \mathbf{D}\Delta u \end{aligned} \tag{4.9}$$

Where $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ and $\mathbf{D}$ are the matrices which describe the system, y is the output vector and Δ is the small change around the operation point [156]. After linearization and applying the Laplace transformation all transfer functions between inputs and state variables can be obtained using:

$$\mathbf{G}(s) = \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B} + \mathbf{D}. \tag{4.10}$$

The small signal transfer functions can be validated by superimposing a small perturbation (approximately 5 % of the actual nominal value, [153]) to the duty cycle and/or the switching frequency of the large signal model and by performing an AC analysis over a certain perturbation frequency range. The linearized small signal transfer functions match well with the measured small signal transfer functions, if the perturbation frequency is maximal 20 % of the nominal switching frequency, as it has been shown in [153]. It is worth mentioning that the resulting transfer function matrix $\mathbf{G}(s)$ is only valid in the region close to the chosen operation point and has to be recalculated if another operation point is in the scope of interest.

4.1.3 Control of an IPOS system with embedded ISOP systems

The output voltage V_{out} of the resonant modulator system can be controlled by the duty cycle D and/or by the frequency f [157]. Due to the high pulsed output power of 159.75 kW of a single SPRC-Bm, the input voltage charging unit is not able to keep the DC link voltage V_{DL} constant during the pulse. This results in an input and consequently also in an output voltage droop which has to be compensated.
The voltage droop of V_{out} and the influence of component tolerances are discussed first. Afterwards, an detailed investigation concerning input and output voltage balancing methods is presented.

4.1.3.1 Voltage droop compensation / component tolerances

Voltage droop compensation Figure 4.6 (a) (output voltage versus frequency) and Fig. 4.6 (b) (output voltage versus duty cycle) show the

output voltage at the beginning of the pulse, with an input voltage of $V_{\mathrm{DL}} = 400\,\mathrm{V}$ (blue lines) and at the end of the pulse discharged to an input voltage of $V_{\mathrm{DL}} = 330\,\mathrm{V}$ (red lines). The solid lines are the nominal transfer characteristics and the dashed lines represent the component tolerances. If the modulator is operated with a constant frequency f_A, the output voltage starting in point A ($V_{\mathrm{out}} = 12.75\,\mathrm{kV}$) is decreasing and will end in point E ($V_{\mathrm{out}} = 10.6\,\mathrm{kV}$) (see Fig. 4.6 (a) and (b)). The crosses depicted in Fig. 4.6 (b), marked with D_{fA}, D'_{fA} and D''_{fA}, define the minimum duty cycles, which allow zero voltage switching (ZVS) if the SPRC-Bm is operated above the resonance frequency (see Fig. 4.6 (a)). To compensate the voltage droop,the frequency f_A is reduced during the pulse until it reaches f_B in point B, see Fig. 4.6 (a).

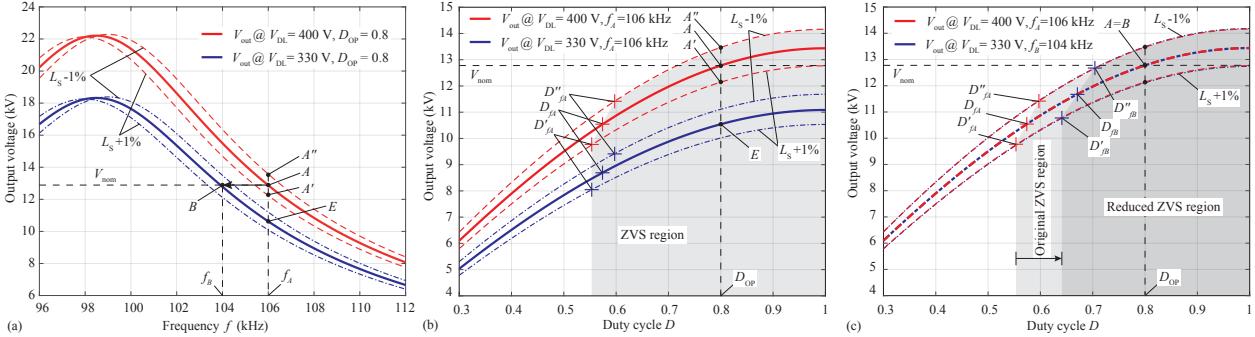

Figure 4.6: Output voltage characteristics given for different input voltages in (a) versus frequency and in (b) and (c) versus duty cycle. The red curves are the voltages at the beginning of the pulse with an input voltage $V_{\mathrm{DL}} = 400\,\mathrm{V}$ and the blue curves are the voltages at the end of the pulse with $V_{\mathrm{DL}} = 330\,\mathrm{V}$ due to the voltage droop of the main capacitor. The dashed lines indicate the tolerances of the series inductance L_{S}. If the modulator would be operated with constant frequency f_A, the output voltage starting in point A is decreasing and will end in point E ((a) and (b)). To compensate the voltage droop, the frequency f_A is reduced until it reaches f_B in point B, ((a) and (c)). The reduction of the frequency leads to an overlap of the output voltage characteristics and a constant output voltage respectively, but also to a reduction of the ZVS range (c).

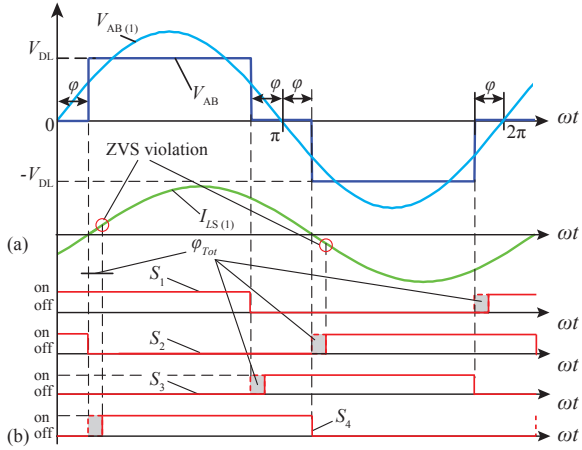

Figure 4.7: (a) Input impedance angle φ between $V_{\mathrm{AB}\,(1)}$ and $I_{LS\,(1)}$. (b) Switching signals of the switches $S_1 - S_4$ with the interlocking angle φ_{Tot}. A ZVS violation occurs in the switches S_2 and S_4 of the SPRC-Bm because the current $I_{LS\,(1)}$ crosses zero before the switches S_2 and S_4 turn on.

The compensation is realized by decreasing the frequency linearly, if the output voltage V_{out} crosses a certain limit. The reduction of the frequency leads to an overlap of the output voltage characteristics (compare Fig. 4.6 (b) and (c)), but the minimum duty cycles D_{fA}, D'_{fA} and D''_{fA} are moving towards higher duty cycle values and ending in D_{fB}, D'_{fB} and D''_{fB}. This leads to a reduced ZVS range, which has to be considered during the design process. The minimum duty cycles can be calculated by

$$D = \left(\frac{\pi}{2} - \varphi_{\mathrm{ZVS}}\right)\frac{2}{\pi}, \quad \text{with} \quad \varphi_{\mathrm{ZVS}} = \varphi - \varphi_{Tot}. \tag{4.11}$$

The angle φ is the input impedance angle between the first harmonic of the full bridge output voltage $V_{\mathrm{AB}(1)}$ and the resonant current $I_{\mathrm{LS}(1)}$ (see Fig. 4.7 (a)) and is calculated with (35) in [54]. This angle has to be reduced by the interlocking angle φ_{Tot} to ensure ZVS in all switches of the SPRC Bm. Figure 4.7 (b) shows the ZVS violation where the interlocking angle is not considered in the switching signals.

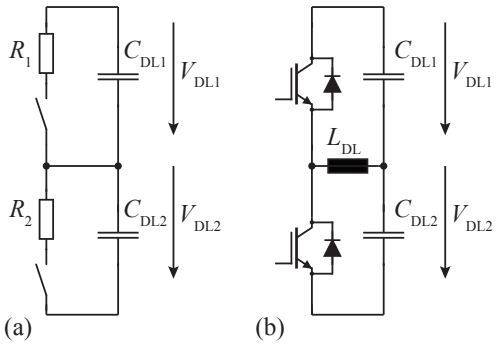

Figure 4.8: (a) Switched resistor balancing and (b) active balancing.

Component tolerances The tolerance discussion is based on the converter design given in [77], which is the prototype system related to the proposed controller design. The total tolerance $s(k)$ of parts which are formed by k components is given by

$$s(k) = \frac{s_1}{\sqrt{k}} \tag{4.12}$$

where s_1 is the tolerance of a single component. The tolerance s_1 of the used NP0 ceramic capacitors in [77] is 5 %. This results in a total tolerance $s_{CS}(k) = \pm 0.167\,\%$ for C_S which is made of 896 capacitors and a total tolerance $s_{CP}(k) = \pm 0.34\,\%$ for C_P which is made of 216 NP0 capacitors. Therefore, it can be concluded that the resonant capacitors have a negligible tolerance. However, the inductor L_S which is a single component has a relatively large tolerance. The influence of this tolerance is clearly visible in Fig. 4.6. The variation of the inductance by $\pm 1\,\%$ (dashed lines) results in a voltage change of $\mp 5\,\%$ in point A' and A'' compared to the nominal value V_{nom} (solid lines) in point A.

4.1.3.2 Input and output voltage balancing

For IPOS systems equal power sharing is achieved by ensuring output voltage sharing (OVS) which results in equal input current sharing (ICS) [148]. Unfortunately, the ICS of the IPOS system does not lead to equal input voltage sharing of the SPRC-Bms of the embedded ISOP systems. Due to the tolerances of the resonant inductor each of the

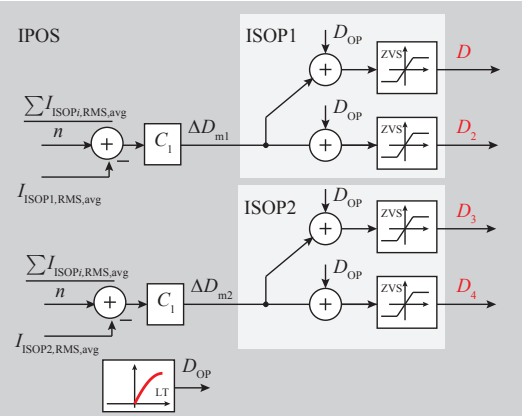

Figure 4.9: Control block diagram of the output voltage balancing, based on the resonant currents where n is the number of ISOP systems. The operation point duty cycle D_{OP} is given from an lookup table (LT).

two SPRC-Bms in the ISOP system could transfer different amounts of power to the output, which is provided by their input capacitors. This results in an input voltage divergence which has to be compensated either with the help of an auxiliary circuit or by control.

If the input voltage balancing can not be achieved by control, since for example the ZVS condition is violated, different auxiliary circuits can be used to balance the input voltage. The input voltage balancing concept realized with an auxiliary circuit and an output voltage balancing by control is given first. Afterwards, additionally a method based on an input and output voltage balancing purely by control is presented.

Input voltage balancing by auxiliary circuit and output voltage balancing by control In Fig. 4.8 (a), the input voltage balancing is achieved with switched auxiliary resistors which are in parallel to the DC link capacitors C_{DL} [158]. The resistors discharge the input capacitors to equal voltages by turning on their switches, hence leading to an equal power sharing. However, the unbalanced power has to be dissipated by the auxiliary resistors. This drawback is avoided by the circuit shown in Fig. 4.8 (b) [159]. There, the unbalanced power from

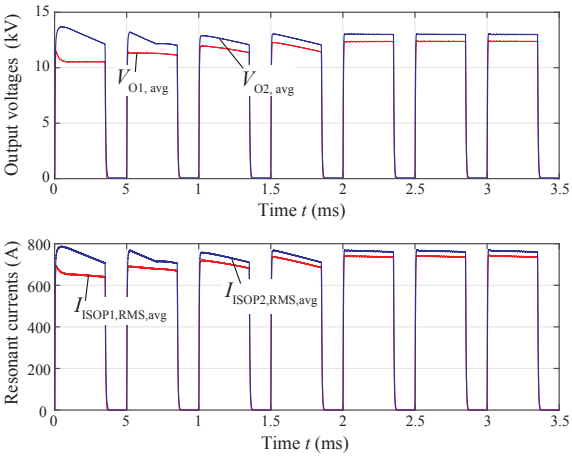

Figure 4.10: Comparison of the dynamic behaviour between the averaged output voltages ($V_{\mathrm{O1,avg}}, V_{\mathrm{O2,avg}}$) and the averaged resonant RMS currents ($I_{\mathrm{ISOP1,RMS,avg}}, I_{\mathrm{ISOP2,RMS,avg}}$) of the ISOP systems.

one capacitor is used to charge the other capacitor until both have equal voltages. Therefore, the active buck balancing circuit is used for the input voltage balancing. If $V_{\mathrm{DL1}} > V_{\mathrm{DL2}}$, the circuit acts as a buck converter where V_{DL1} is the input voltage and V_{DL2} is the output voltage. If $V_{\mathrm{DL1}} < V_{\mathrm{DL2}}$, the circuit acts as a buck converter where V_{DL2} is the input voltage and V_{DL1} is the output voltage.
For the output voltage balancing, the concept shown in Fig. 4.9 could be employed. If it is not possible to access all output voltages, e.g. the high voltage transformers are oil isolated, an alternative way to balance the output voltages of each ISOP system is to balance the resonant currents of each ISOP system. A comparison of the dynamic behaviour between the averaged output voltages ($V_{\mathrm{O1,avg}}, V_{\mathrm{O2,avg}}$) and the averaged resonant RMS currents ($I_{\mathrm{ISOP1,RMS,avg}}, I_{\mathrm{ISOP2,RMS,avg}}$) of the ISOP systems is shown in Fig. 4.10. There,

$$I_{\mathrm{ISOP1,RMS,avg}} = \frac{I_{\mathrm{res1,RMS}} + I_{\mathrm{res2,RMS}}}{2} \tag{4.13}$$

and

$$I_{\mathrm{ISOP2,RMS,avg}} = \frac{I_{\mathrm{res3,RMS}} + I_{\mathrm{res4,RMS}}}{2}, \tag{4.14}$$

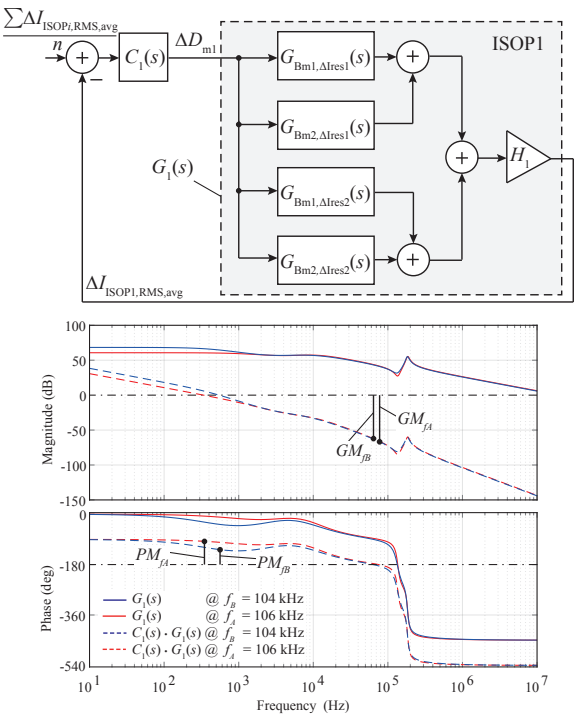

Figure 4.11: Small signal control block diagram and open loop bode diagram of the output voltage compensation based on the resonant currents of an ISOP system, with (dashed lines) and without (solid lines) compensator. The compensator $C_1(s)$ is a pure integral controller with $T_\mathrm{I} = 0.5$ leading to the phase margins of $PM_{fB} = 53.6\,^\circ$ and $PM_{fA} = 83.2\,^\circ$. The gain margins are $GM_{fB} = 62.7\,\mathrm{dB}$ and $GM_{fA} = 65.6\,\mathrm{dB}$.

where $I_{\mathrm{res},i,\mathrm{RMS}}$ is the resonant RMS current of the i-th SPRC-Bm (see Fig. 4.4 (a)). In order that the duty cycle variation $\Delta D_{\mathrm{m}i}$ in the IPOS control loop does not interfere with the operating point duty cycle D_{OP}, the decoupling condition

$$\sum \Delta D_{\mathrm{m}i} = 0 \tag{4.15}$$

has to be fulfilled. The proof that $\Delta D_{\mathrm{m}i}$ is not interfering with D_{OP} is (for n=2)

$$\begin{aligned}\Delta D_{\mathrm{m1}} &= \left(\frac{\sum \Delta I_{\mathrm{ISOP}i,\mathrm{RMS,avg}}}{n} - \Delta I_{\mathrm{ISOP1,RMS,avg}}\right) C_1 \\ \Delta D_{\mathrm{m2}} &= \left(\frac{\sum \Delta I_{\mathrm{ISOP}i,\mathrm{RMS,avg}}}{n} - \Delta I_{\mathrm{ISOP2,RMS,avg}}\right) C_1 \\ \Delta D_{\mathrm{m1}} &+ \Delta D_{\mathrm{m2}} = 0\end{aligned} \tag{4.16}$$

with

$$\Delta I_{\mathrm{ISOP2,RMS,avg}} = \sum \Delta I_{\mathrm{ISOP}i,\mathrm{RMS,avg}} - \Delta I_{\mathrm{ISOP1,RMS,avg}} \tag{4.17}$$

The small signal control block diagram and the open loop bode diagram of the output voltage compensation, with (dashed lines) and without (solid lines) compensator, are shown in Fig. 4.11. The compensator $C_1(s)$ is a pure integral controller with $T_{\mathrm{I}} = 0.5$, leading to the phase margins of $PM_{fB} = 53.6\,^\circ$ and $PM_{fA} = 83.2\,^\circ$.

$$C_1(s) = \frac{1}{sT_{\mathrm{I}}} \tag{4.18}$$

The gain margins are $GM_{fB} = 62.7\,\mathrm{dB}$ and $GM_{fA} = 65.6\,\mathrm{dB}$, with $f_B = 104\,\mathrm{kHz}$ and $f_A = 106\,\mathrm{kHz}$, defining the frequency range of the droop compensation. The minor influence of f_A and f_B on the transfer characteristics is shown in Fig. 4.11. Since the droop compensation reduces the influence of the variable input voltage, the duty cycle to the averaged resonant RMS current transfer function is derived from the small signal control block diagram of the reduced IPOS system with fix input voltage shown in Fig. 4.11 as

$$\begin{aligned}G_1(s) = \frac{\Delta I_{\mathrm{ISOPi,RMS,avg}}}{\Delta D_{\mathrm{m}i}} &= [G_{\mathrm{Bm1},\Delta\mathrm{Ires1}}(s) + \\ &+ G_{\mathrm{Bm2},\Delta\mathrm{Ires1}}(s) + G_{\mathrm{Bm1},\Delta\mathrm{Ires2}}(s) + \\ &+ G_{\mathrm{Bm2},\Delta\mathrm{Ires2}}(s)] \cdot H_1.\end{aligned} \tag{4.19}$$

$G_{\mathrm{Bm}i,\Delta\mathrm{Ires}j}(s)$ is the resonant RMS current transfer function from the i-th SPRC-Bm to the j-th resonant RMS current and the constant factor $H_1 = 0.5$ to calculate the average.
A detailed derivation of the transfer function $G_1(s)$ is given in appendix B.

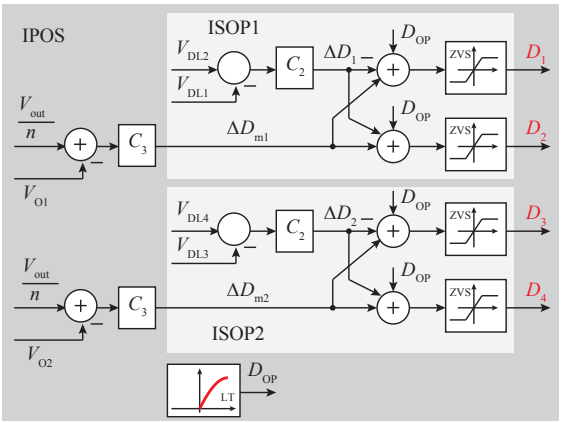

Figure 4.12: Control block diagram of the input and output voltage balancing, where n is the number of ISOP systems. The operation point duty cycle D_{OP} is given from an lookup table (LT).

Input and output voltage balancing by control The control strategy for the ISOP system as depicted in Fig. 4.12 is discussed in a first step and afterwards the strategy for the IPOS system based on the regulation of the output voltages is developed. In the literature several possibilities to control ISOP systems exist. The concepts presented in [147], [148] and [149] show an easily implementable control strategy which employs just two control loops. In the considered system, these two loops are further reduced to one, because D_{OP}, which is responsible for the operation point is given from a lookup table (see Fig. 4.12). To ensure an equal power sharing of the ISOP system one has to ensure an equal input voltage sharing (IVS) which automatically results in equal output current sharing (OCS) and respectively equal power sharing [148]. For IPOS systems equal power sharing is achieved by ensuring output voltage sharing (OVS) which leads to equal input current sharing (ICS) [148]. In order that both the duty cycle variation ΔD_i in the ISOP and $\Delta D_{\mathrm{m}i}$ in the IPOS control loop do not interfere with the operation point duty cycle D_{OP}, the decoupling conditions

$$\sum \Delta D_i = 0 \quad \text{and} \quad \sum \Delta D_{\mathrm{m}i} = 0 \tag{4.20}$$

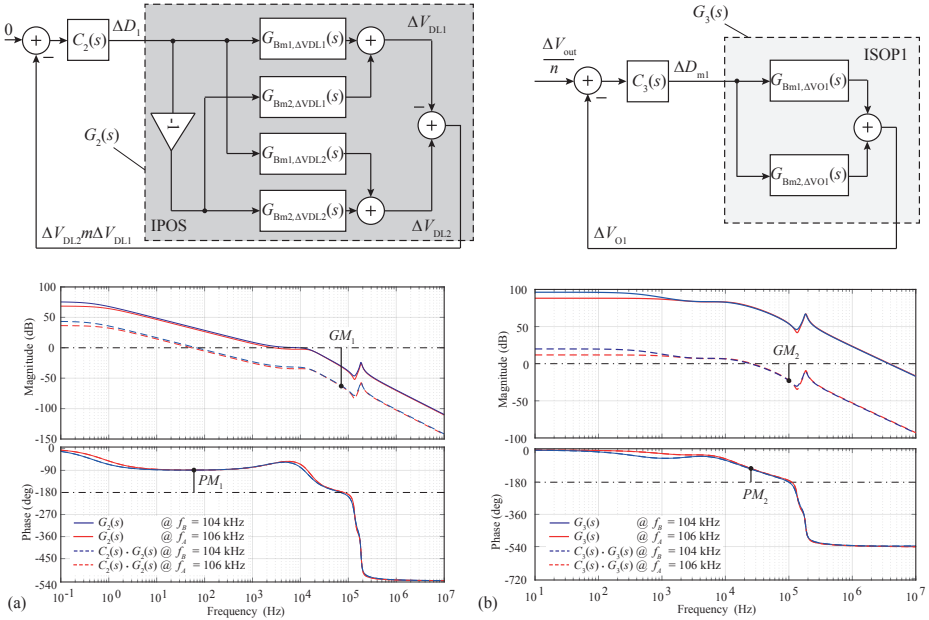

Figure 4.13: Small signal control block diagram and open loop bode diagram of (a) the input voltage regulation and (b) the output voltage compensation with (dashed lines) and without (solid lines) compensator. The compensators $C_2(s)$ and $C_3(s)$ are proportional controllers with $K_{p2} = 0.025$ and $K_{p3} = 152.368\text{E–}6$ leading to the phase margins of $PM_1 = 91\,^\circ$ and $PM_2 = 75\,^\circ$. The gain margins are $GM_1 = 62\,\text{dB}$ and $GM_2 = 19.5\,\text{dB}$. Both diagrams are given for the frequency range of the droop compensation to point out their minor influences on the transfer characteristics.

have to be fulfilled. The proof from (4.15) for $\Delta D_{\mathrm{m}i}$ is still valid by replacing the resonant currents from Fig. 4.9 by the output voltages shown in Fig. 4.12. The decoupling condition for ΔD_i is fulfilled by applying the same value ΔD_i for each SPRC-Bm with opposite sign within an ISOP system. The small signal control block diagrams and open loop bode diagrams of the input voltage and the output voltage compensation, with (dashed lines) and without (solid lines) compensators, are shown in Fig. 4.13 (a), respectively (b). The compensators $C_2(s)$ and $C_3(s)$ are simple proportional controllers with $K_{\mathrm{p2}} = 0.025$ and $K_{\mathrm{p3}} = 152.368\mathrm{E}{-6}$, resulting in a phase margins of $PM_1 = 91\,^\circ$ and $PM_2 = 75\,^\circ$. The gain margins are $GM_1 = 62\,\mathrm{dB}$ and $GM_2 = 19.5\,\mathrm{dB}$. Again, both open loop functions are evaluated for different switching frequencies (f_B=104 kHz, f_A=106 kHz) to point out their minor influences on the transfer characteristics (see Fig. 4.13 (a) and (b)), hence leading to fix compensator gains for the full droop compensation frequency range.
Using the transfer functions from the small signal model of the reduced IPOS system with variable input voltage and the control loop depicted in Fig. 4.13 (a), the duty cycle to input voltage difference transfer function can be obtained as

$$\begin{aligned} G_2(s) = \frac{\Delta V_{\mathrm{DL2}} m \Delta V_{\mathrm{DL1}}}{\Delta D_1} &= -G_{\mathrm{Bm1},\Delta\mathrm{VDL1}}(s) + \\ &+ G_{\mathrm{Bm2},\Delta\mathrm{VDL1}}(s) + G_{\mathrm{Bm1},\Delta\mathrm{VDL2}}(s) + \\ &- G_{\mathrm{Bm2},\Delta\mathrm{VDL2}}(s) \end{aligned} \tag{4.21}$$

where $G_{\mathrm{Bm}i,\Delta\mathrm{VDL}j}$ is the input voltage transfer function from the i-th SPRC-Bm to the j-th input voltage. Due to the droop compensation the duty cycle to output voltage transfer function is derived from the small signal model of the reduced ISOP-IPOS system with fix input voltage and the control loop depicted in Fig. 4.13 (b) as

$$G_3(s) = \frac{\Delta V_{\mathrm{O1}}}{\Delta D_{\mathrm{m1}}} = G_{\mathrm{Bm1},\Delta\mathrm{VO1}}(s) + G_{\mathrm{Bm2},\Delta\mathrm{VO1}}(s) \tag{4.22}$$

where $G_{\mathrm{Bm}i,\Delta\mathrm{VO1}}$ is the output voltage transfer function from the i-th SPRC-Bm to the first output voltage.
A detailed derivation of the transfer functions $G_2(s)$ and $G_3(s)$ is given in appendix B.

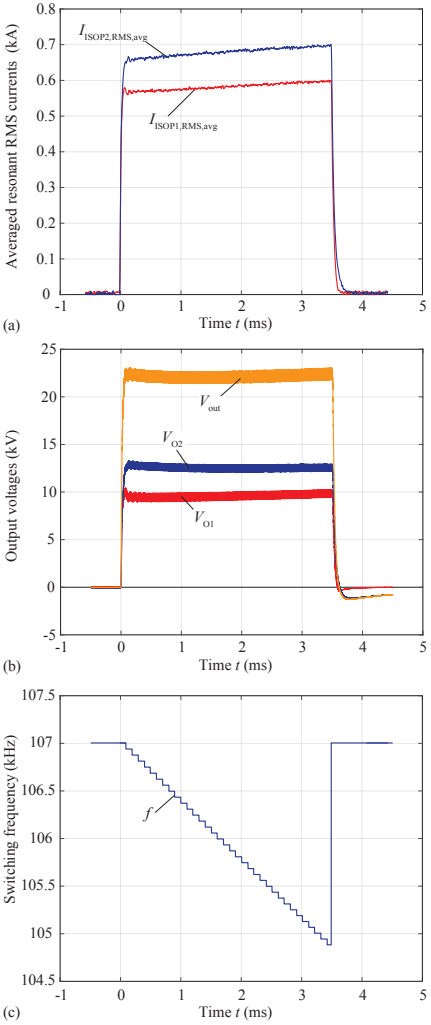

Figure 4.14: Measured IPOS signals with no output voltage balancing. (a) Averaged resonant RMS currents $I_{\mathrm{ISOP1,RMS,avg}}$, $I_{\mathrm{ISOP2,RMS,avg}}$. (b) Output voltages V_{O1},V_{O2} and V_{out}. (c) Adaption of the switching frequency for the droop compensation with a start frequency of 107 kHz and an end frequency of 104.8 kHz.

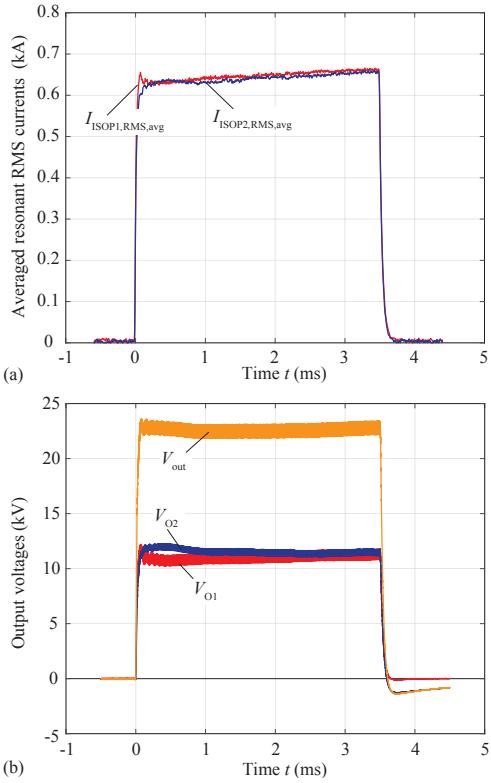

Figure 4.15: Measured IPOS signals with active output voltage balancing. (a) Averaged resonant RMS currents $I_{\mathrm{ISOP1,RMS,avg}}$, $I_{\mathrm{ISOP2,RMS,avg}}$. (b) Output voltages V_{O1}, V_{O2} and V_{out}. The adaption of the switching frequency for the droop compensation with a start frequency of 107 kHz and an end frequency of 104.8 kHz is the same as depicted in Fig. 4.14 (c). The used integral compensator value is $T_{\mathrm{I}} = 0.5$.

4.1.4 Measurement and simulation results

In the following, first measurement results of the IPOS system (see Fig. 4.4 (a)) utilising the input voltage balancing by an auxiliary circuit and the output voltage balancing by control are presented. Afterwards, simulation results based on the input and the output voltage balancing by control only are shown.

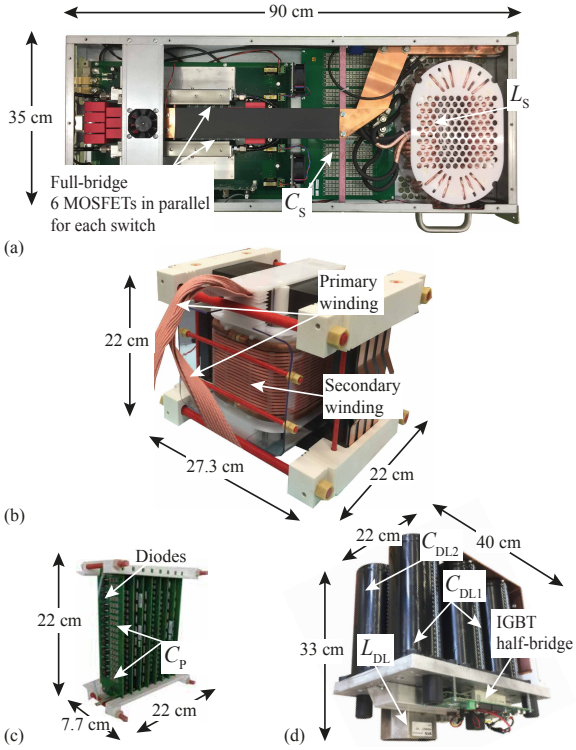

Figure 4.16: Single SPRC-Bm consisting of (a) a full-bridge with 6 MOSFETs in parallel for each switch, a series inductor L_S and a series capacitor C_S, (b) an high voltage high frequency transformer and (c) an output rectifier with parallel capacitor C_P. (d) Auxiliary circuit for the input voltage balancing (Fig. 4.8 (b)).

4.1.4.1 Measurement results of the IPOS system based on the input voltage balancing by an auxiliary circuit and output voltage balancing by control

The measured averaged resonant RMS currents $I_{\mathrm{ISOP1,RMS,avg}}$, $I_{\mathrm{ISOP2,RMS,avg}}$ and the measured ISOP output voltages (V_{O1},V_{O2} and V_{out}) for a system without output voltage balancing are depicted in Fig. 4.14 (a) and (b). For compensating the droop the switching frequency is decreased from 107 kHz to 104.8 kHz (see. Fig. 4.14 (c)). The measured resonance

Table 4.3: Measured component and initial values.

	Bm1	Bm2	Bm3	Bm4
L_S (µH)	4.4	4.31	4.25	4.29
V_{DL} (V)	400.8	400.2	399.3	401.7
R_L (Ω)	1220			

inductance (L_S), the input voltages (V_{DL}) and the load resistor (R_L) are given in Tab. 4.3. The IPOS system is operated with an output voltage of 23 kV compared to the nominal output voltage of 25.5 kV, due to the component tolerances and the different load value (compare nominal load value in Tab. 4.4). Figure 4.15 shows all voltages and currents in case of an active output voltage balancing. The droop compensation by adapting the switching frequency is the same as depicted in Fig. 4.14 (c). The applied pure integral compensator value is $T_I = 0.5$ and the control cycle of the implemented control algorithm is 80 kS/s. The output voltages are well balanced which leads to an equally distributed power stress between the single SPRC-Bms. Figure 4.16 shows the components of a single SPRC-Bm consisting of a full-bridge with 6 MOSFETs in parallel for each switch, a series inductor L_S, a series capacitor C_S (Fig. 4.16 (a)), the high voltage high frequency transformer (Fig. 4.16 (b)) and an output rectifier with parallel capacitor C_P (Fig. 4.16 (c)). The active input voltage balancing auxiliary circuit (Fig. 4.8 (b)), is shown in Fig. 4.16 (d). Two of these auxiliary circuits are used for the reduced IPOS prototype system.

4.1.4.2 Simulation results of the IPOS system based on the input and output voltage balancing by control

The pure control based approach is more sensitive to the ZVS reduction due to the input voltage droop and the component tolerances (see section 4.1.3.1). This can result in destructive hard switching of the full bridge switches. In order to obtain a robust system, the solution with auxiliary circuit was implemented and the pure control based is therefore verified only by simulations.
Figures 4.17 (a) and (b) show the input and output voltages in case the modules have nominal component values plus tolerances. The inductance values are varied by ± 1 % and the DC link capacitance values

Table 4.4: Nominal component values with tolerances and initial values used for the simulations.

	Bm1	Bm2	Bm3	Bm4
L_S (µH)	4.241	4.199	4.157	4.199
C_S (nF)	840	840	840	840
C_P (nF)	4.234	4.234	4.234	4.234
$\ddot{u}$ (−)	20	20	20	20
C_{DL} (mF)	30	31.5	31.5	30
V_{DL} (V)	409.75	390.25	390.25	409.75
C_f (nF)	20		20	
R_L (Ω)	1150			

by 5 % with according initial voltages. The exact values are given in Tab. 4.4. All modules are operated interleaved with a start switching frequency of 106 kHz, an end frequency of 104.9 kHz (see Fig. 4.17 (c)) and a duty cycle D_{OP} of 0.8. This results in an output voltage operating point of 25.5 kV (= 2 x 12.75 kV). The pulse repetition rate is increased to 200 Hz to decrease the simulation times and memory consumption. In the pulse break after each 3.5 ms pulse, the DC link capacitors are recharged to 800 V in total. Applying the control loops given in section 4.1.3.2 results in a stable operation as can be seen in Fig. 4.17 (a) and (b). The input voltage controller compensates the voltage difference after four pulses. During these four pulses, the droop compensation is not active because the output voltage does not reach the nominal voltage limit so that the modules are operated with constant frequency. The output voltage compensation is also achieved after four pulses. The used compensator values are $K_{p2} = 0.025$ and $K_{p3} = 152.368E–6$.

4.1.5 Conclusion

In this paper, a large signal model for a nested ISOP-IPOS system with non constant input voltages is presented in detail. Additionally, the transition to the small signal model is derived. Two control strategies for an optimal power sharing, input and output voltage balancing are given for the nested system. In the first case, the input voltage bal-

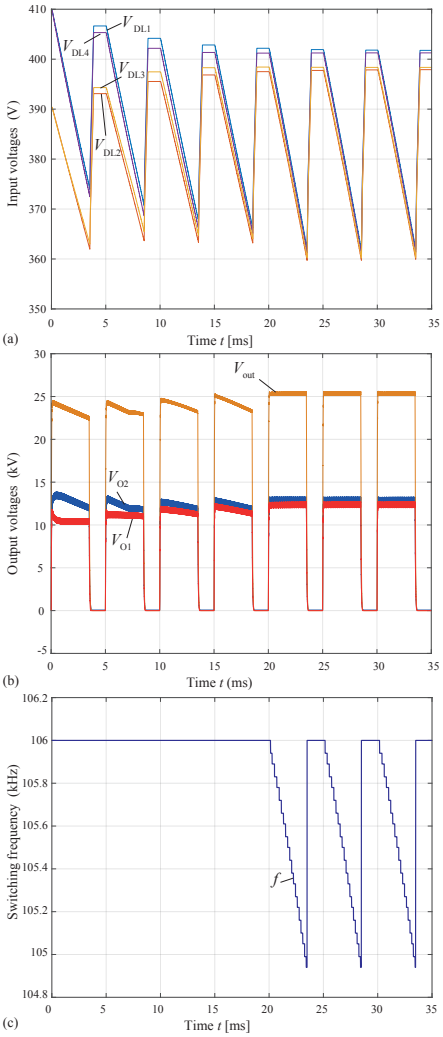

Figure 4.17: (a) Input voltages V_{DL1},V_{DL2},V_{DL3} and V_{DL4}, in case all control loops are active. (b) Output voltages V_{O1},V_{O2} and V_{out}. (c) Adaption of the switching frequency for the droop compensation with a start frequency of 106 kHz and an end frequency of 104.9 kHz. The compensator values are $K_{\mathrm{p2}} = 0.025$ and $K_{\mathrm{p3}} = 152.368\mathrm{E}{-6}$.

ancing is achieved with the help of an auxiliary circuit and the output voltage balancing by control of the resonant currents. The performance of the proposed controller is demonstrated with measurement results. Further, an input and output voltage balancing by control is presented and verified by simulations. In addition, the effects of the output voltage droop compensation of the IPOS system depending on the DC link capacitor and resonant tank components tolerances is shown.

4.1.6 Appendix A

The full set of equations of the reduced IPOS system consisting of 4 SPRC-Bm with variable input voltage is given below. Each set (4.25), (4.26), (4.27), (4.28) is for a single SPRC-Bm. (4.23) and (4.24) are the linking equations for the parallel output connection of the ISOP system and the series output connection of the IPOS system. (4.25e), (4.26e), (4.27e) and (4.28e) consider the variable input voltage of each SPRC-Bm. All equations are related to Fig.4.4 (b) and all magnitudes and components are transferred to the primary sides of the transformers with $R'_{\mathrm{L}} = R_{\mathrm{L}}/\ddot{u}^2$, $C'_{\mathrm{f}x} = C_{\mathrm{f}x}\ddot{u}^2$ and $C'_{\mathrm{P}x} = C_{\mathrm{P}x}\ddot{u}^2$. If a system with constant input voltage is investigated x_{10}, x_{11}, x_{21} and x_{22} have to be replaced by V_{DL0}, V_{DL02}, V_{DL03} and V_{DL04} and (4.25e), (4.26e), (4.27e) and (4.28e) are removed from the system.

$$\begin{aligned}\dot{x_5} = &-\frac{x_5 + x_{16}}{C'_{\mathrm{f}} R'_{\mathrm{L}}} + \frac{2\sqrt{x_1^2 + x_2^2}}{C'_{\mathrm{f}}\pi}[1 + \cos(\psi)] + \\ &+ \frac{2\sqrt{x_6^2 + x_7^2}}{C'_{\mathrm{f}}\pi}[1 + \cos(\psi_2)]\end{aligned} \tag{4.23}$$

$$\begin{aligned}\dot{x_{16}} = &-\frac{x_{16} + x_5}{C'_{\mathrm{f2}} R'_{\mathrm{L}}} + \frac{2\sqrt{x_{12}^2 + x_{13}^2}}{C'_{\mathrm{f2}}\pi}[1 + \cos(\psi_3)] + \\ &+ \frac{2\sqrt{x_{17}^2 + x_{18}^2}}{C'_{\mathrm{f2}}\pi}[1 + \cos(\psi_4)]\end{aligned} \tag{4.24}$$

$$\dot{x_1} = \frac{x_{10}\sin(D\pi)}{\pi L_{\mathrm{S}}} - \frac{r x_1 + x_3 + x_{\mathrm{a}}}{L_{\mathrm{S}}} + \omega x_2 \tag{4.25a}$$

$$\dot{x_2} = \frac{x_{10}[\cos(D\pi) - 1]}{\pi L_{\mathrm{S}}} - \frac{r x_2 + x_4 + x_{\mathrm{b}}}{L_{\mathrm{S}}} - \omega x_1 \tag{4.25b}$$

$$\dot{x_3} = \frac{1}{C_{\mathrm{S}}} x_1 + \omega x_4 \tag{4.25c}$$

$$\dot{x_4} = \frac{1}{C_{\mathrm{S}}} x_2 - \omega x_3 \tag{4.25d}$$

$$\dot{x_{10}} = -\frac{(4\sqrt{x_1^2 + x_2^2} - 2x_5 C'_{\mathrm{P}}\omega)}{\pi} \frac{x_5}{x_{10}} \frac{1}{C_{\mathrm{DL1}}} \tag{4.25e}$$

$$x_{\mathrm{a}} = \frac{1}{\pi C'_{\mathrm{P}}\omega}(x_1 \sin(\psi)^2 + x_2\mu) \tag{4.25f}$$

$$x_{\mathrm{b}} = \frac{1}{\pi C'_{\mathrm{P}}\omega}(x_2 \sin(\psi)^2 - x_1\mu) \tag{4.25g}$$

$$\cos\psi = 1 - \frac{x_5 C'_{\mathrm{P}}\omega}{\sqrt{x_1^2 + x_2^2}} \tag{4.25h}$$

$$\mu = \psi - \sin(\psi)\cos(\psi) \tag{4.25i}$$

$$\dot{x_6} = \frac{x_{11}\sin(D_2\pi)}{\pi L_{\mathrm{S2}}} - \frac{rx_6 + x_8 + x_{\mathrm{a2}}}{L_{\mathrm{S2}}} + \omega x_7 \tag{4.26a}$$

$$\dot{x_7} = \frac{x_{11}[\cos(D_2\pi) - 1]}{\pi L_{\mathrm{S2}}} - \frac{rx_7 + x_9 + x_{\mathrm{b2}}}{L_{\mathrm{S2}}} - \omega x_6 \tag{4.26b}$$

$$\dot{x_8} = \frac{1}{C_{\mathrm{S2}}} x_6 + \omega x_9 \tag{4.26c}$$

$$\dot{x_9} = \frac{1}{C_{\mathrm{S2}}} x_7 - \omega x_8 \tag{4.26d}$$

$$\dot{x_{11}} = -\frac{(4\sqrt{x_6^2 + x_7^2} - 2x_5 C'_{\mathrm{P2}}\omega)}{\pi} \frac{x_5}{x_{11}} \frac{1}{C_{\mathrm{DL2}}} \tag{4.26e}$$

$$x_{\mathrm{a2}} = \frac{1}{\pi C'_{\mathrm{P2}}\omega}(x_6 \sin(\psi_2)^2 + x_7\mu_2) \tag{4.26f}$$

$$x_{\mathrm{b2}} = \frac{1}{\pi C'_{\mathrm{P2}}\omega}(x_7 \sin(\psi_2)^2 - x_6\mu_2) \tag{4.26g}$$

$$\cos\psi_2 = 1 - \frac{x_5 C'_{\mathrm{P2}}\omega}{\sqrt{x_6^2 + x_7^2}} \tag{4.26h}$$

$$\mu_2 = \psi_2 - \sin_2(\psi_2)\cos(\psi_2) \tag{4.26i}$$

$$\dot{x_{12}} = \frac{x_{21}\sin(D_3\pi)}{\pi L_{\mathrm{S3}}} - \frac{rx_{12} + x_{14} + x_{\mathrm{a3}}}{L_{\mathrm{S3}}} + \omega x_{13} \tag{4.27a}$$

$$\dot{x_{13}} = \frac{x_{21}[\cos(D_3\pi) - 1]}{\pi L_{\mathrm{S3}}} - \frac{rx_{13} + x_{15} + x_{\mathrm{b3}}}{L_{\mathrm{S3}}} - \omega x_{12} \tag{4.27b}$$

$$\dot{x_{14}} = \frac{1}{C_{\mathrm{S3}}} x_{12} + \omega x_{15} \tag{4.27c}$$

$$\dot{x_{15}} = \frac{1}{C_{\mathrm{S3}}} x_{13} - \omega x_{14} \tag{4.27d}$$

$$\dot{x_{21}} = -\frac{(4\sqrt{x_{12}^2 + x_{13}^2} - 2x_{16}C'_{\mathrm{P3}}\omega)}{\pi} \frac{x_{16}}{x_{21}} \frac{1}{C_{\mathrm{DL3}}} \tag{4.27e}$$

$$x_{\mathrm{a3}} = \frac{1}{\pi C'_{\mathrm{P3}}\omega}(x_{12}\sin(\psi_3)^2 + x_{13}\mu_3) \tag{4.27f}$$

$$x_{\mathrm{b3}} = \frac{1}{\pi C'_{\mathrm{P3}}\omega}(x_{13}\sin(\psi_3)^2 - x_{12}\mu_3) \tag{4.27g}$$

$$\cos\psi_3 = 1 - \frac{x_{16}C'_{\mathrm{P3}}\omega}{\sqrt{x_{12}^2 + x_{13}^2}} \tag{4.27h}$$

$$\mu_3 = \psi_3 - \sin(\psi_3)\cos(\psi_3) \tag{4.27i}$$

$$\dot{x_{17}} = \frac{x_{22}\sin(D_4\pi)}{\pi L_{\mathrm{S4}}} - \frac{rx_{17}+x_{19}+x_{\mathrm{a4}}}{L_{\mathrm{S4}}} + \omega x_{18} \tag{4.28a}$$

$$\dot{x_{18}} = \frac{x_{22}[\cos(D_4\pi)-1]}{\pi L_{\mathrm{S4}}} - \frac{rx_{18}+x_{20}+x_{\mathrm{b4}}}{L_{\mathrm{S4}}} - \omega x_{17} \tag{4.28b}$$

$$\dot{x_{19}} = \frac{1}{C_{\mathrm{S4}}} x_{17} + \omega x_{20} \tag{4.28c}$$

$$\dot{x_{20}} = \frac{1}{C_{\mathrm{S4}}} x_{18} - \omega x_{19} \tag{4.28d}$$

$$\dot{x_{22}} = -\frac{(4\sqrt{x_{17}^2 + x_{18}^2} - 2x_{16}C'_{\mathrm{P4}}\omega)}{\pi} \frac{x_{16}}{x_{22}} \frac{1}{C_{\mathrm{DL4}}} \tag{4.28e}$$

$$x_{\mathrm{a4}} = \frac{1}{\pi C'_{\mathrm{P4}}\omega}(x_{17}\sin(\psi_4)^2 + x_{18}\mu_4) \tag{4.28f}$$

$$x_{\mathrm{b4}} = \frac{1}{\pi C'_{\mathrm{P4}}\omega}(x_{18}\sin(\psi_4)^2 - x_{17}\mu_4) \tag{4.28g}$$

$$\cos\psi_4 = 1 - \frac{x_{16}C'_{\mathrm{P4}}\omega}{\sqrt{x_{17}^2 + x_{18}^2}} \tag{4.28h}$$

$$\mu_4 = \psi_4 - \sin_2(\psi_4)\cos(\psi_4) \tag{4.28i}$$

4.1.7 Appendix B

The derivation of the transfer functions of an IPOS system consisting of 4 SPRC-Bm with variable and fixed input voltage, $G_2(s), G_3(s)$ and $G_1(s)$, used for the controller design, is given in the following. After the linearization of the equations in appendix A around a chosen operation point, given in Tab. 4.5 and by reintroducing the linearized state space equations from (4.9)

$$\begin{aligned} \Delta\dot{x} =& \mathbf{A}\Delta x + \mathbf{B}\Delta u \\ \Delta y =& \mathbf{C}\Delta x + \mathbf{D}\Delta u \end{aligned} \tag{4.29}$$

the state vector Δx and the input vector Δu for an ISOP system with fixed input voltage are given as

$$\Delta x_{\text{ISOP,fix}} = \begin{bmatrix} \Delta x_1 \, \Delta x_2 \, \Delta x_3 \, \Delta x_4 \, \Delta x_5 \, \Delta x_6 \, \Delta x_7 \, \Delta x_8 \, \Delta x_9 \end{bmatrix}^T$$

$$\Delta u_{\text{ISOP,fix}} = \begin{bmatrix} \Delta D \\ \Delta\omega \\ \Delta V_{\text{DL}} \\ \Delta D_2 \\ \Delta\omega_2 \\ \Delta V_{\text{DL2}} \end{bmatrix}.$$

The system matrix $\mathbf{A}$ and the input matrix $\mathbf{B}$ are derived as

$$\mathbf{A}_{\text{ISOP,fix}} = \begin{bmatrix} a_{11} & a_{12} & a_{13} & 0 & a_{15} & 0 & 0 & 0 & 0 \\ a_{21} & a_{22} & 0 & a_{24} & a_{25} & 0 & 0 & 0 & 0 \\ a_{31} & 0 & 0 & a_{34} & 0 & 0 & 0 & 0 & 0 \\ 0 & a_{42} & a_{43} & 0 & 0 & 0 & 0 & 0 & 0 \\ a_{51} & a_{52} & 0 & 0 & a_{55} & a_{56} & a_{57} & 0 & 0 \\ 0 & 0 & 0 & 0 & a_{65} & a_{66} & a_{67} & a_{68} & 0 \\ 0 & 0 & 0 & 0 & a_{75} & a_{76} & a_{77} & 0 & a_{79} \\ 0 & 0 & 0 & 0 & 0 & a_{86} & 0 & 0 & a_{89} \\ 0 & 0 & 0 & 0 & 0 & 0 & a_{97} & a_{98} & 0 \end{bmatrix}$$

$$\mathbf{B}_{\mathrm{ISOP,fix}} = \begin{bmatrix} b_{11} & b_{12} & b_{13} & 0 & 0 & 0 \\ b_{21} & b_{22} & b_{23} & 0 & 0 & 0 \\ 0 & b_{32} & 0 & 0 & 0 & 0 \\ 0 & b_{42} & 0 & 0 & 0 & 0 \\ 0 & b_{52} & 0 & 0 & b_{55} & 0 \\ 0 & 0 & 0 & b_{64} & b_{65} & b_{66} \\ 0 & 0 & 0 & b_{74} & b_{75} & b_{76} \\ 0 & 0 & 0 & 0 & b_{85} & 0 \\ 0 & 0 & 0 & 0 & b_{95} & 0 \end{bmatrix}.$$

It is assumed that all four SPRC-Bms have the same component values, therefore $a_{11}=a_{66}$, $a_{12}=a_{67}$, $a_{13}=a_{68}$, $a_{15}=a_{65}$, $a_{21}=a_{76}$, $a_{22}=a_{77}$, $a_{24}=a_{79}$, $a_{25}=a_{75}$, $a_{31}=a_{86}$, $a_{34}=a_{89}$, $a_{42}=a_{97}$, $a_{43}=a_{98}$, $a_{51}=a_{56}$, $a_{52}=a_{57}$ and a_{55} is the coupling coefficient between both SPRC-Bms in the ISOP system. Also, $b_{11}=b_{64}$, $b_{12}=b_{65}$, $b_{13}=b_{66}$, $b_{21}=b_{74}$, $b_{22}=b_{75}$, $b_{23}=b_{76}$, $b_{32}=b_{85}$, $b_{42}=b_{95}$ and $b_{52}=b_{55}$.
The coefficients for the system matrix **A** are given below and the subindex $_0$ signals the corresponding operation point magnitude of the state and input variables.

$$Z_1 = \sqrt{-\frac{x_{05} C_{\mathrm{P}} \omega_0 Z_3}{Z_5^{3/2}}} \tag{4.30}$$

$$Z_2 = Z_1 \omega_0 x_{05} x_{01} (-C_{\mathrm{P}} Z_5^{3/2} \omega_0 x_{05} + Z_5^2) \tag{4.31}$$

$$Z_3 = x_{05} C_{\mathrm{P}} \omega_0 \sqrt{Z_5} - 2 Z_5 \tag{4.32}$$

$$Z_4 = \frac{\pi}{2} - \arcsin\left(-1 + \frac{x_{05} C_{\mathrm{P}} \omega_0}{\sqrt{Z_5}}\right) \tag{4.33}$$

$$Z_5 = x_{01}^2 + x_{02}^2 \tag{4.34}$$

$$Z_6 = \frac{Z_2}{L_{\mathrm{S}} \pi C_{\mathrm{P}} \omega_0^2 Z_5^3 x_{05} Z_3} - 2 \frac{x_{01} Z_1}{L_{\mathrm{S}} \pi C_{\mathrm{P}} \omega_0 Z_5^2} \tag{4.35}$$

$$Z_7 = \frac{x_{05} x_{01}}{L_{\mathrm{S}} \pi Z_5^{5/2} Z_1} - 2 \frac{x_{01} Z_4}{L_{\mathrm{S}} \pi C_{\mathrm{P}} \omega_0 Z_5^2} \tag{4.36}$$

$$\begin{aligned} Z_8 = &- \omega_0 Z_1 (-C_{\mathrm{P}} Z_5^{3/2} \omega_0 x_{05} Z_5 + x_{01}^6 + x_{02}^6 + \\ &+ 3 Z_5 x_{01}^2 x_{02}^2) \end{aligned} \tag{4.37}$$

$$Z_9 = -\frac{x_{05}}{L_{\mathrm{S}} \pi \omega_0 {Z_5}^{3/2} Z_1} - \frac{Z_4}{L_{\mathrm{S}} \pi C_{\mathrm{P}} {\omega_0}^2 Z_5} \tag{4.38}$$

Table 4.5: Component values and operation points of the SPRC Bms of an IPOS system with fixed and variable input voltage, used for the linearization.

Bm1	Bm2	Bm3	Bm4		
Component and operation point input values					
L_{S}	L_{S2}	L_{S3}	L_{S4}	(μH)	4.199
C_{S}	C_{S2}	C_{S3}	C_{S4}	(nF)	840
C'_{P}	C'_{P2}	C'_{P3}	C'_{P4}	(μF)	1.696
r	r	r	r	(Ω)	0.01
C'_{f}		C'_{f2}		(μF)	8
R'_{L}				(Ω)	2.875
C_{DL1}	C_{DL2}	C_{DL3}	C_{DL4}	(mF)	30
ω_0	ω_{02}	ω_{03}	ω_{04}	(krad/s)	$2 \cdot \pi \cdot 106$
D_0	D_{02}	D_{03}	D_{04}	(−)	0.8
Operation point magnitudes of a system with fixed input voltage					
V_{DL0}	V_{DL02}	V_{DL03}	V_{DL04}	(V)	400
x_{01}	x_{06}	x_{012}	x_{017}	(A)	−324.11
x_{02}	x_{07}	x_{013}	x_{018}	(A)	−422.94
x_{03}	x_{08}	x_{014}	x_{019}	(V)	−755.98
x_{04}	x_{09}	x_{015}	x_{020}	(V)	579.33
x_{05}		x_{016}		(V)	635.88
Operation point magnitudes of a system with variable input voltage					
x_{010}	x_{011}	x_{021}	x_{022}	(V)	380.15
x_{01}	x_{06}	x_{012}	x_{017}	(A)	−308.29
x_{02}	x_{07}	x_{013}	x_{018}	(A)	−402.01
x_{03}	x_{08}	x_{014}	x_{019}	(V)	−718.59
x_{04}	x_{09}	x_{015}	x_{020}	(V)	551.08
x_{05}		x_{016}		(V)	604.65

$$Z_{10} = \frac{Z_8 \frac{x_{05}}{w_0}}{L_{\mathrm{S}} \pi C_{\mathrm{P}} {\omega_0}^2 {Z_5}^3 x_{05} Z_3} - \frac{Z_1}{L_{\mathrm{S}} \pi C_{\mathrm{P}} {\omega_0}^2 Z_5} \tag{4.39}$$

$$a_{11} = \frac{2x_{05}}{L_S\pi\sqrt{Z_5}}\left(\frac{x_{01}^2}{Z_5}-1\right)+\frac{C_P\omega_0 x_{05}^2}{Z_5 L_S\pi}\left(1-\frac{2x_{01}^2}{Z_5}\right)+ \\ -\frac{r}{L_S}+\frac{Z_2 x_{02}}{L_S\pi Z_5^2\omega_0 Z_3}\left(-\frac{1}{\sqrt{Z_5}}+\frac{1}{C_P\omega_0 x_{05}}\right)+ \\ +\frac{x_{02}x_{05}x_{01}}{L_S\pi {Z_5}^{3/2}}\left(Z_1+\frac{1}{Z_1}\right) \tag{4.40}$$

$$a_{12} = \frac{x_{05}}{L_S\pi Z_5^{3/2}}\Bigg[2x_{02}x_{01}-Z_1Z_5+ \\ +x_{02}^2\left(\frac{1}{Z_1}+Z_1-2\frac{C_P\omega_0 x_{01}x_{05}}{\sqrt{Z_5}x_{02}}\right)\Bigg]+\frac{-\pi+Z_1+Z_4}{L_S C_P\pi\omega_0}+ \\ +\omega_0+\frac{Z_2\frac{x_{02}^2}{x_{01}}\left(\sqrt{Z_5}-C_P\omega_0 x_{05}\right)}{L_S\pi C_P\omega_0^2 Z_5^{5/2}x_{05}Z_3} \tag{4.41}$$

$$a_{13} = a_{24} = \frac{-1}{L_S} \tag{4.42}$$

$$a_{15} = \frac{C_P\omega_0 x_{01}x_{05}}{0.5L_S\pi Z_5}-\frac{2x_{01}+x_{02}Z_1+\frac{x_{02}}{Z_1}}{L_S\pi\sqrt{Z_5}}+ \\ +\frac{x_{02}Z_8(\sqrt{Z_5}-x_{05}\omega_0 C_P)}{L_S\pi C_P\omega_0^2 Z_5^{5/2}x_{05}Z_3} \tag{4.43}$$

$$a_{21} = \frac{-C_P\omega_0 x_{01}x_{05}^2x_{02}}{0.5L_S\pi Z_5^2}-x_{01}Z_5(Z_6+Z_7)-\omega_0+ \\ +\frac{x_{01}^2x_{05}\left(\frac{2x_{02}}{x_{01}}-Z_1\right)}{L_S\pi Z_5^{3/2}}+\frac{Z_1x_{05}}{L_S\pi\sqrt{Z_5}}+\frac{Z_2x_{01}}{L_S\pi Z_5^{5/2}\omega_0 Z_3}+ \\ +\frac{(\pi-Z_4-Z_1)(Z_5+2x_{01}^2)-2\pi x_{01}^2}{L_S\pi C_P\omega_0 Z_5} \tag{4.44}$$

$$a_{22} = \frac{x_{05}^2C_P\omega_0}{L_S\pi Z_5}\left(1-\frac{2x_{02}^2}{Z_5}\right)-x_{02}Z_5(Z_6+Z_7)+ \\ +\frac{Z_3x_{02}}{L_S\pi Z_5^{5/2}\omega_0 Z_3}+\frac{x_{05}(2x_{02}^2-x_{02}Z_1x_{01}-2Z_5)}{L_S\pi Z_5^{3/2}}+ \\ -\frac{2x_{02}x_{01}(Z_1+Z_4)}{L_S C_P\pi\omega_0 Z_5}-\frac{r}{L_S} \tag{4.45}$$

$$a_{25} = \frac{Z_1 x_{01} + \frac{x_{01}}{Z_1} - 2x_{02}}{L_S \pi \sqrt{Z_5}} - \frac{Z_8 x_{01}(Z_5 - \omega_0 C_P \sqrt{Z_5} x_{05})}{L_S \pi C_P \omega_0^2 Z_5^3 x_{05} Z_3} + \\ + \frac{C_P \omega_0 x_{02} x_{05}}{0.5 L_S \pi Z_5} \tag{4.46}$$

$$a_{31} = a_{42} = \frac{1}{C_S} \tag{4.47}$$

$$a_{34} = -a_{43} = \omega_0 \tag{4.48}$$

$$a_{51} = \frac{4x_{01}}{C_f \sqrt{Z_5} \pi} \tag{4.49}$$

$$a_{52} = \frac{4x_{02}}{C_f \sqrt{Z_5} \pi} \tag{4.50}$$

$$a_{55} = \frac{1}{C_f} \left(-\frac{1}{R_L} - 2\frac{C_P \omega_0}{\pi} - 2\frac{C_{P2} \omega_{02}}{\pi} \right) \tag{4.51}$$

Next, the coefficients for the input matrix **B** are given below.

$$b_{11} = \frac{V_{DL0} \cos(D_0 \pi)}{L_S} \tag{4.52}$$

$$b_{12} = \frac{C_P x_{01} x_{05}^2}{L_S \pi Z_5} - \frac{x_{02} Z_8 (\omega_0 x_{05} C_P - \sqrt{Z_5})}{L_S \pi C_P Z_5^{5/2} \omega_0^3 Z_3} + \\ + \frac{x_{02}(\pi - Z_4 - Z_1)}{L_S \pi C_P \omega_0^2} - \frac{x_{02} x_{05}}{L_S \pi \omega_0 \sqrt{Z_5} Z_1} + x_{02} \tag{4.53}$$

$$b_{13} = \frac{\sin(D_0 \pi)}{L_S \pi} \tag{4.54}$$

$$b_{21} = -\frac{V_{DL0} \sin(D_0 \pi)}{L_S} \tag{4.55}$$

$$b_{22} = \frac{C_P x_{02} x_{05}^2}{L_S \pi Z_5} - x_{01} Z_5 (Z_9 + Z_{10}) - x_{01} + \\ + \frac{Z_8 x_{05} x_{01}}{L_S \pi Z_5^{5/2} \omega_0^2 Z_3} - \frac{x_{01}}{L_S C_P \omega_0^2} \tag{4.56}$$

$$b_{23} = \frac{\cos(D_0 \pi) - 1}{L_S \pi} \tag{4.57}$$

$$b_{32} = x_{04} \tag{4.58}$$

$$b_{42} = -x_{03} \tag{4.59}$$

$$b_{52} = -\frac{2x_{05}C_{\mathrm{P}}}{C_{\mathrm{f}}\pi} \tag{4.60}$$

For an ISOP system with variable input voltage the state and the input vector are written as

$$\Delta x_{\mathrm{ISOP,var}} = \begin{bmatrix} [\Delta x_{\mathrm{ISOP,fix}}]^T & \Delta x_{10} & \Delta x_{11} \end{bmatrix}^T$$

$$\Delta u_{\mathrm{ISOP,var}} = \begin{bmatrix} \Delta D \\ \Delta\omega \\ \Delta D_2 \\ \Delta\omega_2 \end{bmatrix},$$

where the input vector $\Delta x_{\mathrm{ISOP,var}}$ is composed of $\Delta x_{\mathrm{ISOP,fix}}$ and the variable input voltages Δx_{10} and Δx_{11}. The input vector $\Delta u_{\mathrm{ISOP,var}}$ is reduced to four inputs. Also the system matrix $\mathbf{A}_{\mathrm{ISOP,var}}$ contains $\mathbf{A}_{\mathrm{ISOP,fix}}$ with identical ceofficients and is derived as

$$\mathbf{A}_{\mathrm{ISOP,var}} = \begin{bmatrix} \begin{bmatrix} & & & & & & & & & \\ & & & & & & & & & \\ & & & & & & & & & \\ & & & & & & & & & \\ & & & & \mathbf{A}_{\mathrm{ISOP,fix}} & & & & & \\ & & & & & & & & & \\ & & & & & & & & & \\ & & & & & & & & & \\ & & & & & & & & & \end{bmatrix} & \begin{matrix} a_{110} & 0 \\ a_{210} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & a_{611} \\ 0 & a_{711} \\ 0 & 0 \\ 0 & 0 \end{matrix} \\ \begin{matrix} a_{101} & a_{102} & 0 & 0 & a_{105} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & a_{115} & a_{116} & a_{117} & 0 & 0 \end{matrix} & \begin{matrix} a_{1010} & 0 \\ 0 & a_{1111} \end{matrix} \end{bmatrix}.$$

The additional coefficients of $\mathbf{A}_{\mathrm{ISOP,var}}$ are

$$a_{101} = -4\frac{x_{01}x_{05}}{\sqrt{Z_5}\pi x_{010}C_{\mathrm{DL1}}} \tag{4.61}$$

$$a_{102} = -4\frac{x_{02}x_{05}}{\sqrt{Z_5}\pi x_{010}C_{\mathrm{DL1}}} \tag{4.62}$$

$$a_{105} = -4\frac{(\sqrt{Z_5} - x_{05}C_{\mathrm{P}}\omega_0)}{x_{010}C_{\mathrm{DL1}}\pi} \tag{4.63}$$

$$a_{1010} = -2\frac{\left(x_{05}C_{\mathrm{P}}\omega_0 - 2\sqrt{Z_5}\right)x_{05}}{\pi {x_{010}}^2 C_{\mathrm{DL1}}} \tag{4.64}$$

$$a_{110} = \frac{\sin(D_0\pi)}{L_{\mathrm{S}}\pi} \tag{4.65}$$

$$a_{210} = \frac{\cos(D_0\pi) - 1}{L_{\mathrm{S}}\pi} \tag{4.66}$$

with $a_{110} = a_{611}$, $a_{210} = a_{711}$, $a_{101} = a_{116}$, $a_{102} = a_{117}$, $a_{105} = a_{115}$ and $a_{1010} = a_{1111}$.
The input matrix $\mathbf{B}_{\mathrm{ISOP,var}}$ is given as

$$\mathbf{B}_{\mathrm{ISOP,var}} = \begin{bmatrix} b_{11} & b_{12} & 0 & 0 \\ b_{21} & b_{22} & 0 & 0 \\ 0 & b_{32} & 0 & 0 \\ 0 & b_{42} & 0 & 0 \\ 0 & b_{52} & 0 & b_{54} \\ 0 & 0 & b_{63} & b_{64} \\ 0 & 0 & b_{73} & b_{74} \\ 0 & 0 & 0 & b_{84} \\ 0 & 0 & 0 & b_{94} \\ 0 & b_{102} & 0 & 0 \\ 0 & 0 & 0 & b_{114} \end{bmatrix},$$

where the coefficients $b_{11}, b_{12}, b_{21}, b_{22}, b_{32}, b_{42}$ and b_{52} are the same as the coefficients of the matrix $\mathbf{B}_{\mathrm{ISOP,fix}}$, unless in b_{11} and b_{21}, V_{DL0} is replaced by x_{010}. Within the matrix $\mathbf{B}_{\mathrm{ISOP,var}}$, the coefficients are $b_{11} = b_{63}$, $b_{12} = b_{64}$, $b_{21} = b_{73}$, $b_{22} = b_{74}$, $b_{32} = b_{84}$, $b_{42} = b_{94}$, $b_{52} = b_{54}$ and $b_{102} = b_{114}$ with

$$b_{102} = \frac{2x_{05}^2 C_{\mathrm{P}}}{\pi x_{010} C_{\mathrm{DL1}}}. \tag{4.67}$$

Finally, the state space representation of the IPOS system either with fixed or variable input voltage is given with the state vector

$$\Delta x_{\mathrm{IPOS}} = \begin{bmatrix} [\Delta x_{\mathrm{ISOP1}}]^T & [\Delta x_{\mathrm{ISOP2}}]^T \end{bmatrix}^T$$

and the input vector

$$\Delta u_{\mathrm{IPOS}} = \begin{bmatrix} [\Delta u_{\mathrm{ISOP1}}]^T & [\Delta u_{\mathrm{ISOP2}}]^T \end{bmatrix}^T.$$

The state matrix $\mathbf{A}_{\mathrm{IPOS}}$ is formed by the two ISOP state matrices in the diagonal and the coefficients

$$a_{514} = -\frac{1}{C_{\mathrm{f}} R_{\mathrm{L}}} \tag{4.68}$$

and

$$a_{145} = -\frac{1}{C_{\mathrm{f2}} R_{\mathrm{L}}}, \tag{4.69}$$

if an ISOP with fixed input voltage is considered. If an ISOP with variable input voltage is considered, $a_{514} \rightarrow a_{516}$ and $a_{145} \rightarrow a_{165}$, calculated with (4.1.7) and (4.1.7). The rest of the matrix is filled with zeros. The coefficients a_{514}, a_{145}, a_{516} and a_{165} represent the series output connection of the ISOP systems.

$$\mathbf{A}_{\mathrm{IPOS}} = \begin{bmatrix} \begin{bmatrix} & & \\ & \mathbf{A}_{\mathrm{ISOP1}} & \\ & & \end{bmatrix} \begin{bmatrix} 0 & \cdots & 0 \\ \vdots & a_{514}, & \vdots \\ & a_{516} & \\ 0 & \cdots & 0 \end{bmatrix} \\ \begin{bmatrix} 0 & \cdots & 0 \\ \vdots & a_{145}, & \vdots \\ & a_{165} & \\ 0 & \cdots & 0 \end{bmatrix} \begin{bmatrix} & & \\ & \mathbf{A}_{\mathrm{ISOP2}} & \\ & & \end{bmatrix} \end{bmatrix}$$

The input matrix $\mathbf{B}_{\mathrm{IPOS}}$ is formed by the two ISOP input matrices in the diagonal and zeros elsewhere.

$$\mathbf{B}_{\mathrm{IPOS}} = \begin{bmatrix} \begin{bmatrix} \\ \mathbf{B}_{\mathrm{ISOP1}} \\ \end{bmatrix} & \begin{bmatrix} \\ \mathbf{0} \\ \end{bmatrix} \\ \begin{bmatrix} \\ \mathbf{0} \\ \end{bmatrix} & \begin{bmatrix} \\ \mathbf{B}_{\mathrm{ISOP2}} \\ \end{bmatrix} \end{bmatrix}$$

The output voltage and the RMS resonant currents are the output equations of the fixed input voltage ISOP system

$$y_{1,\text{fix}} = x_5 \cdot \ddot{u} = V_{\text{O1}} \cdot \ddot{u} \tag{4.70}$$

$$y_{2,\text{fix}} = \sqrt{2(x_1^2 + x_2^2} = I_{\text{res1,RMS}} \tag{4.71}$$

$$y_{3,\text{fix}} = \sqrt{2(x_6^2 + x_7^2} = I_{\text{res2,RMS}} \tag{4.72}$$

with $\ddot{u} = 20$, which is the transformers ratio. After the linearization of (4.1.7), (4.1.7) and (4.1.7), the output matrix $\mathbf{C_{IPOS,fix}}$ of the IPOS system is given as

$$\mathbf{C_{IPOS,fix}} = \left[\begin{bmatrix} 0 & 0 & 0 & 0 & \ddot{u} & 0 & 0 & 0 & 0 \\ c_{21} & c_{22} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & c_{36} & c_{37} & 0 & 0 \end{bmatrix}, \begin{bmatrix} 0 \\ \mathbf{3x9} \\ 0 \end{bmatrix} \right],$$

with the coefficients

$$c_{21} = \frac{\sqrt{2}x_{01}}{\sqrt{x_{01}^2 + x_{02}^2}} \tag{4.73}$$

$$c_{22} = \frac{\sqrt{2}x_{02}}{\sqrt{x_{01}^2 + x_{02}^2}}, \tag{4.74}$$

where $c_{36} = c_{21}$ and $c_{37} = c_{22}$, due to the same component values of all SPRC Bms. The output equations of the IPOS with variable input voltages are

$$y_{1,\text{var}} = x_{10} = V_{\text{DL1}} \tag{4.75}$$

$$y_{2,\text{var}} = x_{11} = V_{\text{DL2}}, \tag{4.76}$$

leading to the output matrix $\mathbf{C_{IPOS,var}}$ of the IPOS system

$$\mathbf{C_{IPOS,var}} = \left[\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \begin{bmatrix} \mathbf{0} \\ \mathbf{2x11} \end{bmatrix} \right].$$

Reintroducing

$$\begin{aligned} G_2(s) = &-G_{\text{Bm1},\Delta\text{VDL1}}(s) + G_{\text{Bm2},\Delta\text{VDL1}}(s) + \\ &+ G_{\text{Bm1},\Delta\text{VDL2}}(s) - G_{\text{Bm2},\Delta\text{VDL2}}(s) \end{aligned} \tag{4.77}$$

and using the state space equations of the varibale input voltage IPOS system the transfer functions forming $G_2(s)$ are derived as

$$G_{\mathrm{Bm1},\Delta\mathrm{VDL1}}(s) = \left.\frac{\Delta V_{\mathrm{DL1}}}{\Delta D}\right|_{\Delta\omega,\Delta D_2,\Delta\omega_2=0} \tag{4.78}$$

$$G_{\mathrm{Bm2},\Delta\mathrm{VDL1}}(s) = \left.\frac{\Delta V_{\mathrm{DL1}}}{\Delta D_2}\right|_{\Delta D,\Delta\omega,\Delta\omega_2=0} \tag{4.79}$$

$$G_{\mathrm{Bm1},\Delta\mathrm{VDL2}}(s) = \left.\frac{\Delta V_{\mathrm{DL2}}}{\Delta D}\right|_{\Delta\omega,\Delta D_2,\Delta\omega_2=0} \tag{4.80}$$

$$G_{\mathrm{Bm2},\Delta\mathrm{VDL2}}(s) = \left.\frac{\Delta V_{\mathrm{DL2}}}{\Delta D_2}\right|_{\Delta D,\Delta\omega,\Delta\omega_2=0} \tag{4.81}$$

Using the state space equations of the IPOS system with fixed input voltage the transfer functions forming $G_3(s)$

$$G_3(s) = G_{\mathrm{Bm1},\Delta\mathrm{VO1}}(s) + G_{\mathrm{Bm2},\Delta\mathrm{VO1}}(s) \tag{4.82}$$

and $G_1(s)$

$$\begin{aligned} G_1(s) = [&G_{\mathrm{Bm1},\Delta\mathrm{Ires1}}(s) + G_{\mathrm{Bm2},\Delta\mathrm{Ires1}}(s) + \\ &G_{\mathrm{Bm1},\Delta\mathrm{Ires2}}(s) + G_{\mathrm{Bm2},\Delta\mathrm{Ires2}}(s)] \cdot H_1, \end{aligned} \tag{4.83}$$

are given as

$$G_{\mathrm{Bm1},\Delta\mathrm{VO1}}(s) = \left.\frac{\Delta V_{\mathrm{O1}}}{\Delta D}\right|_{\Delta\omega,\Delta V_{\mathrm{DL1}},\Delta D_2,\Delta\omega_2,\Delta V_{\mathrm{DL2}}=0} \tag{4.84}$$

$$G_{\mathrm{Bm2},\Delta\mathrm{VO1}}(s) = \left.\frac{\Delta V_{\mathrm{O1}}}{\Delta D_2}\right|_{\Delta D,\Delta\omega,\Delta V_{\mathrm{DL1}},\Delta\omega_2,\Delta V_{\mathrm{DL2}}=0} \tag{4.85}$$

respectively

$$G_{\mathrm{Bm1},\Delta\mathrm{Ires1}}(s) = \left.\frac{\Delta I_{\mathrm{res1,RMS}}}{\Delta D}\right|_{\Delta\omega,\Delta V_{\mathrm{DL1}},\Delta D_2,\Delta\omega_2,\Delta V_{\mathrm{DL2}}=0} \tag{4.86}$$

$$G_{\mathrm{Bm2},\Delta\mathrm{Ires1}}(s) = \left.\frac{\Delta I_{\mathrm{res1,RMS}}}{\Delta D_2}\right|_{\Delta D,\Delta\omega,\Delta V_{\mathrm{DL1}},\Delta\omega_2,\Delta V_{\mathrm{DL2}}=0} \tag{4.87}$$

$$G_{\mathrm{Bm1},\Delta\mathrm{Ires2}}(s) = \left.\frac{\Delta I_{\mathrm{res2,RMS}}}{\Delta D}\right|_{\Delta\omega,\Delta V_G,\Delta D_2,\Delta\omega_2,\Delta V_{\mathrm{DL2}}=0} \tag{4.88}$$

Table 4.6: Nominator and denominator coefficients in s-domain of the transfer functions.

$G_1(s)$			
$Z(s)$		$N(s)$	
b_0	347.858141666217 E30	a_0	320.874817640644 E27
b_1	87.8086792032053 E27	a_1	99.7921833632613 E24
b_2	5.08050633578414 E24	a_2	8.26581530811099 E21
b_3	-94.1273080386993 E18	a_3	165.063231946826 E15
b_6	7.48114064263216 E12	a_4	1.35900330214233 E12
b_5	129.640460164061 E06	a_5	222.894213465120 E03
b_6	0	a_6	1
$G_2(s)$			
$Z(s)$		$N(s)$	
b_0	10.1212247856719 E27	a_0	3.79065890642367 E24
b_1	182.008775742464 E24	a_1	827.226019150503 E21
b_2	8.52047738455378 E21	a_2	13.6251584893958 E21
b_3	-1.06934095719994 E15	a_3	135.072774356601 E15
b_6	11.7186228653460 E09	a_4	1.37063207938328 E12
b_5	0	a_5	185.741250905273 E03
b_6	0	a_6	1
$G_3(s)$			
$Z(s)$		$N(s)$	
b_0	329.836149464061 E33	a_0	12.9421960277760 E30
b_1	23.0516073912384 E30	a_1	1.76733652416190 E27
b_2	421.040002120177 E24	a_2	43.7851209147386 E21
b_3	-34.4322590784590 E18	a_3	461.534766030359 E15
b_6	581.373641944023 E12	a_4	1.40764795593576 E12
b_5	292.448439615617 E03	a_5	441.215443874179 E03
b_6	0	a_6	1

$$G_{\mathrm{Bm2},\Delta\mathrm{Ires2}}(s) = \left.\frac{\Delta I_{\mathrm{res2,RMS}}}{\Delta D_2}\right|_{\Delta D,\Delta\omega,\Delta V_{\mathrm{DL1}},\Delta\omega_2,\Delta V_{\mathrm{DL2}}=0} \tag{4.89}$$

Finally, the coefficients used in

$$G(s) = \frac{Z(s)}{N(s)} = \frac{b_m s^m + b_{m-1}s^{m-1} + \ldots + b_1 s + b_0}{a_n s^n + a_{n-1}s^{n-1} + \ldots + a_1 s + a_0} \tag{4.90}$$

which forms the transfer functions $G_1(s)$, $G_2(s)$ and $G_3(s)$ are given as a balanced realization [160] in Tab. 4.6.

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5

Overall modulator system

In this chapter, the final overall design of the long pulse modulator is summarized and all built system components are presented and discussed. The modulator is operated under nominal load conditions and the thermal design is verified by a long term heat run test. A dynamic pulse performance evaluation is carried out based on pulse voltage measurements, regarding the pulse specifications, as e.g. rise time, fall time and the achieved flat-top ripple. Based on the measured steady state oil temperature, which is achieved from the long term heat run test, all critical temperatures of the HV-HF transformers are estimated. All critical temperatures stay well below the given limits. In addition, an efficiency evaluation of the complete modulator system, as well as the final achieved pulse efficiency is presented.

5.1 Journal I.: System Design and Measurements of a 115 kV/3.5 ms Solid State Long Pulse Modulator for the European Spallation Source

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Abstract

In this paper, the results of a 2.88 MW solid state long pulse modulator, which has been designed for the new linear collider at the european spallation source in Lund, are summarized. The presented modulator generates an output voltage pulse of 115 kV with a pulse length of 3.5 ms. The main components of the modular system, which include a series parallel resonance converter, a high voltage high frequency transformer and an output rectifier, are discussed. The modulator design is verified by measurements performed with a full scale prototype, which is operated under nominal load conditions. A detailed output voltage ripple evaluation is given and in addition, the system design has been proven by a 7 and 2/3 hours heat run test. All specifications are well within the given limits and the maximum occurring temperatures in the transformer stay below 110 °C even under worst case assumptions. The system achieves a pulse efficiency (determined by the pulse shape) of 96.78 %, an overall electrical system efficiency of 91.9 % and a combined pulse system efficiency of 89 %.

5.1.1 Introduction

For performing the planned high sophisticated material science experiments at the new linear collider at the European Spallation Source (ESS) in Lund, 2.88 MW long pulse modulators with a pulsed output voltage of 115 kV and pulse lengths in the range of milliseconds are required (see Tab. 5.1). Applying direct switched topologies, as e.g. the approachs presented in [6] and [4], for these modulators have the drawback that the pulse generating components (e.g. the solid state switch) have to be designed for the full pulse voltage. This drawback could

Table 5.1: Modulator specifications

Pulse specifications		
Pulse voltage	V_K	$-115\,kV$
Pulse current	I_K	$25\,A$
Pulse power	P_K	$2.88\,MW$
Pulse repetition rate	P_{RR}	$14\,Hz$
Pulse width	T_P	$3.5\,ms$
Pulse duty cycle	D	0.05
Efficiency specifications		
Pulse rise time (0..99 % of V_K)	t_{rise}	$150\,\mu s$
Pulse fall time (100..10 % of V_K)	t_{fall}	$150\,\mu s$
System efficiency	η_{sys}	$\geq 90\,\%$
Pulse voltage ripple frequency specifications		
$f < 300\,Hz$		1 % of V_K
$300\,Hz < f \leq 1\,kHz$		0.3 % of V_K
$1\,kHz < f \leq 100\,kHz$		0.1 % of V_K
$100\,kHz < f \leq 300\,kHz$		0.3 % of V_K
$f > 300\,kHz$		1 % of V_K

be avoided by using pulse transformers. However, pulse transformer based topologies (e.g. [41], [90]) require a huge transformer due to the high voltage time product caused by the large pulse length. In order to avoid the large transformers, series/parallel connected DC/DC converters switching at a high frequency resulting in a small voltage time product for the transformer can be used. Such DC/DC modules can be for example based on single active bridge converters with transformer and output rectifier as presented in [161], or on soft switched series parallel resonance converters (SPRC) as shown in Fig. 5.2 (b) and presented in [68], [162]. For generating the high output voltage, usually several modules are connected in series at the output. Due to the resonant tank, the SPRC has sinusoidal currents and voltages resulting in low EMI and allows ZVS for all switches, which is beneficial for MOSFETs and

enables high switching frequencies. Therefore, that topology is chosen for the considered modulator system. The SPRC topology consists of 18 SPRC-basic modules (SPRC-Bm) (see Fig. 5.2 (b)), which are operated at high switching frequencies (100 kHz - 110 kHz) to minimize the dimensions of the reactive components and the transformers. Further, to achieve the given pulse specifications in Tab. 5.1 an optimization procedure is used to design the components.
In this paper, a full scale prototype system and measurements of the output voltage pulse for the prototype system are presented. In section 5.1.2, first the optimization procedure required for determining the optimal design parameters is presented and all design results are summarized. Afterwards, the built prototype system is introduced in section 5.1.3 and the components of a SPRC-Bm are described. In section 5.1.4, the critical temperatures of the transformers are determined under the assumption of a worst case isolation oil temperature. Finally, the performance is evaluated by measured nominal output voltage pulses in section 5.1.5.

5.1.2 Optimization procedure

Due to the high number of degrees of freedom as for example the transformer geometry, number of turns or the number of parallel semiconductor devices/chip area, an optimization procedure, as depicted in Fig. 5.1, has been developed for optimally designing the modulator system. First, all electrical parameters as for example the primary current I_{prim} of the transformer, the transformer turns ratio N, the switching frequency f, the DC-link voltage V_{DL} or the output voltage of the transformer V_{sec} are determined with the electrical model of a single SPRC-Bm. These parameters in combination with the user defined constraints are used within the optimization loops to minimize the transformer volume and to optimize the number of parallel switches of the full bridge for minimal losses. In addition, the transformer leakage inductance L_σ and the stray capacitance C_{d} are determined with models given in [162], because L_σ is part of the resonant inductance L_{S} and C_{d} is part of the parallel capacitance C_{P}.
After the transformer optimization, a post isolation field conform design check of the transformer is performed with the help of FEM computations. This step is performed outside of the optimization loop because it is not possible to include a detailed model of the complex isolation

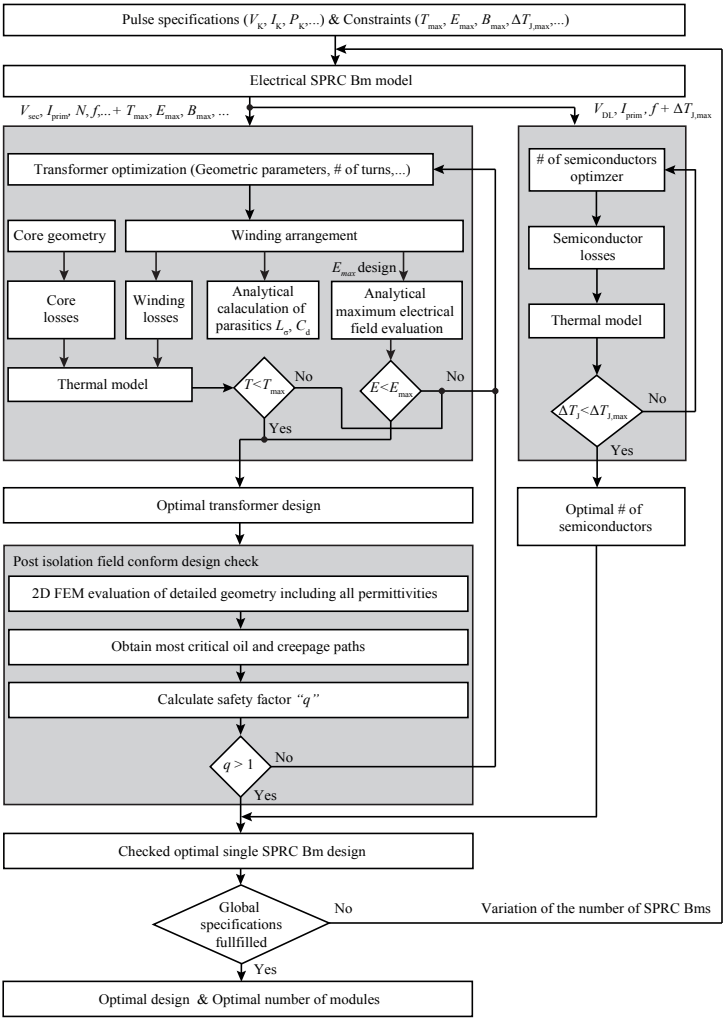

Figure 5.1: Developed optimization procedure of the full modulator system, which leads to an optimal design of a single SPRC-Bm and an optimal number of modules.

structure in the optimization routine without increasing the computational effort too much.

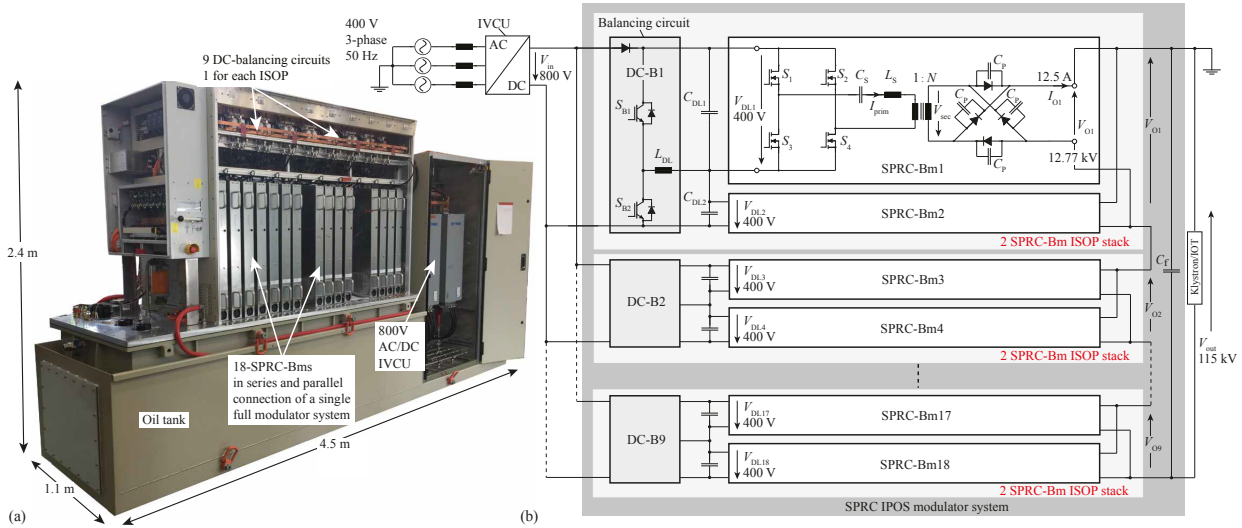

Figure 5.2: (a) Prototype system of the long pulse modulator (specifications see Tab. 5.1). The depicted setup includes two separate full modulator systems (2 x 18 SPRC-Bms in total) with a power of 2 x 2.88 MW during the pulse. (b) Block diagram of one full modulator system. There, two SPRC-Bms form an input series-output parallel (ISOP) connected stack and 9 of the ISOP stacks are connected in parallel at the input and in series at the output forming an IPOS system [163], [77]. To balance the input voltages, active balancing circuits (DC-Bi) are used. The modulator system is powered by the input voltage charging unit (IVCU), which is a PFC boost converter. The full modulator system has been built by AMPEGON AG.

The detailed description of the transformer optimization procedure is given in [104] and the applied thermal model of the semiconductor switches is presented in [68].
Finally, if all global specifications (see Tab. 5.1) are fulfilled, the procedure results in an optimal set of parameters and components of the SPRC-Bm and in an optimal number of modules for the modulator system. The optimization results for the considered specifications in Tab. 5.1 are summarized in Tab. 5.2.

5.1.3 Prototype system

Based on the optimization results, the prototype modulator system has been built and is presented together with the components of the single SPRC-Bm in the following.

5.1.3.1 Full modulator system

The modulator system and its basic block diagram are depicted in Fig. 5.2 (a) and (b). A single SPRC-Bm of the modulator consists of a MOSFET full bridge, a resonant tank, a transformer and an output rectifier as presented in [164] and depicted in Fig. 5.2 (b). Two SPRC-Bms with a 400 V DC-link voltage are connected in series at the input, sharing the same 800 V input voltage bus. At the output, the modules are connected in parallel, forming an input series output parallel stack (ISOP). To achieve the full output voltage and to deliver the full output power given in Tab. 5.1, nine of the ISOP stacks are connected in parallel at the input and in series at the output, forming an IPOS system (see Fig. 5.2 (b)).
Each ISOP system also contains an active balancing circuit (DC-Bi) [163], [77], which equalizes the DC-link voltage $V_{\mathrm{DL},i}$ at the input of the SPRC-Bm after each pulse. The active balancing circuit is shown in Fig. 5.3 (a) and (b). This circuit acts as a buck converter where V_{DL1} is the input voltage and V_{DL2} is the output voltage, in case $V_{\mathrm{DL1}} > V_{\mathrm{DL2}}$. In contrast, it acts as a buck converter with V_{DL2} as input voltage and with V_{DL1} as the output voltage if $V_{\mathrm{DL1}} < V_{\mathrm{DL2}}$. IGBTs are used for the buck converter because of the hard switching and the 800 V DC-link. To keep the control simple, the balancing circuit is operated at the fixed frequency f_{bal} and the fixed duty cycle D_{bal} in discontinuous conduction mode (DCM). All component values as e.g. the DC-link capacitor $C_{\mathrm{DL},i}$ and the buck inductance L_{DL} values are given in Tab. 5.3.

Table 5.2: Optimization results of a single SPRC-Bm and optimal number of modules.

Parameters and component values of a single SPRC-Bm					
V_{O1}	12.75 kV	L_S	4.199 µH	L_T	3.373 µH
I_{O1}	12.5 A	C_S	0.837 µF	$V_{DL,i}$	400 V
P_{O1}	160 kW	C_P	4.23 nF	f	100 kHz-110 kHz
# of turns for L_T			Type: HF-litz wire		
21			3 x 6390 x 0.071 mm		
# of capacitors for C_S			Type: SMD 2225		
896			C2225N153J102T		
# of capacitors for a single C_P			Type: SMD 2220		
216			C5750C0G2J104J280KC		
Semiconductors					
# of H-bridge switches			Type: MAX247		
4 x 6 = 24			STY139N65M5		
# of rectifier diodes			Type: SMD D^3PAK		
4 x 36 = 144			APT60DQ120SG		
Electric and magnetic parameters of the transformer					
V_{sec}	12.75 kV		E_{max}		< 12 kV/mm
I_{prim}	1200 A_{peak}		B_{max}		<= 200 mT
N	20		T_{max}		103.3 °C
L_σ	0.826 µH		C_d		69.3 pF
Transformer core					
Type:			Ferrite K2008 U126/20		
# of cores:			16		
Transformer windings					
Type:			HF-litz wire		
# of Primary Wdg. N_P	2		18 x 405 x 0.071 mm		
# of Secondary Wdg. N_S	40		1125 x 0.071 mm		
Overall system					
# of SPRC-Bms in parallel and series			2 x 9		

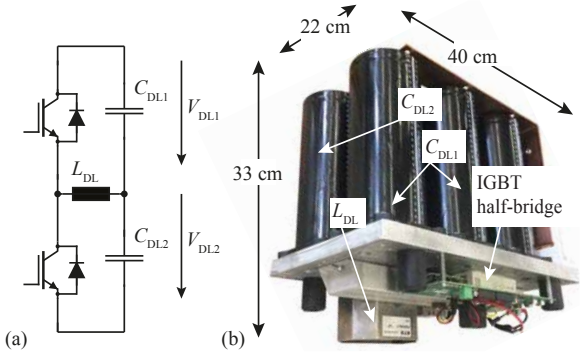

Figure 5.3: (a) Active input voltage balancing circuit operated with fixed switching frequency f_{bal} and fixed duty cycle D_{bal} in DCM. (b) Built balancing bridge.

Table 5.3: Parameters and component values of the active balancing circuit.

D_{bal}	0.3	f_{bal}	37 kHz
$C_{\mathrm{DL},i}$	3 x 10 mF = 30 mF	L_{DL}	220 µH
# of capacitors for $C_{\mathrm{DL},i}$		Type: Electrolytic	
3		Epcos B43455A5109M007	
# of IGBT half bridges		Type: Infineon module	
1		FF50R12RT4	

The input voltage charging unit (IVCU) is based on an industrial PFC boost converter [165] with an AC to DC efficiency $> 98\,\%$. It is connected to a standard three phase 400 V grid and provides the 800 V DC-link voltage V_{in} for the SPRC-Bms.
The voltage sharing between the SPRC-Bms could be balanced by the control presented in [163], [77]. The controller also performs a droop compensation for a constant pulse voltage, which compensates the input voltage droop due to the high power consumption during the pulse. Further details of the different control systems can be found in [163], [77].
In the following, the optimized components of a single SPRC-Bm are discussed.

5.1.3.2 Single SPRC-Bm components

The single SPRC-Bm (see Fig. 5.4 (a)) consists of a water cooled full bridge with 4 semiconductor switches each with 6 MOSFETs in parallel.
The required series inductance L_S is realized by the sum of the leakage inductance of the transformer L_σ and an external inductance L_T [162]. Due to the high switching frequency of 100 kHz to 110 kHz and the high resonant peak current of up to 1200 A_{peak}, an air toroid has been designed for the external inductance L_T in order to keep the losses low and to avoid saturation effects. The 21 turns winding is made of 3 parallel connected litz wires each with 6390 mm x 0.071 mm strands.
The series capacitance C_S is implemented by a single double layered printed circuit board with 896 series/parallel connected NP0 dielectric ceramic capacitors. The 896 capacitors have low losses, are stable over a wide range of temperatures and frequencies and also do not suffer from DC voltage derating.
The parallel capacitance C_P (see Fig. 5.4 (b) and (c)) is made of 216 series and parallel connected ceramic capacitors of the same type of capacitors as the series capacitance. The influence of the stray capacitance C_d of the transformer is not considered in the design of C_P, because it is negligible (see Tab. 5.2). The series/parallel connection of k component parts results in a low total tolerance $s(k) = s_1/\sqrt{k}$, where s_1 is the tolerance of each of the k-components. This is mandatory for parallel and series connected SPRC-Bm systems because the component tolerances are significantly influencing the transfer characteristic of the SPRC-Bms and could lead to unequal power sharing between the parallel connected SPRC-Bms [163], [77].
The output rectifier depicted in Fig. 5.4 (b) consists of 144 diodes in total, where one diode branch consists of 36 diodes. Each diode branch is made of 2 printed circuit boards due to the high output voltage. The schematic of the output rectifier is depicted in Fig. 5.4 (c) at the left side and has the same basic behavior as the standard rectifier circuit at the right side. In the left hand side circuit, the parallel capacitor C_P acts as resonant tank element, as a filter at the output of the rectifier, and it is additionally utilised to symmetrize the rectifier diodes voltages.
The high voltage and high frequency (HV-HF) transformer is shown in Fig. 5.4 (d). Litz wire is used for the primary and the secondary winding and ferrite as core material due to the high switching frequency. The

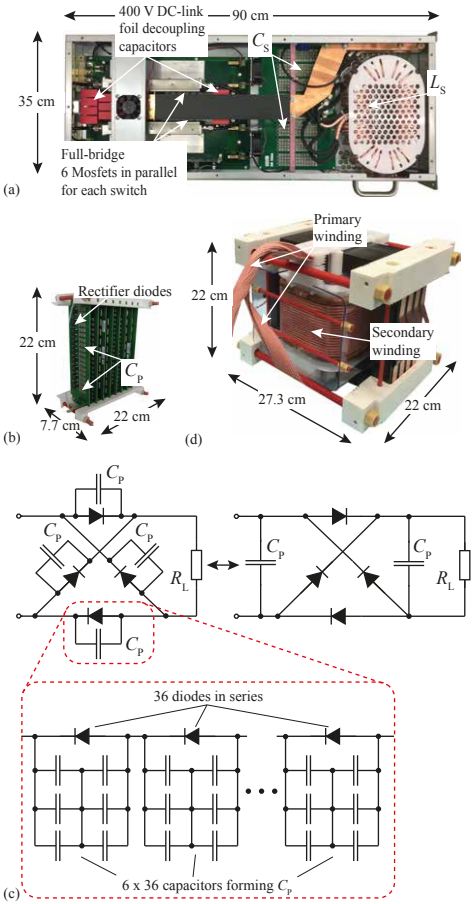

Figure 5.4: (a) Single SPRC-Bm consisting of the full bridge with 6 MOSFETs in parallel for each switch, the series capacitance C_S and the series inductance L_S. (b) Output voltage rectifier and parallel capacitance C_P. (c) Schematics of the output rectifier with identical input-to-output behaviour. The parallel capacitor C_P is additionally used for the voltage balancing of the rectifier diodes in the configuration on the left side compared to the standard circuit on the right side. One diode branch consists of 36 diodes in series with 6 capacitors in series and in parallel for each diode. (d) High voltage high frequency transformer.

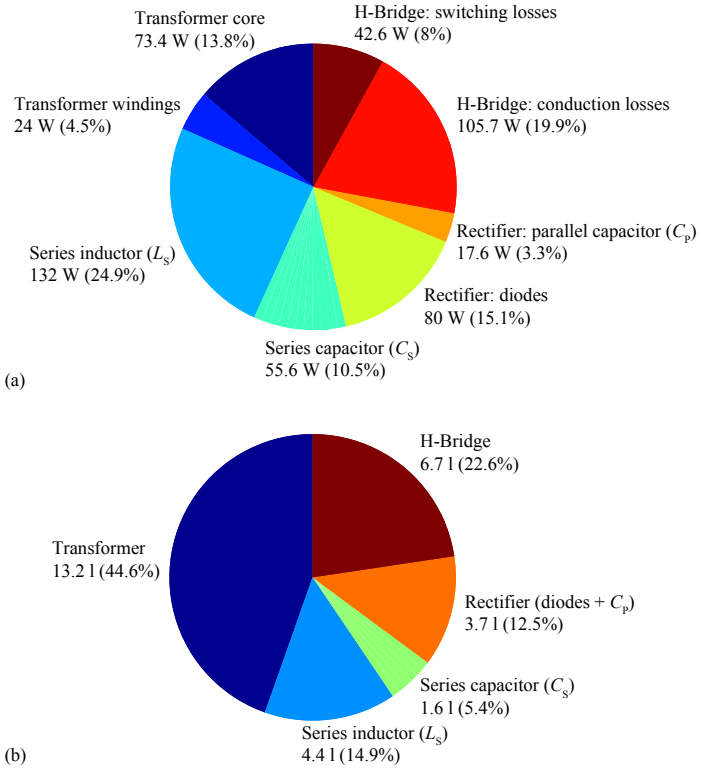

Figure 5.5: (a) Averaged loss distribution and (b) volume distribution of a single SPRC-Bm.

isolation of the transformer is designed with respect to the full output voltage of 115 kV due to the series connection of the SPRC-Bms. The turns ratio N of the transformer is $N_S : N_P = 20$. The detailed design of the HV-HF transformer is presented in [104].
Figure 5.5 (a) shows the loss distribution and Fig. 5.5 (b) shows the volume distribution of a single SPRC-Bm. The main losses are generated in the switches due to the high conduction losses caused by the high resonant current. Due to the high isolation voltage of 115 kV, the volume of the transformer is the largest one compared to the other module components, as can be seen in Fig. 5.5 (b).
In the following, a critical temperature evaluation of the transformer is

given.

5.1.4 Transformer temperature evaluation

Due to the required high isolation voltage of the transformer (115 kV) it is not possible to directly measure the critical temperatures inside the transformer during normal operation. Therefore, the critical transformer temperatures as for example the temperatures inside the core and at the surface of the core (T_1, T_4) and the temperatures inside the windings (T_2, T_3) are estimated with the validated thermal model given in Fig. 5.6, which is derived in [143], [52]. It includes the convective heat transfer from the core and/or the winding surfaces to the ambient ($R_{\text{c-amb}}$, $R_{\text{ws-amb}}$, $R_{\text{wp-amb}}$) and the conductive heat transfer inside the transformer, which is represented by the thermal resistors of the windings, the core and the bobbins (R_{ws}, R_{wp}, R_{cl}, $R_{\text{wp-ws}}$). The losses of the windings and the core are modelled by equivalent current sources (P_{cr}, P_{cl}, P_{wp}, P_{ws}). The model has been verified with measurements of the transformer temperatures, where the transformer has been operated at a reduced output voltage V_{sec} of 3.04 kV in air without isolation oil. The measurement system was a Flir ThermoVision A320 thermal camera [166] and the calculated temperature values have a maximal deviation of +12.5 % compared to the measured values as presented in [143].
By replacing the thermal parameters of air with the parameters of the isolation oil given in [167], all critical temperatures during normal operation can be determined with the model.

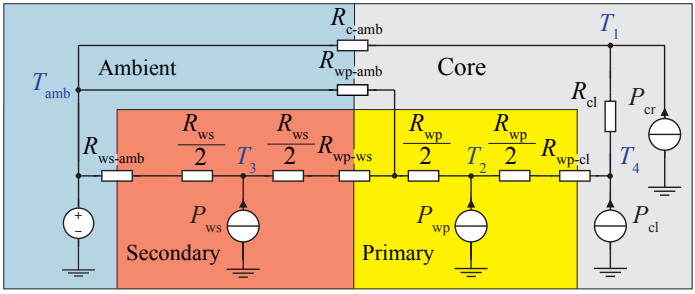

Figure 5.6: Simplified thermal equivalent circuit of the SPRC-Bm transformer, which is shown in Fig. 5.4 (d).

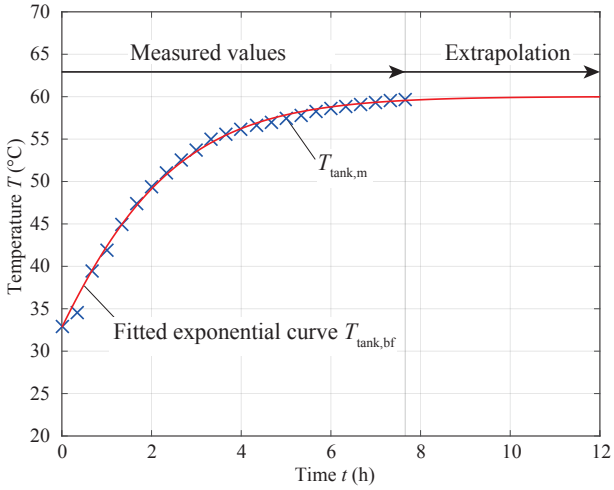

Figure 5.7: Measured oil temperature $T_{\text{tank,m}}$ inside the tank of Fig. 5.2 (a) and the exponentially fitted curve $T_{\text{tank,bf}}$, which is used for extrapolation until a stable temperature is reached.

In order to determine the ambient (oil) temperature T_{amb}, which is required for the thermal model, a PT1000 temperature sensor [168] is used inside the oil tank. The final oil temperature settles at approximately 60 °C after a heat run test of $7\frac{2}{3}$h, where both modulator systems from Fig. 5.2 (a) are dissipating the transformer and rectifier losses into the oil. The systems were operated with two separate water cooled resistive loads (2 x 4.6 kΩ) at nominal pulse conditions (see pulse specifications in Tab. 5.1). The oil is cooled by an oil to water heat exchange system with a water inlet temperature of 21.5 °C and a water outlet temperature of 27.9 °C. Figure 5.7 shows the measured oil temperature data $T_{\text{tank,m}}$, which is used for fitting to the exponential curve $T_{\text{tank,bf}}$ to estimate the steady state temperature of the oil. Table 5.4 shows the calculated temperatures of the transformer, the calculated thermal resistor values for the thermal model and the estimated losses of the windings and the core. A worst case ambient temperature of 65 °C (measured ambient temperature of 60 °C plus a margin of 5 °C) is used for the calculations. All critical temperatures are below 110 °C, which is the allowed maximal temperature.

Table 5.4: Operation point and temperatures of the test transformer

Averaged high frequency losses			
P_{wp}	13 W	P_{ws}	11 W
P_{cl}	22 W	P_{cr}	51.4 W
Lumped thermal resistors			
R_{wp}	0.5 K/W	$R_{\mathrm{wp\text{-}amb}}$	0.63 K/W
R_{ws}	0.9 K/W	$R_{\mathrm{ws\text{-}amb}}$	0.35 K/W
R_{cl}	2.82 K/W	$R_{\mathrm{c\text{-}amb}}$	0.21 K/W
$R_{\mathrm{wp\text{-}cl}}$	1.43 K/W	$R_{\mathrm{wp\text{-}ws}}$	2.585 K/W
Ambient (oil) temperature			
T_{amb}		65 °C	
Calculated temperatures			
T_1	71.7 °C	T_2	85.2 °C
T_3	75.08 °C	T_4	103.3 °C

5.1.5 Measurement results

In the following, the measured output voltage pulse is evaluated with regard to the pulse specifications given in Tab. 5.1.

5.1.5.1 Dynamic pulse perfomance

The modulator system is designed for a nominal output voltage of 115 kV. The switching frequency is starting at 103.93 kHz at the beginning of the pulse and is ending at 101.24 kHz in order to compensate the decreasing DC-link capacitor voltage. Figure 5.8 (a) shows a measured output voltage pulse, where V_{out} (blue line) is the output voltage and $V_{\mathrm{out,avg}}$ (green line) is the averaged voltage pulse, which is used for calculating the rise time t_{rise} and the fall time t_{fall}. The SPRC-Bms are working interleaved with an interleaving angle κ:

$$\kappa_{k,m} = \frac{(k-1)\pi}{K} + \frac{(m-1)\pi}{MK} \tag{5.1}$$

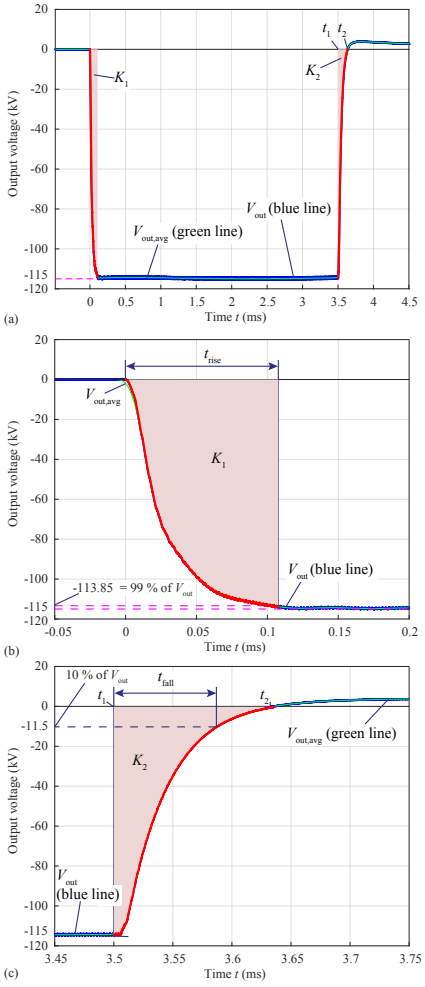

Figure 5.8: (a) Measured output voltage pulse V_{out} (blue line) and averaged output voltage pulse $V_{\text{out,avg}}$ (green line). (b) The zoomed view of the beginning of the pulse shows the achieved rise time $t_{\text{rise}} = 107.76\,\mu\text{s}$. (c) The zoomed view of the end of the pulse shows the achieved fall time $t_{\text{fall}} = 83.48\,\mu\text{s}$. The areas K_1 and K_2 represent the part of the transferred energy, which could not be used in the klystron load.

and

$$k = [1 \dots K], \quad m = [1 \dots M], \tag{5.2}$$

where each ISOP stack consists of $K = 2$ SPRC-Bms and $M = 9$ of this ISOP stacks are connected in series forming the IPOS system.
The rise time is $t_{\text{rise}} = 107.76\,\mu\text{s}$ (0..99 % of V_{K}) (see Fig. 5.8 (b)) and the fall time is $t_{\text{fall}} = 83.48\,\mu\text{s}$ (100..10 % of V_{K}) (see Fig. 5.8 (c)). Both times are well below the given limits in Tab. 5.1. The pulse efficiency η_{pulse} is the ratio between the ideal rectangular and the real pulse with limited rise and fall time [169]

$$\eta_{\text{pulse}} = \left(\frac{K_{\text{ideal}}}{K_{\text{real}}} \right) \cdot 100\,\% = 96.78\,\% \tag{5.3}$$

with

$$K_{\text{ideal}} = V_{\text{K}} \cdot (t_1 - t_{\text{rise}}) \tag{5.4}$$

$$K_{\text{real}} = \int_0^{t_2} V_{\text{out}} \mathrm{d}t \tag{5.5}$$

The areas K_1 (see Fig. 5.8 (b)) and K_2 (see Fig. 5.8 (c)) represent the part of the transferred energy, which is lost\cannot be used because the klystron load can just be initiated at a certain high voltage level [90]. After the pulse dynamics, the ripple of the output voltage pulse in Fig. 5.8 (a) is evaluated in the following.

5.1.5.2 Output voltage ripple evaluation

Figure 5.9 shows a zoomed region of the flat-top of the measured output voltage pulse of Fig. 5.8 (a). The blue part, which starts at t_{rise} and ends at t_1, is used for calculating the ripple spectrum and results in the lowest resolvable frequency component f_1 of 294.8 Hz with

$$f_1 = \frac{1}{t_1 - t_{\text{rise}}} \tag{5.6}$$

The measured data is sampled at a rate of 250 MS/s and has been processed with a moving average filter with a cutoff frequency of 104 kHz resulting in $V_{\text{out,avg}}$. This resulting averaged voltage gives a good indication for the low frequency ripple during the flat-top (see Fig. 5.9). The resulting output voltage ripple spectrum is depicted in Fig. 5.10. There, an overview is given for the full spectrum from 0 to 6 MHz

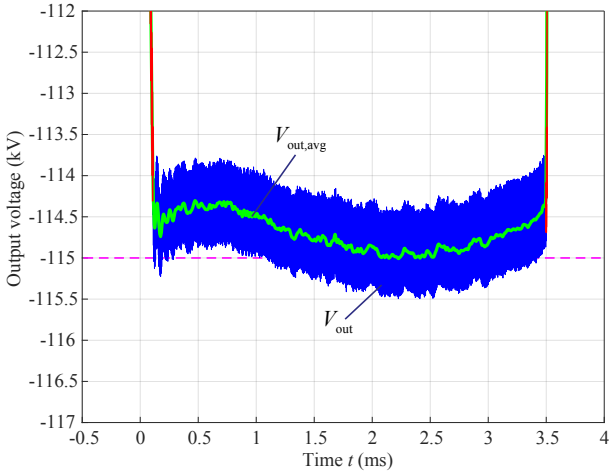

Figure 5.9: Zoom of the flat-top of the measured output voltage pulse V_{out} given in Fig. 5.8 (a). In addition, the measured averaged output voltage pulse $V_{\text{out,avg}}$ (green line) is shown. The blue part of the flat-top is used for determining the ripple spectrum.

(Fig. 5.10 (a)), from 0 to 1 MHz (Fig. 5.10 (b)) and for the low frequency range from 0 to 1 kHz (Fig. 5.10 (c)). It is clearly visible that all frequency components are well within the yellow area, which indicates the maximum allowed peak to peak ripple voltage for each frequency component (see Tab. 5.1). The main switching frequency is around 100 kHz and because of the full wave output rectifier, the main output voltage ripple frequency of a single SPRC-Bm is around 200 kHz. Despite the interleaving of all SPRC-Bms, also multiples of the 200 kHz appear in the spectrum below 9 x 200 kHz due to the component tolerances. Figure 5.11 shows the averaged loss distribution of the full modulator system including the losses of 18 SPRC-Bms, the IVCU and the pulse shape losses. The main losses occur in the SPRC-Bms, but also the non ideal pulse shape (see Fig. 5.8) results in about a third of the losses.

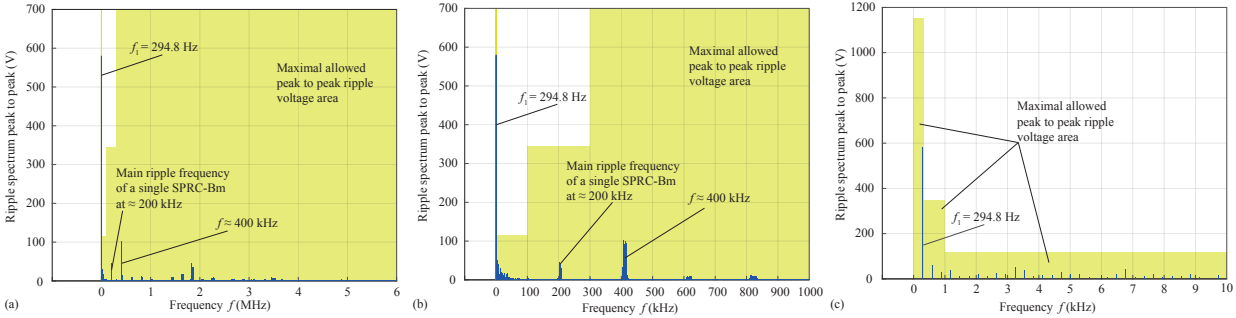

Figure 5.10: Ripple spectrum of the analyzed output voltage pulse in Fig. 5.9. (a) Full spectrum from 0 Hz to 6 MHz. (b) Zoomed view of the spectrum from 0 Hz to 1 MHz. (c) Zoomed view of the spectrum from 0 Hz to 10 kHz. The main ripple frequency of the output voltage of a single SPRC-Bm is around 200 kHz. The yellow area indicates the maximum allowed peak to peak ripple voltage for each frequency component, according to Tab. 5.1.

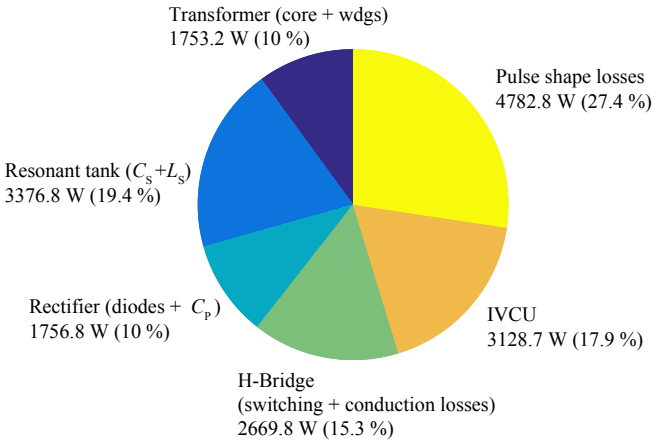

Figure 5.11: Averaged loss distribution of the full modulator system including the losses of 18 SPRC-Bms, the IVCU and the pulse shape losses. The resulting efficiencies are listed in Tab. 5.5.

Table 5.5: System efficiency

Single SPRC-Bm efficiency $\eta_{\text{SPRC-Bm}}$	93.75 %
Efficiency of the IVCU η_{IVCU}	98 %
Output voltage pulse parameters	
Pulse rise time t_{rise}	107.76 µs
Pulse fall time t_{fall}	83.48 µs
Pulse efficiency η_{pulse}	96.78 %
Overall system	
# of SPRC-Bms in parallel and series	2 x 9
Electrical system efficiency $\eta_{\text{elec,sys}} = \eta_{\text{SPRC-Bm}} \cdot \eta_{\text{IVCU}}$	91.9 %
Pulse system efficiency $\eta_{\text{pulse,sys}} = \eta_{\text{elec,sys}} \cdot \eta_{\text{pulse}}$	89 %

Table 5.5 lists the achieved system performance. The designed system easily fulfills the global pulse specifications from Tab. 5.1 and

achieves an electrical system efficiency $\eta_{\text{elec,sys}}$ of 91.9 % and a pulse system efficiency $\eta_{\text{pulse,sys}}$ of 89 %, which also considers the losses of the nonideal pulse shape. For the entire system 18 SPRC-Bm (2 x 9 units connected in parallel) are required.

5.1.6 Conclusion

In this paper, a long pulse modulator prototype system is presented and a detailed description of the measured pulse parameters is given. Two SPRC-Bms connected in series at the input and in parallel at the output forming an ISOP stack. To generate the given output voltage of 115 kV, nine of this ISOP stacks are connected in series. A detailed description of each SPRC-Bm component is presented. Due to the high operating frequency and the high resonant current, litz wire is used as winding material for the inductive components and six MOSFETs are connected in parallel, forming a switch in each sub module to keep the losses low. All critical temperatures of the transformer stay well below 110 °C, with an assumed worst case isolation oil temperature of 65 °C. The measured output voltage pulses are well within the given specification. The achieved rise time of 107.76 µs and the achieved fall time of 83.48 µs result in a pulse efficiency of 96.78 %, an overall electrical system efficiency of 91.9 % and a pulse system efficiency of 89 %, taking also the losses due to the non ideal pulse shape into account.

ACKNOWLEDGMENT

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6 Conclusion and Outlook

6.1 Conclusion

In this thesis, the design of a novel modular long pulse modulator system, which is capable to generate 115 kV voltage pulses with a pulse duration of 3.5 ms and a pulse repetition rate of 14 Hz is presented. The modulator system consists of 18 series parallel resonance converter basic modules, called SPRC-Bm in the following, which are operated interleaved to reduce the output pulse voltage ripple to a minimum.
After a detailed literature search for suitable topologies, the SPRC was identified as the most suitable approach. This topology allows for an isolated modular design, whereby parasitic elements of the transformer can be integrated directly in the resonant circuit and a natural short-circuit protection due to the series resonant inductance is given. The first part of this summary presents the modeling of an SPRC-Bm, while the second part describes the evolution of the overall system control.
With the help of an optimization algorithm, the components of a single module and the total number of individual modules required were determined with regard to the desired output power / voltage in terms of highest efficiency and smallest possible size. This algorithm is based on a multi-domain model of the SPRC, which is described in the following. An analytic electrical model consisting of the resonant circuit, the high-voltage high-frequency transformer and the output rectifier, delivers the required component values for the resonant circuit. All losses of the inverter, the rectifier, as well as all elements of the resonant circuit including core and eddy current losses, were integrated for a study regarding the efficiency.

In order to ensure proper maximum operating temperatures, an equivalent analytical thermal circuit of the high-voltage high-frequency transformer was created. This circuit includes a new analytical model for the determination of the thermal winding resistance consisting of litz or round wire and makes a comparison of different insulating and cooling media possible. The developed analytical models are verified by measurements with non-potted and epoxy-potted solid wire test setups and test setups for litz wire. The thermal equivalent circuit of the test transformer shows a good match between the measured and the predicted temperature distribution, whereas the error between the calculated and the measured temperatures is between 1.3 % and 12.5 %.
In a next step, a thermal evaluation of the full bridge switches was performed. For this evaluation, a transient thermal model of the semiconductor switches was developed. This model returns the temperature profile of the semiconductor junction layer, as well as important lifetime parameters. Based on these parameters, an estimate was made about the number of required components.
In order to consider the influence of the parasitic elements of the transformer in the optimization procedure, the calculation of the stray capacitance is implemented with the help of the mirror charge method, respectively the leakage inductance is calculated with the help of the mirror current method. Both transformer parasitics are verified with measurements. In addition, an isolation model of the transformer, which is also based on the mirror charge method, is created. Based on this model, the maximum field strengths inside and outside the core window can be calculated and thus the minimum insulation distances of the winding to the core and between the windings can be determined.
The resulting optimized components of a single SPRC-Bm were then fabricated, measured and validated with the existing models. In order to evaluate the insulation design of the transformer, it was additionally subjected to a high-voltage and partial discharge test.
In addition, an analytical description of the output voltage ripple for an arbitrary number of output series, output parallel or output parallel-output series connected SPRC-Bms, which are operated interleaved, is presented. The derived formulas can be used for ripple investigations due to component tolerances and optimal interleaving angles.
Two control strategies for an optimal power sharing, input and output voltage balancing, as well as a voltage droop compensation are presented for the overall system. In the first case, the input voltage

balancing is achieved with the help of an auxiliary circuit and the output voltage balancing by control of the resonant currents. The performance of the proposed controller is demonstrated with measurement results. Further, an input and output voltage balancing by control is presented and the performance could be demonstrated in simulations on the basis of a switched overall system taking into account component tolerances and different power consumption of the individual modules. For the determination of the control parameters in a first step, the nonlinear large-signal model of a single SPRC with variable input voltage was derived and compared with simulations. Afterwards, a basic non-linear large-signal model of the overall system was obtained. This developed basic non-linear large signal model allows an easy extension of the number of modules and can be investigated with any common circuit simulators. Based on the basic non-linear large-signal model a linear small-signal model was analytically derived, which provides all important parameters for a valid controller design. In addition, the effects of component tolerances between the individual SPRC modules were investigated and verified by measurements.
Finally, a full scale prototype has been manufactured, which is operated under nominal load conditions. The system design has been proven by a 7 and 2/3 hours heat run test, generating output voltage pulses of 115 kV with a pulse length of 3.5 ms and a repetition rate of 14 Hz. All critical temperatures of the transformer stay well below 110 °C, with an assumed worst case isolation oil temperature of 65 °C.
The measured output voltage pulses are well within the given specification of the allowed voltage ripple frequency spectrum, as well as the resulting rise and fall times are well below the allowed rise and fall times. The achieved rise time of 107.76 µs and the achieved fall time of 83.48 µs result in a pulse efficiency of 96.78 %, an overall electrical system efficiency of 91.9 % and a pulse system efficiency of 89 %, taking also the losses due to the non ideal pulse shape into account.

6.2 Outlook

In this thesis, a new concept for a long pulse modulator in the millisecond range with an output voltage of 115 kV and a pulsed output power of 2.88 MW has been developed. All required models for an optimized design were analytically derived and verified by prototype measurements. For future projects in the long pulse area, this work represents

a solid start point, where the analytical models, as well as the obtained experience with the full scale prototype system can be used to reduce development time and development costs to a minimum.
A reduction of the complexity of the modulator system could be achieved by using the now (2018) available MOSFET modules with a breakdown voltage of 1200 V, which were not available at 2013 for a reasonable price. The two parallel connected SPRC-Bms, which form an ISOP system, could be reduced to a single SPRC-Bm, which results in a reduction of modules by the factor of two and the input voltage balancing would be not necessary any more. A redesign of the H-bridge has to be performed, whereas the resonant tank, the high-voltage high-frequency transformer and the output rectifier would only need minor improvements.
A further interesting future topic may be the extension and the improvement of the presented thermal model for litz wire windings. This is still an ongoing important field of research, where a more accurate model would lead to a higher efficiency and more compact designs of transformers, inductors or electrical machines.

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