Fault Current Interruption in Multiterminal HVDC Networks

Digital Object Identifier: 10.1109/TPWRD.2015.2448761,

Fault Current Interruption in Multiterminal HVDC Networks

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***Abstract*—In a multiterminal HVDC network, dc circuit breakers are required at each end of a line to selectively isolate a fault. Several circuit breaker concepts have been implemented in PSCAD, which differ significantly in their structure and performance. This paper describes the interaction of the different HVDC circuit breaker topologies with a meshed four terminal network and assesses their performance in terms of maximum currents and voltages. The trade-off between network parameters and circuit breaker requirements is analyzed.**

***Index Terms*—HVDC Circuit Breaker, HVDC transmission, Power system transients, Power system faults, Power system simulation, PSCAD.**

I. Introduction

HVDC Circuit Breakers (CB) are widely considered as a key enabling technology for future multiterminal HVDC (MTDC) networks [1], which have been envisioned in various studies and projects from academia and industry. The availability of HVDC CBs will be critical for the reliability of these networks. Point-to-point HVDC connections can be adequately protected by conventional CBs on the ac side of the converter, even if this results in the de-energization of the entire dc system [2]. A real MTDC grid, however, requires dc CBs at each end of a line section to selectively isolate a fault by quickly and reliably breaking the fault current.

The interruption of an HVDC circuit requires generally the following [3]: a current zero has to be produced, the magnetic energy that is stored in the system inductance has to be dissipated, and sufficient dielectric strength has to be established to withstand the transient recovery voltage (TRV). The first and second requirement are fulfilled rather easily in ac systems given the natural current zero crossing. In dc systems, however, the CB has to produce the current zero itself. This can be done either by insertion of a counteracting voltage or by injection of a current with opposite polarity. For practical purposes, the interruption process has to be completed within a certain time and the resulting switching surge has to be within the insulation's withstand capability.

An HVDC CB has to be able to create a current zero, to dissipate the energy stored in the circuit, and to establish the dielectric strength. While dc CBs are available for low and medium voltage applications, only transfer and load current switches are in use in HVDC systems [1]. Numerous concepts for such an HVDC CB have been presented up to now in patents and articles, which all show a similar arrangement with a switching element in the nominal path to build the voltage withstand capability, a commutation path to create the current zero, and an absorber path to dissipate the stored energy. The main switching element can either be an arc between the contacts of a mechanical CB, a solid-state based semiconducting device or the combination of both. Each of the proposed CB concept has advantages and drawbacks either in on-state losses or speed [4].

The design of the HVDC CB has to be chosen according to the expected maximum fault current in a MTDC network, which depends on various factors. These prospective fault current influencing factors include among others: the dc capacitor size and fault resistance [5], the transmission line technology [6], the grounding scheme [7], and the layout of the MTDC network [8], [9].

It has been shown that the expected fault current exceeds the breaking capability of most of the proposed HVDC CB concepts or their construction costs are not economical. Therefore, the MTDC network design has to be adapted to the CBs capability and additional fault clearing support options have to be chosen as addressed in [4].

Recent publications either present detailed HVDC CB modeling concepts, but without specific implementation [10], or demonstrate their functionality based on simplified simulations with a single voltage source [11], or are applied with focus on the differences between HVDC system configurations in a radial MTDC grid [12]. The paper at hand aims to combine the transient network study in a meshed MTDC layout with detailed HVDC CB models to analyze the interaction between CB and network. Detailed simulations in EMTDC-PSCAD of the fault current interruption process are presented and the influence of the different components are analyzed based on parameter variations.

The modeling of four different HVDC CB concepts in PSCAD are presented and their performance is studied in a meshed four-terminal MTDC cable network during the current interruption process of a pole-to-ground fault. The influence of the CB itself, the network components, and the protection system properties on the maximum fault currents, as well as maximum and minimum voltages in the system are shown.

The considered CB concepts include the passive and active resonance CB, the solid-state based CB, as well as a hybrid CB concept. Results are presented for a cable systems, since cables yield higher fault current levels than overhead lines (OHL) [6]. Pole-to-ground faults are regarded as significantly more frequent compared to pole-to-pole faults [13], particularly lightning related faults in OHL systems, although the latter

Manuscript received November 3, 2014; revised Month xx, 2014; accepted Month xx, 2014. This work was financially supported by ABB Switzerland Ltd., Siemens AG, Alstom Grid, Swiss Federal Office of Energy (BfE), and CTI (SCCER-FURIES). Paper no. TPWRD-xxxxx-xxxx.

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fault would lead to more severe conditions [14].

II. Modeling of MTDC

The performance of the different HVDC CBs is tested in a meshed four-terminal MTDC network as shown in Fig. 1 using PSCAD simulations. The pole-to-ground fault occurs at a distance of $50\,\mathrm{km}$ to terminal 1 and $150\,\mathrm{km}$ to terminal 2. CBs are installed at all cable ends, but only CB1 and CB2 are tripped assuming differential relaying [15]. The chosen network layout and cable lengths result in higher fault currents in CB1 than in CB2 in order to demonstrate their different behavior.

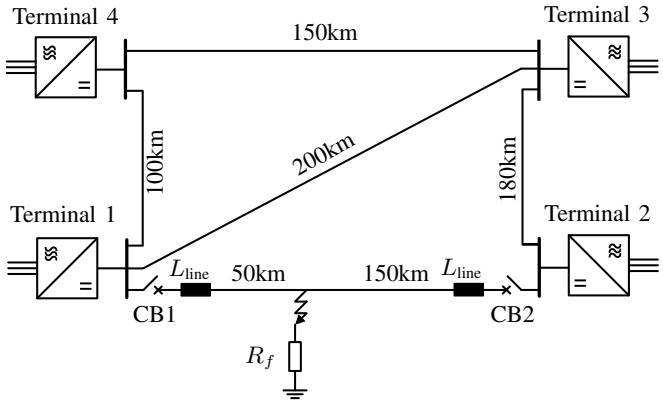

Fig. 1. MTDC network layout (CBs and inductors only shown for line 12)

A. Cable Model

The cross-section of the frequency-dependent, distributed-parameter cable model is derived from a real $150\,\mathrm{kV}$ XLPE VSC-HVDC submarine cable [16], [17]. The cross-section has been scaled up to a $320\,\mathrm{kV}$ cable respecting the diameter of the copper conductor [18], while keeping the electric field stress in cold condition similar. The same material properties and cable cross-section dimensions as in [5] are applied. The cable sheath is assumed to have ground potential over the whole cable length and is, therefore, mathematically eliminated in the simulations.

B. Converter Model

The converters are modeled as a generic $\pm 320\,\mathrm{kV}$ bipolar half-bridge VSC topology with concentrated midpoint-grounded dc capacitors C_{cap} at each terminal and line reactors L_{line} at each cable end in series to the CBs as illustrated in Fig. 2. The value of C_{cap} depends on the converter technology and can be zero in case of modular multilevel converter (MMC). The converter's local overcurrent protection blocks the IGBT modules above a threshold value of about twice the nominal current [19] to protect them from overcurrents making the half-bridge based VSC an uncontrolled rectifier [20]. Therefore, the converter model to be implemented for the transient period can be simplified to the diode rectifier shown in Fig. 2. No post-fault control strategy for the converters is implemented in the model and the tripped converters remain blocked throughout the simulation time. Equal ac network parameters are assumed at all terminals, so there is no power flow if all converters are blocked. This is a valid assumption, as only the transient period is of interest.

The ac network adjacent to the converter terminal is modeled by its equivalent short-circuit impedance consisting of R_{ac} and L_{ac}, and a voltage source V_{ac}. The converter transformer with reactance L_{t} has a grounded star point on the high voltage side and delta windings on the secondary side. An additional phase reactor L_{s} is installed between converter bridge and transformer for harmonic filtering of the ac currents. In an MMC, the phase reactor L_{s} represents the arm reactors.

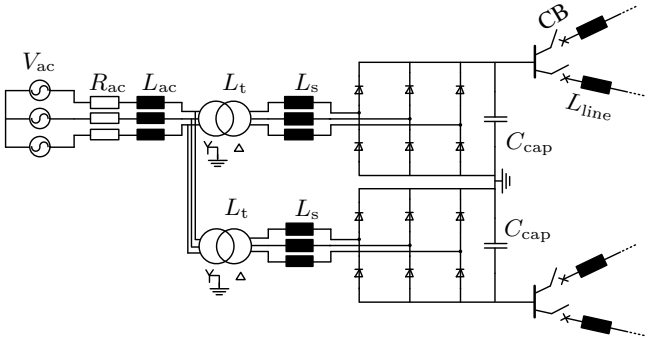

Fig. 2. Electrical equivalent scheme of the converter model with blocked IGBTs (V_{ac}: ac voltage, R_{ac}: ac resistance, L_{ac}: ac inductance, L_{t}: Transformer reactance, L_{s}: phase reactor, C_{cap}: dc capacitor, L_{line}: line reactor)

III. HVDC CB Concepts and Modeling

Four different HVDC CB concepts and their modeling in PSCAD will be presented in the following: the passive (P-RCB) and active resonance CB (A-RCB), the hybrid CB (HCB), and the full solid-state CB (SCB) concept.

A simple fault detection mechanism is implemented at CB1 and CB2 (cf. Fig. 1) with a level comparator to simulate differential protection [15] and selective opening of the CBs at the faulted line ends. All other CBs remain closed. A very optimistic detection delay $\Delta T_{\mathrm{detect}}$ of $1\,\mathrm{ms}$ [15] is chosen for all CB concepts. The detection delay is defined as the time from occurrence of the fault to sending the trip signal to the CB and accounts for all signal processing and communication delays as required in differential protection schemes [15].

A. P-RCB and A-RCB

The passive and active resonance CB as illustrated in Fig. 3 have a mechanical breaker in the nominal path, which is usually an ac air-blast CB [21] or an SF6 puffer CB [22] for the P-RCB and a vacuum CB [23] for the A-RCB. In the passive scheme, the components in the red boxes in Fig. 3 do not exist, whereas in the A-RCB, the capacitor C_{res} is pre-charged by closing "S_b" and the active current injection is initiated through closing of "S_a". Both auxiliary switches S_a and S_b are modelled as ideal switches.

The temporal development of the current and voltage during the interruption process in the P-RCB [21], [22], [24] is

illustrated in Fig. 4 with example curves for the current in the nominal path (red), in the commutation path (green), in the absorber path (cyan), the sum of all currents (blue), and the CB voltage (magenta). Note that the CB parameters in Fig. 4 are different from the ones presented in Section IV-A2 to improve the visibility of the oscillating currents.

After the current has exceeded the CB threshold at $0.6\,\mathrm{ms}$ and the differential protection system has given the trip signal selectively to the CB at $1.6\,\mathrm{ms}$, the CB is tripped and the drive starts to move the contacts. An optimistic estimate of $\Delta T_{\mathrm{opening}} = 4\,\mathrm{ms}$ is assumed for the delay between the trip signal and contact separation. The arc voltage forces the current to commutate into the commutation path, which consists of a resonance circuit with an inductance L_{res}, a capacitor C_{res}, and a parasitic resistance R_{res} as indicated in Fig. 3. After another $\Delta T_{\mathrm{nozzle}} = 5\,\mathrm{ms}$, the moving contact cleared the nozzle and the CB is able to clear the arc. Also the chosen $\Delta T_{\mathrm{nozzle}}$ is a an optimistic lower estimate for fast gas CBs. Once the nozzle is cleared, the arc has a negative V-I characteristic. Together with a sufficiently s mall parasitic resistance, the oscillations of the current in the commutation path start to grow at $10.6\,\mathrm{ms}$ (green curve in Fig. 4). This oscillating current is superimposed on the current through the nominal path (red), which results in a current zero crossing at around $29\,\mathrm{ms}$ and extinction of the arc. At that time, the total current (blue) is still high due to the stored energy in the system inductance and resonance inductor. After the arc extinction, the capacitor C_{res} is charged by the commutated current, until the threshold voltage of the metal oxide arrester (MOA) is exceeded. Then, the current commutates into the absorber path (cyan) and the voltage across the CB (magenta curve) rises rapidly. The fault current (blue) starts to decrease when the voltage across the CB is larger than the system voltage after about $30\,\mathrm{ms}$. The PSCAD built-in MOA is used for the energy dissipation in the absorber path. The non-linear V-I characteristic curve for dc applications is taken from [7]. The reference voltage is chosen in order to have a leakage current of $1\,\mathrm{mA}$ under continuous operation voltage. The residual current disconnector "RD" as shown in Fig. 3 is opened after current zero at around $43\,\mathrm{ms}$.

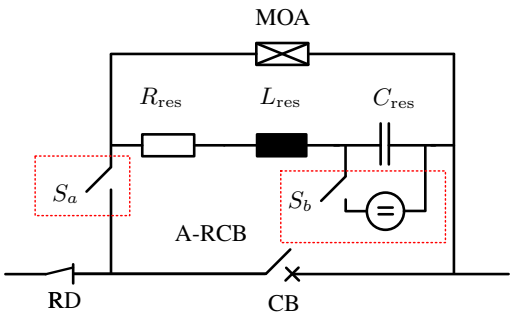

Fig. 3. P-RCB and A-RCB model with additional components in red boxes

The current interruption process in the active scheme (A-RCB) [23], [25] is shown in Fig. 5. A CB opening delay of $4\,\mathrm{ms}$ is again assumed, but can possibly be reduced, if a vacuum CB with special electromagnetic drive was used

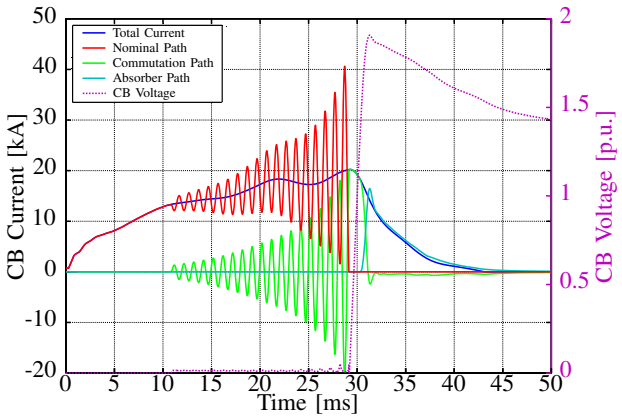

Fig. 4. Fault Current Interruption in P-RCB

[26]. Through closing of "S_a" after contact separation, the pre-charged capacitor C_{res} injects a negative current (green curve in Fig. 5) into the nominal path (red), which forces the arc current to zero. This considerably reduces the time to the first current zero crossing as compared to the passive scheme. It requires, however, an additional charging unit with a dc source. It is assumed that the CB's required voltage withstand capability is reached within the rise time of the capacitor voltage of $2\,\mathrm{ms}$.

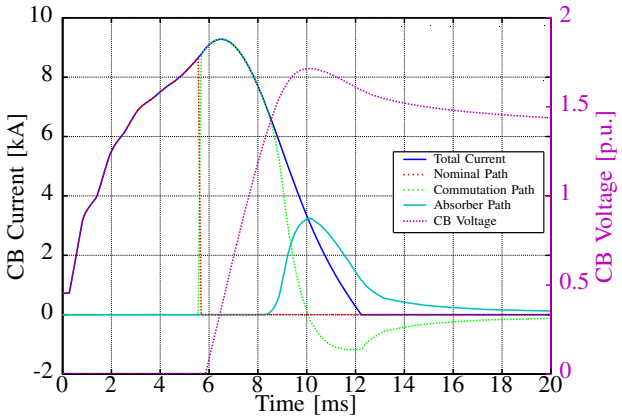

Fig. 5. Fault Current Interruption in A-RCB

1) Arc Modeling: In contrast to the A-RCB with active current injection, the passive concept requires a negative V-I characteristic of the arc conductance to achieve an unstable, growing oscillation in the resonance circuit. Therefore, an accurate modeling of the arc burning and extinction process is needed.

Black-box arc models are widely used to simulate the dynamic arc behavior due to their computational efficiency. Their accuracy, however, depends on the exact description of the arc parameter functions. The determination of these functions is difficult and they are usually only valid under specific conditions [27]. Nevertheless, the dynamic arc behavior in P-RCB can successfully be predicted as presented in [22], [27].

The entire process of arc elongation during contact opening, dynamic behavior during cooling, and arc behavior near current zero cannot be described by a single black-box arc model. Therefore, an approximation of two submodels is chosen for

the study at hand. One model for the arc elongation until nozzle opening assuming clogged gas flow and one model for the dynamic behavior under forced cooling in the high-current and low-current range near current zero.

Arc elongation: During the arc elongation period, the arc resistance r_{arc} exhibits a positive V-I characteristic:

$$r_{\mathrm{arc}}(t) = \frac{E_{\mathrm{arc}} \cdot l_{\mathrm{arc}}/T_{\mathrm{nozzle}}}{i_{\mathrm{arc}}} \cdot t \quad , \tag{1}$$

where l_{arc} is the arc length at nozzle opening, E_{arc} the arc voltage gradient, i_{arc} the instantaneous arc current, and T_{nozzle} the required time for nozzle opening.

Arc dynamics: After opening of the nozzle, the gas flow increases and the arc characteristic is dominated by the heating and cooling dynamics modeled as black-box model.

The majority of the available black-box models are modifications of Mayr's [28] and Cassie's equation [29] that are based on the energy balance equation, which describes the change in the arc column's energy content resulting from the imbalance between ohmic heating and forced cooling.

Mayr's equation originally assumed constant arc cooling power P and arc time constant τ. A modification of it can be found in [30]:

$$\dot{g} = \frac{g}{\tau(g)} \left(\frac{u \cdot i}{P(g)} - 1 \right) \tag{2}$$

with the arc parameters $P(g)$ and $\tau(g)$ depending on the arc conductance g. These two arc parameters are described by power functions

$$P(g) = \quad P_0 \cdot g^{\alpha} \tag{3}$$

$$\tau(g) = \quad \tau_0 \cdot g^{\beta} \quad . \tag{4}$$

The constant cooling power factor P_0 depends linearly on the blow pressure p resulting in $P(g) = p \cdot P_0 \cdot g^{\alpha}$ [24], [27].

To implement the dynamic arc model into PSCAD, equation (2) has to be transformed into integral form:

$$g = \int_0^t \frac{1}{\tau(g)} \left(\frac{i^2}{P(g)} - g \right) dt' \quad . \tag{5}$$

B. HCB

There are numerous different hybrid HVDC CB arrangements [31], [32]. The description and modeling of all of them is beyond the scope of this study and one representative concept similar to [33] as illustrated in Fig. 6 is chosen.

To reduce the losses during normal operation, the nominal path consists only of a few IGBTs and a fast mechanical disconnector in series. Series connected IGBTs with full voltage withstand capability are installed in the commutation path and a MOA in the absorber path. For zero voltage switching and loss reduction, all IGBTs are protected by RCD snubber circuits consisting of a snubber capacitor C_{s}, a resistor R_{s}, and a diode. Note that Fig. 6 shows only the IGBTs for the positive current direction. For reverse blocking ability of the HCB, the same number of IGBTs with opposite polarity has to be installed in series.

After receiving the trip signal from the protection at around $1.6\,\mathrm{ms}$ the IGBTs in the nominal path are blocked and the disconnector "D" is opened. The current commutates into the snubber circuit and into the commutation path (green curve) about $10\,\mu\mathrm{s}$ later as illustrated in Fig. 7. The current in the nominal path (red curve) is reduced to zero immediately. After full opening of the mechanical disconnector, the IGBTs in the commutation path are blocked at around $4.6\,\mathrm{ms}$ and the current commutates in their snubber circuits. In contrast to the SCB, the HCB cannot interrupt the current immediately after commutation, but has to wait until the disconnector "D" has fully established its dielectric strength to be able to withstand the TRV. This delay is named commutation delay and is assumed to be $3\,\mathrm{ms}$. Afterwards, the TRV rises rapidly and the current commutates into the absorber path (cyan curve), where the remaining energy is dissipated. Again, the fault current starts to decrease as soon as the voltage across the CB (magenta curve) exceeds the system voltage (yellow curve).

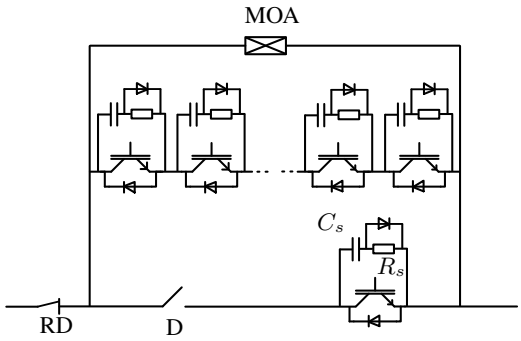

Fig. 6. HCB Model

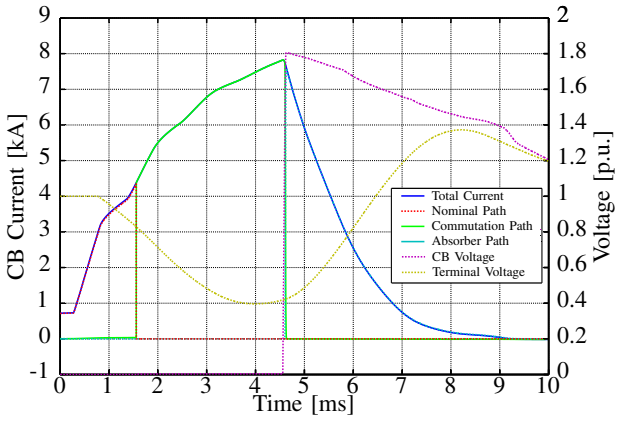

Fig. 7. Fault Current Interruption in HCB

C. SCB

The SCB configuration as illustrated in Fig. 8 has been chosen among different possible concepts [32]–[35]. This SCB has RCD snubber circuits parallel to each IGBT as explained in Section III-B and the MOA parallel to the nominal path.

The current interruption process of the SCB is illustrated in Fig. 9. At around $1.6\,\mathrm{ms}$, the IGBTs are blocked and the current commutates into the snubber circuits (green curve).

Meanwhile, the voltage across the CB (magenta dashed curve) rises and the current commutates finally into the absorber path (cyan curve) at around $2.5\,\mathrm{ms}$.

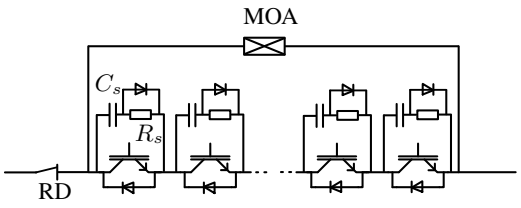

Fig. 8. SCB Model

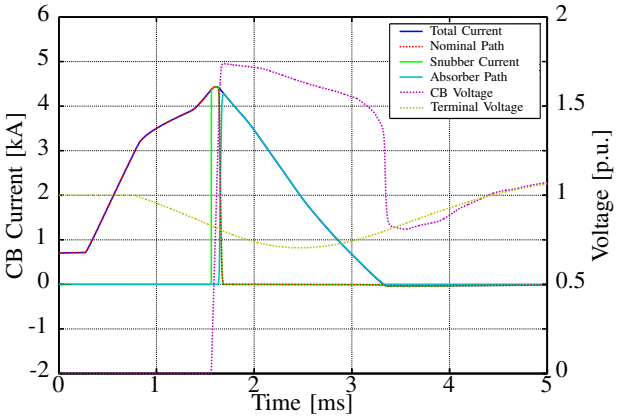

Fig. 9. Fault Current Interruption in SCB

IV. Results and Discussion

The simulations are performed in PSCAD using a time step of $1\,\mu\mathrm{s}$. Results for the CB concept comparison in the base case and parameter variations are presented and discussed in the following paragraphs.

A. Parameters

1) Base Case System Parameters: The default system parameters for the interaction study are summarized in Table I. In the base case, a line reactor of $100\,\mathrm{mH}$ is installed between cable end and CB (cf. Fig. 2) to limit the $\mathrm{d}i/\mathrm{d}t$ of the fault current [36]. The short-circuit power ratio (SCR) is defined as the ratio of the short-circuit capacity at the point of common coupling (PCC) and the rated power of the converter.

2) Base Case CB Parameters: The parameters for all CB types are given in Table II.

A snubber capacitor of $85\,\mu\mathrm{F}$ per IGBT is chosen to limit the rate of rise of the voltage to $300\,\mathrm{V}/\mu\mathrm{s}$ [36].

B. Comparison of CB Concepts in the Base Case

The different HVDC CB concepts presented in Section III are compared in terms of interruption time, maximum CB fault current, and maximum and minimum voltages at the terminals during the fault current interruption process.

The interruption time is defined as the time from fault detection at the CB to current zero (CZ) in the faulted line, i.e. when the CB's total current i_{total} becomes zero. In contrast to the breaking time that considers only the time until current zero in the nominal path, the interruption time takes also the energy dissipation process into account. Another performance indicator is the time, when the $\mathrm{d}i/\mathrm{d}t$ of the total current becomes negative for the first time. Table III presents the comparison of the different CB concepts in terms of time to CZ and time to negative $\mathrm{d}i/\mathrm{d}t$ in the base case. Table III summarizes also the corresponding maximum fault currents through CB1 and CB2 at the ends of the faulted cable for the different CB concepts. As expected, the SCB has the lowest interruption time below $5\,\mathrm{ms}$ and, therefore, also the lowest maximum CB current of about $5\,\mathrm{kA}$, whereas the P-RCB concept reveals the highest interruption time of up to $94\,\mathrm{ms}$ and $27\,\mathrm{kA}$ maximum current in CB1. The P-RCB concept

TABLE I
Base Case System Parameters

Parameter	Value
Rated Converter Power (per pole)	$450\,\mathrm{MW}$
DC Voltage	$\pm 320\,\mathrm{kV}$
AC Voltage (L-L, RMS)	$400\,\mathrm{kV}$
AC Frequency	$50\,\mathrm{Hz}$
SCR of AC Network	20
X/R of AC Network	10
Transformer Leakage Reactance	$0.1\,\mathrm{p.u.}$
Transformer Turns Ratio	216/400
Converter Phase Reactor	$0.05\,\mathrm{p.u.}$
DC Capacitor	$50\,\mu\mathrm{F}$
Line Reactor	$100\,\mathrm{mH}$
Fault Resistance	$2\,\Omega$
Converter Trip Threshold	$2.8\,\mathrm{kA}$
CB Trip Threshold	$2\,\mathrm{kA}$
$\Delta T_{\mathrm{detect}}$	$1\,\mathrm{ms}$

TABLE II
CB Parameters

Parameter	Value	Ref.
A/P-RCB:		
Main CB:		
$\Delta T_{\mathrm{opening}}$	$4\,\mathrm{ms}$	[37]
$\Delta T_{\mathrm{nozzle}}$ (P-RCB)	$5\,\mathrm{ms}$	[37]
Arc Model (P-RCB):		
Arc Voltage Gradient, E_{arc}	$1.4\,\mathrm{kV/m}$	[38]
Arc Length, l_{arc}	$5\,\mathrm{cm}$	
P_0	$393\,\mathrm{kW}$	[27]
a	0.25	[27]
τ_0	$15\,\mu\mathrm{s}$	[27]
b	0.5	[27]
Blow Pressure	$70\,\mathrm{bar}$	
Commutation Path:		
C_{res}	$50\,\mu\mathrm{F}$	
L_{res}	$500\,\mu\mathrm{H}$	
R_{res}	$0\,\Omega$	
Pre-charge voltage (A-RCB)	$40\,\mathrm{kV}$	
HCB:		
Commutation Delay	$3\,\mathrm{ms}$	[33]
IGBT forward voltage (@$1\,\mathrm{kA}$,$125\,^\circ\mathrm{C}$)	$2.6\,\mathrm{V}$	[39]
# of IGBTs in Commutation Path	192	
R_{s}	$70\,\Omega$	
C_{s}	$85\,\mu\mathrm{F}$	[36]
SCB:		
IGBT forward voltage (@$1\,\mathrm{kA}$,$125\,^\circ\mathrm{C}$)	$2.6\,\mathrm{V}$	[39]
# of IGBTs in Nominal Path	192	
R_{s}	$70\,\Omega$	
C_{s}	$85\,\mu\mathrm{F}$	[36]

TABLE III
INTERRUPTION TIME AND MAXIMUM CB CURRENT IN BASE CASE

CB Type	Time to CZ [ms]		Time to di/dt < 0 [ms]		Max I_{CB} [kA]	
	CB1	CB2	CB1	CB2	CB1	CB2
SCB	3.3	4.0	1.6	2.5	4.4	5.1
HCB	9.2	9.0	4.6	5.6	7.8	6.0
A-RCB	12.2	13.6	6.5	7.0	9.3	6.4
P-RCB	94.2	27.9	73.2	21.1	26.5	10.4

exhibits also the highest difference between CB1 and CB2 in terms of interruption time and maximum fault current. It takes more than three times longer to interrupt the current in CB1 than in CB2. Fast CBs with interruption times below 10 ms act within the capacitor dominated period of the transient fault current [5] and the loading of the CBs is almost equal given the same dc capacitor size at both terminals. Slow acting-CBs, such as the P-RCB, however, interrupt the current in the later ac infeed dominated period, during which the fault location is decisive. CB1 is located closer to the fault as compared to CB2 and has more feeders at the adjacent busbar, through which the terminals 3 and 4 feed the ground fault (cf. Fig. 1).

The fact that CB2 opens earlier than CB1 even worsens CB1's situation due to re-routing of the fault currents in the network as depicted in Fig. 10 for a system with P-RCBs. After CB2 has interrupted the fault current at around 28 ms (green curve), line currents i_{32} (cyan curve) and i_{43} (yellow curve) change their direction and all four terminals feed the fault current in CB1. This results in a higher current load in CB1 (blue solid curve) as compared to the case if CB2 would not open at all (blue dashed curve) and the interruption time increased by about 142%. In this simulation, due to the slow reaction of the P-RCB, the current through all converters exceeds the threshold value and all converters are blocked. Thus, even after the fault is cleared by CB1 and CB2, the current through all lines is zero (see also explanation in Section II-B).

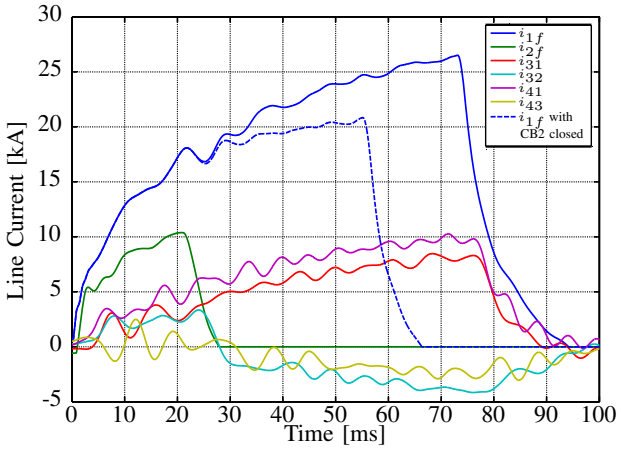

Fig. 10. Line currents in MTDC network with slow P-RCB

The corresponding terminal voltages of all four terminals are illustrated in Fig. 11 for the P-RCB. After fault inception at 0 ms, the voltages at all four terminals drop to about 0.4 p.u. within 10 ms in the network with P-RCBs. In contrast, the terminal voltages decrease only to about 0.7 p.u. using SCBs as shown in Fig. 12.

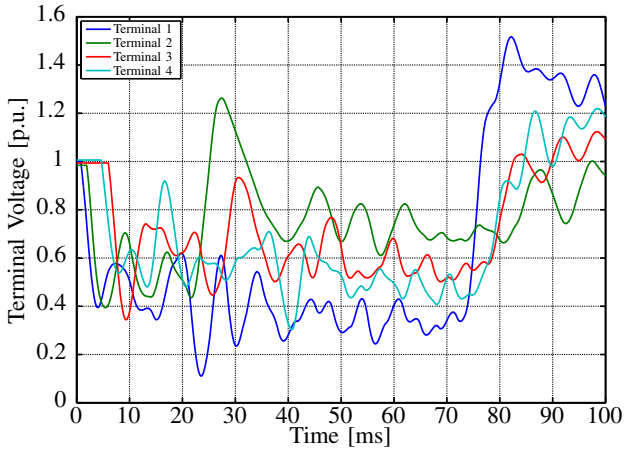

Fig. 11. Terminal voltages in MTDC network with slow P-RCB

The SCB reveals better performance in terms of minimum terminal voltages, because the fault is cleared before the terminal voltages reach their lowest possible level as in the slow-acting P-RCB. The lower limit of the terminal voltage depends on the line reactor and dc capacitor size as will be explained in Sections IV-C and IV-D. It also depends on the fault resistance and the distance to the fault as described in [5].

The P-RCB exhibits not only lower minimum voltages, but also higher overvoltages after fault clearing compared to the SCB as can be seen in Fig. 11. After the current is interrupted in CB2 at 28 ms, the voltage at terminal 2 (green curve) rises to about 1.3 p.u. and the voltage at terminal 1 decreases even further to about 0.1 p.u.. The voltage at terminal 1 later increases to 1.5 p.u. after fault clearance in CB1. The higher overvoltages using P-RCBs are due to the higher currents in the MOAs and, consequently, increased TRV and terminal voltages as compared to the SCB case.

A comparison of maximum and minimum terminal voltages for all CB concepts is illustrated in Fig. 12. A trend towards lower minimum voltages at all terminals can be seen for an increasing interruption time, whereas the maximum overvoltages do not show a clear trend. Due to the high time difference between current interruption at CB1 and CB2 in the P-RCB, the maximum overvoltages differ considerably among the terminals, e.g. 1.1 p.u. at terminal 3 and 1.5 p.u. at terminal 1. In general, the remote terminals 3 and 4 are less affected than the terminals 1 and 2 closest to the ground fault.

The insulation demands for the IGBTs in the SCB and HCB can be drastically reduced, if the MOAs are installed in a freewheeling path [34] instead of arrester stacks parallel to the main switch.

C. Influence of Line Reactor

Figure 13 shows the influence of the line reactor size on the maximum CB current and the maximum terminal and CB voltages in a network with SCBs. A small 10 μF dc capacitor is applied in all the variations to amplify the effect of the line

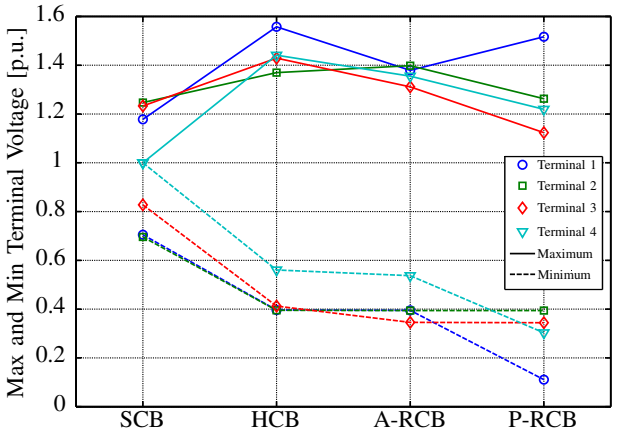

Fig. 12. Maximum and Minimum Terminal Voltages in the Base Case

reactor on the CB performance. A larger line reactor reduces the maximum current in CB1 (blue curve) and CB2 (red curve) as expected. A 200 mH reactor results in a maximum current of around 4 kA, whereas CB1 has to interrupt a fault current of 15 kA in case of a small 1 mH reactor in series. A larger line reactor is beneficial in terms of maximum fault current, but it increases substantially the maximum terminal voltage (magenta curve) from 1.1 p.u. at 1 mH to 1.7 p.u. at 150 mH. The voltage across the CBs (cyan curve), however, is only marginally influenced by the reactor size and remains within 1.7 and 1.8 p.u.. The reactor size has no impact on the minimum terminal voltage, which stays at around 0.3 p.u. (not shown in Fig. 13). The increase in the terminal voltage due to an increase in reactor size is maximum between 0 and 50 mH. Above this value, the line reactor size has much less influence on the terminal overvoltage.

In general, large line reactors should be avoided, because they deteriorate the control performance due to the increased system time constant. Also the volume and mass of the converter station increases with increasing reactor size, which is critical in offshore applications [40].

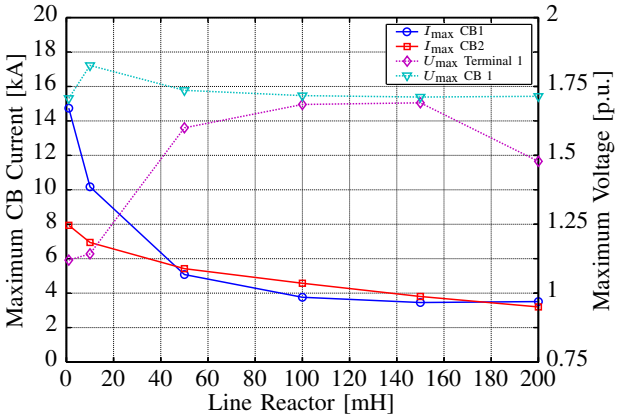

Fig. 13. Influence of line reactor size on SCB performance (C_{cap} = 10 μF)

D. Influence of DC Capacitor

In contrast to the line reactor, an increasing dc capacitor size results in an increasing maximum CB current as illustrated in Fig. 14. The line reactor is kept constant at 10 mH for all capacitor values. A large dc capacitor might seem a disadvantage at first glance, since the maximum current in CB1 (blue curve) increases from 10 kA in case of a small dc capacitor of 1 μF to about 15 kA with a large 200 μF capacitor. The voltage stability is, however, considerably improved with a larger dc capacitor due to its voltage supporting function. The minimum terminal voltage (green curve) is increased from 0 to 0.8 p.u. and the overvoltage at terminal 1 (magenta curve) is completely suppressed with capacitors larger than 100 μF. The CB voltage (cyan curve) is again only marginal affected by the dc capacitor size and remains between 1.8 and 1.9 p.u..

A further disadvantage of large dc capacitors is the increased the system inertia and converter station footprint.

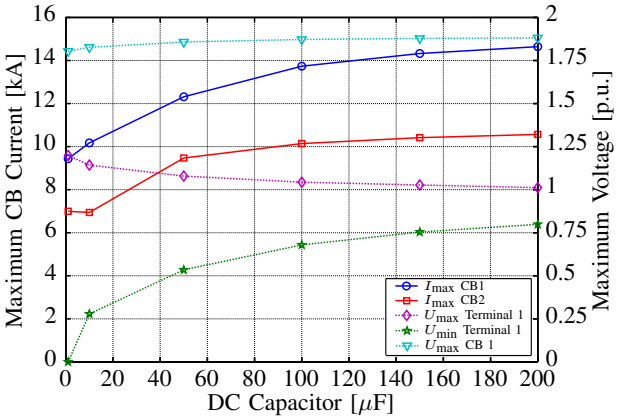

Fig. 14. Influence of dc capacitor size on SCB performance (L_{line} = 10 mH)

E. Influence of Commutation Delay

In contrast to the SCB, most HCB concepts allow for proactive switching [15], [33], [35], i.e. after local detection of an overcurrent, the current can be commutated temporarily into the commutation path without interruption, while the selective protection is deciding, which CBs have to interrupt. With proactive control, the performance of the HCB can be improved and the time delay of the mechanical disconnector can be partly compensated. Fig. 15 compares the required time to CZ and the time to $\mathrm{d}i/\mathrm{d}t < 0$ in a SCB and a HCB for different protection delays between 1 and 6 ms. The base case parameters as summarized in Section IV-A2 are used in these simulations. For protection delays below 4 ms, the HCB (blue line) requires 9.2 ms independently of the protection delay, while the interruption time in the SCB (red line) increases with increasing protection delay. The HCB achieves the same interruption times as the SCB only for long protection delays of more than 4 ms, but the gap between the two concepts is significantly reduced even for short protection delays. For a protection delay of 1 ms, the interruption in the HCB is about 2.8 times the interruption time in the SCB, whereas for a delay of 3 ms, the HCB is only about 50% slower than the SCB with respect to time to CZ. The time to negative $\mathrm{d}i/\mathrm{d}t$ shows an even smaller gap of 28%. The HCB exhibits, however, much lower steady-state losses than the SCB and does not require constant cooling of the IGBTs. The losses in a SCB amount to about 499 kW using 192 IGBTs [39].

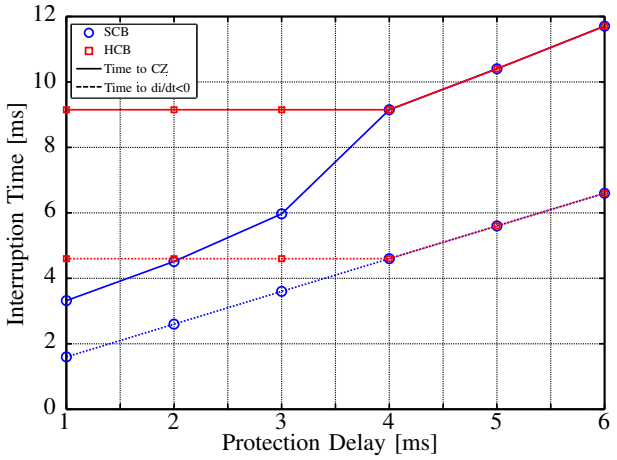

Fig. 15. Influence of protection delay on interruption time in CB1

V. Conclusions

In this paper, four different HVDC CB concepts are implemented into PSCAD. A comparison of the CBŠs performance is made with respect to interruption time, maximum CB current, maximum and minimum terminal voltages, and maximum voltage across the CB.

This study has demonstrated the complex interaction between CB and network components and revealed the trade-off between CB requirement specification and network parameters. The choice of the CB results in a mutual optimization of line reactor size and CB technology. Therefore, also slower CB concepts with high current interruption capability and/or along with large reactors can be of interest.

CB concepts, in which the interruption time depends on the current amplitude (e.g. the passive resonance concept), are unsuitable, as the interruption current of the second breaker to clear could be excessively high.

Due to the high rate of rise of the fault current in a MTDC network, the fault has to be cleared by the CBs as fast as possible. As expected, the fast CB concepts, such as SCB and HCB, perform better than the slower P-RCB and A-RCB. They yield lower interruption times below $10\,\mathrm{ms}$ and, consequently, lower maximum CB currents and voltages. Also the terminals experience less overvoltages and higher minimum terminal voltages.

The performance of the CB depends not only on the CB concept, but also on the network parameters, such as the line inductor, dc capacitor, and protection scheme. A larger inductor results in lower CB currents, but much higher maximum terminal voltages. Again, this implies that the interruption time is the most important CB requirement. A larger dc capacitor, in turn, improves dc voltage stability, i.e. mitigates overvoltages at the terminals and decreases considerably the voltage drops, but increases slightly the maximum CB current.

The detection delay of the network protection impacts mainly the fast CB concepts with short interruption times. In general, the HCB performs worse than the SCB, but the gap between the two concepts becomes smaller with increasing detection delay, if proactive switching control in the HCB is used. In systems with protection schemes, which not only rely on local measurements, e.g. differential protection, CB concepts with proactive switching become more attractive, since their interruption time does not increase proportionally. The choice between SCB and HCB is thus very much influenced by the chosen protection strategy and vice versa.

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